Diagnosis of Power Switches with Power-Distribution-Network Consideration

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***Abstract*—This paper examines diagnosis of power switches when the power-distribution-network (PDN) is considered as a high resolution distributed electrical model. The analysis shows that for a diagnosis method to perform high diagnosis accuracy and resolution, the distributed nature of PDN should not be simplified by a lumped model. For this reason, a PDN-aware diagnosis method for power switches fault grading is proposed. The proposed method utilizes a novel signature generation design-for-testability (DFT) unit, the signatures of which are processed by a novel diagnosis algorithm that grades the magnitude of faults. Through simulations of physical layout SPICE models, we explore the trade-offs of the proposed method between diagnosis accuracy and diagnosis resolution against area overhead and we show that 100% diagnosis accuracy and up to 98% diagnosis resolution can be achieved with negligible cost.**

***Index Terms*—power gating, diagnosis, fault grading**

I. Introduction

Power gating is a low power design technique that assures energy efficiency of sub-100-nm CMOS technologies [14] by switching-off logic blocks to reduce leakage power during periods of inactivity. It is implemented by utilizing header power switches on the supply voltage or footer power switches on the ground of the power-gated block in either *fine-grain* or *coarse-grain* design styles. A *fine-grain* style incorporates a switch within each logic cell. At the *coarse-grain* style, each switch is responsible for a logic block. The latter is more popular and the focus of this work, since it requires less silicon, is more robust against process variations, is applicable on hard blocks and is compatible with existing physical libraries [4]. Due to their critical role, power switches subordinate performance may undermine the low power benefits and the correct functionality of the power-gated blocks [9].

Design-for-testability (DFT) is a design technique for identifying physical defects at Integrated Circuits (ICs) during their lifetime from the manufacturing to the field. It consists of *fault models* that abstract the behaviour of physical defects and *DFT logic* that provides the engineering means to apply the tests and collect the results. During manufacturing testing, which is a crucial step for any fabrication process to avoid shipping defective devices to customers [2], the test result is usually a pass/fail response. However, in most manufacturing practices [13], the test result is accompanied by additional information, which is usually a sequence of bits, called *signature*. With the appropriate processing, known as *test diagnosis* [17], signatures reveal information related to defect properties, such as their magnitude and location. Perhaps the most important role of a diagnosis method, is fault grading, which is a quantification of defect magnitude. Fault grading is critical for tracing the root cause of a test failure and is useful for improving both the manufacturing testing process and the manufacturability of the fabrication process [2], [15], [17]. The fault grading quality is evaluated by *diagnosis accuracy*, a metric that quantifies the likelihood of diagnosis result to be correct and by *diagnosis resolution*, a metric that quantifies the amount of information revealed by the diagnosis result [3].

Testing power switches against stuck-open faults is crucial for assuring that the power-gated domain will not suffer from small delays due to power-grid IR-drop. There are several DFT solutions to test power switches against stuck-opens [5], [6], [8], [10], [11], [16], [18], [19]. However, it was shown in [16] that they suffer from test quality loss, because they rely on a lumped model for the power-distribution-network (PDN) without considering its distributed nature. A PDN-aware manufacturing testing method was proposed in [16]. However, that method provides only a pass/fail test response and not any signature information related to the defect magnitude that caused the failure. Therefore, it can not be used for fault grading diagnosis of the failing dies.

In this paper, we propose a novel PDN-aware fault grading diagnosis method for power switches. Section II reviews the state-of-the-art PDN-aware manufacturing testing method [16] and highlights its limited diagnostic capabilities. Section III analyses the diagnosis quality loss of a PDN-unaware diagnosis method [10], when it performs in a distributed PDN environment and shows that they can reach up to 67% on accuracy loss and up to 63% on resolution loss. For this reason, Section IV presents a diagnosis method that accounts for a distributed PDN model. The proposed PDN-aware diagnosis method is equipped with a novel signature generation logic, the signatures of which are processed by a novel diagnosis algorithm for fault grading. In Section V, we explore the trade-offs of the proposed method between accuracy and resolution against area overhead, through simulations of physical layout SPICE models, and we show that 100% accuracy and up to 98% resolution can be achieved with negligible area overhead.

II. Motivation

Power switches testing for stuck-open faults is performed by clustering the power switches in m segments-under-test (SUTs) of segment-size L power switches [6], [16]. Figure 1 presents the state-of-the-art DFT architecture [16] for

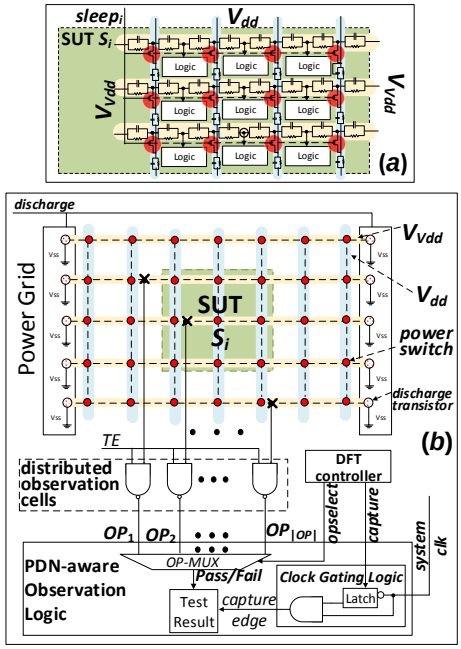


Fig. 1. (a) Distributed PDN model; (b) DFT considering PDN [16]

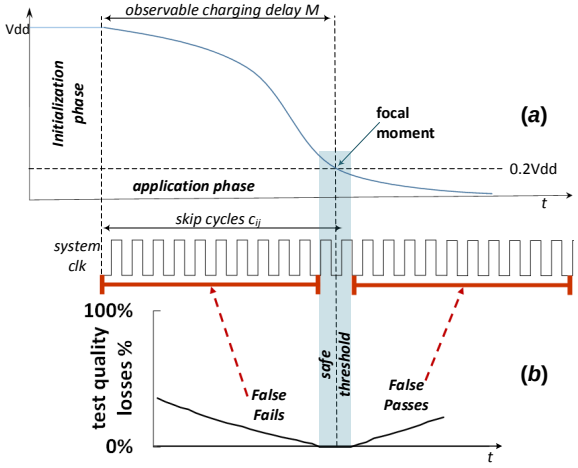


Fig. 2. (a) test process for stuck-opens; (b) test generation considering PDN

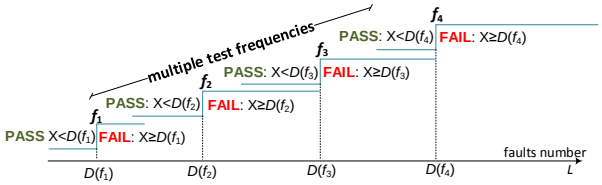


Fig. 3. Diagnosis method without considering PDN [10]

delay-based testing against stuck-open faults on header power switches that considers a distributed PDN model (Figure 1(a)). The test process (Figure 2(a)) starts with the initialization phase, during which the control logic fully discharges the V_{Vdd} power network by using the discharge transistors [11]. During application phase, a single SUT S_i is waken-up by deasserting the $sleep_i$ signal (Figure 1(a)). Upon capture moment, a NAND observation gate is selected, by properly setting the *opselect* signal, to capture its output at a "Test Result" memory cell. The captured value indicates if the V_{Vdd} power network is sufficiently charged at the capture moment. That moment, denoted as *focal moment*, is when the transient voltage at the NAND gate reaches logic-0 value under the fault-free scenario. For analog-to-digital conversion, the voltage level of $\leq 0.2V_{Vdd}$ used as logic-0, and voltage $\geq 0.8V_{Vdd}$ as logic-1. When considering process with $\pm 3\sigma$ variation, logic threshold voltage of a gate is within 20%-80% of V_{dd} [20]. The time elapsed from the start of the application phase to focal moment is the *observable charging delay M*.

It was shown in [16] that when a distributed PDN model (Figure 1(a)) is considered, the *observable charging delay M* exhibits deviations based on the relative position between the activated SUT and the observation point. These deviations negatevily affect test quality with fault coverage loss or yield loss. To avoid this loss, [16] proposes distributed observation points and a variable capture moment selection mechanism based on clock-gating of the system-clock, both shown in Figure 1(b). During test generation, highlighted in Figure 2(b), the rising edges of the system clock are evaluated for their test quality performance according to their deviation from the *focal moment* (Figure 1(a)). Those clock edges before the focal moment are susceptible to false fails and those that follow it to false passes. A safe threshold on the maximum acceptable deviation is used, as a criterion to select clock edges that do not exhibit any test quality loss. Finally, each test is a triplet of SUT S_i, observation point OP_j and skip cycles c_{ij}. In conclusion, although this manufacturing testing method considers a distributed PDN model, its diagnostic capabilities are limited since it only provides a pass/fail response.

It should be noted that [10] proposes a power switches diagnosis method (Figure 3). This method uses multiple test results from various test frequencies $f_1 > f_2 > \ldots > f_n$. If the test of test frequency f_i passes (fails), then the defect magnitude X is diagnosed smaller (larger or equal) than the defect magnitude $D(f_i)$ related with frequency f_i. This method assumes that faulty scenarios with same amount of faults F have the same impact on the observable charging delay. However, in the next section we show that in a distributed PDN test environment, this assumption does not hold. There, the charging delay of faulty scenarios exhibits deviations that affect the diagnosis accuracy and resolution results of this method.

III. PDN-aware Fault Expression Analysis

In this section we show that the observable charging delay of faulty scenarios exhibit deviations, based on faulty switches location, when a distributed PDN is consider. Then, we show how these deviations affect the diagnosis quality of a diagnosis method [10] that is based on a lumped-PDN model.

We analysed various benchmarks from the IWLS'05 benchmark suite [1]. The results of this section are based on the *ethernet*, which is the largest among them. To generate the power grid RC distributed model, we synthesized the circuits using a 90nm library and operational voltage of V_{dd}=1.2V

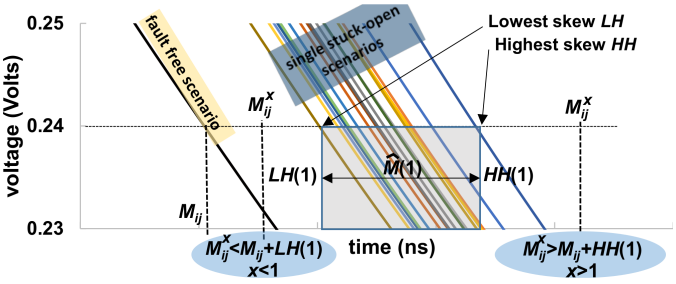


Fig. 4. Fault expression range $\widehat{M}(F)$ with a distributed PDN model

using the grid power gating style [4], [12]. We constraint IR-drop during physical synthesis to be $\leq$5% using 2048 header switches. Then, we followed the method shown in [16] to generate a distributed power grid SPICE model (Table II) and design the DFT logic.

A. Fault expression deviations at a distributed PDN model

Using the distributed model, we examine the impact of faulty scenarios on the observable charging delay by fault injecting F number of stuck-open faults. The result for F=1 is shown in Figure 4 and corresponds to the segmentation setup of $L \times m = 128 \times 16$ of the *ethernet*. The graph lines show the transient voltage from a single NAND observation point. The isolated darker shaded line at the left of the graph shows the behaviour during the fault-free scenario, while the other lines belong to the L single stuck-open faulty scenarios ($F = 1$) for every switch in the SUT. As expected, the faulty scenarios exhibit a higher delay. We denote this additional delay as skew H. It should be pointed out that from this experiment we conclude that the relative location of the considered fault and observation point, affects the observable charging delay. We refer to this relationship as **fault expression location dependency**. Particularly, the faulty scenario with the earliest logic-0 value arrival exhibits the "lowest skew" *LH* and belongs to a faulty scenario where the faulty switch is very far from the observation point. Similarly, the one with the latest arrival exhibits the "highest skew"*HH* and belongs to a faulty scenario where the faulty switch is very close to the observation point. These two values are marked as *LH*(1) and *HH*(1) in Figure 4 to denote that they are related to the single (F=1) stuck-open faulty scenarios. Based on these bounds, we denote as *fault expression range*, the range $\widehat{M}(F)$=[M+*LH*(F), M+*HH*(F)]. Range $\widehat{M}(1)$ for this experiment is shown shaded in Figure 4.

B. Diagnosis without PDN and diagnosis resolution

Figure 5(a) shows the impact of faults magnitude on the observable charging delay, when a lumped PDN model is considered for the DFT of Figure 1(b). The 'x'-axis is the number of stuck-open faulty switches F and the 'y'-axis is the observable charging delay of the faulty scenarios with F number of faults $M(F)$. The lumped PDN model does not consider the position of the faulty switches on the power grid. Therefore, the charging delay $M(F)$ is a single value for each F, no matter which the F faulty switches are. In this environment, the diagnosis method of [10] with three test

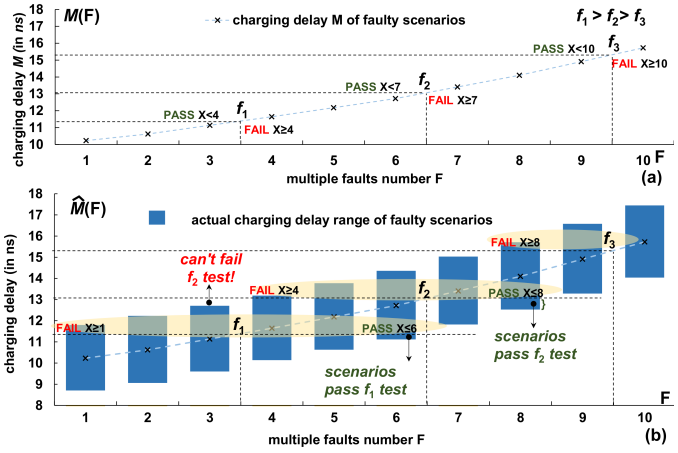


Fig. 5. (a) Fault grading through a lumped PDN model and multiple test clocks. (b) Fault expression deviations with a distributed PDN model

TABLE I
DIAGNOSIS QUALITY EVALUATION ON RESOLUTION AND ACCURACY WHEN POWER NETWORK IS IGNORED

scenarios			expected results			actual results			*Rez*	*Acc*
f_1	f_2	f_3	diagnosis	size	*Rez*	diagnosis	size	*Rez*	Loss	Loss
P	-	-	$1 \leq X \leq 3$	3	80	$1 \leq X \leq 6$	6	50	38%	50%
F	P	-	$4 \leq X \leq 6$	3	80	$1 \leq X \leq 8$	8	30	**63%**	62%
F	F	P	$7 \leq X \leq 9$	3	80	$4 \leq X \leq 10$	7	40	50%	57%
F	F	F	$X = 10$	1	100	$8 \leq X \leq 10$	3	80	20%	**67%**

frequencies f_1, f_2 and f_3, with f_1>f_2>f_3, leads to the results shown in Table I, under column 'expected results'. Each row in Table I corresponds to one, among the possible, diagnosis scenario for three test frequencies f_1, f_2 and f_3 (with 'P' for PASS and 'F' for FAIL, possible scenarios are P−−, FP−, FFP, FFF). Column 'size' contains the diagnosis range size, and column '*Rez*' contains the *diagnosis resolution*:

$$Rez(\text{diagnosis}) = [1 - \frac{(\text{diagnosis range size}) - 1}{E}] \times 100 \quad (1)$$

where E is the maximum expected number of faults. For this analysis, we used E=10. The bigger the diagnosis range size, the lower the resolution. For example, $Rez(X{=}10){=}100\%$, $Rez(6{<}X{\leq}9){=}80\%$ and $Rez(1{\leq}X{\leq}10) = 10\%$.

C. Fault expression chart and diagnosis quality loss

By comparing the expected diagnosis results of [10] (Table I) with results generated through Monte Carlo fault injections, we evaluate the impact of ignoring the distributed PDN nature on diagnosis quality. To do so, for each possible number of faults F in the range $1{\leq}F{\leq}10$, we perform 200 F-fault injections and gather the fault expression ranges $\widehat{M}(F)$. We plot these ranges in the chart shown in Figure 5(b), denoted as *fault expression chart* C_{ij} of SUT S_i through observation point OP_j hereafter. The 'x'-axis shows the injected number of faults F and the 'y'-axis shows the fault expression ranges $\widehat{M}(F)$ for $1{\leq}F{\leq}10$. The diagnosis results (diagnosis, size, Rez) for this diagnosis chart and test frequencies f_1, f_2 and f_3 are contained in column 'actual results' in Table I. The final two columns 'Rez Loss' and 'Acc. Loss.' evaluate the resolution loss and the accuracy

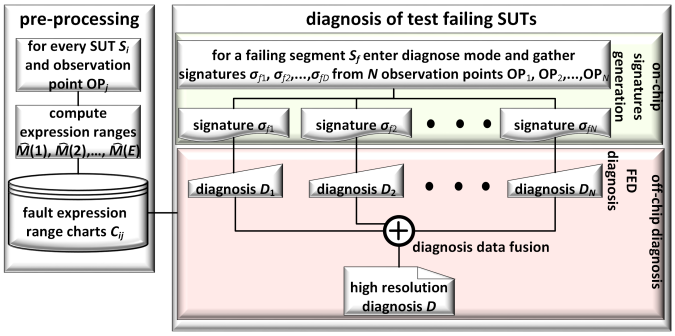


Fig. 6. Flow of the proposed diagnosis method

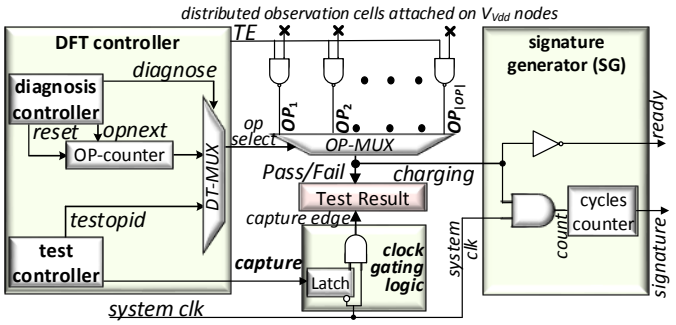


Fig. 7. Proposed DFT architecture

loss of [10] in a distributed PDN environment, computed as (Rez Loss)=(Rez(expected)-Rez(actual))/Rez(expected) and (Acc Loss)=(1−(expected size)/(actual size)). The worst case diagnosis resolution and accuracy loss are evaluated as 63% and 67%, respectively. These data motivate the need for a diagnosis faults grading method that considers the fault expression ranges in order to deliver accurate results.

It should be noted that [10] could be adapted to account for a distributed PDN. However, another limitation of this method is the multiple test frequencies requirement for high diagnosis resolution. In the next section, we present a novel signature generation unit that does not suffer from this limitation. Its signatures are processed by a novel diagnosis method that delivers high resolution with 100% diagnosis accuracy.

IV. PDN-aware Fault Grading Diagnosis

In this section the proposed PDN-aware diagnosis method for fault grading stuck opens of power switches is presented. The flow of the proposed diagnosis method is shown in Figure 6. It consists of two major steps:

Pre-processing: The first is a pre-processing step, performed through fault simulations, to create a fault expression charts C_{ij} database for every pair of SUT S_i and observation point OP_j. Faults expression location dependency, described in Section III-A, speeds-up this process.

Diagnosis of test failing SUTs: The second step consists of two phases. The first phase is the on-chip collection of signatures from the failing SUTs of the test process described in Section II. During this phase, the DFT logic, which will be presented in Section IV-A, gets into 'diagnose' mode. In this mode, it collects measurements of the charging delay M through a signature generator unit. The next phase is the application of the diagnosis algorithm, described in Section IV-B, for post-processing off-chip the collected signatures, according to the fault expression charts computed during the pre-processing phase.

In Section IV-C, an additional step for high resolution diagnosis is presented, the basic idea of which is to perform diagnosis from (N) different observation points. Data of each diagnosis exhibits low resolution, but when they are fused together [7], a higher resolution diagnosis result is obtained.

A. Diagnosis Architecture

The proposed diagnosis architecture is shown in Figure 7. It consists of three major blocks. A **DFT controller** that contains a *test controller* to control the test application process for stuck-open described in Section II and a *diagnosis controller* for setting the DFT into 'diagnose' and 'shift-out' modes. In 'diagnose' mode, the diagnosis controller repeats a test for tests-per-fail N times, with a different observation point selected by the OP-counter at each iteration in order to collect multiple signatures. From these signatures, multiple diagnosis results are obtained and are used to enhance diagnosis resolution. A **shift register** (SR) (not shown in Figure 7) is required for storing the signatures before shifting them out of the circuit, in 'shift-out' controller mode. Finally, the **signature generator (SG)** measures, on-chip, the observable charging delay M_{ij}. It uses a cycles counter (CC) that counts the system clock cycles elapsed, until the observation cell output reaches logic-0 which indicates that the circuit is charged.

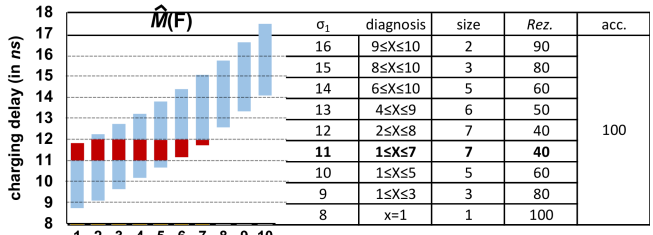
B. Diagnosis with fault expression charts

This paragraph explains how a fault expression chart C_{ij} (Figure 5(b)) can be used for diagnosis. Consider the graph in Figure 4 that shows the $\widehat{M}(1)$ expression range for F=1 stuck-open fault. If the observable charging delay of a scenario with (unknown) X faults M^X is lower than the delay of the least skewed faulty scenario with F=1 faults (M^X<M+$LH(1)$) then the SUT should suffer from X<1 faults. Similarly, if the observable charging delay of a faulty scenario with X number of faults is higher than the most skewed faulty scenario with $F=1$ faults (M^X>M+$HH(1)$), then the SUT should suffer of X>1 faults (note that M denotes the fault-free scenario delay). This is the core of the proposed diagnosis algorithm and will be called *fault-expression-based diagnosis* (FED):

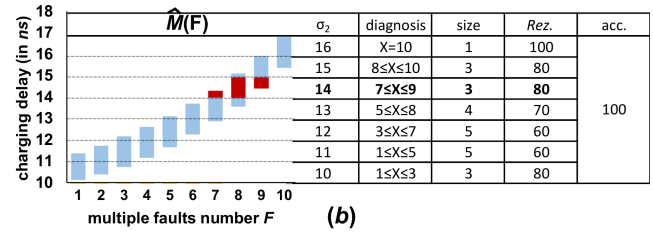
$$X \begin{cases} < F & \text{when } M^X < M + LH(F) \\ > F & \text{when } M^X > M + HH(F) \\ \text{unknown} & \text{otherwise} \end{cases} \qquad \text{(FED)}$$

Given a fault expression chart C_{ij}, FED is applied iteratively on the $\widehat{M}(F)$ ranges contained in the chart. The following example illustrates this process.

Example: In Figure 8(a) we present the fault expression chart for the segmentation setup of L×m=32×64 of the *ethernet*



σ_1	diagnosis	size	Rez.	acc.
16	9≤X≤10	2	90	100
15	8≤X≤10	3	80	
14	6≤X≤10	5	60	
13	4≤X≤9	6	50	
12	2≤X≤8	7	40	
11	**1≤X≤7**	**7**	**40**	
10	1≤X≤5	5	60	
9	1≤X≤3	3	80	
8	x=1	1	100	



σ_2	diagnosis	size	Rez.	acc.
16	X=10	1	100	100
15	8≤X≤10	3	80	
14	**7≤X≤9**	**3**	**80**	
13	5≤X≤8	4	70	
12	3≤X≤7	5	60	
11	1≤X≤5	5	60	
10	1≤X≤3	3	80	

(c)

σ_1 / σ_2	8 X=1	9 1≤X≤3	10 1≤X≤5	**11** **1≤X≤7**	12 2≤X≤8	13 4≤X≤9	14 6≤X≤10	15 8≤X≤10
10 1≤X≤3	X=1 100%	1≤X≤3 80%	1≤X≤3 80%	1≤X≤3 80%	2≤X≤3 90%	NA		
11 1≤X≤5	X=1 100%	1≤X≤3 80%	1≤X≤5 60%	1≤X≤5 60%	2≤X≤5 70%	4≤X≤5 90%	NA	
12 3≤X≤7		X=3 100%	3≤X≤5 80%	3≤X≤7 60%	3≤X≤7 60%	4≤X≤7 70%	6≤X≤7 90%	NA
13 5≤X≤8	NA		X=5 100%	5≤X≤7 80%	5≤X≤8 70%	5≤X≤8 70%	6≤X≤8 80%	X=8 100%
14 **7≤X≤9**		NA		**X=7** **100%**	7≤X≤8 90%	7≤X≤9 80%	7≤X≤9 80%	8≤X≤9 90%
15 8≤X≤10			NA	NA	X=8 100%	8≤X≤9 90%	8≤X≤10 80%	8≤X≤10 80%

Fig. 8. Fault expression charts and diagnosis tables: (a) for observation point OP_1 signatures σ_1; (b) for observation point OP_2 signatures σ_2. (c) Fusion combinations table ($\sigma_1 \times \sigma_2$) for higher accuracy.

circuit. The expression ranges $\widehat{M}(F)$ for F-multiple stuck-open faults in the range $1 \leq F \leq 10$ are shown. The signatures σ_1 are obtained assuming system clock frequency of f=1GHz (period T=1ns). The *diagnosis table* is obtained from this graph. Firstly, note that the SG unit counts the clock cycles elapsed until the circuit is charged. As a result a signature is obtained, which is a quantized estimation of the actual delay and always an integer value. The *diagnosis table* is shown nested in Figure 8. First column shows the possible signature values σ_1 and the second one the diagnosis range of that signature according to the fault expression ranges of the chart. The diagnosis range is obtained by a simple overlap check between the rectangles that correspond to the duration of the signature value (one period T=1ns of the system clock) and the expression ranges. This check is shaded in Figure 8(a) for the signature value σ_1=11 and the diagnosis is found $1 \leq X \leq 7$. Column 'size' contains the diagnosis range size and fourth column the diagnosis resolution Rez. For the examined case Rez. is found in the range [40%, 100%]. ■

C. Diagnosis data fusion to enhance diagnosis resolution

This section presents the fusion [7] of low diagnosis resolution results, gathered from different observation points, into a diagnosis with higher resolution. Consider the expression chart in Figure 8(b). This chart belongs to the same SUT examined in chart Figure 8(a), but in this case the fault expression ranges belong to a different observation point. The diagnosis tables of these charts are merged into the *fusion diagnosis table*, shown in Figure8(c). From fusion table, higher resolution diagnosis results are obtained, because it contains information about all $\sigma_1 \times \sigma_2$ possible combinations. For example, if σ_1=11 and σ_2=14, the fused diagnosis is X=7 with $Rez_{\sigma_1 \times \sigma_2}$ (X=7)=100%, which is larger than both $Rez_{\sigma_1}(1 \leq X \leq 7)$=40% and $Rez_{\sigma_2}(7 \leq X \leq 9)$= 80%.

TABLE II
DISTRIBUTED PDN MODELS SYNTHESIZED WITH A 90NM LIBRARY

model & circ.		ethernet (157.5K ge)	s38417 (30.5K ge)	s38584 (26.9K ge)
R (Ω)	count	240514	60502	56984
	min	1.0E-03	1.0E-03	1.0E-03
	max	7.6E+02	2.9E+02	3.3E+02
C (F)	count	150058	56537	52527
	min	8.5E-23	6.0E-23	8.5E-23
	max	1.8E-14	2.8E-14	4.5E-14

V. SIMULATION RESULTS

In this section we evaluate, through SPICE simulation, the performance of the proposed PDN-aware diagnosis method (Figure 6) on various circuits. We analysed a large number of circuits from the IWLS'05 suite [1] and selected three representatives: the *ethernet* (the largest of the IWLS'05), the *s38417* and the *s38584* circuits (the largest of ISCAS'89 included in IWLS'05 suite). Circuits size, in gate equivalents (ge) and their distributed PDN models are shown in Table II. One ge is the area of a two input NAND gate. The PDN model (V_{dd}, V_{Vdd} and V_{ss}) consist of 'count' number of resistances 'R' and capacitances 'C', with value in the range ['min', 'max']. Next, we explore the trade-offs of the proposed method (Figure 6) on accuracy, resolution and area cost. The operating frequency of the benchmarks is f = 1GHz.

A. Diagnosis accuracy & resolution evaluation results

Table III shows the results of the proposed method. First two columns contain the examined circuit and $L \times m$ segmentation setup. Third column contains the signature size $|\sigma|$ in bits and fourth column shows the achieved diagnosis accuracy. Note that the proposed FED diagnosis, described in Section IV-B, achieves 100% diagnosis accuracy in all examined cases. The columns that follow contain, in pairs, the average resolution for all possible signature values (under column $\overline{Rez}$) and the area overhead (under column 'area') compared to [16]. Maximum expected faults E, of Formula (1), is set to E=10 for the *ethernet* and E=L for the remaining circuits, since they are small and charge rapidly during the fault-free scenario. Each pair belongs to a different tests-per-fail N parameter of the fusion diagnosis method, described in Section IV-C. For N=1 the results belong to the case without applying fusion diagnosis. For *ethernet* and N=1, note that, as the number of segments m increases from m=8 to m=128, the resolution increases from 10% to 85%, because the segment size L decreases. Meanwhile, although the area overhead increases, it remains less than 16.6% additional silicon compared to [16]. Therefore, we conclude that FED diagnosis increases accuracy with minimum area requirement.

The next pairs of columns, in Table III, contain the results for N=2,3 and 4. A tests-per-fail parameter N>1 activates

TABLE III
ACCURACY, RESOLUTION AND AREA COST OF THE PROPOSED METHOD

basic info		$\|\sigma\|$	Acc	**N=1**		N=2		N=3		N=4	
circuit	$L \times m$		%	$\overline{Rez}$	area	$\overline{Rez}$	area	$\overline{Rez}$	area	$\overline{Rez}$	area
ethernet	256×8	3	100	**10**	9.2	22	11.0	30	12.9	**34**	14.8
	128×16	4		23	11.0	38	13.5	46	16.0	49	18.5
	64×32	6		45	14.2	66	17.9	77	21.6	81	25.3
	32×64	6		63	14.8	83	18.5	92	22.2	**96**	**26.0**
	16×128	7		85	16.6	94	21.0	97	25.3	98	29.7
s38417	128×4	3		12	12.1	20	14.8	24	17.4	26	20.0
	64×8	4		70	13.0	78	15.6	80	18.3	81	20.9
	32×16	4		77	15.6	85	19.2	88	22.7	89	26.2
	16×8	4		85	16.5	94	20.0	97	23.6	98	27.1
s38584	128×4	3		19	12.6	32	15.4	39	18.2	41	20.9
	64×8	4		77	13.6	86	16.3	88	19.1	89	21.8
	32×16	4		85	16.3	94	20.0	97	23.7	98	27.4
	16×8	4		95	17.2	97	20.9	98	24.6	98	28.3

fusion diagnosis to increase diagnosis resolution. Particularly, for *ethernet* and L=256, average diagnosis resolution $\overline{Rez}$ increases from 10% to 34%. The low resolution of that case is attributed to the large segment size L, which causes a rapid circuit charge. However, even in that case, fusion diagnosis achieves a $3.4\times$ resolution increase compared to the case of N=1. For a smaller segment size L=32 and N=4, the achieved resolution is 96% with just 26% additional silicon compared to [16]. Therefore, we conclude that fusion diagnosis increases resolution with minimum area cost.

B. Hardware overhead

The area overhead of the proposed DFT (Figure 7) compared to [16] is caused by: the SG unit, the diagnosis controller (with the OP-counter) and the shift register SR. The **SG unit** consist only of a NAND gate, an inverter and the cycles counter CC, which is of $|\sigma|$=$log_2(\lceil max(\sigma) \rceil)$+2 bits size, with $max(\sigma)$ the maximum possible signature value. That value is computed by $max(\sigma)$=$max(M)/T$, with $max(M)$ the highest possible observable charging delay during the fault-free scenarios and T the clock period and so $|\sigma|$=$log_2(\lceil max(M)/T \rceil)$+2. Two additional bits are used to avoid CC counter overflow during faulty scenarios, where the delay can be higher. **Diagnosis controller** consists of a small FSM for the 'diagnose' and 'shift-out' states and the OP-counter of maximum size |OP-counter|=$log_2(m)$, with m the SUTs number. **SR size** is |SR| = $log_2(m)$+$|\sigma|\times N$, with $|\sigma|$ the signature size in bits and N the tests-per-fail parameter of fusion diagnosis. Finally, the highest area overhead of the proposed DFT, among the results in Table III, is less than 29.7% compared to [16], which is very low. Compared to benchmark circuits, that area is $<0.12\%$ *ethernet* area, $<0.44\%$ *s38417* area and $<0.48\%$ s38584 area. Note that the proposed area overhead drops as the size of the circuit increases, clearly showing scalability to large designs.

VI. CONCLUSIONS

We showed that diagnosis of power switches must consider a distributed PDN model to deliver 100% diagnosis accuracy with high resolution. Therefore, we proposed a novel PDN-aware fault grading diagnosis method (Figure 6). The proposed method is equipped with a novel signature generation DFT (Figure 7), the signatures of which are processed by a novel diagnosis algorithm (Section IV-B) for high accuracy fault grading. To enhance diagnosis resolution, fusion of diagnosis data, collected from multiple tests, was proposed (Section IV-C). Through simulations of physical layout SPICE models (Table II), we explored the trade-offs of the proposed method between accuracy and resolution against area cost (Table III) and we showed 100% diagnosis accuracy and 98% diagnosis resolution with negligible area cost.

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