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**UNIVERSITY OF SOUTHAMPTON**

FACULTY OF PHYSICAL AND APPLIED SCIENCES

Electronics and Computer Science

**Confined Nanoscale Chalcogenide Phase  
Change Material and Memory**

by

**Ruomeng Huang**

Thesis for the degree of Doctor of Philosophy

January 2015



UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF PHYSICAL AND APPLIED SCIENCES

Electronics and Computer Science

Doctor of Philosophy

CONFINED NANOSCALE CHALCOGENIDE PHASE CHANGE MATERIAL AND  
MEMORY

by Ruomeng Huang

The miniaturization of memory devices has been one of the major driving forces in the exploration of ever faster, smaller and more efficient memory concepts. Among all the competitors for the next generation of non-volatile memory, phase change materials based random access memory has emerged as a leading candidate. A better understanding of nanoscale properties of phase change materials and the ability of selective depositing them into confined nanostructures are substantially important in the long march towards smaller more densely packed memory bits.

A novel top-down spacer etch technique has been developed for fabricating sub-hundred nanometre phase change  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  nanowires. Taking advantage of this technique which allows precise control over nanowire position and geometries, the contact properties between phase change material and metallic electrode in nanoscale can be quantitatively investigated. The results reveal a specific contact resistance of  $7.56 \times 10^{-5} \Omega \cdot \text{cm}^2$  between TiN and crystalline  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ , and  $6.39 \times 10^{-2} \Omega \cdot \text{cm}^2$  between TiN and amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  under an applied voltage of 2 V. These results suggest the dominant role played by contact resistance in the total resistance of phase change memory device, and highlight the importance of interfacial properties of nanoscale phase change materials.

Novel approaches, electrodeposition and chemical vapour deposition (CVD), are deployed for the selective deposition of phase change materials into confined nanostructures. The research reported here shows, for the first time, the electrodeposition of ternary GeSbTe phase change materials by adopting a non-aqueous electrolyte. This technique offers easy control over the deposited material properties (e.g. composition, morphology) and demonstrates great capability of selective depositing phase change materials into nanoscale holes with smallest size presented in this thesis of around 50 nm. The electrodeposited  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  material is shown to have a promising switching behaviour showing 200 cycles with 3 orders of magnitude resistance change.

The research on chemical vapour deposition of six chalcogenide phase change materials ( $\text{Ga}_2\text{Se}_3$ ,  $\text{Ga}_2\text{Te}_3$ ,  $\text{SnSe}_2$ ,  $\text{TiSe}_2$ ,  $\text{Bi}_2\text{Te}_3$  and  $\text{Sb}_2\text{Te}_3$ ) displays an unusual selective

growth behaviour. All materials, except  $\text{Ga}_2\text{Se}_3$ , have demonstrated to some extent selectivity onto the TiN surface in the lithographically patterned  $\text{SiO}_2/\text{TiN}$  substrates with  $\text{Bi}_2\text{Te}_3$  and  $\text{Sb}_2\text{Te}_3$  exhibiting the best selectivity onto nanostructures. Both substrate surface properties and materials properties are suggested to play a role in this selective deposition behaviour.

## Declaration of Authorship

I, Ruomeng Huang , declare that the thesis entitled *Confined Nanoscale Chalcogenide Phase Change Material and Memory* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
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# List of Publications

## Journal Publications

### Chapter 4

**R. Huang**, K. Sun, K. S. Kiang, R. Chen, Y. Wang, B. Gholipour, D. W. Hewak, C. H. de Groot (2014) **Contact Resistance Measurement of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  Phase Change Materials to TiN Electrode by Spacer Etched Nanowire**, *Semiconductor Science and Technology*, 29(9), 095003.

### Chapter 5 (authors in alphabetical order)

P. N. Bartlett, D. A. Cook, C. H. de Groot, A. L. Hector, **R. Huang**, A. Jolleys, G. P. Kissling, W. Levason, S. J. Pearce, G. Reid (2013) **Non-aqueous Electrodeposition of Metals and Metalloids from Halometallate Salts**, *RSC Advances*, 3(36), 15645-15654.

P. N. Bartlett, S. L. Benjamin, C. H. de Groot, A. L. Hector, **R. Huang**, A. Jolleys, G. P. Kissling, W. Levason, S. J. Pearce, G. Reid, Y. Wang (2014) **Nanostructured  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  by Electrodeposition for Applications in Phase Change Memory**, *Nature Materials*, (Submitted).

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K. George, C. H. de Groot, C. Gurnani, A. L. Hector, **R. Huang**, M. Jura, W. Levason, G. Reid (2013) **Telluroether and Selenoether Complexes as Single Source Reagents for Low Pressure Chemical Vapor Deposition of Crystalline  $\text{Ga}_2\text{Te}_3$  and  $\text{Ga}_2\text{Se}_3$  Thin Films**, *Chemistry of Materials*, 25(9), 18291836.

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S. L. Benjamin, C. H. de Groot, C. Gurnani, A. L. Hector, **R. Huang**, E. Koukharenko, W. Levason, G. Reid (2014) **Chemical Vapour Deposition of Antimony Chalcogenides with Positional and Orientational Control: Precursor Design and Substrate Selectivity**, *J. Mater. Chem. C*, 3(2), 423-430.

#### Not in the thesis

L. Zhong, P. A. Reed, **R. Huang**, C. H. de Groot, L. Jiang (2014) **Resistive Switching of Cu/SiC/Au Memory Devices with a High ON/OFF Ratio**, *Solid State Electronics*, 94, 98-102.

L. Zhong, L. Jiang, **R. Huang**, C. H. de Groot (2014) **Nonpolar Resistive Switching in Cu/SiC/Au Non-volatile Resistive Memory Devices**, *Applied Physics Letter*, 104, 093507.

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K. A. Morgan, **R. Huang**, K. Potter, C. Shaw, W. Redman-White, C. H. de Groot (2014) **Total Dose Hardness of TiN/HfO<sub>x</sub>/TiN Resistive Random Access Memory**, *IEEE Trans. Nuclear Science*, 61(6), 2991-2996.

## Conference Publications

### Chapter 4

**R. Huang**, K. Sun, K. S. Kiang, R. Chen, Y. Wang, B. Gholipour, D. W. Hewak, C. H. de Groot (2014) **Contact Resistance Measurement of Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> Phase Change Materials to TiN Electrode by Spacer Etched Nanowire**, *Materials Research Society Spring Meeting*, San Francisco, California, USA.

**R. Huang**, K. Sun, K. S. Kiang, R. Chen, Y. Wang, B. Gholipour, D. W. Hewak, C. H. de Groot (2013) **A Novel Top-down Fabrication Process for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> Phase**

**Change Material Nanowires**, *13th Non-Volatile Memory Technology Symposium*, Minneapolis, Minnesota, USA.

## Chapter 5

**R. Huang**, P. N. Bartlett, S. L. Benjamin, C. Gurnani, A. L. Hector, A. Jolleys, G. P. Kissling, W. Levason, S. Pearce, G. Reid, C. H. de Groot (2013) **Selective Deposition of Phase Change Materials by Chemical Vapor Deposition and Electrodeposition**, *European\Phase Change and Ovonic Symposium*, Berlin, Germany.

**R. Huang**, P. N. Bartlett, S. L. Benjamin, C. Gurnani, A. L. Hector, A. Jolleys, G. P. Kissling, W. Levason, S. Pearce, G. Reid, C. H. de Groot (2014) **Electrodeposition of Phase Change Random Access Memory**, *European\Phase Change and Ovonic Symposium*, Marseille, France.

## Chapter 6

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*To My Dear Wife,  
Huihui Sun*



# Chapter 1

## Introduction

### 1.1 Non-volatile memory

The performance of memory devices has been the bottleneck for current computing systems as its scaling has been outpaced by performance of processor since the 1980's. The invention of massively parallel computing with multicore processors in recent years has further widened this gap and burdened the already strained memory system. The development of denser, faster and less energy-consuming non-volatile memory (NVM) hence becomes critical to the innovations in modern information technology. Charge-based flash memory has been introduced to mitigate the gap, yet it offers little relief to the performance bottleneck as it suffers from a long programming time, limited number of write/erase cycles and performance degradation as the scaling limit is approached. The development of non-charge-based memory is therefore essential for extending Moore's law over the few next decades.

A number of novel information storage concepts for NVM are proposed with the aim to go beyond the limitations of conventional random access memory (RAM) and Flash memory. Notable examples include storing data in the direction of magnetic orientation (magnetic RAM-MRAM) [1], in the electric polarization of a ferroelectric material (ferroelectric RAM-FRAM) [2], in the resistance of a memory device (resistive RAM-RRAM) [3], or in the resistance of the storage media itself (phase change RAM-PCRAM) [4]. These emerging new NVM technologies have great potential to stimulate the increasing application of memory devices in various markets of industry and transportation, enterprise storage, mobile phones, mass storage, and smart cards, as shown in Fig.1.1. Although the market is still considerably smaller than the volatile dynamic RAM (DRAM) and Flash NAND-dominant markets (which enjoyed combined revenues of \$50+ billion on 2012), the improvement in the scalability and chip density of those novel memories will help to spark many new applications, and the market is expected to increase to

\$2,000 million by 2018 with mobile phones, smart cards, and enterprise storage as main growth drivers (Fig.1.2), according to a recently published report [5].

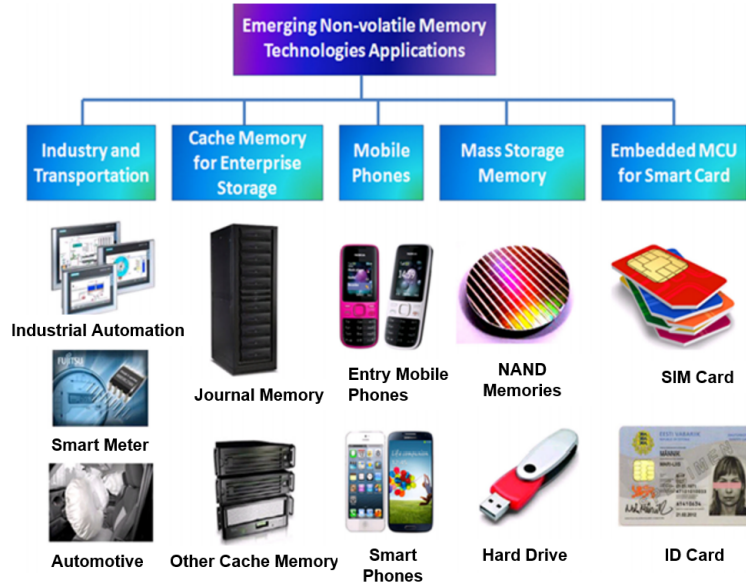


Figure 1.1: Emerging NVM applications in various markets. Reprinted from [6].

It is necessary for new technologies to match certain parameters to be able to deliver most for industry adoption. Parameters like scalability, endurance, device speed, power consumption and cost must be seriously considered to achieve the real massive adoption of emerging NVM to replace NAND and DRAM. Among all the contenders for the next generation of memory, PCRAM is the most mature technique with its products already been industrially manufactured. Table.1.1 compares the PCRAM with the well developed DRAM and Flash technologies, as well as the novel competing technologies. It is clear the strength of PCRAM lies in the competitive write speed, comparatively low energy operation and good potential for scaling to reduced dimensions.

One additional advantage for PCRAM over other technologies is its conceptually clear data storage principle, which relies on the amorphous-crystalline phase transitions of a thin bi-stable chalcogenide film. Both amorphous and crystalline materials have been widely used by humans for thousands of years. For one specific material such as carbon, technological applications for its distinct phases have also been found in various areas for their different properties. The phase change materials, however, are actually characterised by the substantial differences of their physical properties, in particular the electrical and optical properties of their amorphous and crystalline phases together with the ability to rapidly switch between these two phases (detailed switching mechanism is discussed in Chapter 2).

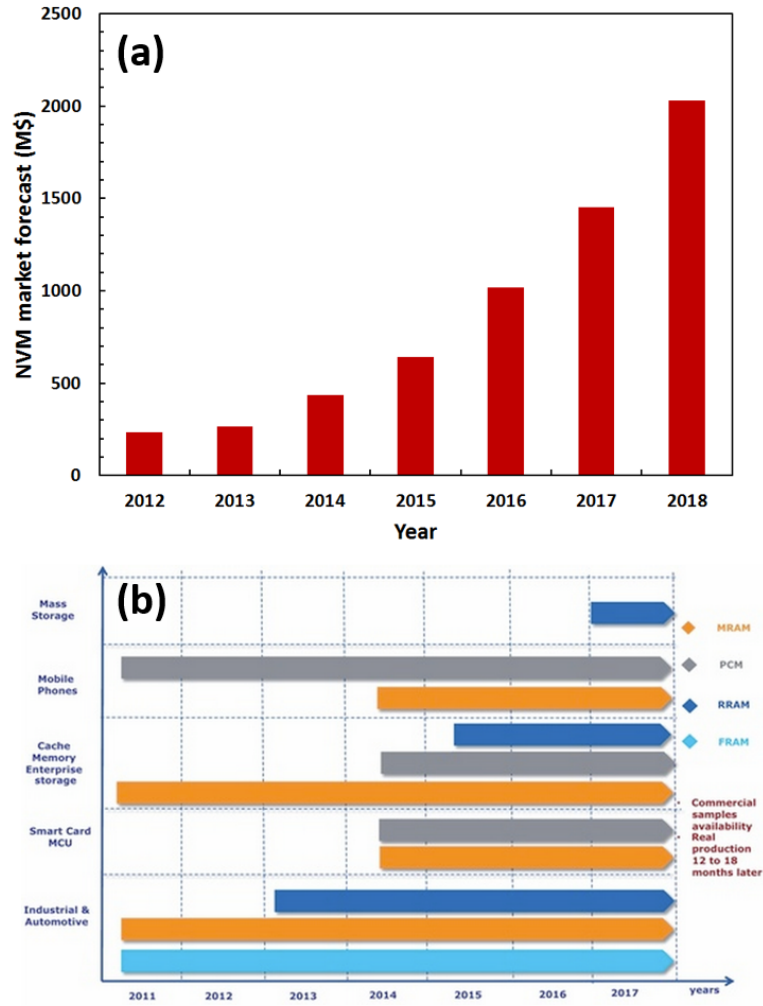


Figure 1.2: (a) Emerging NVM market forecast by applications from 2012 to 2018; (b) Emerging NVM technologies times to market. Reprinted from [5].

One of the first descriptions of phase change materials [7] and memory devices [8] was patented by A. David Pearson *et al.* from Bell Telephone Laboratories. In their works, two stable resistance states as well as a region of negative differential resistance were presented for As-Te-I alloys and the devices made from them. Specifically, the negative differential resistance serves as a characteristic for the so-called threshold switching which is one of the most important properties of phase change materials and will be described in detail in the following chapter. However, the use of a phase change material in two different phases for technological applications was first proposed by Ovshinsky, who patented [9] and published [10] this idea in 1966 and 1968, respectively. In his work, he demonstrated a repeated threshold switching between a high-conductivity state and a low-conductivity state using chalcogenide alloys of the  $\text{Te}_{48}\text{As}_{30}\text{Si}_{12}\text{Ge}_{10}$  system. He recognised the potential technological implications for data storage using these kinds of alloys and also proposed a large number of possible solid-state memory device configurations based on the phase change switching [9].

Table 1.1: An up-to-date comparison of data storage technologies. Reprinted from [5].

	PCRAM	FRAM	MRAM	RRAM	DRAM	Flash NAND
<b>Nonvolatile</b>	Yes	Yes	Yes	Yes	No	Yes
<b>Endurance</b>	Medium ( $10^8$ )	High ( $10^{12}$ )	High ( $10^{15}$ )	Medium ( $10^8$ )	High ( $10^{15}$ )	Low ( $10^5$ )
<b>2012 latest technological node produced (nm)</b>	45 nm	130 nm	130 nm	R&D	30 nm	20 nm
<b>Cell size (<math>F^2</math>)</b>	Medium (6-12)	Large (15-20)	Large/Medium (6-40)	Medium (6-12)	Small (6-10)	Very Small (4)
<b>Write speed</b>	Medium (75 ns)	Medium (100 ns)	High (10 ns)	Medium (75 ns)	High (10 ns)	Low (1000 ns)
<b>Power consumption</b>	Low	Low	High/Low	Low	Low	Very High
<b>Cost (\$/Gb)</b>	Medium (few)	High (10000)	High (100-1000)	R&D	Low (1)	Very Low (0.1)

The basis of phase change optical storage was first presented by Feinleib *et al.* [11] by inducing a phase change in a  $\text{Te}_{81}\text{Ge}_{15}\text{Sb}_2\text{S}_2$  alloy using laser heating. In this case, the difference in optical reflectivity between amorphous and crystalline phases of the phase change material was utilised to store the data. The writing and reading of the data is accomplished by laser pulses.

Despite the fact that the idea of using phase change material in data storage has already been realised in the 1960s, the commercialization of this idea was largely hindered by the fact that early phase change materials required long crystallisation times in microsecond range as well as large switching currents in the hundred mA range [12]. Besides, the limitation in the cyclability was also an obstacle. It was not until 1987 when Yamada *et al.* [13] discovered fast switching alloys on the pseudobinary line between GeTe and  $\text{Sb}_2\text{Te}_3$  that a great boost was received in the development of phase change research and technology. These new alloys show large optical contrast over a wide range of wavelengths, short crystallisation times and good cyclability which enable a whole new rewritable phase change optical storage technology. These alloys are still extremely successful today. This discovery led to the very successful rewritable optical storage technology with the third generation 100-GB capacity Blu-ray disks [14] being the latest product.

Inspired by the great success achieved in the optical phase change technology, the research in solid-state memory devices based on PCRAMs has also attracted more and more attention from numerous companies. BAE Systems [15], Hitachi [16], IBM [17], Intel [18], Macronix [17], NXP [19], Qimonda [17], Renesa [16], Samsung [20], and STMicroelectronics [21] have all launched research and development projects to investigate phase change random access memory (PCRAM) technology. Also, Micron has announced high volume availability of its 45 nm phase change memory chips [22]. IBM has also recently demonstrated the next-generation of phase change memory which can be up to 275 times faster than the conventional solid state disk [23]. These intense research and development efforts provides a promising potential for PCRAM to replace

the conventional electrical storage technologies such as Flash to be the next generation memory device. This suggests a bright future for the commercialization of PCRAM technology.

## 1.2 Thesis aim

The worldwide interest in the development of the next generation of computer memory stimulates research into new materials as well as new design of devices to fulfil the needs of storing vast amount of information. A bar chart is displayed in Fig.1.3 which represents the number of articles published with the term “phase change memory” in the title under the Web of Science database. A dramatic increase of the publications can be witnessed in phase change based memory for the recent half decade.

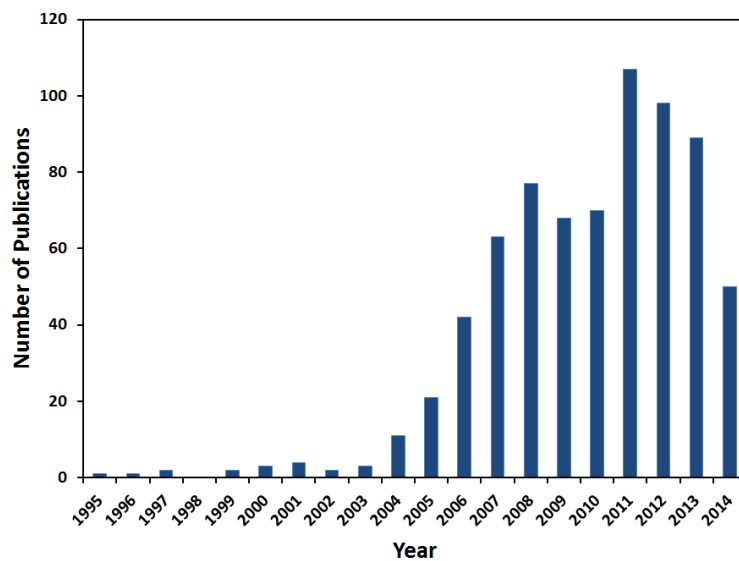


Figure 1.3: Numbers of article publications with the search term “Phase Change Memory” as a function of time (by Web of Science database).

For PCRAM to be viewed as a promising technology, it must demonstrate scalability for at least several generations to justify the heavy investment the industry needs to commit. Many efforts have already been directed to investigate the nanoscale phase change properties at both material and device level.

This project will be mainly focusing on developing novel approaches for fabricating and depositing nanoscale phase change materials and memories. These will serve as platforms for investigations of material and device properties in nanoscale. One objective in this project is to investigate the contact resistance between phase change materials and electrodes. Interfacial resistance has become increasingly important with the scaling of device size. Nanowire-structured phase change memory devices will be fabricated

through a novel approach. This technique allows fabrication of nanowires with defined dimensions, from which the contact resistances can be separated from the total resistance and compared with the material resistance. Another main purpose for this project is to realize selective growth of phase change materials into confined nanoscale structures (holes). In a memory array, joule heating at a cell site may contribute to heat-up an adjacent amorphous bit, thus speeding up its crystallization, eventually leading to data loss. The so-called thermal cross-talk issue has largely hindered the further scaling down of PCRAM. Separating phase change materials by selective deposition into confined nano-structure can largely mitigate this issue. However, the conventional deposition of phase change materials by sputtering does not allow selective deposition and is unable to uniformly fill small holes. Two novel deposition approaches, chemical vapour deposition and electrodeposition, will be used to fulfil the aim of selective deposition of phase change materials into confined nanostructures.

### 1.3 Thesis outline

The thesis has been organised in a way as shown below:

Chapter 2 gives a general background review of chalcogenide phase change materials. It first focuses on the phase change phenomenon in which the transition mechanisms between the crystalline and amorphous phases are described in detail. This is followed by a brief introduction of phase change materials diagram as well as its device operation principle. The properties of phase change materials are then reviewed together with their behaviours when scaling down. Sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin films and phase change memory devices are characterised and described in this chapter to help better understand the properties of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  material. This also serves as a benchmark for investigation of phase change materials deposited in Chapter 5 and Chapter 6.

Chapter 3 introduces the tools and techniques used during the course of this work, again illustrate with data of sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ . All of these methodologies have been employed at some point throughout this work.

Chapter 4 is the account of work done in investigating the properties of nanoscaled  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  memory device, especially the contact resistance between the  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and the electrode. A novel top-down spacer etch approach for fabricating sub-hundred nanometre nanowires is introduced.  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  nanowire devices are fabricated through this approach to study the contact behaviour between phase change material and TiN electrode in nanoscale. Subsequently, the results observed are shown and discussed.

Chapter 5 describes the work of depositing and characterising of GeSbTe phase change materials by electrodeposition in non-aqueous solutions. The depositions of individual elements are presented first. This is followed by the deposition and characterisation of

ternary GeSbTe films. Deposition into nanostructure is also demonstrated. Phase change memory devices are fabricated and characterised based on the deposited  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  material.

Chapter 6 presents the selective deposition of chalcogenide phase change materials by chemical vapour deposition. Several binary chalcogenides including  $\text{Ga}_2\text{Se}_3$ ,  $\text{Ga}_2\text{Te}_3$ ,  $\text{SnSe}_2$ ,  $\text{TiSe}_2$ ,  $\text{Bi}_2\text{Te}_3$  and  $\text{Sb}_2\text{Te}_3$  are deposited onto patterned substrates and the selectivity behaviours are investigated. In addition, systematic characterisation works are set out to characterise their chemical and electrical properties.

The final chapter summarises the results of this work and suggests areas of possible advancement and work generated as a result of this research.



## Chapter 2

# Chalcogenide Phase Change Memory

The concept of phase change memory relies on the ability to swiftly switch the phase change materials between amorphous and crystalline states. For each switch to happen, enough energy should be put into the system to break the atomic bonds. It is then possible for the atoms to settle into different structures, either crystalline or amorphous, depending on the cooling rate. The energy provided to the system can be achieved by either optical or electrical mechanisms. In optical switching, the material is exposed to intense laser beams. In electrical switching, a current or voltage pulse or sweep is applied to switch the material through Joule heating.

### 2.1 Phase change optical data storage

Optical data storage represents a major chapter in the information storage history. Optical phase change device has been an area of intense research for the past 3 decades which brings great commercial success with the productions of CDs (Compact Discs), DVDs (Digital Versatile Discs) and BDs (Blu-ray discs). Data recording and erasing in these discs are achieved by the crystallographic structural changes of thin film phase change materials heated by a laser pulse.

In the writing process, the amorphization of the phase change material is achieved by heating the phase-change thin films with sufficient laser power above its melting point and then rapidly quenching to room temperature. The erasing process, on the other hand, is realized by annealing the phase-change films at the temperature between the crystallization temperature and the melting point with a medium power laser irradiation. The overwriting of the data is also feasible by laser power modulation between a peak recording power level and a bias erasing level as shown in Fig.2.1. This overwrite method

shows that the films irradiated with the peak power become amorphous, and those irradiated with the bias power change to the crystalline phase, no matter which phase the phase-change material is in before the overwriting.

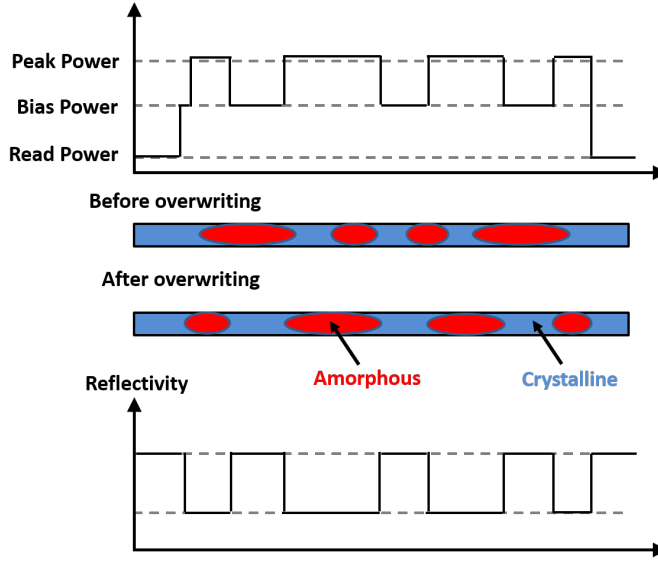


Figure 2.1: Overwriting methods of phase change optical recording.

For a rewritable CD or DVD, a thin layer of phase change material is sandwiched between dielectric layers. The reproduction of recorded informations utilises the different optical indices in their crystalline and amorphous states, which leads to different reflectivities. The relation between the optical constants and the material reflectivity is given by:

$$R = \frac{(n - 1)^2 + k^2}{(n + 1)^2 + k^2} \quad (2.1)$$

where  $n$  is the index of refraction and  $k$  is the coefficient of extinction. However, in real optical devices, the actual reflection is determined by not only the optical constants but also the thickness of each layer, as well as surface and interface roughness, etc.

When incident light wave propagates in a material, the light gets absorbed. The absorption coefficient  $\alpha$  for a material is defined by the relation:

$$I = I_0 \exp(-\alpha x) \quad (2.2)$$

where  $I_0$  is the initial light intensity and  $x$  is the distance it propagates in the material. The value of  $\alpha$  determined from Equation 2.2 can then be related to the optical constant  $k$  by

$$\alpha = 4\pi k/\lambda \quad (2.3)$$

where  $\lambda$  is the wavelength of incident light. It is hence clear that the optical constant  $k$  will effect the reflection of the material and can serve as an indication for us to compare the optical change for phase change materials.

The values of the optical constants and absorption coefficient obtained from sputtered thin films of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  in this work are shown in Fig.2.2 which are in a good agreement with those reported [24, 25, 26]. The small difference could be explained by the different deposition methods used for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  films. It is worth mentioning here that the optical constants are in fact not constants and depend on the wavelength as well as the film thickness.

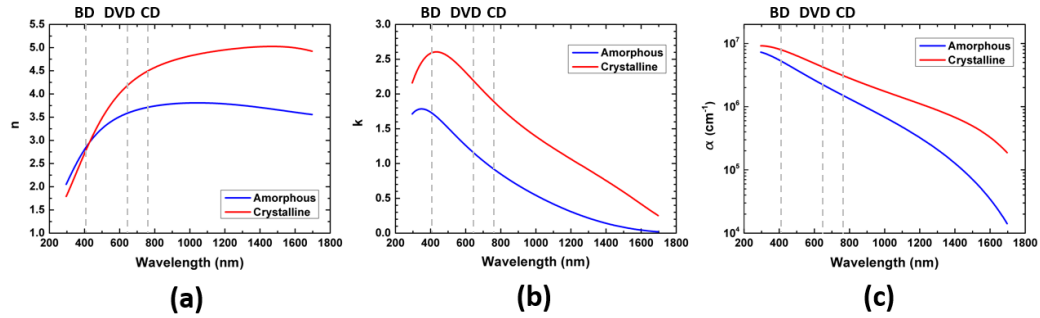


Figure 2.2: Optical constants (a)  $n$ , (b)  $k$ , and (c)  $\alpha$  of amorphous and rocksalt crystalline phases of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  films. CD, DVD, and BD marks the laser wavelength used for rewritable CDs, DVDs, and BDs, respectively. Results were obtained by fitting the spectroscopic ellipsometry data of sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin films with a Cody-Lorentz oscillator model. More details can be found in Section 3.2.5.

Significant differences between the optical constants of amorphous and crystalline phases are evident in both visible and near-infrared range. This striking difference is the enabling feature of the phase change optical recording. However, it is also obvious that the technological move to shorter wavelengths for increased optical storage density becomes problematic because the optical contrast is reduced. That is why Blu-ray discs apply compositions other than  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ . Another important optical parameter is the optical band gap. The values of optical band-gap were determined to be 0.696 eV for amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and 0.517 eV for crystalline  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and are in good agreements with the reference [26, 27].

## 2.2 Phase change random access memory

The basic principle for phase change random access memory (PCRAM) device operation is to utilize the large resistivity contrast between crystalline (low resistivity) and amorphous (high resistivity) phases of the phase change material. The low and high resistance states can be obtained by set and reset processes, respectively, as shown in Fig. 2.3.

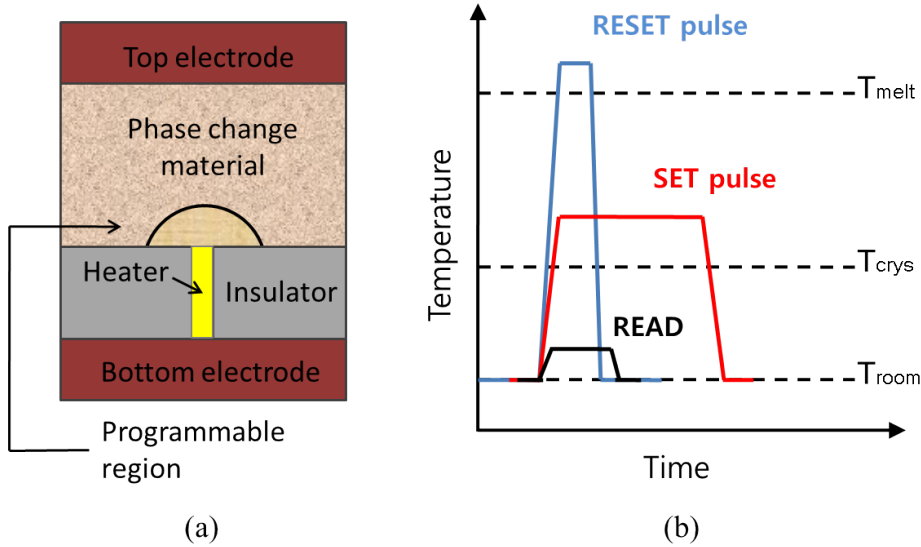


Figure 2.3: (a) The cross-section schematic of the conventional PCM cell. The electrical current passes through the phase change material between the top electrode and heater. Current crowding at the heater to phase change material contact results in a programmable region illustrated by the mushroom boundary. This is typically referred to as the mushroom cell. (b) PCM cells are programmed and read by applying electrical pulses which change temperature accordingly.

The set of the PCRAM cell from amorphous into crystalline state can be achieved by applying a medium electrical current pulse to anneal the programming region at a temperature between the crystallisation temperature and the melting temperature for a time period long enough for the crystallisation to occur. This can also be done by just applying a DC voltage or current to anneal the material as it does not require a quenching process which can only be achieved by electrical pulse. To read the state of the programming region, the resistance of the cell is measured by passing an small electrical current which is too low to disturb the state. The reset of PCRAM to the amorphous state (high resistance) requires the melt-quenching process as discussed above, in which the crystalline material is first melted and then cooled down so fast that it solidifies into the amorphous state. This is done by applying a large electrical current pulse for a short time period. Since the formed high-resistance amorphous region is in series with

the remaining crystalline region, it will predominantly determine the resistance of the PCRAM cell between the top electrode contact and the bottom electrode contact.

Fig. 2.4 shows a typical current-voltage curve for set and reset states of a PCRAM [28] using DC current sweeping. The large resistance contrast between amorphous and crystalline phases can be seen for voltages below the threshold switching voltage  $V_{th}$ . The reset state is in the high-resistance state below  $V_{th}$  and shows electronic threshold switching behaviour at  $V_{th}$ , which indicates a negative differential resistance. The set process critically depends on this electronic threshold switching effect. When the electric field across the amorphous region reaches a threshold value, the resistance of the amorphous region goes into a lower resistance state which has resistivity comparable to the crystalline state. This is essential for the successful set programming of the PCRAM as the resistance in reset state is too high to conduct enough current and provide enough Joule heating for the crystallisation of PCRAM cell. The electronic threshold switching effect lowers the resistance of the phase change material to dynamic resistance and enables set programming.

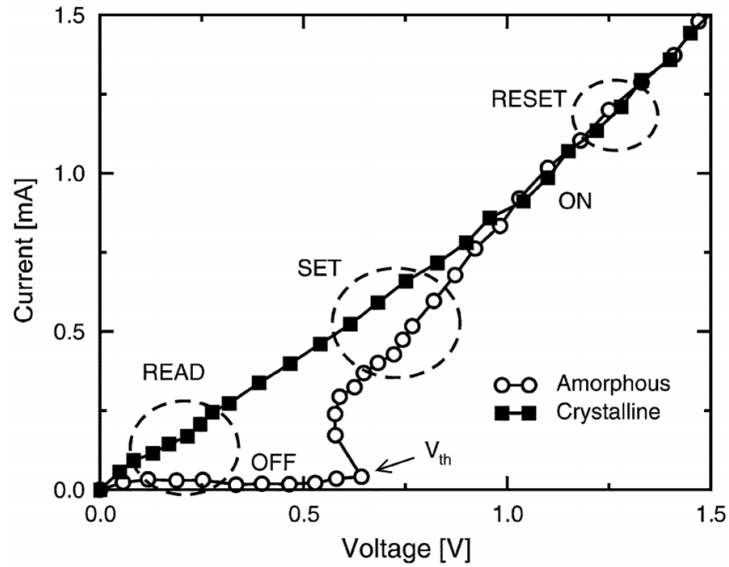


Figure 2.4: A typical I-V curves for set and reset state of a PCM by DC current sweeping. Reprinted from [28].

However, this threshold switching is reversible and the resistance of the cell can return to the high state if the phase of the material has not been changed yet before the removal of the voltage. If the voltage is applied for sufficiently long time, it will then lead to the phase change and a permanent change of resistance. This is illustrated in Fig. 2.5 in which DC voltage sweeping is applied on a pristine  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  phase change device. The device is in a high resistance ( $\text{M}\Omega$ ) state after the fabrication processes. A first resistive switch was observed at a voltage of 5.9 V where the current dramatically increased and hit the compliance current. It is worth mentioning here that a compliance current is necessary for voltage sweeping as it protects the devices from a hard breakdown due

to overheating. However, this first threshold switching did not provide enough heat to crystallise the entire  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  layer and the resistance went back to a high state upon removal of the voltage. A second voltage sweeping induced a resistive switching. This time, crystallisation has taken place and the materials is now in low resistance ( $\text{k}\Omega$ ) state. The decrease of threshold voltage is possibly due to the partial crystallization of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film in the first sweeping, resulting in a thinner amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  layer. This can be proved by the slightly decreased resistance ( $1.09 \text{ M}\Omega$ ) after the first sweeping. After a second sweeping, the heat generated was sufficient enough to crystallise the entire layer and the devices stayed in a low resistance state ( $933 \Omega$ ). In practical, this set programming time can be a limitation for the operating speed of actual PCRAM devices since it takes a finite time to fully crystallise the amorphous region.

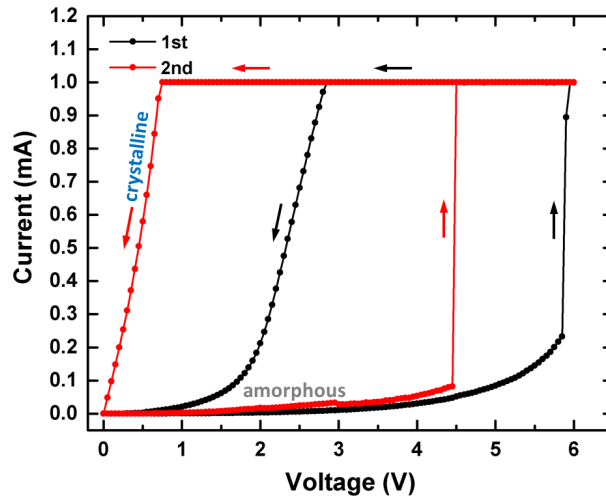


Figure 2.5: Typical current-voltage characteristic of a pristine  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  phase change device by voltage sweeping. Phase change does not happen after the first DC sweeping (black) and the material returned to high resistive state upon removal of the voltage. The second DC sweeping induces crystallisation and the material stays in low resistive state. The results were obtained from a sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  memory device with a size of  $4 \mu\text{m}$  fabricated in this work.

The electronic threshold switching effect is the key property for phase change materials, although the exact mechanism is still unclear and requires further investigation. It is suggested by Krebs *et al.* that the important parameter for threshold switching is a critical electrical field which differs for different materials [29]. The threshold voltage is solely a function of material thickness rather than other parameters such as device size. This can be proved by Fig.2.6 in which the switching characteristic of pristine  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  devices with same material thickness but different sizes are shown using DC current sweeping. In this case, no compliance is required as the threshold current is much lower than the breakdown current. The resistive switching behaviour in current sweeping is indicated by the snap-back character where the voltage suddenly drops to

a lower value due to the decrease of resistance. It is obvious that all devices with same thickness have similar threshold voltages (5 - 6 V), while the device size only affects the device resistance in both states. For a larger device with a relative lower resistance, a higher current is required to reach the threshold voltage, and vice versa.

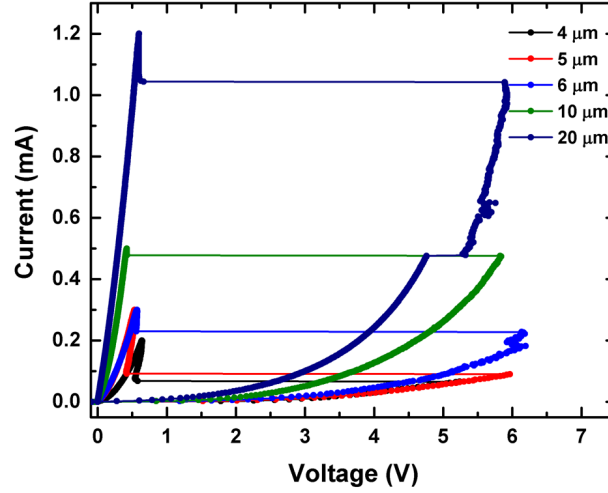


Figure 2.6: Typical current-voltage characteristic of pristine  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  phase change devices with same material thickness but different sizes by current sweeping. The results were obtained from several sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  memory devices with different sizes fabricated in this work.

It is also worth pointing out that there is a difference between the first crystallisation and re-crystallisation of a PCRAM cell. Normally, re-crystallisation of a non-pristine cell requires a smaller voltage as the amorphous volume created in the reset process only accounts for a small portion of the entire cell. Fig. 2.7 shows the second set process for the same device in Fig. 2.5. After first crystallisation from pristine amorphous state, the device was reset back to the high resistance reset state. A much lower threshold voltage was then observed (*ca.* 1.45 V) for the second set process which indicates the reset process only partially amorphized the  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  layer. This partially amorphized volume then serves as the programmable region of the cell for the future switchings and only this threshold voltage is relevant from the practical point of view.

The reset of the PCRAM device is the most energy demanding task as sufficiently high current has to be applied to lift the temperature to the melting point of the material. This is normally achieved by applying a relative high electrical pulse with short width (*ca.* 100 ns) and a short trailing edge (*ca.* 20 ns) to meet the requirement of melt and quenching. During the reset operation, the interface between the material and heater first gets melted which subsequently acts as the major Joule heating source within the structure due to its large conductivity. The peak temperature reached at the material/heater contact can be written as [30]:

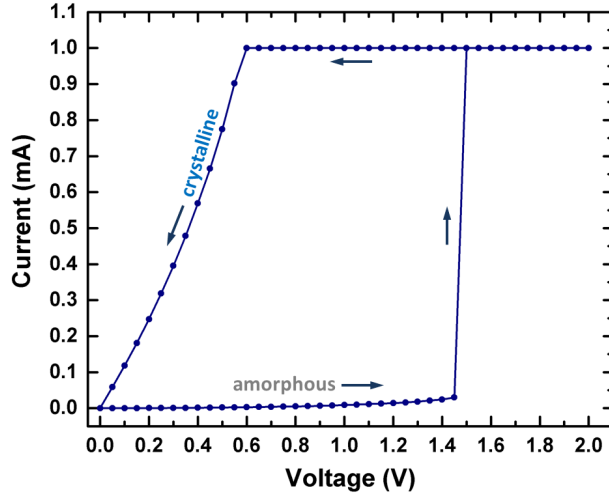


Figure 2.7: Typical current-voltage characteristic of non-pristine  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  phase change device by voltage sweeping. The results were obtained from a sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  memory device with a size of  $4\ \mu\text{m}$  fabricated in this work.

$$\Delta T \approx R_{th} R_h I^2 \quad (2.4)$$

where  $R_h I^2$  corresponds to the heating power developed across the bottom electrode while  $R_{th}$  corresponds to the thermal resistance accounting for the heat diffusion from the hot volume to the surroundings. The reset current  $I_m$  required to reach the melting temperature can then be derived as:

$$I_m \approx \sqrt{\frac{\Delta T_m}{R_{th} R_h}} \quad (2.5)$$

It is clear in this equation that the reduction of  $I_m$  can be achieved by scaling the device dimensions. A shrinking of all linear dimensions by a factor of  $k$  would lead to an increase of both electrical and thermal resistance by a factor of  $k$ , which should decrease  $I_m$  by the same factor. This assumption is supported by the practical device performances as shown in Fig.2.8 where a linear relationship was observed between  $I_m$  and set resistance [30]. In fact, scaling as the main contributor to the power performance improvement for PCRAM has been pursued from the very beginning of the industrial exploitation of this technology and is also a main motivation of this work.

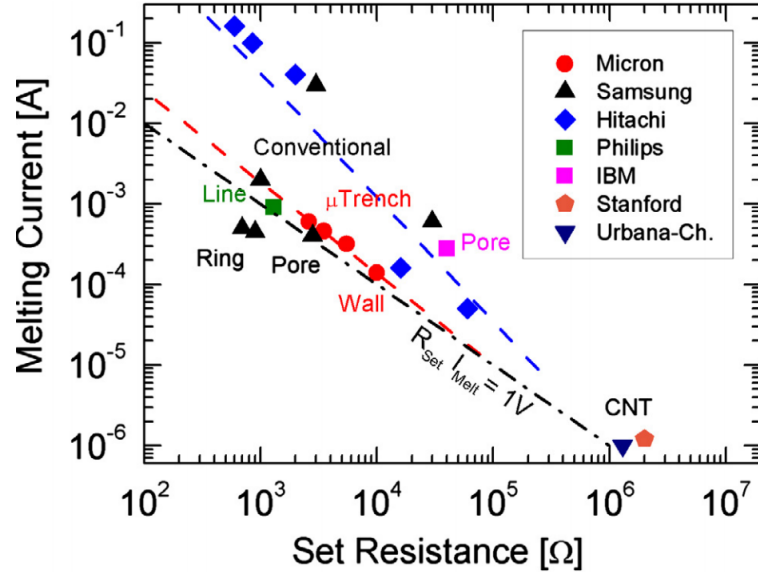


Figure 2.8: Melting temperature as a function of set resistance. Reprinted from [30]

Apart from scaling, material engineering also serves as an effective way to decrease  $I_m$  by increasing the electrical/thermal resistivity or decreasing the melting temperature of the material. This will be discussed in more detail in the following section.

The reset programming also has a huge impact on the reliability of PCRAM. Fig. 2.9 shows the typical cycling dependence of resistance window with the number of  $10^9$  times [31]. Although known to feature remarkable endurance compared with flash memory, cell degradation is still the major concern for PCRAM. One problem is the so-called “stuck-set”, in which the resistance of the reset state progressively drops and the device fails by being stuck in the low-resistance state. This problem is normally caused by either heater seasoning or stoichiometric shifts of the phase change material. The heating resistance decreases during cycling which weakens the heating capability of the device, resulting in a lower peak temperature reached during programming. This then leads to a thinner and thinner amorphous area as well as a lower reset resistance. However, the “stuck-set” caused by this heater seasoning is reversible under a larger reset pulse. On the other hand, the stoichiometric shifts-induced “stuck-set” is permanent in which the properties of phase change materials are deteriorated by reactions with electrode materials [32], phase separation of the alloy species due to incongruent melting [33] and ion migration promoted by the high temperature and current density [34]. Fig. 2.10 shows the cycling dependence of resistance window in which the “stuck-set” happens after 50 cycles of switching.

In addition, PCRAM device may also fail in a “stuck-open” state. This is typically related to the relatively large change in mass density between the two phases of phase change materials. Normally, the crystalline phase has a 5-10% higher density compared

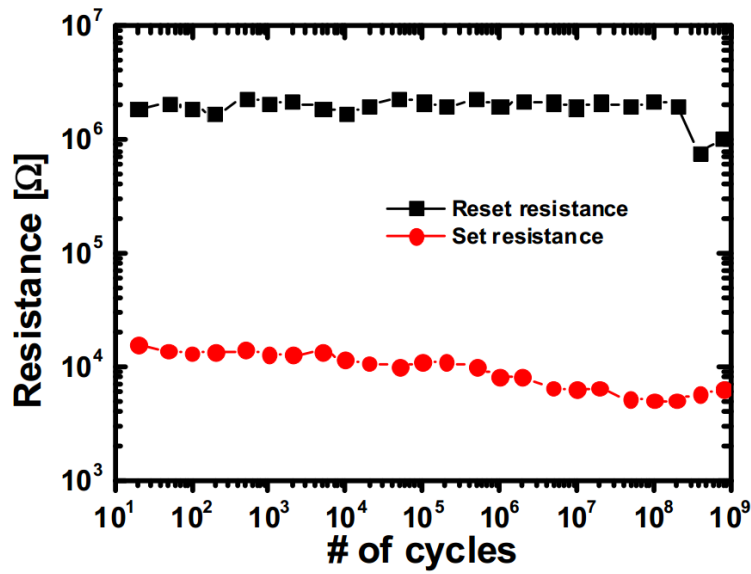


Figure 2.9: Typical endurance performance of a PCRAM cell at 45 nm node. Reprinted from [31]

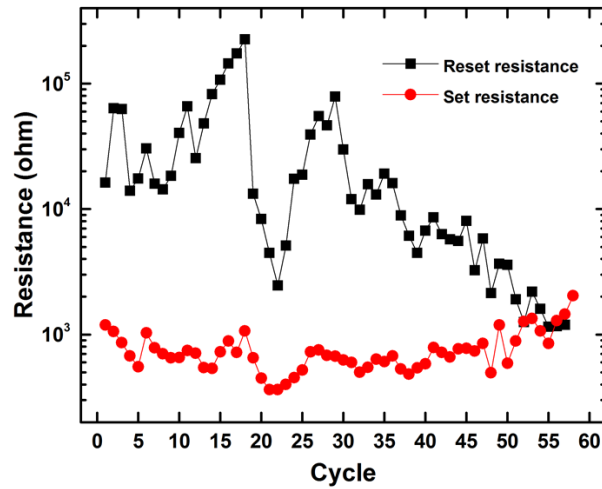


Figure 2.10: Typical “stuck-set” in the cycling of PCRAM. The reset resistance drops to the level of set resistance after 50 cycles. The results were obtained from a sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  memory device with a size of  $8\ \mu\text{m}$  fabricated in this work.

with the amorphous phase [35]. When the device is cycling repeatedly between the two phases, void could be formed at the interface with the bottom contact, leading to detrimental problem for phase change memory [36]. It is suggested that the void formation could be mitigated by doping and care interfacial cleaning [37]. A better solution would be to use phase change materials with zero-density change between two phases. Putero *et al.* has recently reported the mass density changes of a series of Ga-Sb alloys. It was found that at a particular composition ( $\text{Ga}_{0.3}\text{Sb}_{0.7}$ ), the mass density is equal for thin layers in both phases [38]. This is extremely interesting for PCRAM applications.

The read process of PCRAM is normally done by apply a small voltage across the device and read the current. It is worth noting that advantages of  $I_m$  reduction brought by increasing set resistance could have a negative impact on the reading speed. A fast reading (below 50 ns) requires relatively larger current of a few microampere, which limits the maximum value of set resistance to below about 200 k $\Omega$ .

## 2.3 Phase change operation

The phase of the material affects its structural, optical and electrical properties. Materials in the amorphous phase have a large energy band-gap which leads to a low intrinsic absorption and high resistivity. Crystalline materials have a small band-gap which enables electrical conduction at room temperature. Normally, crystalline materials have a higher refractive index (at visible wavelengths) as well as a lower electrical resistance as compared to the amorphous materials with the same chemical composition. The switching between these two phases are realized by the amorphization and crystallisation processes as discussed below.

### 2.3.1 Amorphization

Amorphization of phase change material is a so-called melt-quenching process. Fig.2.11 shows a schematic of the glass formation process where the amorphous phase is achieved by fast cooling of melted (liquid) material. If the cooling rate is fast compared with the characteristic time constants (e.g. the kinetics) of the crystallisation process, the phase change material will be supercooled and enter a glassy state in a narrow temperature range near the glass transition temperature  $T_g$ . The glass transition temperature can be defined as that, below which the ability of the material to rearrange itself becomes long compared to experimentally accessible times (*ca.*  $10^2$  sec) and hence the material behaves as mechanically rigid, though structurally disordered. During the glass transition process, the volume of the material undergoes no sudden change and the materials enters a metastable state whose volume and free energy depends on the cooling rate. The reached glassy state has an elastic modulus but lacks long range order.

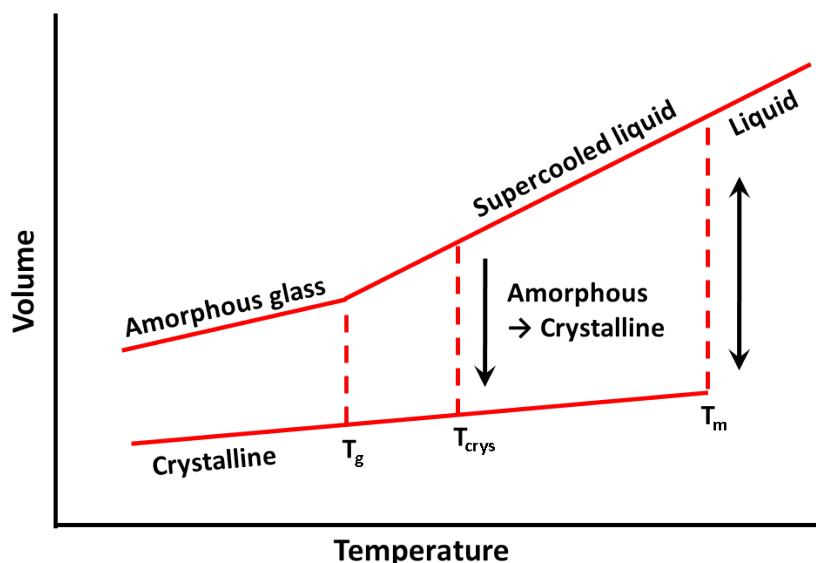


Figure 2.11: A schematic view of the glass formation diagram.

### 2.3.2 Crystallisation

Crystallisation of phase change materials from the amorphous phase happens when the temperature reaches a certain value. This value is defined as crystallisation temperature which will be discussed in more detail in the following section. It is worth mentioning here that crystallisation can also be achieved by cooling melted material at a medium rate as contrary to the quenching process in amorphization. However, this is unlikely to happen in actual phase change memory device as the melting temperature is much higher than the crystallisation temperature.

When the temperature requirement is met, crystallisation starts with two processes. The first process is the crystal nucleation. This consists of two types: homogeneous nucleation, in which the nucleation only occurs in the interior of the system and heterogeneous nucleation in which the material is in contact with a foreign substance that acts as a preferred nucleation site. The second process of crystallisation is crystal growth where the stable crystal cluster grows to macroscopic size.

Based on the speed of these two processes, the phase change materials can then be classed into two groups: nucleation dominated (driven) and growth dominated (driven) as shown in Fig. 2.12. Nucleation dominated materials have relatively short incubation times, high nucleation rates, but slow growth velocities while growth dominated materials have relatively long incubation times, low nucleation rates, and high growth velocities.

One class of materials (e.g. Ge-Sb-Te system) shows a nucleation dominated crystallisation process for which the nucleation rate is higher than the growth rate. In this case, the crystallisation of an amorphous material mark will start by homogeneous nucleation

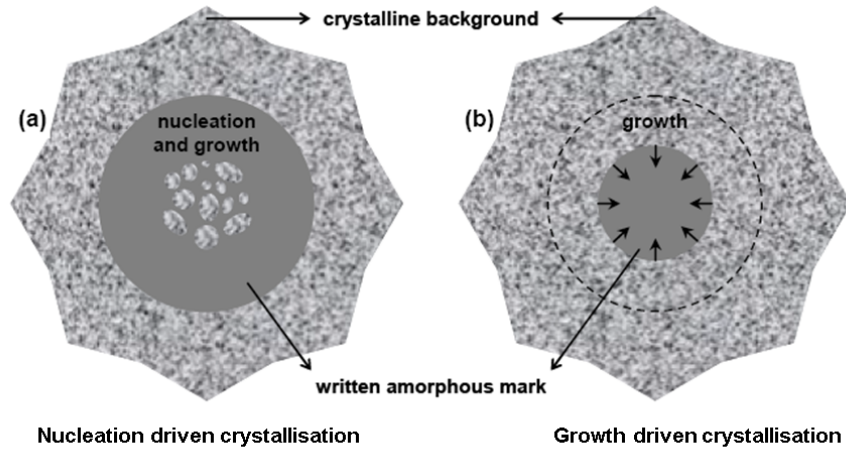


Figure 2.12: Nucleation driven crystallisation (a) versus growth driven crystallisation (b). Reprinted from [39].

in the centre or all over the amorphous mark and proceed towards the circular rim of the amorphous mark (i.e. the interface between the amorphous mark and crystalline surrounding). While for another class of materials, crystallisation will start at the interface and proceed towards the centre of the mark and show growth dominated crystallisation process (e.g. doped Sb-Te system). However, it is worth mentioning that the rates of two processes also depend on the temperature, it is hence possible for the same material to behave like a nucleation dominated material at low temperature but like a growth dominated material at high temperature, such as Ag- and In-doped  $\text{Sb}_2\text{Te}$  (AIST) [40].

## 2.4 Chalcogenides phase change materials

Although the two transitions discussed above can be found in many materials, most known materials suitable for phase change memory application can be found in the category of so-called chalcogenides. The name chalcogenide originates from the Greek word *chalcos* - 'ore' and *gen* - 'formation'. Thus the term chalcogenide is generally considered to mean 'ore former'. It can exist naturally as mineral such as  $\text{FeS}_2$  (pyrite) and  $\text{AuTe}_2$  (calaverite). Normally, a chalcogenide refers to a chemical consisting of at least one chalcogen ion and at least one more electropositive element. Although all elements in group 6 of the periodic table are formally defined as chalcogens, the term is more commonly reserved for sulfides, selenides, and tellurides, rather than oxides. This division can be explained by both historic and scientific reasons. Historically, it is a tradition to treat the oxide materials separately since they are the oldest-known glass forming systems, silica in particular, while most of the chalcogenides were newly found. Scientifically, oxide materials behave rather differently compared with chalcogenides especially with respect to band-gap energies. Conventional oxides, like silica, are poor

electrical conductors with a large energy gap (10 eV for SiO<sub>2</sub>). On the other hand, chalcogenides are mostly semiconductors with band gaps between 1 eV to 3 eV.

Chalcogenides have already found use in lenses and prisms, special optical fibres and even as windows in submarines with their unique optical properties such as long wavelength transmissions and high non-linear refractive indices. More importantly, the discovery of their ability to switch their properties based on switching their structure from glass (amorphous phase) to crystal (crystalline phase) enables them to be widely used in information storage. It should be noted that since chalcogenides can exist over a wide range of compositions, not all of them exist in a glassy form and hence can be used to store information. The model of a binary glass-forming chalcogenide is considered to be analogous to silica where two chalcogen elements (group 6) are bonded to a single group 4 element. Besides, another class of chalcogenides with glass-forming behaviours are three chalcogens bonded to two group 5 elements. These two classes mark the most stable binary chalcogenide glasses and can exist in a wide range of atomic ratios. An even greater engineering capacity lies in ternary chalcogenide glasses which allow a larger variety of atoms to be incorporated into the glass structure. The categorization of amorphous chalcogenides can be classed by atoms to which they bond to form amorphous systems as shown in Table.2.1 [41].

Table 2.1: Amorphous chalcogenide systems grouped by class [41]

Class	Examples
Pure chalcogenide	S, Se, Te, $S_xSe_{1-x}$
Pnictogen-chalcogen (V-VI)	$As_2S_3$ , $Sb_2Te_3$ , $Bi_2Te_3$ , $P_2Se$
Tetragen-chalcogen (IV-VI)	$SiSe_2$ , $SnSe_2$ , $GeS_2$ , $Ge_2Sb_2Te_5$ , GaLaS
III-VI	$B_2S_3$ , $Ga_xSe_{1-x}$ , $Ga_xTe_{1-x}$ , $In_xSe_{1-x}$
Metal chalcogenide	$MoS_3$ , $WS_3$ , $Ag_2S-GeS_2$
Chalco-halides	As-Se-I, Ge-S-Br, Te-Cl

Apart from having both amorphous and crystalline states, to be a good candidate for phase change memory devices, certain requirements must be met with regards to the material properties which will be discussed in detail in the next section. Fig.2.13 shows the ternary phase diagram for materials which have been investigated for the last few decades for phase change memory devices. Among these materials, the pseudo-binary alloys lying on the GeTe-Sb<sub>2</sub>Te<sub>3</sub> tie line and doped SbTe alloys are the most successful candidates for memory devices.

The GeSbTe system is the most studied phase change materials and is currently used in both optical and electrical phase change memory devices. Materials in this system enjoy the advantage of short crystallisation times, such as Ge<sub>1</sub>Sb<sub>4</sub>Te<sub>7</sub> (30 ns), Ge<sub>1</sub>Sb<sub>2</sub>Te<sub>4</sub> (40 ns) and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> (50 ns). Most of the studies have been focused on Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> due

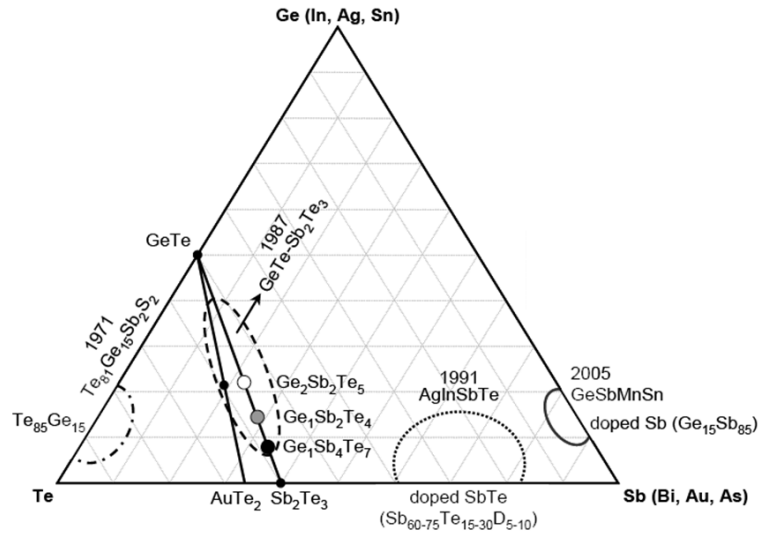


Figure 2.13: Ternary phase diagram showing various phase-change alloy compositions studied for various phase-change memory devices in the past two decades. D: dopant. Reprinted from [42].

to its excellent scalability, rapid phase switching speed and large optical and electrical contrast between two states [43, 44, 45]. However, a major problem for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> is its relatively low crystallisation temperature which might lead to a low data retention time. In addition, the phase separation because of the low melting temperature and high vapour pressure for Te will also cause a reduction of reliability of the material. It has been suggested that by adding dopants to this alloy, properties such as crystallisation temperature can be enhanced. Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> with different dopants such as N [46, 47, 48, 49, 50], C [51], In [52], SiO<sub>2</sub> [53], Sn [54], Ti [55], Ce [56] have been reported with enhanced phase change behaviour.

The binary GeTe system has been considered as an alternative material to GeSbTe due to its excellent phase change properties such as larger resistance contrast and higher data retention time [57]. However, its higher melting temperature (*ca.* 700) has largely obstructed its application in PCRAM. It has been reported that an increase of Te content from GeTe to GeTe<sub>4</sub> could significantly reduce the melting temperature (*ca.* 380) without reducing the crystallisation temperature [58]. Besides, the addition of a third element to GeTe were also proved to be an effective method to further improve the properties of GeTe thin films. GeTe films incorporated with dopants such as C [59, 60], Si [61], N [62], HfO<sub>2</sub> [63], were also found to show competitive phase change behaviours.

The Sb-Te system has also attracted a lot of attention, although stoichiometric Sb<sub>2</sub>Te<sub>3</sub> itself is not a proper phase change materials due to its low crystallisation temperature [64]. Alloys of Sb-Te with other compositional ratios show more decent properties as

phase change material with higher crystallisation temperatures and larger electrical contrast between two phases such as SbTe and Sb<sub>2</sub>Te [65]. The importance of Sb-Te system lies in its ability to include a variety of dopants. Numerous dopants have been added to Sb-Te system in order to explore potential phase change materials. Dopants like Si [66, 67, 68, 69, 70], N [71, 72], Ga [73], Cu [74], Al [75, 76], In [77], Ti [78], HfO<sub>2</sub> [79], SiN [80] have been studied and show favourable behaviour for phase change memory device such as better thermal stability, lower power consumption and faster switching time.

Apart from those traditional phase change materials in the Ge-Sb-Te ternary phase diagram, alternative materials have also been synthesized and deposited and show promising feature for potential phase change memory materials. Ga-Sb alloys as a promising alternative has been extensively investigated as strong candidates for the application of PCRAM [81, 82, 38]. Compare with Ge-Sb-Te, they show high thermal stability and very short crystallization times ( $< 15$  ns). More importantly, a zero-mass density change upon crystallisation was observed for the Ga<sub>0.3</sub>Sb<sub>0.7</sub> alloy. This is particular interesting in PCRAM application to avoid film delamination or void formation. Hewak *et al.* demonstrates phase change devices using gallium lanthanum sulphide (GLS) alloys, showing low power consumption with improved thermal stability and endurance [83]. Sotou *et al.* also reported an improved thermal stability and better data retention by using Ge<sub>1</sub>Cu<sub>2</sub>Te<sub>3</sub> alloy [84, 85].

## 2.5 Properties of phase change materials

Research on properties of phase change materials is essential for application in industry. Some of the properties are directly related to the performance of memory devices. Despite their importance, the understanding of these properties has been limited, and materials development and optimization have mostly been empirical. Eight properties of phase change materials are investigated in this section through both literature review and own experiments. Here, we mainly focus on the application in PCRAM and their behaviours with scaled dimensions in both lateral and vertical directions.

### 2.5.1 Crystallisation time

Crystallisation time is the time required for the phase transition from amorphous to crystalline. This is the data rate limiting factor since crystallisation of phase change material requires a considerable amount of time to happen as we discussed in the previous section. As a matter of fact, the application of phase change materials has not been taken seriously until the discovery of the fast switching materials on the Sb<sub>2</sub>Te<sub>3</sub>-GeTe pseudo-binary line (with Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> the most popular candidate). For future development, a

shorter crystallisation time is favourable from the memory device perspective since it means a quicker switching time.

It is important to distinguish the crystallisation time required for as-deposited amorphous material and the re-crystallisation time required for melt-quenched amorphous material. As-deposited amorphous material has a longer crystallisation time compared with its melt-quenched state. Fig. 2.14(a) compares the crystallisation time between as-deposited and melt-quenched amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  by comparing their relative change in reflectivity upon laser exposure for various laser powers and pulse lengths [86]. It is obvious that for melt-quenched material, a shorter time (a few nanoseconds) is enough for crystallisation while for as-deposited material, a much longer time (100 ns) is required. This discrepancy can be explained by two reasons. The melt-quenched material has a crystalline-amorphous border where the crystal can grow directly from without the requirement of nucleation. In addition, the melt-quenched material has a higher medium-range order and already contains small ordered regions which act as nucleation centers [87]. In this case, a more dramatic difference can be expected on growth-dominated material which has a low nucleation rate but a high growth rate as shown in Fig. 2.14(b) for  $\text{Ge}_{15}\text{Sb}_{85}$  [86]. From the practical application point of view, only the re-crystallisation time of melt-quenched materials is relevant.

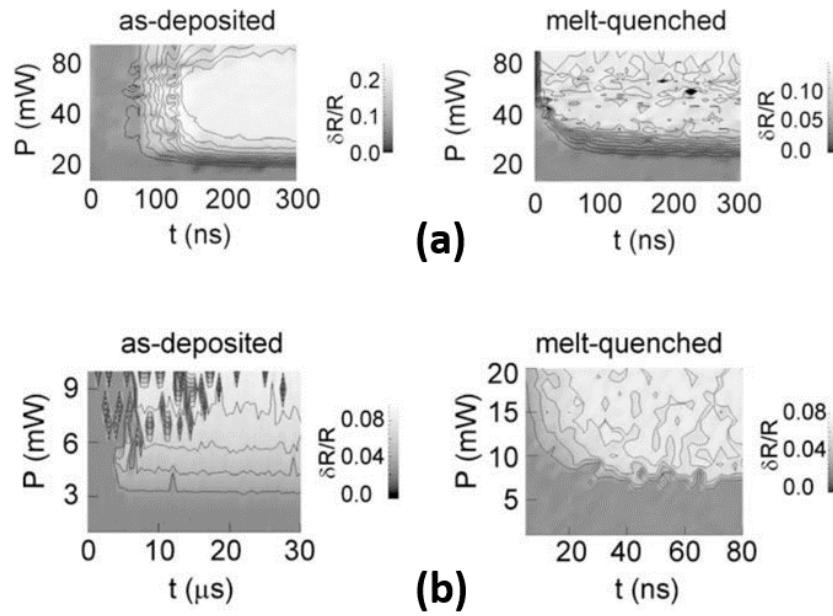


Figure 2.14: Relative change in reflectivity for (a)  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and (b)  $\text{Ge}_{15}\text{Sb}_{85}$  for as deposited and melt-quenched materials. Crystallisation happens when the reflectivity starts to change. Reprinted from [86].

Apart from material itself, both substrate and capping layer will influence the re-crystallisation time and this influence becomes stronger when the film thickness is

reduced as the interface plays a more important role. For nucleation-dominated materials and growth-dominated materials, opposite trend of re-crystallisation time was found [88]. While the Ge-Sb-Te materials (nucleation-dominated) had an increase re-crystallisation time, Ag-In-Sb-Te materials (growth-dominated) experienced a decrease of re-crystallisation time when the film thickness was reduced. In this case, the growth-dominated materials have a more promising application in discs with thin films. On the other hand, an optimum thickness where crystallisation time is minimized was presented for Sb-Te based materials by Marten *et al.* [89]. The re-crystallisation time decreased as the film thickness reduced to 9 nm and then increased dramatically as the film thickness was further reduced. The interplay of the interfacial energies at the amorphous-crystalline and phase-change-dielectric boundaries was believed to be the reason for this behaviour.

Apart from the film thickness, the scaling of phase change material cell size was also investigated. A shorter re-crystallisation time for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  was observed as the device diameter is reduced as shown in Fig.2.15(a) [43]. The minimum re-crystallisation time was 2.5 ns for a cell size with diameter of 19 nm. A same trend was also observed in  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  nanowires [90]. At a higher surface-to-volume ratio for nanowires, the heterogeneous nucleation is enhanced and thus leads to the size-dependent crystallisation behaviour.

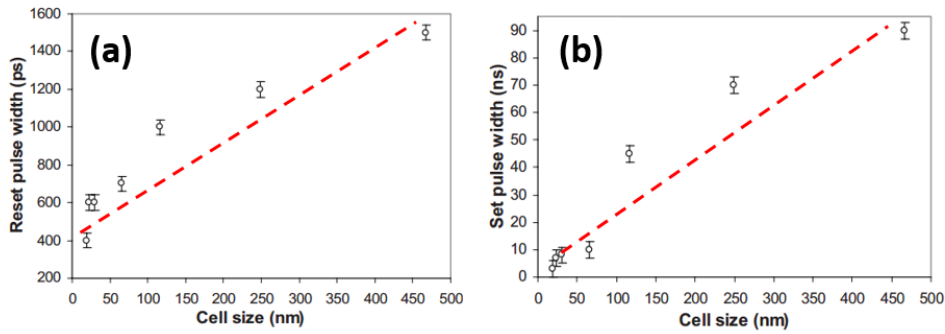


Figure 2.15: The shortest (a) set and (b) reset switching pulse width as a function of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  cell size varying from 500 nm to 19 nm for set process measured on pore devices. The pulse amplitudes are 0.8 V and 4.5 V for set and reset, respectively. The dotted lines serve as a guide of eye. Reprinted from [43].

### 2.5.2 Melt-quenching time

Melt-quenching time is the time required to heat the crystalline phase change material to its melting temperature and hence is largely depended on the melting temperature. For a strong enough power, the melting time can be extremely short compared with the

re-crystallisation time [91]. A reduced melting time was also found for thinner Sb films by fast laser test [92].

For the electrical pulse induced melting, the same trend can be observed for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  with reduced cell size with the shortest melting time being around 400 ps as shown in Fig.2.15(b) [43].

### 2.5.3 Crystallisation temperature

The crystallisation temperature ( $T_x$ ) is one of the most important parameters since it determines the data retention, thermal stability as well as the power required to crystallize the material. The crystallisation temperature for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin film can be determined by measuring the diffraction patterns of film annealed at different temperatures. Diffraction pattern of crystalline film with periodic atom arrangement will have sharp interference maxima while no peaks can be observed for amorphous film (more details for X-ray diffraction can be found in Chapter 3). Fig.2.16 shows the X-ray diffraction (XRD) patterns for the same  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  films annealed at temperature from 100°C to 200°C. It is clear that the as-deposited film is in amorphous state. This phase remains after annealing at 140°C. A phase change is then obtained when annealing at temperatures higher than 160°C where clear diffraction peaks can be observed. The  $T_x$  can hence be determined to be between 140°C and 160°C.

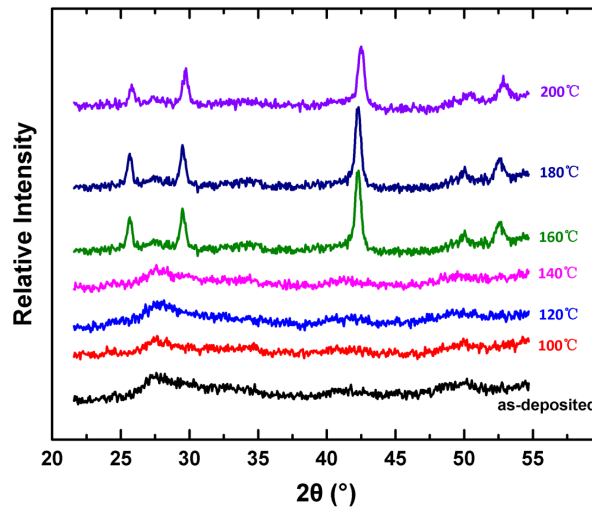


Figure 2.16: XRD patterns for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  films annealed at different temperatures. Crystallisation temperature can be determined to be between 140°C and 160°C. Pattern was collected in grazing incidence ( $\theta = 3^\circ$ ) with a  $\text{Cu-K}_\alpha$  radiation (1.54 Å).

More precise measurement of  $T_x$  can be obtained using time-resolved XRD or *in-situ* electrical resistivity measurements. Fig. 2.17 shows the intensity of the diffracted XRD peaks as a function of temperature for a 50 nm thick GST film using time-resolved XRD [45]. The film crystallisation happens at about 155°C where the metastable face-centred cubic crystalline phase peaks can be clearly observed. This matches the  $T_x$  range obtained above. The film then undergoes another phase transformation into the stable hexagonal phase at about 370°C.

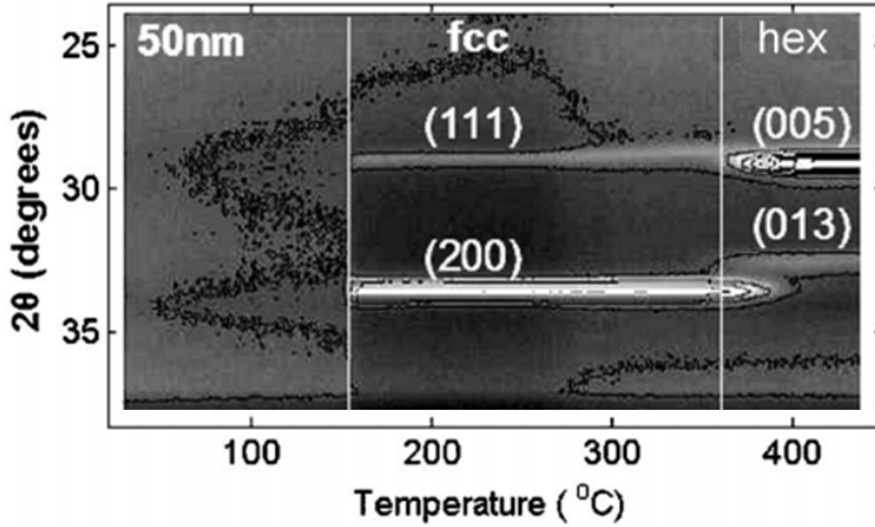


Figure 2.17: Time-resolved XRD peak intensity for 50 nm  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film. Reprinted from [45].

Crystallisation temperature is found to be strongly dependant on several factors such as film thickness, heating rate, interfacial layers, material composition and etc. The dependence of  $T_x$  on film thickness was investigated where a strong increase was observed when the film thickness of phase change material was reduced below a certain thickness as shown in Fig. 2.18 [45].

This increased  $T_x$  can be fitted by an exponential function [93] of the form:

$$T_x = T_{ax} + (T_{melt} - T_{ax}) e^{-d/C} \quad (2.6)$$

where  $T_x$  is crystallisation temperature for the thin film,  $T_{ax}$  is crystallisation temperature of the bulk material or a thick film,  $T_{melt}$  is the melting point of the material,  $d$  is the film thickness and  $C$  is a fitting constant. This thickness dependent crystallization mechanism can be explained by the increased interfacial energy which leads to the increase of the nucleation barrier. This has larger influence on nucleation-dominated materials than growth-dominated materials as less and less bulk material is available

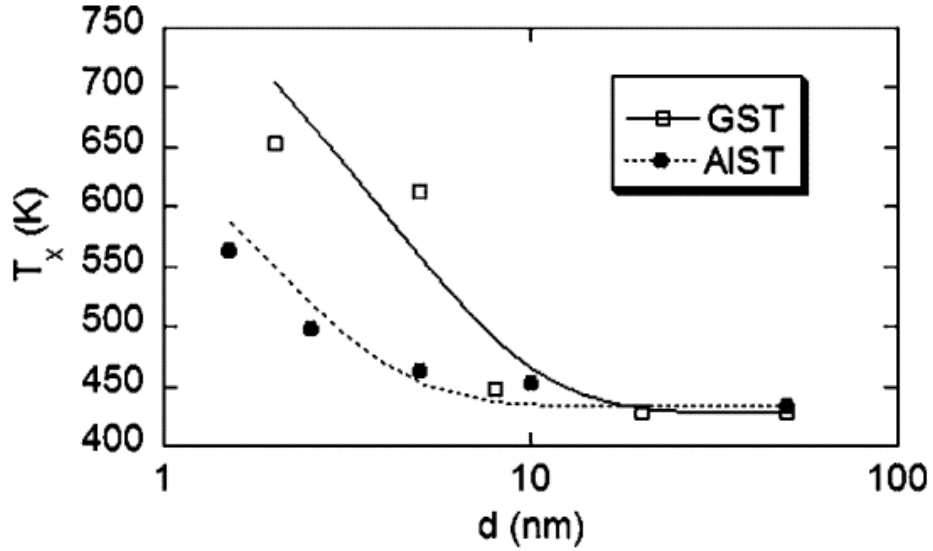


Figure 2.18: Crystallization temperature as a function of film thickness for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and In-doped  $\text{Sb}_2\text{Te}$  (AIST). The lines are fits according to Equation 2.6. Reprinted from [45].

for nucleation to happen as the film become thinner and thinner [45]. In addition, the change of crystallisation kinetics in ultra-thin films affect the crystallisation process [94]

A higher  $T_x$  is normally favourable for its application in memory device as it offers better thermal stability and data retention time. This increased  $T_x$  with thinner films indicates a promising prospect for the scalability of PCRAM technology.

Interfacial layers also play an important role in crystallisation temperature. However, the effects vary a lot for different interfacial materials. Raoux *et al.* observed a substantial increase of  $T_x$  with decreasing film thickness for the cladding materials Si, SiN, SiC, and TiN [95]. Opposite behaviour were observed for metallic interfaces where  $T_x$  decreased when the film thickness was reduced, with the exception of Pt.

The influence of heating rate on  $T_x$  was also studied. Fig.2.19 shows the resistivity dependence on temperature for the samples with a 30 nm  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film using *in-situ* exothermal electrical resistivity measurements [94]. The measurement was carried from 21 to 220°C at different heating rate and the crystallisation process can be characterized by the steep resistivity change. It indicates that, for the same film thickness,  $T_x$  increases with the heating rate increasing.

With respect to material composition, it was found that a large temperature range can be obtained by varying the elemental composition range in one phase change material [86]. With an increase of Ge ratio in the GeSb alloy, a much higher  $T_x$  (up to 450°C) was observed. Besides, as-deposited and melt-quenched similar materials have also been found to have a large difference in  $T_x$  [96].

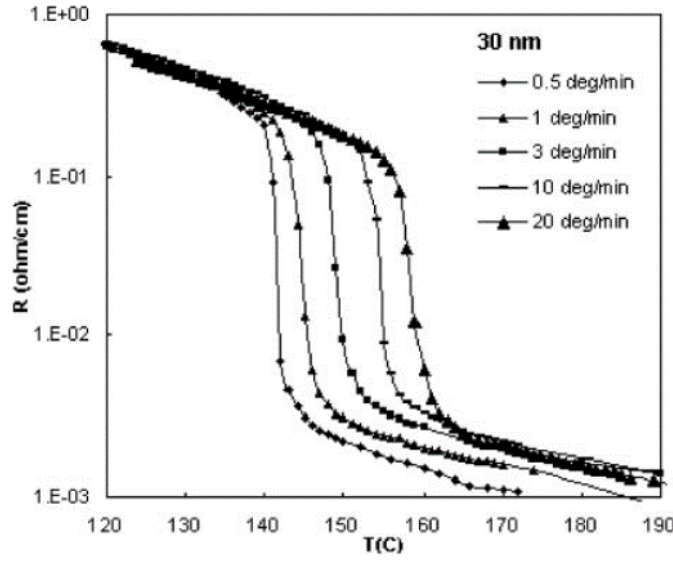


Figure 2.19: *in-situ* exothermal electrical resistivity measurements of a 30 nm  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film at different heating rate. Reprinted from [94].

The native drawback of relative low crystallisation temperature for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  has sparked an extensive search for novel active phase change materials with higher  $T_x$ . Among which, Ga containing binary or ternary materials have attracted large attentions due to their high crystallisation temperature. GaSb [97], ,  $\text{TeGa}_2\text{Sb}_{14}$  [98], Ga-Sb-Se [99] and Ga-Sb-Te [81] materials have all been studied with  $T_x$  higher than  $200^\circ\text{C}$  observed. Especially for  $\text{Ga}_2\text{Te}_3$ , where a high  $T_x$  of  $446.9^\circ\text{C}$  was demonstrated [100]. In addition, Ga:La:S film developed by Hewak *et al.* also display a high  $T_x$  above  $250^\circ\text{C}$  [83].

#### 2.5.4 Melting temperature

The melting temperature ( $T_m$ ) is a crucial parameter for PCRAM as it determines the power required to reset the device. Since the melt-quench (reset) process requires the highest power consumption, melting temperature becomes the power limitation for PCRAM. A low melting point is hence desirable for reducing the power consumption as indicated by Equation 2.5.

Typical phase change materials normally have a high melting temperature which is between  $500^\circ\text{C}$  and  $800^\circ\text{C}$ . For instance,  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  bulk material has a  $T_m$  of  $632^\circ\text{C}$ , GeTe bulk material has a melting point of  $725^\circ\text{C}$ . However, materials with lower  $T_m$  were also found in Se-Sb-Te family [101] and As-Te-Ge family [102], both with a melting point below  $400^\circ\text{C}$ . A melting temperature of  $383^\circ\text{C}$  of  $\text{GeTe}_4$  was also presented by Jiang *et al.* recently [58].

Apart from being a material property, melting temperature was also found to be a function of film thickness for thin films. This dependence was studied by Raoux *et*

*al.* using time-resolved XRD in which the melting temperature was defined by the disappearance of the XRD peaks [86]. A reduction of more than 100°C in melting point was observed when the GeTe film thickness was decreased to about 2 nm as shown in Fig.2.20. This size effect of a reduction in  $T_m$  is favourable for the application in PCRAM. An even stronger reduction of  $T_m$  was observed in GeTe nanowires by Sun and his colleagues [103]. The melting point of a single crystalline GeTe nanowire with diameters range from 50 - 80 nm was found to be 46% lower than that of its bulk counterpart (from 725°C to 390°C). The increase in the surface-to-volume ratio of atoms was involved to explain this size-dependent amorphization behaviour [87].

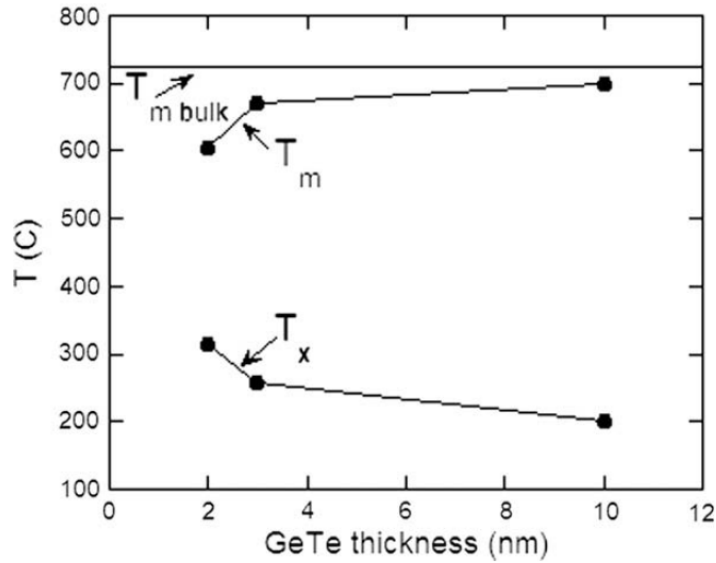


Figure 2.20: Melting temperature  $T_m$  and crystallisation temperature  $T_x$  of GeTe thin films as a function of film thickness compared to the melting temperature of GeTe bulk material ( $T_m$  bulk). Reprinted from [86].

### 2.5.5 Thermal conductivity

Thermal resistance, like melting temperature, also plays an important role in the power consumption of PCRAM as demonstrated in Equation 2.8. In a memory array, joule heating at a cell site may contribute to the adjacent cells due to high thermal conductivity of the material. Further increasing the array density will aggravate this problem, eventually leading to data loss. Thermal isolation is therefore required to solve this so-called thermal cross-talk issue. From this standpoint, the adoption of materials with low thermal conductivity would be helpful. However, unlike previous parameters all of which have a strong dependence on the material composition, the thermal conductivity was found to be relatively stable for various phase change materials. For materials with

stoichiometries between  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and  $\text{GeTe}$ , the thermal conductivity was found between 0.15 and 0.35 W/mK and between 0.5 and 2.0 W/mK for amorphous phase and crystalline phase, respectively [104].

Thermal boundary resistance (TBR) is a measure of an interfacial resistance to thermal flow. When an energy carrier attempts to traverse the interface, scattering will occur due to the differences in electronic and vibrational properties in different materials. TBR exists even at atomically perfect interfaces and proves to be an effective additional thermal insulation. It was found to have strong influences on the device temperature profile and programming current [105, 106, 107]. Fig.2.21 shows the simulated temperature distributions for a cell with no TBR and one with a TBR of  $50 \text{ m}^2\text{K/GW}$  during reset programming [108]. The incorporation of TBR reduces the temperature gradient in the lateral direction and enforces a temperature profile which minimizes overheating in the center of the active regions. This facilitates the formation of an amorphous volume which completely encapsulates the bottom electrode, resulting in a minimum reset current. The combined effects of favourable temperature profile and increased effective thermal resistance can lead to a reduced programming current [109, 110, 111].

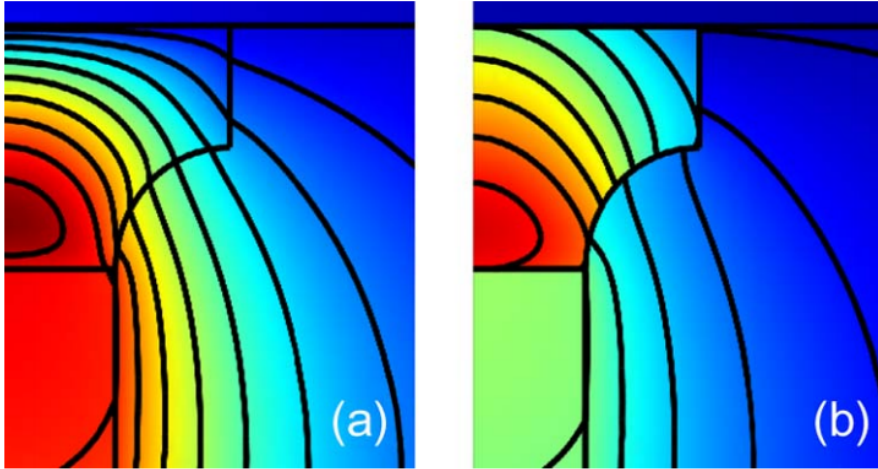


Figure 2.21: Temperature profiles for reset simulations with  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thickness of 50 nm. (a) No TBR is applied between the  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  interfaces. (b) Result of a TBR of  $50 \text{ m}^2\text{K/GW}$ . The temperature scale is the same in each figure. The peak temperature in (a) is 1092 K with a programming current of 1.6 mA, and the peak temperature in (b) is 1015 K with a programming current of 1.2 mA. Reprinted from [108].

It is also suggested that a  $10 \text{ m}^2\text{K/GW}$   $\text{Ge}_2\text{Sb}_2\text{Te}_5\text{-SiO}_2$  thermal boundary resistance corresponds to the thermal resistance of about 10 nm  $\text{SiO}_2$  layer as shown in Fig.2.22 [112]. TBR engineering is therefore considered as a key factor for PCRAM performance, especially in nanoscale.

Along with the engineering of TBR, another way of lowering programming current is through novel design of cell structures. Confined cell designs were found to enable

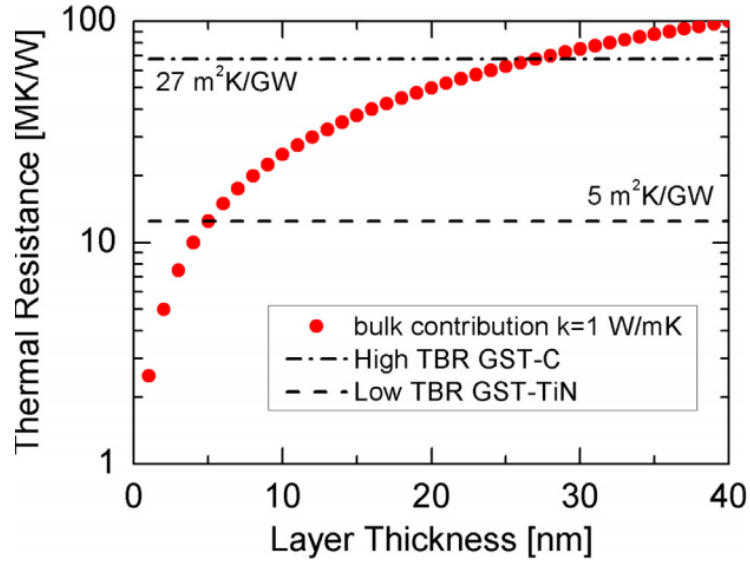


Figure 2.22: Thermal Boundary Resistance of typical interfaces compared to bulk thermal resistance of  $\text{SiO}_2$  layers with thickness reported on the x-axis. Reprinted from [30].

dramatical reduction of programming current together with enhanced reliability and scaling prospects [113, 114, 115, 116]. This is the structure will be mainly adopted in this thesis.

### 2.5.6 Resistivity in both phases

As chalcogenide semiconductors, phase change materials have different band diagrams in the crystalline and amorphous phases as shown in Fig.2.23. It is clear that amorphous phase has a larger energy gap compared with crystalline phase. For  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ , the band-gap for the amorphous phase is 0.7 eV while for the crystalline phase it is 0.5 eV [28]. More importantly, unlike in crystalline phase where the band-gap and conduction/valence bands are clearly distinct, the amorphous phase has a band gap with a large concentration of localised states. As a result, the Fermi level  $E_F$  has been pinned around mid gap and the conduction in amorphous phase is dominated by Poole-Frenkel (PF) transport among the localised states in the forbidden gap, with a relatively large activation energy and high effective resistivity [117]. On the other hand, the crystalline phase has a conventional p-type semiconductor band diagram. The possible reason for p-type is believed to be the vacancy-related states acting as acceptors [28].

The resistance in both crystalline phase and amorphous phase are essential parameters for phase change memory device performance. A high on/off ratio is favourable for its application since it not only means a good read margin, but also provides the potential for multiple bits application [119]. Nevertheless, the crystalline phase resistances should also

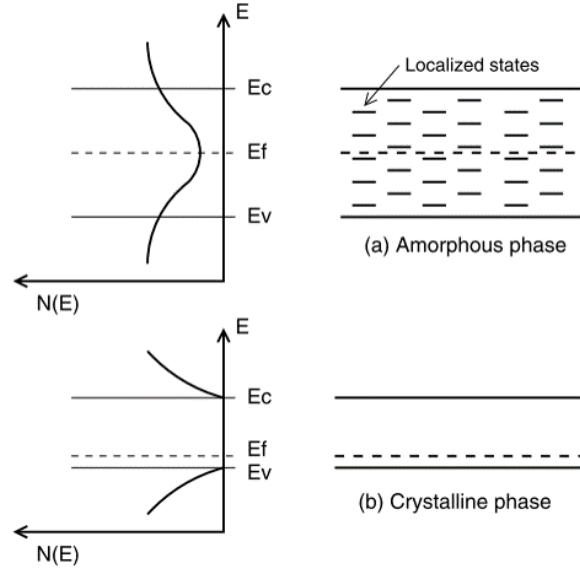


Figure 2.23: Schematic drawing of the band diagrams for a chalcogenide semiconductor in either the crystalline (a) or the amorphous (b) phase. Reprinted from [118].

be relatively high since it helps reduce the reset current by a larger voltage drop across the phase change material. Note that the as-deposited amorphous material has a higher resistance compared with its melt-quenched amorphous material. While for practical application, only resistance of melt-quenched amorphous materials is relevant. Both resistances are strongly dependent on materials as shown in Fig.2.24. The resistivities can also be manipulated easily by doping different type and amount of dopants as discussed above. However, no significant dependence on film thickness was observed for both resistivities. A small increase of amorphous phase resistivity was presented by Wei *et al.* when the  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film thickness was reduced from 100 nm to 3.5 nm [94], but it is insignificant compared with the on/off ratio which has several orders of magnitude between the amorphous and crystalline phases. Cheng *et al.* also investigated the thickness dependence for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  films, although the resistivities for different films varied significantly, the actual on/off ratio remained constant as shown in Fig.2.25 [120].

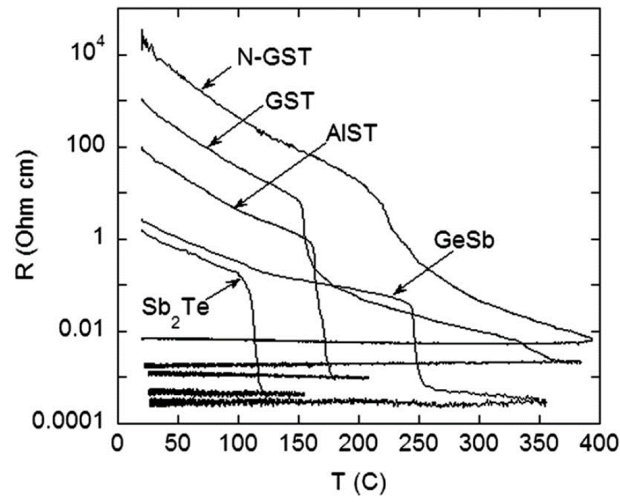


Figure 2.24: Resistivity as a function of temperature for 50 nm blanket films of GST, N-GST, GeSb,  $Sb_2Te$ , and AIST. Reprinted from [65].

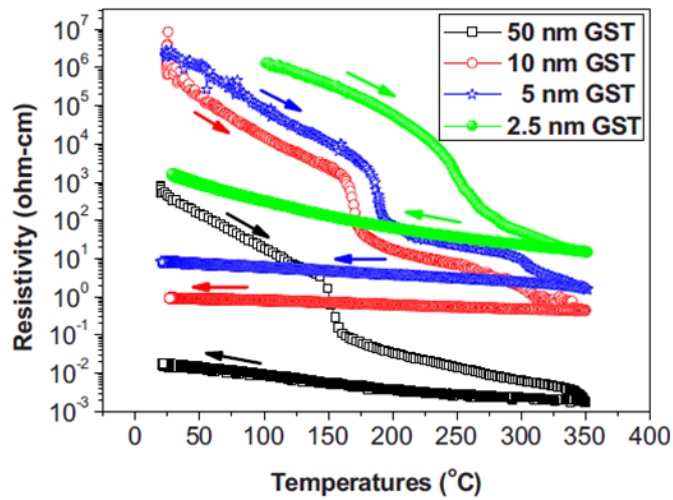


Figure 2.25: Resistivity as a function of temperature for  $Ge_2Sb_2Te_5$  films of various thickness. Reprinted from [120].



## Chapter 3

# Tools and Techniques

### 3.1 Fabrication

#### 3.1.1 Sputtering

Sputtering is a method of depositing thin films onto a substrate by eroding a material from the sputtering target. The working principle for sputtering is shown in Fig.3.1(a). It is achieved by bombarding the target surface with ions under high voltage acceleration. As a result of the ion impingement, atoms will be ejected from the target surface due to the momentum transfer by the impinging ions. The ions are formed from a glow discharge process where inert gas atoms are ionised by an electric discharge to form plasma. Plasma is defined as a gas with charged and neutral particles such as electrons, positive ions, atoms and molecules and is neutral overall. In most cases, plasma is created by argon gas which is fed into the sputtering chamber. During the sputtering process, the sputtering target is negatively biased (typically up to few hundred volts) to attract the ionised  $\text{Ar}^+$  ions from the plasma which leads to the collision on the target surface. The ionised argon ions also help to produce more secondary electrons for further ionization of the sputtering gas. It is essential to keep a sufficient ionization rate in order to sustain a stable plasma. The ionization rate inside the chamber is significantly influenced by the gas pressure. A higher gas pressure will cause more collision and consequently increase the deposition rate. However, we should note that at very high pressure, the deposition rate will be decreased since the target atoms will get scattered before even reaching the surface. Hence, an optimised gas pressure should be found to achieve the highest deposition rate.

Sputtering enjoys a variety of advantages. It enables uniform film deposition over a large area with good film adhesion. The deposited film properties can be easily tuned by adjusting the parameters such as gas ratio, gas pressure, etc.. In addition, formation of new alloys can also be realised in sputtering by simultaneous sputtering of multiple

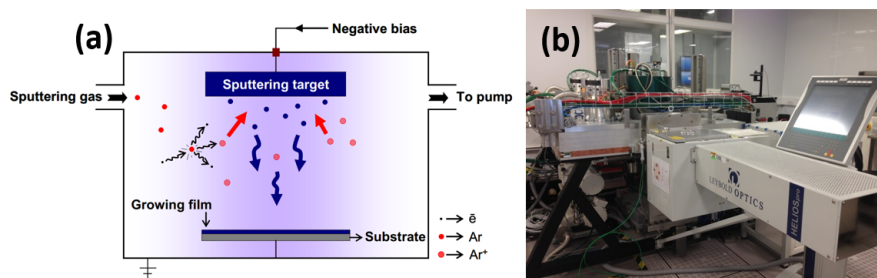


Figure 3.1: (a) A typical sputtering system. Reprinted from [39]; (b) A Leybold Optics (HELIOS Pro XL) system.

targets. All these merits have made sputtering one of the most powerful techniques in modern manufacturing, with more surfaces coated in more industries than ever before. From semiconductors to credit cards; from compact discs to auto parts; sputtering is adding new value to a growing list of products every day. Sputtering is also the most popular deposition technique in fabricating phase change memory devices. In this thesis particular, sputtering has been employed to deposit both the chalcogenide phase change material ( $\text{Ge}_2\text{Sb}_2\text{Te}_5$ ) as well as the device electrode (TiN) and insulator ( $\text{SiO}_2$ ). However, it is worth mentioning that two different types of sputtering are adopted. A more conventional RF sputtering is used for the deposition of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film where a single composition  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  target is bombarded to achieve a stoichiometric  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  layer. For the deposition of TiN and  $\text{SiO}_2$ , a plasma assisted magnetron sputtering is utilized by a Leybold Optics (HELIOS Pro XL) system (shown in Fig. 3.1(b)). This process combines reactive middle frequency sputtering with an additional RF plasma source in which elemental targets (e.g. Ti and Si) is used together with RF plasma sources (e.g.  $\text{N}_2$  and  $\text{O}_2$ ) to form desired films. Details of these sputtering processes can be found in Section 4.2.

However, sputtering also suffers obvious drawbacks such as expensive set-up and poor conformality. More importantly, sputtering does not allow selective deposition and also struggles in filling nanoscale features. These have significantly hindered its further application in particular areas especially for nanoscale deposition. Alternative deposition approaches hence need to be investigated.

### 3.1.2 Electrodeposition

Electrodeposition, also called electroplating or electrochemical deposition, is a process of coating an electrically conductive item (electrode) with a thin layer of metal by reducing dissolved metal cations using electrical current. The basic working principle of electrodeposition is shown in Fig. 3.2(a) where the electrode to be coated serves as a cathode and is placed into a solution with one or more metal salts. The metal salt ‘MA’

dissociates in the solution to form positively charged metal cations  $M^{n+}$  and negatively charged salt anions  $A^{n-}$ . When a potential difference is applied between the cathode and anode, positively charged  $M^{n+}$  cations are attracted to the negatively charged cathode electrode while the negatively charged  $A^{n-}$  anions are attracted to the positively charged anode electrode. A electrical circuit is hence formed between both electrodes and solution.  $M^{n+}$  cations are then reduced to the metallic form  $M$  and deposited onto the cathode.

Electrodeposition, although a relative new deposition technique for the semiconductor industry, has attracted attention as an alternative for semiconductor deposition due to its several advantages over conventional deposition methods. The most attractive feature for electrodeposition is its simplicity and low cost. It is usually carried out at room-temperature in normal laboratory conditions without requiring a vacuum system. It allows deposition of a wide range of materials and also enables an extensive control over films properties. More importantly in this work, electrodeposition is used to deposit ternary GeSbTe phase change materials due to its excellent spatial selectivity (deposition only occurs in contact with the electrode). This removes the requirement for lithographical definition of the phase change memory. Hence higher aspect ratio, confined cell structures in which the phase change memory is in the trench of the bottom electrode instead of on top of the trench become feasible. The home-made electrodeposition system in this thesis is placed in a glovebox as shown in Fig.3.2(b). Details of the specific non-aqueous electrodeposition used in this work for the deposition of GeSbTe materials are described in Chapter 5.

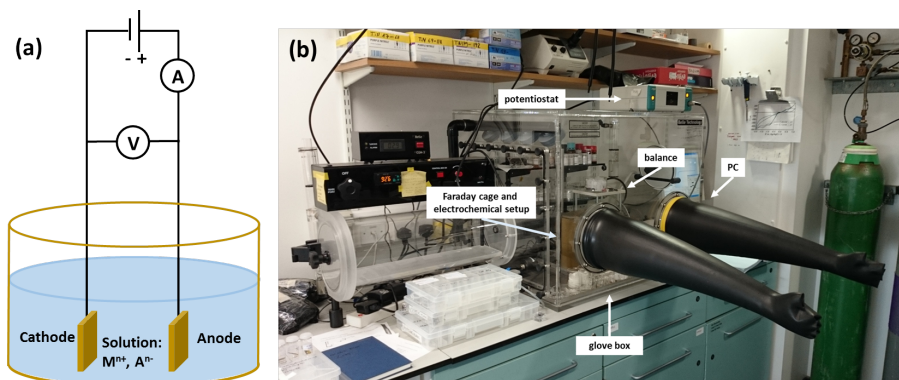


Figure 3.2: (a) Schematics of an electrolytic cell for plating metal ‘M’ from a solution of the metal salt ‘MA’; (b) The set-up of the CVD system used in this thesis.

Cyclic voltammetry is generally used to study the electrochemical properties of an analyte in solution. In a cyclic voltammetry experiment, the working electrode potential is ramped linearly versus time until the set potential is reached, and the working electrode’s potential is ramped in the opposite direction to return to the initial potential. Fig.3.3 shows a typical cyclic voltammogram for electrodeposition of Sb in this work. It

is characterised by a steep deposition onset at negative voltage where the  $\text{Sb}^{3+}$  species start reduce to the Sb elements. The deposition remains when the voltage becomes positive where the oxidation of Sb elements starts. It is worth mentioning that no deposition is made after one cyclic voltammetry scan. In actual deposition process, a fixed voltage is applied and deposition time is used to control the resultant film thickness.

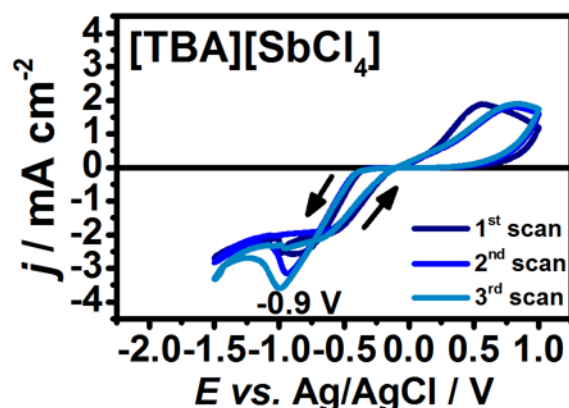


Figure 3.3: Cyclic voltammograms of  $0.01 \text{ mol dm}^{-3}$   $[\text{TBA}][\text{SbCl}_4]$  in dichloromethane containing  $0.1 \text{ mol dm}^{-3}$   $[\text{TBA}]\text{Cl}$  as the supporting electrolyte measured on masked TiN electrodes. The potential scan rate was  $50 \text{ mV s}^{-1}$ . Deposition experiments and graph were taken by Dr. Gabriela P. Kissling.

### 3.1.3 Chemical vapour deposition (CVD)

CVD can be defined as the deposition of a thin film on a heated surface in a chamber from the reaction of vapour-phase precursor(s). The precursor gas or gases are flowing into the chamber and the chemical reactions occur on the heated surface or in vapour phase above the substrate surface. This is also accompanied by the production of chemical by-products which are exhausted out of the chamber along with unreacted precursor gases. There is a variety of CVD techniques available nowadays based on different variants. The process can be carried out in hot-wall reactors and cold-wall reactors, at sub-torr total pressures to above-atmospheric pressures, with and without carrier gases, and at temperatures ranging from  $200 - 1600^\circ\text{C}$  [121]. Particular variants are plasma enhanced CVD (PECVD) and metal organic CVD (MOCVD) in which enhancements like plasma and metal organic precursors are applied. CVD has been implemented in numerous deposition processes for integrated circuit manufacturing such as the deposition of polysilicon, silicon dioxide, silicon nitride, metal nitrides and etc..

As a deposition method, CVD enjoys a number of advantages. One of the primary advantages lies in its conformal deposition profile, i.e., the film thickness on the sidewall of features is comparable to the thickness on the top. This is especially beneficial when

comparing with the conventional sputtering technique which suffers a relatively poor conformity when depositing phase change materials. Besides, CVD enables depositions of a wide variety of materials with very high purity. On the other hand, one major disadvantages for CVD is the fact that films are usually deposited at elevated temperatures which limits the kind of substrates that can be deposited on. Furthermore, it leads to stresses in the film deposited on materials with different thermal expansion coefficients and might cause mechanical instability of the films deposited. In addition, some CVD precursors can be highly toxic, explosive, or corrosive and the byproducts can also be hazardous, which require extensive engineering controls.

CVD has been used in this thesis to deposit binary chalcogenides where a home-made set-up is used as shown in Fig.3.4. This set-up consists of a commercially available furnace and a closed-end silica tube in which both precursors and substrates are loaded (Fig.3.4(b)). Details of CVD experiments can be found in Section 6.2.3.

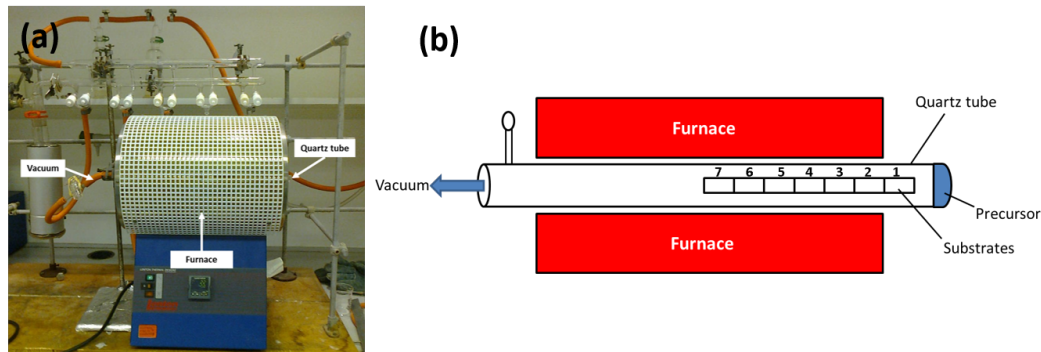


Figure 3.4: (a) Set-up of the CVD system used in this work; Schematic representation of the set-up (topview).

### 3.1.4 Photolithography

Photolithography (also known as optical lithography or UV lithography) is a process used in microfabrication to pattern Si wafers. It uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical on the substrate. These chemicals, usually termed resist or photoresist, will be either structurally weakened or strengthened by interaction with radiation. The conventional photolithography process consists of three main steps as listed below:

**Resist coating** The sample is covered with resist by spin coating. A couple of drops of resist is dispensed onto a pre-cleaned sample. The sample is then spun rapidly to spread the resist over the wafer, producing a uniform layer. The spin coating typically runs at 1000 to 6000 rpm for 30 to 60 seconds, and produces a layer between 0.5 and 2.5 micrometres thick. Normally, a higher spin speed and a longer spin time will lead

to a thinner resist. Besides, the resulting thickness can also be controlled by choosing different resist. A Brewer Cee 2000 Spinner was used in this thesis to coat the resist. Preparation of the resist is concluded by a pre-bake, where the wafer is gently heated in a hotplate (Sawtech Hotplate in this thesis) to evaporate the resist solvent and to partially solidify the resist.

**Exposure** The resist coating is then exposed through a mask as shown in Fig.3.5(a). A high-quality photomask is made of a glass (quartz or soda lime) support with a patterned layer of chromium. The 2D pattern on the mask is transferred to the resist where it becomes a 3D physical pattern after development. For the exposure, three projection methods, contact, proximity and projection, can be used depending on the photolithography machine. For contact method, the mask and the resist on the sample are in physical contact. This minimises the loss of resolution but the mask can be easily damaged. The proximity mode, on the other hand, leaves a 3 - 50  $\mu\text{m}$  gap between the mask and the sample to protect the mask while a loss of resolution from the light diffraction in the gap is a trade-off. Projection or stepper lithography is more widely used in modern lithography system in which a demagnified image of the mask is projected, with the aid of a lens, onto the photoresist. This method has a high resolution while no contact needs to be made between the mask and the sample. However, it does have a limited field of view and hence a ‘step and repeat’ is required for exposure of a whole wafer.

The resolution for photolithography is limited by the light diffraction and can be expressed by the following equation:

$$R = k_1 \cdot \frac{\lambda}{NA} \quad (3.1)$$

where  $R$  is the resolution and is defined by the minimum half-pitch that can be obtained in the resist after exposure and development,  $\lambda$  is the light wavelength and  $NA$  is the numerical aperture,  $k_1$  is an empirical factor which incorporates any variables except the wavelength and the  $NA$  that can improve the resolution of the resist pattern. It is clear that for a higher resolution, a light with shorter wavelength should be used.

The amount of exposure on the resist is defined by exposure dose which is a product of exposure intensity and exposure time. It is worth mentioning here that features with different sizes have different optimised exposure doses to achieve the exact replica of features on the mask. Generally, a smaller feature requires a relative larger dose while a larger feature needs slightly smaller dose. However, since only one dose can be used for one exposure, this will inevitably incur different extend of over- and under-exposure for features with different sizes. In this work particular, circular and square features with

sizes ranging from  $1\text{ }\mu\text{m}$  to  $100\text{ }\mu\text{m}$  have been integrated in one mask design. It is hence difficult to achieve the exact replica of the all mask features onto resist. Normally, the exposure dose is optimized based on smaller features while leaving the larger feature slightly over-exposed. In this thesis, all photolithography exposures have been carried out using an EVG 620TB mask aligner (as shown in Fig.3.5(b)) under contact mode. This aligner is equipped with a 436 nm mercury line which gives a resolution of about  $1\text{ }\mu\text{m}$ .

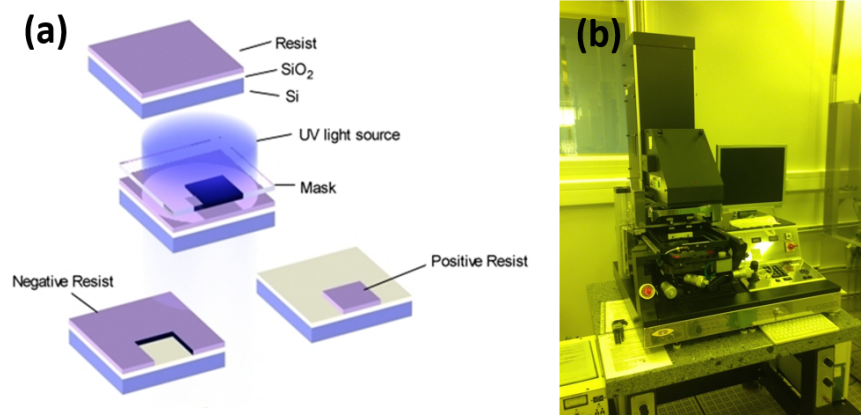


Figure 3.5: (a) Simplified process diagram for the photolithography technique. Reprinted from [122]; (b) A EVG620TB Mask Aligner.

**Development** During the exposure process, the resist undergoes a chemical reaction. Depending on the chemical composition of the resist, either the exposed region of resist will become less stable (positive resist) or more stable (negative resist) upon radiation. Hence during the developing process, either the exposed resist region for positive resist or the unexposed region for negative resist will be dissolved in the developer (Fig.3.5(b)). The photolithography process is usually followed by a process such as etching, lift-off and ion implantation, to transfer the resist pattern into the actual layer.

### 3.1.5 Electron beam (E-beam) lithography

E-beam lithography consists of the same three main steps as photolithography described above. The major difference is that, instead of using UV light radiation through a patterned mask, E-beam lithography utilises a focused beam of electrons to create the pattern directly on the E-beam sensitive resist point-by-point. The primary advantage of E-beam lithography is that it beats the diffraction limit of light and provides a much higher resolution (*ca.* 10 nm). Besides, since it is a maskless lithography, the patterning is flexible. However, E-beam lithography requires very sensitive and expensive machine

and also suffers the limitation of low throughput. The E-beam system used in this thesis is a JEOL JBX-9300FS E-Beam Lithography System.

### 3.1.6 Etching

Etching is used in microfabrication to chemically remove layers from the surface of a wafer during manufacturing. It is often divided into two classes, wet etching and plasma etching (dry etching). Each of these exists in several varieties. Wet etching equipment consists of a (heated) quartz bath, and plasma etching equipment is a vacuum chamber with an RF-generator and a gas system. In this work, all the etching used was plasma etching as it enables anisotropic etch profiles. For wet etching, an undercut of the sample will form due to its isotropic etching behaviour as shown in Fig.3.6.

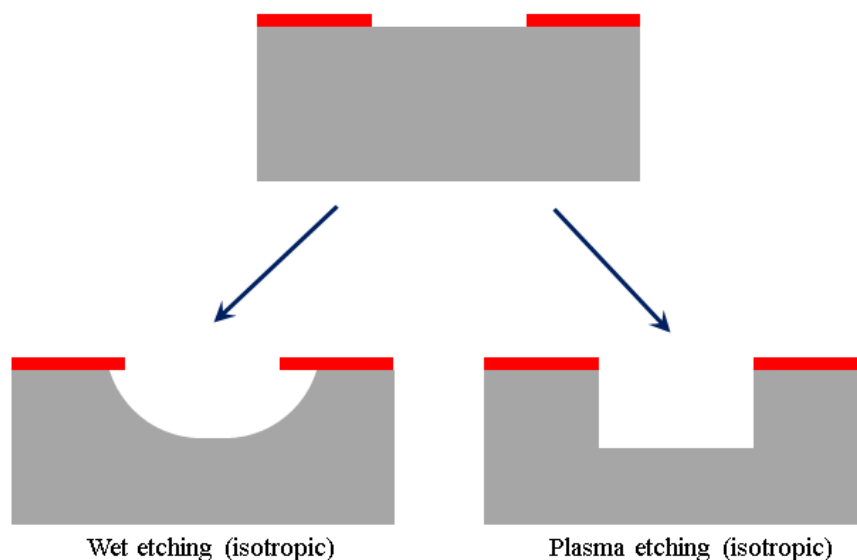


Figure 3.6: Wet and plasma etching profiles.

**Reactive-ion etching** Reactive-ion etching (RIE) is a typical plasma etching technology used in microfabrication. It uses chemically reactive plasma generated by electromagnetic field to remove the material on the sample. Fig.3.7(a) shows a typical RIE system in which gases are introduced through the top electrode while samples are placed on the powered bottom electrode. The plasma is initiated in the system by applying a strong RF (radio frequency) electromagnetic field (typically at a frequency of 13.56 MHz with a power of a few hundred watts) to the wafer platter. The oscillating electric field ionises the gas molecules by stripping them of electrons, creating a plasma. In a plasma discharge, a number of mechanisms for gas-phase reaction are operative and generate both ions and excited neutrals. The ionic species are accelerated by the RF field and impart energy directionally to the surface and the excited neutrals like  $CF^*$  can be very

reactive. Hence, it is a combination of chemical and physical processes. Due to the mostly vertical delivery of reactive ions, RIE can produce very anisotropic etch profiles which are critical for high-fidelity pattern transfer. The etch conditions in a RIE system depend strongly on the many process parameters, such as pressure, gas flows, and RF power. For example, a low pressure operation usually favours anisotropy because the bombardment is more directional. However, the tradeoff is a lower etch rate since a bigger pump or a reduced flow rate is required. RIE in this work is performed using a Plasmalab 80+ (Oxford Instrument) (shown in Fig. 3.7(b)) and has been predominantly used to etch  $\text{SiO}_2$  right after the photolithography process. Details of RIE process can be found in Section 5.2.2.

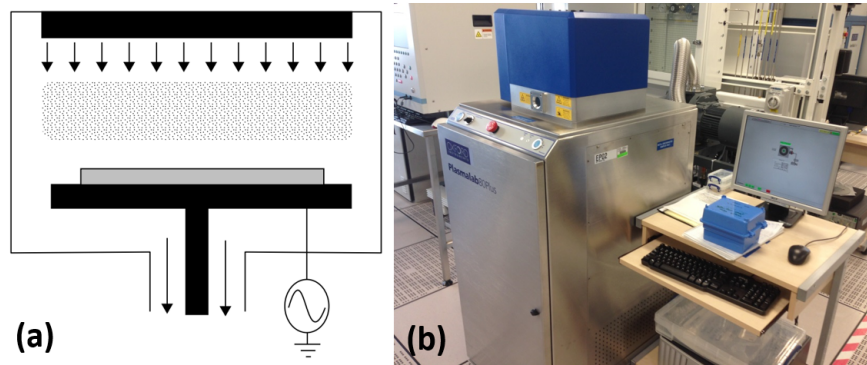


Figure 3.7: (a) RIE system: gas are introduced through the top electrode, samples are on the powered bottom electrode. Reprinted from [121]; (b) A Plasmalab 80+ RIE system.

**Ion beam etching** Ion beam etching (IBE) is a type of plasma dry etching process. Unlike RIE in which a chemical reaction is involved, IBE works by physically removing the target materials with a stream of accelerated ions. Ions are generated in a discharge chamber where atoms of a gas (Ar) are ionized by energetic electron bombardment similar to RIE. These ions are then accelerated when passing through a negatively biased grid to form the ion beam. After acceleration, a neutralize filament is used to introduce electrons to balance the positively charged ions and prevent the build-up of positive charge on the working plate. In this case, the beam current and voltage can be independently controlled to obtain desired ion energy and beam current density. The etching happens when the ion particles bombard the surface of the target while it is mounted on a rotating holder inside a vacuum chamber. The ions strike the target materials while they rotate. This ensures uniform removal of waste material resulting in straight side walls in all features with zero undercutting. The substrate plate can be tilted to different angles with respect of the incoming ions, offering further control over the sidewall profile. The substrate and plate are cooled by a dedicated chiller and helium is used as a conductive medium to transfer heat during etching. IBE owns the

advantage of high uniformity and repeatability and the ability to shape sidewall profile. It can serve as a universal etching solution to all materials due to its physical etching nature. However, note that this also results in a poor selectivity of IBE compared with RIE, and generally, a low etch rate. A second type of IBE, Reactive IBE (RIBE) is available, in which chemical reactive gas such as  $\text{SF}_6$ ,  $\text{CHF}_3$  can be added to the inert gas to create reactive gas. Using chemically reactive gas, etch rates and selectivity can be improved. In this thesis, IBE has been specifically chosen to perform etch on  $\text{Ge}_2\text{Sb}_2\text{Te}_2$  layer due to its high uniformity and non-selectivity. This model adopted is a Ionfab 300Plus Ion Beam System (Oxford Instrument). More details of the etching process can be found in chapter 4.

## 3.2 Characterisation

### 3.2.1 Scanning electron microscopy

Scanning electron microscopy (SEM) is one of the most important analytical techniques for materials and surface analysis. It utilises an energetically well-defined and highly focused beam of electrons to scan across the sample to obtain information. The electrons interact with the atoms of the surface layers producing signals that contain information about the surface topography, elemental composition and other properties such as electrical conductivity.

The process begins with the generation of an electron beam (with an energy range from 0.2 keV to 40 keV) typically from a thermionic electron source (e.g., tungsten filament) or a field emission gun (FEG). A series of electromagnetic lens then focuses the beam into a very fine spot with the size of 1 to 10 nm. A set of scanning coils or pairs of deflector plates are installed typically in the final lens to deflect the beam in orthogonal lateral directions so that the beam can scan over a rectangular area of the sample surface.

When the primary electron beam bombards the sample surface, the incident electrons will scatter both elastically and inelastically. During an elastic scattering event, the electron changes in direction while the kinetic energy remains the same. Back scattered electrons are produced by this type of scattering. On the other hand, for an inelastic scattering, part of the energy of the incident electron is transferred to its colliding partner and will produce diverse effects as listed below:

1. Secondary electrons production: Produced from the interaction between energetic electrons and weakly bonded valence electrons of the sample with an energy up to around 50 eV.

2. Characteristic X-ray radiation: When an inner shell electron is kicked out by an incident electron, its vacant state will then be filled by another electron from a higher shell and hence emit an X-ray photon.
3. Auger electron production: The energy from the refilling of the vacant state is simultaneously transferred to another electron that leaves the specimen as an Auger electron.
4. Cathodoluminescence: Visible light fluorescence from the recombination of electron-hole pairs induced by excitation of electrons in the valence band during inelastic scattering in a semiconducting sample.
5. Phonon excitation

The total region of the sample that interacts with the primary electrons is called the interaction volume which has a teardrop shape which extends from less than 100 nm to around  $5\text{ }\mu\text{m}$  into the surface as shown in Fig.3.8. The size of the interaction volume depends on the electron's landing energy, the atomic number of the specimen and the specimen's density.

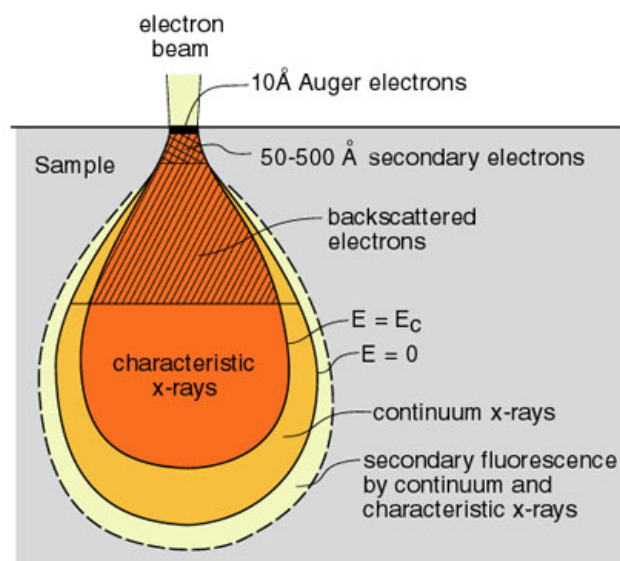


Figure 3.8: Interaction volume showing the regions of various electron-specimen interactions. Reprinted from [123].

For SEM, the most common imaging mode collects the low energy secondary electrons. Since these electrons have much less energy than the primary electrons, they can only emerge from the top layer (few nanometres) of the sample, and hence provides a high resolution. Normally, secondary electrons are detected by a scintillator-photomultiplier system known as the Everhart-Thornley detector. The electrons strike a scintillator which then emits light. The light is transmitted to a photomultiplier which converts the photons in an electrical signal that can be amplified. The incident electron beam scans

the sample point-by-point, while for each point, the number of the secondary electrons is counted and stored in the computer system. The image displayed is therefore a distribution map of the intensity of the signal being emitted from the scanned area of the specimen; that is, the brightness of the signal depends on the number of secondary electrons reaching the detector. Since the number of secondary electrons that escapes from the specimen depends strongly on the angle of the beam with the specimen surface, SEM is very useful in studying the surface feature (topography) of a sample. The SEM mainly used in this thesis is a JSM-7500F (JEOL) Field Emission Scanning Electron Microscope. This enables a good resolution of 2 nm with several scanning mode suitable for different surfaces.

### 3.2.2 Energy dispersive X-ray spectroscopy

Energy dispersive X-ray spectroscopy (EDX or EDS) is an analytical technique used to study the chemical composition of a sample. By analyzing X-rays emitted from the sample, it is able to perform both qualitative and quantitative analysis of the material. Since EDX is used in conjunction with a scanning electron microscope (SEM) or transmission electron microscope (TEM), analysis can be performed on a very small amount of materials, or a very small part of a larger sample. The qualitative analysis is based on the fundamental principle that each element has a unique atomic structure allowing X-rays that are characteristic of an element's atomic structure to be identified from one another. When the sample is bombarded with a collimated, high energy electron beam, some inner shell electrons of the material will be knocked out while the vacancies left behind will be ultimately filled by outer shell electrons. The energy lost during this electron transition from outer shell to inner shell is released as X-rays which can be collected by a detector and subsequently transformed into a voltage proportional to the X-ray energy. Since the energy release depends on the energy differences between the atomic orbitals, it enables us to find out which elements are present in the material. Quantitative analysis can be performed by measuring the number of emitted X-ray of each energy and provides us the information of relative proportions of the elements. Fig.3.9 demonstrates possible electron transitions between different energy levels in the atom after being struck by an electron beam. The real situation, however, is more complex than this figure since each of the L and M orbitals are in fact composed of subshells with finer energy separations. This leads to a large number of possible transitions and hence gives rise to a number of line series. The K series of lines are most frequently used for lighter elements, while for heavier elements, the L and M series of lines are used since the energy required to knock out a K-shell electron will increase with the atomic number.

The lateral resolution of EDX is predominantly determined by the size of the interaction volume beneath the surface of the sample. Unlike the secondary electrons, where only

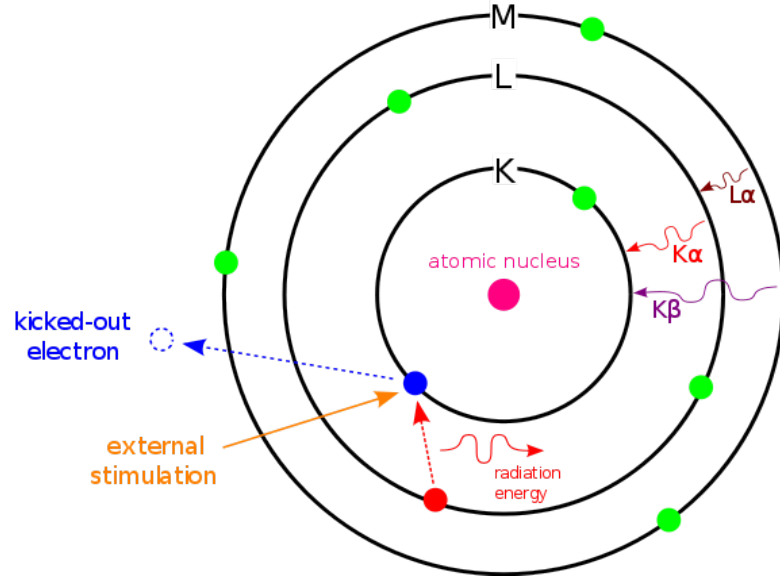


Figure 3.9: The possible electronic transitions that can lead to X-ray emission from an individual atom. Reprinted from [124].

the ones generated close to the surface can escape from the sample, X-rays can escape from the sample even if they are generated in the deeper area. This leads to a limited lateral resolution unless the sample is very thin.

The EDX used in this thesis is a x-act 10 mm<sup>2</sup> Silicon Drift Detector (Oxford Instrument) operated by an INCAEnergy EDS X-ray Microanalysis System as shown in Fig.3.10(a). The system enables a lateral resolution of around 0.3  $\mu\text{m}$  and a energy resolution of 150 keV. A plot of an EDX measurement is shown in Fig.3.10(b). The measurement was carried out with a 20 kV accelerating voltage and 2.0 nA beam current on a standard PbTe sample with a nominal atom composition of 50% for each element. It is seen that there are multiple peaks for both lead and tellurium. Since they are both heavy elements with K series lines energy larger than 70 keV, only L and M shell electrons can be knocked out under this situation and detected by EDX. The chemical composition presented in the plot is calculated on the basis of the default standardization in INCA which lead to a 2% error comparing with this nominal standard PbTe.

It is worth mentioning that the performance of this EDX is significantly limited by these two resolutions. Detection of nano-scaled features can be challenging as the feature size approaches the lateral resolution. It is also difficult to deconvolve overlapped peaks from alloys consisting of two adjacent elements (e.g. SbTe) due to the limitation in energy resolution. Fig.3.11 shows a typical EDX measurement on a sputtered Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> film with a thickness of 300 nm, the ratio of Ge:Sb:Te was measured to be 2:2.3:6.3. The discrepancy between the nominal ratio and the measured ratio is possibly due to the limitations of EDX when dealing with thin film and adjacent peaks (Sb and Te in this

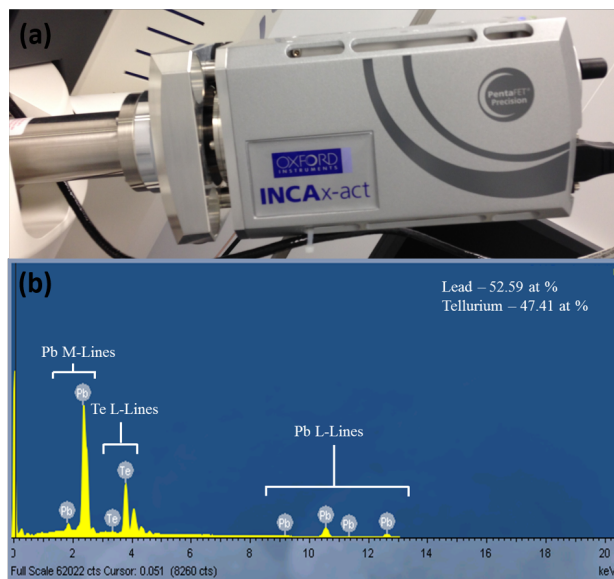


Figure 3.10: (a) A x-act 10 mm<sup>2</sup> Silicon Drift Detector (Oxford Instrument); (b) An EDX spectrum of PbTe with nominal composition. The peak positions are characteristic to the element and intensity is proportional to the quantity.

case). The difference between the resultant composition and the target composition in the sputtering process should also be considered.

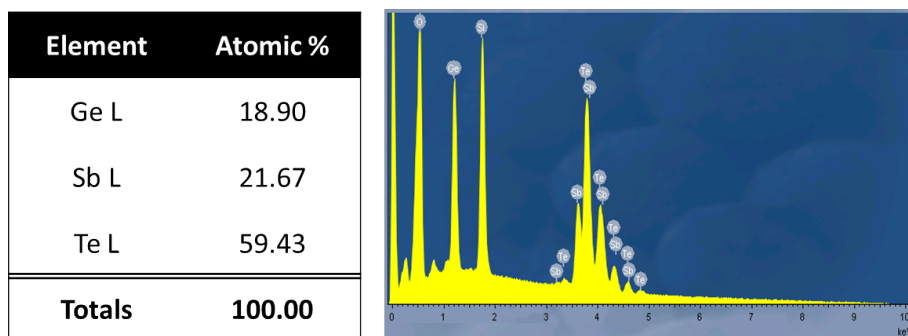


Figure 3.11: Energy dispersive X-ray of sputtered 300 nm Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> film on top of a SiO<sub>2</sub> film.

EDX is widely used in this thesis to investigate the compositional properties of the deposited chalcogenide phase change materials. To achieve better quantification, stoichiometric powder was purchased and measured as reference for each material deposited in this thesis. For Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>, standardized Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> target was used.

### 3.2.3 X-ray diffraction

X-ray diffraction (XRD) technique reveals information about the crystal structure, chemical composition and physical properties of a material [125]. It is based on the scattered

intensity of an incident X-ray beam hitting a sample as a function of incident and scattered angle, polarization, and wavelength or energy. Although the typical photon energies for X-rays are ranging from 100 eV to 100 keV, for the application of XRD, only hard X-rays (1 keV - 120 keV) should be used since the X-rays have short wavelengths (a few Å to 0.1 Å), comparable to the size of atoms. They enable probing the structural arrangement of atoms and molecules in a wide range of materials. The energetic X-rays can penetrate deep into the materials and provide information about the bulk structure. X-rays for XRD are produced by bombarding a stationary or rotating solid target with a focused electron beam accelerated across a high voltage field. Common targets used include Cu and Mo, which emit 8 keV and 14 keV X-rays with corresponding wavelengths of 1.54 Å and 0.8 Å respectively.

The generated X-rays will primarily interact with core electrons. When these X-rays collide with electrons, some photons from the incident beam will be deflected from the direction in which they originally travelled. If the collision only changes the momentum of the incident photon while the wavelength of the scattered X-ray photon is left unchanged, the process is called elastic scattering. These scattered X-rays will carry information about the electron distribution in the material and they are quantitatively measured in the XRD experiments to form diffraction patterns. While for inelastic scattering process (scattering X-rays with different wavelengths), the scattered X-rays only contribute to the background noise in a diffraction pattern.

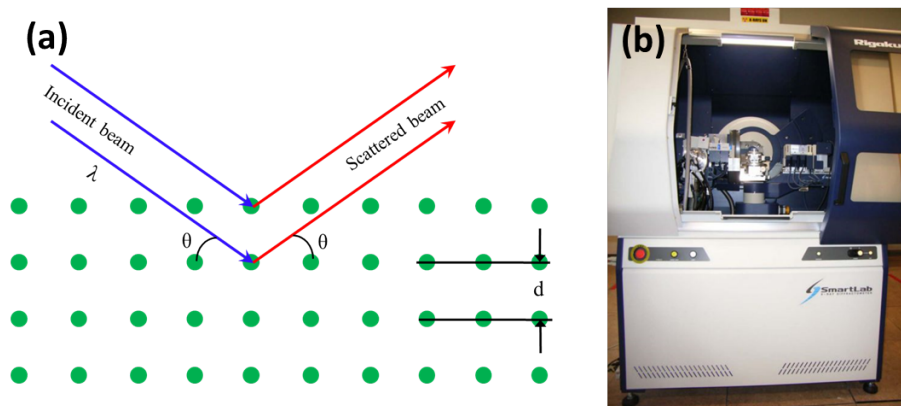


Figure 3.12: (a) Bragg's law; (b) A Rigaku SmartLab system.

The diffracted X-rays from different atoms can interfere with each other and lead to an intensity distribution which is modulated by this interaction. If the atoms have a periodic arrangement, such as in crystals, the diffracted waves will then have sharp interference maxima (peaks) with the same symmetry as the distribution of atoms. In this case, the measuring of this diffraction pattern will provide us the distribution of the atoms in a material. The corresponding peaks in XRD pattern are directly related to the atomic distance according to the Bragg's law as shown in Fig.3.12(a) and can be written as

$$n\lambda = 2d \sin \theta \quad (3.2)$$

where  $n$  is an integer representing the order of the diffraction peak,  $\lambda$  is the wavelength of incident X-ray and  $\theta$  is the scattering angle.  $d$  is the inter-plane distance which can be calculated from the equation. When recording the 2-D diffraction pattern, concentric rings of scattering peaks corresponding to the various  $d$  spacings in the crystal lattice can be observed. These scattering peaks can then be used to identify the underlying structure of the material based on their positions and intensities.

In addition, the crystal grain size  $\tau$  can also be obtained by using Scherrer's formula [126]

$$\tau = \frac{K\lambda}{B \cos \theta} \quad (3.3)$$

where  $K$  is the shape factor and has a typical value about 0.89.  $\lambda$  is the X-ray wavelength,  $B$  is the line broadening at half the maximum intensity (FWHM) in radians and  $\theta$  is the Bragg angle.

In order to understand the preferred orientation of the crystallites, texture coefficient can be calculated from each line in XRD pattern using Equation 3.4 [127]

$$C_{(hkl)} = \frac{I_{(hkl)i}}{I_{o(hkl)i}} \bigg/ \frac{1}{n} \sum_n \frac{I_{(hkl)n}}{I_{o(hkl)n}} \quad (3.4)$$

where  $C_{(hkl)}$  is the texture coefficient of the facet  $\{hkl\}$ .  $I_{(hkl)}$  is the intensity of the (hkl) reflection of the sample under analysis,  $I_{o(hkl)}$  is the intensity of the (hkl) reflection of a polycrystalline bulk sample and 'n' is the number of reflections taken into account. By using this equation, the preferred orientation of the facets can be understood. For facets with no preferred orientation,  $C_{(hkl)}$  is expected to be unity while for a preferred grown facet,  $C_{(hkl)}$  is expected to be higher than unity.

In this these, grazing incidence diffraction technique is used for all XRD measurements onto deposited thin films to investigate the crystallinity of the deposited chalcogenide materials. Compared with conventional powder XRD in which X-ray radiation has a large penetration depth, glazing incidence diffraction is performed at very low incident angle to maximize the signal from thin layers. One XRD system used in this work is a Rigaku SmartLab system (as shown in Fig.3.12(b)) which enables XRD measurements onto sub-hundred nanometre thin films. However, it is still inevitable for thinner films

to have low diffracted intensities compared to the substrate and background. In this case, careful background subtraction should be carried out during analysis.

Fig. 3.13 shows a typical XRD pattern for crystalline sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film with peaks assigned. The crystal structure corresponds to the rock-salt phase which is consistent with cubic space group  $\text{Fm}\bar{3}\text{m}$ . The lattice constant was calculated to be  $a = 6.035 \text{ \AA}$  (JCPDS file 54-0484 value for fcc GST:  $a = 6.037 \text{ \AA}$ ).

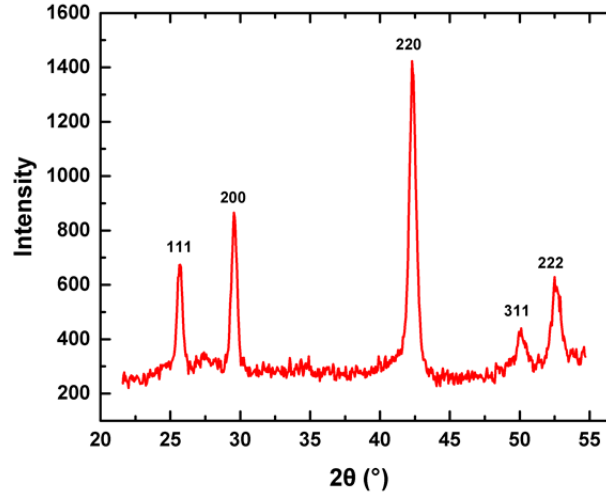


Figure 3.13: XRD pattern of a crystalline  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film giving a lattice parameter of  $a = 6.035 \text{ \AA}$ . Pattern was collected in grazing incidence ( $\theta = 3^\circ$ ) with a  $\text{Cu-K}\alpha$  radiation ( $1.54 \text{ \AA}$ ). Peaks were indexed using JCPDS file 54-0484.

### 3.2.4 Raman spectroscopy

Raman spectroscopy is a spectroscopic technique used to study the vibrational, rotational and other low-frequency modes in a system based on inelastic scattering of monochromatic light [128]. The photon of the monochromatic light, usually a laser source, are absorbed and then remitted by the system. Inelastic scattering happens when the frequency of photons in monochromatic light changes during interaction with the system. In consequence, the frequency of the remitted photons is shifted either up and down in comparison with the original monochromatic frequency and this is the so called Raman effect.

The Raman effect originates from the molecular deformation in electric field  $E$  determined by the molecular polarization  $\alpha$ . Consider the laser beam as an oscillating electromagnetic wave with electrical vector  $E$ , it induces an electrical dipole moment of  $P = \alpha E$  when interacting with the system and deforms molecules. In other words, this monochromatic laser light with frequency  $\nu_0$  excites molecules and transforms them

into oscillating dipoles which emit lights with three different frequencies as shown in Fig.3.14(a).

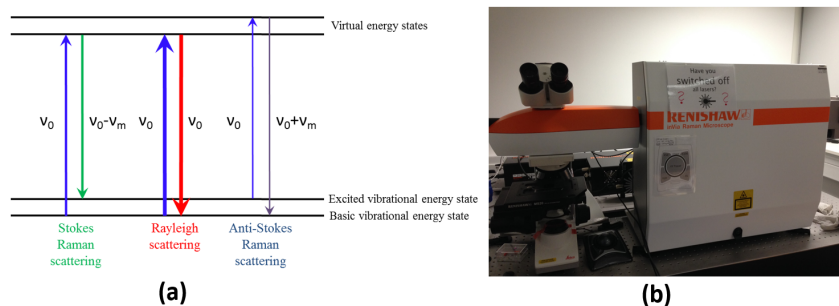


Figure 3.14: (a) Energy level diagram of the states involved in Raman signal; (b) A Renishaw inVia Raman microscope.

1. A molecule with no Raman-active modes (change in the polarizability of the molecule) is first excited by a photon with frequency  $\nu_0$  from basic vibrational state to a virtual energy state. After it relaxes, it will return to the original vibrational state and emit lights with same frequency  $\nu_0$  as the excitation source. This type of interaction is called Rayleigh scattering and it consists of about 99.999% of all incident photons.
2. A photon with frequency  $\nu_0$  is absorbed by a Raman-active molecule which is in a basic vibrational state during the time of interaction. Part of the photon's energy is transferred into the Raman-active mode with frequency  $\nu_m$  and left the frequency of emitted light to be reduced to  $\nu_0 - \nu_m$ . This type of interaction is called Stokes Raman scattering.
3. A photon with frequency  $\nu_0$  is absorbed by a Raman-active molecule which is already in a excited vibrational state during the time of interaction. Excessive energy of excited Raman-active mode can be released and leads to an increased frequency of  $\nu_0 + \nu_m$  for the emitted light after the molecule returns to the basic vibrational state. This interaction is called Anti-Stokes Raman scattering.

Note that only about 0.001% of the incident light will induce inelastic Raman signal with frequency  $\nu_0 \pm \nu_m$  which indicates a very weak signal and special measures should be taken to distinguish it from the predominant Rayleigh scattering (e.g. notch filters). Also, Anti-Stokes scattering has less intensity compared with Stokes scattering since there are much more molecules in the basic vibrational state than in the excited state according to the Boltzmann distribution. In addition, the Raman effect should not be confused with absorption (as with fluorescence) where the molecule is excited to a discrete energy level and the fluorescence effect should be eliminated during experiments.

Raman spectroscopy is used in this thesis to study the bonding and confirm the composition of the deposited materials. The Raman system used in this thesis is a Renishaw

inVia Raman microscope as shown in Fig.3.14(b). It equips with 3 multi-line lasers (532 nm, 633 nm and 754 nm) and a set of microscopes up to  $50\times$  which enables measurement onto features as small as  $1\ \mu\text{m}$ . Gaussian curves were used in this work to fit all Raman spectra in this work to extract peak information. Fig.3.15 shows a typical Raman spectrum for sputtered amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film. Two peaks positioned at  $124\ \text{cm}^{-1}$  and  $142\ \text{cm}^{-1}$  can be identified and correspond to the  $A_1$  mode of  $\text{GeTe}_{(4-n)}\text{Ge}_n$  ( $n = 1, 2$ ) and Sb-Te vibrations in  $\text{SbTe}_3$ , respectively. It helps the identification of the film composition. More detailed Raman analysis of GeSbTe film will be conducted in Section 5.3.2.

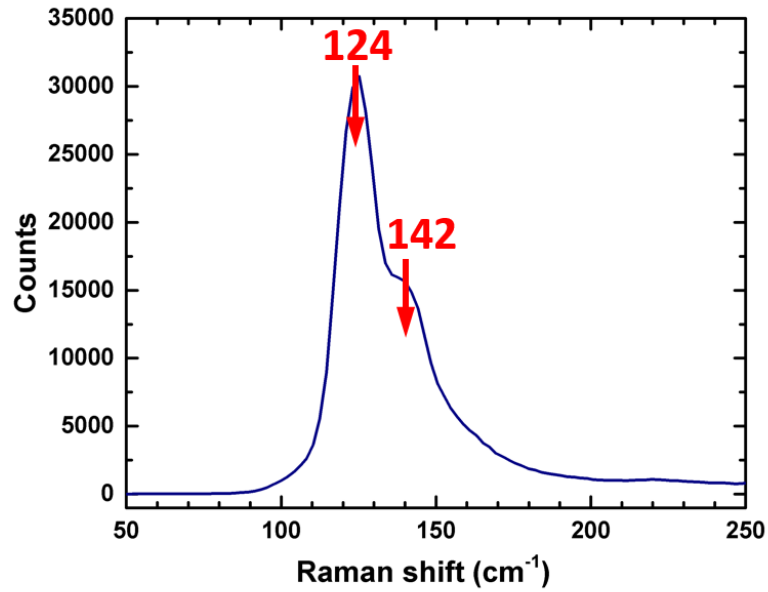


Figure 3.15: A typical Raman spectrum of a sputtered amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  film.

### 3.2.5 Spectroscopic ellipsometry

Spectroscopic ellipsometry measures a change in polarization as light reflects or transmits from a material structure. The polarization change is represented as an amplitude ratio  $\Psi$ , and the phase difference  $\Delta$ , both of which depend on the film properties and the technique can hence be used to determine the film thickness and optical constants in return. It is rapid, contactless and non-destructive and is an excellent technique to perform precise and accurate characterisation of a film thickness as well as optical constants.

The mathematical theory for ellipsometric analysis is based on the Fresnel reflection and transmission equations for polarised light encountering boundaries in planar multi-layered materials [129]. The ellipsometric measurement can be expressed by

$$\tan(\Psi) \cdot e^{i\Delta} = \rho = \frac{r_p}{r_s} \quad (3.5)$$

where  $r_p$  and  $r_s$  are the complex Fresnel reflection coefficients of the sample for p- (in the plane of incidence) and s- (perpendicular to the plane of incidence) polarised light. Ellipsometry measures the complex ratio  $\rho$  as a function of wavelength. For a bulk sample, the optical constant can then be directly inverted from the data measured using the Pseudo transforms by assuming the surface oxide and/or roughness effects are negligible. The transform is given as

$$\langle \tilde{n} \rangle = (\langle n \rangle + i \langle k \rangle)^2 = \langle \tilde{\varepsilon} \rangle = \langle \varepsilon_1 \rangle + i \langle \varepsilon_2 \rangle \sin(\phi)^2 \cdot \left[ 1 + \tan(\phi)^2 \cdot \left( \frac{1 - \rho}{1 + \rho} \right)^2 \right] \quad (3.6)$$

where  $\phi$  is the angle of incidence and  $\rho$  is the complex ratio in Equation 3.5. Both complex refractive index ( $\tilde{n}$ ) and dielectric function ( $\tilde{\varepsilon}$ ) are descriptions for optical properties and they are related to each other as shown in Equation 3.6. The complex refractive index ( $\tilde{n}$ ) consists of the index of refraction ( $n$ ) and extinction coefficient ( $k$ ). The index is related to the phase velocity of light in the material while the extinction coefficient is related to the absorption coefficient and describes the loss of wave energy to the material. On the other hand, the dielectric function also consists of two parts,  $\varepsilon_1$  and  $\varepsilon_2$ .  $\varepsilon_1$  represents the polarization of the material when an electric field is applied due to the creation of electric dipoles and  $\varepsilon_2$  represents the absorption in a material. A positive  $\varepsilon_2$  indicates an absorptive material while  $\varepsilon_2 = 0$  indicates a transparent material. Note that  $\varepsilon_1$  and  $\varepsilon_2$  are not independent but interrelated via the Kramers-Kronig (K-K) relation [130]. In this work, a M-2000 Ellipsometer (J.A. Woollam Co.) is used for all ellipsometric measurements.

Spectroscopic ellipsometry was used to measure the optical constants of both amorphous and crystalline (fcc)  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin films. After the raw data are obtained, a model has to be built up for the analysis of ellipsometric data. Generally, a Cody-Lorentz oscillator is used to model the  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  layer. And the surface layer is modeled with 50% void and 50% phase change layer in the Bruggemann effective medium approximation (EMA). The optical constants as well as the thickness can then be obtained by numerical fitting, starting with the initial estimates provided by the user. The results of fitted optical constants are shown in Fig.2.2 in Chapter 2.1.

### 3.2.6 Atomic force microscopy

Atomic force microscopy (AFM) is one of the primary forms of scanning probe microscopes (SPM) which consists of a broad group of instruments used to image and measure properties of material from the micro to the atomic level. SPM images are obtained by scanning a sharp probe across a surface while monitoring and compiling the probe-sample interactions to provide an image. The position of the probe, both vertically and laterally, is controlled by a scanner. For AFM specifically, the probe contains a sharp tip (typically less than  $5\text{ }\mu\text{m}$  tall and often less than  $50\text{ nm}$  in diameter at the apex) which is located at the end of a cantilever with a typical length of  $100$  to  $500\text{ }\mu\text{m}$ . During the scanning, the cantilever is bended or deflected due to the forces between the tip and the sample surface. These deflections are measured by a detector and consequently generate the map of surface topography by plotting the data point by point and line by line as shown in Fig.3.16(a).

The AFM used in this work is a Veeco Multimode Scanning Probe Microscope which is operated by a NanoScope V Controller as shown in Fig.3.16(b). It enables primary modes like tapping and contact modes which provide the topography image of a surface. Besides, several secondary modes are also available such as conductive-AFM (C-AFM) and magnetic force microscopy.

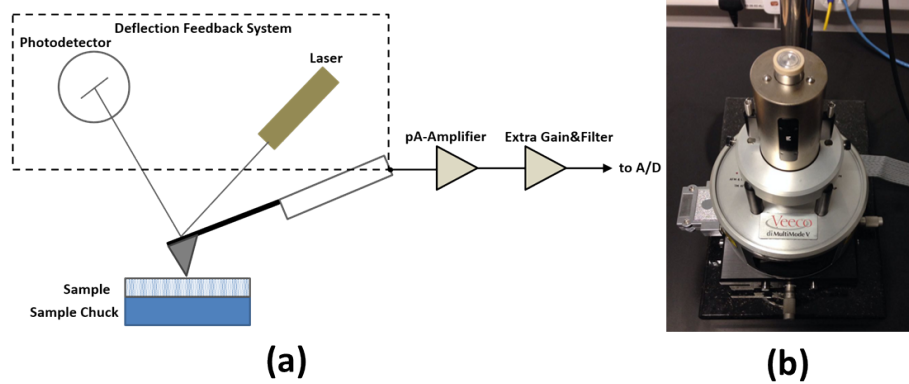


Figure 3.16: (a) Schematic of an AFM Block Diagram; (b) A Veeco Multimode Scanning Probe Microscope.

### 3.2.7 Van der Pauw method

Van der Pauw method is a technique used to measure the sheet resistance and the Hall coefficient of a sample and provide us with important properties such as material resistivity, material doping type, material majority carrier density as well the mobility of the majority carrier. The measurement of sheet resistance involves applying a current and measuring voltage using four small contacts on the circumference of a flat, arbitrarily

shaped sample with uniform thickness. The resistivity  $\rho$  is given by

$$\rho = R_S \cdot t \quad (3.7)$$

where sheet resistance  $R_S$  can be derived from several measurements (normally 4 or 8) that are made around the periphery of the sample with those four contacts.  $t$  is the film thickness.

Hall measurement is based on Hall effect in which a charged particle (electrons and holes in this case) travelling in a magnetic field will experience a Lorentz force which is proportional to the strength of the field as well as its travelling velocity [131]. For Hall measurement, the magnetic field is usually perpendicular to the travelling direction of the particle which leads to the strongest force

$$F_L = qvB \quad (3.8)$$

where  $q$  is the charge on the particle,  $v$  is traveling velocity and  $B$  is the strength of the magnetic field. In case of a semiconducting material, the velocity of the carrier is proportional to the current applied on the sample

$$v = \frac{I}{n_m A q} \quad (3.9)$$

where  $n_m$  is the carrier density,  $A$  is the cross-sectional area of the material and  $q$  here is the elementary charge. After an external magnetic field is applied perpendicular to the direction of current flow, the carriers which experience the Lorentz force will accumulate at one edge of the sample while the side of accumulation edge depends on the polarity of the carrier charge. The Lorentz force in this case can be written as

$$F_L = \frac{IB}{n_m A} \quad (3.10)$$

This accumulation will then create an electric field across the material due to the uneven distribution of charges resulting in a potential difference across the material known as Hall voltage  $V_H$ . The electric field force exerted on the carrier helps to counteract the Lorentz force to reach a balance where the current will only flow along the material. Hence, the strength of the electric field can be obtained and the Hall voltage can then be calculated as

$$V_H = wE = \frac{wIB}{qn_m A} = \frac{IB}{qn_m t} \quad (3.11)$$

where  $w$  is the width of the material and  $t$  is the material thickness. By measuring the Hall voltage, one can calculate the carrier density  $n_m$  provided that the current, magnetic field and material thickness are known. In addition, the majority carrier mobility can also be derived by the formula of semiconductor resistivity.

$$\rho = \frac{1}{qn_m \mu_m} \quad (3.12)$$

where  $\mu_m$  is the majority carrier mobility.

The formulas given above only apply for materials where current transportation relies mostly on one type of carrier such as metals and extrinsic semiconductors. For intrinsic or near intrinsic semiconductors in which both electrons and holes are contributing to the conductivity, the calculation of the Hall voltage needs to be adjusted to

$$V_H = \frac{IB}{t} \frac{(p\mu_h^2 - n\mu_e^2)}{e(p\mu_h + n\mu_e)^2} \quad (3.13)$$

where  $n$  and  $p$  are the electron and hole concentration,  $\mu_e$  and  $\mu_h$  are the electron and hole mobility, respectively.

The Van der Pauw method enjoys the advantage that it can measure samples with arbitrary size, since the geometric spacing of the contacts is unimportant. It has been widely used in this thesis to study the electrical properties of the deposited materials. A Nanometrics HL5500PC Hall Effect Measurement System is used for all Hall measurements. It enables measurements over a wide range of resistances ( $\Omega$ -G $\Omega$ ). Equipped with vacuum pump and liquid nitrogen, the measurement can be performed in a temperature range from 77 K to 300 K.



## Chapter 4

# Properties of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ nanowires

### 4.1 Introduction

$\text{Ge}_2\text{Sb}_2\text{Te}_5$  (GST) phase change material, as mentioned in previous chapters, has become the most important phase change materials in data storage industry. A good insight of conventional sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ , such as its electrical and crystallinity properties, shall be useful for our further studies of phase change materials deposited by other methods. In addition, the miniaturization of each memory cell is one of the major driving forces in the development of denser and more power efficient memory devices. However, as the memory size scales down, the relative contribution of the contacts to the total resistance will increase which can directly affect the memory performance. Although phase change materials and memories have been extensively investigated in recent years, only a few studies focus on the contact properties between phase change materials and metal electrodes [132, 133]. Hence, a better understanding of the contact resistance in phase change device, especially in nanoscale cells, will be beneficial for the improvement of scaling, power consumption and programming properties of future phase change random access memory (PCRAM) cells.

Nanowire-based technology is a powerful approach to assemble memory devices on ultra-small scales for its sub-lithographic size and unique geometry. It provides the potential for highly scaled phase change memory devices and multilevel memory applications. Phase change nanowires based on different materials such as GeTe [134, 135, 136, 103, 137], GeSb [138],  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  [139, 140, 90, 141, 142],  $\text{Ge}_1\text{Sb}_2\text{Te}_4$  [143],  $\text{In}_2\text{Se}_3$  [144] have been previously synthesized and demonstrated nano-second level switching time at very low powers, suggesting that nanowires could be ideal for data storage devices. In addition, this one-dimensional phase change nanostructure can also provide a valuable scientific research platform for understanding the material properties at the nanoscale.

To date, most of the methods used to synthesize phase change nanowires are based on bottom-up technology such as thermal evaporation method under vapor-liquid-solid (VLS) mechanism [143, 141, 137, 137, 139] and metal organic chemical vapour deposition (MOCVD) [144]. However, this technology suffers from disadvantages such as poor nanowire diameter/position control, non-CMOS-compatibility and poor reproducibility. On the contrary, a top-down technology offers better control over the fabrication process and is highly reproducible and CMOS-compatible. The conventional way for top-down nanowire fabrication is by e-beam lithography, however, this introduces a high cost with low writing speeds compared with other lithographic techniques.

Here we use a spacer etch process to fabricate GST phase change nanowires. This spacer etch technique can be used as a low-cost alternative to e-beam lithography for sub-hundred nanometre nanowire fabrication [145]. Unlike bottom-up technology, it is compatible with current CMOS process and the geometry and location of the nanowires can be precisely controlled. Most importantly, it provides a feasible and systematic approach to study the contact resistance between the nanoscale GST material and the metal contact.

This chapter can be divided into two parts. In the first part, we will focus on the deposition and characterisation of titanium nitride (TiN) film which serves as the contact electrode in this work. In the second part,  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  phase change nanowires will be fabricated by novel spacer etch approaches. The study of contact resistance between the nanoscale  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and TiN electrodes will be conducted based on the devices fabricated from the spacer etched  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  nanowires.

## 4.2 Deposition and characterisation of TiN films

Titanium nitride is an unique material which exhibits both metallic (Ti-Ti) and covalent (Ti-N) bonding characteristics [146]. The metallic bonding enables TiN to have an electrical conductivity and metallic reflectance while the covalent bonding leads to its high melting point, extreme hardness and excellent thermal and chemical stability. TiN has been used in microelectronics as a conductive barrier between active device and metal contacts. It is able to block the diffusion of metal into silicon while providing a good electrical connection due to its high conductivity. Recently, the use of TiN as electrode has also attracted more and more attention. Unlike other metallic electrodes which have issues with passivating oxide film formation, TiN, due to its exceptional chemical stability, extreme corrosion resistance and good electrical properties, has become a promising alternative to traditional electrodes. Hence, TiN was chosen as electrode for all work in this thesis.

TiN films have been deposited on the surfaces of different substrates using various techniques such as chemical vapor deposition (CVD) [147, 148], magnetron sputtering [149],

and ion beam assisted deposition [150]. The deposition of TiN films by sputtering has important advantages such as low levels of impurities and easy control of the deposition rate. Besides, films with different morphology and crystallographic structures can also be obtained by this deposition method [151].

TiN films in this thesis were deposited by medium frequency magnetron sputtering (Leybold HELIOS XL) at room temperature. This process combines reactive middle frequency sputtering with an additional RF plasma source. During each rotation of the plate holding the substrate, a thin layer of Ti was deposited from dual magnetron metal targets (99.99 % purity) using a power of 300 W in an Ar atmosphere. The thin film was then transformed into a nitride layer by passing the substrate underneath the  $\text{N}_2$  plasma of the RF source. The  $\text{N}_2$  and Ar flow rates were maintained at 30 and 35 sccm, respectively and a high drive speed of 180 rpm was applied to enhance the film uniformity. The chamber pressure was set to be  $10^{-5}$  mbar. The deposition rate was found to be 0.161 nm/s. In order to study the properties of sputtered TiN films, films with different thicknesses ranging from 25 nm to 125 nm were deposited.

The room temperature electrical resistivity of TiN films were investigated by measuring the sheet resistance of the TiN thin films. In this thesis, sheet resistances of TiN films with different thicknesses were measured by four probe technique (Jandel 4-probe analyser). The resistivity of the TiN was then obtained from the sheet resistance using Equation.3.7. The sheet resistance value of the films decreased from  $39 \Omega/\square$  to  $6.4 \Omega/\square$  with the increase in thickness as shown in Fig.4.1 while the resistivity can be obtained by the slope of the line. The resistivity of TiN deposited was found to be  $85 \mu\Omega\cdot\text{cm}$  which is only a factor of 2 higher than the theoretical resistivity of bulk crystalline TiN ( $30 \mu\Omega\cdot\text{cm}$ ) hence indicates a good conductivity. TiN films deposited in other works show different resistivities ranging from  $20 \mu\Omega\cdot\text{cm}$  to  $200 \mu\Omega\cdot\text{cm}$  due to different deposition parameters such as gas ratio [146, 152]. For comparison, Ti has a resistivity of  $42 \mu\Omega\cdot\text{cm}$ .

It is worth mentioning that the compositional study of sputtered TiN films by EDX proved to be challenging as the detection of light element (nitrogen) in EDX is more difficult compared to heavier elements. It becomes especially difficult when detecting a light element and a heavy element together, like TiN in this case, since the X-ray produced by light elements can be easily absorbed by the heavy element. Even though the absorbing issue has already been taken into account in the EDX software, the accuracy of the measurement is still poor. No conclusive measurements were possible.

X-ray diffraction measurements were carried out on these TiN films and only peaks for TiN were observed as shown in Fig.4.2, suggesting stoichiometric TiN.

The thermal stability of the deposited TiN films was investigated by annealing the sample at different high temperatures. It was found that the TiN thin films were easily oxidized when they were heated up to  $200^\circ\text{C}$ . Note that bulk TiN has a oxidation

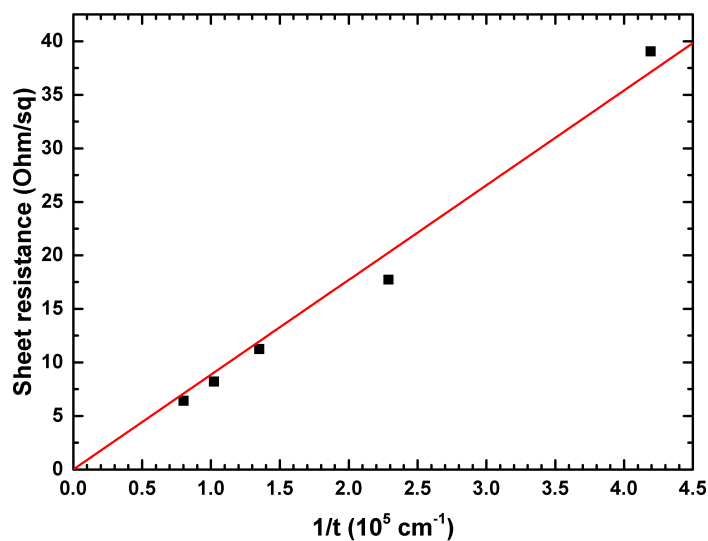


Figure 4.1: Sheet resistance of TiN films of different thicknesses. The red line indicates a linear fit of data to Equation.3.7. The resistivity of this TiN film can hence be extracted from the slope of this line and is  $85 \mu\Omega\text{-cm}$ .

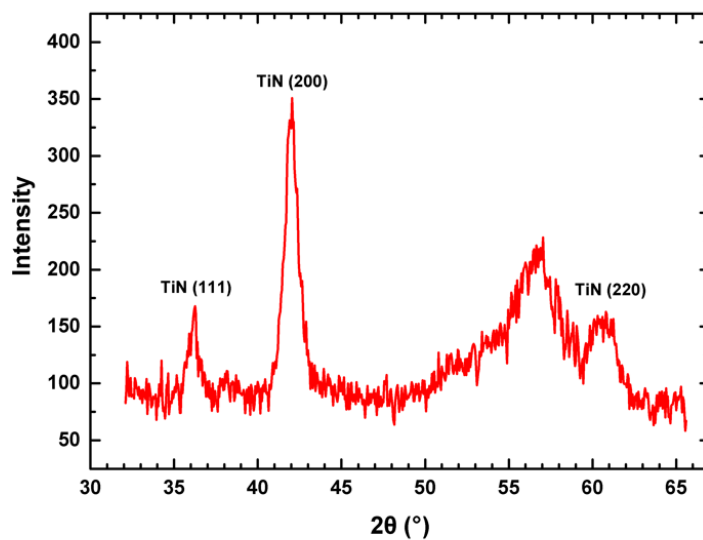


Figure 4.2: XRD measurement of TiN film with a nominal thickness of 75 nm on a Si substrate. Peaks labelled match the stoichiometric TiN. Pattern was collected in grazing incidence ( $\theta = 3^\circ$ ) with a  $\text{Cu-K}_\alpha$  radiation ( $1.54 \text{ \AA}$ ).

temperature of  $800^\circ\text{C}$  in normal atmosphere. The discrepancy in this case might be explained by the fact that instead of bulk TiN, we had very thin TiN films which can be oxidized much more easier than bulk TiN. In order to avoid oxidization, Rapid Thermal Annealing (RTA) technique was used to anneal TiN samples. It enables the annealing to start at room temperature in either vacuum or argon ambient. Besides, it also enables a high heating rate by which the sample can be heated to a high temperature within a short time. After loading the sample, the annealing chamber underwent a pump and purge cycle for three times to get rid of oxygen. Then the chamber was heated to set temperatures of  $300^\circ\text{C}$ ,  $400^\circ\text{C}$ ,  $500^\circ\text{C}$  and  $600^\circ\text{C}$  in 40 seconds and annealed for 20 minutes. In this experiment, silicon chips with 75 nm TiN deposited on top were used.

The sheet resistances of annealed TiN films were measured and compared with non-annealed films. An insignificant decrease of sheet resistance was found between these films. For the non-annealed TiN film, the sheet resistance was  $12.19 \Omega/\square$ , while for annealed films, sheet resistances were  $11.65 \Omega/\square$ ,  $11.90 \Omega/\square$ ,  $11.86 \Omega/\square$ ,  $12.09 \Omega/\square$  after anneal at  $300^\circ\text{C}$ ,  $400^\circ\text{C}$ ,  $500^\circ\text{C}$  and  $600^\circ\text{C}$ , respectively. Note that the measured sheet resistance for TiN film on small chip (1 cm by 2 cm in this case) was slightly higher than that was measured on a whole wafer. This is because the basic assumption for 4-point probe measurement of thin film is that the size of this film is large such as a 6-inch wafer. For relatively small size films as in our case, a correction factor which is smaller than one is required to obtain the correct sheet resistance value.

Fig.4.3 shows the XRD patterns for non-annealed TiN film and films annealed at  $400^\circ\text{C}$  and  $600^\circ\text{C}$ . Same characteristic peaks were observed with slightly shifted angles and peak intensity. This shift towards a high angle is possibly caused by the relaxation of crystal structure after annealing, leading to a reduced inter-plane distance. The surface morphology of TiN films was studied using atomic force microscopy (AFM). Fig.4.4 shows the topography of a non-annealed TiN film with a nominal thickness of 75 nm. The surface roughness was found to be 0.321 nm which indicates a smooth surface of TiN film. For annealed films, the surface roughness was found to be the same.

## 4.3 Spacer etch $\text{Ge}_2\text{Sb}_2\text{Te}_5$ nanowire and contact resistance measurement

### 4.3.1 Fabrication of spacer etched $\text{Ge}_2\text{Sb}_2\text{Te}_5$ nanowire

The overall fabrication process is described in Fig.4.5. A 400 nm thermal  $\text{SiO}_2$  was grown on a pre-cleaned Si wafer (Fig.4.5(a)). This layer was patterned with a photolithography process using a pre-designed mask (Fig.4.5(b)), followed by a reactive ion etching of the  $\text{SiO}_2$  to create a trench with a depth of 100 nm (Fig.4.5(c)). The photolithography was carried out using an EVG620TB with a positive resist Shipley 1813. The etching was

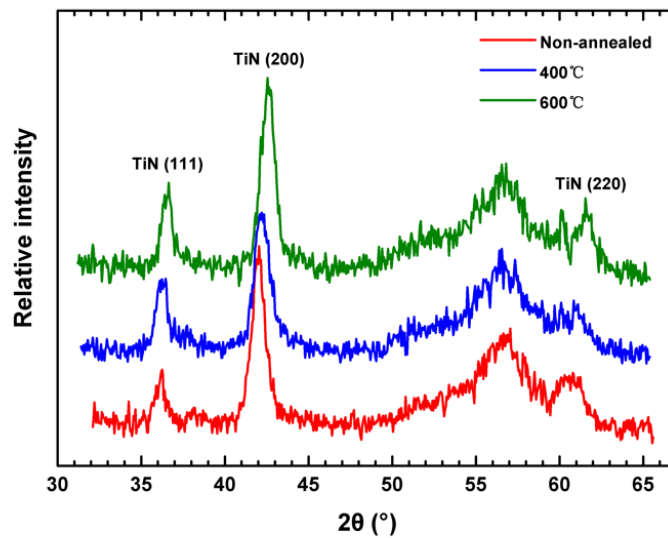


Figure 4.3: XRD patterns of non-annealed TiN film and films on Si substrates annealed at 400°C and 600°C with the same thickness of 75 nm. Patterns were collected in grazing incidence ( $\theta = 3^{\circ}$ ) with a Cu- $\text{K}\alpha$  radiation (1.54 Å).

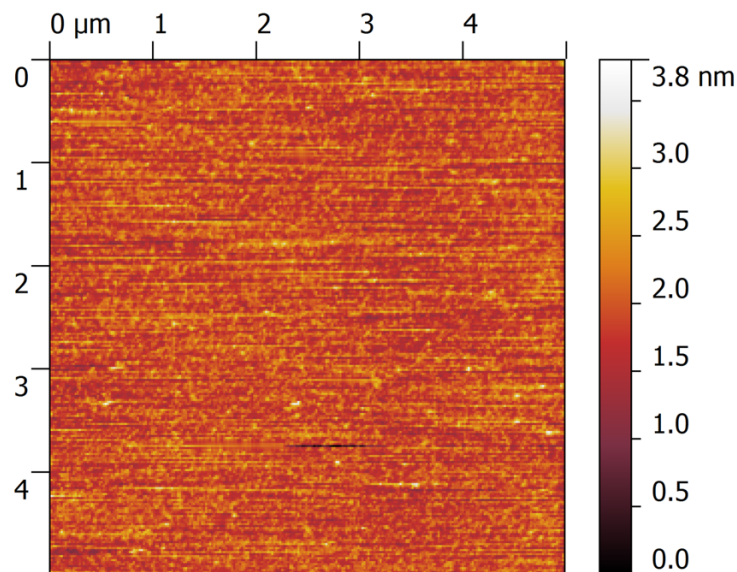


Figure 4.4: Topography of a TiN film with a thickness of 75 nm. The surface roughness of this film is 0.238 nm.

performed by an OIPT Plasmalab 80+ with  $\text{CHF}_3$  and Ar. After resist stripping, an amorphous GST layer with a thickness of 100 nm was deposited on the etched  $\text{SiO}_2$  by RF sputtering from a target of the composition  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  at a power of 45 W (Fig.4.5(d)). The deposition of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin films was conducted by Dr. Behrad Gholipour. It took place in a Kurt J. Lesker NANO38-SPUTTER thin film deposition system with a background pressure of 3 mTorr. High purity argon was used as the sputtering gas and the distance between the target and the substrate was 150 mm. The substrate was kept at room temperature initially and less than  $10^\circ\text{C}$  temperature increase was observed while the film was being formed. The power used was 45 W and the argon gas flow was 37 sccm. The deposition rate was found to be  $0.89 \text{ \AA/s}$ . The deposited film thicknesses varied for different applications. The  $\text{SiO}_2$  trenches created in the previous process serve as a step for the following spacer etch. The GST nanowire can then be formed by an anisotropic etching process.

This etching process is crucial in fabricating spacer etch nanowires. Ion beam etching was chosen in this work to etch the GST as it provides high uniformity and reproducibility with limited overetch damage due to its physical etch process. The nature of the process and its non-selectivity results in the GST at the  $\text{SiO}_2$  step forming the desired nanowire (Fig.4.5(e)). In this work, the nanowires were formed using Ionfab ion beam etcher by Oxford Instrument Plasma Technology. The etch condition was set to a RF power of 700 W, a beam current of 300 mA, beam voltage of 500 V and an acceleration voltage of 400 V. Extra care has been given to control process temperature by setting the sample chuck to  $5^\circ\text{C}$  and applying a helium flow for the heat transfer to avoid GST crystallization during the etch process. The conditions for IBE are tabulated in Table.4.1.

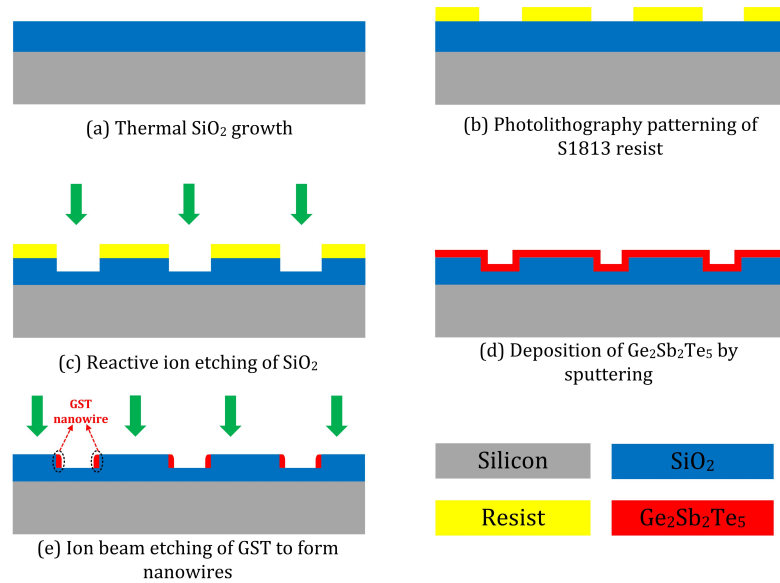


Figure 4.5: Fabrication process for spacer etch  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  nanowire.

Table 4.1: Optimised IBE parametres for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin film etching.

Parametre	Value
Beam Voltage	500 V
Beam Current	300 mA
RF Power	500 W
Neutralizer Current	550 mA
Rotation Speed	20 rpm
Cooling temperature	20°C

The etch rate is determined by etching a 300 nm  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin film for different times and measuring the remaining thickness of the thin film. The thickness of etching is plotted against etching time in Fig.4.6. The etch rate can be extracted from interpolated line and was found to be 1.55 nm/s.

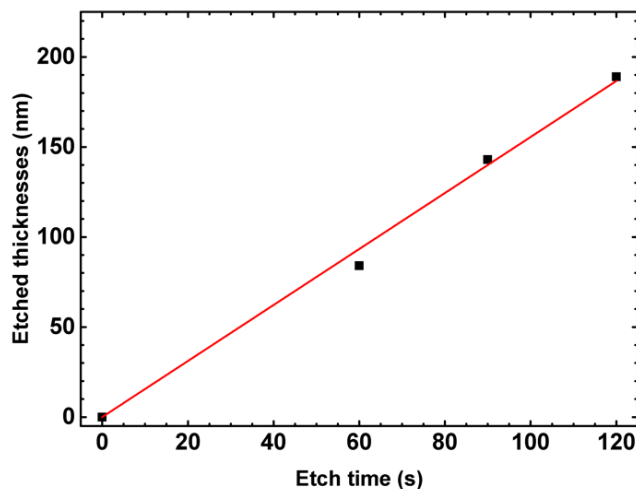


Figure 4.6: Thickness of etching, measured by cross-section SEM, as a function of etch time in seconds.

The nanowire-to-TiN structure devices were fabricated by depositing and patterning TiN electrodes on two ends of the  $\text{SiO}_2$  trench by photolithography and lift-off processes. A negative nLOF AZ2070 resist was used in this photolithography process. This is followed by the deposition of the electrode film. Immediately before TiN film deposition, an Argon plasma treatment was given in the chamber to remove any native oxide and surface contamination on GST surface. Subsequently, 125 nm TiN film electrodes were deposited using medium frequency plasma assisted magnetron sputtering (Leybold Optics HELIOS Pro XL) at room temperature. This process combines reactive middle frequency sputtering with an additional RF plasma source. During each rotation of

the plate holding the substrate, a thin layer of Ti was deposited from dual magnetron metal targets (99.99% purity) using a power of 3000 W in an Ar atmosphere. The thin film was then transformed into a nitride layer by passing the substrate underneath the  $\text{N}_2$  plasma of the RF source. The  $\text{N}_2$  and Ar flow rates were maintained at 30 and 35 sccm, respectively, and a high drive speed of 180 rpm was applied to enhance the film uniformity. The TiN electrodes were then formed using an acetone lift-off process.

### 4.3.2 Standard characterisation of spacer etch GST nanowire

Fig.4.7(a) shows a cross-section scanning electron microscope (SEM) image of a sample after GST film deposition over the  $\text{SiO}_2$  step. The GST layer can be identified on top of the thermal oxide layer and is about 110 nm in thickness. The GST film thickness on the sidewall was measured to be 50 nm and is reduced due to the non-conformity of the sputtering process. This region of the GST will eventually form the spacer nanowire after etching.

Fig.4.7(b) shows a cross-section SEM image of the sample after a 30-second etch. A clear decrease of the GST layer thickness from 100 nm to 55 nm can be observed. Additional etching of 20 seconds further decreased the film thickness while the GST along the sidewall remained untouched as shown in Fig.4.7(c). After another 30-second etch, the GST on the planar surface has been completely removed (Fig.4.7(d)), leaving a GST nanowire along the  $\text{SiO}_2$  step. The dimensions of the nanowire was measured to be 50 nm  $\times$  100 nm (width  $\times$  height) which match the GST film thickness on the sidewall and the  $\text{SiO}_2$  trench depth, respectively, indicating that the nanowire dimensions can be precisely controlled by the fabrication process. The nanowire height is determined by the height of the  $\text{SiO}_2$  step and can be controlled during the RIE process. The nanowire width is tuneable through the thickness of the deposited GST layer. The nanowire length is determined by the length of  $\text{SiO}_2$  trench.

The continuity of the nanowires was investigated by observation under optical microscope using differential interference contrast mode. Fig.4.8(a) shows a Nomarski micrograph of the spacer etched GST nanowires. A clear contrast can be observed between the  $\text{SiO}_2$  trenches and the GST nanowires adjacent to their boundaries. All nanowires appear to be continuous with no evidence of discontinuities. A high magnification SEM image of a single GST nanowire is shown Fig.4.8(b). The width of the nanowire is measured to be 48 nm which matches the data obtained from the cross-section SEM. It is worth mentioning that the nanowire shows some roughness which is attributed to the sidewall line edge roughness of the  $\text{SiO}_2$  trench. This could be further improved through a higher resolution photolithography process.

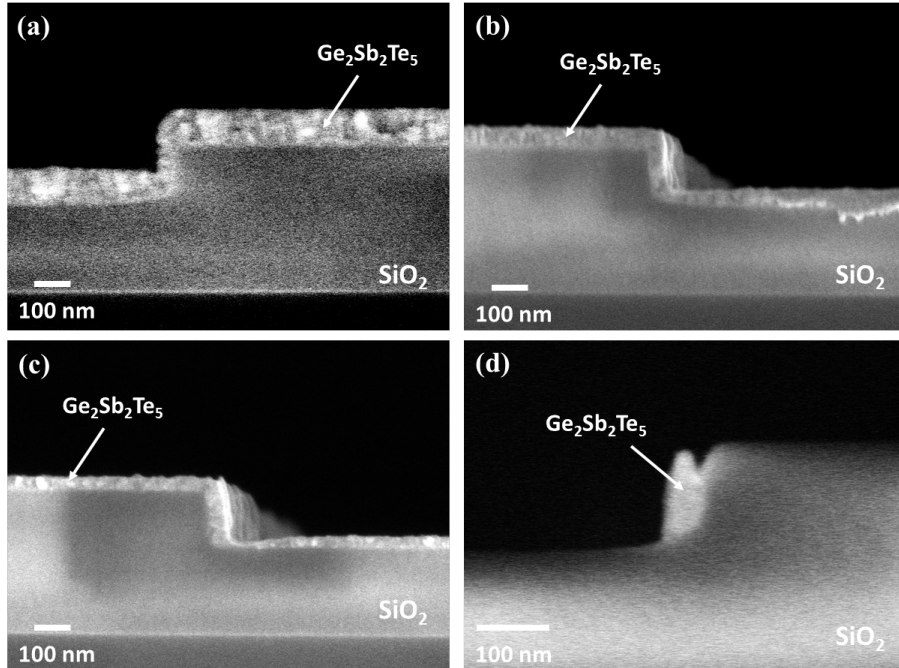


Figure 4.7: Cross-section SEM images of samples (a) before GST spacer etch, (b) after a 30-second etch, (c) after a 50-second etch and (d) after a 80-second etch. The nanowire is obtained after 80-second etch and the cross-sectional dimension of the nanowire is measured to be  $50 \text{ nm} \times 100 \text{ nm}$  (width  $\times$  height)

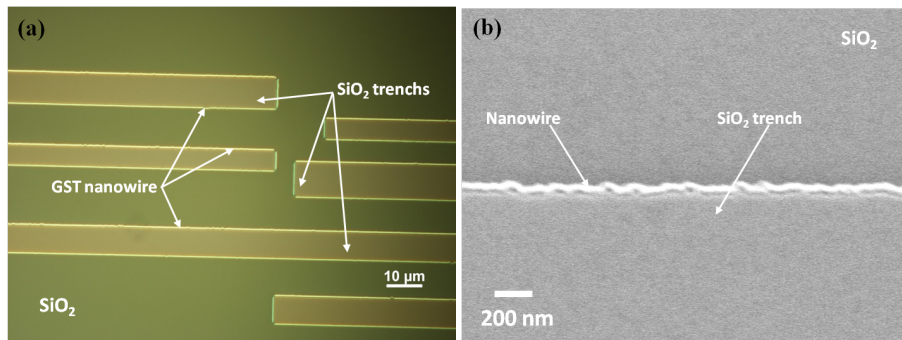


Figure 4.8: (a) Nomarski micrograph of spacer etch GST nanowire, nanowires can be observed at the edge of  $\text{SiO}_2$  trenches; (b) SEM image of one spacer etch GST nanowire with line edge roughness.

### 4.3.3 Electrical properties of spacer etch GST nanowire

**Phase change property** Two-terminal devices were fabricated in order to study the electrical properties of the nanowires and contact resistances. Fig.4.9 shows a fabricated nanowire device with several parallel nanowires obtained from  $\text{SiO}_2$  trenches. It is obvious that two identical nanowires are formed within each  $\text{SiO}_2$  trench. Two ends of the nanowires were covered by TiN electrodes, leaving an active nanowire length of  $20\text{ }\mu\text{m}$ . Different contact areas can be obtained by incorporating several  $\text{SiO}_2$  trenches into one device. It is worth mentioning that the contact area of this device cannot be calculated directly from the total surface area of all nanowires covered underneath the TiN electrodes as the distribution of current density is not uniform within this area and additional care has to be taken in calculating the actual contact area for this device. Here we used COMSOL to simulate the current distribution between the TiN electrodes and the GST nanowires. A single GST nanowire device structure was first built in COMSOL based on the actual dimensions of the device. A DC bias of  $10\text{ V}$  was then simulated on two TiN electrodes while the resultant current density distribution between the TiN electrodes and GST nanowires was used to determine the effective contact area. The results revealed that for each single nanowire, current flow from TiN electrodes to the nanowires were within an area of  $75\text{ nm} \times 150\text{ nm}$  away from the edge of the TiN electrodes. The actual contact area for one device can then be calculated from this effective contact area of each nanowire and the number of nanowires.

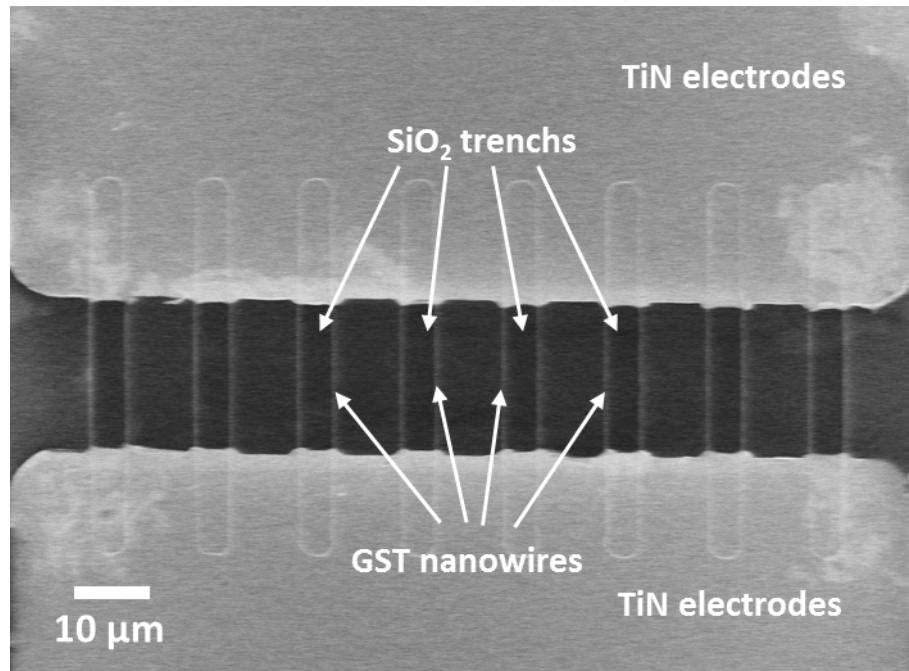


Figure 4.9: A fabricated nanowire device with several parallel nanowires. The effective length of the nanowire is  $20\text{ }\mu\text{m}$  and is determined by the distance between two TiN electrodes

The current-voltage (I-V) characteristics of the devices were measured using a DC sweep on the two TiN electrodes by an Agilent B1500A semiconductor device analyser attached to a Cascade probe station. The phase change property of the nanowires was characterized first to evaluate the potential degradation of the GST material during the ion beam etching process. A DC sweep from 0 to 10 V was carried out on amorphous (as-deposited) devices with a length of 20  $\mu\text{m}$ . It is worth mentioning that this voltage is much lower than the threshold voltage and will not induce any switching behaviour [29]. The same devices were then annealed in  $\text{N}_2$  ambient at 200° (above the crystalline temperature of GST) for 5 minutes to crystallize the GST nanowire. The annealed devices were subsequently characterized under the same DC sweep condition.

Fig.4.10 shows current/voltage measurement of devices with nanowires in parallel of 20, 50 and 100 before and after annealing, all with an effective length of 20  $\mu\text{m}$ . Devices before the annealing (Fig.4.10, solid lines) give low currents and the resistance are extracted to be about 200 M $\Omega$  for device with 20 NWs. Devices after the annealing (Fig.4.10, dashed lines) give significantly high current and the extracted resistances was found to be about 130 k $\Omega$  for the same device, significantly lower than results before annealing. This gives a resistance ratio of around  $10^3$  between the as-deposited and annealed devices which is similar to that for other memory cells with similar architectures fabricated from these phase change materials [19]. This suggests that the phase change property was well retained during the etching process.

**Contact resistance for crystalline GST** In order to study the GST-TiN interface property, the I-V characteristics are re-plotted on a linear scale. I-V curves of crystalline GST nanowires are shown in Fig.4.11(a) and display a linear relation for all three different contact areas. This linear I-V curve indicates an Ohmic contact between crystalline GST nanowire and the TiN electrodes and hence can be analysed using a modified transmission line model (TLM) method [153]. The TLM method is a well-known simple and reliable technique for measuring both the contact resistance at a metal/semiconductor Ohmic interface and the resistivity of the semiconductor. The traditional TLM measures the resistance of a thin film semiconductor, while in this work we modified this model to adapt to our nanowire devices. We assume that the other parasitic resistances such as the TiN layer to be negligible as the used TiN is much more conductive ( $\rho_{\text{TiN}} = 85 \mu\Omega\cdot\text{cm}$  in this work) than both crystalline and amorphous GST. The total resistance ( $R_T$ ) then only consists of the resistance of nanowire ( $R_{\text{NW}}$ ) and the two GST-TiN electrode contacts ( $R_C$ ) and can be written as:

$$R_T = R_{\text{NW}} + 2R_C = \frac{\rho_{\text{NW}}}{A_{\text{NW}}} \cdot l + 2 \cdot \frac{\rho_C}{A_C} \quad (4.1)$$

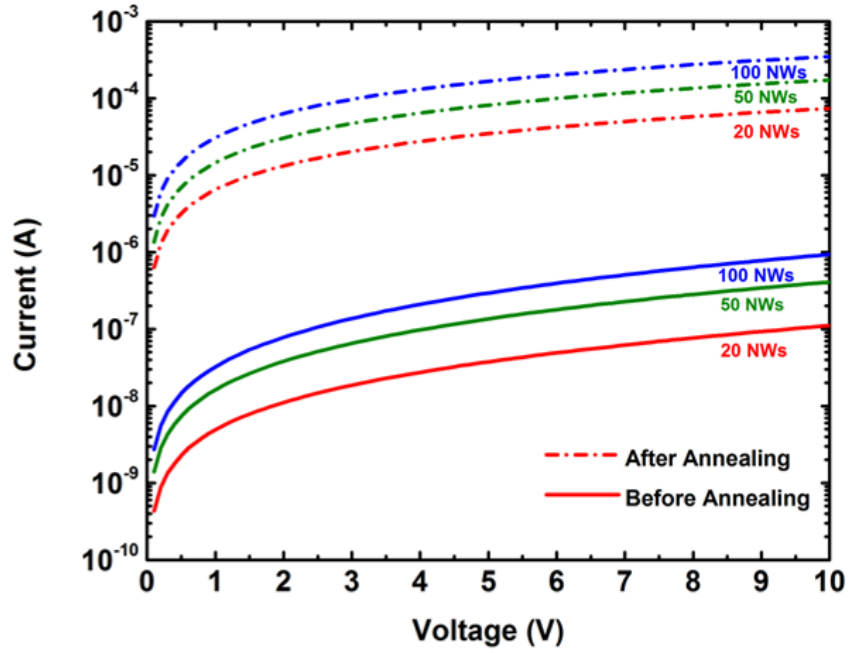


Figure 4.10: I-V characteristic of GST nanowires devices with 20 (red), 50 (green) and 100 (blue) nanowires in parallel in both amorphous state (before annealing, solid lines) and crystalline state (after annealing, dotted lines). The effective length is  $20\ \mu\text{m}$  for all devices.

where  $\rho_{NW}$  is the resistivity of GST in crystalline state;  $A_{NW}$  is the cross-section area of the nanowire devices which can be calculated from the cross-section of each nanowire and the number of nanowires,  $l$  is the length of nanowires which is determined by the distance between two TiN contacts as discussed above,  $\rho_C$  accounts for the specific contact resistance between GST nanowire and TiN electrode and  $A_C$  is the contact area.

TLM analyses were carried out using nine different combinations of the devices geometries with three different nanowire lengths ( $20\ \mu\text{m}$ ,  $25\ \mu\text{m}$  and  $30\ \mu\text{m}$ ) and three different contact areas (20NWs, 50NWs and 100NWs). For each combination, DC sweep measurements were made on several copies of identical devices. The total resistances were calculated from the linear fit of the I-V curve of each device. The average result for each combination is plotted in Fig.4.11(b) with resistance against nanowire length. For three sets of devices with different contact areas, resistances obtained from three different nanowire lengths all display linear  $R_T$ - $l$  relations with pronouncedly positive slopes which further prove the validation of the TLM for this work. The interception of each linear trend line corresponds to the contact resistance for each contact area. It is evident that the contact resistance plays an important part in the total resistance and its contribution to  $R_T$  increases with an increasing nanowire numbers. The resulting relation of contact resistance and contact area is shown in Fig.4.11(c). A linear relation between

$R_C$  and  $1/A_C$  is observed which matches the relations indicated in Equation 4.1. The specific contact resistance is  $7.56 \times 10^{-5} \Omega \cdot \text{cm}^{-2}$  from the linear fit. The resistances originating from the nanowires are extracted from the gradients of the linear fitted lines in Fig. 4.11(b) where each gradient accounts for the nanowire resistance per length. By plotting  $R_{NW}/l$  against  $1/A_{NW}$  as shown in Fig. 4.11(d), another linear fit was observed and the GST resistivity was found to be  $3.37 \times 10^{-2} \Omega \cdot \text{cm}$ .

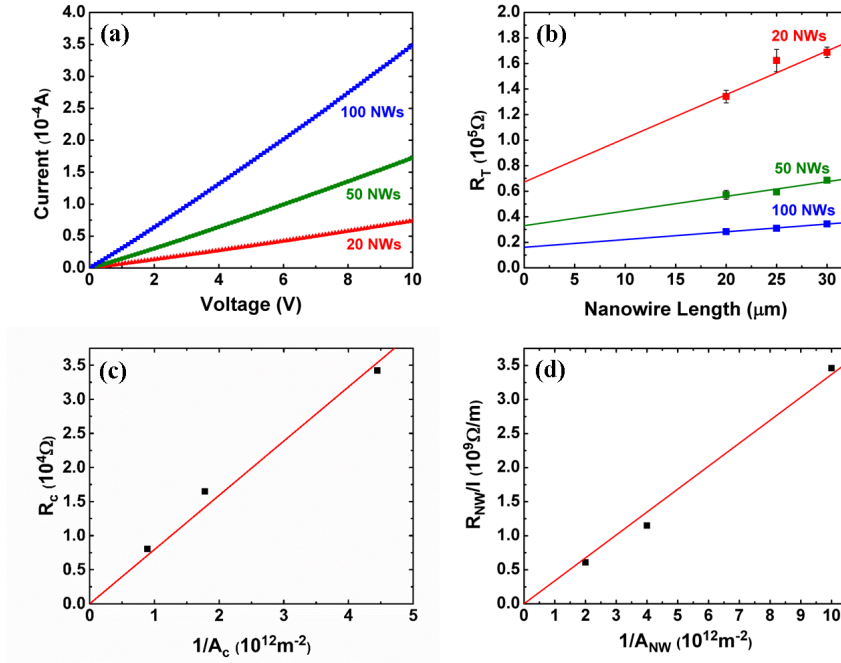


Figure 4.11: (a) I-V curves of crystalline GST nanowire devices with 20, 50 and 100 nanowires; (b) Total resistance  $R_T$  as a function of nanowire length; the gradient and intercept of each linear fit represent nanowire resistance per length and contact resistance  $R_C$ , respectively; (c) Contact resistance  $R_C$  versus contact area; the gradient is the specific contact resistance between TiN and crystalline GST; (d) Nanowire resistance per length versus nanowire cross-section; the gradient is the resistivity of crystalline GST.

**Contact resistance for amorphous GST** Unlike in the crystalline state, the I-V characteristics of the GST nanowire device in amorphous indicate non-linear conductive behaviour of amorphous GST with TiN electrode as shown in Fig. 4.11(a). Good linear fits are obtained for all devices with different contact areas in a  $\ln(I)$ - $V^{1/2}$  plot (not shown), which is explained well with the following equation of Schottky emission conduction mechanism [154]:

$$I = I_0 e^{\frac{q \sqrt{q/4\pi\epsilon_i}}{kT} \sqrt{E}} \quad (4.2)$$

where  $E$  is electrical field,  $q$  is the electronic charge,  $\varepsilon_i$  is dielectric constant of the material,  $k$  is the Boltzmann's constant, and  $T$  is absolute temperature.  $I_0$  is known as the thermal stimulated current when no voltage is applied. The value of  $I_0$  can be calculated from the intercept of each fitted line and has an expression of

$$I_0 = AA^*T^2 e^{\frac{-q\Phi_B}{kT}} \quad (4.3)$$

in which  $A$  is the contact area,  $A^*$  is Richardson's constant and  $\Phi_B$  is Schottky Barrier Height. Schottky barrier between crystalline and amorphous GeSb phase change materials has been suggested before [155]. Here this work proves the existence of Schottky barrier between the amorphous GST and TiN electrode. The value of  $\Phi_B$  can be derived by linear fitting  $I_0$  as a function of contact area  $A$  as shown in the inset of Fig.4.11(a). A good fit was observed and the Schottky Barrier Height  $\Phi_B$  was calculated to be *ca.* 0.6 eV. This suggests a noticeable contribution of the Schottky barrier at the amorphous GST/TiN interfaces to the overall resistance. Similar behaviour has also been observed in other metal/semiconductor memory device [156]. The disappearance of the Schottky barrier upon annealing could be due to the annealing process which is believed to improve the Schottky contacts between metal and semiconductor contacts [157], or due to the band gap reduction from amorphous state to crystalline state [158].

In order to calculate the specific contact resistance between amorphous GST and TiN, we measured the total resistance  $R_T$  under an applied voltage of 2 V. This voltage is small enough not to induce any switching or heating effect. The resultant  $R_T$  of different devices are plotted in Fig.4.11(b). Good linear fittings against the nanowire length are observed for all three sets of devices. This suggests that TLM method is still valid and could be used in calculating the specific contact resistance and resistivity for amorphous GST under a small applied voltage.  $R_C$  between amorphous GST and TiN can be extracted from the intercept of each line. A specific contact resistance of  $6.39 \times 10^{-2} \Omega \cdot \text{cm}^2$  was obtained by linear fitting  $R_C$  with a function of  $1/A_C$  as shown in Fig.4.11(c). The resistivity of amorphous GST was calculated by first extracting the value of nanowire resistance per length from the gradients of linear fitted lines in Fig.4.11(b) and then plotting it against  $1/A_{NW}$  as shown in Fig.4.11(d). A good linear fit is again observed and the resistivity of amorphous GST at 2 V applied voltage is  $54.5 \Omega \cdot \text{cm}$ .

All values obtained from this work are summarized and compared with reported values in Table 4.2. It should be mentioned that the data from this work are from nanowire devices whilst those in literature are from thin film devices. For the resistivity of c-GST, this work gives a consistent result with that in [133] and [24] and much lower than [158]. The discrepancy could be due to growth of GST under different conditions. In addition, the electrical conductance of nanowires is expected to be different from those of thin

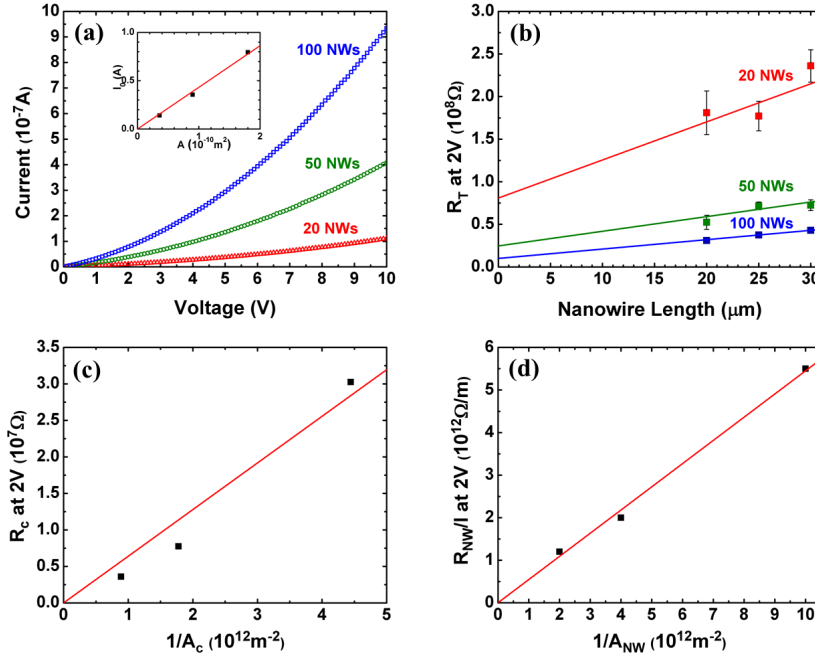


Figure 4.12: (a) I-V curves of amorphous GST nanowire devices with 20, 50 and 100 nanowires; the inset is a linear fit of the thermal stimulated current as a function of contact area  $A$ ; (b) Total resistance  $R_T$  as a function of nanowire length under a 2 V applied voltage; the gradient and intercept of each linear fit represent nanowire resistance per length and contact resistance  $R_C$ , respectively; (c) Contact resistance  $R_C$  versus contact area; the gradient is the specific contact resistance between TiN and amorphous GST; (d) Nanowire resistance per length versus nanowire cross-section; the gradient is the resistivity of amorphous GST.

films and this could also play a role in the discrepancy. The resistivity of amorphous GST has a wide range. Lower values of a-GST resistivity have also been reported ranging from *ca.* 100 to 300  $\Omega\cdot\text{cm}$  [159, 160, 161].

Table 4.2: Resistivity  $\rho$  of GST and specific contact resistance  $\rho_C$  of GST-TiN in both crystalline and amorphous phases, compared with previous reports.

Reference	$\rho$ (c-GST) ( $\text{m}\Omega\cdot\text{cm}$ )	$\rho$ (a-GST) ( $\Omega\cdot\text{cm}$ )	$\rho_C$ (c-GST) ( $\mu\Omega\cdot\text{cm}^2$ )	$\rho_C$ (c-GST) ( $\mu\Omega\cdot\text{cm}^2$ )
This work (GST-TiN)	34	54.5	80	64 (at 2 V)
Roy <i>et al.</i> (GST-TiW) [133]	20	805	3.5	95
Kato <i>et al.</i> [158]	500	3000	N/A	N/A
Lee <i>et al.</i> [24]	20	2000	N/A	N/A

N/A: not available

**Relative importance of contact resistance** The proportion of contact resistance to the total resistance can then be calculated using the values obtained in this work. It is worth mentioning that in this work the contact area  $A_C$  is not as same as the cross-section area  $A_{NW}$  of nanowires allowing for an independent extraction of both values. For a conventional vertical phase change memory structure where the two areas are identical, the ratio of  $R_C$  to  $R_T$  can be calculated at different GST thicknesses using values obtained in our work. Note that here the GST thickness in vertical structure corresponds to the nanowire length in lateral structure. The proportion of contact resistance to the total resistance in such device is displayed in Fig.4.13 as a function of different GST film thicknesses. It is evident that contact resistance dominates the total resistance for film thicknesses that are smaller than  $1 \mu\text{m}$  in both crystalline and amorphous states. This indicates that in actual memory devices, the change in resistance between two phases is predominantly an interfacial effect.

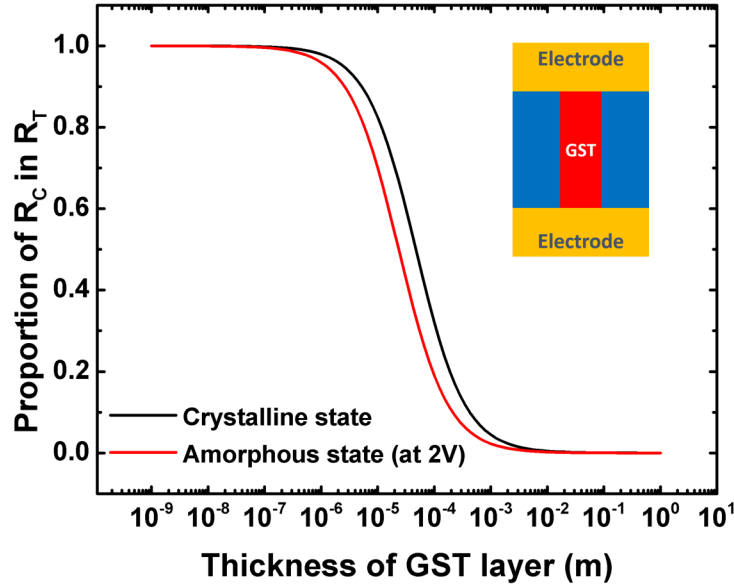


Figure 4.13: Calculated proportion of contact resistance ( $R_C$ ) in total resistance ( $R_T$ ) for a conventional vertical GST device with different GST thicknesses. the inset is the sketch of the phase change memory cell in this calculation.

## 4.4 Summary

A novel e-beam free, top-down fabrication process for a phase change material nanowire is demonstrated using a spacer etch approach. According to the method, the dimensions and locations of the nanowires can be precisely controlled. It can be easily applied to other phase change materials and materials related to nanoelectronics. In addition,

the contact resistance properties between nanowires and TiN metal contacts have been investigated. In amorphous state, a Schottky barrier of *ca.* 0.6 eV between the interface of GST and TiN electrode is the main contributing factor to the total resistance of the devices. The specific contact resistance between GST and TiN electrode was found to be  $7.56 \times 10^{-5} \Omega \cdot \text{cm}^2$  in the crystalline state and  $6.39 \times 10^{-2} \Omega \cdot \text{cm}^2$  in the amorphous state under an applied voltage of 2 V. These values are similar to those between GST and TiW electrodes. This work suggested that the contact resistance plays a dominant role in the total resistance of GST memory device in both crystalline and amorphous states.

## Chapter 5

# Electrodeposition of GeSbTe Phase Change Memory

### 5.1 Introduction

Although being a relatively mature technology with products available for sale, there are still critical issues to be solved in the phase change memory technology. One problem is the high temperature (power) required to switch the chalcogenides from crystalline to amorphous and the consequent thermal cross-talk between adjacent cells, as mentioned in Chapter 2. It is the major problem in the conventional mushroom phase change device structure and this cross-talk has largely hindered the further scaling of memory cells as shown in Fig.5.1(a). In this structure, a thin film of phase change material is deposited, normally by sputtering, on top of an array of individual heaters (bottom electrodes) where each heater serves as a single device. When a reset pulse is applied, heat is generated at the interface between heater and phase change material, dissipating further into the crystalline region of phase change material in a semi-spherical shape. This forms a so-called active switching area which is normally larger than the size of the heater itself. Further scaling of the device will inevitably lead to a point where the active area of one cell starts to affect its adjacent cells. Growth of the entire device inside a contact hole is hence more favourable as it could reduce the thermal cross-talk and simultaneously reduce the currents required for the switching operations (Fig.5.1(b)). The conventional deposition of phase change materials by sputtering does not allow selective deposition and is unable to uniformly fill small holes. Hence, other deposition approaches have to be investigated.

Electrodeposition is a well-established material preparation approach in the electronics industry [162]. The bottom-up nature of electrodeposition makes it a promising technique to depositing materials selectively into conductive nanoscale holes without issue of void formation. Several attempts have already been made to deposit phase change

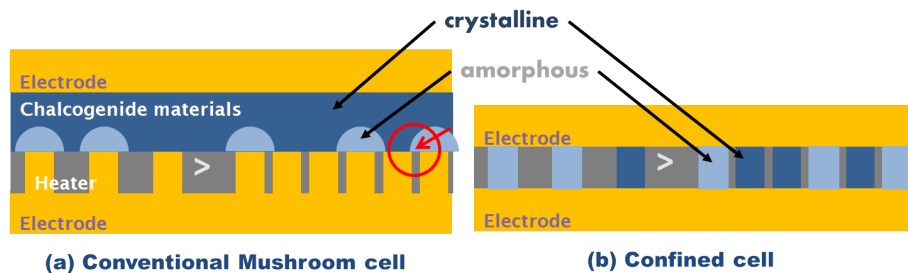


Figure 5.1: Illustration of a conventional mushroom type phase change memory structure (a), and a novel confined cell structure (b).

materials by electrodeposition and binary chalcogenides, such as  $\text{Sb}_2\text{Te}_3$  and  $\text{Bi}_2\text{Te}_3$  were successfully deposited [163, 164]. However, the electrodeposition of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  has not yet been achieved. The main issue being the rather extreme conditions required in the electrodeposition of Ge; When deposited from aqueous systems, the Ge deposition occurs at similar potentials to water splitting, leading to bubble formation. This makes the controlled preparation of alloys challenging. No works have been published on the electrodeposition of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  phase change materials with the only notable exception demonstrated by Liang *et al.* [165]. It demonstrates the feasibility of electrodepositing ternary  $\text{Ge}_x\text{Sb}_y\text{Te}_z$  materials by adopting an electrochemical atomic layer deposition (E-ALD) approach in aqueous solutions, and the ternary films were deposited with a wide range of compositions by alternating the binary cycles ( $\text{Sb}_x\text{Te}_y$  and  $\text{Ge}_x\text{Te}_y$ ) in various combinations. However, no electrical characterisations were performed to investigate the phase change behaviour of the deposited films. In addition, this process itself requires complicated set-up [166], and because it is an ALD process, the deposition rate is slow.

In this chapter, we present an electrodeposition method based on a novel non-aqueous (organic) electrolyte. The preparation of phase change alloys becomes accessible thanks to suitably tailored precursor compounds containing the relevant elements. The non-aqueous electrolyte has a wider electrochemical window, facilitating the deposition of Ge. The electrodeposition of individual elements will be presented first together with the characterisation of the deposited films. Then, ternary GeSbTe phase change films will be electrodeposited and control of the material composition will be demonstrated. The selective deposition of these materials into sub-hundred nanometre holes will be investigated. Finally, phase change memory devices based on these electrodeposited materials will be fabricated and characterised.

## 5.2 Experiment

### 5.2.1 Precursor preparation

All precursors in this chapter were synthesised by Dr. Andrew Jolleys. The electrolytes were prepared from  $[\text{TBA}][\text{GeCl}_5]$  for deposition of Ge,  $[\text{TBA}][\text{SbCl}_4]$  for deposition of Sb and  $[\text{TBA}]_2[\text{TeCl}_6]$  for the deposition of Te. The detailed preparation processes for these electrolytes can be found in our research paper [167]. When depositing GeSbTe materials, three precursors were dissolved together into a dichloromethane with 0.1 mM  $[\text{TBA}]\text{Cl}$  for improved conductivity to form electrolyte and the ratio of each precursor was optimised to control the composition of the resulting material.

### 5.2.2 Substrate preparation and characterisation

**Masked substrates** Deposition area plays an important role in electrodeposition as discussed in the previous chapter. In order to accurately understand the electrodeposition, the electrode area must be controlled. In this case, masked substrates with well-defined electrode areas were employed for thin film deposition. The fabrication process for these masked substrates is presented in Fig.5.2. A 200 nm TiN layer was first deposited onto a Si wafer patterned with a lithographically applied grid structure. After removal of the grid structure the intended electrode and contact areas were protected with a second lithographically applied resist and a layer of  $\text{SiO}_2$  was deposited on top of the TiN to mask the non-relevant areas of the electrode chips. In all processes marker pen was used as the resist. The lift-off process was performed by washing the substrate with acetone and isopropanol (IPA). A 100 nm layer of  $\text{SiO}_2$  was deposited by medium frequency dual magnetron sputtering using pure Si targets (99.99% purity) at a MF magnetron power of 4350 W in an  $\text{O}_2/\text{Ar}$  atmosphere. The  $\text{O}_2$  and Ar flow rates were maintained at 20 and 40 sccm, respectively. The layer was then further oxidized using an  $\text{O}_2$  plasma in the additional RF plasma source operating at 2000 W with an  $\text{O}_2$  flow rate of 30 sccm. A drive speed of 180 rpm yielded a deposition rate of 0.3 nm/s. After a final lift-off process, the wafer was cut along the initial grid lines. Before the electrochemical experiments the TiN electrodes were cleaned by dipping into acetone and IPA for 15 minutes each.

**Lithographically patterned substrates** To study the selective electrodeposition behaviour into small structures/holes, two types of lithographically patterned substrates with  $\text{SiO}_2/\text{TiN}$  hole structures were designed and fabricated. For hole-sizes ranging from 1  $\mu\text{m}$  to 100  $\mu\text{m}$ , the patterning was performed by photolithography using a pre-designed mask. The fabrication process is shown in Fig.5.3. For hole sizes in the nanometre range, E-beam lithography was used instead.

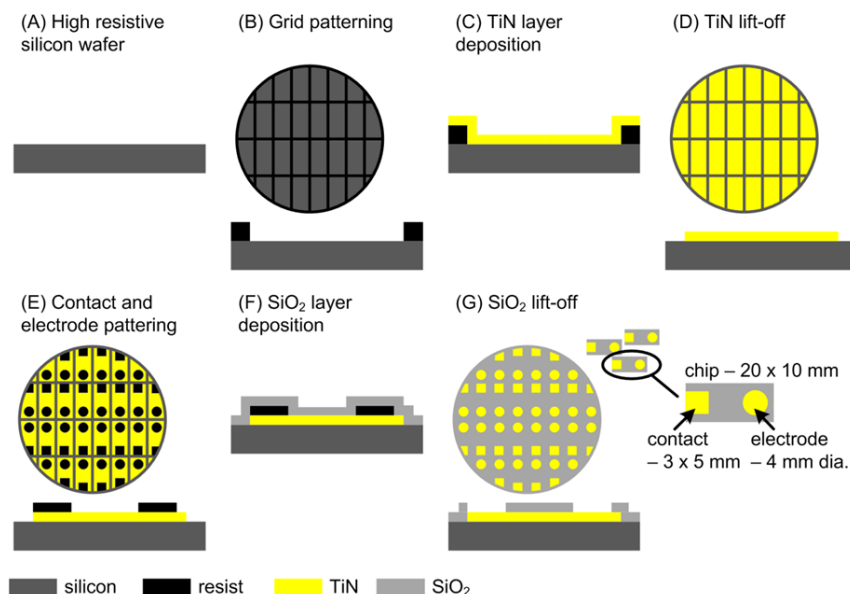


Figure 5.2: Cartoon of the steps involved in the preparation of area-defined TiN electrodes. Not drawn to scale. A first layer of resist was applied to the silicon wafer (A) in order to define individual cells and avoid current leaking at the electrode edges (B). A TiN film was then deposited onto the patterned wafer (C). This was followed by a lift-off process to remove the resist using acetone and to expose the grid regions (D). A second layer of resist was used to define the contact and electrode areas (E) before a layer of SiO<sub>2</sub> was deposited as insulator (F). A second lift-off process was performed by removing the resist with acetone (G) and the TiN electrodes were washed with acetone and isopropanol before the electrochemical experiments.

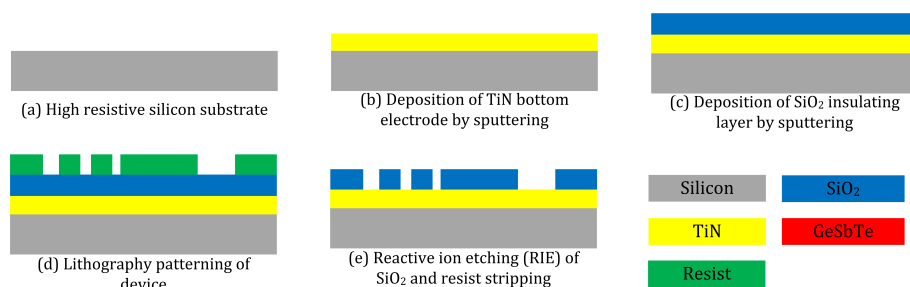


Figure 5.3: Fabrication process of SiO<sub>2</sub>/TiN photolithographically patterned substrate. Both TiN and SiO<sub>2</sub> layers are 200 nm thick and the hole sizes range from 1  $\mu\text{m}$  to 100  $\mu\text{m}$ .

High resistive ( $20 \Omega\cdot\text{cm}$ ) silicon wafers were used to mitigate the electrodeposition on the edge and backside of the patterned substrates (Fig.5.3(a)). A 200 nm TiN conducting layer and a 200 nm  $\text{SiO}_2$  insulating layer were then sputtered onto the Si consecutively using the same recipe discussed in the previous section (Fig.5.3(b)-(c)).

The sample then underwent the lithography process. For photolithography, a positive resist, S1813 was chosen. The spin speed was set to be 5000 rpm for 30 seconds which gives a resist thickness of 1000 nm. This is followed by a soft bake at  $110^\circ\text{C}$  for 90 seconds to dry the resist. In the exposure process, an exposure time of 5.5 seconds was chosen. The resist patterning took place in the following development step where the wafer was immersed in a container filled with the required developer, MF 319 in this case. The exposed area was corroded by the developer and the exact replica of the photomask was formed in the resist (Fig.5.3(d)). The developing time was around 35 to 40 seconds. The wafer was then soaked in and rinsed with DI water. For E-beam lithography, a similar 3-step process was adapted from photolithography. First, two layers of MMA (methyl methacrylate) were coated on the sample to obtain a 300 nm layer, created from two 150 nm layers. After coating of each layer, the sample was baked for 90 s at  $180^\circ\text{C}$ . After cooling down, the sample was sent to be exposed in a JEOL JBX-9300FS E-Beam Lithography System. The gun current was set to 6 nA with an accelerating voltage of 100 kV. The aperture size was  $60 \mu\text{m}$  and the spot size was 9.5 nm. Scan step was kept at 8 nm to obtain a high resolution. The layout was pre-designed by L-Edit. After exposure, the resist was developed in a MiBA and IPA (1:1) mixed solution for 60 s following by rinsing in an IPA solution for 30 s.

Etching of  $\text{SiO}_2$  was performed by a RIE80+ with  $\text{CHF}_3$  and Ar, with gas rates of 16 sccm and 34 sccm, respectively for both photolithography and E-beam lithography patterned samples (Fig.5.3(e)). The RIE power was set to 200 W and the etching rate was found to be  $0.47 \text{ nm}\cdot\text{s}^{-1}$ . For a  $1 \mu\text{m}$  thick  $\text{SiO}_2$  layer, an etching time of 36 minutes was required. Normally, an extra 3 minutes of etching was added to ensure the throughout etch of  $\text{SiO}_2$ , the TiN layer underneath served as an etch stop.

Fig.5.4 illustrates the 3-D layouts of these two patterned substrates. The big window with a size of  $3 \text{ mm} \times 4 \text{ mm}$  on the top of both substrates was designed as a contact pad for electrodeposition. It is worth mentioning that for E-beam patterned substrates, these big windows were patterned by photolithography first while E-beam technology was only used for patterning of the small holes.

### 5.2.3 Electrodeposition of individual elements

The electrochemical experiments presented in this work were conducted by Dr. Gabriela P. Kissling. All experiments were performed in a dry nitrogen atmosphere inside a glove box (Belle Technology) to efficiently avoid air and moisture. Dry dichloromethane

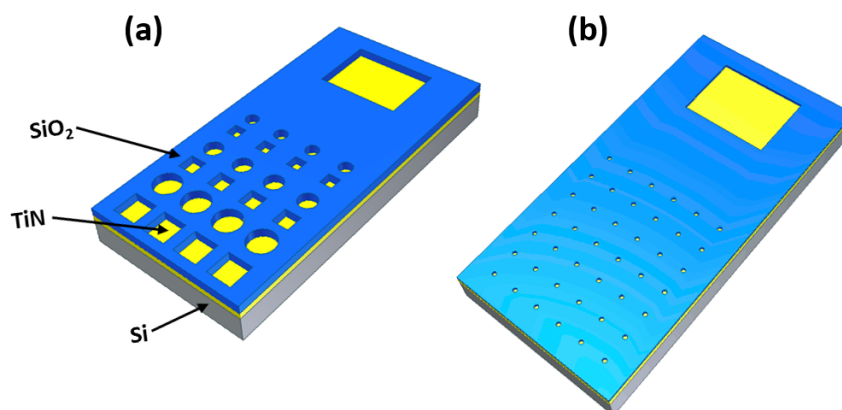


Figure 5.4: 3-D cartoon image for photolithography patterned substrate (a) and E-beam lithography patterned substrate (b).

was used as the solvent. All electrolytes were prepared with  $0.01 \text{ mol dm}^{-3}$  of the tetrabutylammonium chlorometallate salts as the redox species and  $0.1 \text{ mol dm}^{-3}$  tetrabutylammonium chloride (Fluka,  $\geq 99.0\%$ ) as the supporting electrolyte. A Pt gauze was used as the counter electrode, and a home-made Ag/AgCl electrode (in  $0.1 \text{ mol dm}^{-3}$  [TBA]Cl in  $\text{CH}_2\text{Cl}_2$ ) was used as the reference electrode. More details can be found in our research paper [167]. For individual elements, masked TiN substrates were used. The electrochemical experiments were performed in a one-compartment electrochemical cell. A microAutolab 3 potentiostat and the Autolab GPES or Nova software were used for the electrochemical measurements.

Cyclic voltammograms obtained for Ge, Sb and Te are presented in Fig. 5.5. These voltammograms could serve as benchmarks for future electrodeposition of ternary GeSbTe materials.

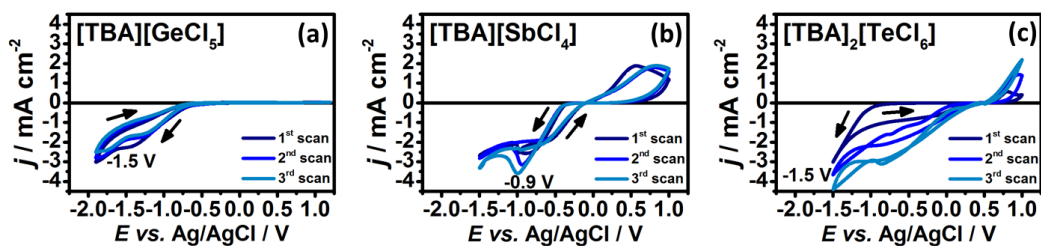


Figure 5.5: Cyclic voltammograms of  $0.01 \text{ mol dm}^{-3}$  [TBA][GeCl<sub>5</sub>] (a), [TBA][SbCl<sub>4</sub>] (b) and [TBA]<sub>2</sub>[TeCl<sub>6</sub>] (c) in dichloromethane containing  $0.1 \text{ mol dm}^{-3}$  [TBA]Cl as the supporting electrolyte measured on masked TiN electrodes. The potential scan rate was  $50 \text{ mV s}^{-1}$ . Deposition experiments and graph were taken by Dr. Gabriela P. Kissling.

### 5.2.4 Electrodeposition of GeSbTe materials

Electrolytes containing all three precursors was prepared for the deposition of ternary GeSbTe materials. The composition of the deposited GeSbTe film can be precisely controlled by adjusting the concentrations of each precursor in the electrolyte. In fact, the ability of depositing a wide range of composition is one of the advantages for electrodeposition. Here in this work, the effort was first put into achieving the composition of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ . To achieve the right 2:2:5 composition, an electrolyte with 1 mM Ge, 1 mM Sb and 2 mM Te in 100 mM TBACl was used. The cyclic voltammogram is shown in Fig. 5.6 where a deposition voltage of -1.75 V was adopted to ensure the deposition of all three elements. Both masked and lithographically patterned substrates were used for GeSbTe deposition. For the same electrolyte, the film thickness is controlled by the deposition time.

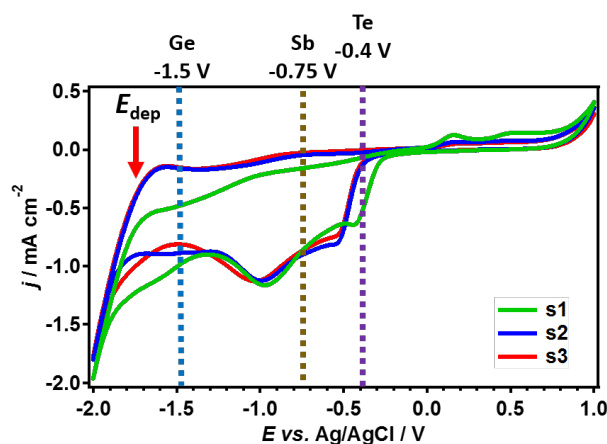


Figure 5.6: A typical cyclic voltammogram for electrodeposition of GeSbTe. The labelled deposition potentials for each element serve as indications of possible potential for the deposition to take place and cannot be directly related to the reduction peak of each element. Deposition experiments and graph were taken by Dr. Gabriela P. Kissling.

### 5.2.5 Device fabrication from electrodeposited GeSbTe

In order to study the switching behaviour of the deposited GeSbTe materials, memory devices were fabricated from both thin film and micro- and nano-patterned samples. Cartoon images of the fabricated devices are shown in Fig. 5.7. Here, either lift-off or etch process was adopted for the patterning of the TiN top electrodes.

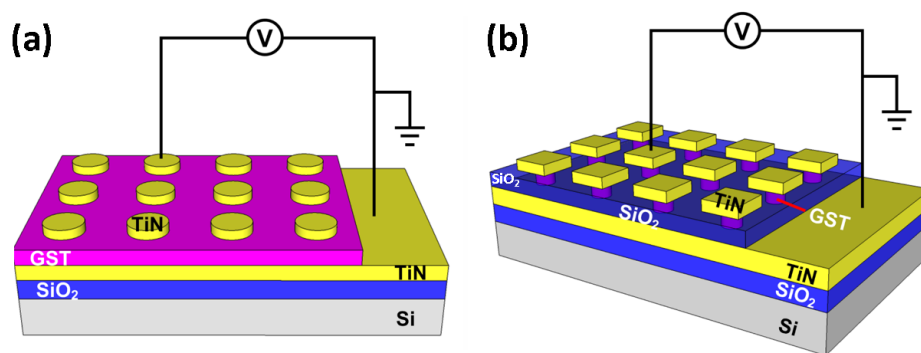


Figure 5.7: Cartoon images of electrodeposited GeSbTe (a) thin film memory device with a size of  $50\ \mu\text{m}$  and (b) micro- or nano-patterned memory device with sizes ranging from  $100\ \text{nm}$  to  $100\ \mu\text{m}$ . Both  $\text{SiO}_2$  and TiN layers are  $200\ \text{nm}$  thick.

### 5.2.6 Characterisation

All deposited samples were investigated using scanning electron microscopy (SEM) at an accelerating voltage of  $10\ \text{kV}$  using a Zeiss EVO LS 25, and energy dispersive X-ray (EDX) data were obtained with an Oxford INCAx-act X-ray detector. For high-resolution SEM, a field emission SEM (Jeol JSM 7500F) was used. XRD patterns were collected in grazing incidence ( $\theta = 3^\circ$ ) using a Bruker D8 with GADDS diffractometer except to look for preferred orientation, when a Siemens D5000 Bragg-Brentano system or a Rigaku SmartLab system with a 2-bounce primary monochromator were used. All systems use  $\text{Cu-K}_\alpha$  radiation. Raman scattering spectra of the deposited films were measured at room temperature on a Renishaw InVia Micro Raman Spectrometer using a helium-neon laser with a wavelength of  $632.8\ \text{nm}$ . The incident laser power was adjusted to  $1\ \text{mW}$  for all samples. The characterisation of the  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  devices was conducted with an Agilent B1500A semiconductor device analyser for the DC measurements and a Keithley analyser for the pulsing measurement.

## 5.3 Results and discussion

### 5.3.1 Individual elements

The morphology of the single elements were investigated by SEM, as shown in Fig. 5.8. Ge shows a smoother surface compared the other two elements, while large granules can be clearly observed on both Sb and Te surfaces. The insets are the low magnification micrographs showing homogeneous surfaces for all elements across the entire deposition area. EDX confirms that the deposited films were pure except for traces of Cl and C,

as shown in Fig.5.9. These impurities originated from the electrolytes. The Ti and Si signals were from the substrates.

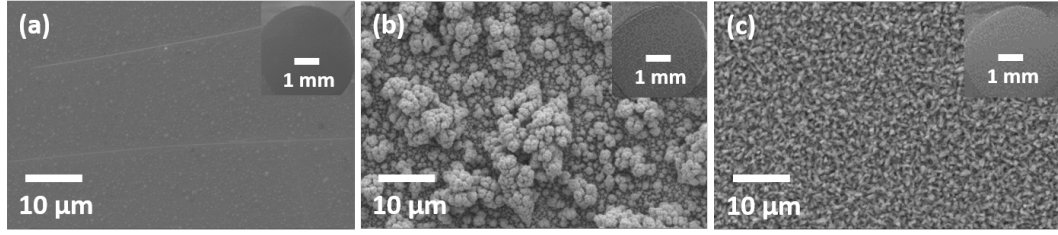


Figure 5.8: SEM images of Ge (a), Sb (b) and Te (c) films by electrodeposition. The insets are the low magnification SEM images. Deposition experiments and graph were taken by Dr. Gabriela P. Kissling.

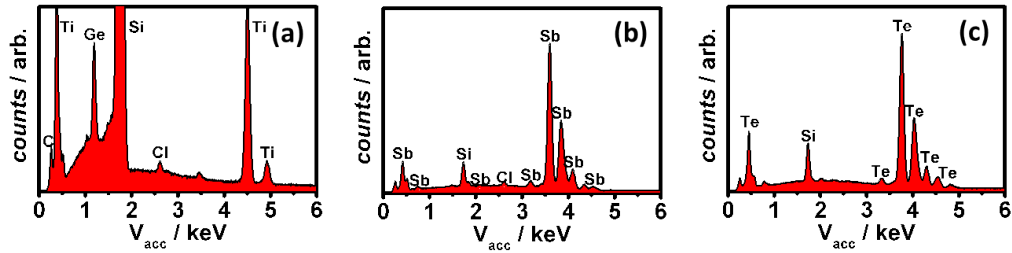


Figure 5.9: EDX spectra of Ge (a), Sb (b) and Te (c) films by electrodeposition. Deposition experiments and graph were taken by Dr. Gabriela P. Kissling.

Raman spectroscopy was used to investigate the as-deposited films, as shown in Fig.5.10. The as-deposited Ge film shows a broad peak at  $\sim 274 \text{ cm}^{-1}$  which corresponds to the amorphous Ge peak [168], a good match with the smooth film observed in the SEM image. For as-deposited Sb films, two peaks positioned at  $\sim 120 \text{ cm}^{-1}$  and  $\sim 150 \text{ cm}^{-1}$  were observed, which coincide well with the reported crystalline Sb  $E_g$  and  $A_{1g}$  peaks [169]. The as-deposited Te film also demonstrates a Raman spectrum which matches crystalline Te with two peaks at  $\sim 120 \text{ cm}^{-1}$  and  $\sim 138 \text{ cm}^{-1}$ , both representing the Te-Te bond vibrations [170].

The crystalline properties of the deposited films were studied by XRD. As-deposited amorphous Ge films were first crystallized by annealing in an Ar atmosphere at  $600^\circ\text{C}$  for 15 mins, while the Sb and Te films were studied as-deposited. XRD spectra for all three elements are shown in Fig.5.11, all in good matches with the standards, indicating good quality of the deposited films.

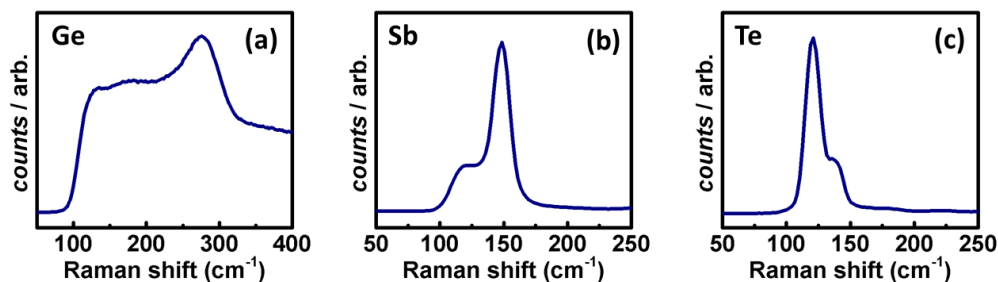


Figure 5.10: Raman spectra of Ge (a), Sb (b) and Te (c) films by electrodeposition.

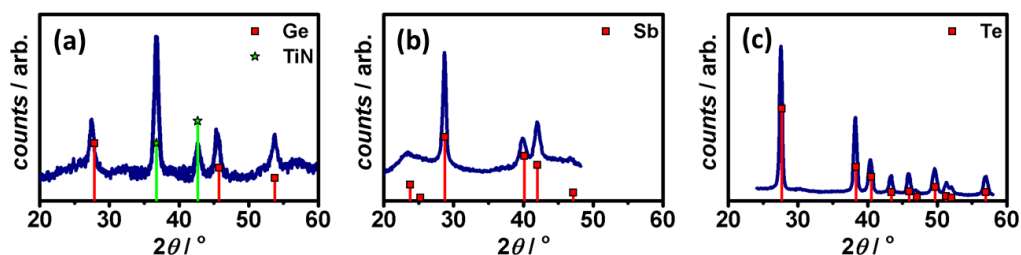


Figure 5.11: XRD spectra of annealed (600°C) Ge (a), as-deposited Sb (b) and as-deposited Te (c) films by electrodeposition.

### 5.3.2 GeSbTe thin films

The SEM images reveal the morphology of the deposited GeSbTe thin films. A continuous as-deposited film can be observed as shown in Fig. 5.12(a). There are some noticeable dirt on the film surface which possibly come from the electrolyte. The film comprises of regular small granules with sizes around 100 nm. The cross-sectional SEM (Fig. 5.12(b)) shows the film thickness is approximately 100 nm. After annealing at 410°C in a N<sub>2</sub> ambient, the morphology underwent a significant change as shown in Fig. 5.12(c), while the film thickness remained the same (Fig. 5.12(d)).

The film composition was characterised by EDX with the spectrum and compositional ratio shown in Fig. 5.13. All Ge, Sb and Te peaks can be clearly observed with negligible C content. Ti and Si peaks from the substrate have also been detected as the film thickness is significantly smaller than the interaction volume. EDX spectroscopy reveals a Ge:Sb:Te ratio of 2:1.71:4.66, which is very close to the targeted ratio of 2:2:5. As mentioned in the previous chapter, EDX measurement of GeSbTe can be very challenging due to the overlap of the Sb and Te peaks, a 2% measurement error is acceptable in these circumstances.

XRD measurements were also taken to study the crystal structure of the electrodeposited GeSbTe film. The as-deposited film is mostly amorphous as no obvious GeSbTe peak

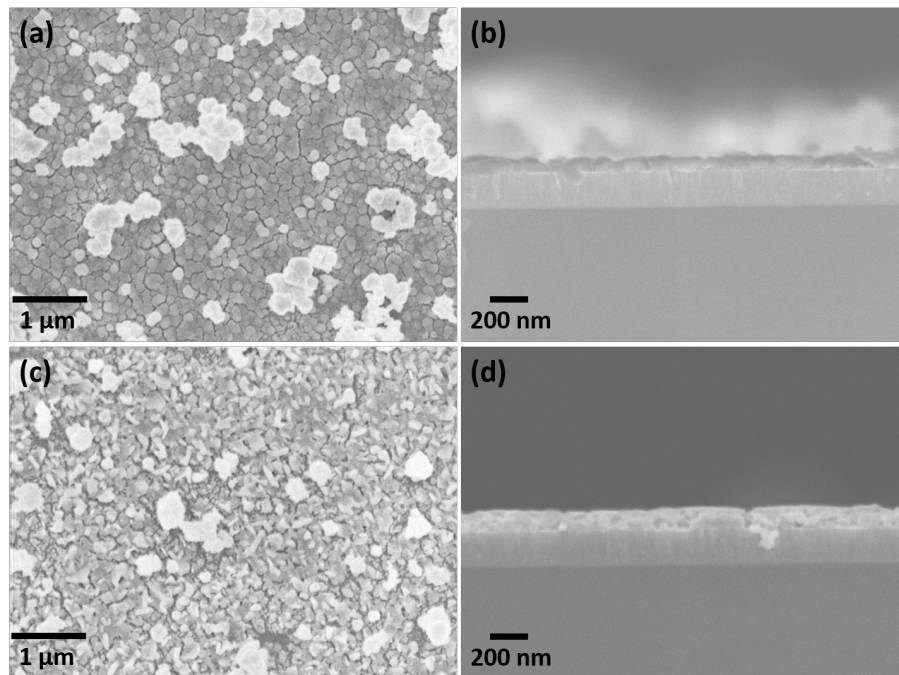


Figure 5.12: Top (a) and cross-sectional (b) SEM images of as-deposited GeSbTe film; Top (c) and cross-sectional (d) SEM images of GeSbTe film after annealing at 410°C in a N<sub>2</sub> ambient.

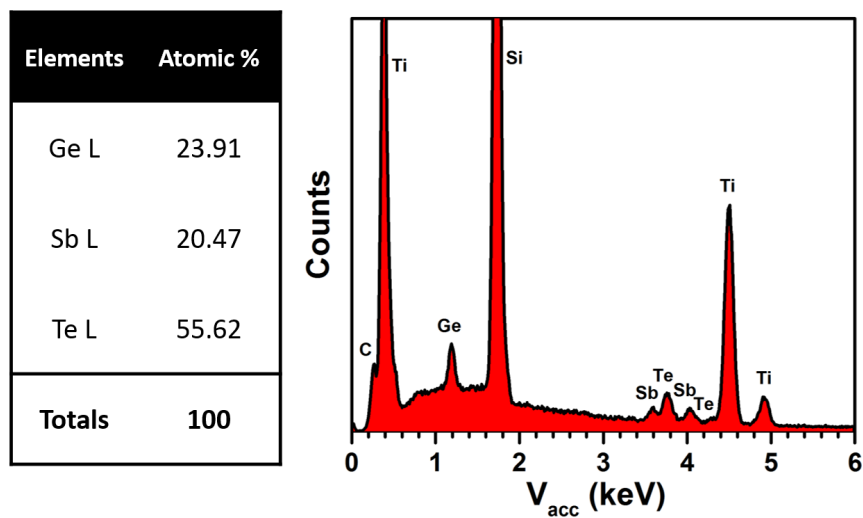


Figure 5.13: EDX spectrum of electrodeposited GeSbTe film.

can be observed in the XRD pattern (red pattern in Fig.5.14) and the granular shaped materials in Fig.5.12(c) are not crystallised GeSbTe grains. While other peaks positioned at  $37^\circ$  and  $42.8^\circ$  can be readily assigned to the TiN peaks from the substrate, one small peak at  $\sim 27.6^\circ$  remained unclear. Careful investigation of that peak reveals it is a Te 0 1 1 peak, suggesting the possible existence of Te nanocrystals in the as-deposited GeSbTe film. The film was then annealed in an  $N_2$  atmosphere for 15 minutes at elevated temperatures. The increase of annealing temperature saw the rise of a rather broad peak adjacent to the Te peak. This peak, positioned at  $\sim 28^\circ$ , is believed to be the 1 0 3 peak of crystalline  $Ge_2Sb_2Te_5$  in a stable  $P\bar{3}m$  phase which contains distorted rocksalt-type crystal blocks. This suggests the change of phase of the GeSbTe film from amorphous to crystalline. However, it is worth mentioning that this crystal structure is different to the typical fcc structure of crystalline  $Ge_2Sb_2Te_5$  as shown in Fig.3.13, and this 1 0 3 peak, together with the 1 0 6 peak positioned at  $\sim 38^\circ$ , suggest multiple stacking sequences are present [171].

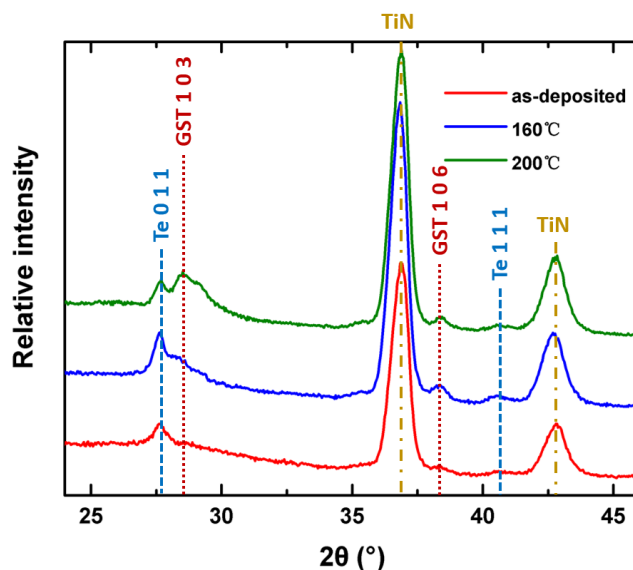


Figure 5.14: XRD patterns of electrodeposited GeSbTe film annealed at different temperatures. GeSbTe indices are based on the stable  $P\bar{3}m$  phase [171].

This phase change behaviour is further investigated using *in-situ* ramp annealing XRD as shown in Fig.5.15. The first appearance of the GST peak can be observed at an annealing temperature of  $160^\circ\text{C}$ , indicating the start of the phase change. This temperature matches well with the crystallisation temperature of sputtered GST shown in Chapter 2. The peak then became dominant after annealing at up to  $300^\circ\text{C}$ . Very interestingly, the Te peak positioned at  $\sim 27.6^\circ$  disappeared at a temperature of  $300^\circ\text{C}$ , suggesting the incorporation of Te nanocrystals into GeSbTe alloy.

Temperature-dependent XRD provides a better resolution of the intensity change for those two peaks as shown in Fig.5.16. The accurate crystallisation temperature can

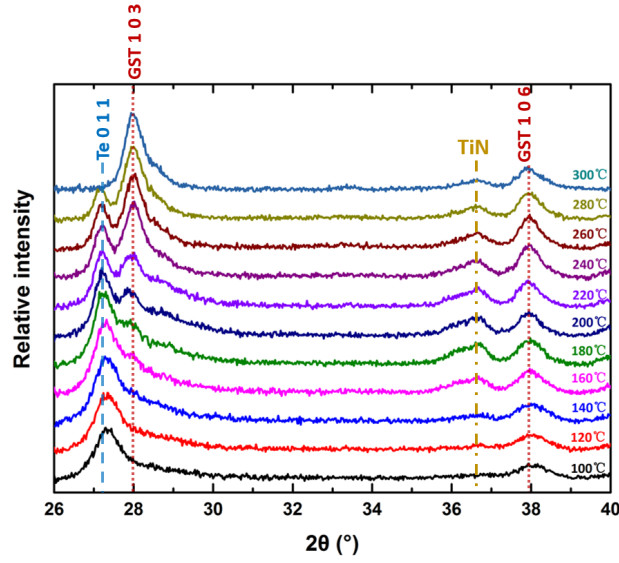


Figure 5.15: *in-situ* ramp annealing XRD of electrodeposited GeSbTe film annealed between the temperature range of 100°C to 300°C. GeSbTe indices are based on the stable  $P\bar{3}m$  phase [171]. Deposition experiments and graph were taken by Dr. Gabriela P. Kissling.

be identified as  $\sim 150^\circ\text{C}$  by the first appearance of the 1 0 3 GST peak at  $28^\circ$ . The intensity of this peak increases dramatically at  $\sim 240^\circ\text{C}$ . The intensity of the Te peak drops quite significantly at roughly the same temperature. It is reasonable to speculate that the increase of GST at  $\sim 240^\circ\text{C}$  is due to the incorporation of Te.

Raman spectra were also recorded for as-deposited and annealed GeSbTe films. The as-deposited GeSbTe film shows a similar Raman pattern to the sputtered GST, as shown in Fig. 5.17. Spectra were fitted by two Gaussian curves with two peaks positioned at  $124\text{ cm}^{-1}$  and  $142\text{ cm}^{-1}$ , respectively. The peak at  $124\text{ cm}^{-1}$  can be attributed to the  $A_1$  mode of  $\text{GeTe}_{(4-n)}\text{Ge}_n$  ( $n = 1, 2$ ) corner-sharing tetrahedra [172, 173, 174]. The  $142\text{ cm}^{-1}$  peak, on the other hand, is believed to be originated from Sb-Te vibrations in  $\text{SbTe}_3$  units or from defective octahedral coordination of Sb atoms [25, 174].

The effect of film annealing on the Raman pattern is shown in Fig. 5.18, in which films were annealed at different temperatures up to  $200^\circ\text{C}$ . A shift of the  $124\text{ cm}^{-1}$  peak towards lower wavenumber can be observed. It is suggested that the Raman band at  $124\text{ cm}^{-1}$  for amorphous GST films will decompose into  $\sim 105\text{ cm}^{-1}$  and  $\sim 135\text{ cm}^{-1}$  feature for crystalline layers [174]. The band shift can be explained by the co-existence of both amorphous and crystalline phases in the film. This speculation is also supported by the XRD results in Fig. 5.16, in which the crystalline peak is rather weak until the temperature reaches  $240^\circ\text{C}$ . The Raman band at  $\sim 142\text{ cm}^{-1}$  is also proposed to partly transform into  $\sim 110\text{ cm}^{-1}$  and  $\sim 160\text{ cm}^{-1}$  after crystallisation [174]. This also corresponds to our

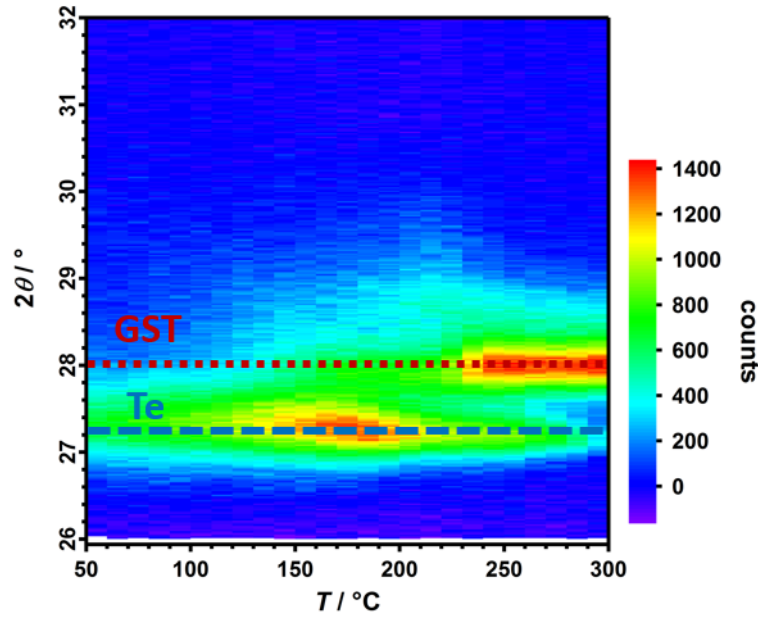


Figure 5.16: Temperature-dependent XRD of electrodeposited GeSbTe film annealed between the temperature range of 50°C to 300°C. Deposition experiments and graph were taken by Dr. Gabriela P. Kissling.

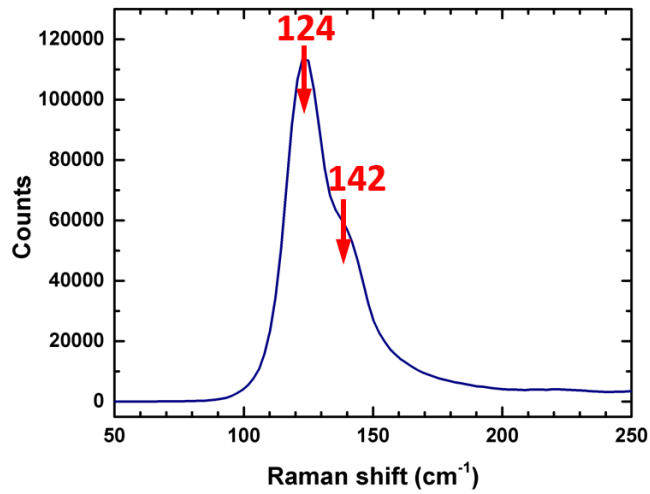


Figure 5.17: Raman spectrum of as-deposited GeSbTe film.

observation of the decrease in the  $\sim 142 \text{ cm}^{-1}$  peak intensity and the appearance of the  $\sim 160 \text{ cm}^{-1}$  peak at temperatures above  $160^\circ\text{C}$ .

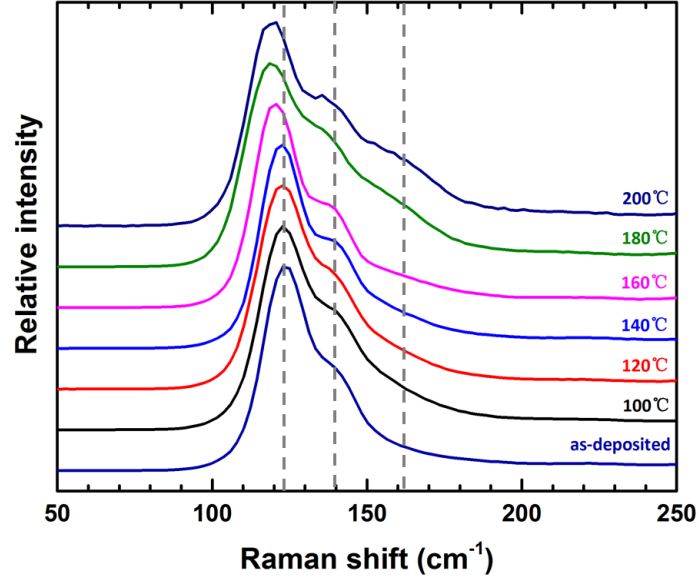


Figure 5.18: Raman spectra of electrodeposited GeSbTe films annealed at different temperatures.

### 5.3.3 Expanding the composition range

Control over the film composition can be achieved by adjusting the precursor concentrations in the electrolyte for electrodeposition. Figure 5.19 shows the ternary phase diagram of electrodeposited GeSbTe films by varying the concentration of Te (a) and Sb (b) precursors, respectively.  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  serves as an exemplary target for the deposition as pinpointed by the star in the figure. In Figure 5.19(a), the amount of Ge and Sb precursors were fixed at 1 mM while the amount of Te precursor was changing from 0 mM to 1.4 mM. The increase of Te precursor saw an increase of Te concentration in the deposited film. This suggests that more Te precursor is required for the deposition to reach the 2:2:5 composition (labelled by the star). In Figure 5.19(b), the targeted 2:2:5 composition was met by increasing the Sb precursor while fixing the amount of both Ge and Te precursors to 1 and 2 mM, respectively.

This demonstrates electrodeposition can be an easy way of accessing different GeSbTe compositions. In addition, doping with a fourth element should also be possible.

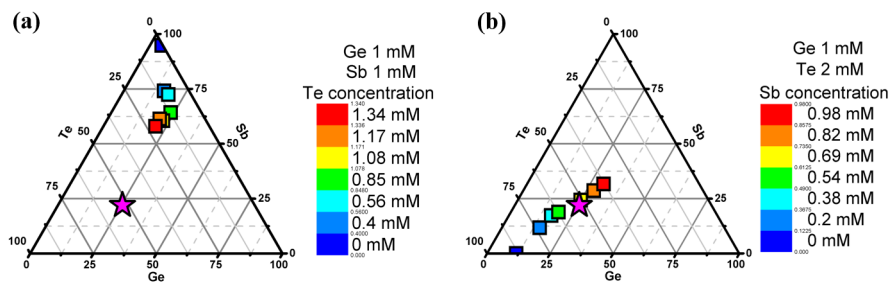


Figure 5.19: Ternary phase diagrams depicting the compositions of electrodeposited GeSbTe films by varying (a) Te precursor concentration and (b) Sb precursor concentration. The star is positioned at the composition of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ .

### 5.3.4 GeSbTe in patterned substrates

The electrodeposition of GeSbTe into patterned substrates was also studied. Fig. 5.20 shows the SEM images of an electrodeposited substrate with 200 nm hole arrays patterned by E-beam lithography. The deposited materials can be identified by the evenly distributed bumps observed on the substrate. The electrodeposition appears to be very uniform across a wide area as the sizes of all bumps are homogeneous as shown in Fig. 5.20(a)-(b). This uniformity even remains when the density of array changes significantly as shown in Fig. 5.20(c). The bump size in the denser array (left) appears to be quite similar to that in the less dense array (right). Fig. 5.20(d) shows an image with higher magnification. The size of each bump is  $\sim 2 \mu\text{m}$ , indicating an overfilling of material during the electrodeposition process.

The cross-sectional SEM images taken from line structures reveal the characteristics of hole filling, as shown in Fig. 5.21. The line width is 500 nm, 200 nm and 100 nm, respectively. However, the actual contact areas have been reduced to  $\sim 200$  nm,  $\sim 100$  nm and  $\sim 50$  nm in the  $\text{SiO}_2$  etching process. This shows a great potential of electrodeposition in nano-scale hole filling. A further scaling down of the hole size to sub-20 nm can be very promising. It can be observed from the images that the material was first grown within the confined hole. After filling the hole, significant over-growth started with a higher rate in the lateral direction than the vertical direction.

The over-filling of GeSbTe can be controlled by adjusting the deposition time. Time-dependent depositions were conducted with the same substrates and electrolyte for different times ranging from 10 s to 600 s. Examination of the bump size in SEM images (Fig. 5.22) showed that the size increases quite rapidly within the first 100 s of deposition before it saturates at  $\sim 2 \mu\text{m}$ . Almost no increase of bump size is observed after 100 s. The smallest bump size obtained is  $\sim 750$  nm for a deposition time of 10 s. It is worth mentioning that a more aggressive decrease of deposition time to 2 s resulted holes in which no material can be observed. Alternative methods are required to solve

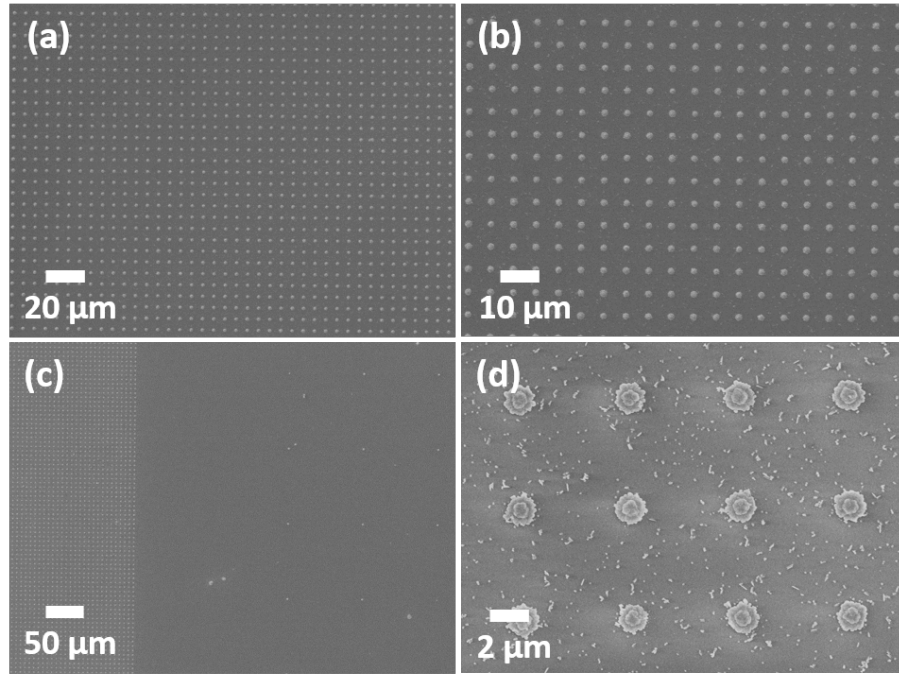


Figure 5.20: SEM images of GeSbTe deposited into a substrate with 200 nm hole arrays patterned by E-beam lithography.

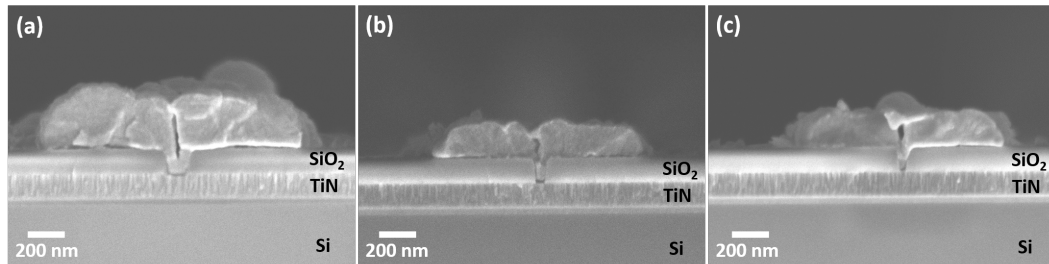


Figure 5.21: Cross-sectional SEM images of GeSbTe deposited into E-beam patterned line structures with line widths of (a) 500 nm, (b) 200 nm and (c) 100 nm, respectively.

this over-filling issue, one possible solution is to dilute the electrolyte used while keeping the deposition time long enough for the material growth to happen.

The composition and crystallinity of the deposited materials on the patterned substrates were investigated. Fig.5.23 shows the EDX spectra taken from one GeSbTe bump (Fig.5.23(a)) and cross-sectional area within the line structure (Fig.5.23(b)). All three elements can be identified in both spectra, with no sign of other impurities except a trace of C. It is worth mentioning here that the elements ratio in both measurement do not match with  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ . This is not a surprise for EDX measurement on nanoscaled material with overlapping peaks. Hence in this circumstance, EDX serves more as a

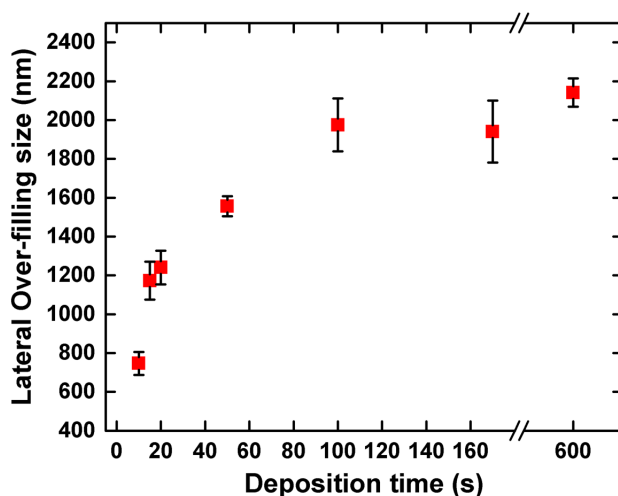


Figure 5.22: Variation of the size of over-filling at different deposition time. The values and error bars were obtained by SEM measurement of 10 bumps in a sample.

qualitative characterisation. The XRD measurement on the deposited E-beam substrates after annealing at 200°C shows similar pattern to that of the thin film. While the GST peak can be observed, the Te peak is still in existence as shown in Fig.5.24.

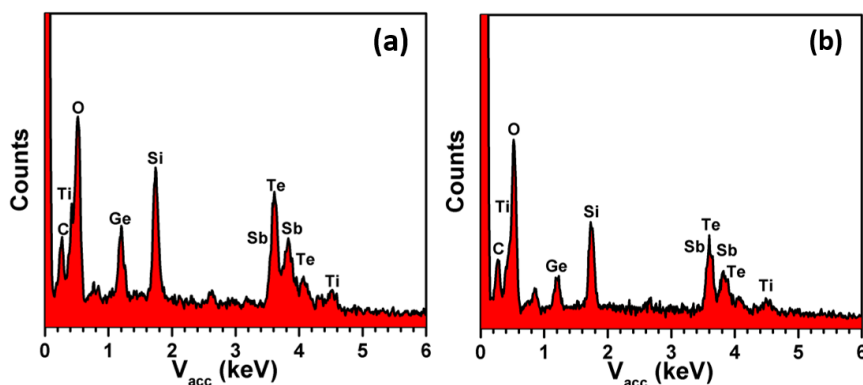


Figure 5.23: (a) EDX spectrum of an electrodeposited GeSbTe in E-beam patterned hole structure; (b) Cross-sectional EDX spectrum of electrodeposited GeSbTe in E-beam patterned line structure.

Similar Raman spectra were obtained from the as-deposited E-beam substrates. Two peaks positioned at  $124\text{ cm}^{-1}$  and  $142\text{ cm}^{-1}$  were detected (shown in Fig.5.25) which are good matches to the results of the GeSbTe thin film. All characterisations from EDX, XRD and Raman suggest that the properties of GeSbTe deposited into E-beam patterned substrates are similar to the GeSbTe thin film, indicating the consistence of electrodeposition in this work.

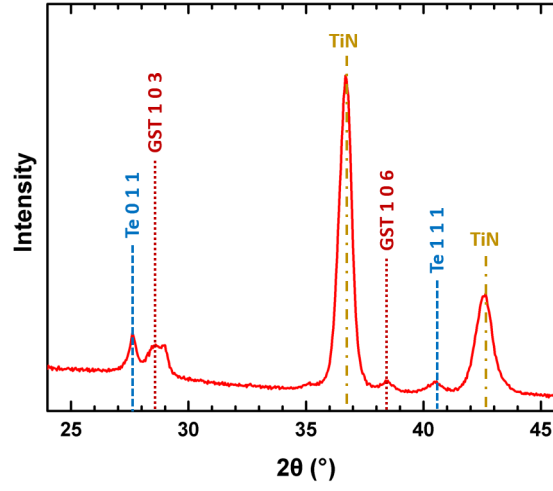


Figure 5.24: XRD spectrum of electrodeposited GeSbTe in E-beam patterned hole structure after annealing at 200°C. GeSbTe indices are based on the stable  $P\bar{3}m$  phase [171].

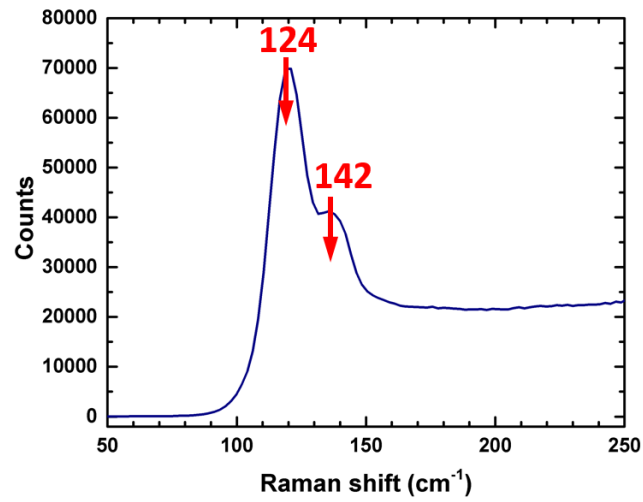


Figure 5.25: Raman spectrum of electrodeposited GeSbTe in E-beam patterned hole structure.

### 5.3.5 GeSbTe memory devices

Phase change memory devices were fabricated in order to further investigate the properties of the electrodeposited GeSbTe in this work. As the material characterisations on nanoscale sized areas are not fully conclusive, the electrical measurements are crucial in validating the phase change property of the deposited material.

**GeSbTe thin film memory devices** Fig.5.26 shows the I-V characteristic curves for the as-fabricated GeSbTe thin film memory device by DC voltage sweeping. Starting from a high resistance state, the as-deposited GeSbTe can be proved to be in the amorphous state. This matches with the XRD result on the as-deposited GeSbTe thin film. The resistivity remains high until the voltage increases to the threshold value ( $\sim 3.5$  V), where the current suddenly increases to the compliance current. This suggests the material switches rapidly from the amorphous state into a highly conductive crystalline state. The threshold voltage of the pristine device from the electrodeposited GeSbTe is slightly lower than that of the device made from sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  in this work ( $\sim 6$  V shown in Chapter 2) although they have the same thickness of 100 nm. This is possibly due to existence of nuclei in the electrodeposited GeSbTe which facilitates the crystallisation. The threshold voltage for re-crystallisation was investigated after resetting the device back to the amorphous state using an 200 ns electrical pulse of 6 V. Lower threshold voltages were observed with a uniform distribution around 1.3 V, indicating a stable programming region was formed within the device, as shown in Fig.5.27.

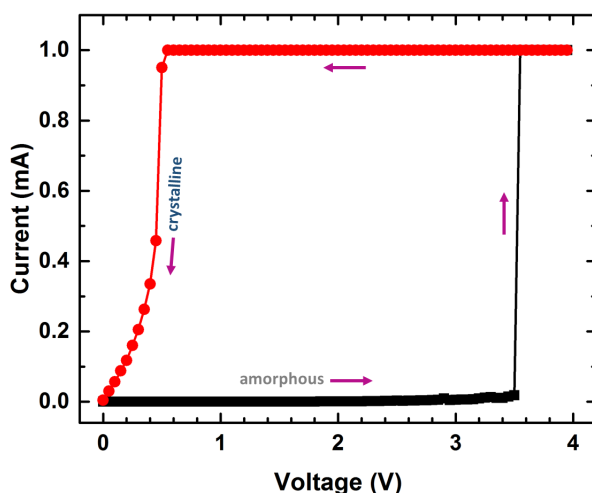


Figure 5.26: I-V characteristic of pristine  $50\mu\text{m}$  GeSbTe thin film memory device from electrodeposition.

The endurance of the device is studied using electrical pulsing to both set and reset the device. An electrical pulse rated at 2 V, 1 ms was applied for the set operation. For the

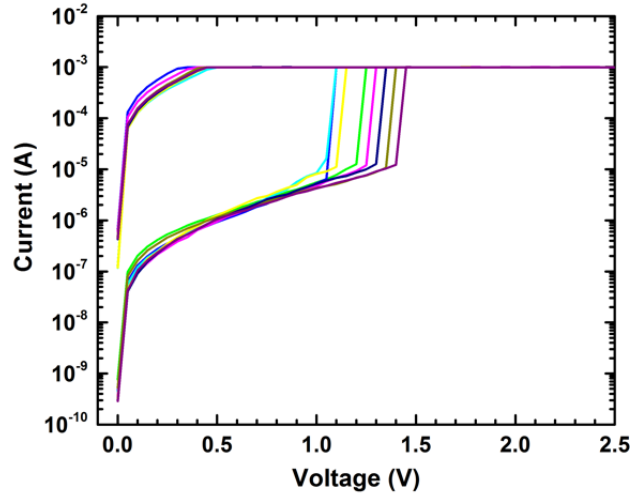


Figure 5.27: I-V characteristics for the re-crystallisation programming of the 50  $\mu\text{m}$  electrodeposited GeSbTe thin film memory device.

reset operation, 200 ns pulses with different voltages were used. The set-up of electrical pulses is shown in Fig.5.28, where a read pulse of 0.1 V is applied after each set and reset pulse to get the resistance of the device. Fig.5.29(a) shows the first 100 cycles of the device reset by a 4 V pulse where a reduction of reset resistance can be observed after 80 cycles, showing a typical “stuck-set” behaviour as discussed in Chapter 2. However, this “stuck-set” is not permanent as an increase of reset voltage can slowly bring the reset resistance back to the higher level. This is shown in Fig.5.29(b) in which a larger voltage of 5 V was applied. The reset resistance increases gradually back to the original level within the first 10 cycles. It is noted that there was a fluctuation of the reset resistance, though at least one order of magnitude was displayed for the ratio between set and reset states. Compared with our sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  devices in Chapter 2, this electrodeposited GeSbTe showed better switching behaviour with better uniformity and endurance.

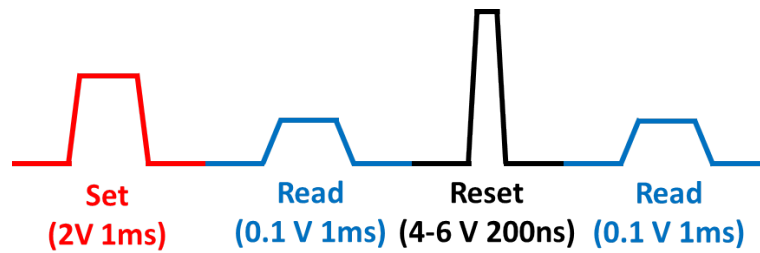


Figure 5.28: Electrical pulse sequence for the endurance test of 50  $\mu\text{m}$  electrodeposited GeSbTe phase change memory devices.

The reset pulse was then adjusted to 6 V where a good endurance and stable reset

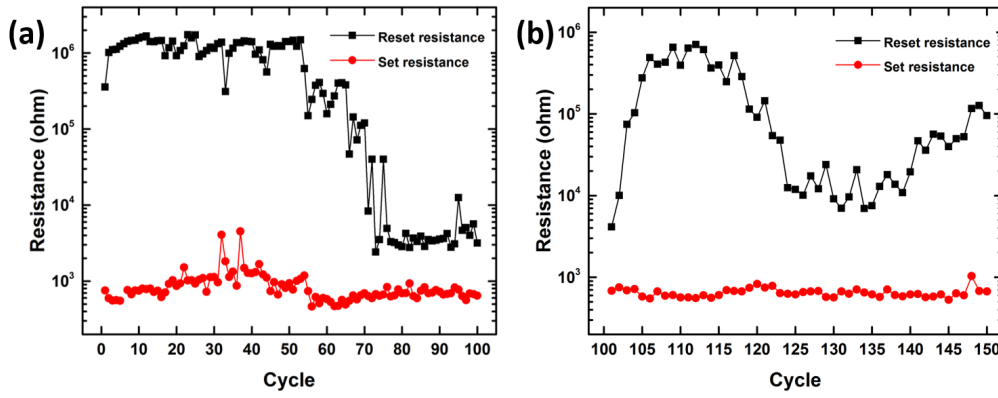


Figure 5.29: Endurance characteristics of the 50  $\mu\text{m}$  electrodeposited GeSbTe memory device using first a 4 V reset pulse (a) and then a 5 V reset pulse (b). The “stuck-set” issue in (a) featured by the reduction of reset resistance can be mitigated by increasing the reset voltage in (b).

resistance was obtained as shown in Fig. 5.30. The device shows a good endurance up to 180 cycles without failure. More importantly, a good resistance ratio of  $\sim 10^3$  remained between the set and reset states.

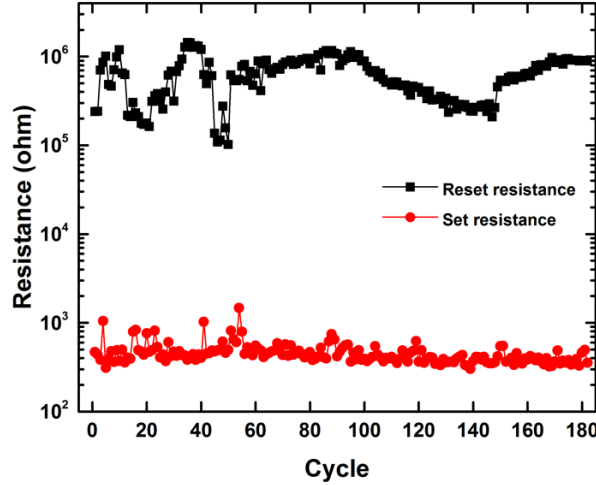


Figure 5.30: The endurance characteristic of the 50  $\mu\text{m}$  electrodeposited GeSbTe thin film memory device with sequences of reset pulses (6 V, 200 ns) and set pulse (2 V, 1 ms).

**GeSbTe micro- and nano-patterned memory devices** Similar switching behaviours were also observed on GeSbTe micro-patterned memory devices. Fig. 5.31 shows a typical endurance cycling test for a 20  $\mu\text{m}$  device using set pulses of 3 V, 1 ms and

reset pulses of 4 V, 200 ns. Stable and repetitive SET-RESET transitions were again observed with a good resistance ratio of around 3 orders.

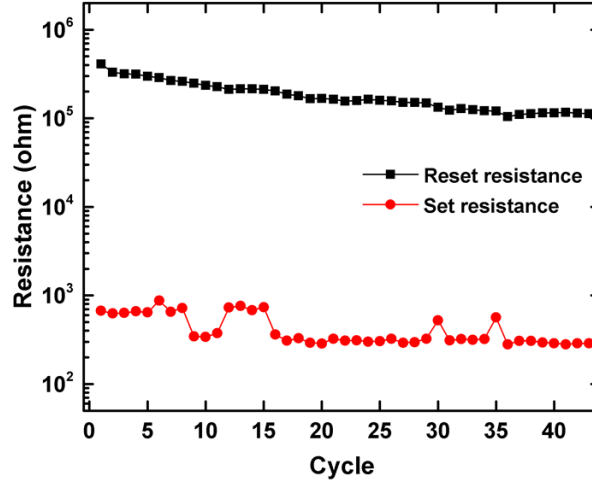


Figure 5.31: The endurance characteristic of a 20  $\mu\text{m}$  GeSbTe memory device with sequences of reset pulses (4 V, 200 ns) and set pulse (3 V, 1 ms).

For GeSbTe nano-patterned memory devices, a larger proportion of devices were found to be open circuit after the fabrication processes. This is likely due to the breakage of TiN top electrode over the over-filled GeSbTe on the nano-patterned holes as shown in Fig. 5.21. However, for the remaining working devices, electrical switchings were also achieved. Fig. 5.32 shows a DC sweeping of a non-pristine 100 nm GeSbTe memory device. The threshold switching behaviour from amorphous to crystalline state can be clearly observed at 1.7 V.

Fig. 5.33 shows the measured device resistance for a 100 nm GeSbTe memory device as a function of reset voltages. In this case, the device was subjected to a sequence of voltage pulses of constant width (200 ns) and varying magnitude, and the device resistance was measured at 0.1 V after each pulse. The initial low-resistance state corresponds to a resistance of  $8.0 \times 10^4 \Omega$ . This low-resistance state remains till 6 V and then begins to increase sharply to high-resistance state of  $1.3 \times 10^6 \Omega$  at 7 V. Fig. 5.34 illustrates a programming cycle of a 100 nm GeSbTe memory device switched between high- and low-resistance states repeatedly. The device set operation here was done with DC sweeping, and the reset operation was accomplished with a 7 V, 200 ns pulse. The electrical measurements of GeSbTe memory devices suggest good phase change property of the GeSbTe material electrodeposited in this work, and this good property remains even when scaled down to 100 nm.

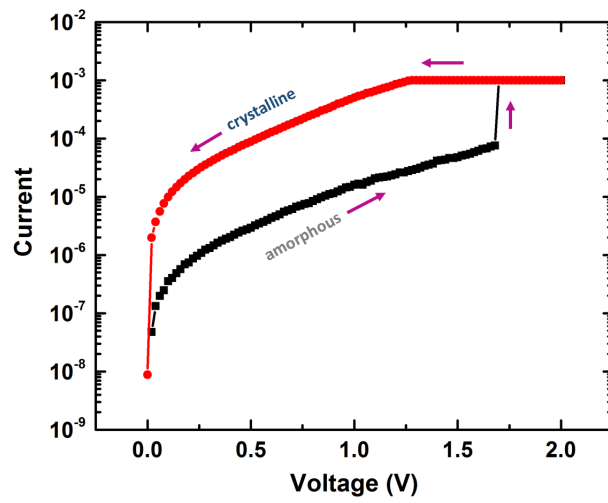


Figure 5.32: I-V characteristic of a non-pristine 100 nm GeSbTe memory device from electrodeposition.

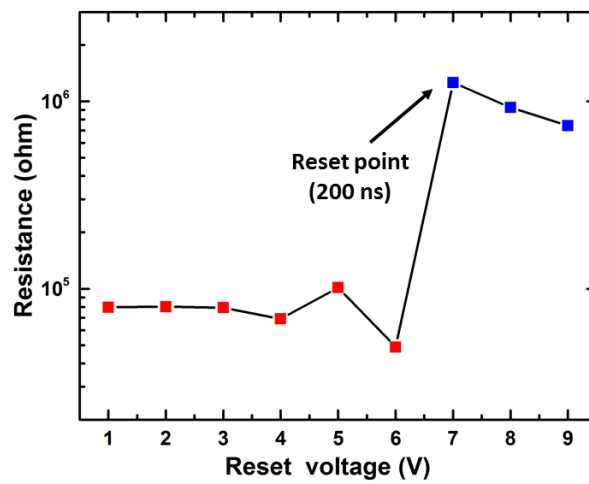


Figure 5.33: Switching behaviour of a 100 nm GeSbTe memory device as a function of reset pulse voltage. The pulse width is 200 ns.

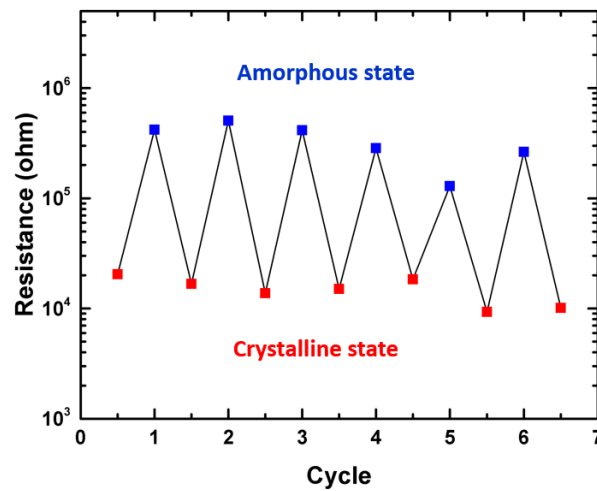


Figure 5.34: Repeated resistance measurements of a 100 nm GeSbTe memory device. Device was switched between high- and low-resistance states using voltage pulse (7 V, 200 ns) and DC sweeping (3 V), respectively.

## 5.4 Summary

In this chapter, GeSbTe phase change material was deposited by non-aqueous electrodeposition. High purity thin films were obtained with good uniformity and smooth surface. EDX and Raman measurements confirmed the composition of the deposited films. XRD data shows a phase change behaviour of the as-deposited film from amorphous to crystalline at a temperature  $\sim 150^\circ\text{C}$ , which is a good match with sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ .

Electrodeposition into nano-patterned holes shows a good uniformity with homogeneous GeSbTe bump obtained in each hole. The material composition was also confirmed by EDX, XRD and Raman measurements. Selective deposition into hole sizes of  $\sim 50$  nm was presented with a great potential to go even further down to sub-20 nm. The issue of hole over-filling was discussed with potential solutions suggested.

Electrical measurements on GeSbTe memory devices display a good switching behaviour which is better than the sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  fabricated in this work. With the high quality of material deposited and the ability of filling nano-scale holes, electrodeposition demonstrated in this work can be considered to be a novel promising preparation technique for PCRAM devices.



## Chapter 6

# Selective Chemical Vapour Deposition of Chalcogenide Phase Change Materials

### 6.1 Introduction

Apart from electrodeposition discussed in the previous chapter, chemical vapour deposition (CVD) as an alternative for depositing chalcogenide phase change materials has also been studied in this work. CVD enables the production of thin films with superior quality compared to those obtained by sputtering in terms of conformity, coverage and stoichiometry control. Beside, it also enjoys the advantages of providing materials with higher purity and most importantly, expanding the scope for potential new phase change materials. Many metal chalcogenide materials can be deposited via CVD techniques and this has stimulated a large amount of work on the development of tailored CVD precursors for their production. Phase change materials like GeSb, Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> have been successfully deposited by CVD [175, 176, 177].

Despite being a popular method for depositing phase change materials, CVD has been mostly used to achieve planar films rather than selective hole filling. Admittedly, area selective growth is never a natural feature for CVD comparing with electrodeposition. Nevertheless, selective deposition onto one surface in the presence of another surface is still possible [178]. One notable example is the selective CVD of metals which has been comprehensively reviewed by Hampden-Smith *et al.* [179, 180] with a variety of mechanisms proposed. Nucleation is suggested to play a vital role in the selective deposition behaviour and can be affected by both chemical and physical approaches.

Selective growth of phase change materials inside a particular area (e.g. contact hole for PCRAM) could be advantageous as discussed in the previous chapter. Examples of area

selective binary (or ternary) compound semiconductor deposition via CVD are rare, with only few notable examples were found on phase change materials. Choi *et al.* reported a selective growth of stoichiometric GST on the TiN plugging material in the contact hole formed in the SiO<sub>2</sub> dielectric layer by using multiple precursors (Ge(i-C<sub>4</sub>H<sub>9</sub>)<sub>4</sub>, Sb(i-C<sub>3</sub>H<sub>7</sub>)<sub>3</sub>, and Te(i-C<sub>3</sub>H<sub>7</sub>)<sub>2</sub>) [181]. This was followed by a more throughout study of the substrate influence on the selective deposition behaviour [182]. The substrate dependent growth behaviour was attributed to the electron donation from the substrate. Surfaces with more free electrons like conductive TiN surface and heavily reduced TiO<sub>2</sub> surface have a much higher growth rate of GeSbTe comparing with insulating surfaces such as SiO<sub>2</sub> and HfO<sub>2</sub>. Eom *et al.* demonstrated a selective deposition of (GeTe)<sub>(1-x)</sub>(Sb<sub>2</sub>Te<sub>3</sub>)<sub>x</sub> within 120 nm diameter pores by atomic layer deposition (ALD) using Te(SiMe<sub>3</sub>)<sub>2</sub>, Ge(OMe)<sub>4</sub> and Sb(OEt)<sub>3</sub> [183].

This chapter aims to study the selective chemical vapour deposition behaviour of depositing chalcogenide phase change materials. A group of binary chalcogenides, including Ga<sub>2</sub>E<sub>3</sub> (E = Se or Te), SnSe<sub>2</sub>, TiSe<sub>2</sub>, Bi<sub>2</sub>Te<sub>3</sub> and Sb<sub>2</sub>Te<sub>3</sub> will be deposited by CVD using home-made single precursors. In most CVD cases, dual or multiple sources have to be used for different elements. Being able to deposit alloys using single source reagents can be advantageous as it can offer improved stoichiometry and fewer defects, as well as often being safer and easier to handle. Also to the best of our knowledge, no selective deposition behaviour was observed by single source CVD reagents.

Ga<sub>2</sub>Se<sub>3</sub> has very interesting electrical and optical properties and has shown promising memory switching behaviour [184]. Ga<sub>2</sub>Te<sub>3</sub> is also an attractive material for phase change memory applications due to its high crystallization temperature (446.9 °C), and its wider band gap ( $E_{opt} = 1.22$  eV at 273 K) and higher room temperature resistivity in the crystalline state comparing with Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> [100].

SnSe<sub>2</sub> is a narrow band-gap (*ca.* 0.9 eV) semiconductor and is of interest for a number of optical and electronic applications[185, 186, 187]. The study of Sn-Se compound system as new phase change materials has also attracted significant interest during recent years [188], and it was found that SnSe<sub>2</sub> is one of the most promising candidates for a new generation of phase change material. It has a fast recrystallisation time around 20 ns and a more than 10<sup>5</sup> times resistivity contrast which is comparable to that of Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. Besides, SnSe<sub>2</sub> enjoys a higher crystallization temperature (220°C) than Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> (150°C), which implies a better data retention time. All these properties are favourable in the application point of view. The deposition of SnSe<sub>2</sub> films has been reported via different methods. Chung *et al.* deposited thin films of SnSe<sub>2</sub> via evaporation from single element sources in a molecular beam epitaxy (MBE) deposition system [188]. The as-deposited SnSe<sub>2</sub> film was found to be in amorphous state. Wang *et al.*, on the other hand, reported the use of chalcogenidometallate clusters as a solution-processable precursor to SnSe<sub>2</sub>. The precursor was first spin-coated onto substrates and then thermally decomposed into a crystalline SnSe<sub>2</sub> film [189]. Boscher *etal.* presented

an atmospheric pressure chemical vapour deposition of  $\text{SnSe}_2$ ,  $\text{SnSe}$  and  $\text{SnSe-SnSe}_2$  thin films from the reaction of  $\text{SnCl}_4$  and diethyl selenide on glass [190]. The deposition temperature varied from  $350^\circ\text{C}$  to  $650^\circ\text{C}$  while pure  $\text{SnSe}_2$  films could only be obtained at certain temperature and position on the substrate, and the rests are  $\text{SnSe}$  and mixture of  $\text{SnSe-SnSe}_2$ . This has largely hindered its application as phase change material.

$\text{TiSe}_2$  is one of the most widely studied metal chalcogenides mainly because of its intriguing electronic properties.  $\text{TiSe}_2$  has a small bandgap of 0.15 eV [191] and exhibits charge density wave transitions at lower temperatures and superconductivity with Cu intercalation [192] in addition to its semi-metallic behaviour. Transitional metal dichalcogenides like  $\text{TiSe}_2$  are emerging as important functional materials [193], making them promising candidates for spintronics [194], energy storage devices [195], electrocatalysts for hydrogen evolution [196] and as high performance materials for optoelectronics [197].

$\text{Bi}_2\text{Te}_3$  is a layered semiconductor with a narrow band-gap of 0.16 eV, and its alloys are commonly used in commercial thermoelectric (TE) devices as they have among the best room temperature thermoelectric properties of known bulk materials [198, 199]. However,  $\text{Bi}_2\text{Te}_3$  was also found to possessing reversible memory switching properties with recent finding showing  $\text{Bi}_2\text{Te}_3$  a considerable promise as building blocks for phase change memory [200].

$\text{Sb}_2\text{Te}_3$  also has a narrow band-gap of 0.28 eV. Unlike  $\text{Bi}_2\text{Te}_3$ ,  $\text{Sb}_2\text{Te}_3$  is a vital component of the popular ternary  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and has been widely used in rewritable optical media. Although its relative low crystallization temperature ( $< 100^\circ\text{C}$ ) has limited the use of  $\text{Sb}_2\text{Te}_3$  in phase change memory devices, significant research interests have still been drawn to improve its crystallization characteristic and electrical properties due to its faster phase change speed and lower power consumption because of its growth-dominated crystallization process and low melting point when comparing with nucleation dominated  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  [75]. Great improvements have been achieved by doping  $\text{Sb}_2\text{Te}_3$  with different elements such as N [71], Si [69, 68], Al [76] and etc..

Selective deposition behaviour of the six chalcogenide materials will be investigated using lithographically patterned substrates. Trend of selective deposition as well as the origins of this exceptional selectivity will also be discussed. The compositional (EDX and XPS), structural (Raman, XRD, SEM, AFM) and electrical (Hall measurements) properties of the deposited films will be presented as well.

## 6.2 Experiment

### 6.2.1 Precursor preparation and characterisation

The precursor preparation and characterisation in this chapter were conducted by Dr. Kathryn George for  $\text{Ga}_2\text{E}_3$  ( $\text{E} = \text{Se}$  or  $\text{Te}$ ), Dr. Chitra Gurnani for  $\text{SnSe}_2$ ,  $\text{TiSe}_2$  and  $\text{Bi}_2\text{Te}_3$  and Dr. Sophie L. Benjamin for  $\text{Sb}_2\text{Te}_3$  using Schlenk, vacuum line and glove-box techniques under a dry nitrogen atmosphere. Table 6.1 lists out all the precursors used in this work, the detailed synthesis and characterisation information of these precursors can be found in our research papers [201, 202, 203, 204, 205].

Table 6.1: List of single source precursors used in this chapter.

Materials	Precursors
$\text{Ga}_2\text{Se}_3$	$\text{GaCl}_3(\text{Se}_n\text{Bu}_2)$ $\text{GaCl}_3\{^n\text{BuSe}(\text{CH}_2)_2\text{Se}^n\text{Bu}\}$
$\text{Ga}_2\text{Te}_3$	$\text{GaCl}_3(\text{Te}_n\text{Bu}_2)$
$\text{SnSe}_2$	$\text{SnCl}_4\{^n\text{BuSe}(\text{CH}_2)_2\text{Se}^n\text{Bu}\}$ $\text{SnCl}_4\{^n\text{BuSe}(\text{CH}_2)_3\text{Se}^n\text{Bu}\}$
$\text{TiSe}_2$	$\text{TiCl}_4(^n\text{Bu}_2\text{Se})_2$
$\text{Bi}_2\text{Te}_3$	$\text{BiCl}_3(\text{Te}^n\text{Bu}_2)_3$
$\text{Sb}_2\text{Te}_3$	$\text{MeSb}(\text{Te}^n\text{Bu})_2$

### 6.2.2 Substrate preparation and pre-treatment

Similar to the previous chapter,  $\text{SiO}_2/\text{TiN}$  lithographically patterned substrates were prepared in order to study the selectivity between the conductive TiN surface and insulating  $\text{SiO}_2$  surface. Selective deposition of chalcogenide alloys into TiN surface is particularly favoured in the application point of view. Normally for device fabrication of confined structures, a process of etching is inevitable, while for phase change material, its properties could be deteriorated during the etching process. Hence, being able to deposit the material selectively into a specific conductive region (holes or trenches) on a patterned substrate will largely facilitate the fabrication process and enhance the device performance. Photolithography was used to pattern features with sizes ranging from  $1\text{ }\mu\text{m}$  to  $100\text{ }\mu\text{m}$ . A layer of  $\text{SiO}_2$  film with thickness of  $1\text{ }\mu\text{m}$  was deposited on the TiN films and subsequently patterned and etched. The details of photolithography and etching processes can also be found in the previous chapter. To investigate the selective deposition behaviour in nanoscale, features with sizes from  $1000\text{ nm}$  to  $100\text{ nm}$  were patterned by E-beam lithography on the photolithographically patterned substrates. This fabrication process is shown in Fig. 6.1. It is worth mentioning for E-beam patterned substrates, the  $\text{SiO}_2$  layer was reduced to  $200\text{ nm}$  to maintain a reasonable aspect ratio.

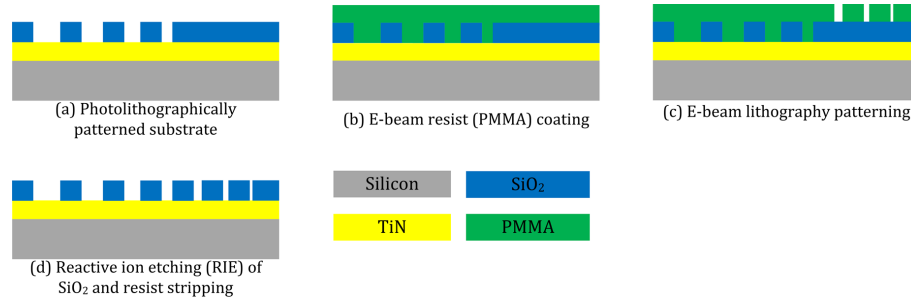


Figure 6.1: Fabrication process of E-beam patterned substrate for selective chemical vapour deposition with sizes ranging from 1000 nm to 100 nm.

In addition, to help us get a better understanding of the surface influence on the selectivity,  $\text{SiO}_2/\text{Si}$  patterned substrates were fabricated to study the selectivity between Si and  $\text{SiO}_2$ . This was done by photolithographically patterning the  $\text{SiO}_2$  films and then reactive-ion etching the exposed  $\text{SiO}_2$  area away. Fig. 6.2 illustrates the 3-D layout of these two patterned substrates.

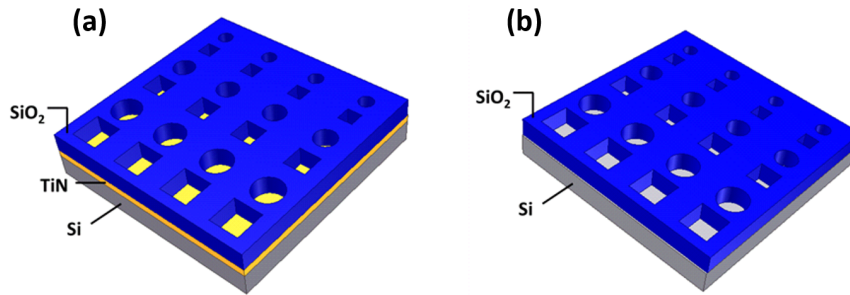


Figure 6.2: 3-D cartoon image for patterned substrates: (a)  $\text{SiO}_2/\text{TiN}$  and (b)  $\text{SiO}_2/\text{Si}$ .

The properties of the deposited materials were characterised in the form of thin films. This was achieved by depositing those materials onto unpatterned substrates ( $\text{SiO}_2$  on top of Si in this work). All patterned and unpatterned substrates were subsequently cut into small tiles ( $8 \text{ mm} \times 20 \text{ mm}$ ) suitable for our CVD system.

### 6.2.3 Chemical vapour deposition of chalcogenide materials

The low pressure chemical vapour deposition (LPCVD) in this work was conducted by Dr. Kathryn George for  $\text{Ga}_2\text{Se}_3$  and  $\text{Ga}_2\text{Te}_3$ , Dr. Chitra Gurnani for  $\text{SnSe}_2$  and  $\text{TiSe}_2$ , and Dr. Sophie Benjamin for  $\text{Bi}_2\text{Te}_3$  and  $\text{Sb}_2\text{Te}_3$ . The experiment set-up is shown in Fig. 6.3. For a typical deposition, both precursor and substrates were loaded into a closed-end quartz tube in glove-box. The amount of precursors loaded varies for each

deposition. Large doses ( $\sim 100$  mg) were normally used to achieve thick films while small doses ( $\sim 5$  mg) were used for thinner films. For selective deposition, small doses ( $\sim 5$  mg) were applied.

The precursor, with amount varying from 5 mg to 100 mg, was first placed to the close end and then several substrates, either unpatterned or patterned substrates, were positioned end-to-end near the precursor. In this work, normally 7 identical substrates were placed for each deposition. After loading the substrates, the tube was set in a furnace such that precursor was outside the heated zone; the tube was evacuated, then heated to the set temperature under 0.0067 kPa and the furnace was allowed to stabilise. The tube position was subsequently adjusted so that the precursor was moved towards the hot zone until melting was observed. The tube was then remained unmoved until the solid precursor had melted and completely evaporated (no residual precursor remained), i.e. *ca.* 1-3 h. After this, the tube was cooled to room temperature and transferred to the glove box where the tiles were removed and stored under an  $N_2$  atmosphere prior to analysis. The deposition coverage depends on different substrates as well as the position of the substrates. Table.6.2 lists deposition parameters for all six materials in this work.

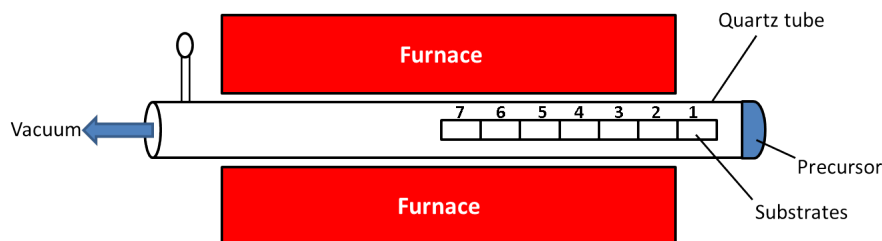


Figure 6.3: Schematic representation of LPCVD set-up (topview).

Table 6.2: List of chemical vapour deposition parameters in this chapter.

Materials	T ( $^{\circ}$ C)	Selective deposition	Film deposition		
		Precursor (mg)	Precursor thick (mg)	Precursor thin (mg)	Appearance
$Ga_2Se_3$	500	5	100	5	matt orange
$Ga_2Te_3$	500	5	100	5	shiny dark gray
$SnSe_2$	450-550	2-5	100	5	silvery-black reflective
$TiSe_2$	580	5-8	100	5	purple reflective
$Bi_2Te_3$	450-500	5		50	silvery grey
$Sb_2Te_3$	300-450	5		50	silvery grey

#### 6.2.4 Film characterisation

Scanning electron microscopy (SEM) was performed on samples at an accelerating voltage of 10 kV using a Zeiss EVO LS 25, and energy dispersive X-ray (EDX) data were

obtained with an Oxford INCAx-act X-ray detector. The cross-section SEM measurements were carried out with a field emission SEM (Jeol JSM 7500F) at an accelerating voltage of 2 kV. Atomic force microscopy (AFM) was conducted using a Veeco Dimension 3100 in tapping mode.

XRD patterns were collected in grazing incidence ( $\theta = 3^\circ$ ) using a Bruker D8 with GADDS diffractometer except to look for preferred orientation, when a Rigaku Smart-Lab system with a 2-bounce primary monochromator were used. All systems use Cu-K $\alpha$  radiation. The texture coefficient was obtained by dividing the average change in intensity for reflections associated with the relevant crystallographic direction by an average of the intensity change across all reflections. Microfocus XRD patterns were collected at beam line I18 of the Diamond Light Source using 16.8 keV (0.738 Å) X-rays focussed to a  $2\ \mu\text{m} \times 4\ \mu\text{m}$  FWHM spot. An aligned optical microscope was used to locate regions of interest on the sample and diffraction patterns were collected through the 0.6 mm Si substrate and 125 nm TiN film using a  $4000 \times 2500$  pixel CCD detector; a data collection on an identical substrate with no deposited film was used to subtract the substrate contributions to the signal.

Raman scattering spectra of the deposited films were measured at room temperature on a Renishaw InVia Micro Raman Spectrometer using a helium-neon laser with a wavelength of 632.8 nm. The incident laser power was adjusted to 1 mW for all samples. Hall measurements were performed at room temperature on a Nanometrics HL5500PC with a current of 1 mA. Contact angles were determined using a Krauss DSA100 Drop shape Analyser purpose built arrangement assembled on a vibrationally isolated platform. The drop of water was expelled through a microsyringe onto the surface of the substrate. The contact angle  $\theta$  was measured using a microscope equipped with a goniometer. The contact angle was estimated as the tangent normal to the drop at the intersection between the sessile drop and the surface. All reported contact angles are the average of at least three measurements taken at different locations and have a maximum error of  $\pm 2^\circ$ .

### 6.3 Selective CVD growth in confined structures

The selective deposition behaviours of all five chalcogenides were investigated by SEM and EDX mapping to observe the distribution of materials across the TiN and SiO $_2$  surfaces. The goodness of the selectivity was judged by the smallest size where selectivity still exists.

### 6.3.1 Selective deposition of $\text{Ga}_2\text{Se}_3$ and $\text{Ga}_2\text{Te}_3$

No selectivity was observed for  $\text{Ga}_2\text{Se}_3$  films as both TiN and  $\text{SiO}_2$  surfaces were covered after deposition. LPCVD of  $\text{Ga}_2\text{Te}_3$  thin films showed a preference for deposition onto TiN over  $\text{SiO}_2$ . SEM images (Fig. 6.4) of such a film show that deposition of  $\text{Ga}_2\text{Te}_3$  is preferred onto the TiN surfaces within the photolithographically etched substrate, although the selectivity is not high and can only be observed on large TiN surfaces.

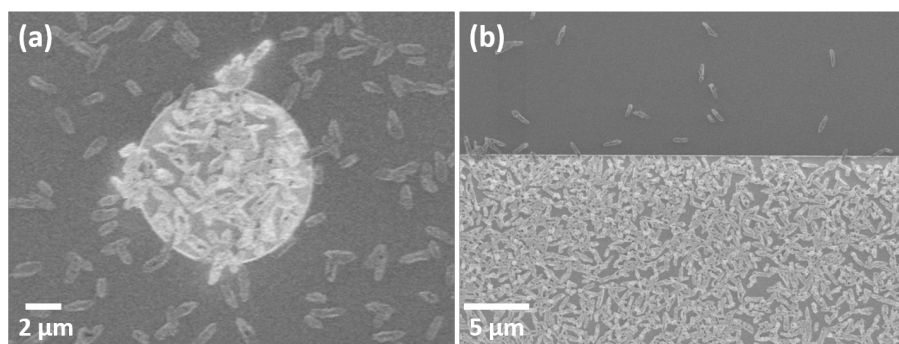


Figure 6.4: SEM image showing the preferential deposition of  $\text{Ga}_2\text{Te}_3$  onto the TiN surface ((a) inside the circle and (b) bottom half of image) relative to the  $\text{SiO}_2$  surface ((a) outside of the circle and (b) top half) of a patterned TiN/ $\text{SiO}_2$  substrate.

### 6.3.2 Selective deposition of $\text{SnSe}_2$

The selective deposition behaviour is much more prominent for  $\text{SnSe}_2$  over  $\text{SiO}_2/\text{TiN}$  patterned substrates. All  $\text{SnSe}_2$  films were found grown on exposed TiN regions within the holes. No deposition was found on  $\text{SiO}_2$ . For different hole sizes, selective deposition was observed from big holes (80 to 100  $\mu\text{m}$  diameter) to small holes (5  $\mu\text{m}$  diameter) as shown in Fig. 6.5. While a selective deposition can also be seen in 2  $\mu\text{m}$  holes, it was limited by the size of individual  $\text{SnSe}_2$  crystallites (*ca.* 1.6  $\mu\text{m} \times 2.0 \mu\text{m}$  across the hexagon). The nucleation which initiated on the TiN surface was further grown outside the hole on the  $\text{SiO}_2$  surface as shown in Fig. 6.5(d).

EDX element mapping was used to confirm that the selective deposition of  $\text{SnSe}_2$  was only occurring within the holes with growth occurring preferentially onto the TiN surface as shown in Fig. 6.6 for big holes and Fig. 6.7 for small holes. Note that TiN film underneath the  $\text{SnSe}_2$  and  $\text{SiO}_2$  films can also be detected from inside and outside the holes, while a more intense Ti in side hole indicates a thinner film of  $\text{SnSe}_2$  compared with that of  $\text{SiO}_2$ .

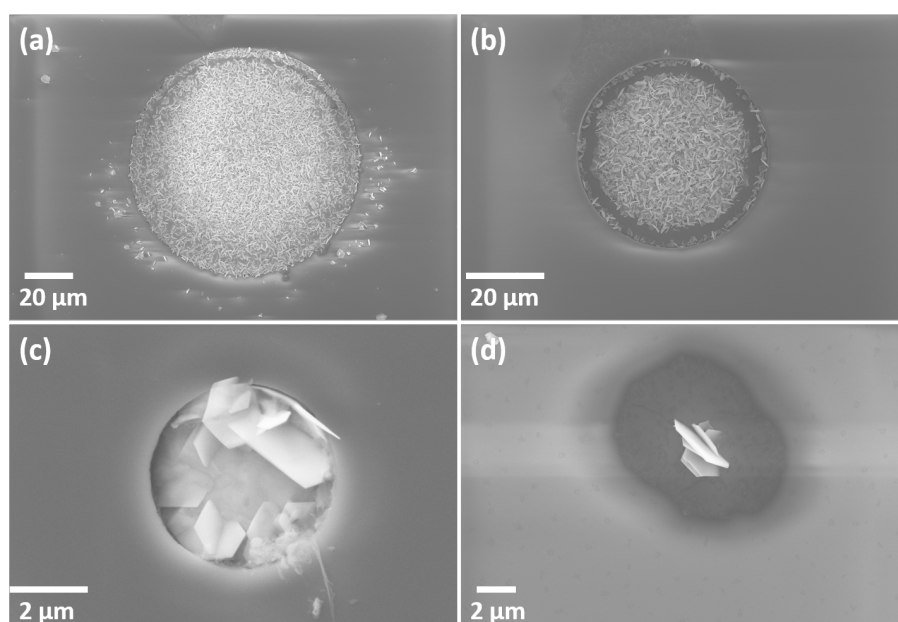


Figure 6.5: SEM images showing selective growth of SnSe<sub>2</sub> onto the TiN on a patterned SiO<sub>2</sub>/TiN substrate in the (a) hole with 100  $\mu\text{m}$  diameter, (b) hole with 50  $\mu\text{m}$  diameter, (c) hole with 5  $\mu\text{m}$  diameter and (d) hole with 2  $\mu\text{m}$  diameter.

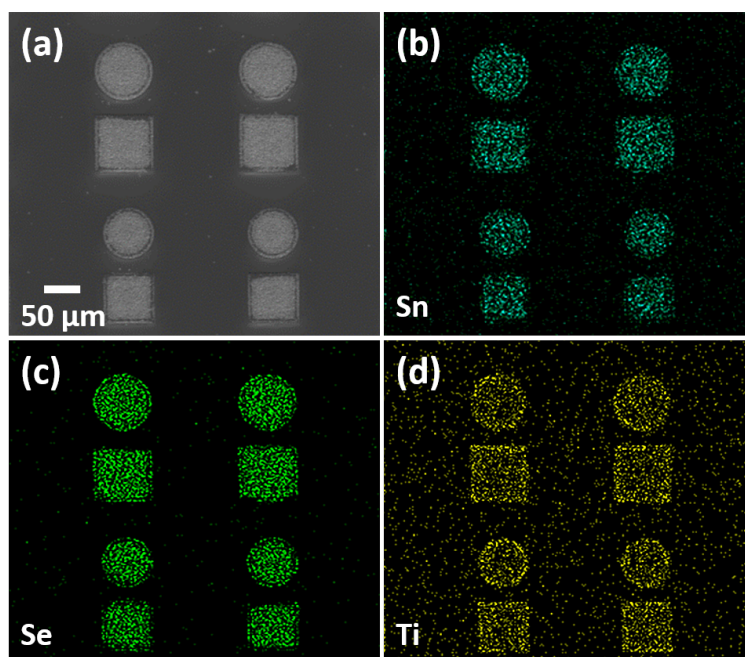


Figure 6.6: SEM image (a) and EDX element maps (b) - (d) confirming the selective deposition of SnSe<sub>2</sub> occurring only within the holes (80  $\mu\text{m}$  diameter) with growth occurring preferentially onto the TiN surface.

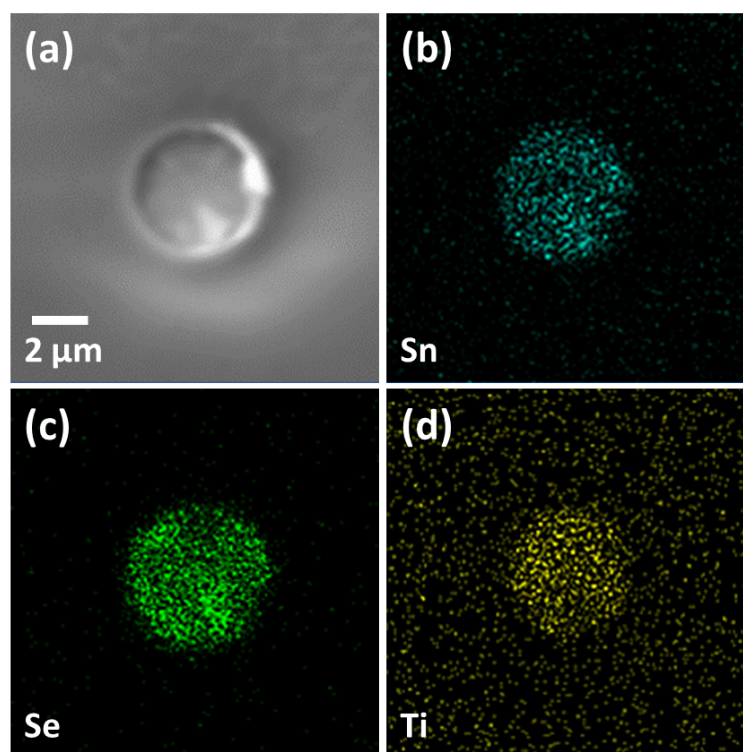


Figure 6.7: SEM image (a) and EDX element maps (b) - (d) confirming the selective deposition of  $\text{SnSe}_2$  occurring only within the holes ( $5\ \mu\text{m}$  diameter) with growth occurring preferentially onto the TiN surface.

### 6.3.3 Selective deposition of $\text{TiSe}_2$

Selective deposition experiments of  $\text{TiSe}_2$  resulted in even higher selective deposition within the conducting TiN holes of the patterned substrates compared with  $\text{SnSe}_2$  (Fig.6.8). The coverage was densest on the substrates which lay in the hotter zone of the furnace. This high substrate selectivity was observed for all sizes of holes varying from the large ( $80\text{--}100\ \mu\text{m}$ ) diameters to the smaller ( $2\text{--}5\ \mu\text{m}$ ) diameters, as illustrated in the Fig.6.9 and Fig.6.10 respectively.

This substrate selective deposition of  $\text{TiSe}_2$  is also observed for  $2\ \mu\text{m}$  diameter holes, smaller than observed for  $\text{SnSe}_2$  where this scale of selectivity was limited to  $5\ \mu\text{m}$  by the size of the individual  $\text{SnSe}_2$  crystallites ( $\sim 1.6\ \mu\text{m} \times 2.0\ \mu\text{m}$  across the hexagon). The SEM images suggest that the average size (in x-y plane) of individual  $\text{TiSe}_2$  crystallites varies from  $\sim 1.2\ \mu\text{m}$  (within  $100\ \mu\text{m}$  TiN holes) to  $\sim 600\ \text{nm}$  (within  $2\ \mu\text{m}$  TiN holes).

Microfocus X-ray diffraction experiments were performed on  $\text{TiSe}_2$  samples at beam line I18 of the Diamond Light Source using a  $2\ \mu\text{m} \times 4\ \mu\text{m}$  beam impinging on the region of sample of interest normal to the substrate and with the diffracted beam collected after passing through the substrate. Fig.6.11 shows typical diffraction patterns after subtraction of a background collected on a blank substrate. These patterns show conclusively

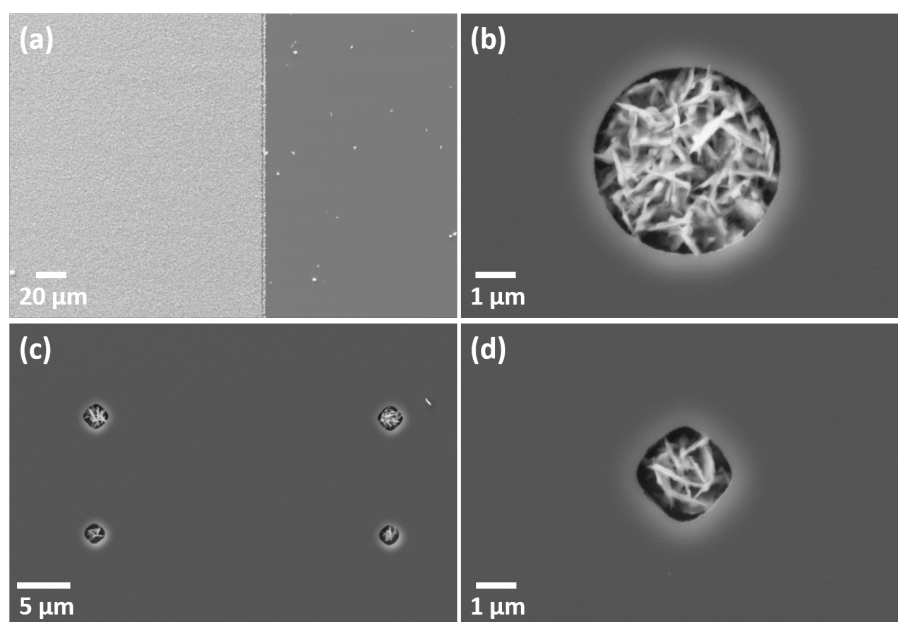


Figure 6.8: SEM images (a) showing selective growth of  $\text{TiSe}_2$  onto the TiN on a patterned TiN (left)/ $\text{SiO}_2$  (right) substrate; showing selective deposition of  $\text{TiSe}_2$  within (b)  $5\ \mu\text{m}$  and (c)-(d)  $2\ \mu\text{m}$  TiN holes of a TiN/ $\text{SiO}_2$  patterned substrate.

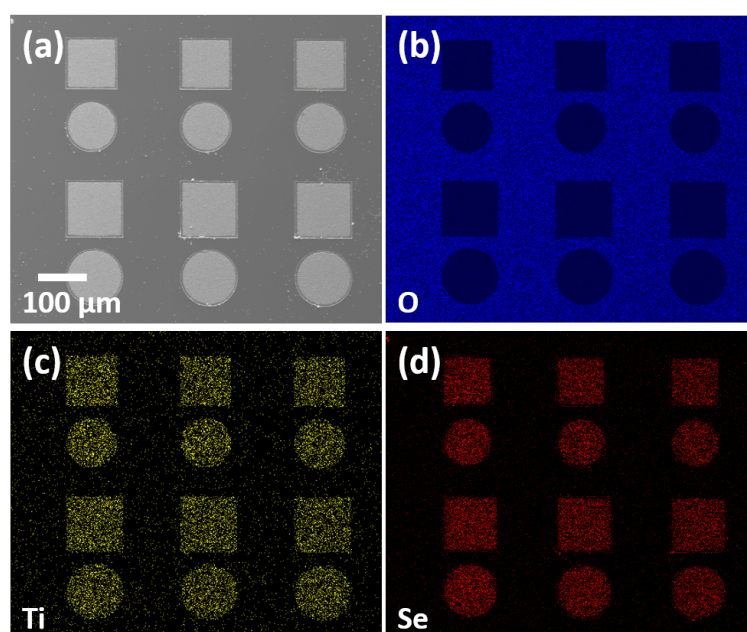


Figure 6.9: SEM image (a) and EDX element maps (b) - (d) confirming the selective deposition of  $\text{TiSe}_2$  occurring only within the holes ( $80\ \mu\text{m}$  diameter) with growth occurring preferentially onto the TiN surface.

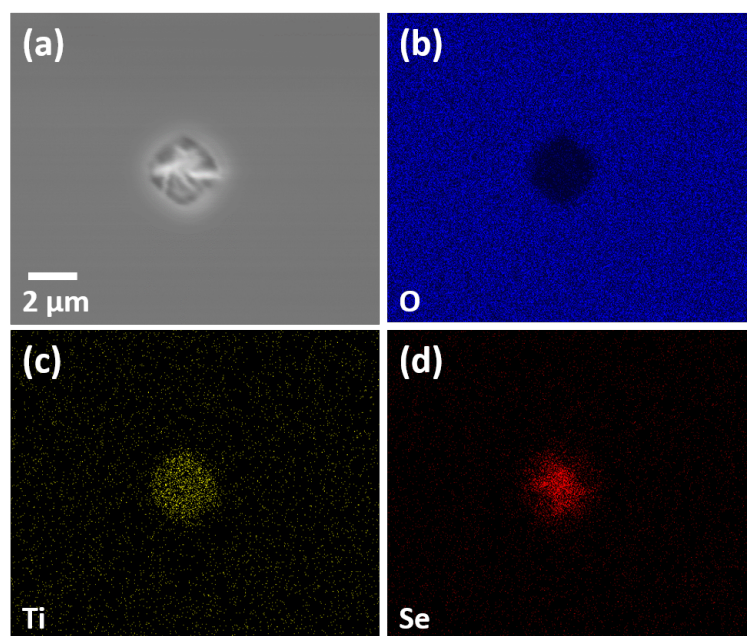


Figure 6.10: SEM image (a) and EDX element maps (b) - (d) confirming the selective deposition of  $\text{TiSe}_2$  occurring only within the holes ( $2\ \mu\text{m}$  diameter) with growth occurring preferentially onto the TiN surface.

that the same material was being produced in all hole sizes as on flat substrates. The beam size was small enough for the sampling region to be the same with these different sized holes and a grid of sample positions was collected to ensure that patterns were obtained with the beam in the center of the hole, but it was found that the patterns collected from samples deposited into smaller holes were always much more heavily textured than from those deposited in larger holes. This suggests a smaller number of crystallites in the beam footprint in smaller holes, which could be related to a smaller amount of deposit, or to larger crystallites. Examination of the crystallite sizes in SEM images Fig. 6.12 showed that both the length and thickness of crystallites increases with the hole size but that the thickness of the crystals stops increasing above  $\sim 20\ \mu\text{m}$  hole size whereas their lengths continue to increase.

The smallest holes have a diameter of  $2\ \mu\text{m}$  and a depth determined by the  $1\ \mu\text{m}$  thickness of the silica film. Combining the diffraction and SEM results shows that a smaller number of crystallites is deposited per unit area in the smaller holes and that the crystallite size is also smaller. The obvious explanations are that diffusion to the surface is less efficient than in the larger holes or that the smaller deposition area acts less efficiently to supply adsorbed species to the growth process. Neither is compelling since, with no carrier gas, the boundary layer for diffusion should be very thin and the aspect ratio of the smallest holes is not large, whereas a larger area may contain more adsorbed material, but it also has a larger area across which growth can occur. It may be that the side walls of the holes have a more significant effect on the transport of

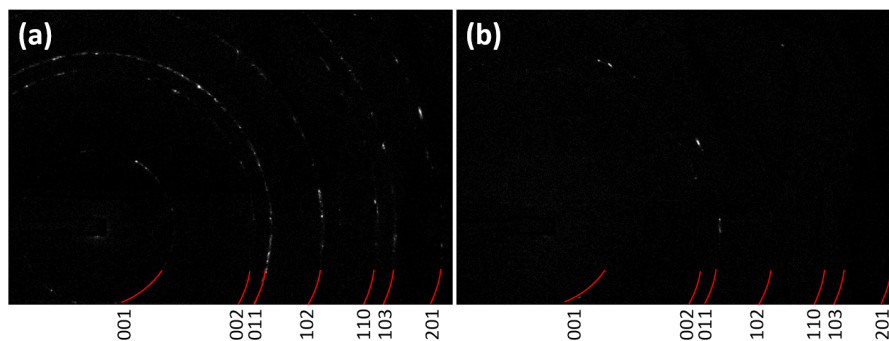


Figure 6.11: Microfocus X-ray diffraction patterns collected on  $\text{TiSe}_2$  samples selectively deposited into  $100\ \mu\text{m}$  (a) and  $5\ \mu\text{m}$  (b) holes. Similar XRD pattern was observed for  $\text{TiSe}_2$  thin films as shown in Fig.6.31.

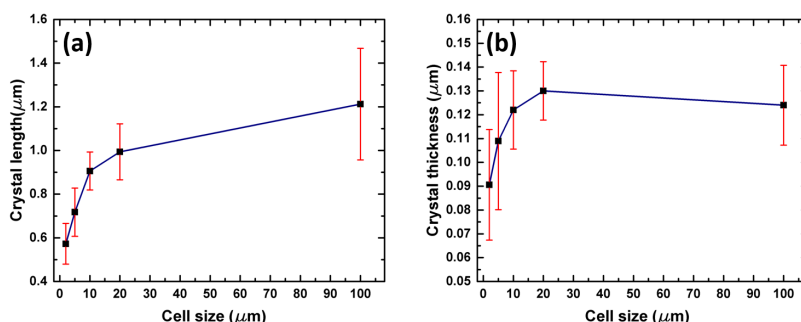


Figure 6.12: Variation of crystallite length (along a-axis of hexagonal plate) (a) and width (along c-axis) (b) with the size of hole into which the sample is deposited. The black line is to provide a guide to the eye and the values/error bars were obtained by SEM measurement of 10 crystallites in a sample.

the precursor as the hole size becomes smaller, and that this is the determining factor controlling growth into the holes.

#### 6.3.4 Selective deposition of $\text{Bi}_2\text{Te}_3$

**$\text{Bi}_2\text{Te}_3$  micro-scale selectivity** Selective deposition of  $\text{Bi}_2\text{Te}_3$  were first tried on photolithographically patterned  $\text{SiO}_2/\text{TiN}$  substrates with hole sizes ranging from  $100\ \mu\text{m}$  to  $2\ \mu\text{m}$ . The quantity of precursor plays an important role for selectivity. It was found an excess amount of precursor could lead to overfilling of the holes accompanied by some deposition onto the  $\text{SiO}_2$  layer, whereas too little precursor resulted in incomplete filling. However, careful control of the quantity of reagent allows a continuous film to be deposited within each well. Under carefully controlled conditions  $\text{Bi}_2\text{Te}_3$  was deposited into these  $\text{TiN}$  holes with excellent substrate selectivity. The holes were filled with crystals while no deposition was observed on the surrounding  $\text{SiO}_2$  insulating layer

(Fig.6.13). In addition, significant reduction of crystal size was observed after the deposition temperature was lowered from 500°C to 450°C as shown in Fig.6.13(d). However, a further decrease of deposition temperature to 400°C resulted in very little material being deposited. Fig.6.14 shows a EDX mapping over a 2  $\mu\text{m}$  hole where both Bi and Te can were only found existed within the hole.

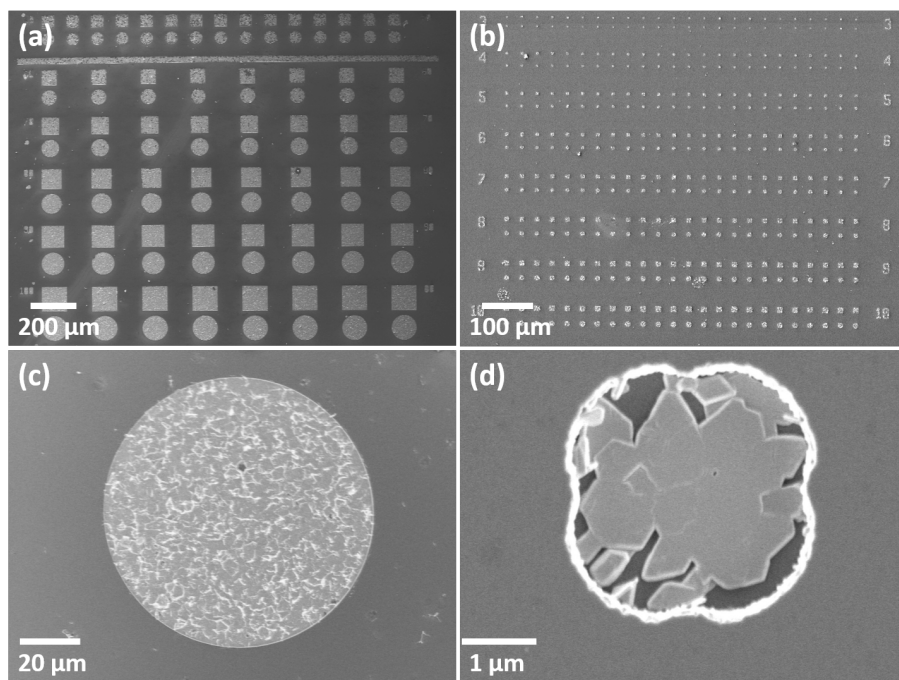


Figure 6.13: SEM image showing  $\text{Bi}_2\text{Te}_3$  selectively grown into the TiN holes of diameter (a) 50 to 100  $\mu\text{m}$  and (b) 3 to 10  $\mu\text{m}$  on a patterned  $\text{SiO}_2/\text{TiN}$  substrate array (the numbers indicate the diameter of the wells in microns in each case); (c) Magnified SEM image of a 100  $\mu\text{m}$  hole, illustrating the very high selectivity for  $\text{Bi}_2\text{Te}_3$  film growth only onto the TiN surface; (d) Magnified SEM image of a 3  $\mu\text{m}$  hole, illustrating the crystal size has been significantly reduced to  $< 1 \mu\text{m}$  due to a lower deposition temperature

**$\text{Bi}_2\text{Te}_3$  nano-scale selectivity** In order to investigate the applicability of this technique toward nanostructuring of  $\text{Bi}_2\text{Te}_3$  materials, E-Beam patterned  $\text{SiO}_2/\text{TiN}$  substrates were used for deposition. LPCVD onto these substrates resulted in selective growth of a single nanocrystal into the holes, although around 20-25% of the nanowells are empty or have nucleations. EDX measurements confirms the existence of both Bi and Te, but the low signal relative to that from the substrate precluded accurate determination of the Bi:Te ratio.

The crystals lie flat in the base of the holes with diameter of  $\geq 1 \mu\text{m}$  (Fig.6.15(a)-(b)), whereas in those of 100-200 nm diameter the individual crystallite size is larger than the wells in which they sit (generally 200-500 nm across and less than 100 nm thick). SEM images (Fig.6.15(c)-(f)) show that almost all of the crystals in these smallest wells stand

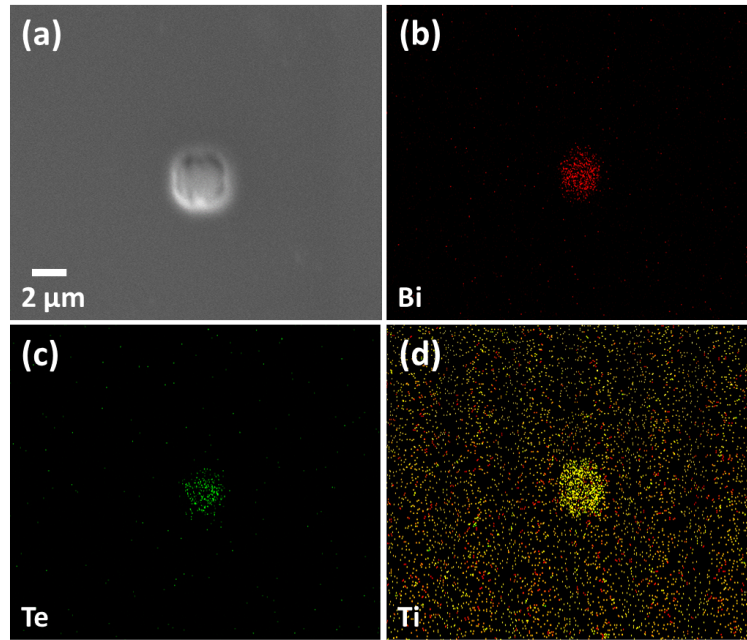


Figure 6.14: SEM image (a) and EDX element maps (b) - (d) confirming the selective deposition of  $\text{Bi}_2\text{Te}_3$  occurring only within the holes ( $2\ \mu\text{m}$  diameter) with growth occurring preferentially onto the TiN surface.

on end, occupying a larger footprint above the substrate. The orientation of crystallites in  $\leq 200\ \text{nm}$  holes is *ca.*  $90^\circ$  to those in the  $\geq 1\ \mu\text{m}$  holes. For the intermediate  $500\ \text{nm}$  holes, both behaviours were observed as shown in Fig. 6.15(g)-(h). This can be correlated with the size of the nanocrystal relative to the diameter of the hole, suggesting that the change to  $\langle 1\ 1\ 0 \rangle$  preferred orientation reduces the less favourable interactions of the larger  $\text{Bi}_2\text{Te}_3$  crystals with the  $\text{SiO}_2$  walls (Fig. 6.15(g)). This switching of the preferred orientation simply by reducing the dimensions of the recessed TiN regions is extremely unusual, and, coupled with the demonstrated ability to selectively grow crystalline  $\text{Bi}_2\text{Te}_3$  in predetermined areas, offers exciting prospects not only phase change memory but also in applications such as thermoelectric using this new precursor and LPCVD method.

### 6.3.5 Selective deposition of $\text{Sb}_2\text{Te}_3$

**$\text{Sb}_2\text{Te}_3$  micro-scale selectivity** Similar to  $\text{Bi}_2\text{Te}_3$ , the deposition of  $\text{Sb}_2\text{Te}_3$  also shows a good selectivity over photolithographically patterned substrates. SEM images show that deposition occurs exclusively onto the exposed TiN surface, with the  $\text{SiO}_2$  surface remaining bare (Fig. 6.16). The control of precursor quantity was again found to have an effect onto the thickness and morphology of the materials and the deposits can be

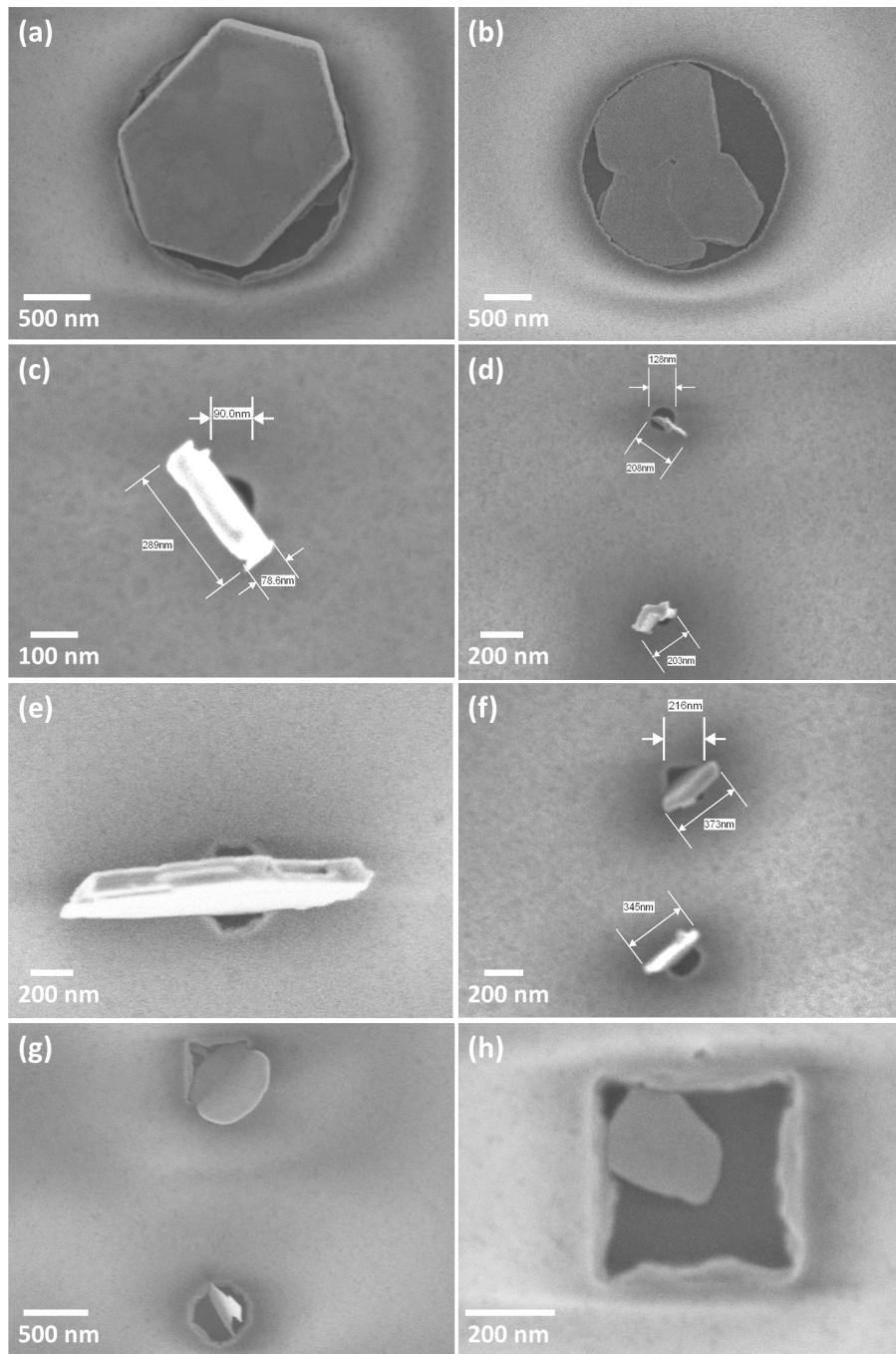


Figure 6.15: SEM images of  $\text{Bi}_2\text{Te}_3$  single nanocrystals occupying (a)-(b)  $2\ \mu\text{m}$  holes on a  $\text{SiO}_2/\text{TiN}$  patterned substrate, showing the  $\langle 0\ 0\ 1 \rangle$  preferred orientation; SEM images of individual nanocrystals of  $\text{Bi}_2\text{Te}_3$  contacting through a crystal edge to the TiN surface within (c)-(d) 100 and (e)-(f) 200 nm holes, resulting in  $\langle 1\ 1\ 0 \rangle$  preferred orientation; SEM image of  $\text{Bi}_2\text{Te}_3$  nanocrystals occupying 500 nm holes, showing both the  $\langle 1\ 1\ 0 \rangle$  preferred orientation (g) and the  $\langle 0\ 0\ 1 \rangle$  preferred orientation (h).

varied from those which protrude significantly from the surrounding silica (Fig.6.16(a)-(b)), to very thin layers of crystals which lie flat on the base of the TiN wells (Fig.6.16(c)-(d)). EDX mapping confirms both Sb and Te elements only occurring within the TiN holes as shown in Fig.6.17.

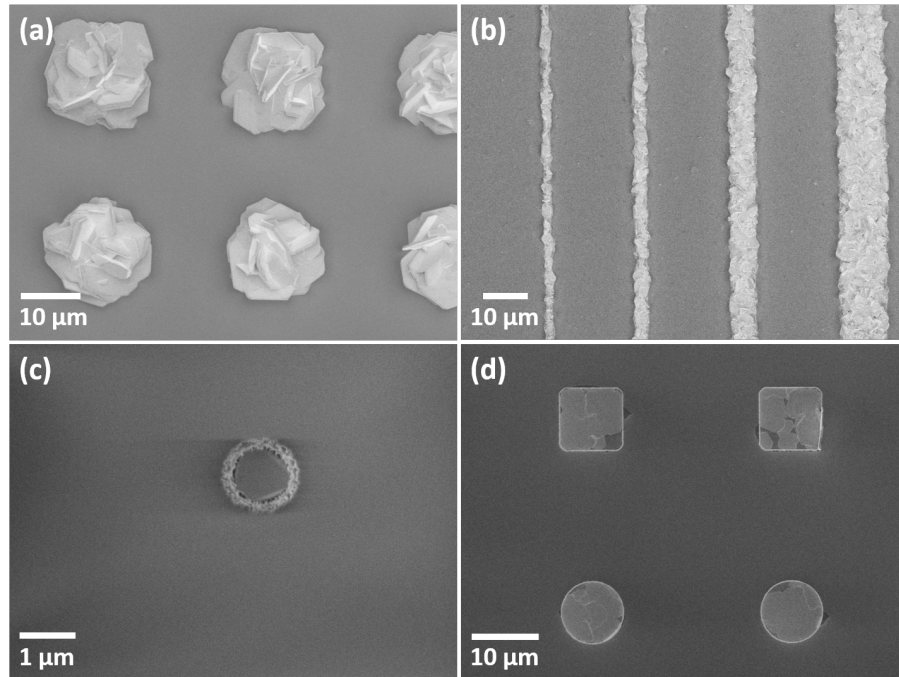


Figure 6.16: SEM image showing  $\text{Sb}_2\text{Te}_3$  selectively grown into photolithographically patterned substrates.

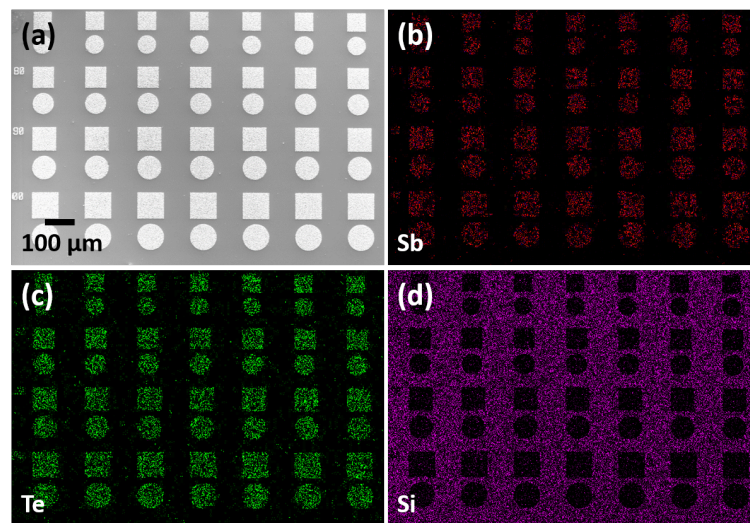


Figure 6.17: SEM image (a) and EDX element maps (b) - (d) confirming the selective deposition of  $\text{Sb}_2\text{Te}_3$  occurring only within the holes with growth occurring preferentially onto the TiN surface.

**Sb<sub>2</sub>Te<sub>3</sub> nano-scale selectivity** Excellent selectivity was maintained on the nanoscale, with very few crystals observed outside of the wells as shown in Fig.6.18. Again, similar switching of the preferred orientation from  $\langle 1\ 1\ 0 \rangle$  to  $\langle 0\ 0\ 1 \rangle$  can also be observed with the changing of hole size from 100-200 nm to 500 nm.

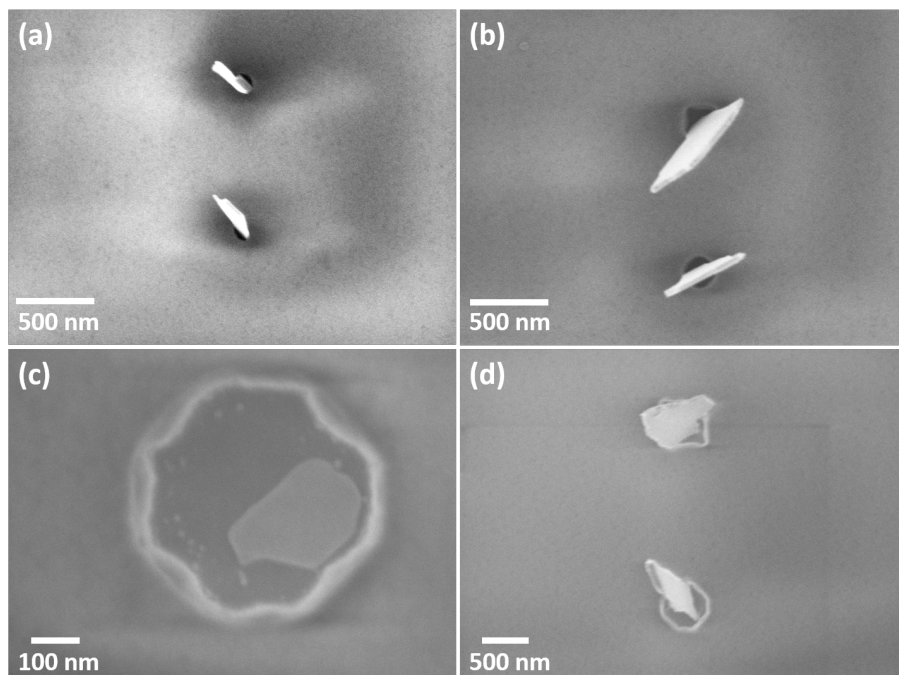


Figure 6.18: SEM images of individual nanocrystals of Sb<sub>2</sub>Te<sub>3</sub> contacting through a crystal edge to the TiN surface within (a)-(b) 100 - 200 nm holes, resulting in  $\langle 1\ 1\ 0 \rangle$  preferred orientation, and (c)-(d) 500 nm holes, resulting in both  $\langle 1\ 1\ 0 \rangle$  and  $\langle 0\ 0\ 1 \rangle$  preferred orientations.

## 6.4 Material characterisations of thin films

### 6.4.1 Film morphology

**Ga<sub>2</sub>Se<sub>3</sub>** Film morphologies were first studied by scanning electron microscopy. The deposited Ga<sub>2</sub>Se<sub>3</sub> films shows a regular morphology formed of small crystallites as shown in Fig.6.19(a). Cross-sectional SEM images of typical films reveal the film thickness is  $\sim 0.8\ \mu\text{m}$  (Fig.6.19(b)). Reagent-limited films grown by 5 mg of precursor had the same morphology (Fig.6.19(c)), but were much thinner (Fig.6.19(d)).

**Ga<sub>2</sub>Te<sub>3</sub>** SEM images of deposited Ga<sub>2</sub>Te<sub>3</sub> films show that the substrates have quite uniform coverage of the deposited film and the morphology comprises of regular rod-shaped crystallites approximately  $1\ \mu\text{m}$  in length (Fig.6.20(a)). The cross-sectional SEM (Fig.6.20(b)) shows that the film produced from LPCVD from 100 mg precursor is *ca.*

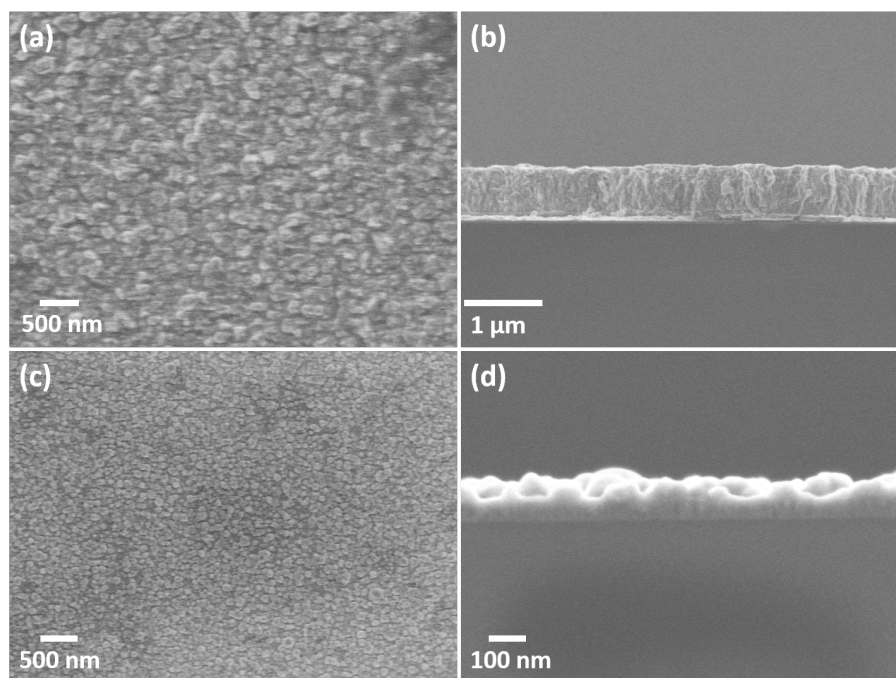


Figure 6.19: (a) Top and (b) cross-section SEM image of a  $\text{Ga}_2\text{Se}_3$  thin film grown via LPCVD using 100 mg precursor. (c) Top and (d) cross-section SEM image of a  $\text{Ga}_2\text{Se}_3$  thin film grown via LPCVD using 5 mg precursor.

4  $\mu\text{m}$  in depth. When reagent amount was reduced to 20 mg, film thickness decreased to *ca.* 2  $\mu\text{m}$  (Fig.6.20(d)) and the  $\text{Ga}_2\text{Te}_3$  crystallites also became smaller to *ca.* 100 nm (Fig.6.20(c)).

**SnSe<sub>2</sub>** For large amount of precursor (100 mg),  $\text{SnSe}_2$  deposition produced a regular morphology formed of hexagonal plate crystallites as shown in Fig.6.21(a). No significant difference was found for the morphology on different substrates. Normally, for the substrate which gave the best deposition, the coverage was around one third of the substrate and the covered film was continuous with thickness gradually decreasing from the substrate edge to the centre. At the region closer to the precursor (near the edge of the substrate), a dense, thick and compacted film was observed. While at the region further away from the precursor, the film became much thinner and discontinuous.

A much smaller amount of precursor (5 mg) resulted a much thinner film. The SEM image shows the majority of the crystallites lying flat on the substrate surface instead of standing up as shown in Fig.6.21(c). The film thickness went down from 30  $\mu\text{m}$  for the thick film (Fig.6.21(b)) to around 0.5  $\mu\text{m}$  for the thin film (Fig.6.21(d)). This flat film from smaller amount of precursor suggests that the film was first grown horizontally for a few micrometres, while with more precursor coming, it started to grown vertically, showing a strong preferred orientation which will be discussed in the crystal structure section below.

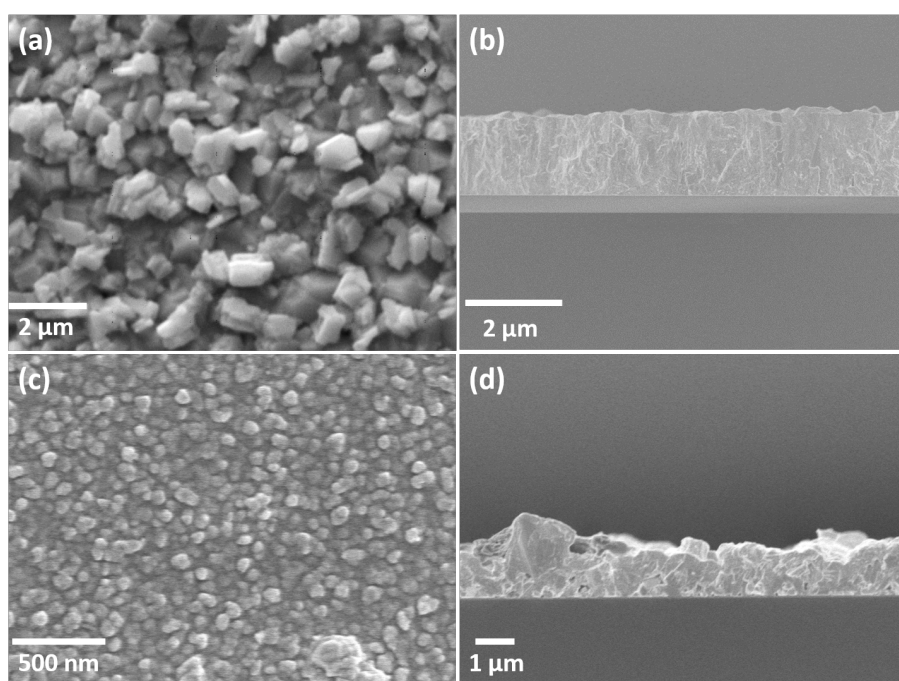


Figure 6.20: (a) Top and (b) cross-section SEM image of a  $\text{Ga}_2\text{Te}_3$  thin film grown via LPCVD using 100 mg precursor. (c) Top and (d) cross-section SEM image of a  $\text{Ga}_2\text{Te}_3$  thin film grown via LPCVD using 20 mg precursor.

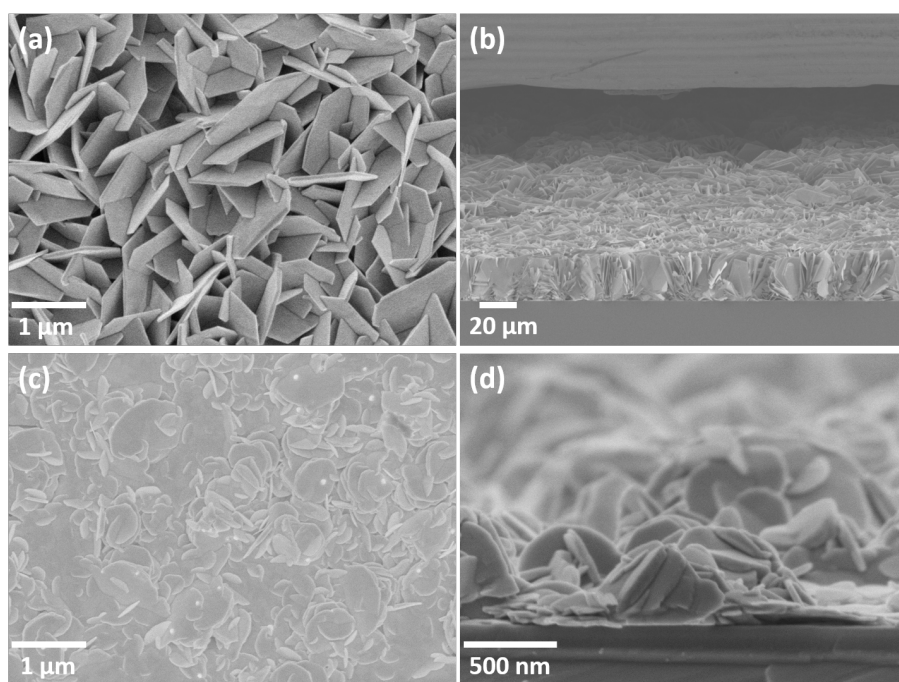


Figure 6.21: (a) Top and (b) cross-section SEM image of a  $\text{SnSe}_2$  film grown via LPCVD using 100 mg precursor. (c) Top and (d) cross-section SEM image of a  $\text{SnSe}_2$  thin film grown via LPCVD using 5 mg precursor.

**TiSe<sub>2</sub>** TiSe<sub>2</sub> depositions using 100 mg of precursor showed a regular morphology formed of hexagonal plate crystallites by SEM analysis (Fig.6.22(a)). Most of the crystallites are aligned with their flat surfaces perpendicular to the substrate surface and cross-sectional SEM showed these films were 4-5  $\mu\text{m}$  thick (Fig.6.22(b)). However, cross-section SEM analysis of reagent-limited films grown at 600°C using 5-7 mg showed films that were much thinner (*ca.* 300 nm) (Fig.6.22(c) and (d)).

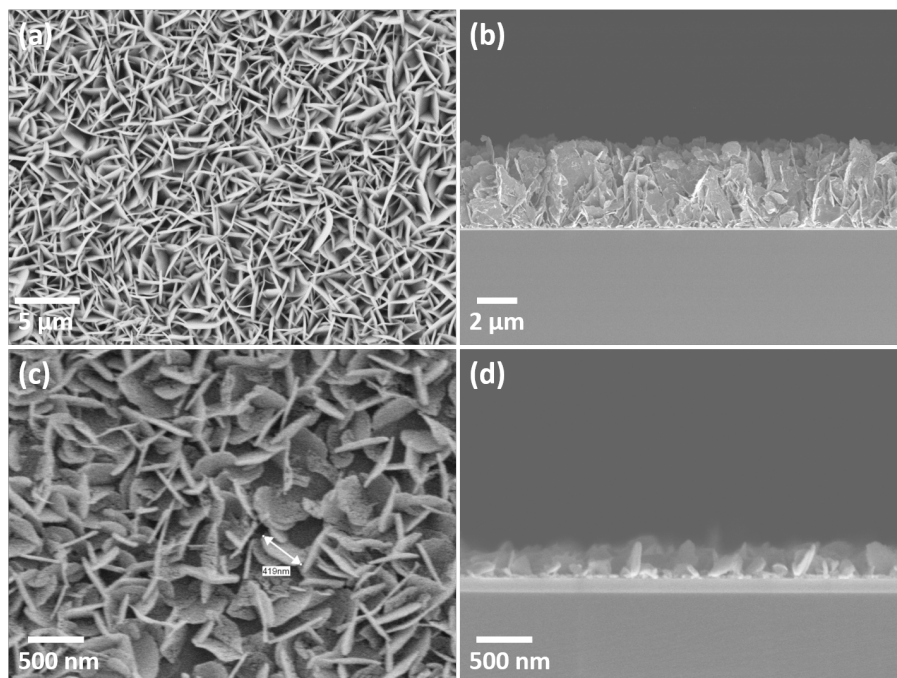


Figure 6.22: SEM images of hexagonal TiSe<sub>2</sub>: (a) top view and (b) cross section of film deposited from 100 mg of reagent, showing the film thickness of  $\sim 4 \mu\text{m}$ , with hexagonal crystallites essentially randomly oriented on the substrate; (c) top view of a much thinner film deposited using 5 mg of reagent; (d) cross-section of this thin film.

**Bi<sub>2</sub>Te<sub>3</sub>** SEM images of deposited Bi<sub>2</sub>Te<sub>3</sub> films are shown in Fig.6.23. Films are formed of continuous hexagonal Bi<sub>2</sub>Te<sub>3</sub> crystals with size around 2  $\mu\text{m}$  compiling on each other. Film thickness was found to be *ca.* 1.0  $\mu\text{m}$ .

**Sb<sub>2</sub>Te<sub>3</sub>** SEM images of deposited Sb<sub>2</sub>Te<sub>3</sub> films are shown in Fig.6.24. All films are formed of continuous hexagonal crystals stacking on each other. Film thickness was found to be *ca.* 2.0  $\mu\text{m}$ . However, it is worth mentioning that the film thickness decreases along the substrates. At the far end of the substrate, film becomes much thinner.

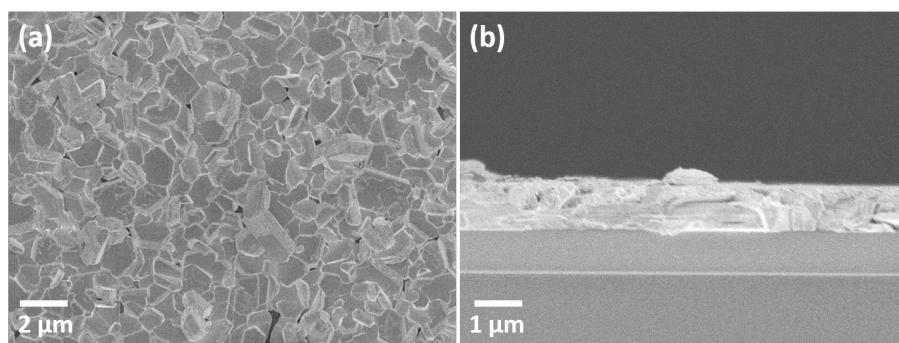


Figure 6.23: (a) Top view of  $\text{Bi}_2\text{Te}_3$  film; (b) Cross-sectional SEM of  $\text{Bi}_2\text{Te}_3$  film deposited on  $\text{SiO}_2$  substrate.

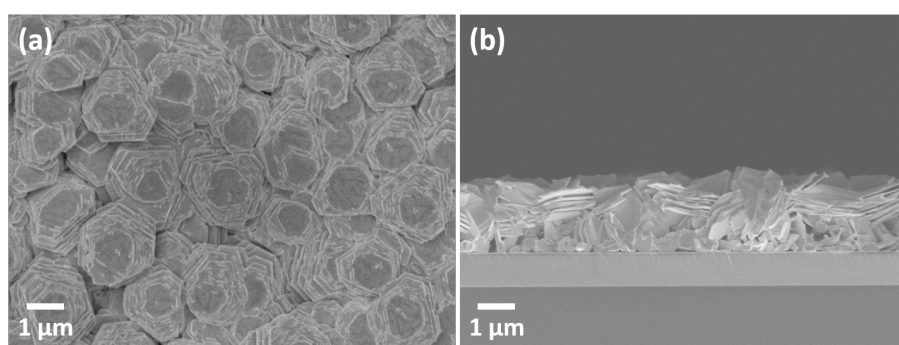


Figure 6.24: (a) Top view of  $\text{Sb}_2\text{Te}_3$  film; (b) Cross-sectional SEM of  $\text{Sb}_2\text{Te}_3$  film deposited on  $\text{SiO}_2$  substrate.

#### 6.4.2 Chemical composition and bonding

Chemical composition of the deposited thin films were investigated by EDX measurements. EDX spectroscopy on  $\text{Ga}_2\text{Se}_3$  films showed a Ga:Se ratio of 1:1.50 ( $\text{Ga}_2\text{Se}_3$ ), with negligible Cl or C content as shown in Fig. 6.25(a); EDX measurements of  $\text{Ga}_2\text{Te}_3$  films also show a 1:1.50 ratio of Ga:Te, with no observable Cl, O or C impurities (Fig. 6.25(b)); EDX measurements on  $\text{SnSe}_2$  were performed on the cross section of the film. The EDX spectrum is shown in Fig. 6.25(c) where Sn and Se are the dominant peaks. Only a small trace of C (2.67 %) and O (2.56 %) was detected which most likely were coming from the contamination on the cleaved surface. The Sn:Se ratio is 1:2 as confirmed by EDX quantification; For  $\text{TiSe}_2$  thin films, EDX measurements show that the Ti:Se ratio is 1:2 (29.2% Ti, 59.2% Se), and while there is no residual Cl impurity present, a small amount of carbon (7.0%) incorporation is observed (Si and O from the silica substrate account for the remaining 5%) as shown in Fig. 6.25(d); EDX spectroscopy of the  $\text{Bi}_2\text{Te}_3$  films gave a consistent Bi:Te ratio of 2:3 (40.31% Bi, 59.69% Te), measured quantitatively against a reference sample of  $\text{Bi}_2\text{Te}_3$  (99.99%, Strem Chemicals) as shown in Fig. 6.25(e); For  $\text{Sb}_2\text{Te}_3$ , the peaks for these elements overlap in the EDX spectrum, quantitative WDX

calibrated against elemental standards gives Sb:Te = 41.9:58.1, which is in close agreement with the expected value of 40:60. The only other significant peak in the EDX spectrum corresponds to carbon. No obvious impurities were observed Fig.6.25(f). All materials were confirmed to be stoichiometric with negligible impurities, indicating the high quality of the film deposited.

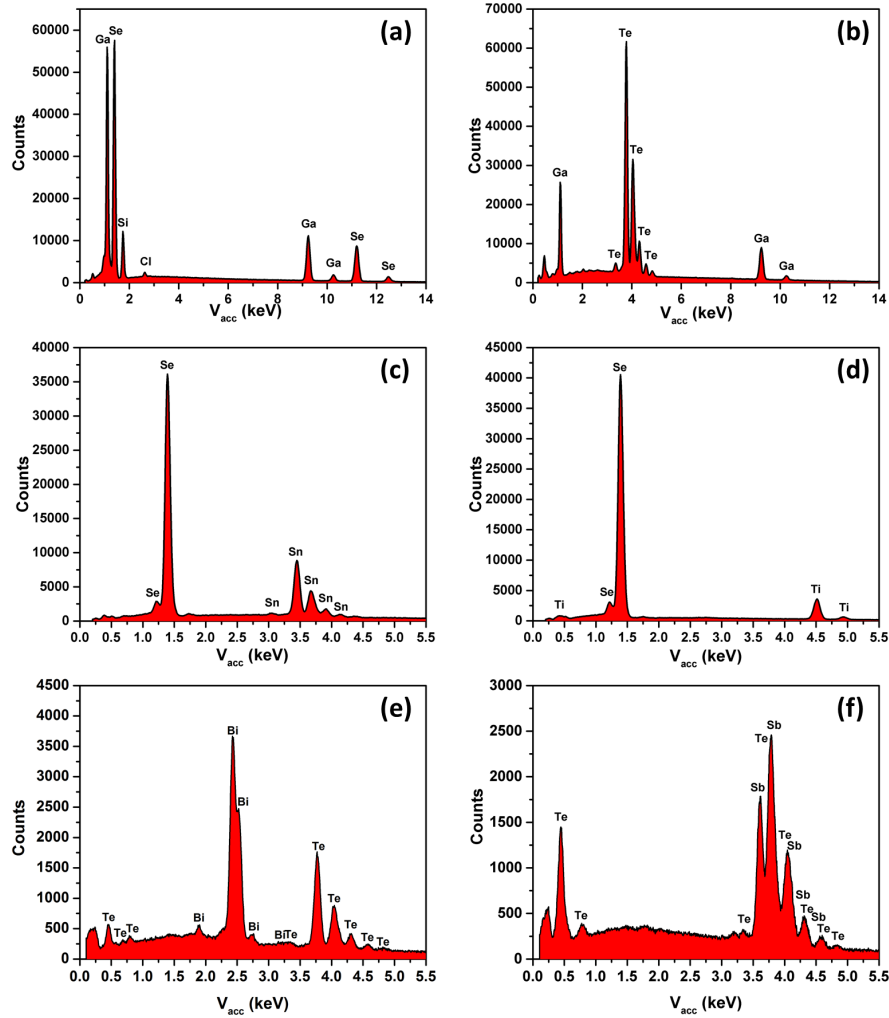


Figure 6.25: EDX spectra of typical  $Ga_2Se_3$  (a),  $Ga_2Te_3$  (b),  $SnSe_2$  (c),  $TiSe_2$  (d),  $Bi_2Te_3$  (e) and  $Sb_2Te_3$  (f) thin films grown via LPCVD.

Chemical bonding features for all materials were studied using Raman spectroscopy and are shown in Fig.6.26. Raman spectrum of  $Ga_2Se_3$  shows a sharp peak at  $155\text{ cm}^{-1}$  ( $A_1$  vibrational mode) and two broad peaks at  $260\text{ cm}^{-1}$  and  $293\text{ cm}^{-1}$  (Fig.6.26(a)), in accord with the literature data [206];  $Ga_2Te_3$  films deposited also displayed three peaks positioned at  $123\text{ cm}^{-1}$ ,  $157\text{ cm}^{-1}$  and  $226\text{ cm}^{-1}$  (Fig.6.26(b)), which are good matches with reported crystalline  $Ga_2Te_3$  data [207]; For  $SnSe_2$  films, one intense and sharp band was detected at  $182.4\text{ cm}^{-1}$  as shown in Fig.6.26(c) which is consistent with crystalline hexagonal  $SnSe_2$  [208]. This band is assigned to the  $A_{1g}$  Raman-active

mode;  $\text{TiSe}_2$  showed an intense peak at  $197\text{ cm}^{-1}$  and a weaker peak at  $138\text{ cm}^{-1}$  (Fig.6.26(d)) corresponding to Raman active  $A_{1g}$  and  $E_g$  symmetry phonons of the bulk hexagonal 1T- $\text{TiSe}_2$  respectively [209]; Raman measurements of  $\text{Bi}_2\text{Te}_3$  revealed three peaks positioned at  $105$ ,  $120$  and  $135\text{ cm}^{-1}$  which can be ascribed to the  $E_g$ ,  $A_{1u}$  and  $A_{2g}$  peaks reported in the reference [210] as shown in Fig.6.26(e); Raman measurements on  $\text{Sb}_2\text{Te}_3$  thin films reveal three main peaks positioned at  $120$ ,  $138$ , and  $165\text{ cm}^{-1}$ , respectively (Fig.6.26(f)). These are in good agreement with the  $E_{2g}$ ,  $A_{2u}$  and  $A_{1g}$  vibration modes of  $\text{Sb}_2\text{Te}_3$  previously reported [211]. With all the spectra recorded, no significant variation can be found in the peak position as well as peak width. Good matches with literature data were obtained for all materials. Raman spectrum on a single  $\text{Bi}_2\text{Te}_3$  nanocrystals (shown in Fig.6.27) was also found similar to that of the thin film  $\text{Bi}_2\text{Te}_3$  in Fig.6.26(e), suggesting the purity of nanocrystals deposited in this work.

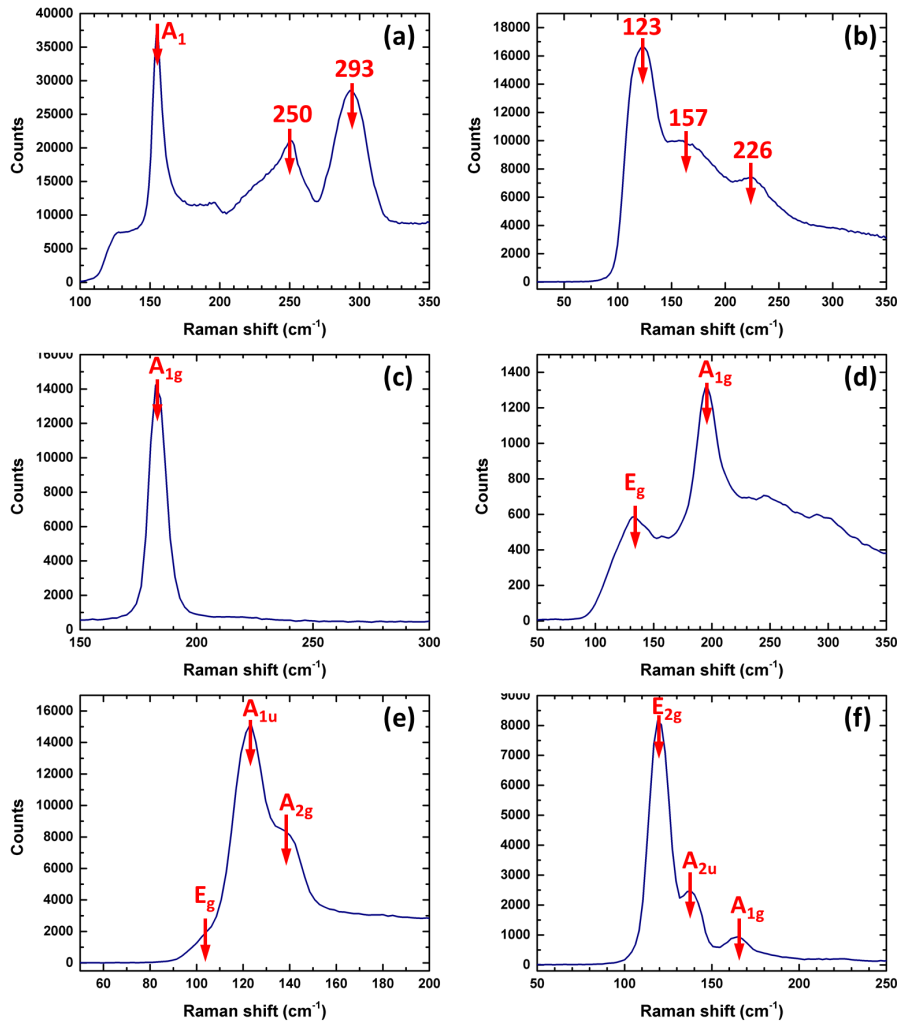


Figure 6.26: Raman spectra of typical  $\text{Ga}_2\text{Se}_3$  (a),  $\text{Ga}_2\text{Te}_3$  (b),  $\text{SnSe}_2$  (c),  $\text{TiSe}_2$  (d),  $\text{Bi}_2\text{Te}_3$  (e) and  $\text{Sb}_2\text{Te}_3$  (f) thin films grown via LPCVD.

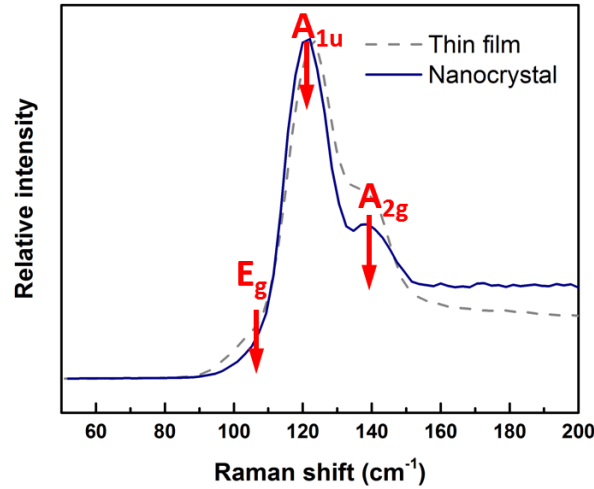


Figure 6.27: Raman spectra of  $\text{Bi}_2\text{Te}_3$  nanocrystal array within 200 nm holes (solid line) and  $\text{Bi}_2\text{Te}_3$  thin film (dashed line) grown via LPCVD. The broad features at high frequency are from the substrate.

#### 6.4.3 Crystal structure

X-ray diffraction patterns of  $\text{Ga}_2\text{Se}_3$  films matched with the monoclinic form (Cc) of  $\text{Ga}_2\text{Se}_3$  as shown in Fig. 6.28. Lattice parameters are not available in this case because of the overlapped peaks. XRD measurements of  $\text{Ga}_2\text{Te}_3$  also confirm the crystallinity of the deposited film, and the diffraction pattern (Fig. 6.29) is in accord with that of cubic  $\text{Ga}_2\text{Te}_3$  ( $F\bar{4}3m$ ); indexing and refining the peaks gives a lattice parameter,  $a = 5.8913$  Å (literature data from ICSD:  $a = 5.886(5)$ ,  $5.896(3)$  Å).

XRD measurements conducted on the  $\text{SnSe}_2$  deposited confirmed to be crystalline hexagonal  $\text{SnSe}_2$  in all cases with no evidence for other phases (such as  $\text{SnSe}$  and  $\text{SnO}_2$ ). Fig. 6.30 shows a typical XRD pattern for  $\text{SnSe}_2$  thick film deposited with 100 mg precursor (blue). The pattern matches with standard  $\text{SnSe}_2$  XRD files with lattice parameter to be  $a = 3.8101$  Å,  $c = 6.1347$  Å. No significant variation was observed in the lattice parameters of this phase with deposition temperature. However, for thin films ( $0.5$  μm to  $2$  μm), there was a strong evidence from the XRD pattern indicating a preferred orientation of the crystallites. With most of the crystallites lying flat on the surface as shown in Fig. 6.21(c), an intensification of 001, 002 and 003 peaks was observed as shown in Fig. 6.30(red) due to the strong alignment of the c-axis perpendicular to the substrate surface. The calculated average texture coefficients of 00 $l$  (001, 002 and 003) reflections is 2.8 which confirms the preferred orientation behaviour. For thick films, while the XRD pattern is closer to the standard, some preferred orientation can also be observed from the diffraction data based on  $hk0$  Fig. 6.21(a) indicates the growth direction of the crystallites mostly has the xy plane close to perpendicular to the surface. The average

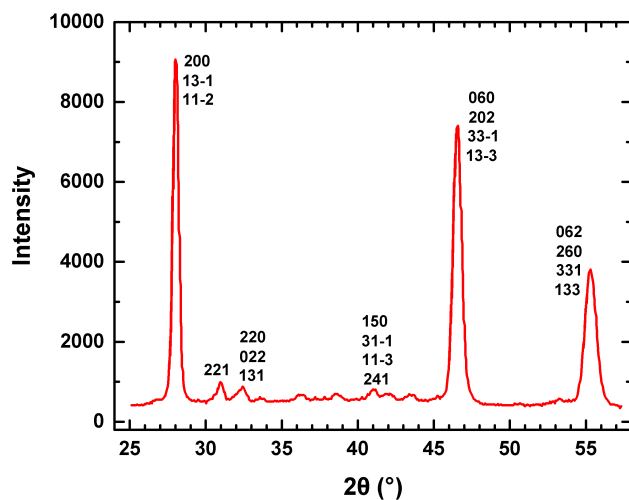


Figure 6.28: XRD pattern from a typical Ga<sub>2</sub>Se<sub>3</sub> thin film (monoclinic, Cc) grown via LPCVD. Pattern was collected in grazing incidence ( $\theta = 3^\circ$ ) with a Cu-K $\alpha$  radiation (1.54 Å). Peaks were indexed using JCPDS file 44-1012. Measurements were taken by Dr. Kathryn George.

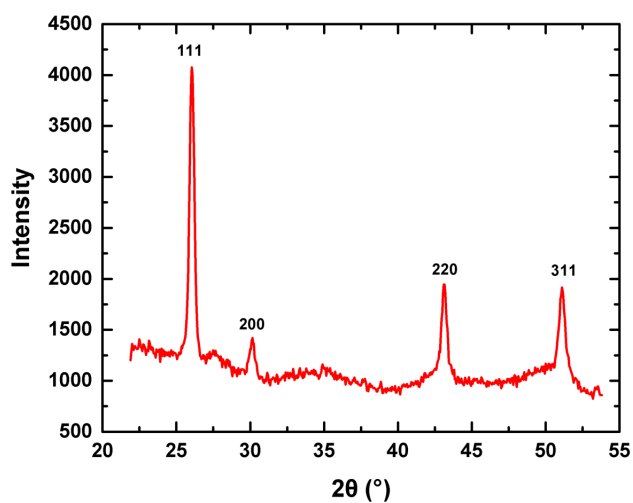


Figure 6.29: XRD pattern for Ga<sub>2</sub>Te<sub>3</sub> thin film grown via LPCVD, giving lattice parameters:  $a = 5.8913$  Å. Pattern was collected in grazing incidence ( $\theta = 3^\circ$ ) with a Cu-K $\alpha$  radiation (1.54 Å). Peaks were indexed using JCPDS file 35-1490.

texture coefficients for  $hk0$  (100, 110 and 200) reflections,  $C_{hk0}$ , is 1.6. This level of preferred orientation corresponds to a two-fold suppression of the peaks related to the  $c$ -axis.

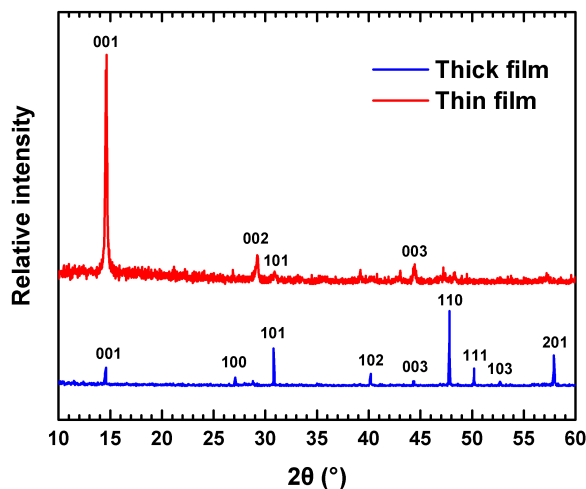


Figure 6.30: XRD of a thick film (blue) of  $\text{SnSe}_2$ , giving lattice parameters:  $a = 3.8101 \text{ \AA}$ ,  $c = 6.1347 \text{ \AA}$ ; and thin film (red) (the peaks labeled are consistent with  $a = 3.81 \text{ \AA}$  and  $c = 6.13 \text{ \AA}$ , although could not be refined reliably from the small number of diffraction peaks observed). Patterns were collected in grazing incidence ( $\theta = 3^\circ$ ) with a  $\text{Cu-K}\alpha$  radiation ( $1.54 \text{ \AA}$ ). Peaks were indexed using JCPDS file 01-089-3197.

$\text{TiSe}_2$  XRD measurements confirmed it as crystalline hexagonal  $\text{TiSe}_2$  in all cases, with strongly textured diffraction patterns as expected from the large, oriented crystallites observed in the SEM images. No other crystalline impurities were observed. Rietveld refinement of a pattern from a thick film collected in symmetric  $\theta$ - $2\theta$  geometry (Fig. 6.31) revealed lattice parameters of  $a = 3.53489$  and  $c = 6.0036 \text{ \AA}$ , close to those of bulk  $\text{TiSe}_2$  (space group  $P\bar{3}m1$ ,  $a = 3.540$  and  $c = 6.008 \text{ \AA}$ ) [212].

For  $\text{Bi}_2\text{Te}_3$ , XRD data were collected for films deposited onto  $\text{SiO}_2$  at  $500^\circ\text{C}$  and into  $40 - 100 \mu\text{m}$  TiN holes on a patterned substrate at  $450^\circ\text{C}$ . The XRD patterns identify trigonal ( $R\bar{3}m$ )  $\text{Bi}_2\text{Te}_3$  as the only phase present. The refined lattice parameters are in good agreement with literature data [213]. However, relative peak intensities differ significantly compared to literature values for bulk  $\text{Bi}_2\text{Te}_3$ , indicating strongly preferred  $c$ -axis orientation of the crystallites. The degree of preferred orientation varies between films deposited onto different substrates (Fig. 6.32), with the highest degree of orientation observed from microfocus XRD from individual filled wells in the micro-scale arrays. These XRD patterns display only  $00l$  reflections (Fig. 6.32(a)). The identification of this preferred orientation is consistent with its SEM image (see Fig. 6.13(c)) where all the crystals are lying flat within the TiN hole.

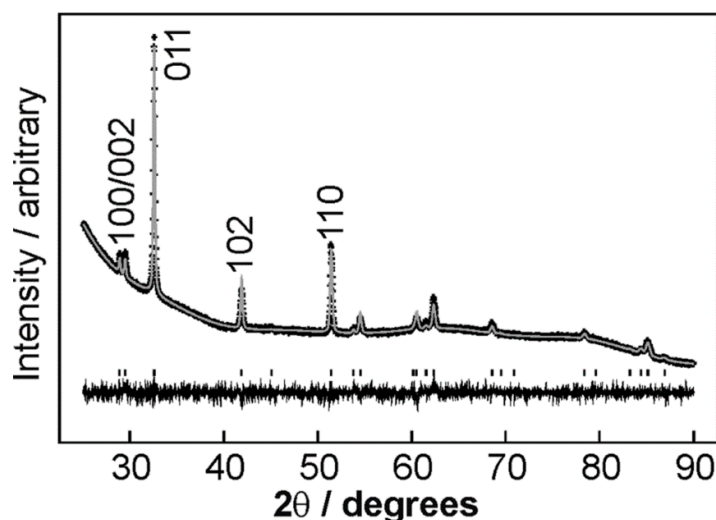


Figure 6.31: Fit to the XRD pattern for  $\text{TiSe}_2$  in  $P\bar{3}m1$  ( $R_{wp} = 1.7\%$ ,  $R_p = 1.2\%$ ). Crosses mark the data points, the upper continuous line the fit, and the lower continuous line the difference. Tick marks show the positions of allowed reflections, the first five of which are also labelled. The background shape is due to the substrate. Pattern was collected in symmetric  $\theta$ - $2\theta$  geometry with a  $\text{Cu-K}\alpha$  radiation ( $1.54 \text{ \AA}$ ). Peaks were indexed using JCPDS file 65-1885.

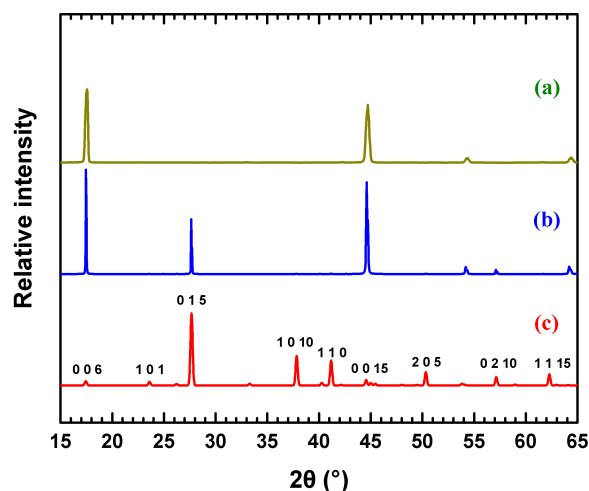


Figure 6.32: X-ray diffraction patterns from symmetric scans of  $\text{Bi}_2\text{Te}_3$  films deposited on various substrates. (a):  $\text{Bi}_2\text{Te}_3$  contained in a  $100 \mu\text{m}$  diameter hole on a  $\text{SiO}_2/\text{TiN}$  patterned substrate; (b): deposited onto a flat  $\text{SiO}_2$  substrate, giving lattice parameters:  $a = 4.378$  and  $c = 30.46 \text{ \AA}$ ; (c): indexed literature pattern generated by ICSD from reference [213]. Patterns were collected in grazing incidence ( $\theta = 3^\circ$ ) with a  $\text{Cu-K}\alpha$  radiation ( $1.54 \text{ \AA}$ ). Measurements were taken by Dr. Sophie L. Benjamin.

XRD patterns of  $\text{Sb}_2\text{Te}_3$  show the same phase ( $R\bar{3}m$ ) for all  $\text{Sb}_2\text{Te}_3$  thin films (Fig. 6.33). The refined lattice parameters,  $a = 4.24674$  and  $b = 30.1889$  Å are in good agreement with the literature data from JCPDS file ( $a = 4.25$  and  $b = 29.96$  Å). A summary of XRD results for all materials are presented in Table 6.3.

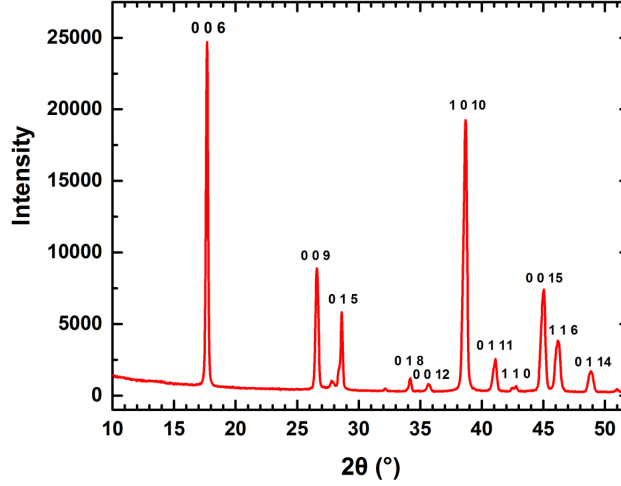


Figure 6.33: XRD pattern for  $\text{Sb}_2\text{Te}_3$  thin film grown via LPCVD, giving lattice parameters:  $a = 4.247$  and  $b = 30.20$  Å. Peaks were indexed using JCPDS file 72-1990. Patterns were collected in grazing incidence ( $\theta = 3^\circ$ ) with a  $\text{Cu-K}\alpha$  radiation (1.54 Å). Measurements were taken by Dr. Sophie L. Benjamin.

Table 6.3: Summary of the XRD measurement results for all thin film materials deposited by LPCVD in this work.

Materials	Lattice system	Space group	Lattice parameters (Å)		Reference Lattice parameters (Å)		
			a	c	a	b	Ref.
$\text{Ga}_2\text{Se}_3$	monoclinic	Cc	-	-	-	-	-
$\text{Ga}_2\text{Te}_3$	cubic	$F\bar{4}3m$	5.891	-	5.886(5)	-	[214]
$\text{SnSe}_2$	hexagonal	$P\bar{3}m1$	3.810	6.135	3.810	6.140	[214]
$\text{TiSe}_2$	hexagonal	$P\bar{3}m1$	3.535	6.004	3.540	6.008	[212]
$\text{Bi}_2\text{Te}_3$	trigonal	$R\bar{3}m$	4.378	30.46	4.383	30.41	[213]
$\text{Sb}_2\text{Te}_3$	hexagonal	$R\bar{3}mh$	4.247	30.20	4.250	29.96	[214]

#### 6.4.4 Electrical properties

Electrical properties of all deposited thin films were studied by Hall measurements. All experiments were performed under a magnetic field of 0.5 Tesla at room temperature using thin film samples deposited on  $\text{SiO}_2$  substrates. Fig. 6.34 is a typical I-V characteristic between contact 1 and 2 and contact 3 and 4 taken on one  $\text{Bi}_2\text{Te}_3$  film. The obtained linear relation between the current and voltage indicates good Ohmic contact between the material and the metal probes. The slightly different slopes of the two

curves suggest an asymmetric contact layout, which will be corrected in the calculation process to provide accurate results.

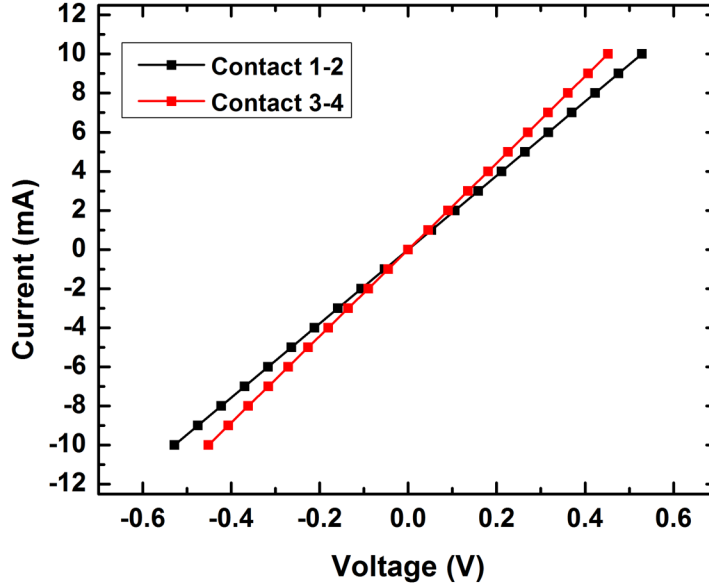


Figure 6.34: I-V characteristic of a  $\text{Bi}_2\text{Te}_3$  film taken in Hall measurement.

Hall measurements on  $\text{Ga}_2\text{Se}_3$  deposited in this work confirmed it to be a p-type semiconductor with a resistivity of  $(9 \pm 1) \times 10^3 \Omega\cdot\text{cm}$ . Carrier type is in agreement with bulk measurements literature [215, 216]. The carrier density and mobility were found to be  $2 \times 10^{13} \text{ cm}^{-3}$  and  $20 - 80 \text{ cm}^2/\text{V}\cdot\text{s}$ , respectively. It should be noted that thin film conductivity does sensitively depend on exact composition and microstructure and for phase change materials, also the number of crystallisation cycles. The effect of the arrangement of the vacancies in the crystal structure (see X-ray diffraction) might also play a role [217, 218]. Hence there is a large spread in thin film data in the literature. The non-uniformity of  $\text{Ga}_2\text{Se}_3$  film is also relevant, and hence our data for the  $\text{Ga}_2\text{Se}_3$  are indicative rather than authoritative.

$\text{Ga}_2\text{Te}_3$  was found to be a p-type semiconductor with a resistivity of  $195 \pm 10 \Omega\cdot\text{cm}$  and a carrier density of  $5 \times 10^{15} \text{ cm}^{-3}$ . Comparing with  $\text{Ga}_2\text{Se}_3$ , the resistivity of  $\text{Ga}_2\text{Te}_3$  is lower as expected from the difference in band-gap (approximated 2.0 eV for  $\text{Ga}_2\text{Se}_3$  and 1.1 eV for  $\text{Ga}_2\text{Te}_3$ ). The resistivity and carrier type are consistent with recent thermoelectric characterisation on bulk samples, suggesting a close to stoichiometric compound [219, 220]. The hole mobility of the film was found to be in a range of  $10 - 40 \text{ cm}^2/\text{V}\cdot\text{s}$ .

$\text{SnSe}_2$  was confirmed to be n type with a resistivity of  $210 \pm 10 \text{ m}\Omega\cdot\text{cm}$  with a mobility in a range of  $2 - 6 \text{ cm}^2/\text{V}\cdot\text{s}$ . This low level resistivity is consistent with the films being in

the crystalline state. The resistivities measured for our samples are *ca.* 10 times higher than those reported for other SnSe<sub>2</sub> films deposited via spin-coating and annealing or molecular beam epitaxy, 30 mΩ·cm [188] and 22 mΩ·cm [189] respectively, possibly reflecting the large grain boundary contribution and the different film morphology in the SnSe<sub>2</sub> deposits. The crystalline resistivity of SnSe<sub>2</sub> is much higher than that of Ge<sub>1</sub>Sb<sub>2</sub>Te<sub>4</sub> ( $\rho = 1.6 \text{ m}\Omega\cdot\text{cm}$ ) [221], which is favorable for applications since a high crystalline resistivity ensures a low reset current for low power consumption in PCRAM devices. The carrier density was measured as  $5.0 \times 10^{18} \text{ cm}^{-3}$ , which is in reasonable agreement with SnSe<sub>2</sub> films prepared by molecular beam epitaxy (MBE) [188].

The resistivity of the TiSe<sub>2</sub> films was found to be  $(3.36 \pm 0.05) \times 10^{-3} \Omega\cdot\text{cm}$ . Similar values have been reported in literature [222, 223], and this high conductivity is consistent with the very small bandgap for TiSe<sub>2</sub> of around 150 meV. This small bandgap results in a near intrinsic semiconductor with both electrons and holes contributing to the conductivity as described in Equation 3.13. The Hall coefficient is  $(9 \pm 2) \times 10^4 \text{ cm}^3/\text{C}$ , hence a minimum electron carrier density of  $1 \times 10^{22} \text{ cm}^{-3}$ . The sign of the Hall coefficient might indicate n-type conduction, but is more likely to reflect the higher electron than hole mobility.

For Bi<sub>2</sub>Te<sub>3</sub> films, the resistivity was measured as  $(5.65 \pm 0.02) \times 10^{-4} \Omega\cdot\text{cm}$ . The Bi<sub>2</sub>Te<sub>3</sub> was found to be a n-type with a carrier concentration of  $1.95 \times 10^{20} \text{ cm}^{-3}$ , and a mobility of  $56.6 \text{ cm}^2/\text{V}\cdot\text{s}$ . These data are comparable with values reported in the literature [213, 210]

Hall measurements show the deposited Sb<sub>2</sub>Te<sub>3</sub> to be p-type semiconductor with a charge carrier density of  $5 \times 10^{19} \text{ cm}^{-3}$ . A charge carrier mobility of  $138 \text{ cm}^2/\text{V}\cdot\text{s}$  was measured, yielding a electrical resistivity of  $(9.9 \pm 0.9) \times 10^{-4} \Omega\cdot\text{cm}$ . These results are comparable with Sb<sub>2</sub>Te<sub>3</sub> deposited from other techniques such as molecular beam epitaxy [213] and atomic layer deposition [224]. All the electrical measurement results are summarised in Table 6.4.

#### 6.4.5 Thermoelectric properties

Apart from the application in phase change memory, both Bi<sub>2</sub>Te<sub>3</sub> and Sb<sub>2</sub>Te<sub>3</sub> also enjoy excellent thermoelectric properties and are predicted to be the best candidates for thermoelectric devices at near room temperature [227]. Thermoelectric properties of these two materials deposited in this work were investigated by measuring their Seebeck coefficients (S). The mean Seebeck coefficient for Bi<sub>2</sub>Te<sub>3</sub> was measured to be  $-109 \mu\text{V}/\text{K}$ , consistent with films of n-type conductivity. The Seebeck coefficient of Sb<sub>2</sub>Te<sub>3</sub> was measured to be  $90 \mu\text{V}/\text{K}$ , consistent with films of p-type conductivity. The thermoelectric power factor ( $S^2\sigma$ ) can then be obtained from the Seebeck coefficient and film resistivity. The Bi<sub>2</sub>Te<sub>3</sub> films deposited in this work have a power factor value of  $21.14 \mu\text{W}/\text{cm}\cdot\text{K}^2$

Table 6.4: Summary of the Hall measurement results for all thin film materials deposited by LPCVD in this work compared with previous reports.

Materials (Band-gap) [225]	Reference	Type	Resistivity ( $\Omega \cdot \text{cm}$ )	Carrier density ( $\text{cm}^{-3}$ )	Mobility ( $\text{cm}^2/\text{V} \cdot \text{s}$ )
<b>Ga<sub>2</sub>Se<sub>3</sub></b> (2.0 eV)	<b>This work</b>	p	$(9 \pm 1) \times 10^3$	$2 \times 10^{13}$	20 - 80
	Ref. [215]	p	$1.2 \times 10^{11}$ (398K)	$2.0 \times 10^7$ (398K)	-
<b>Ga<sub>2</sub>Te<sub>3</sub></b> (1.1 eV)	<b>This work</b>	p	$(2.0 \pm 0.1) \times 10^2$	$5 \times 10^{15}$	10 - 40
	Ref. [207]	n	$\sim 1.0 \times 10^6$	$4 \times 10^{13}$	0.3
<b>SnSe<sub>2</sub></b> (0.97 eV)	<b>This work</b>	n	$(2.1 \pm 0.1) \times 10^{-1}$	$5 \times 10^{18}$	2 - 6
	Ref. [226]	n	$2.8 \times 10^{-1}$	$7.9 \times 10^{17}$	29.3
<b>TiSe<sub>2</sub></b> (0.15 eV)	<b>This work</b>	n	$(3.36 \pm 0.05) \times 10^{-3}$	$1 \times 10^{22}$	0.2
	Ref. [222]	p	$\sim 1.0 \times 10^{-3}$	$2 \times 10^{20}$	22
<b>Bi<sub>2</sub>Te<sub>3</sub></b> (0.16 eV)	<b>This work</b>	n	$(5.62 \pm 0.02) \times 10^{-4}$	$2 \times 10^{20}$	56.6
	Ref. [213]	n	$2.96 \times 10^{-3}$	$2.7 \times 10^{19}$	80
<b>Sb<sub>2</sub>Te<sub>3</sub></b> (0.28 eV)	<b>This work</b>	p	$(9.9 \pm 0.8) \times 10^{-4}$	$5 \times 10^{19}$	138
	Ref. [224]	p	$1.0 \times 10^{-4}$	$2.4 \times 10^{18}$	270

which is considerably higher than reported values [228, 229]. For Sb<sub>2</sub>Te<sub>3</sub>, the power factor value is  $8.19 \mu\text{W}/\text{cm} \cdot \text{K}^2$ , comparable with reported value [230]. These promising results are believed to be attributed to the nanostructured feature of the deposited films. It has been found recently that nanostructured materials can lead to a much enhanced efficiency over traditionally used bulk thermoelectrics [231]. A further improvement of these thermoelectric properties can hence be expected on the single nanocrystals of Bi<sub>2</sub>Te<sub>3</sub> and Sb<sub>2</sub>Te<sub>3</sub> from the highly selective growth.

## 6.5 An insight into selectivity

The depositions of above five chalcogenides showed varying degrees of selectivities. Both materials and substrate could contribute to this selective behaviour. To understand the effect of different substrates to the selective behaviour, deposition experiments were performed on three different substrates. Unpatterned Si, SiO<sub>2</sub> and TiN substrates were used for depositing SnSe<sub>2</sub> films under the same condition. While the observed morphology was essentially the same for each substrate type, the SEM data suggested denser film growth onto TiN and SiO<sub>2</sub> compared to Si. On this basis reagent-limited LPCVD experiments of SnSe<sub>2</sub> were further undertaken onto patterned SiO<sub>2</sub>/Si substrates to study the selective behaviour between Si and SiO<sub>2</sub> surfaces. SEM images of the resulting films (Fig. 6.35) show very clearly that a dense and flat-lying SnSe<sub>2</sub> film was deposited on SiO<sub>2</sub> while nothing was on Si area which clearly showing the SnSe<sub>2</sub> film growth onto the SiO<sub>2</sub> is preferred, resulting in very high selectivity. This result, combined with the selectivity over TiN surface on the SiO<sub>2</sub>/TiN patterned substrates shown in previous section, indicate a preferred trend of deposition, first on TiN surface, then on SiO<sub>2</sub> surface and finally, on Si surface.

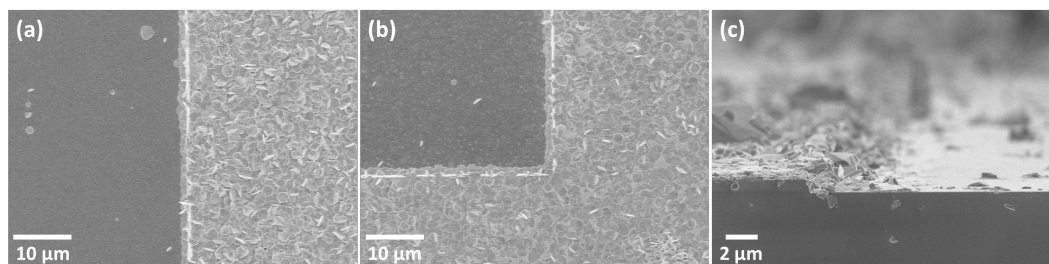


Figure 6.35: SEM images showing selective growth of  $\text{SnSe}_2$  onto the  $\text{SiO}_2$  on a patterned  $\text{SiO}_2/\text{Si}$  substrate. (a) Si (left) and  $\text{SiO}_2$  (right), (b) Si (inner) and  $\text{SiO}_2$  (outer), (c) cross section view with Si (right) and  $\text{SiO}_2$  (left).

The potential reason behind this selective deposition behaviour was studied by the roughness as well as hydrophily on different surfaces. The roughness measurements were conducted by AFM scanning on Si,  $\text{SiO}_2$  and TiN surfaces, all measurements demonstrated very smooth films (Si-0.87 nm,  $\text{SiO}_2$ -0.65 nm and TiN-1.5 nm) indicating the surface roughness of the different types of substrate are essentially invariant and not affecting this selective deposition behaviour. The hydrophily was studied by measuring the contact angles of a water droplet on different surfaces. The measured contact angles for Si,  $\text{SiO}_2$  and TiN were  $28.5^\circ$ ,  $57.6^\circ$  and  $73.6^\circ$ , respectively, as shown in Fig. 6.36 which shows a strong correlation with the selectivity observed. This suggests the deposition has a greater tendency to happen on the surface which is more hydrophobic. The possible explanation for this tendency could be explained by the hydrophobic nature of the n-butyl tail groups in the precursor complexes, leading to a higher affinity for adsorption of the precursor onto the most hydrophobic surface (i.e. TiN rather than  $\text{SiO}_2$  for the  $\text{SiO}_2/\text{TiN}$  patterned substrates and  $\text{SiO}_2$  rather than Si on the  $\text{SiO}_2/\text{Si}$  patterned substrates). Cao and co-workers have very recently demonstrated a strong mediation effect of substrates for growth of layered chalcogenide materials signifying dynamics of growth reaction which leads to facile migration of metal chalcogenide adatoms onto substrates [232].

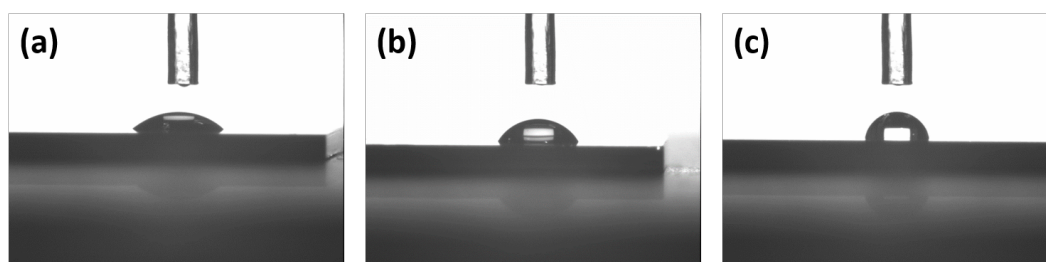


Figure 6.36: Contact angle measurements on (a) Si surface, (b)  $\text{SiO}_2$  surface and (c) TiN surface. The resulting angles were  $28.5^\circ$ ,  $57.6^\circ$  and  $73.6^\circ$ , respectively.

Apart from the surface effects onto the selectivity, the deposited materials themselves also demonstrate a tendency of selective deposition in correlation with their band-gaps

and conductivities as shown in Fig.6.37. Better selectivity was obtained on narrow bandgap materials with high conductivities (i.e.  $\text{Sb}_2\text{Te}_3$ ,  $\text{Bi}_2\text{Te}_3$ ,  $\text{TiSe}_2$  and  $\text{SnSe}_2$ ). For wide band-gap chalcogenides (i.e.  $\text{Ga}_2\text{Te}_3$  and  $\text{Ga}_2\text{Se}_3$ ), little or no selectivity was observed. The mechanism behind this correlation requires further investigation.

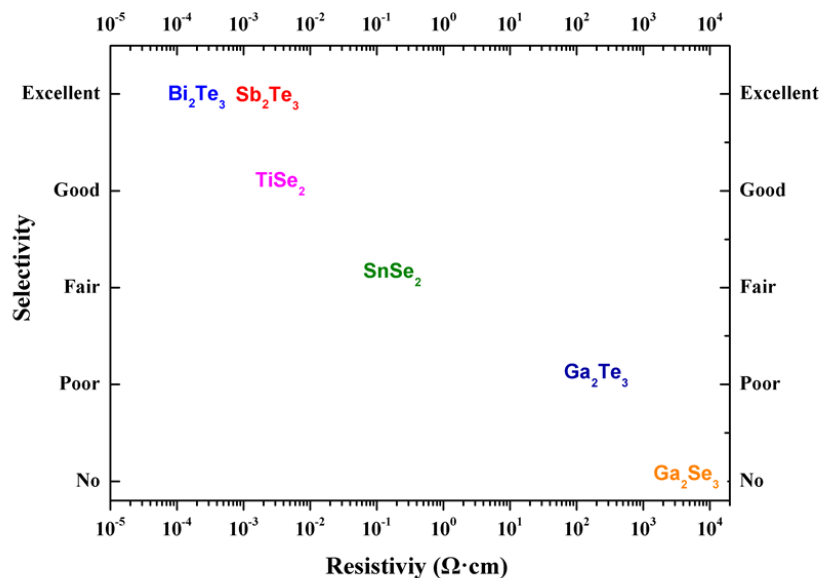


Figure 6.37: Selectivity of single precursor chemical vapour deposited chalcogenides as a function of material resistivity.

## 6.6 Summary

This chapter demonstrates the selective chemical vapour deposition behaviour of six chalcogenides films,  $\text{Ga}_2\text{Se}_3$ ,  $\text{Ga}_2\text{Te}_3$ ,  $\text{SnSe}_2$ ,  $\text{TiSe}_2$ ,  $\text{Bi}_2\text{Te}_3$  and  $\text{Sb}_2\text{Te}_3$  using single source precursors. Different levels of selective depositions behaviour were observed over lithographically patterned  $\text{SiO}_2/\text{TiN}$  substrates. Preference was found to be for TiN in all cases except for  $\text{Ga}_2\text{Se}_3$  where no selectivity was observed. Materials with lower resistivity were found to have better selective behaviour. The most conductive  $\text{Bi}_2\text{Te}_3$  enjoys the best selectivity into nano-patterned structures. Substrate surface also plays an vital role in the selectivity. Deposition of  $\text{SnSe}_2$  was preferred onto  $\text{SiO}_2$  for  $\text{SiO}_2/\text{Si}$  substrate and onto TiN for  $\text{SiO}_2/\text{TiN}$  substrate. Hydrophilic properties of the surface was suggested to be an additional mechanism which lies behind this selectivity.

All the films were confirmed to be single phase and crystalline with little or no impurities by EDX, XRD and Raman measurements. The electrical properties were characterized using Hall measurements where the conductivities obtained were in a good agreement with the band-gap of each material.

# Chapter 7

## Summary

The principal aim pursued within this work has been the application of phase change materials for emerging electrical data storage and information processing applications. To meet the requirement for the next generation data storage technology, a better understanding of phase change properties in nanoscale is essential for the future development of phase change memory device. In addition, phase change memory demands the exploration of optimised device structure which enables thermally stable, ultra-low power, high speed, non-volatile high density data storage and processing. To this end, this research follows both routes in investigating the nanoscale phase change properties and depositing phase change materials and memories by novel approaches.

### Properties of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ nanowires and contact resistance

The novel e-beam free, top-down spacer etch process has been successfully used in fabrication sub-hundred  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  nanowires. The advantages of this method in nanowire dimension and location control enabled the separation of contact resistance from the total resistance of the nanowire device fabricated. The specific contact resistance between GST and TiN electrode was found to be  $7.56 \times 10^{-5} \Omega\cdot\text{cm}^2$  in the crystalline state and  $6.39 \times 10^{-2} \Omega\cdot\text{cm}^2$  in the amorphous state under an applied voltage of 2 V. This contact resistance can contribute to more than 90% of total resistance when the material thickness is below 1  $\mu\text{m}$ . In addition, a Schottky barrier of  $\sim 0.6$  eV between the interface of GST and TiN electrode was found to be the main contributing factor to the total resistance of the devices. This work suggested that the contact resistance plays a dominant role in the total resistance of GST memory device in both crystalline and amorphous states. Interface engineering can play a vital role for the future development of PCRAM.

## Electrodeposition of GeSbTe phase change memory

GeSbTe phase change material was deposited by non-aqueous electrodeposition. High purity thin films were obtained with good uniformity and smooth surface. EDX and Ramans measurements confirmed the composition of deposited film. XRD data shows a phase change behaviour of the as-deposited film from amorphous to crystalline at a temperature  $\sim 150^\circ\text{C}$ , which is a good match with sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ . Electrodeposition into nano-patterned holes shows good uniformity with a homogeneous GeSbTe bump obtained in each hole. The material composition was confirmed by EDX, XRD and Raman measurements. Selective deposition into hole size of around 50 nm was presented with a great potential to go even further down to sub-20 nm. The issue of hole over-filling was discussed with potential solutions suggested. Electrical measurements on the GeSbTe memory device display a promising switching behaviour of 200 cycles with 3 orders of magnitude resistance change, which is comparable to the sputtered  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  fabricated in this work. Similar switching behaviour was observed in micro-patterned, and, more importantly, nano-patterned devices. With the high quality of material deposited and the ability of filling nano-scale holes, electrodeposition demonstrated in this work can be considered to be a novel promising deposition techniques in the application of PCRAM.

The next step for this work is to further scale down the hole size to sub-20 nm to meet the requirement of the coming 14 nm technology node. New substrate fabrication recipe will be developed to produce features of such small scale. This also demands more precise control during the electrodeposition process to ensure good deposition while minimizing the over-filling. Phase change memory devices will then be fabricated based on these confined nanoscale materials. The electrical switching behaviour will be extensively studied. Essential parameters like the reset current, operating power, endurance and data retention will be investigated together with the scaling factor.

## Selective chemical vapour deposition of chalcogenide phase change materials

This work demonstrates the selective chemical vapour deposition behaviours of six chalcogenides films,  $\text{Ga}_2\text{Se}_3$ ,  $\text{Ga}_2\text{Te}_3$ ,  $\text{SnSe}_2$ ,  $\text{TiSe}_2$ ,  $\text{Bi}_2\text{Te}_3$  and  $\text{Sb}_2\text{Te}_3$  using single source precursors. All materials, except  $\text{Ga}_2\text{Se}_3$ , have demonstrated to some extent selectivity onto the TiN surface in the lithographically patterned  $\text{SiO}_2/\text{TiN}$  substrates with  $\text{Bi}_2\text{Te}_3$  and  $\text{Sb}_2\text{Te}_3$  exhibiting the best selectivity onto nano-patterned structures. A correlation between material resistivity and the scale of selectivity was observed. In addition, the influence of surface to the selective deposition behaviour has also been investigated by using different surface materials in the patterned substrate. Deposition

of SnSe<sub>2</sub> was preferred onto SiO<sub>2</sub> for SiO<sub>2</sub>/Si substrate and onto TiN for SiO<sub>2</sub>/TiN substrate. Hydrophilic properties of the surface was suggested to be the mechanism behind this selectivity. All the films were confirmed to be single phase and crystalline with little or no impurities as evidenced by EDX, XRD and Raman measurements. The electrical properties were characterized using Hall measurements where the conductivities obtained were in a good agreement with the band-gap of each material.

The selective chemical vapour deposition platform built up in this work allows synthesising high quality single nanocrystals while controlling their positions precisely. Taking advantage of this, characterisation of individual single nanocrystals is possible. The compositional, morphological, crystalline and electrical properties can all be investigated on different crystal dimensions to better understand the influence of scaling on material properties. Fabrication of phase change memory devices based on these nanocrystals are possible with great potentials of demonstrating good switching behaviours, and shedding new lights on the understanding the threshold mechanism for phase change materials.



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