UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Electronics and Computer Science

Radiation Effects and Reliability of Dielectrics in CMOS Transistors and Resistive Memories

by

Katrina Anne Morgan

Thesis for the degree of Doctor of Philosophy

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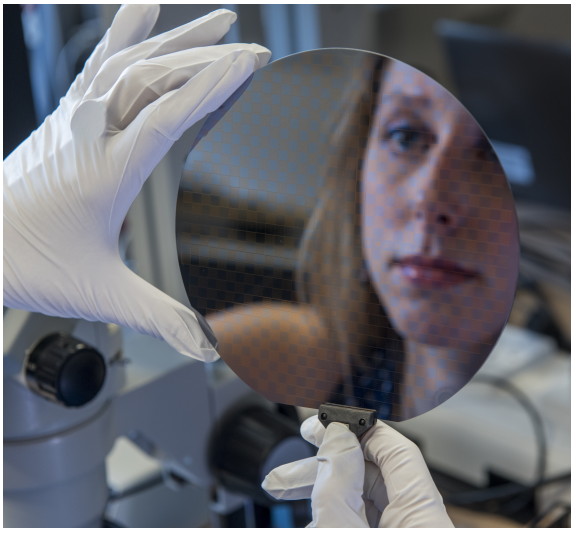

"All brontosauruses are thin at one end, much, much thicker in the middle, and then thin again at the far end. That is my theory, it is mine and belongs to me, and I own it, and what it is too." - John Cleese, Monty Python's Flying Circus, Episode 31, 1972

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ABSTRACT

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RADIATION EFFECTS AND RELIABILITY OF DIELECTRICS IN CMOS TRANSISTORS AND RESISTIVE MEMORIES

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Many industries heavily rely upon advances in electronic devices. As development of electronics continues, new structures and new materials are being utilised. The reliability of these new technologies therefore need to meet the same high levels as the traditional technologies that they are replacing.

Industries such as space and nuclear in particular, face an additional challenge affecting the reliability of their electrical devices; radiation. Ionizing radiation in particular can damage dielectric layers in devices such as metal-oxide-semiconductor (MOS) transistors and resistive memories. In either case, controlling the radiation effects of dielectrics is essential for the reliability of these devices.

High-k MOS capacitors have been fabricated, analysed and irradiated and compared to a reference silicon dioxide MOS capacitor. Hafnium oxide and aluminium oxide were used for the dielectric layer, with Al and TiN used for the top electrode. C-V measurements indicated the high quality of the TiN/HfO_2/Si structure in particular, with an interfacial equivalent oxide thickness (EOT) of less than half the total EOT of 1.9 nm. The TiN/HfO_2/Si capacitor showed superior capacitance and leakage current properties when compared to silicon dioxide capacitors verifying the successful fabrication of high quality, high-k MOS capacitors. The ionizng radiation results showed a voltage shift of less than 100 mV up to 3 Mrad(Si) for the TiN/HfO_2/Si capacitors. These radiation hardness levels are in the same order of magnitude as silicon dioxide structures. High-k dielectrics can therefore be used as a replacement for silicon dioxide gate oxides without decreasing the radiation hardness of the device, whilst simultaneously achieving reduced leakage current.

Two types of TiN/HfO_x/TiN resistive memory cells have been fabricated where the top 200 nm TiN electrode has been deposited by two different sputtering methods; reactive, using a titanium target in a nitrogen environment, and non-reactive, using a titanium nitride target. Characterization of the materials shows that the reactive TiN is single-phase stoichiometric TiN with a sheet resistance of 7 Ω/square. The non-reactive TiN

has a sheet resistance of 300 Ω/square and was found to contain significant amounts of oxygen. The resistive switching behavior differs for both memory cells. The reactive stoichiometric TiN device results in bipolar switching with a R_{OFF}/R_{ON} ratio of 50. The non-reactive TiN results in unipolar switching with a R_{OFF}/R_{ON} ratio of more than 10^3. These results show that an oxygen rich layer between the top electrode and insulator affects the R_{OFF} value. It supports the theory of oxygen vacancies leading to the formation of conductive filaments.

Resistive random access memory based on TiN/HfO_x/TiN has been fabricated, with the stoichiometry of the HfO_x layer altered through control of atomic layer deposition (ALD) temperature. Sweep and pulsed electrical characteristics were extracted before and after ^{60}Co gamma irradiation. Monoclinic HfO_x deposited at 400 °C did not result in resistive switching. Deposition at 300 °C and 350 °C resulted in cubic HfO_x which switched successfully. Both stoichiometric HfO_2 and sub-oxides HfO_{2-x} result in similar memory characteristics. All memory cells are shown to be radiation hard up to 10 Mrad(Si), independent of stoichiometry.

Amorphous silicon carbide Cu/a-SiC/Au resistive memory cells are measured using the pulsed voltage technique and exhibit the highest R_{OFF}/R_{ON} ratio recorded for any resistive memory. The switching kinetics are investigated and fitted to a numerical model, using thermal conductivity and resistivity properties of the dielectric. The SET mechanism of the Cu/a-SiC/Au memory cells is found to be due to ionic motion without thermal contributions, whereas the RESET mechanism is found to be due to thermally assisted ionic motion. The conductive filament diameter is extracted to be $\Phi \sim 4$ nm. The high thermal conductivity and resistivity for the Cu/a-SiC/Au memory cells result in slow switching but with high thermal reliability and stability, showing potential for use in harsh environments. Radiation properties of SiC memory cells were investigated. No change was seen in DC sweep or pulsed switching nor in conductive mechanisms, up to 2 Mrad(Si) using ^{60}Co gamma irradiation.

High-k metal gate MOS capacitors, valence change memory (VCM) and electrochemical metallization memory (ECM) cells have all shown high tolerance to ionizing radiation with negligible change seen in device parameters. This indicates that the radiation sensitive region within a memory circuit is the select device used to address the memory cell, such as transistors, and not the memory cell itself. In particular, within transistors, the gate oxide is essentially radiation hard, even when using high-k dielectrics, due to the thin layer. Therefore the areas within a circuit that are susceptible to ionizing radiation damage remain to be the buried oxides and isolation oxides.

Declaration of Authorship

I, Katrina Anne Morgan , declare that the thesis entitled *Radiation Effects and Reliability of Dielectrics in CMOS Transistors and Resistive Memories* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
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List of Publications

Journal Publications

K. Morgan, R.Huang, K. Potter, C. Shaw, W. Redman-White, C. H. de Groot (2014) **Total Dose Hardness of TiN/HfO$_x$/TiN Resistive Random Access Memory,** *IEEE Transactions on Nuclear Science,* 61(6), 2991-2996.

K. Morgan, J. Fan, R.Huang, L. Zhong, R. Gowers, L. Jiang, C. H. de Groot (2015) **Switching Kinetics of SiC Resistive Memory for Harsh Environments,** *Applied Physics Letters,* (Submitted).

K. Potter, **K. Morgan**, C. Shaw, P. Ashburn, W. Redman-White, C. H. de Groot (2014) **Total Ionizing Dose Response of Fluorine implanted Silicon-On-Insulator Buried Oxide,** *Microelectronics Reliability,* 54, 2339-2343.

C. Shaw, K. Potter, **K. Morgan**, E. Chatzikyriakou, P. Ashburn, W. Redman-White, C. H. de Groot (2014) **Total Dose Radiation Hardening of MOS Transistors by Fluorine Implantation,** *IEEE Transactions of Nuclear Science,* (To be submitted).

Conference Publications

K. Morgan, R.Huang, K. Potter, C. Shaw, W. Redman-White, C. H. de Groot (2014) **Total Dose Hardness of TiN/HfO$_x$/TiN Resistive Random Access Memory Devices,** *Nuclear and Space Radiation Effects Conference (NSREC),* Paris, France.

K. Morgan, R.Huang, S. Pearce, C. H. de Groot (2014) **The Effect of Atomic Layer Deposition Temperature on Switching Properties of HfO$_x$ Resistive RAM Devices,** *IEEE International Symposium on Circuits and Systems (ISCAS),* Melbourne, Australia, 432-435.

K. Morgan, R.Huang, S. Pearce, L. Zhong, L. Jiang, C. H. de Groot (2014) **Effect of Stoichiometry of TiN Electrode on the Switching Behavior of TiN/HfO$_x$/TiN Structures for Resistive RAM** *Materials Research Society (MRS)* Boston, USA.

Technical Reports

K. Morgan, (2013) **Radiation Hardness of High-k Dielectrics,** *AWE,* Aldermaston, Hampshire, UK.

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List of Acronyms

ALD atomic layer deposition
APC automatic pressure control
BEOL back-end-of-line
BOX buried oxide
CBRAM conductive bridging random access memory
CF conductive filament
CMOS complementary metal oxide semiconductor
CPU central processing unit
DOE design of experiment
DRAM dynamic random access memory
ECM electrochemical metallization
EDX electron-dispersive X-ray dispersive Spectroscopy
EHP electron hole pair
EOT equivalent oxide thickness
EPR electron paramagnetic resonance
FEGSEM field emission scanning electron microscope
FeRAM ferroelectric memory
GADDs general area detector diffraction system
HfAA hafnium alkylamides
HKMG high k metal gate
HRS high resistance state
ICP inductively coupled plasma
ITRS international roadmap for semiconductors
LRS low resistance state
MOS metal oxide semiconductor
MOSFET metal oxide semiconductor field effect transistor
MRAM magnetic random access memory
MSE mean squared error
nMOS n type MOS
NVM non volatile memory
NOV neutral oxygen vacancy
OIPT Oxford instruments plasma technology
PCM programmable metallization cell
PCRAM phase change random access memory
pMOS p type MOS
RAM random access memory
RF radio frequency
RIE reactive ion etcher
RRAM resistive random access memory

SCM storage class memory
SEM scanning electron microscope
SiC silicon carbide
SiMOX separation by implantation of oxygen
SOI silicon on insulator
SRAM static random access memory
STI shallow trench isolation
TEMAH tetrakis(ehtlmethlyamino)hafnium
TID total ionizing dose
TMAl triemthylaluminium
VCM valence change memory
XPS x-ray photoelectron spectroscopy
XRD x-ray diffraction

Contents

Chapter 1

Introduction

1.1 CMOS Logic and Memory

Complementary Metal-Oxide-Semiconductor (CMOS) technology consists of using an array of alternating p-type and n-type Metal-Oxide-Semiconductor (MOS) transistors in the same substrate enabling construction of integrated circuits including microprocessors, power devices and semiconductor memories. MOS field effect transistors (MOSFETs) are the most common transistor found in both digital and analogue circuits today [1]. The basic principle of a MOSFET was introduced by J.E. Lilienfeld in 1930 [2] and five years later O. Heil came up with the idea of using an electric field to alter the resistance in a semiconducting material [3]. W.B. Schockley and G. Pearson did further studies in the 1940's [4] but it wasn't until the 1960's when the idea became practically possible when D. Kahng and M.M. Atalla fabricated the first MOSFET [5].

Since the first MOSFET was fabricated the size of the device has become increasingly smaller. In 1959 the integrated chip (IC) era began and since then the number of components per IC chip has been increasing exponentially [1]. G. Moore made a prediction that the number of transistors per chip will double approximately every two years as shown in Figure 1.1.

As the transistor count increases, the size of the transistors must decrease which has resulted in rapid scaling into deep sub micron regimes. Following Moore's Law, an International Technology Roadmap for Semiconductors (ITRS) has been created to predict the size of components in the future. For MOSFETs, the roadmap predictions, produced in 2007, are shown in Table 1.1 which shows a dramatic decrease in physical gate length. This physical gate length is the property of a MOSFET that is the vital parameter and the current size has only become possible with new fabrication techniques.

With the scaling of CMOS, the packing density needs to be high whilst keeping the individual MOSFETs electrically isolated. However the source and drain implants have

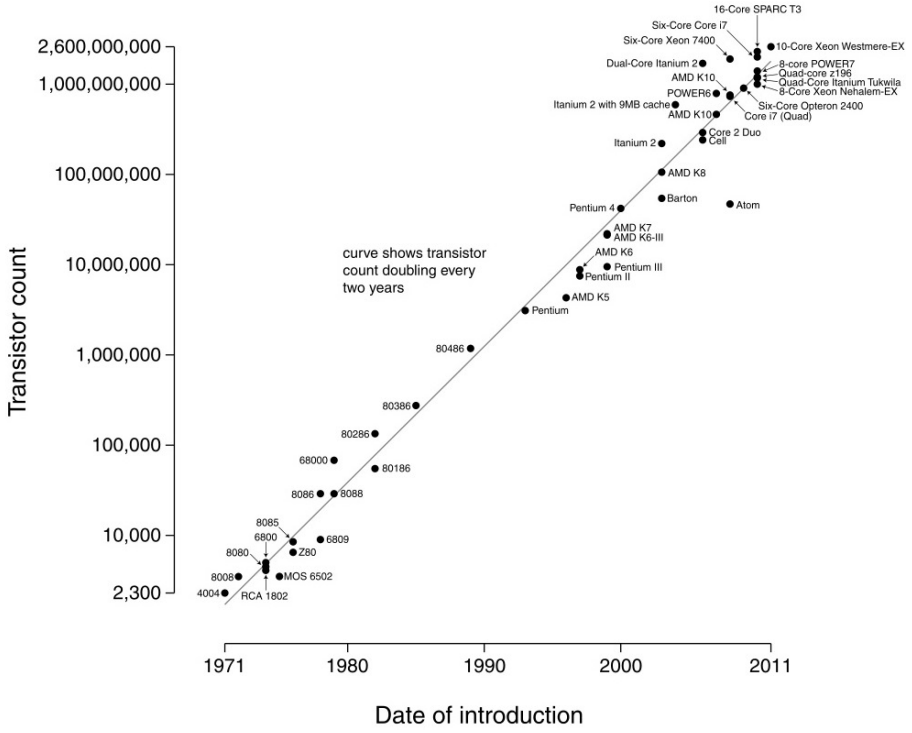


Figure 1.1: Microprocessor Transistor Counts from 1971 to 2011 and G. Moore's Prediction of increasing number of transistors per chip [6]

Year	**2003**	**2004**	**2005**	**2006**	**2007**	**2008**	**2009**
Physical Gate Length(nm)	45	37	32	28	25	22	20
Year	**2010**	**2012**	**2014**	**2016**	**2018**	**2020**	**2022**
Physical Gate Length(nm)	18	14	11	9	7	5.6	4.5

Table 1.1: ITRS Roadmap for Semiconductors 2007 Edition: Prediction of Physical Gate Length of MOSFETs [7].

to be isolated from one another. This is done through the use of a field oxide which can be seen in Figure 1.2(a), labelled as the STI. Here the field oxide is separating the highly doped n^+ drain region of an nMOSFET from the highly doped p^+ source region of a pMOSFET. This oxide is named after the technique used to isolate the two implant areas which is called *Shallow Trench Isolation* or STI.

The use of bulk wafers for CMOS transistors, as shown in Figure 1.2(a), was a traditional method. For these, the bulk or substrate was made from one piece of semiconductor. However it was later realised that when the carriers are transported in the semiconducting material of a MOSFET, they only occupy the top 0.1-0.2 μm. Over 99.9 percent of the semiconductor is used solely as a stable handle for the rest of the active device. This large area of inactive semiconducting material can give way to unwanted effects such as leakage currents [8].

The need for high performance and low power consumption was strong and it seemed a

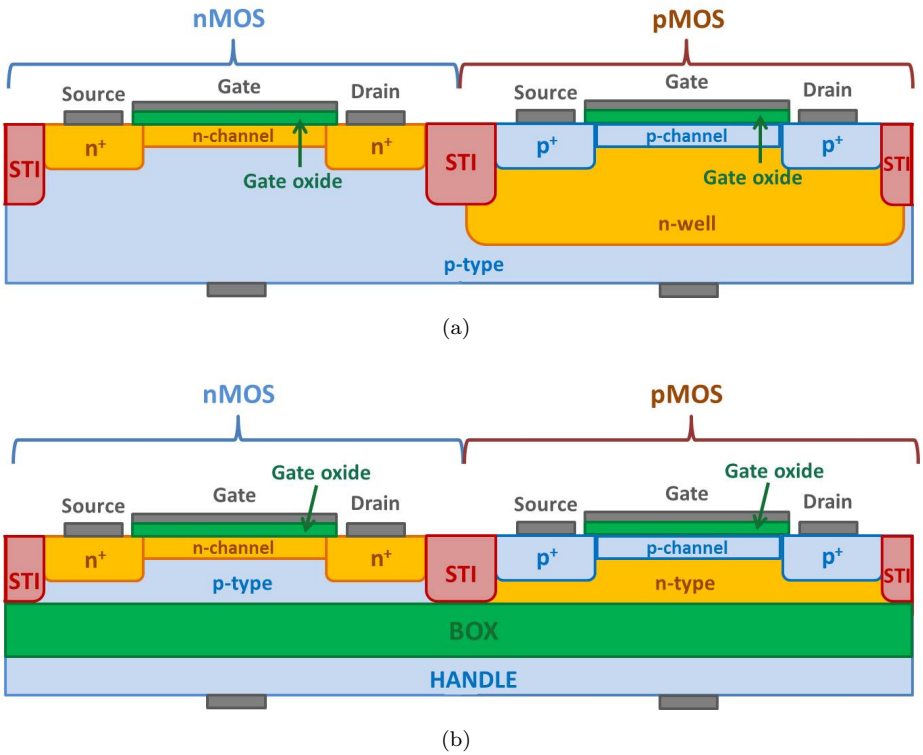


Figure 1.2: Schematic Diagram of (a) bulk MOS technology with shallow trench isolation and (b) silicon-on-insulator technology.

new technology offered a solution [9]. In the 1990's, oxide properties improved, resulting in Silicon-on-Insulator (SOI). Figure 1.2(b) shows this has the same design as the bulk CMOS but with one exception; an additional layer of insulating material. This insulating material, an oxide known as the Buried Oxide or BOX, is located in the centre of the substrate which splits this large area of semiconducting material into two. The top layer of semiconductor is still used as the active part of the device, known as the body, whereas the bottom layer which is electrically isolated from the rest of the device, is used for mechanical stability only. This is known as silicon-on-insulator (SOI) and is shown in Figure 1.2(b) where the oxide layer and substrate handle are clearly labelled, with nMOS device on the left hand side and a pMOS device on the right hand side.

As predicted by the International Technology Roadmap for Semiconductors, the sizes of these components are dramatically decreasing and as a result of this scaling, one of the dimensions that has reached its operating limit, is the gate oxide thickness. To overcome this physical limit, high-k dielectrics are being utilized as a silicon dioxide replacement. The high-k allows thicker physical layers of oxides to be used, overcoming the scaling limitation, allowing the MOS transistor to be brought back in line with the ITRS roadmap predictions.

As CMOS industry moves away from silicon dioxide towards high-k dielectrics, another structural change is needed. This change is the top electrode, or gate contact, material.

High-k materials must be used in conjunction with metal gates, rather than the previous poly-silicon contacts. Poly-Si cannot be used as a gate material in combination with these high-k dielectrics, due to the resulting high threshold voltages and poor channel mobilities; therefore metal gates are used. From this, it can be seen that the structure of a high-k metal gate (HKMG) is needed to ensure high capacitive, low leakage MOS transistors.

Transistors are used throughout computer architecture today, for both logic and memory. A computer can be split into two main units; a central processing unit (CPU) and memory. The CPU performs logic, arithmetic and control operations and the memory stores the instructions and data for the CPU. Traditionally a CPU is made up of thousands of transistors on one chip (microprocessor) and the memory is made up of traditional memory hierarchy, as depicted in Figure 1.3(a).

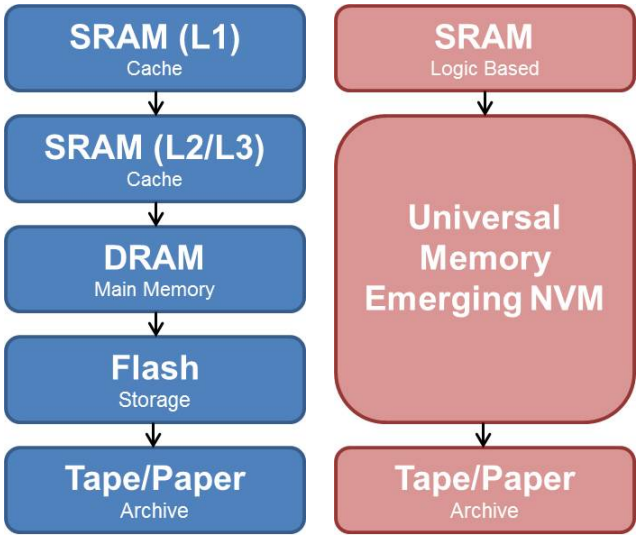


Figure 1.3: (a) Traditional memory hierarchy (b) Universal memory hierarchy, adapted from [10].

Traditional memory consists of two types of volatile memory; static random access memory (SRAM) and dynamic random access memory (DRAM). SRAM is normally stored on the logic processor, with level 1 (L1) being closest to the logic core, resulting in it being the fastest memory in the hierarchy. It is used to store instructions and data for future requests, also known as cache. The main memory is constructed from DRAM, which is typically separated from the logic processor and bridges the hard disk with SRAM. SRAM is constructed from 6 transistors arranged in a specific configuration whereas DRAM works by charging and discharging a capacitor alongside a select MOSFET. Both these volatile memories have low read and write times meant for high performance. In addition to these volatile memories, non-volatile memory (NVM) is needed to store the essential information that must be maintained without power. This is usually done using a floating gate MOSFET known as Flash, which comes in two

main designs; NOR and NAND. However, flash memory has reached physical limitations including dielectric thickness and applied voltages required due to the demand for higher electric fields needed for programming/erase operations, whilst retaining low leakage [11]. In the radiation environment, the large amounts of transistors in SRAM, DRAM and Flash also decrease overall radiation hardness of the traditional memory hierarchy.

New systems are being investigated as a replacement to this transitional memory hierarchy, known as universal storage class memory (SCM). In this universal memory hierarchy, as shown in Figure 1.3(b), emerging NVM cells offer high speed, scalable and cheap replacements for DRAM and Flash. This tackles many problems simultaneously including the lack of volatility of DRAM and the high power needs and scaling issues of Flash. In order for the emerging memory to act as a buffer between SRAM and hard disk, the requirements needed include being back-end-of-line (BEOL) compatible, with $> 10^{15}$ endurance cycles, > 10 years retention and read/write times of < 10 ns [10].

The emerging SCM types include phase change memory (PCRAM), ferroelectric memory (FeRAM), magneto-resistive memory (MRAM) and resistive switching random access memory (RRAM) [12]. The most promising class of emerging non volatile memory is resistive switching based memory, RRAM. A comparison between traditional and emerging NVM memories is shown in Table 1.2. Due to excellent memory properties, including scaling down to sub-10nm dimensions, high density arrays, low power and simple device structures, RRAM is fast becoming a strong candidate for the next type of non-volatile memory.

RRAM is based upon resistive switching whereby the resistance of the device is altered through an electrically induced change. RRAM cells consist of a simple metal-insulator-metal (MIM) cell where the insulator layer is often a mixed-conducting oxide, or a chalcogenide [12,13]. Switching cycles occur between a high resistance state (HRS) and a low resistance state (LRS).

	Traditional Memory				**Emerging Memory**			
	DRAM	**SRAM**	**Flash NOR**	**Flash NAND**	**FeRAM**	**MRAM**	**PCRAM**	**RRAM**
Feature size (F) (nm)	36	45	45	16	180	65	45	<5
Read time	2 ns	0.2 ns	15 ns	0.1 ms	40 ns	35 ns	12 ns	1 ns
Write time	2 ns	0.2 ns	1 us	0.1 ms	65 ns	35 ns	100 ns	<1 ns
Retention time	4 ms	n/a	>10 yr	>10 yr	>10 yr	>10 yr	>10 yr	>10 yr
V_{write} (V)	2.5	1	8-10	15-20	1.3-3.3	1.8	3	<0.5
V_{read} (V)	1.7	1	4.5	4.5	1.3-3.3	1.8	1.2	<0.2
Write endurance	$> 10^{16}$	$> 10^{16}$	10^5	10^5	10^{14}	10^{12}	10^9	$> 10^{12}$
Write energy (J/bit)	$4x10^{-15}$	$5x10^{-16}$	10^{-10}	$4x10^{-16}$	$3x10^{-14}$	$2.5x10^{-12}$	$6x10^{-12}$	$< 10^{-12}$

Table 1.2: Comparison of traditional and emerging memories [14].

1.2 Radiation Hardness of Logic and Memory

Events, such as the failure of the Telstar satellite in 1962, have shown that it is the semiconductor devices that are most prone to failure when irradiated [15]. The type of radiation will vary with different environments caused by a range of activities including fission reactors, high energy particle experiments such as CERN, space and nuclear industry. When a semiconductor device is irradiated there are two different types of damage mechanisms that can occur; Displacement damage and ionizing damage [16]:

- **Displacement Damage:** Atoms are moved from their lattice sites by incident radiation. This affects the crystals electronic characteristics. This depends on the energy and momentum that is transferred to the lattice atoms and is therefore dependent on the particle type (mass) and energy.
- **Ionizing Damage:** Incoming radiation ionizes the device and liberates charge carriers. These carries then travel around the device and become trapped resulting in areas of concentrated charge and therefore parasitic fields. This is independent on the type of radiation but depends on the absorbed energy through which ionization is the dominant absorption mechanism.

The two types of radiation damage can occur from a range of particles such as photons (in the form of X-rays, γ-rays etc), charged particles (such as electrons or protons), neutrons and atomic ions. In the nuclear and space environments, the main cause of displacement damage in semiconducting devices will be from the release of neutrons. One of the effects of displacement damage is the alteration of the minority carrier lifetime in the silicon substrate. For a bipolar device, which is a minority carrier device, the alteration in lifetime will heavily affect the device's gain [17]. However this reliance of the minority carrier lifetime in a MOS device is negligible and therefore MOS devices are relatively insusceptible to displacement damage. Increased junction leakage current is another effect the displacement damage can cause but due to the small dimensions of a MOS device this damage mechanism is not a primary concern. The other type of damage mechanism, ionizing damage, is a big problem for MOS devices and therefore it is this mechanism that this research will focus on.

With the increasing density and scaling of MOSFET features sizes, the possibility of latchup increases. Latchup occurs when ionizing radiation causes a leakage path to form in the silicon, between two MOSFETs in a CMOS structure. This problem was overcome in the radiation industry by transferring to SOI technology. The n-well is no longer present and the active silicon area is heavily reduced, removing the potential leakage path [18]. However the presence of three oxide areas (the gate oxide, STI and BOX) have the potential to reduce the radiation hardness of MOSFETs today. With the move from silicon dioxide, to high-k gate oxides, the radiation tolerance is changed.

Therefore it is vital to investigate the radiation tolerance and effects of the new high-k MOS devices. With the memory occupying around half the chip in a processor today, the

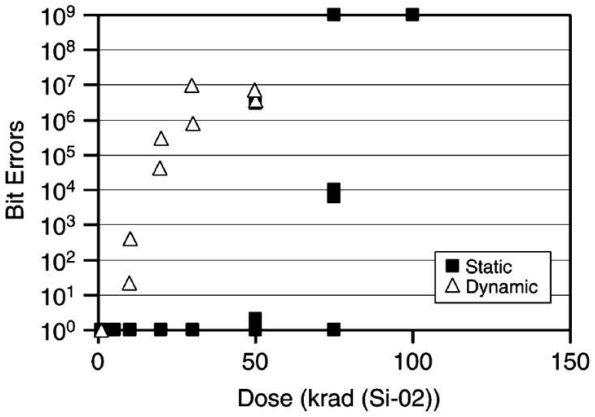


Figure 1.4: Error bit rates for flash memory (90nm node technology) for increasing total ionizing dose [19].

investment into radiation hardened memory is key for developers designing systems for use in radiation environments. Recently, with CMOS processes used to fabricate flash circuitry, high sensitivity to total ionizing dose has been repeatedly seen. The dynamic and static error rates are shown in Figure 1.4 for a 90 nm node flash memory cell whereby the number of errors increases rapidly with total ionizing dose [19]. More recently, improvements in voltage threshold distributions after radiation have been achieved with floating gate devices, although the demand for higher voltage CMOS devices elsewhere in the circuit suggests that ionizing radiation is still a major problem for semiconductor memories [10]. Fundamentally, semiconductor memories have poor radiation hardness levels.

New memories, such as RRAM, offer a potentially radiation hardened replacement for semiconductor memories. Not only does RRAM show superiority in terms of pre-radiation specifications, but also with simple structures and small device areas, RRAM could withstand high levels of ionizing radiation. Therefore it is of the uttermost importance that the radiation effects of resistive memory be investigated.

1.3 Thesis Outline

Due to scaling of devices towards smaller and smaller dimensions, high-k dielectrics are being utilised in MOS capacitor structures to overcome leakage issues, whilst RRAM is the potential replacement for semiconductor memories. Before using these new technologies in harsh environments such as space and nuclear, the radiation effects must be investigated, understood and controlled. The key area where ionizing radiation causes damage is within dielectric layers. Therefore this thesis will investigate the radiation effects and reliability of dielectrics for CMOS transistors and resistive memories.

Chapter 2 defines what is meant by the term dielectric. Following this, the ionizing radiation effects in dielectrics are discussed whereby a well known model of radiation mechanism in silicon dioxide MOS capacitors is explained. Using this, the radiation effects of MOS capacitors are described, followed by the effects seen in MOS transistors. Finally, resistive memory is discussed whereby a theory of switching is described followed by the potential radiation effects.

Chapter 3 describes the development of a high-k metal gate TiN/HfO_x stack. This chapter shows the material characterisation and process development used to control the stoichiometry and crystal structure of the hafnium oxide. Following this, techniques used to control of the TiN electrode stoichiometry are also discussed. The varied stoichiometries and material properties are utilised later for resistive memory in Chapter 5, whilst the fabrication of both TiN and HfO_x are used in Chapter 4, Chapter 5 and Chapter 6.

Chapter 4 presents the investigation into the radiation of high-k MOS capacitors. HfO_2, Al_2O_3 and SiO_2 MOS capacitors were fabricated along with TiN and Al gates. The pre-radiation properties are analysed allowing a comparison between the high-k and conventional silicon dioxide capacitors to be conducted. The MOS capacitors were measured before and after the ionizing radiation. A discussion of the radiation effects on high-k capacitors, compared to silicon dioxide capacitors is included.

Chapter 5 discusses the investigation into effects on switching properties and effects of radiation on TiN/HfO_x/TiN valence change memory cells. Firstly, the role of stoichiometry of the TiN electrode on switching properties are shown, followed by the role of stoichiometry of the HfO_x layer. The ionizing radiation effects on the memory cells with varied stoichiometry of the HfO_x layers are viewed and discussed.

Chapter 6 presents the work conducted on switching kinetics and radiation effects of SiC electrochemical memory cells. Cu/a-SiC/Au ECM memory cells have been measured using pulse voltage scheme and then irradiated. Firstly the switching kinetics of the SiC memory cells are studied, and the switching properties discussed. Following this, the ionizing radiation effects of the SiC memory cells is presented.

Chapter 7 summarises the key results of the work presented in this thesis and concludes with the identification of devices areas with high sensitivity to ionizing radiation.

Chapter 2

Theory of Radiation Effects of Dielectrics

Large amounts of research have been conducted into the ionizing radiation mechanism that occurs in silicon oxide MOS capacitor structure [20–22]. The model for SiO_2 is often used as a basis for radiation effects that occur in other dielectrics and other structures due to the simple structure. The total ionizing dose effects in MOS oxides model is explained in Section 2.2.

Dielectric layers play a key part in the reliability of two types of electrical devices in particular; MOS transistors and resistive memory cells. Within the MOS transistor, three different dielectric areas are present, all of which are prone to radiation effects. The radiation mechanism that can occur in the different types of dielectric layers within a MOS transistor is discussed in Section 2.4.

Within a resistive memory cell, the dielectric layer is sandwiched between two electrodes and acts as the switching layer. The current theory of the switching mechanism is discussed in Section 2.5 followed by a discussion of possible radiation mechanisms.

2.1 Dielectric Materials

All materials can be defined as an insulator or a conductor. Charges have the ability to move freely around conductors, where as in insulators, these charges are attached to atoms or molecules. When insulators are put into an electric field, although not free to move around the material like in conductors, the charge can be displaced by microscopic distances, resulting in polarization.

In an atom, as the electrons and nucleus are pulled apart, their mutual attraction between each other will keep them together, until an equilibrium is reached. This results in

the polarization of the atom. The dipole moment of this atom, $\vec{p}$ is given by Equation 2.1 and will align in the same direction of the electrical field.

$$\vec{p} = \alpha \vec{E} \tag{2.1}$$

The atomic polarizabilty, α depends on the detailed structure of the atom.

When we consider an insulator in an electric field, the polarization is given by the dipole moment per unit volume, $\vec{P}$. In order to calculate the effect of polarization on the initial field, instead of adding all the infinitesimal contributions from all dipoles together, **bound charges** are used, named after the fact that electrons are attached to specific atoms or molecules and therefore cannot be removed. This bound charge is given by the net charge over a surface for uniform polarization, taking into account the charge within the insulator and on the surface. Therefore the field due to the polarization of the medium can be described as the field of the bound charge.

The total field within the medium is defined by the field resulting from the bound charge (field produced by polarization) plus the field due to everything else (known as **free charge**) as shown in Equation 2.2. This free charge can originate from defects like ions in the insulator, or from electrons from nearby conductors.

$$\rho = \rho_b + \rho_f \tag{2.2}$$

Inserting Equation 2.2 into Guass' Law and rearranging then gives Equation 2.3. Part of this equation can then be replaced by introducing the new term, electrical displacement $\vec{D}$, given by Equation 2.4.

$$\nabla \cdot (\epsilon_0 \vec{E} + \vec{P}) = \rho_f \tag{2.3}$$

The electrical displacement is a very useful term as it is dependent only on free charge and is not altered by the introduction of a dielectric.

$$\vec{D} \equiv \epsilon_0 \vec{E} + \vec{P} \tag{2.4}$$

The polarization term $\vec{P}$ is defined in Equation 2.5 where χ_e is the electrical susceptibility of a medium, whose value is dependent not only on the microscopic structure of the material but also external conditions such as temperature. The electrical susceptibility therefore describes how easily the material polarizes.

$$\vec{P} = \epsilon_0 \chi_e \vec{E} \tag{2.5}$$

Using this definition of polarization, the electrical displacement can now be rewritten as Equation 2.6, where the prefactor ϵ is the permittivity of the material, as given by Equation 2.7. Equation 2.6 therefore shows how the electric field, $\vec{E}$ is reduced by amount ϵ due to the effect of polarization.

$$\vec{D} = \epsilon \vec{E} \tag{2.6}$$

$$\epsilon \equiv \epsilon_0(1 + \chi_e) \equiv \epsilon_0\epsilon_r \tag{2.7}$$

Removing the permittivity of free space, ϵ_0, results in a dimensionless quantity, ϵ_r. This is known as the relative permittivity or the dielectric constant of the material and is also given the term k_r [23]. This factor is a measurable term to indicate the amount the effective electric field is decreased due to the polarization of the medium.

From this definition, insulators that result in polarization when situated in an electric field, are referred to as dielectrics. As all insulators polarize in an electric field, all insulators are by definition dielectrics, although the two terms refer to two different physical mechanisms. The term dielectric refers to a medium which polarizes in an electric field whereas the term insulator refers to the ability for a material to resist the flow of electrons.

2.2 Ionizing Radiation Effects in Dielectrics

Radiation is a main concern for reliability of electronics for use in space and nuclear industries. In an radiative environment, the breakdown of dielectrics can be caused by defects within the dielectric reacting to the effects of radiation. The dielectric layers are greatly affected by ionizing radiation in particular, whereby charge is generated within the dielectric itself. It is the reaction between the defects and the charge that can lead to uncontrolled breakdown of the dielectric, resulting in device failure or error.

The ionizing irradiation degradation mechanism has been widely researched for silicon dioxide MOS capacitors. In order to gain a better understanding of defects and degradation mechanisms within other materials and structures, the silicon dioxide mechanism in a MOS capacitor can be viewed as similarities may exist. A brief overview of ionizing radiation terminology is explained first.

2.2.1 Ionizing Radiation

Ionizing radiation can be caused by photons, electrons, protons or atomic ions, as long as they have enough energy to liberate an electron from an atom, creating an ion or an

electron-hole pair (EHP) in the material of interest. For example, if a photon were to cause ionizing radiation in a piece of Silicon, the photon energy must be greater than the band gap of Silicon. Thus the energy needed will differ for material types whereby E_γ >1.1 eV for silicon and E_γ >9 eV for silicon dioxide [15].

The type of ionizing damage that occurs in insulators is referred to as Total Dose effects, also known as Total Ionizing Dose or TID effects. The total dose is the amount of energy deposited in any material by ionizing radiation and is given in units of Rad or Gray, where 1 Gray=100 Rad. The Rad is the unit that will be used where rad is the amount of energy absorbed per unit mass of material and so it can be seen that 1 rad=1 J/kg. The rad is material dependent and therefore the dose will be specified in rads with the material listed in brackets afterwards.

When materials are irradiated by ionizing radiation, electron-hole pairs are created. The number of electrons and holes generated in the material is directly proportional to the total dose, with an increasing number of electron-hole pairs for increased total dose. The type of ionizing radiation that is of particular importance in space and nuclear industry is gamma radiation at high TID levels.

The current theory of ionizing radiation effects, in a metal/silicon-dioxide/silicon structure, is presented here. This two-stage process describes how the defects, that occur in silicon dioxide from fabrication, react with the charge generated from ionizing radiation, leading to altered electrical characteristics. Multiple defects that exist in silicon dioxide have also been observed in many transitional oxides [24]. These similarities enables the comparison between silicon dioxide and transition metal oxides to be drawn, where the vast amount of research conducted on silicon dioxide defects and breakdown can be considered when considering breakdown in other dielectrics, e.g. high-k dielectrics.

2.2.2 Defects in Dielectrics

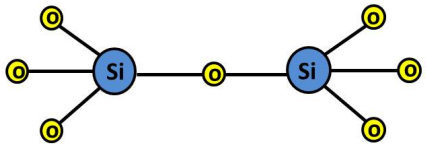
There are three main defects found within a metal/silicon-dioxide/silicon structure and are given here:

1. Neutral Oxygen Vacancies
2. H_2 located at minimum energy sites
3. Silicon-Hydrogen bonds at the oxide/semiconductor interface

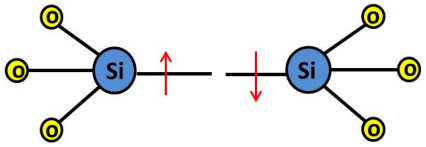
The neutral oxygen vacancy will be explained first. The basis of ideal SiO_2 consists of four oxygen atoms surrounding one silicon atom with highly-directional covalent bonds [25]. These oxygen atoms will then be bonded to one other silicon atom, so that every oxygen atom will be bonded to two silicon atoms, and every silicon atom will be bonded

to four oxygen atoms. This can be seen in Figure 2.1(a) where two silicon atoms, in blue, are connected to four oxygen atoms, in yellow. Please note the angle and bonds are not drawn to scale as this is just a picture representation of the silicon dioxide bonds.

In high temperature oxidation processes fabricating SiO_2, defects can occur when an oxygen atom does not form a bond with two silicon atoms [26]. This lack of an oxygen atom results in two Silicon atoms having an empty bond. These bonds are known as dangling bonds and each contain an unpaired electron of opposite spin. This defect is known as a neutral oxygen vacancy, or NOV, and is depicted in Figure 2.1(b) where the red arrows represent the unpaired electrons. It can also be represented by Equation 2.8 where the black dot represents the dangling bond, and the three lines represent the three individual bonds [27].



(a)

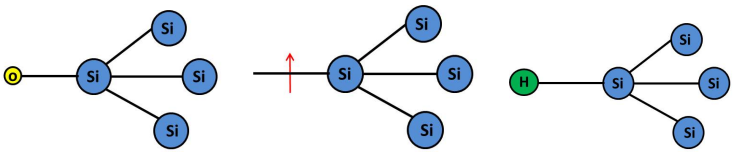


(b)

Figure 2.1: Picture Representation of (a) an ideal SiO_2 bond and (b) a neutral oxygen vacancy, adapted from [27].

$$O_3 \equiv Si^{\bullet} \qquad Si^{\bullet} \equiv O_3 \tag{2.8}$$

Another type of defect occurs due to hydrogen. Throughout the fabrication process, many steps use a hydrogen ambient, in water or gas form. These steps cannot be avoided and this level of hydrogen throughout device fabrication means it is nearly impossible to eliminate unwanted hydrogen [28]. When H_2 enters SiO_2, it will sit at minimum energy sites throughout the oxide and remain there. The third type of defect occurs at the oxide/semiconductor interface. When oxides are fabricated, there are still around 10^{13} cm^2 silicon bonds at the oxide/semiconductor interface that are not passivated with oxygen [22]. These silicon dangling bonds remain at the interface and are then passivated by hydrogen molecules. These hydrogen molecules are due to fabrications steps and diffuse into the oxides in the same manner as the molecular hydrogen described previously [29]. Figure 2.2(a) shows an ideal interface bond with the semiconductor on the right hand side and the oxide starting to form on the left hand side. Figure 2.2(b) shows the dangling silicon bond that occurs if there is no passivation by an oxygen atom



(a) (b) (c)

Figure 2.2: Silicon-silicon dioxide interface for (a) ideal silicon-silicon dioxide interface, (b) non-ideal Si dangling bond at silicon-silicon Dioxide interface and (c) non ideal Si-H Bond at silicon-silicon dioxide interface, adapted from [27].

and an unpaired electron is shown by the red arrow. Figure 2.2(c) shows the dangling bond which has been passivated by a hydrogen atom, leaving behind a Si-H bond.

The Si-H bond, the NOV and the molecular hydrogen are all defects that exist before the device is exposed to external or internal factors. It is *these* defects which later react with ionizing radiation, leading to device failure.

2.2.3 Ionizing Radiation Mechanism

Figure 2.3 depicts the MOS structure, where the three sections represent the metal, the silicon dioxide and the silicon substrate. The black and white dots in Figure 2.3 represent an electron-hole pair that has been generated due to the incoming ionizing radiation. Due to the bias on the device, these electrons and holes will be transported through the oxide in opposite directions. Before this happens however, some of the electrons and holes will recombine. The number of electron-hole pairs that escape recombination is known as the yield. The amount of initial recombination, and therefore this final yield, is dependent on the oxide electric field strength and the energy of the incoming ionizing particle.

If the device was irradiated by a single ion, a strongly ionizing particle would generate a higher density of EHPs in its path. Due to the close proximity between the electrons and holes, the recombination would be high. For a weakly ionizing particle, recombination would be low due to the lower density of EHPs. The yield will be larger if the electric field strength is larger due to the EHPs being accelerated away from each other, reducing the chance of recombination. Figure 2.4 shows a plot of yield as a function of applied field for ^{60}Co gamma rays, 12MeV electrons and is compared to the geminate model [22].

$$N_h = Y(E)\kappa_g D t_{OX} \tag{2.9}$$

The number of holes that remain in the oxide, N_h, can be found by Equation 2.9. This equation calculates the number of EHPs produced initially by the radiation and then takes into account the recombination, with the electric field strength and radiation type

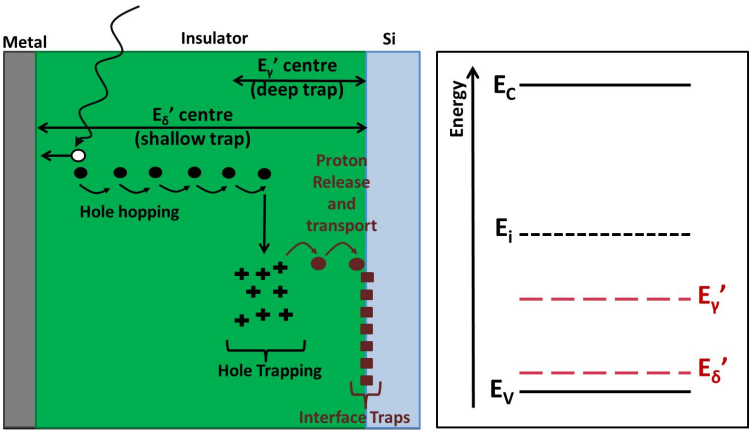


Figure 2.3: Electron-hole pairs generated in oxide by ionizing radiation followed by hole transportation and trap formation in the oxide. Proton release can also occur followed by transportation towards the interface leading to interface trap formation in the oxide. The energies of different traps are shown. This is adapted from [30].

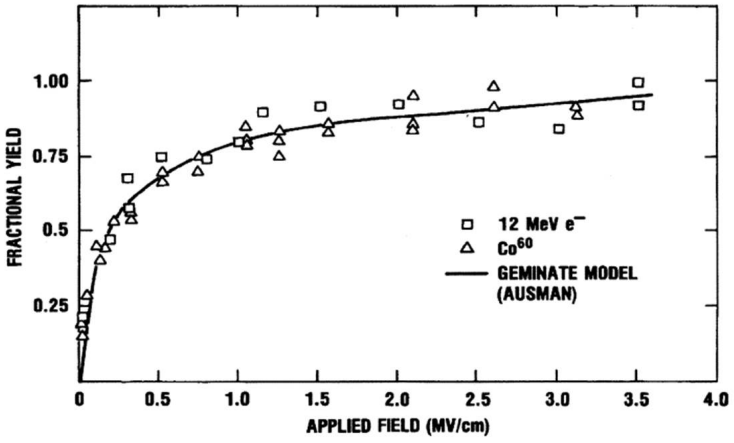


Figure 2.4: Fraction of holes that escape recombination as a function of applied electric field for gamma rays, electrons and compared to geminate model calculations [22].

dependencies. $Y(E)$, the hole yield, takes into account the recombination with the field and radiation type dependencies [20]. κ_g is the total pair generation rate which gives the initial EHP density generated per unit dose, for a certain material. Multiplying this by the total dose D will give the total EHP density generated. This will scale with oxide thickness and so the equation must be multiplied by t_{ox}.

The electrons and holes that escape recombination travel through the oxide at different rates, through different transport mechanisms and in opposite directions. In SiO_2, electrons are extremely mobile and get swept out of the oxide in the first few picoseconds. For a positive bias (on the metal), these electrons will be swept towards the metal as shown by Figure 2.3. The remaining holes then travel towards the oxide/semiconductor interface. This movement is slow and involves reactions with the defects in the oxide.

These reactions between the defects and holes result in two types of traps forming; oxide and interface traps.

Oxide traps occur when holes react with defects throughout the oxide bulk. The traps that occur, can be split into two types: shallow and deep traps. If a shallow trap is formed, the hole may hop through the oxide, towards the interface, between the shallow traps. If however the holes fall into a deep trap, they will become stuck here and contribute to a net positive charge in the oxide. This can be seen in Figure 2.3.

The shallow trap, shown in Figure 2.3 by $E_{\delta}^{'}$, has an energy around 1 eV above the valence band in the oxide, allowing the holes to fall in and escape out of the trap easily. This, along with the positive bias on the electrode, facilitates the hopping towards the interface. The deep trap, shown in Figure 2.3 by $E_{\gamma}^{'}$, has an energy around 3 eV above the valence band. When a hole falls into this trap, it cannot escape back into the valence band and so becomes trapped.

These two traps, or E centres, exist in different parts of the oxide, spatially. The shallow traps can be found throughout most of the bulk oxide, whereas the deeper traps are mostly found near the oxide/silicon interface. This is depicted in Figure 2.3, where the black arrows show the lateral area the traps are most likely to form. The deep traps act differently, depending on their location with respect to the interface [21]. If the deep trap is further away than 3 nm from the interface, the trap acts as a deep hole trap, where the hole forms a fixed positive charge, N_{OX}, known as a *Fixed State*. If however the trap is within 3 nm of the interface, the trap can emit or absorb charge from the silicon, known as a *Switching State* [31]. This is done through electron tunnelling and results in a neutral state but does not remove the trapped hole. This effect is an annealing effect which reduces the effect of the total fixed positive charge in the oxide, over time.

The event of a hole becoming trapped in a deep trap, causes a hydrogen ion (a proton), to be released. Due to the positive charge, this proton then travels towards the interface. The way in which the protons reach the interface was researched by Oldham and McLean [22], where they found the protons hopping distance was 0.26 nm. This matched the distance between the oxygen atoms in SiO_2, and therefore it was verified that the protons hop between the oxygen atoms until they reach the interface. Once the protons reach the interface, a reaction occurs with the Si-H defects, and an interface trap is formed. This proton release, transport and interface trap formation can be seen in Figure 2.3.

This two-stage process whereby a hole becomes trapped, releasing a proton that then travels towards the interface, reacting with the Si-H bond, creating an interface trap has been verified by many different groups [32–38]. There are still a few other theories that some people prefer. A different theory suggest that the formation of interface traps occur from holes reacting with the Si-H bonds, not protons [39]. The dynamics however are not explained and this theory has been disproved by Oldham et al. [40]. Another theory is the interface traps are formed by neutral hydrogen instead of protons, but this

was shown to be very small, by Saks et al. [41]. Therefore the theory that will be used is the two-stage proton transport model, until proved otherwise [22].

The oxide trap formation is explained first, followed by explanation of interface trap formation.

Oxide traps form when the holes, generated by the radiation, come into the vicinity of neutral oxygen vacancies, as shown in Figure 2.5(a). When the hole becomes trapped in the NOV, the NOV structure relaxes back into a different state. This new relaxed structure, in which the hole is trapped, is the E$'$ center. The NOV structure can relax into two different states and it is these two states that form the shallow and deep traps.

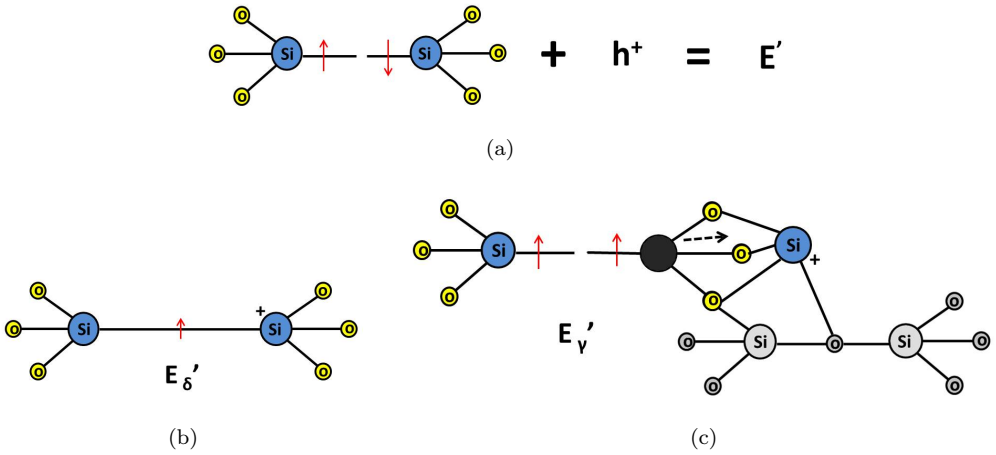


Figure 2.5: Defects in SiO_2 (a) NOV and a hole react to give a E' centre (b) dimer shallow trap formation (c) puckered deep trap formation, adapted from [27].

The shallow trap, E'_δ, is formed when the hole reacts with the NOV, and the NOV structure then relaxes into the state shown in Figure 2.5(b). The two previous silicon dangling bonds have now joined together and lengthened their bonds. The hole is trapped at one of the silicon sites and the two silicon atoms now share an unpaired electron. Due to the trapped hole, the charge of E'_δ is positive. The shallow trap is also known as the *Dimer* E$'$ center, or E'_δ.

The deep trap, E'_γ, is formed when the hole reacts with the NOV, and the NOV structure then relaxes into the state shown in Figure 2.5(c). The black and black atom shows where the silicon atom was previously and the arrow shows where the silicon atom has now moved. In this structure one of the silicon atoms, with the unpaired electron, remains the same as shown on the left hand side of Figure 2.5(c). The other silicon atom however relaxes by passing through the plane of the three original oxygen atom. This silicon atoms then bonds itself to another oxygen atom from another site as shown by the grey arrangement of atoms. This silicon atom is now bonded to *four* oxygen atoms, and the newly bonded oxygen atom is now bonded to *three* silicon atoms. The hole has become

trapped and is located at the new oxygen bond. This structure has a positive charge also and is known as the *Puckered* E′ center, or E'_γ. [21, 26, 42]

These E′ centres are so named due to the unpaired electrons being consistent with observed signatures found using electron paramagnetic resonance (EPR) technique. These defects were then labelled E′ [43, 44]. It is these two different structures that the holes either hop between in the shallow traps, or become fixed charge, in the deep traps.

Long-term annealing effects however can occur, over hours or years, neutralizing or compensating the net positive fixed charge due to holes trapped at deep traps. This annealing is dependent on time, temperature and applied field and occurs through either tunnelling or thermal excitation. At room temperature, tunneling is the dominant mechanism but for increased temperatures, thermal excitation can take over. Many mechanisms were proposed however work by numerous groups have led to one accepted model; an electron tunnels to the neutral Si in a deep trap forming a dipole structure between the trapped electron and hole [22]. As the bias on the device is altered, the extra electron can tunnel between the substrate and the deep trap.

As mentioned before, the trapping of the hole in the deep trap can cause a proton to be released, which then travels on towards the interface, creating interface traps.

The holes produced by ionizing radiation have reacted with one of the defects, the NOV. The holes then become trapped and form the E′ centres. The second defect, molecular hydrogen, then is activated once the E′ centres are formed. Previous to irradiation, the molecular hydrogen sits at minimum energy sites throughout the oxide. When the E′ centres are formed, these sites then become a lower energy site for the molecular hydrogen to react with. It is the reaction of the molecular hydrogen with the E′ centres that releases a proton.

The molecular hydrogen has two different reactions with the two different E′ centres. The E'_δ centre reacts with the hydrogen and then acts as a proton sink. This is shown in Figure 2.6 where the hydrogen has caused the longer Si-Si bond to break, and the molecular hydrogen has separated into two protons, each proton passivating each dangling bond. The structure is stable in this state and the protons will not be released, hence this is said to be a proton *sink*.

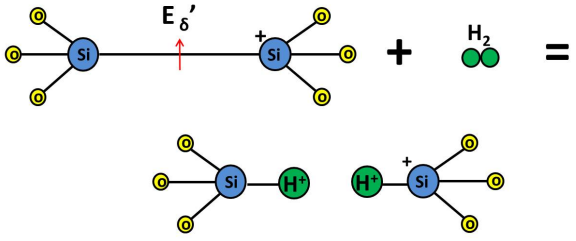


Figure 2.6: Molecular hydrogen reacting with Dimer trap, adapted from [27].

When the molecular hydrogen comes into the vicinity of the E'_γ centre, a proton source is created. This is shown in Figure 2.7 where the molecular hydrogen has separated with one of the protons passivating the dangling bond, whilst the other sits at one of the oxygen sites on the other silicon atom. This proton then travels between the oxygen atoms, until it reaches the interface. This is called a proton *source* due to the release of the proton.

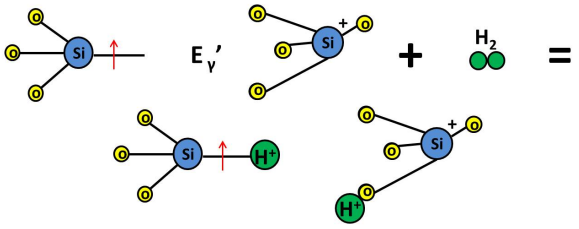


Figure 2.7: Molecular hydrogen reacting with Puckered trap, adapted from [27].

The proton released from the puckered sites will hop through the oxygen atoms until they reach the interface. The proton reacts with the Si-H defects at the interface to form interface traps. The reaction that occurs is given by Equation 2.10, where the interface trap is given by the excited silicon atom, Si^*.

$$Si - H + H^+ \rightarrow Si^* + H_2 \tag{2.10}$$

The molecular hydrogen diffuses away and the trivalent Si defect is left behind and is known as a P_b centre [28]. The interface state is amphoteric in nature whereby they are either positive or negative depending on the device bias. The interface traps lie on the oxide/silicon interface but the charge of the trap is determined by the silicon properties as the traps sit in the silicon band gap. The two different types of traps are known as donor and acceptor traps. Donor and acceptor traps differ in charge with respect to whether they are full or empty of electrons. A donor interface trap is one that is neutral when filled with an electron and positive when empty. An acceptor interface trap is negative when filled with an electorn and neutral when empty. The definitions of donor and acceptor is given in Table 2.1. There is strong evidence that the donor interface traps are located in the lower half of the silicon band gap, whilst the acceptor interface traps are located in the upper half of the silicon band gap [15].

	Donor Charge	**Acceptor Charge**
Full	neutral	negative
Empty	positive	neutral

Table 2.1: Charge of Donor and Acceptor traps with different electron concentration

The position of the fermi level in the silicon, and therefore the bias of the device, determines whether the donor and interface traps are filled or empty, altering the overall

charge at the interface. For a p-type MOS capacitor, for a negative bias, the device will be in accumulation. An accumlation region, full of majority carriers in the silicon is shown in the schematic representation of the device in the lower half of Figure 2.8(a). Figure 2.8(a) also shows the energy band diagram when the device is in accumulation, with the addition of the acceptor and donor trap levels shown by the pink and green stripes respectively. As the fermi level in the silicon at the interface is below both the acceptor and donor traps, neither contain any electrons. Looking at Table 2.1 it can be seen that when both are empty, the donor traps have a positive charge, and when the acceptor traps are empty they are neutral. The net charge is therefore a positive charge at the interface between the oxide and silicon as shown in the picture representation of the device layout in the bottom half of Figure 2.8(a).

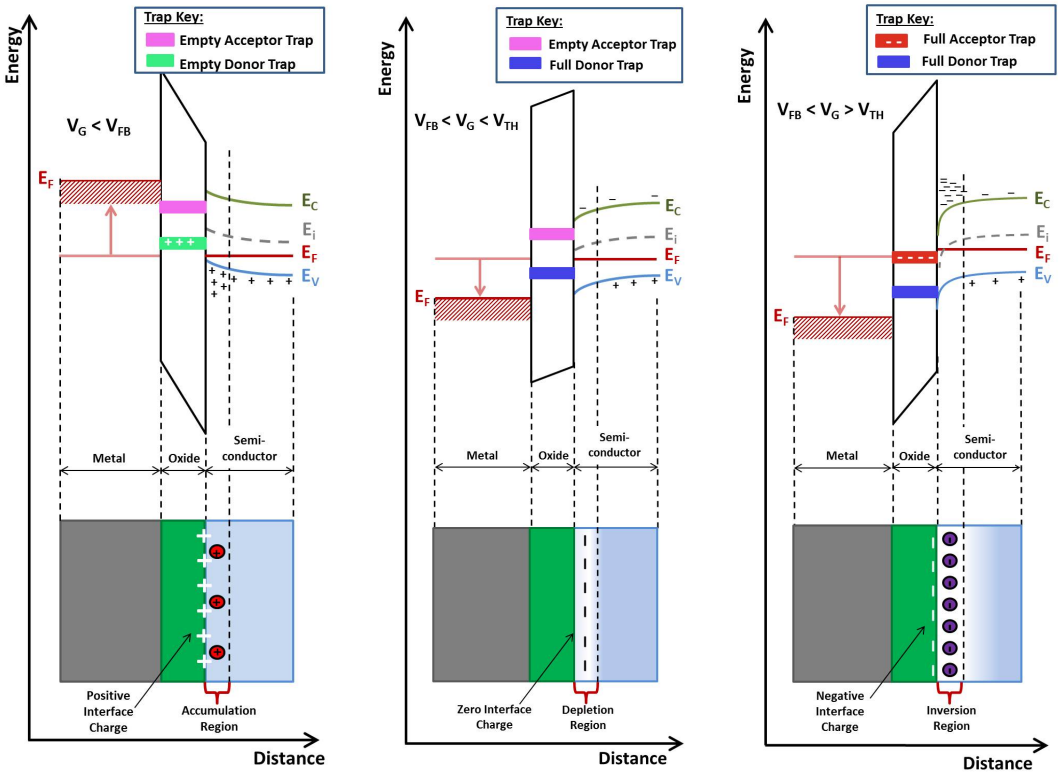


Figure 2.8: Energy band diagrams with schematic representation below, of a p-type MOS capacitor with acceptor and donor interface traps in; (a) accumulation, with both interface traps empty resulting in a positive charge build-up at the interface (b) depletion, with the donor traps filled and the acceptor traps empty resulting in zero interfacial charge build-up (c) and inversion, with both the donor and acceptor interface traps filled resulting in an overall negative charge build-up at the interface.

As the voltage on the metal gate is increased, the device will go into depletion as shown by the schematic representation in the lower half of Figure 2.8(b). This will raise the fermi level in the silicon which can be seen in the energy diagram in Figure 2.8(b). The

donor traps are now fullwith electrons, shown by a blue band, as the fermi level is above the trap level, and therefore neutral in charge. The acceptor traps are still empty, shown by a pink band, and so are also neutral. Therefore the interface traps are neutral and there is no build-up of charge at the interface.

When the bias is increased further, the device will reach inversion whereby minority carriers are thermally generated, resulting in an inversion region in the silicon below the oxide/silicon interface. This is shown by the schematic representation of the device in the lower half of Figure 2.8(c). As the device reaches inversion and the fermi level is risen again, the acceptor traps become full with electrons, shown by the red band. This can be seen in Figure 2.8(c) where the fermi level is above the acceptor trap level. This will result in negative charge building up at the interface between the oxide and silicon.

Depending on the dopant of the substrate and the bias on the device, the interface traps will either be negative, neutral or positive. This will then either contribute or counteract the positive trapped oxide charge from the holes.

2.3 Irradiation of MOS Capacitors

In order to investigate radiation effects on MOS transistors, MOS capacitors are often utilised due their simple structure. Ideal MOS capacitor characteristics are explained first followed by the effects of radiation.

2.3.1 Ideal MOS Capacitor

The MOS capacitor structure can be used as a simplified model of a MOSFETs as the MOS capacitor structure exists within the MOSFET device. A layer of metal deposited on the back of the substrate is used to create an ohmic contact. This section will describe the modes of operation of a MOS capacitor. A p-type substrate will be considered unless stated otherwise, known as a nMOS capacitor. For an *ideal* MOS capacitor, a few assumptions must be made first. These assumptions are uniform doping of substrate, zero current flow in gate oxide and zero charge in gate oxide. An ideal MOS capacitor has four different modes of operation which are dependent upon the voltage applied to the gate. These are flatband, accumulation, depletion and inversion.

The first mode of operation is the 'Flatband' mode. This occurs when the device is in thermal equilibrium with 0 gate voltage applied. If the device is *not* in thermal equilibrium then a voltage must be applied to obtain the flat band mode, known as the flatband voltage V_{FB}. The *Flatband* name comes from the energy band diagram whereby the fermi level of each material is at the same level and therefore appears to be 'flat'. This can be seen in Figure 2.9 with the three vertical sections representing

the metal, oxide and semiconductor layers. For an intrinsic semiconductor the electron and hole concentrations are equal which is represented by the intrinsic fermi level, E_i, which will be exactly half way between the conduction band energy, E_C and the valence band energy, E_V. Figure 2.9 shows a nMOS Capacitor where the fermi level, in the semiconductor, is below E_i due to there being more holes in the valence band than there are electrons in the conduction band. For a pMOS capacitor, the fermi level in the semiconductor, is above E_i due to there being more electrons in the conduction band than there are holes in the valence band. In both of these capacitors there is no build up of charge in the semiconductor at the gate oxide/semiconductor interface. In other words the electron and hole densities are the same at the interface as they are in the main body of the semiconductor.

For a MOS capacitor not in thermal equilibrium, the flatband voltage required for zero band bending in the semiconductor to occur can be calculated. The required parameters include the metal work function, ϕ_M, the semiconductor work function, ϕ_S, half the semiconductor energy gap, $\frac{E_g}{2}$, the electron affinity, χ, and the bulk potential, ψ_B. The flatband voltage for an ideal MOS capacitor is given by the difference between the metal and semiconductor work functions as shown inEquation 2.11.

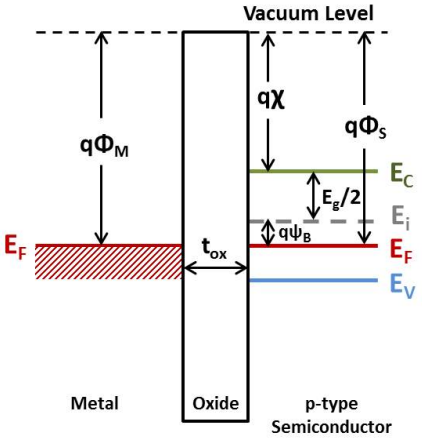


Figure 2.9: Flatband energy band diagram for nMOS capacitor with parameters labelled.

$$V_{FB} = \phi_M - \phi_S = \phi_M - q\chi - \frac{E_g}{2} - \psi_B \tag{2.11}$$

The electron affinity and the energy gap are both constants that are material dependent. The bulk potential is the difference between E_i and E_F. This parameter is *not* constant but depends upon the doping concentration in the semiconductor N_a the intrinsic carrier concentration n_i and the temperature T. This can be seen in Equation 2.12 where k and q are the Boltzmann constant and electric charge respectively. Using Equation 2.11 and Equation 2.12, the flatband voltage can be calculated.

$$\psi_B = \frac{kT}{q} ln \left(\frac{N_a}{n_i} \right) \tag{2.12}$$

When a gate voltage is applied that is no longer equal to the V_{FB}, the flatband condition is no longer met. Depending on the magnitude and the polarity of the voltage applied, there are three more modes that the MOS Capacitor can be in. In order to explain these three modes, the nMOS Capacitor will be taken into consideration first.

The first mode, known as *Accumulation*, occurs when a voltage below the V_{FB} is applied to the gate, which is normally negative. The negative charge on the gate will attract the excess holes in the p-type substrate towards the oxide/semiconductor interface as shown in Figure 2.10(a). This process can also be illustrated using the energy band diagram. Here the negative gate voltage causes the metal fermi level to rise and this then causes the oxide energy band to tilt upwards towards the gate. This tilting of the oxide energy band in turn causes the band bending to occur in the semiconductor. This band bending now means that E_V is closer to E_F at the interface than it is in the bulk, causing the hole concentration to be larger at the interface. This build up of majority carriers forms the accumulation layer.

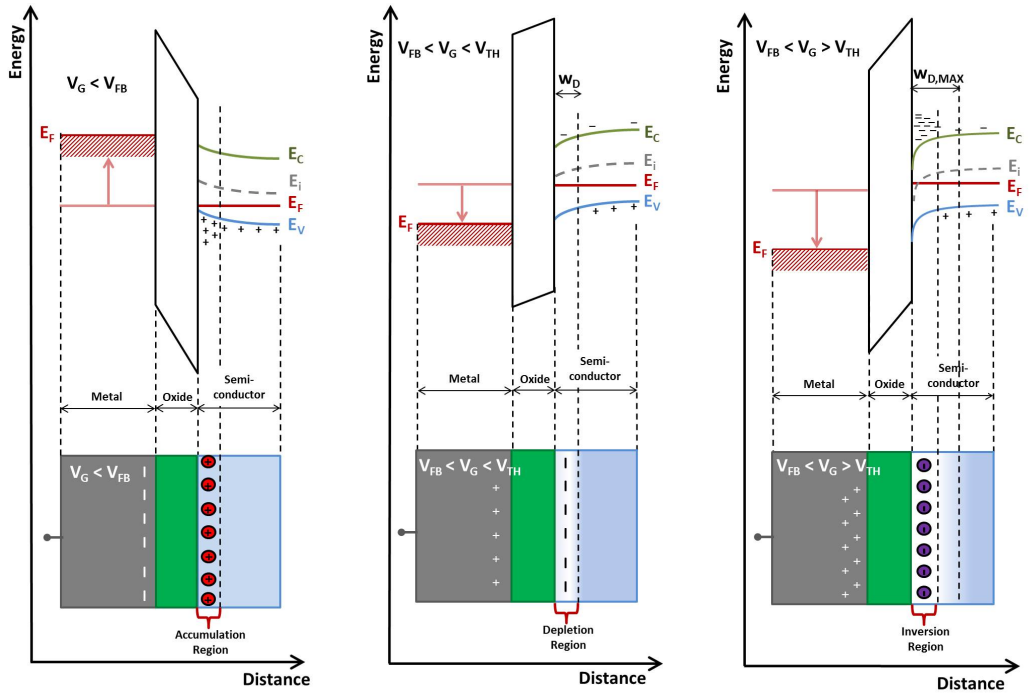


Figure 2.10: Charge build up and energy band diagram shown for an nMOS Capacitor in (a) accumulation (b) depletion and (c) inversion.

The second mode of operation occurs when a small positive applied voltage exceeds V_{FB} and is known as *Depletion*. The positive charge on the gate will cause the holes to

be pushed deeper into the substrate away from the interface. This results in a region, near the interface, that is depleted of mobile carriers leaving behind negatively charged acceptor ions. Figure 2.10(b) shows the depleted region in white under the oxide and also shows the negatively charged acceptor ions. The fermi level in the resulting energy band in the metal decreases which causes the oxide energy bands to tilt downwards towards the gate. Band bending then occurs in the opposite direction in the semiconductor when comparing it to accumulation. At the oxide/Semiconductor interface the E_V is further away from E_F when comparing to the E_V's position deeper in the bulk. This results in holes being depleted away from the interface. With increasing applied voltage, the depletion region width increases and the minority carriers (electrons) will be attracted towards the interface. However in the depletion region the concentration of electrons is negligible. The depletion width is proportional to the square root of band bending (the surface potential, ψ_S, which is the change in potential from bulk to surface). This is shown in Figure 2.11.

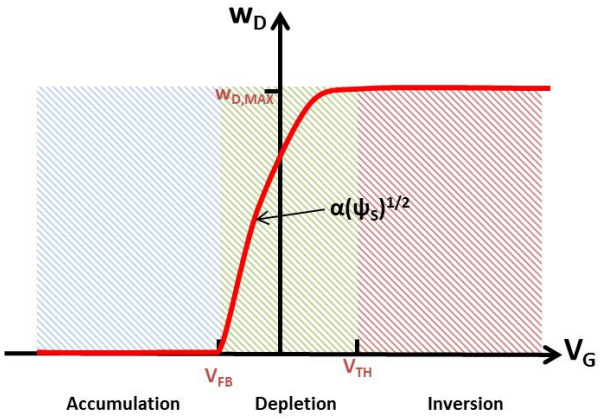


Figure 2.11: Depletion width of a MOS capacitor plotted with respect to gate voltage. Increase in depletion width is proportional to the square root of the surface potential.

The third mode of operation is called strong inversion. If the gate voltage is increased even further, it will eventually reach the situation where the electron concentration at the oxide/semiconductor interface will be greater than or equal to the hole concentration of the bulk semiconductor. The semiconductor material under the interface has now become n-type and this region is known as the n-channel. The threshold voltage, V_{TH}, is reached when the surface potential (amount of band bending) is equal to twice the bulk potential, ψ_B resulting in the surface electron concentration becoming so large that the surface is now inverted, forming an n-channel. This is shown in Figure 2.12.

The n-channel can be seen in Figure 2.10(c). Compared to the energy band diagram for the depletion mode, the band bending for the inversion mode can be seen to be much larger, due to the metal's fermi level being lowered by a greater amount. This causes the hole concentration to decrease further at the interface and also causes the electron

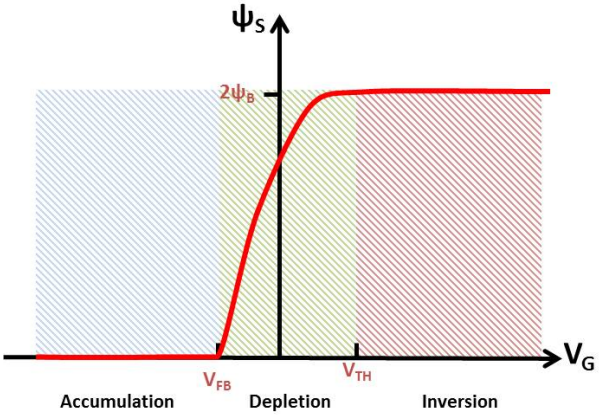


Figure 2.12: Surface potential (amount of band bending) plotted against gate voltage. Threshold voltage reached when surface potential equals twice the bulk potential.

concentration to increase at the interface. The semiconductor band bending is so large that the fermi level in the semiconductor is now very close to E_C at the interface, causing the increased concentration of electrons. This is the formation of the n-channel.

The point of strong inversion, V_{TH}, is mathematically well defined and can be calculated by using Equation 2.13.

$$V_{TH} = 2\psi_B + \gamma\sqrt{2\psi_B} + V_{FB} + V_{ot} \tag{2.13}$$

V_{FB} and ψ_B have already been calculated for the flatband voltage calculations using Equation 2.11 and Equation 2.12. V_{ot} represents the voltage shift caused by trapped oxide charge. The final parameter that needs to be inserted into Equation 2.13 is the body factor, γ. This body factor comes from an effect of the substrate (or body) bias. The body factor is given by Equation 2.14, where ϵ_S and N_a are the permittivity and doping concentration of the substrate respectively, q is the electric charge and C_i is the oxide capacitance.

$$\gamma = \frac{\sqrt{2q\epsilon_S N_a}}{C_{OX}} \tag{2.14}$$

If the applied gate voltage is then increased further, above the threshold voltage, the depth of the depletion width under the interface will not increase further (this is true for the static, equilibrium case). When the electrons form at the interface, the high concentration and rapid increase with gate voltage shield the deeper parts of the bulk semiconductor from any additional charge that is applied to the gate. This leads to a *maximum depletion depth* which cannot be exceeded with increasing V_G. The equation for the maximum depletion depth, $w_{D,max}$, is given by Equation 2.15 where ϵ_S and N_a are

the permittivity and doping concentration of the substrate respectively, q is the electric charge and ψ_B is the bulk potential, given by Equation 2.12. For a MOS capacitor with typical silicon doping of 10^{17} cm^{-3}, the maximum depletion width is calculated to be around 100 nm.

$$w_{D,max} = \sqrt{\frac{4\epsilon_S \psi_B}{qN_a}} \tag{2.15}$$

For a pMOS capacitor, the three modes occur for reversed gate voltage polarities, with V_{TH} having a negative value. Table 2.2 shows the gate voltage required to put *ideal* nMOS and pMOS capacitor's into the three modes and the flatband condition [1,15,45].

	Flatband	**Accumulation**	**Depletion**	**Inversion**
nMOS Capacitor	$V_G = 0$	$V_G < 0$	$0 < V_G < V_{TH}$	$0 < V_G > V_{TH}$
pMOS Capacitor	$V_G = 0$	$V_G > 0$	$0 > V_G > V_{TH}$	$0 > V_G < V_{TH}$

Table 2.2: Applied Gate Voltage on ideal nMOS and pMOS Capacitors required for the operation modes

Capacitance-Voltage (CV) measurements are a powerful tool used for characterizing MOS Capacitors. The CV results contain details about the gate oxide and substrate which can easily be extracted, such as bulk and interface charges, oxide thickness, flatband voltage and threshold voltage . When measuring the CV characteristics of a MOS Capacitor, one probe is placed at the gate contact whilst the other is placed at the back contact (substrate contact). A DC bias is applied which is superimposed with a small AC signal. There are two different type of measurements; high and low frequency. The high frequency, usually at 1 MHz, causes the modulation voltage to change at a rate which is too fast for the minority carriers to respond to. At the lower frequencies the minority carriers *are* able to respond to this voltage modulation. The two different frequency measurement CV curves are shown in Figure 2.13 which shows an nMOS Capacitor in the three different modes of operation as the gate voltage is increased.

The physics behind the shape of the CV curves will now be explained for a nMOS Capacitor. The capacitance in the MOS theory is given by Equation 2.16 where Q_G is the charge on the gate, V_G is the gate voltage and Q_{sub} is the charge on the substrate. The negative sign takes into account that the gate voltage is taken at the top capacitor plate, but the charge on the substrate is taken at the bottom capacitor plate which is the body.

$$C \equiv \frac{dQ_G}{dV_G} = -\frac{dQ_{sub}}{dV_G} \tag{2.16}$$

When an nMOS capacitor is in accumulation the majority carriers form at the oxide/semiconductor interface. In this mode the device is a simple capacitor where the

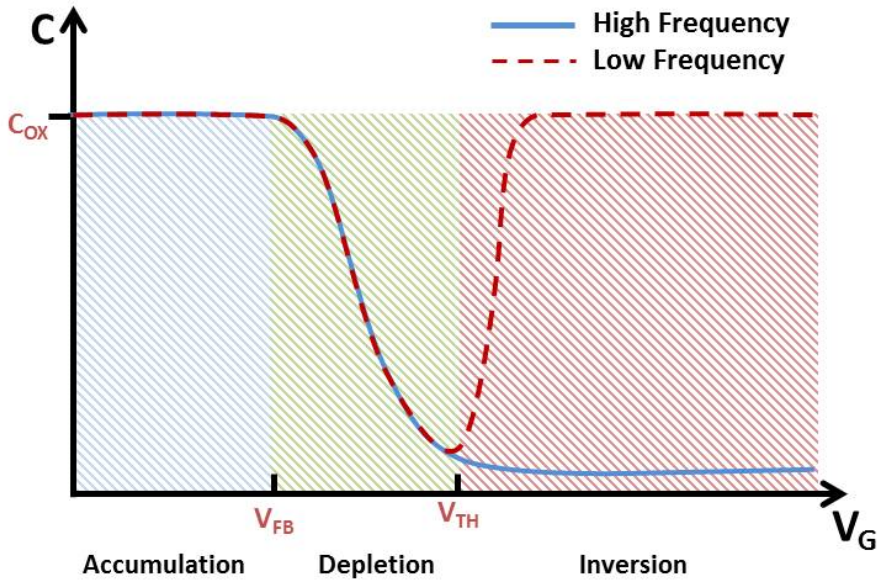
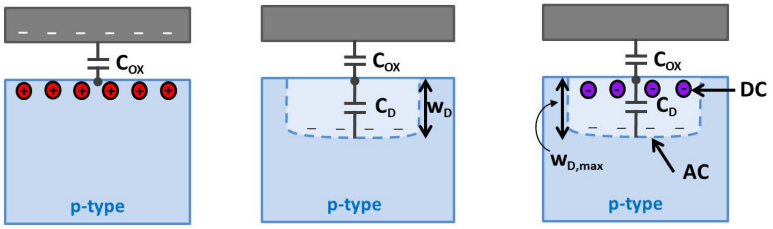


Figure 2.13: High and Low Frequency CV Curves for nMOS Capacitor.

top electrode is the gate. The majority carriers that have formed at the oxide/semiconductor interface are able to respond the the AC signal and act as the bottom electrode. This is depicted in Figure 2.14(a). The total capacitance is therefore that of the gate oxide, C_{OX}. This is the flat part of the curve for the negative gate voltages.



(a) (b) (c)

Figure 2.14: nMOS Capacitor in (a) accumulation region (single capacitor) (b) depletion region (two capacitors in series) and (c) inversion region with no supply of inversion electrons (high frequency case).

As the gate voltage increases, the depletion mode is reached. At this stage the gate oxide capacitor and the depletion layer capacitor, C_D, are both in series. The varying voltage due to the AC signal will cause AC charge to appear at the bottom of the depletion layer and can be seen in Figure 2.14(b). This means the depletion layer will increase and decrease slightly around the w_D width value, at the AC frequency. The total capacitance will be a combination of the oxide capacitance, C_{OX}, and the depletion region capacitance, C_D. The total capacitance is now given by Equation 2.17.

$$C_{total} = \frac{C_{OX}C_D}{C_{OX} + C_D} \tag{2.17}$$

The depletion layer capacitance can be calculated using Equation 2.18, where ϵ_S is the permittivity of the substrate and w_D is the depletion layer width. As V_G increases and the depletion layer width increases, C_D will decrease due to the inverse relation shown in Equation 2.18. This will cause the total capacitance to decrease with increasing gate voltage. This results in a negative CV slope which can be seen in Figure 2.13 for both curves.

$$C_D = \frac{\epsilon_S}{w_D} \tag{2.18}$$

As V_G increases further the device will eventually be put into inversion. This inversion layer is made up of minority carriers and can be labelled Q_{inv}. In a MOSFET, these minority carriers would be supplied by the heavily doped n regions, and the supply of minority carriers would be constant. However in a MOS capacitor these minority charges must be produced through thermal generation which occurs at a very slow rate. The slow generation of minority carriers in the inversion layer, compared to the frequency of the AC signal, causes the high and low frequency signals to differ.

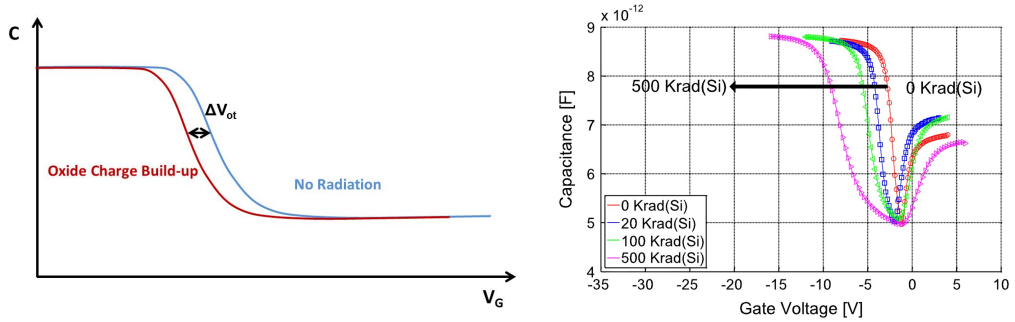
In the low frequency case of a MOS capacitor, the generation of minority carriers that produce Q_{inv} is able to respond to the AC signal. This results in Q_{inv} to increase and decrease at the AC frequency resulting in the inversion layer acting as the bottom electrode for the capacitor. The set-up is therefore similar to the accumulation setup and the total capacitance reverts back to the gate oxide capacitance, C_{OX}.

In the high frequency case of a MOS capacitor, the generation of minority carriers is too slow for the Q_{inv} to respond to the AC signal. The inversion layer therefore does not vary but remains constant at the DC value. The AC signal will therefore cause the width of the depletion region to increase and decrease around the maximum depletion width value, $w_{D,max}$. The width of the depletion region is able to respond to the high frequency signal as it only involves the movement of the majority carriers which are in abundance. The AC charge therefore forms at the bottom of the depletion region which can be seen in Figure 2.14(c). The set-up is now two capacitors in series with the depletion width being at its maximum value. This results in the total capacitance being at its minimum value, due to the inverse relation with depletion width. This can be seen in Equation 2.19, where ϵ_S is the permittivity of the substrate and $w_{D,max}$ is the maximum depletion width [46].

$$C_{min} = \frac{C_{OX}\left(\frac{\epsilon_S}{w_{D,max}}\right)}{C_{OX} + \left(\frac{\epsilon_S}{w_{D,max}}\right)} \tag{2.19}$$

2.3.2 Radiation Effects of MOS Capacitors

When a MOS capacitor is irradiated, the build-up of charge in the oxide will alter a MOS capacitors C-V properties. In MOS capacitors, a build up of positive oxide charge will mean the depletion mode of a MOS capacitor will be reached at lower voltages, resulting in a negative C-V curve shift. This is de-pictured in Figure 2.15(a) and is also seen for smart-cut BOX capacitors without fluorine implantation Figure 2.15(b).



(a) (b)

Figure 2.15: Trapped oxide charge causing negative shift in CV curves shown as (a) picture representation and (b) in 400 nm smart-cut BOX MOS capacitor with no fluorine implant for unbiased configuration (data by K. Potter [47]).

The shift in voltage due to oxide traps can be calculated by using Equation 2.20 where ϵ_r is the dielectric constant of the insulator, ϵ_0 is the permittivity of free space, q is the charge and N_{ot} is the number of oxide traps.

$$V_{ot} = -\frac{t_{ox}}{\epsilon_r \epsilon_0} q N_{ot} \tag{2.20}$$

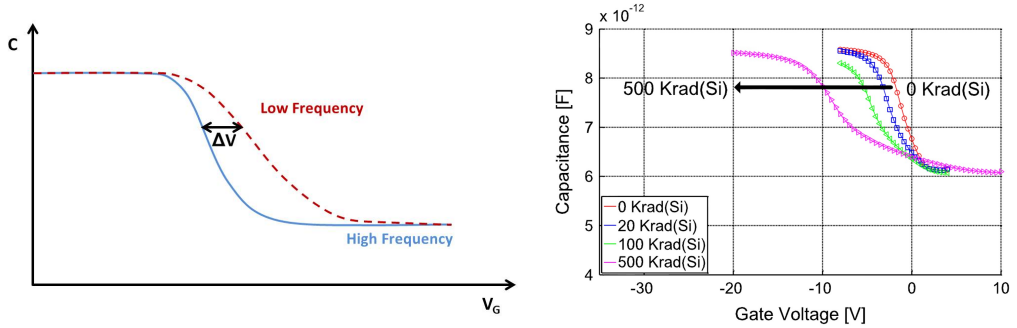
The buildup of oxide traps, N_{ot} is proportional to the thickness of the oxide and the total dose and is given by Equation 2.21 where D is the total ionizing dose, κ_g is the EHP density per rad, $Y(E)$ is the fractional charge yield (the number of EHPs that escape initial recombination divided by the total number of EHPs generated) and f_{ot} is the hole trapping efficiency (function of electric field in the oxide).

$$N_{ot} = D\kappa_g Y(E) f_{ot} t_{ox} \tag{2.21}$$

From this and Equation 2.20 it can be found that the threshold voltage shift caused by the oxide trapped charge is proportional to the oxide thickness squared. This is shown in Equation 2.22 where the negative sign represents the negative voltage shift [21]. This relation shows that for increased thickness in oxide, the effect of oxide traps will be larger. This therefore shows the thinner oxides are more radiation hardened.

$$-\Delta V_t\left(N_{ot}\right) = -V_{ot} = \frac{f_{ot} q D \kappa_g Y(E) t_{ox}^2}{\epsilon_r \epsilon_0} \tag{2.22}$$

For a MOS Capacitor, the effects of the interface traps can be seen by measuring the C-V curve of the device at a low and high frequency. At the high frequency the interface traps cannot fill and empty at a high enough rate when compared to the rate of change in ac voltage. The C-V curve for the high frequency case will therefore be free of interface trap effects. At a low frequency however, the influences the interface traps have will appear in the C-V curve. The traps can now fill and empty in response to the AC signal which causes a shift in the voltage characteristics of the C-V curve. As explained before, in order to overcome the interface traps and switch the device on, an increased magnitude in bias is needed. If the temperature and the doping density is known, by measuring the gradient of the curve, the interface trap densities, D_{it} can be calculated [48]. The *stretching out* of the CV curve due to interface traps is de-pictured in Figure 2.16(a) and can be seen in Figure 2.16(b) for a 400 nm wet thermal oxide capacitor without fluorine implant.



(a) (b)

Figure 2.16: Interface traps causing shift in CV curves shown as (a) picture representation and (b) in 400 nm wet thermal oxide MOS capacitor with no fluorine implant for unbiased configuration (data by K. Potter [47]).

2.3.3 Buried Oxide Capacitors

MOS capacitors can be used to investigate radiation effects on different insulators that exist within a MOS transistor structure. The three insulator layers include gate oxide, buried oxide and the shallow trench isolation.

An investigation into the total dose response of fluorine doped BOX capacitors was conducted by myself and colleagues, as published in [47]. When fabricating buried oxides, different fabrication techniques can be used, resulting in different material properties and therefore different radiation responses. It had previously been shown that using nitrogen and fluorine implants can reduce total ionizing dose effects in BOX oxides fabricated using Separation by IMplantation of Oxygen (SIMOX) technique [49–53].

Little research, however, had been conducted into the role of fluorine implants into an alternate fabrication technique known as smart-cut. This technique involves wafer bonding whereby the dielectric layer is created through bonding oxidized silicon onto another substrate. Following this, the silicon on the top substrate is reduced in thickness, leaving behind the thin active layer for device fabrication. Smart-cut is a specific way of carrying out this technique using ion implantation to cut the top wafer, removing the unwanted silicon.

It was proposed that implanting different species into the oxides will result in passivisation of the interface traps. MOS capacitors were fabricated from Smart-cut SOI wafers, with and without fluorine implantation, in order compare the radiation effects. A batch of wet thermal oxide capacitors were also fabricated, with and without fluorine as a reference batch. In the investigation into total dose response of fluorine doped BOX capacitors, the fluorine doped smart-cut BOX capacitors showed a large negative threshold shift before irradiation. This was attributed to trapping of positively charged fluorine from ion implantation.

It is thought these fluorine ions become trapped at defects within the BOX. These defects are thought to exist at the bonding interface, along with additional defects created during ion implantation. After irradiation, these smart-cut BOX capacitors exhibit threshold and flatband voltage shift whereby this shift is larger for the fluorine implanted oxides. It was concluded that the positive effects of fluorine passivated interface traps was outweighed by the additional defects created through ion implantation. It was concluded that if fluorine doping is used for radiation hardening, utter most care must be taken to ensure non of the doping occurs within the BOX region.

BOX capacitors were shown to successfully investigate the radiation hardness of BOX oxides. The same can be done for gate oxides.

2.3.4 High-k MOS Capacitors

Scaling of MOSFETs has resulted in the reduction of the gate oxide thickness down towards the 1 nm range for silicon dioxide. At this physical thickness, electrons can tunnel between the gate contact and the active silicon area, resulting in increased gate leakage currents. A way to overcome this issue is through the use of high-k dielectrics. When the dielectric constant of a material is increased, the physical thickness of this high-k dielectric can be increased also, whilst maintaining the same capacitance compared to that of a much thinner silicon dioxide capacitor. This can be seen, in mathematic form, when comparing the capacitance of a silicon dioxide capacitor, shown in Equation 2.23, with the high-k capacitance, shown in Equation 2.24.

$$C_{SiO_2} = \frac{\epsilon_0 \epsilon_{SiO_2} A}{t_{SiO2}} \tag{2.23}$$

$$C_{high-k} = \frac{\epsilon_0 \epsilon_{high-k} A}{t_{high-k}} \tag{2.24}$$

One way the 'quality', or 'performance' of the high-k dielectrics is measured is through a term known as 'Equivalent Oxide Thickness' or EOT. Physically, this term describes the silicon dioxide thickness needed in order for the silicon dioxide capacitor to obtain the same capacitance as a high-k capacitor, as shown in Equation 2.25. For dielectrics with an high dielectric constant, the EOT will be very small, hence a very thin silicon dioxide layer would need to be used to acquire the same high capacitance value. Hafnium oxide for example, which has a bulk dielectric constant of 25 [54], can be deposited at a physical thickness of 10 nm whilst achieving an EOT of 1.5 nm.

$$EOT = \frac{\epsilon_{SiO_2}}{\epsilon_{high-k}} \cdot t_{high-k} \tag{2.25}$$

When irradiated, just as in silicon dioxide, defects that exist within high-k dielectrics will react with ionized radiation generated charge. It has been reported that there is a higher defect density in high-k stacks than in silicon dioxide stacks, most likely due to the lack of a shared element between the silicon semiconductor beneath and the top electrode [55]. It could also be due to the different bonds that exist within the materials. The main defects found to exist within high-k dielectrics are oxygen vacancies and silicon-hydrogen bonds [56, 57].

The oxygen vacancy is described as an intrinsic defect in the bulk of many transition oxides [24], and is reported to be present in hafnium oxide gate oxide films specifically [55], along with hafnium vacancies [58]. However, the dominant defect was found to be the oxygen vacancy in hafnium oxide, and has been measured to exist at about 0.3 eV below the hafnium oxide conduction band minimum, formed by breakage of Hf-O or Si-O bonds [56, 59].

Another defect that has been observed in a $Si/SiO_2/HfO_2$ structure is the $Si - H$ bond. This, along with the oxygen vacancies are both defects that have been observed in silicon dioxide. These similarities enables the comparison between silicon dioxide and high-k dielectrics to be drawn, where the vast amount of research conducted on silicon dioxide defects and breakdown can be taken into account when considering breakdown in high-k dielectrics.

Many papers have seen similar effects to those seen in silicon dioxide, whereby the irradiation of other dielectric devices have resulted in a shift in the C-V curve (oxide traps) or a stretch-out in the C-V curve (interface traps) [60]. This indicates similarities may hold true and therefore this phenomenological description can be used as a basis for other structures and materials. Irradiation of these high-k devices can therefore be analysed using a similar method used for silicon dioxide. However, adjustments to the

hole trapping efficiency for example, must be made to account for differences in materials properties, chemical bonds and reactions.

An estimation for the change in EHP density per rad is given by Equation 2.26 where $E_g(\mathrm{SiO_2})$ and E_g(high-k) are the bandgaps for silicon dioxide and the high-k dielectric, respectively.

$$\kappa_g(high-k) = \kappa_g(SiO_2)\frac{E_g(high-k)}{E_g(SiO_2)} \tag{2.26}$$

Due to the relatively new processes that have been used to fabricate high-k dielectrics, the quality and material properties of the thin films, and therefore defects and response to radiation, will alter and improve through process optimization. The radiation response of high-k dielectrics is heavily related to material properties and defects and therefore is an ongoing area of research as fabrication processes develop. As high-k dielectrics replace silicon dioxide, the layers deposited are becoming physically thicker.

High-k dielectrics could potentially have have an increased hole trapping efficiency f_{ot} , will have different κ_g values due to different band gaps and will be thicker compared to thinner silicon dioxide layers. All these reasons could result in the reduction of radiation tolerance for gate oxides in a MOSFET structure. Therefore the radiation effects of high-k MOS capacitors have been investigated, as described in Chapter 4 allowing the hole trapping efficiencies to be compared to silicon dioxide.

The radiation hardness of gate oxides and BOX oxides can be investigated using the capacitor structure. However additional radiation effects within a MOS transistor can occur. My colleagues and I conducted an investigation into the total dose radiation hardening of MOS transistors by fluorine implantation. This not only enabled the transistor response to radiation to be viewed, but also allowed the fluorine doping of the STI to be investigated.

2.4 Irradiation of MOS Transistors

A MOSFET is a four terminal voltage controlled current device and is shown in Figure 2.17. It consists of a doped semiconductor substrate (for example p-type) with two highly doped regions (for example n+) which are the source and drain regions with metal on top for electric contact. On top of the substrate, in between the source and drain region, sits a piece of metal, known as the gate, which is isolated from the substrate by a dielectric, known as the gate oxide. It is this metal-oxide-semiconductor gate structure that gives the MOSFET its 'MOS' part of the name.

The region of substrate underneath the gate is where the current flows between the source and drain and is known as the 'channel'. The type of carrier that flows in the

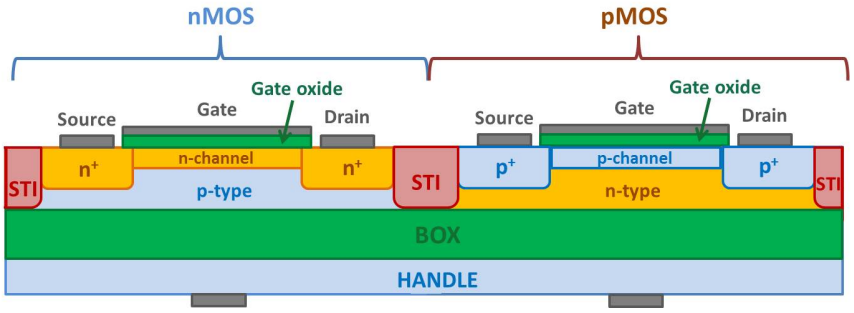


Figure 2.17: Schematic representation of a CMOS layout with both a nMOSFET and pMOSFET, with three areas of oxides present: gate oxide, BOX oxide and STI (field) oxide.

channel will be dependent on whether the MOSFET is a p-channel device or an n-channel transistor. In a n-channel MOSFET, the channel forms between the two n+ regions, where the carriers in the channel are electrons for the n-channel. For a p-channel MOSFET and the carriers are holes in the channel between the two p+ regions for the p-channel.

2.4.1 Ionizing Radiation Effects in MOSFETs

Ionizing radiation effects in MOSFETs occur when electron hole pairs are generated throughout the device. A transition from bulk MOSFETs to SOI MOSFETs occurred in the radiation industry in order to reduce an effect known as latchup. Latchup occurs when ionizing radiation produces EHPs in the silicon resulting in a low resistance path forming between the p-type substrate for example and an n-well. A schematic of latch up is shown in Figure 2.18 whereby the current is flowing from Vdd to ground directly via the two transistors.

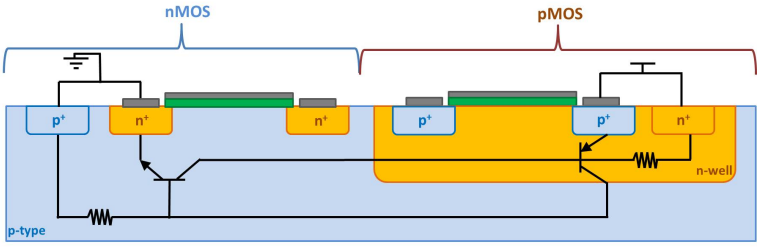


Figure 2.18: Schematic representation of a typical CMOS circuit with two transistors, npn and pnp connected to Vdd and ground. The two transistors can latch onto once another causing current to flow from Vdd to ground directly.

Here the n-well and substrate potentials are controlled by connecting the n+ doped contacts in the n-well to the most positive power supply and the p+ doped contacts in the substrate are connected to the most negative power supply. Photo currents flow in all p/n junctions resulting in a collector current of the pnp transistor flowing into the base

material of the npn transistor. The collector current from the npn transistor will flow into the base material of the pnp transistor. The result of this can cause two MOSFETs to latch onto one another resulting in very high currents flowing at low applied voltages.

The introduction of the BOX layer, using SOI wafers, reduces the active area of the silicon significantly and therefore reduces the latchup effect. The introduction of the BOX however does result in another ionizing radiation effect whereby radiation can generate EHPs in the BOX layer resulting in the lowering of the body-to-source barrier height. Excess electrons are then injected into the body and collected by the drain. If the electric field in the body is large enough, the accelerated electrons can produce more electrons through impact ionization resulting in a steep increase in drain current. A schematic of the charge build-up in the buried oxide inverting a back channel parasitic channel is shown in Figure 2.19.

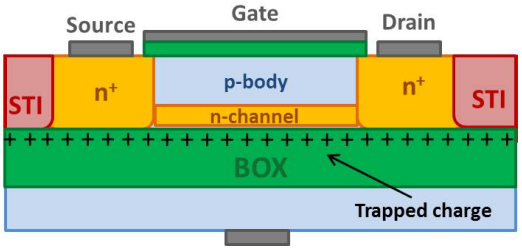


Figure 2.19: Schematic representation of a SOI nMOSFET after ionizing radiation resulting in generation of EHPs in the buried oxide. The result is charge build-up at the BOX/silicon interface causing an inversion of a back-channel.

Similar effects can occur when the STI is irradiated resulting in the generation of EHPs within the STI oxide, resulting in the accumulation of interface and bulk trapped charge. This can lead to side-wall and back channel parasitic devices turning on. The side-wall device can cause current to flow between the drain and source of one MOSFET, known as inter-device leakage and is shown in Figure 2.20. The back channel device between an n and p-type MOSFET, known as intra-device leakage, occurs when a leakage path forms between n+ doped source region of a transistor and the n-well of an adjacent p-channel transistor, as shown in Figure 2.21.

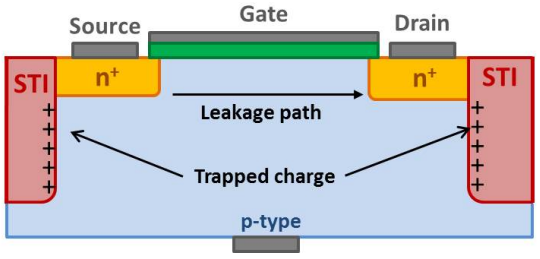


Figure 2.20: Schematic representation of a MOSFET with inter-device leakage path shown after ionizing radiation occurs in STI oxides causing side-wall parasitic device to turn on.

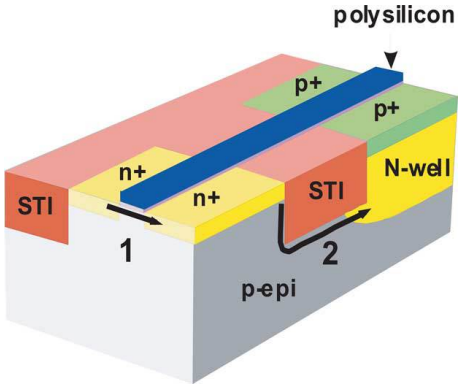
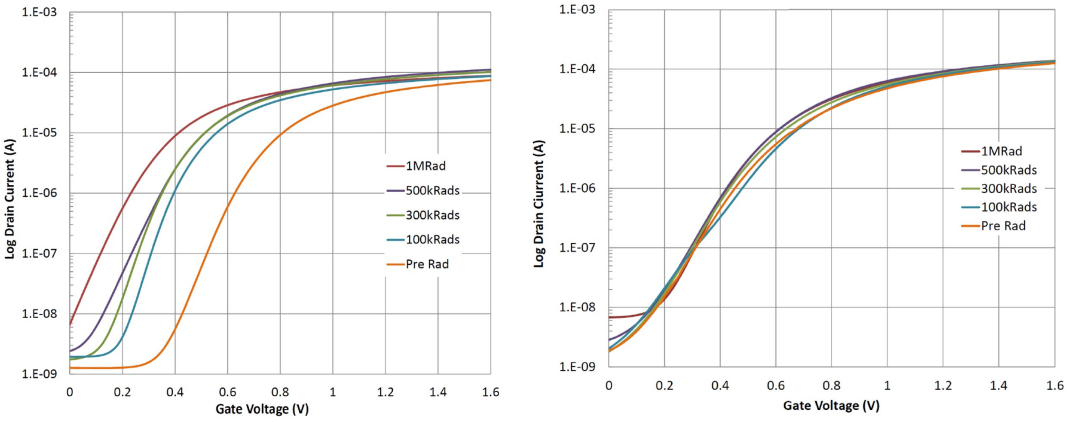


Figure 2.21: 3D Schematic representation of a MOSFET with intra-device leakage path shown after ionizing radiation occurs in STI oxides causing back channel parasitic device to turn on between two adjacent MOSFETs, [20].

Total dose hardness of MOS transistors with fluorine implant were investigated by myself and colleagues. Smart-cut wafers were used to fabricate the transistors, with special care taken to ensure the fluorine implant does not reach the BOX oxide. The fluorine implanted wafers received a blanket fluorine implant of 5x10^{15} cm^{-2} at an energy of 41 keV. The transfer characteristics of the transistors without fluorine and with fluorine implant can be seen in Figure 2.22(a) and Figure 2.22(b), respectively.



(a) (b)

Figure 2.22: Transfer characteristics for NMOS transistors at five different total ionizing dose levels from 100 krad(Si) to 1 Mrad(Si) (a) without fluorine implant and (b) with fluorine implant for unbiased configuration (data by C. Shaw).

Radiation effects in transistors can include a shift in threshold voltage, as described previously by Equation 2.13, an increase in off state leakage, and degradation of the subthreshold slope. This was seen for the transistors without fluorine implant, with a large negative voltage shift of 350 mV. The transistor however with fluorine implant showed no significant threshold voltage shift up to 1 Mrad(Si) and only small amount of leakage at this highest dose level. No change was seen either in subthreshold slope. This indicated that fluorine passivated the interface states in the STI, leading to no

turning on of sidewall parasitics, resulting in NMOS transistors being radiation hard up to 1Mrad(Si).

2.5 Irradiation of Resistive Memory

Resistive switching is based upon an electrically induced change in resistance of a device. RRAM cells consist of a simple MIM cell where the insulator layer is often a mixed-conducting oxide, or a chalcogenide [12, 13]. Switching cycles occur between HRS and LRS. The switching mechanism and operating scheme of resistive memory is explained first, followed by a description of the possible radiation effects.

Memristive switching, where the device can be converted between resistive and conductive states, was first seen in oxides in the 1960's [61]. The idea of using this resistive switching for memory applications was discussed in 1967, where the MIM structure was used [62]. However, at this time the switching phenomena was not actually able to be utilised for memory applications but instead was used as a demonstration of scientific theory [63]. As advances in thin film fabrication developed, an upsurge in the research of resistive switching occurred in the 1990's, where binary metal oxides were used. This improvement in the characterisation and optimisation of thin films and complex metal oxides, along with the reduction in silicon integrated circuit technology, has led to a thriving and active research area based upon resistive switching, where more recently RRAM has become one of the possible applications [61, 64]. In 2004, a paper was published showing the integration of RRAM cells in a CMOS structure, illustrating the CMOS compatibility of RRAM cells [61, 65]. RRAM is also back-end-of-the-line compatible, leading to an idea of a 3D stacked memory array, exhibiting high endurance (10^6 cycles), fast switching speeds (<10ns) with a possibility of low power consumption [61].

2.5.1 Resistive Switching

A RRAM device with a MIM structure can occupy two different resistive states with the ability to switch between these when a voltage is applied to the device. In the majority of memory cells, the basis of this switching occurs when a conducting path, known as a conductive filament (CF), forms in the insulator, connecting the two electrodes. When this filament is ruptured, due to a change in the applied voltage, electrons can no longer flow between the two metal electrodes and the device is said to be in the High Resistance State, or HRS. The switch from HRS to LRS is known as the SET process, whilst the reverse switch is known as the RESET process. Pristine samples that have not been switched before sometimes require a larger applied voltage, with a current compliance, to initiate soft breakdown. This is known as forming and only has to be done once initially for each device. The state of the device can be read easily by applying a small READ voltage, without affecting the state of the device.

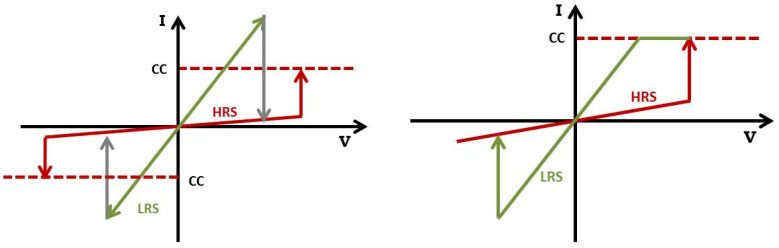


Figure 2.23: Schematic ideal I-V curves showing (a) unipolar and (b) bipolar modes of operation, with current compliance shown as CC.

There are two different types of switching that a device can exhibit; unipolar and bipolar. Unipolar switching is a symmetric switch whereby the switching of the device is dependent on the magnitude of the applied voltage, but not the polarity. This can be seen in Figure 2.23(a), where the device can switch between LRS and HRS in either polarity. Bipolar switching can be seen as anti-symmetric, where the switching depends not only on the amplitude of the voltage, but also on the polarity. This can be seen in Figure 2.23(b), where the transition from HRS to LRS is in the opposite voltage polarity to the transition from LRS to HRS. A current compliance is used to avoid permanent dielectric breakdown, limiting the amount of current that flows through the device.

The physical mechanism of switching between the LRS and HRS is thought to be based upon conductive filament formation and dissolution. The theory behind the formation and rupture of the conductive filament in a MIM structure is currently an active area of research. A phenomenological description of the CF formation and rupture, commonly referenced, is discussed here [61,64,66]. These models can be used but with caution as a unified model is still incomplete due to the lack of experimental and theoretical evidence and device variability.

The CF formation can be caused by a multitude of physical and chemical processes, each of which can occur simultaneously. Even though these processes are interlinked, most memory cells will have a dominant process. The three main processes are *thermal*, *electronic* and *ionic*. The *electronic* effect that can contribute to resistive switching, can occur in the form of electronic charge injection, and/or charge displacement effects. An example of electronic effects can be seen at high electric fields, when electrons can tunnel via a quantum mechanical effect and become trapped at defect sites in the insulator. This can alter the electrostatic barrier and therefore the resistance of the device. *Thermal* effects occur when parts of the insulator are altered through Joule heating. This can cause formation or rupture of local conductive filaments, causing partial dielectric breakdown, which alters the resistance of the device. The last effect, *ionic*, occurs due to the movement of ions and electrochemical redox reactions and will be the main focus of this research. Nanoionic redox based resistive switching can be sub-divided into two classes depending on the type of ion migration: cation or anion. Electrochemical

metallization memory effect (ECM) occurs through electrochemical dissolution and deposition of an active electrode resulting in migration of cations. Therefore cells with an electrochemically active electrode are needed for ECM memory to occur [64]. The second class, valence change memory (VCM) occurs in memory cells in particular, with transition metal oxides as the insulating layer whereby anion migration causes switching to occur [64].

ECM memory cells are known by other names including conductive bridging random access memory (CBRAM) and programmable metallization cells (PMC) [67]. ECM occurs when the MIM structure contains an electrochemically active electrode. The process starts with the oxidation of this electrochemically active electrode resulting in mobile cations. An example of Ag as the active electrode will be used, whereby the anodic dissolution of Ag is shown by Equation 2.27.

$$Ag \overset{Oxidation}{\rightarrow} Ag^{+} + e^{-} \tag{2.27}$$

Under an applied electric field, the cations, e.g. Ag^{+}, drift across the ion conductor (solid electrolyte) layer, towards the other electrode, which is inert. At the inert electrode the cations are reduced and electro-crystallize on the inert electrode surface. The cathodic deposition reaction is given by Equation 2.28.

$$Ag^{+} + e^{-} \overset{Reduction}{\rightarrow} Ag \tag{2.28}$$

This electro-crystallization process continues under electric field and leads to the growth of a filament until the anode and cathode are electrically connected via a conducting filament. This switches the device from HRS to LRS, or OFF to ON. This process is depicted in Figure 2.24, where Figure 2.24(a) shows the dissolution of the Ag to Ag^{+} ions, followed by the migration of the ions towards the inert Pt electrode in Figure 2.24(b), where the ions are reduced. Figure 2.24(c) shows the complete filament formation, becoming a conductive filament. The reset process occurs when the polarity of the applied bias is reversed. The conductive filament ruptures resulting in the device going from LRS to HRS, or ON to OFF [67]. Figure 2.24(d) shows the reset process where the filament is rupturing.

An array of materials have been utilised for ECM cells including Cu [69] and Ag [70] for the electrochemically active electrode and Pt [71], W [72] and Au [73] for the inert electrode. Multiple materials have reportedly shown ECM switching when used as the dielectric/ion conducting layer. This layer is usually thought of as a solid electrolyte but must be extended to include materials with low ionic conductivity [67]. If the layer has a high enough cation mobility in the ECM cell structure, ECM switching can occur. Therefore dielectrics, such as oxides e.g. silicon dioxide [74], have resulted in switching

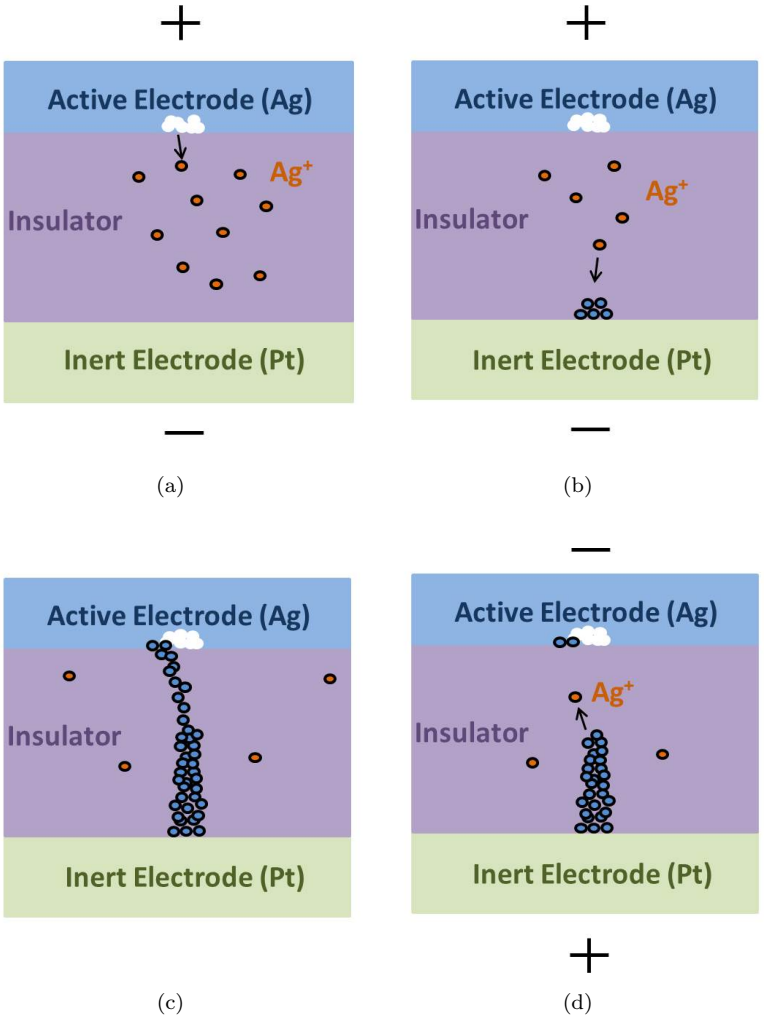


Figure 2.24: Schematic showing cation based switching with an active Ag electrode and an inert Pt electrode, adapted from [68]: (a) Dissolution of metallic Ag to Ag^+ (b) Reduction of Ag^+ (c) Device in LRS, CF formed (d) Device in HRS, CF ruptured.

due to the scaling resulting in high electric fields. Chalcogenides have also been reported for use as the electrolyte layer, such as GeSe [75]. Table 2.3 lists examples of structures of cation based resistive memory cells. Our amorphous SiC memory falls into this category.

Another type of resistive switching occurs through the movement of anions. Anion based switching occurs mostly in transition metal oxides, where defects, typically oxygen ions/vacancies, have a much higher mobility than cations. In VCM switching, it is thought the stoichiometry of the oxide is altered as oxygen vacancies form a conductive filament between the electrodes. [64, 82] In a pristine device, before any bias has been applied, switching cannot occur due to a lack of defect states in the oxide. In order to start the switching procedure, a forming step is used to create an increased number of defects by applying a large voltage. The subsequent electric field, $> 10\text{MV/cm}$, causes oxygen atoms to be knocked out of their lattice, which then drift towards the anode,

Active Electrode	Switching Layer	Counter Electrode
Cu	Cu:HfO_2 [76]	Pt
Cu	Cu:C [77]	Pt
Cu	Cu:SiO_2 [74]	W
Ag	Ag:$Ge_{40}Se_{60}$ [78]	Ni
Cu	SiO_2 [79]	Pt
Cu	GeSe [75]	W
Cu	SiC [71, 80]	Pt
Cu	Cu:WO3 [81]	W
Ag	MSQ [70]	Pt

Table 2.3: Resistive RAM Structures for cation based switching

leaving behind defects in the form of oxygen vacancies. A conductive filament is then formed from the oxygen vacancies, putting the device into its first ON state. This can be seen in Figure 2.26(a). The need for the large forming voltage has been verified in [83], where generation rate of trapped electrons has little dependence on low stress voltages, indicating that the dominant mechanism at low voltages is most likely the filling of existing traps (from fabrication) rather than the creation of traps. It isn't until higher stress voltages (forming voltages) are reached that new traps are created, and the conductive filament is fully formed, causing current-limited dielectric breakdown.

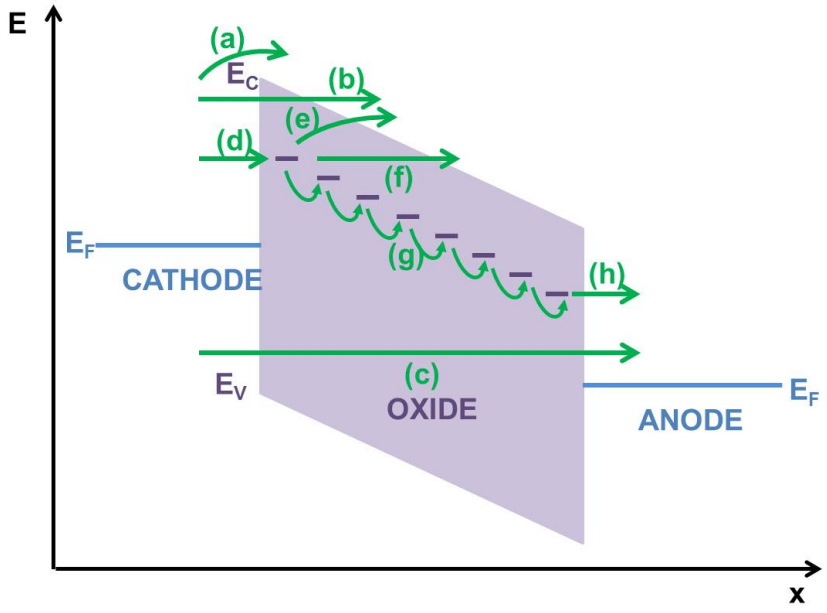


Figure 2.25: Picture representation of MIM energy band diagram showing variety of conduction paths for electrons between cathode and anode, adapted from [61]. (a) schottky emission (b) fowler-nordheim (F-N) tunnelling (c) direct tunnelling (d) tunnelling from cathode to traps (e) emission from trap to conduction band (poole-frenkel) (f) F-N like tunnelling from trap to conduction band (g) trap to trap hopping/tunnelling (h) tunnelling from traps to anode

Depending upon the electrode material types, different switching behaviours occur due to different reactions between oxygen ions and the anode. At the forming stage, and subsequent SET stages, if the anode material is inert, as for unipolar memory cells, the oxygen ions are discharged as neutral non-lattice oxygen. If the anode is oxidizable, as for bipolar memory cells, the oxygen ions react with the anode and form an oxygen reservoir. The oxygen vacancies that are left behind in the bulk oxide grow towards the anode. The oxygen deficient transitional metal cations are left in a reduced valence state. Electrons emitted from the cathode are then trapped. This filament grows towards the anode until it reaches and forms a conducting filament, putting the device into LRS. This is shown in Figure 2.26(b).

There are many ways in which the electrons can travel from the cathode to the anode with the dominant process determined by the transition rate. Due to the array of metal oxides use, the memory cells have different dominant conduction mechanisms depending on material properties (defects, bandgap), fabrication process and interfacial properties. The possible electron conduction paths in a generic MIM stack are depicted in Figure 2.25. Schottky emission occurs when thermally activated electrons travel over the barrier into the conduction band. Fowler-Nordheim tunnelling occurs when electrons tunnel into the conduction band due to high electric field. Direct tunnelling occurs when in thin films due to close proximity of cathode with conduction band. If a large number of defects/traps are located within the oxide, trap assisted tunnelling can also take place. Trap assisted tunnelling can occur in two stages where electrons are trapped within oxide from cathode. These electrons then can tunnel/emit from the trap to the conduction band (Poole-Frenkel emission/Fowler Nordheim respectively). Tunnelling can also occur when electrons tunnel into the anode [61].

After formation, there are enough defects present in the oxide such that subsequent following cycles require a much smaller applied voltage [64, 83]. In order to switch the device back to the HRS, a reset is needed. In this stage, the oxygen ions will travel back into the bulk of the oxide and recombine with the oxygen vacancies, rupturing the filament. The reset mechanism differs depending on whether the device is unipolar or bipolar. A complete explanation of these modes is not fully developed but it is thought bipolar can be explained in terms of ion migration, whilst the unipolar can be explained in terms of ion migration with assisted thermal dissolution. For unipolar memory cells, the concentration gradient of oxygen ions, along with joule heating caused by high currents in the filament, is thought to cause oxygen ions to diffuse from the area around the CF. Unipolar therefore requires a much higher reset current compared to bipolar, to ensure the local temperature around the CF is sufficient to aid this process. In bipolar memory cells, the oxygen reservoir, or interlayer, acts as a diffusion barrier and therefore the thermal dissolution is not enough to reset the bipolar mode. For bipolar, the oxygen ion movement must be done through an electric field change [61]. This is shown in Figure 2.26(c), where the oxygen ions fill in the vacancies and cause the

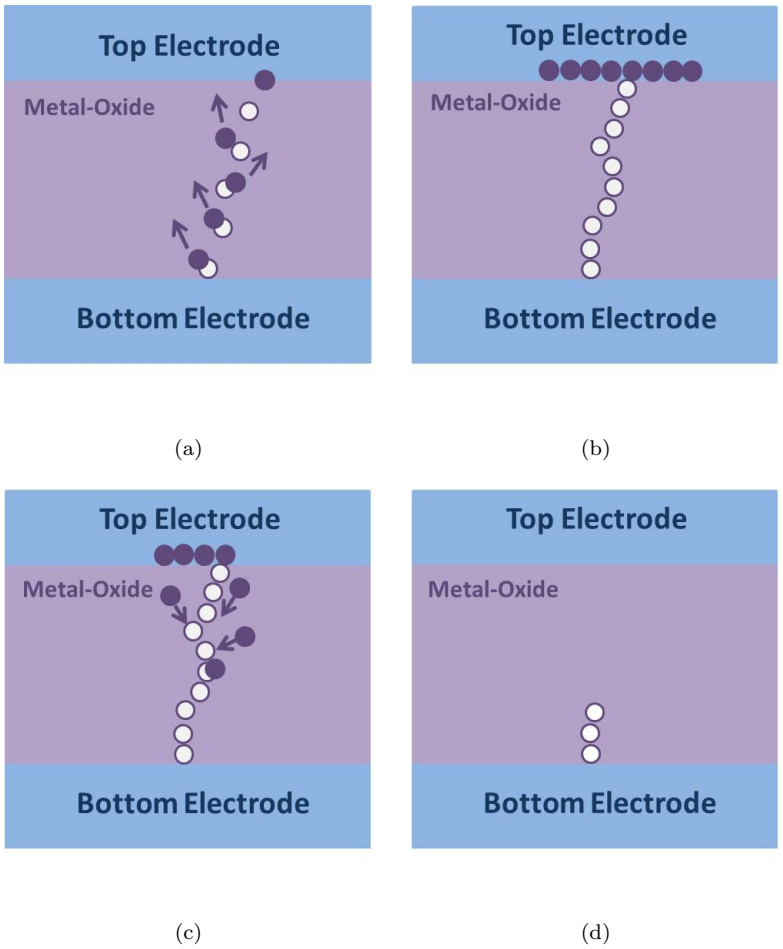


Figure 2.26: Schematic showing anion based switching with oxygen ions shown as purple circles, oxygen vacancies shown as white circles, adapted from [61]: (a) Forming: oxygen ions move towards electrode, leaving behind vacancies (b) LRS: CF formed, interfacial oxide layer formed if top electrode is oxidizable (c) Reset: Oxygen ions drift (bipolar) or diffuse (unipolar) and fill in vacancies (d) HRS: CF ruptured with remaining vacancies acting as virtual cathode.

CF to be ruptured resulting in HRS as shown in Figure 2.26(d). After forming, there are enough defects present in the oxide that such following subsequent cycles require a much smaller applied voltage [64, 83].

Top Electrode	**Metal Oxide Switching Layer**	**Bottom Electrode**
Pt	NiO [84], ZnO [85], HfO_2 [86], TiO_2 [87], ZrO_2 [88]	Pt
Ti	ZrO_2 [88], Al_2O_3 [89]	Pt
TiN	ZnO [90], HfO_2 [91]	Pt
Pd	TaO_y [92]	Pd
TiN	TaO_x [93]	Pt

Table 2.4: Resistive RAM Structures for anion based switching

The understanding of VCM switching mechanism is still limited compared to the ECM switching mechanism. There is still debate over the chemical process due to the challenging in-situ experimental methods of the atomic and electronic structures, during switching [94]. The variety of transitional metal oxides, along with the variety of electrode materials lead to many electrochemical processes that can occur. This also adds further challenge to creating a unified model. An array of materials that have been used for anion based resistive memory cells are shown in Table 2.4. Our HfO_x memory falls into this category.

The differences between VCM and ECM cells, including the physical switching mechanism, the materials/structures and unipolar/bipolar behavoir has led to advantages in applications for each type. VCM cells can be utilized as selection elements in crossbar arrays, helping reduce the sneak-path effect [95]. This 1D1R (one diode, one resistor) structure must have a resistive switching element with unipolar properties due to the diode limiting the reverse current. Therefore in this case, VCM cells have an advantage over ECM cells. The ECM cell however has the potential to exhibit multi-level switching through the control of the metallic filament. The LRS, determined by the SET current compliance can limit the strength of the filament, as well as the strength of the connection between the filament and active electrode. Furthermore a mechanism known as quantized electron transmission, involving the movement of just one metallic ion, indicates the scalability potential for ECM cells [96].

2.5.2 Radiation Effects in Resistive Memory

The radiation tolerance of future memory technologies must be addressed before use in space and nuclear industries. Current Flash technologies can only sustain TID up to 75krad(Si) [97]. Before replacing these memories with resistive memory, the effects of radiation must be investigated. The current understanding of irradiation of VCM memory cells is explained followed by irradiation of ECM memory cells.

The radiation effects of resistive memory cells are not fully understood. A few theories will be explained here in which similarities between radiation effects in silicon dioxide and resistive memory cells exist. One group theorise, for metal oxide resistive memory, electron hole pairs are generated in the oxide followed by some recombination. The remaining electrons and holes migrate through either drift of hopping motion under the internal electric field created by the work function difference between the top and bottom electrode. As the holes move, similar to radiation in silicon dioxide capacitors, some holes become trapped in the bulk and some become trapped near the interface. The proximity of the trapped holes to the electrode interface results in electrons from the electrode recombining with the trapped holes. Remaining trapped holes can act as a path for electron transport [93]. Another group have created a physical picture illustrating the radiation mechanism in hafnium oxide resistive memory cells [97]. It

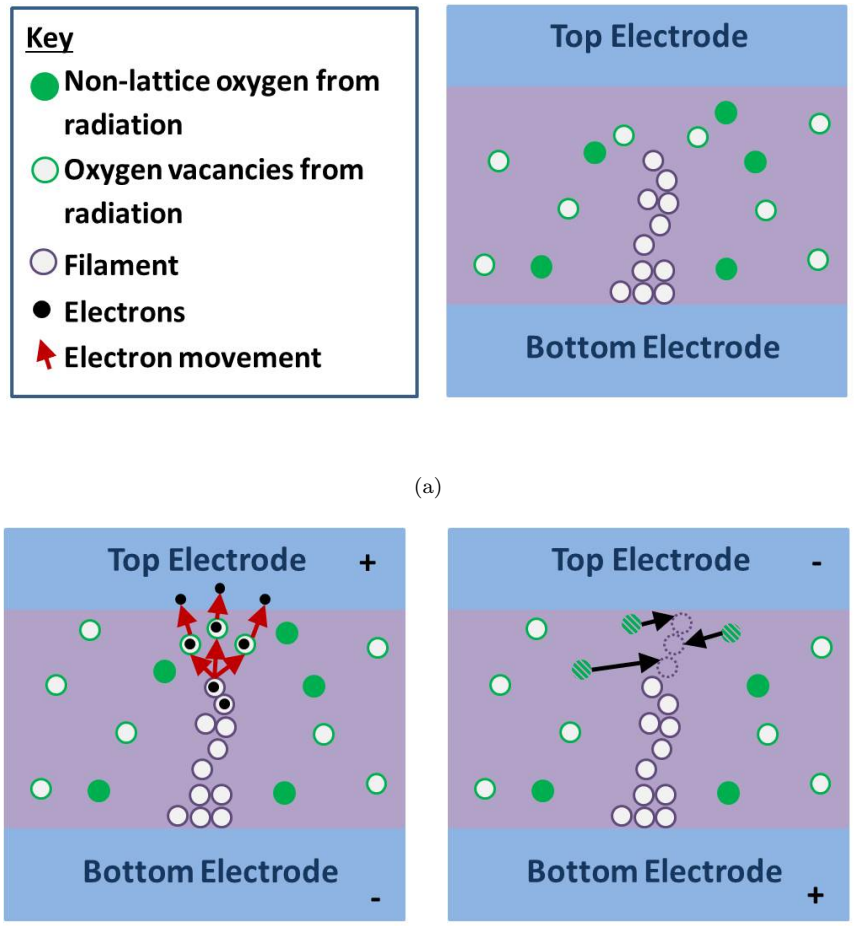


Figure 2.27: Schematic showing physical mechanism of gamma irradiation of a HfO_x RRAM cell, adapted from [97]: (a) Hf-O bonds break resulting in oxygen vacancies and non-lattice oxygen (b) device in HRS with additional path for electrons flipping state to LRS. (c) Device in LRS with non-lattice oxygen recombining with oxygen vacancies in CF resulting in rupture of filament. State is flipped from LRS to HRS.

is proposed, when the device is irradiated, gamma rays break Hf-O bonds, resulting in oxygen vacancies being formed along with non-lattice oxygen in interstitial sites, as seen in Figure 2.27(a). The conductive filament in LRS, or the ruptured filament in HRS, is thought to not be greatly affected by additional oxygen vacancies due to the low numbers of generated vacancies in comparison with the numbers of vacancies in the filament region. It is also thought that the oxygen vacancies are located far from the filament, elsewhere within the bulk oxide. The additional oxygen vacancies that are created by radiation can aid the connection of the filament as seen in Figure 2.27(b). In the LRS, the non-lattice oxygen generated by radiation can migrate towards the conductive filament, aiding the rupturing of the filament, as seen in Figure 2.27(c).

Theories have also been proposed for radiation effects of ECM resistive memory [76].

A theory was proposed for radiation effects in HfO_2 based ECM cells, with metallic filaments. A similar theory to the one used in [97] explaining radiation effects of VCM HfO_x devices was proposed; gamma rays induce oxygen vacancies and oxygen ions causing an increase in leakage current. It also suggests that the gamma induced oxygen vacancies and ions could cause an increase in scattering of metallic ions as these metal ions migrate into the dielectric layer, resulting in an increased set voltage needed to generate an electric field large enough to drive metallic ion migration. In the LRS, it is thought the radiation has little effect on the metallic conducting filament. Theories of radiation effects of other types of non metal-oxide ECM devices have not, to the author's knowledge, been proposed.

2.6 Summary

It is imperative that the radiation effects are understood and controlled if high-k dielectric MOS transistors and resistive memory cells are to be used in nuclear and space environments. In particular, ionizing radiation can cause permanent breakdown and therefore it is of much importance to understand the total ionizing dose effects of said devices.

Dielectric breakdown is thought to occur when internal defects react with generated charge from ionizing radiation. These defects have been studied in depth for silicon dioxide. The three main defects are neutral oxygen vacancies, H_2 located at minimum energy sites and Si-H bonds at the oxide/semiconductor interface. It is believed that when a silicon dioxide MOS capacitor is irradiated by gamma-rays, electron hole pairs are generated in the gate oxide. After some immediate recombination, the remaining electrons are swept out of the oxide due to high mobility. The holes, however, will travel through the oxide, reacting with the pre-radiation defects and become trapped. These form bulk oxide traps which cause a shift in the threshold voltage of the MOS capacitor. The holes that reach the oxide/semi-conductor interface react with Si-H bonds and form interface traps. Interface traps cause a gradient change in the sub-threshold shift on the MOS capacitor.

As scaling occurs for MOS transistors, the silicon dioxide gate oxide is being replaced with high-k dielectrics. As new, thicker, high-k dielectrics are replacing silicon dioxide, the radiation effects of the gate oxide will alter. The radiation mechanism described within silicon dioxide MOS capacitors can be utilised for high-k dielectrics by taking into account the different hole trapping efficiency. This is investigated in Chapter 4.

In a MOS transistor, other oxides exist whereby MOS capacitor structures can be utilised to investigate the radiation effects. Fluorine implantation into smart-cut BOX capacitors were investigated whereby it was proposed this would result in passivation of the interface traps. However the ion implantation resulted in the trapping of positively charged

fluorine and therefore it was concluded if fluorine is used for radiation hardening, to ensure it does not reach the BOX oxide.

BOX and gate oxides can be investigated through MOS capacitor structures. However further investigation into the radiation effects within the STI oxide and the MOS transistor structure is needed. Fluorine was implanted into a MOS transistor and the radiation effects were investigated. Smart-cut SOI wafers were used and therefore care was taken to ensure no fluorine implantation into the BOX occurred. The fluorine implanted MOS transistors showed little degradation when compared to the non fluorine doped transistors, due to passivation of interface traps within the STI. NMOS transistor have been shown to be radiation hard up to 1Mrad(Si) through fluorine doping.

In resistive memory cells, the switching between a high resistance state and a low resistance state is thought to occur due to the formation and dissolution of a conductive filament within the dielectric. Two classes of resistive memory cells exist; electrochemical memory, ECM, and valence change memory, VCM. The conductive filament is formed of metallic ions for ECM or oxygen vacancies for VCM devices. The radiation effects is thought to alter this conducting filament and therefore the switching characteristics of these cells although the exact mechanism is not yet understood.

Increasing understanding and control of radiation effects in dielectrics is imperative to increase the reliability in both high-k MOS transistors and resistive memory cells.

Chapter 3

Development of TiN/HfO_x Stack

High-k dielectrics are being used as silicon dioxide gate oxide replacements in MOS transistors and also utilised as the dielectric layer in resistive memory cells. In particular, hafnium oxide has been reported as the most promising high-k dielectric in a MOS structure, with low leakage currents, negligible charge trapping and good device characteristics [98–100]. Hafnium oxide has also reportedly shown success as a switching dielectric within resistive memory cells with excellent switching characteristics [101–103].

As the CMOS industry moves away from silicon dioxide towards high-k dielectrics, another structural change is required. This change is the top electrode, or gate contact, material. High-k materials must be used in conjunction with metal gates, rather than the previous poly-silicon contacts. Poly-Si cannot be used as a gate material in combination with these high-k dielectrics, due to the resulting high threshold voltages and poor channel mobilities; therefore metal gates are used. From this, it can be seen that a HKMG structure is needed to ensure high capacitive, low leakage CMOS transistors.

Titanium nitride offers a good alternative to metals for a top electrode due to its good electrical conductivity and high melting point, extreme hardness and excellent thermal and chemical stability. The chemical stability can lead to little diffusion into silicon, with potentially small reactivity with oxides as well. This, along with its good electrical properties, makes it a promising alternative to traditional electrodes, such as aluminium.

Development of a TiN/HfO_x stack was conducted. Firstly the development of the hafnium oxide layer will be discussed, followed by the development of the TiN layer.

3.1 HfO_x Development

The hafnium oxide recipe was developed in a three step process; first an initial recipe was run followed by material characterisation, as explained in Section 3.1.1. Following

this, the deposition temperature was investigated, as explained in Section 3.1.2. Finally, a design of experiment (DOE) was performed. This is a systematic way of running a reduced number of runs to obtain a desired output, as explained in Section 3.1.3.

ALD is the primary tool used for depositing HfO_x resulting in uniform, stoichiometric and well controlled layer deposition [104, 105]. ALD is a surface-reaction limited growth method whereby the growth occurs in a cyclic manner. It is a thin-film deposition method which is based on surface reactions where the sources are pulsed into the reaction chamber one at a time, separated by purging steps to evacuate the chamber. The set up of the FlexAl OIPT plasma-assisted ALD used at the University of Southampton is shown in Figure 3.1.

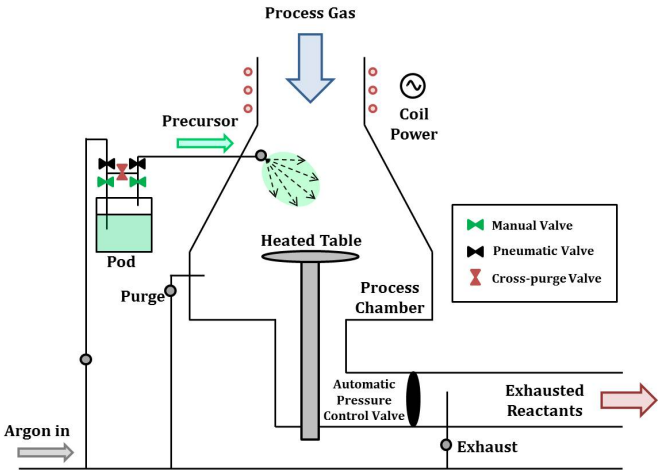


Figure 3.1: FlexAL OIPT ALD tool layout, adapted from [106]

The cycles include exposure of first precursor (AB), purge of reaction chamber, exposure of second precursor (CD) and a final purge of the reaction chamber. Each precursor step saturates the surface of the wafer which then adsorbs the precursor forming a monomolecular layer, resulting in a self-limiting growth method. This method has excellent conformality and uniformity and allows very thin films to be accurately deposited [107]. The reaction can be represented in Equation 3.1 where the two precursors, AB and CD, react with the layers in stages to form the wanted AD film and the BC gas which is purged away. This cycle is repeated until the desired number of layers is achieved.

$$\mathrm{AB\,(adsorbed)} + \mathrm{CD\,(adsorbed)} \Rightarrow \mathrm{AD\,(solid)} + \mathrm{BC\,(gas)} \tag{3.1}$$

An example of the Aluminium Oxide ALD process can be given by Equation 3.2 and is depicted in Figure 3.2. $Al(CH_3)_3$ chemisoprtion occurs on the oxide surface after the plasma releases CH_4 products. -CH_3 groups are removed mainly by O radicals through combustion like reactions [108].

$$\mathrm{Al\,(CH_3)_3\,(TMA) + H_2O \Rightarrow Al_2O_3 + C_xH_y + CO_2} \tag{3.2}$$

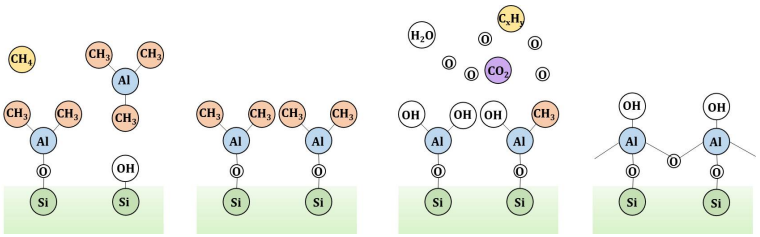


Figure 3.2: ALD mechanism forming aluminium oxide for single layer, adapted from [106].

The two precursors for hafnium oxide consist of the metal precursor and the non-metal precursor. The metal precursor is the chemical tetrakis(ethylmethylamino)hafnium ($Hf[N(CH_3)(C_2H_5]_4$), or TEMAH, and the non-metal precursor can be H_2O, O_3 and O_2 plasma. The chemical reaction for O_3 has been proposed in [105], based upon the reaction between TEMAH and H_2O. Using this, a similar reaction with O_2 plasma is likely.

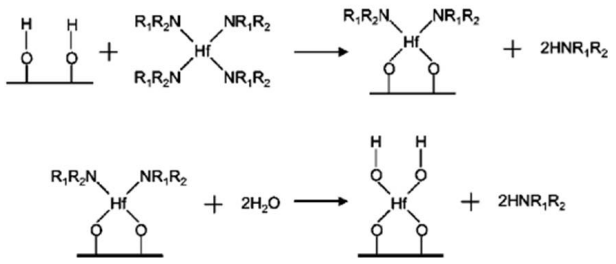
The reaction of TEMAH and H_2O is as follows: HfAA (hafnium alkylamides) react with a surface, eliminating the two alkylamine ligands. Following this, H_2O reacts with the chemisorbed HfAA, removing the other two alkylamine ligands, generating a new surface. The Hf-N bonds in the HfAA molecule are cleaved selectively by H_2O molecules. By products of this reaction include HNEtMe. This is depicted in Figure 3.3(a).

The proposed reaction of TEMAH and O_3 is similar to that of H_2O except with different by products. For this reaction however, the O_3 is thought to cleave most Hf(HNEtMe) molecules at the Hf-N bonds. The HNEtMe molecules are not stable and therefore are oxidized by the O_3 resulting in final by-products of CO_2, H_2O, CH_2O and NO_2/NO. The use of O_3 has resulted in a reduction of H_2O in the samples. This is depicted in Figure 3.3(b).

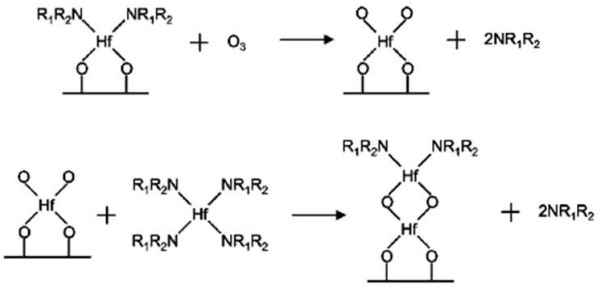
The reaction for TEMAH and O_2 is most likely be similar to the reaction between TEMAH and O_3, although due to limited publications on the TEMAH and O_2 process, the exact chemical reaction is unknown.

3.1.1 HfO$_x$ Basic Material Characterisation

Oxford Instruments plc. provided the cleanroom with a basic recipe for hafnium oxide using the FlexAl OIPT plasma-assisted ALD. The main parameters are shown in Table 3.1. Deposition rate tests were run to verify the working recipe. Ellipsometry was used to measure the thickness of a hafnium oxide layer and the refractive index.



(a)



(b)

Figure 3.3: Proposed TEMAH and (a) H_2O and (b) O_3 reaction mechanisms [105].

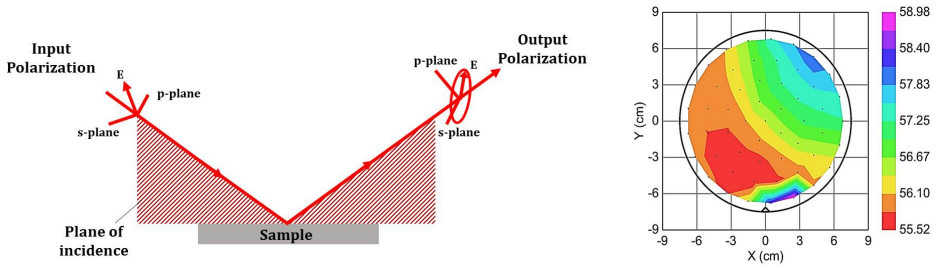
Parameter	Set Values	Parameter	Set Values
$\mathbf{T}_{pod}$ [°C]	70	$\mathbf{t}_{TEMAH}$ [s]	1.5
$\mathbf{T}_{table}$ [°C]	300	$\mathbf{t}_{purge}$ [s]	8
$\mathbf{t}_{plasma}$ [s]	2	$\mathbf{P}_{O_2}$ [mTorr]	80
$\mathbf{P}_{plasma}$ [W]	250		

Table 3.1: Parameters for intial hafnium oxide recipe provided by OIPT.

An ellipsometer is a tool used to measure the thickness and optical properties of films and works by measuring the change in polarization of the light, once the light has been reflected off the sample's surfaces. The state of polarization is characterized by the parameters psi, Ψ, and delta, Δ. Taking the tangent of psi will result in the magnitude of the ratio of reflectivity for the two types of polarized light, and delta is the phase of the light. The setup of the ellipsometer can be seen in Figure 3.4(a).

The data is analysed using an optical model which represents the structure of the sample. The parameters of this model can then be defined and adjusted automatically so that the model provides the closest agreement to the measured data. The accuracy of the model fit to the measured data is given in MSE or mean squared error, where the differences between the measured and fitted data is summed over all the wavelengths the measurement was taken at. An ideal model fit will have an MSE of one [110].

Silicon dioxide, commonly used throughout the CMOS industry, has a very accurate ellipsometry model therefore, as a reference, silicon dioxide wafers were grown through

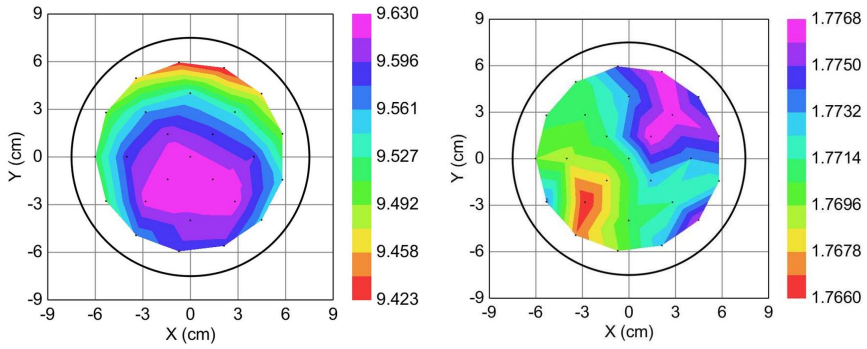


(a) (b)

Figure 3.4: (a) ellipsometry setup, adapted from [109] (b) ellipsometer thickness plots of silicon dioxide in angstroms with a range of 6 percent.

thermal oxidation using a Tempress Clean Furnace Stack, with a dry oxidation recipe at 850 °C. Due to the well-defined model for thermal silicon dioxide, the thickness was fitted whilst holding the optical constants defined. A 2D X-Y plot showing silicon dioxide thickness is shown in Figure 3.4(b) with a thickness of 5.6 nm with a range of 6 percent.

Before developing the hafnium oxide layers, a previously developed aluminium oxide recipe was run in order to verify a successful ellipsometer fit with a known high-k layer. The aluminium oxide layers were deposited using a precursor known as TMAl, triemthylaluminium, along with O_2 plasma. A run enabling verification of the deposition rate was undertaken and measured using the ellipsometer, as shown in Figure 3.5.



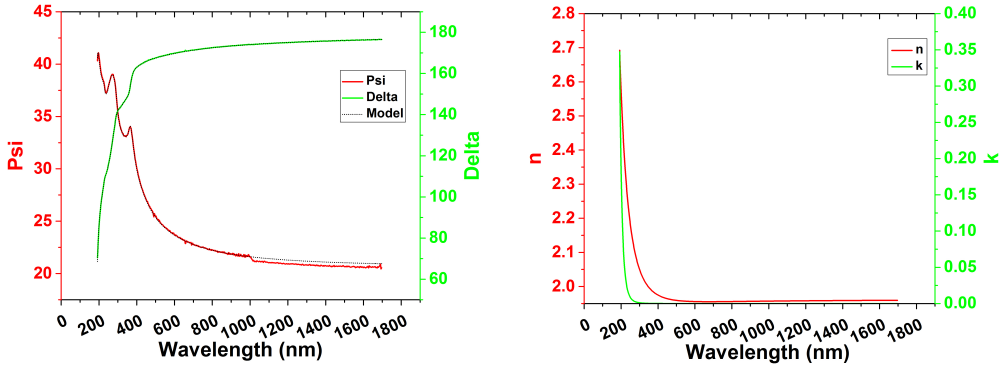
(a) (b)

Figure 3.5: X-Y plots measured by ellipsometry for 90 cycles of aluminium oxide fitted using a Cauchy model showing (a) thickness and (b) refractive index at 632.8 nm.

A Cauchy model was fitted with a good fit with an MSE of around 5, showing a deposition rate of ∼0.1 nm/cycle with a refractive index of ∼1.77, in agreement with literature. Cauchy model allows the film thickness and refractive index, n, to be determined for transparent materials. For Al_2O_3, a molar mass of 101.69 g/mol and a mass density of 3 g/cm^3 can be used to calculate a number density of 1.78x10^{22} Al_2O_3 units/cm^3. This results in a monolayer thickness calculated at $n^{-1/3}$=0.38 nm [111]. This is more than the growth rate of 0.1 nm/cycle and shows that over 3 cycles is needed to achieve one

monolayer. This deposition rate is also slightly higher than some reported atomic layer deposition rates [112, 113]. This can be attributed to the use of an O_2 plasma where an increase in deposition rate of 50-100 percent has previously been reported when O_2 plasma is used. It can be concluded optimised atomic layer deposition growth is achieved giving an efficient deposition rate. A uniformity of 2 percent is achieved for thickness and less than 1 percent for refractive index.

Following the successful fit of the aluminium oxide, hafnium oxide was then measured using the Cauchy model as well. Again a good fit was found with an MSE of around 5. The measured ellipsometer psi and delta are shown in Figure 3.6 with a close fit to the model. The resultant optical constants, refractive index n and transparency k, are also shown in Figure 3.6. The optical constants are in agreement with previously deposited hafnium oxide thin films [114–116].



(a) (b)

Figure 3.6: Ellipsometry measured data fitted with Cauchy model showing (a) psi and delta versus wavelength and (b) optical functions versus wavelength.

The thickness and refractive index were plotted on an X-Y scale, using the same Cauchy fit and can be seen in Figure 3.7. A deposition rate of 0.16 nm/cycle was calculated, with a refractive index of 1.96 at 632.8 nm. The variation in uniformity in thickness seen across the wafer is an acceptable amount and will result in an array of devices with varying oxide thickness of 14 percent, which can be utilised in electrical characterisation. The uniformity pattern of increasing thickness laterally across the wafer indicates it is caused by the TEMAH source injection due to the layout of the tool i.e. the TEMAH source is injected in from the side of the chamber (as shown in Figure 3.1) whereas the O_2 plasma, which comes from the top of the chamber, is positioned over the centre of the wafer.

The deposition rate achieved using this recipe can be compared to the thickness of one monolayer of ideal stoichiometric hafnium oxide to ensure this deposition is within the atomic layer deposition growth window. The monolayer thickness can be calculated by using the mass density and the molar mass of the molecule/atom [111]. For HfO_2, a

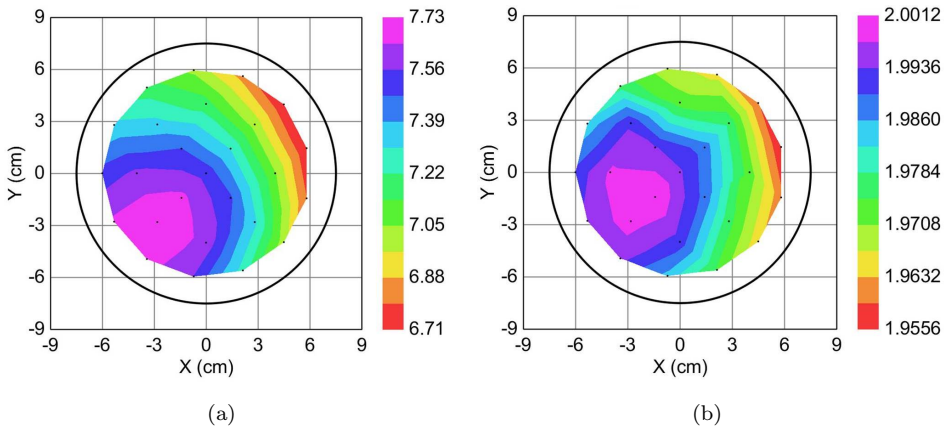


Figure 3.7: Ellipsometry X-Y plots for (a) thickness and (b) refractive index for OIPT initial recipe for hafnium oxide using a Cauchy model.

molar mass of 210.49 g/mol and a mass density of 9.69 g/cm^3 was used [117], giving a number density of 2.77x10^{22} HfO_2 units/cm^3. The monolayer thickness is equal to the inverse cube root of the number density and is calculated to be n$^{-1/3}$=0.33 nm. Again, as in the aluminium oxide case, the monolayer thickness exceeds the growth rate of 0.16 nm/cycle and shows that around 2 cycles is needed to achieve one monolayer. This efficient deposition rate is similar to that of aluminium oxide. This again can be attributed to the use of O_2 plasma, indicating one of the advantages of plasma assisted ALD over thermal ALD.

In order to check the elemental composition, X-ray photoelectron spectroscopy (XPS) is used to detect the elements within the deposited layer. XPS is a surface analysis technique used to identify elements, determine chemical state and quantify an element. It works by firing X-rays at the sample and analysing the energies of emitted photoelectrons as shown in Figure 3.8.

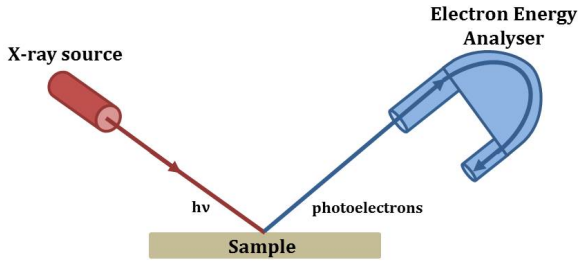


Figure 3.8: XPS setup

Low energy X-rays are produced by firing electrons from an electron gun onto an aluminium target. These bombarding electrons, if the energy is sufficiently high enough, knock out inner shelled electrons within the aluminium target. Electrons within the higher energy states in the aluminium then drop down to fill the vacancy. As this occurs, X-ray's are released with specific energies determined by the electron energy levels

within the target. For aluminium, the X-rays produced are referred to as K α and have energies of 1486 eV. The X-rays are focused onto the sample. As the X-rays hit the sample surface, the atom will be ionized and the inner shell electrons within the sample will be emitted. This is given by Equation 3.3.

$$A + h\nu \rightarrow A^* + e^- \tag{3.3}$$

Only photoelectrons at the outer surface of the sample will then be emitted from the sample as the electrons further down inside the sample will be reabsorbed. This results in XPS being surface sensitive only. Conservation of energy requires that Equation 3.4 is maintained.

$$E(A) + h\nu \equiv E(A^*) + E(e^-) \tag{3.4}$$

The electrons energy, E(e^-), is in the form of kinetic energy, KE. It is the kinetic energy of the photoelectron that is measured, as shown in Equation 3.5.

$$KE = h\nu - (E(A^*) - E(A)) = h\nu - BE \tag{3.5}$$

The latter term in Equation 3.5 refers to the difference in energy from the neutral atom before the X-ray and the ionized atom. This is known as the binding energy, BE, of the electron. Each atom has orbital electrons with certain orbital binding energies, depending on the element the atom is composed of. As the X-ray energy is known, measuring the kinetic energy of an emitted photoelectron will enable the binding energy to be calculated, enabling element of the atom it came from to be determined.

The emitted photoelectrons are focused down by the transfer lens into the electron energy analyser and here the kinetic energy of the emitted photoelectrons is used to determine their energy distribution. Two curved plates are used, of opposite charge creating a potential difference between the plates, putting the photoelectrons into a small orbit in an electrostatic field. At the end of this orbit is a detector as seen in Figure 3.8. By setting the potential difference between these plates, only electrons of certain energies will successfully reach the detector unobstructed. Through sweeping the potential difference, and measuring incoming electron energies, an XPS spectrum is formed. The peaks of the spectrum correspond to the binding energy of the photoelectrons and therefore quantitative analysis can be performed to identify the element.

XPS can also identify chemical bonding information. Atoms that are bound to other atoms result in slightly shifted binding energies of the emitted photoelectrons. These shifts in energy can be measured by the XPS and analysed to determine the compounds of the sample [118]. Additional features of the XPS at the University of Southampton

include an argon etch gun used to etch downwards allowing the elements deeper in the layer to be examined. An electron flood gun can also be used for the control of the surface charging for analysing insulating surfaces.

To investigate the elemental composition of the hafnium oxide layers, HfO$_x$/Si was measured using the argon etch gun between measurements to obtain information about the hafnium oxide layers below the surface. For each measurement, a spectrum showing the different peaks from the different energies of the electrons, and therefore different elements, is plotted. All of the plots from each measurement, taken as the etching continues, can be brought together and analysed so that the atomic concentration of each element is plotted against the time the measurements were taken. This time of measurement will be related to the relative depth, where the measurement taken at time 0 s will be the values of the surface elements, and the measurement taken at a later time will be values of elements found deeper in the layer with 100 s roughly corresponding to the full thickness of hafnium oxide layer of 10 nm.

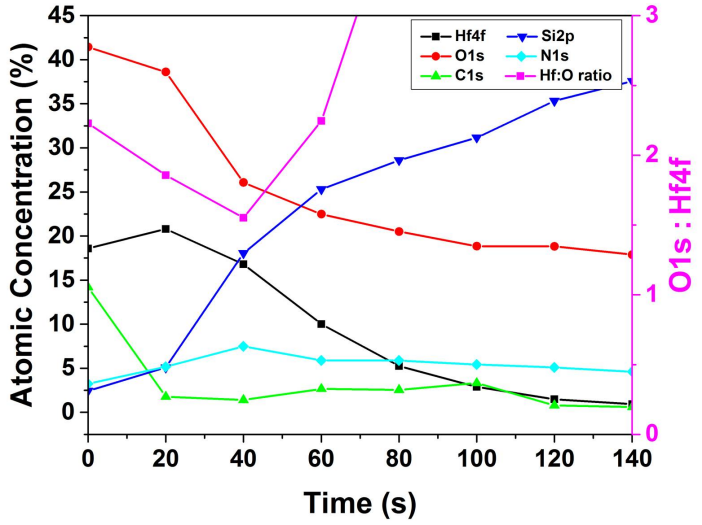


Figure 3.9: Atomic Concentration of Elements throughout the HfO$_2$ layer deposited by ALD. 0 s indicates surface measurement. Etch steps were performed after each measurement with increasing etch step indicated by increased time on x axis.

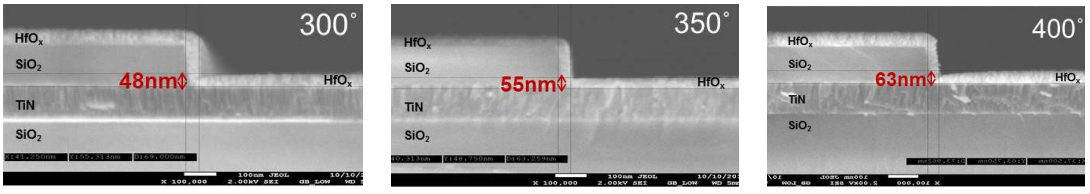
The result for this can be seen in Figure 3.9 where the elements of interest are the oxygen, O1s, the hafnium, Hf4f and the silicon, Si2p. Carbon and nitrogen are surface containments and can be discarded. The oxygen and hafnium together will be the hafnium oxide and the silicon will be that of the silicon wafer. The results show the hafnium and oxide ratio is close to two for the first four etch steps. After this the hafnium levels reduce to background noise levels, indicating at this stage, the measurements are unreliable. This verifies XPS is a surface sensitive technique whereby the first four steps indicate that the deposited material is close to stoichiometric hafnium oxide.

3.1.2 The Effect of ALD Temperature

The second development of HfO$_x$ investigates the table temperature effects. The remaining recipe parameters were kept the same as the initial HfO$_x$ recipe, as listed in Table 3.1, with one change in the system; a new TEMAH supply was ordered and fitted due to the last TEMAH source running out. Previous publications suggested oxygen concentration of the deposited layer in ALD is affected when the temperature of the sample holder is altered [119, 120]. Three different temperatures, 300 °C, 350 °C and 400 °C, were used to control the stoichiometry and crystal structures and investigate its effect on resistive switching.

Scanning electron microscopy (SEM) was conducted using a JEOL JSM 7500F field emitting scanning electron microscope (FESEM) to measure the thickness of all three layers before the top electrode was deposited. SEM uses a beam of high energy electrons that are focused onto a solid specimen, resulting in electron-sample interactions. These interactions give information about the sample that the electrons are interacting with. There are many types of electron-sample interactions, including secondary electrons, backscattered electrons and diffracted backscattered electrons. Photons, visible light and heat can also be generated. Secondary and backscattered electrons are what allow an image to be taken, whereby secondary electrons give the morphology and topography of the sample, and backscattered electrons give different contrast from different compositions, due to different types of materials in a sample.

The cross section for HfOx layers deposited at the three temperatures can be seen in Figure 3.10. The thickness of the hafnium oxide layers are 48nm, 50nm and 63nm for the 300 °C, 350 °C and 400 °C respectively. Following SEM, XRD was performed.



(a) (b) (c)

Figure 3.10: SEM images of memory cell structure with hafnium oxide deposition at ALD temperature of (a) 300 °C (b) 350 °C and (c) 400 °C.

To determine the crystal structure of the hafnium oxide films, X-ray diffraction (XRD) is used. XRD can be used to study crystal structures and atomic spacing from constructive interference of X-ray with similar wavelengths to the spacing of the crystal lattice planes. The X-rays are produced through electron bombardment of typically Cu targets, are filtered into one specific wavelength, and then directed towards the sample to be measured. When Bragg's Law is met, as shown in Equation 3.6, constructive interference occurs, whereby n is an integer, λ is the wavelength of the incoming X-ray,

θ is the scattering angle and the distance, d, is given by the distance between atomic layers. This is de-pictured in Figure 3.11(a). The wavelength of the X-ray is then altered, through a range of 2θ producing a diffraction pattern for all interactions with the entire lattice. The crystal structure will determine the diffraction pattern and can be used to identify the crystal structure of an unknown material, calculate the average spacing between layers of atoms, d, and determine the orientation of a single crystal or grain [121].

$$n\lambda = 2dsin\theta \tag{3.6}$$

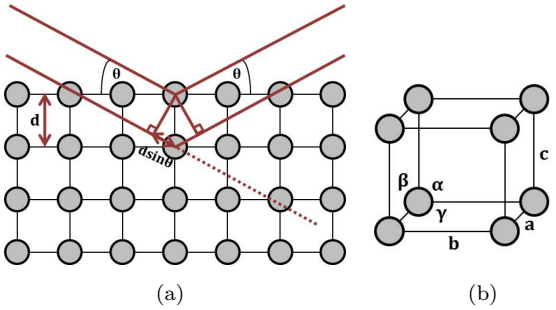


Figure 3.11: (a) Diffraction of X-ray in a Crystal according to Bragg's Law (b) Unit Cell with spacing and angles between atoms defined

Crystal Structure	Unit Cell Dimensions
Cubic	a=b=c, α=β=γ=90 °
Tetragonal	a=b≠c, α=β=γ=90 °
Hexagonal	a=b≠c, α=β=90°,γ=120 °
Monoclinic	a≠b≠c, α=γ=90°,β ≠90 °

Table 3.2: Crystal phase structures defined by distance and angles between atoms in a unit cell.

Crystal structures can be defined by a unit cell whereby the unit cell show the repeated arrangement of atom/s, spaced distance d apart. The unit cell is defined by three lengths, a, b, c, and three angles, α, β, γ as shown in Figure 3.11(b). These values are used to define the crystal structure or phase as given by Table 3.2.

XRD patterns were recorded for HfO$_x$ using grazing incidence $\Theta 1 = 3$ ° using a Bruker D8 with general area detector diffraction system (GADDs) (Cu-K$_{\alpha 1}$) for phase identification. Figure 3.12 shows the XRD pattern for all three deposition temperatures whereby the hafnium oxide is cubic for 300 °C and 350 °C and monoclinic for 400 °C.

XPS was conducted in order to calculate the stoichiometries of all deposited hafnium oxide layers using a Thermo Scientific Theta Probe XPS system. Hf 4f, O 1s and C 1s peak energies were measured whereby the Hf 4f core level spectra and the O 1s core level spectra is shown in Figure 3.13. Previous investigations reported fully oxidized

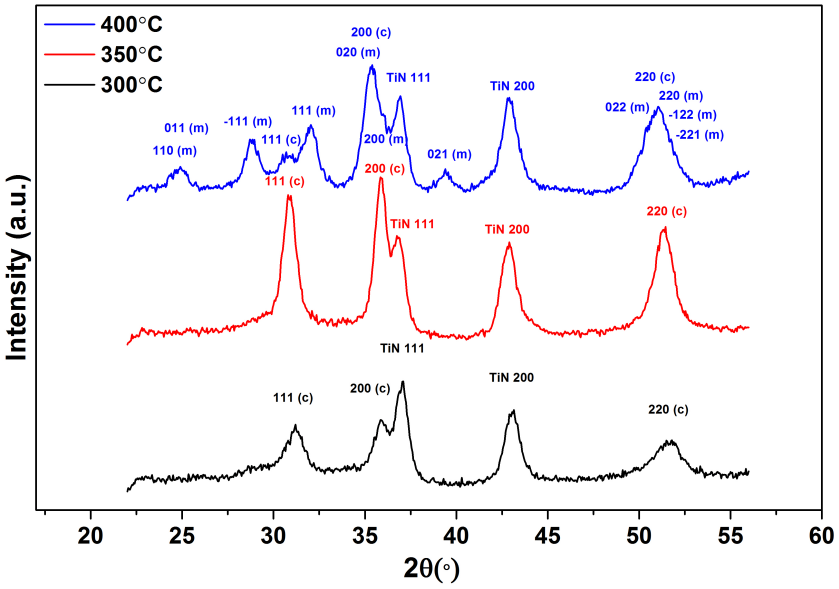
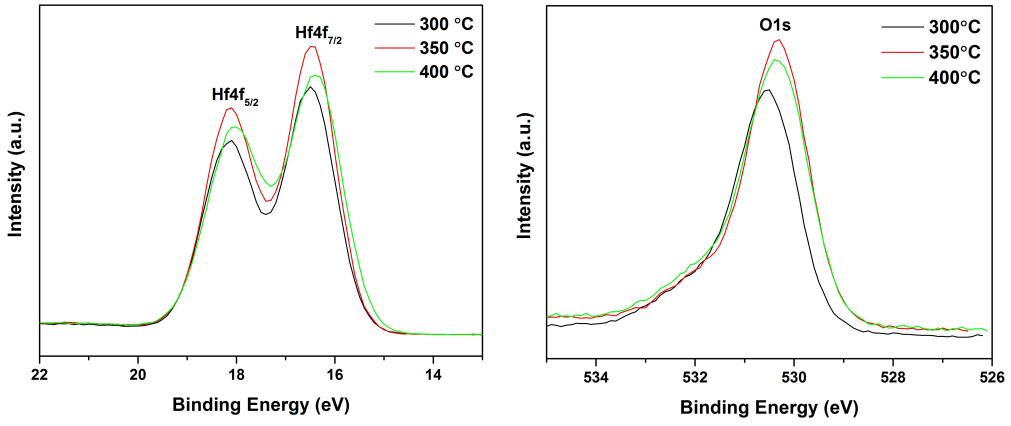


Figure 3.12: XRD pattern for HfO$_x$ at 300 °C, 350 °C and 400 °C. The peaks belonging to HfO$_x$ cubic structures are identified as (c) and monoclinic as (m). TiN peaks are present due to the TiN below.

metal oxide has a lower binding energy than a sub-stoichiometric metal oxide [122]. The shifting of the O 1s peak towards higher binding energies, as seen for the 300 °C in Figure 3.13(b) therefore indicates a lower oxygen concentration. These peaks were fitted using Thermo Avantage software.



(a) (b)

Figure 3.13: XPS results showing core level spectra of (a) Hf 4f and (b) O 1s for three different deposition temperatures of HfO$_x$.

The ratio of hafnium to oxygen is presented in Table 3.3 confirming the oxygen deficiency in hafnium oxide deposited at 300 °C, along with the crystal structures for each temperature. The material characterisation performed indicates the table temperature effects the crystal structure and the oxygen concentration.

ALD Deposition Temperature (°C)	300	350	400
HfO$_x$, x=	1.78±0.05	1.99±0.05	1.95±0.05
Crystal Structure	cubic	cubic	monoclinic

Table 3.3: Hf:O ratio as determined by XPS as a function of atomic layer deposition temperature.

3.1.3 HfO$_x$ Design of Experiment

The ALD tool suffered multiple breakdowns and severe technical errors. This spanned a period of over a year and included faulty automatic pressure control (APC) valves, a broken and replaced chamber vacuum pump, new in-aligned shielding and faults related to the load lock. Following alteration and changes of pumps, shielding and the yearly check, it was decided a re-optimisation of the hafnium oxide recipe was needed. This was done through DOE and is explained in Section 3.1.3.

A DOE was set-up to achieve hafnium oxide deposition with a hafnium to oxide ratio close to 2 (stoichiometric) within the atomic layer deposition growth window. A DOE can be used to determine the effects of many process inputs on the output result. Design of experiments allow for the screening of parameters i.e. identifying parameters that have negligible effects on the wanted outcome allowing the main, larger effect factors to be determined. The effects of the variables of an experiment can be defined as main effects (independent of one another) and interactions (effect of one variable dependent on another). If there are many variables however, assuming the interactions are negligible will allow the number of runs in the DOE to be reduced significantly. For example, 8 variables with 8 variable/factor interactions can result in 256 runs to determine all the interaction and main effects [123].

Seven input parameters were identified for HfO$_x$ including the temperature of the table, the time for the plasma step, the plasma power, the time for the TEMAH dose set-up, the time for the TEMAH purge step, the number of cycles and the oxygen flow pressure during the oxygen plasma steps. Two main outcomes were chosen being stoichiometry and the thickness of the layers. Ellipsometry was used after each run to identify the thickness and refractive index of the layers. The stoichiometry of the layers is measured using XPS.

A Plackett-Burmann experimental design uses a significantly reduced number of runs allowing a high number of variables/factors to be examined, but assumes there are no interaction effects. For each factors, it assumes two levels of minimum and maximum. Therefore a Plackett-Burmann is used for two-level multi-factor experiments allowing for economical detection of large main effects. Due to the cost of the TEMAH source, time and personnel limits, and the 7 variables in the ALD process, a Plackett-Burmann design was chosen. A centre point was added allowing for the curvature in design space

to be identified and it was repeated 3 times allowing for the variability in the same runs to be identified.

Run	**T**$_{table}$ **[°C]**	**t**$_{plasma}$ **[s]**	**P**$_{plasma}$ **[W]**	**t**$_{TEMAH}$ **[s]**	**t**$_{purge}$ **[s]**	**cycles**	**P**$_{O_2}$ **[mTorr]**
G022	400	10	250	2	2	100	15
G023	400	2	250	0.2	8	200	80
G019	400	10	250	2	8	100	80
G018	400	2	600	0.2	2	100	80
G021	400	10	600	0.2	8	200	15
G020	400	2	600	2	2	200	15
G024	335	6	425	1.1	5	150	47.5
G025	335	6	425	1.1	5	150	47.5
G026	335	6	425	1.1	5	150	47.5
G027	250	2	600	2	8	100	80
G028	250	2	250	0.2	2	100	15
G029	250	10	600	2	2	200	80
G030	250	2	250	2	8	200	15
G031	250	10	250	0.2	2	200	80
G032	250	10	600	0.2	8	100	15
G033	400	10	600	0.2	8	200	15

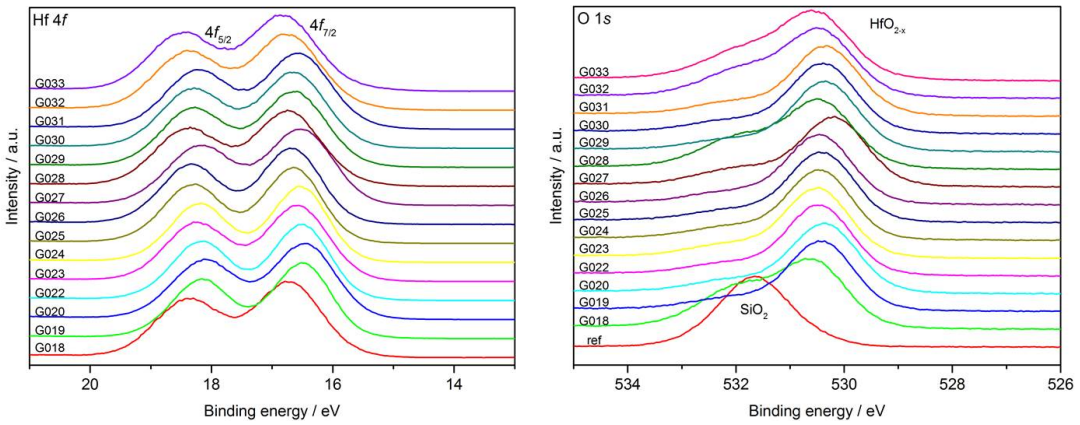
Table 3.4: Plackett-Burmann design with 3-repeat centre point.

The Plackett-Burmann design for the HfO$_x$ DOE is given in Table 3.4. These runs were conducted on silicon pieces (around 1x1cm) due to constraints on full-wafer run costs. The thickness and refractive index, using a Cauchy fit, for all runs are shown in Table 3.5. XPS was used to determine the Hf:O ratio. Figure 3.14(b) and Figure 3.14 show the core level spectra for hafnium and oxygen respectively whilst Figure 3.15 shows the Hf:O ratio extracted from fitting the spectra. The ideal ratio for stoichiometric hafnium oxide is 2.

run	**n(632.8nm)**	**t**$_{HfO_x}$ **[nm]**	**run**	**n(632.8nm)**	**t**$_{HfO_x}$ **[nm]**
G018	2.02	2.2	G026	2.03	35.0
G019	2.04	31.7	G027	2.01	12.4
G020	2.02	7.4	G028	2.03	2.4
G021	2.00	1.8	G029	2.01	10.0
G022	2.01	33.0	G030	2.01	14.7
G023	2.03	5.0	G031	2.02	5.2
G024	2.03	37.1	G032	2.02	2.8
G025	2.03	35.4	G033	2.08	2.8

Table 3.5: Plackett-Burmann design with 3-repeat centre point

Run G021 is not included in XPS results as no hafnium peaks were detected and therefore will no longer be included in DOE analysis. This run is the thinnest deposited layer from ellipsometry results which could explain the lack of hafnium measured. Runs G018, G028, G032 and G033 all show the presence of a secondary peak in the O 1s spectra. This peak aligns in binding energy with silicon dioxide, as shown by reference peak in Figure 3.14.



(a) (b)

Figure 3.14: XPS results showing core level spectra of (a) Hf 4f and (b) O 1s for multiple DOE runs of HfO_x.

These four runs were measured t_{HfO_x} <3 nm by ellipsometry and therefore suggests the silicon dioxide peaks detected originate from XPS measurements of the native silicon dioxide layer situated below the very thin hafnium oxide layers. Fully oxidized metal oxides have lower binding energies than sub-stoichiometric metal oxides. Therefore, the shift to higher peak energies seen in O 1s for G027 indicates less a lower oxygen concentration. This is confirmed by the low Hf:O as seen in Figure 3.15 as determined by fitting the peaks.

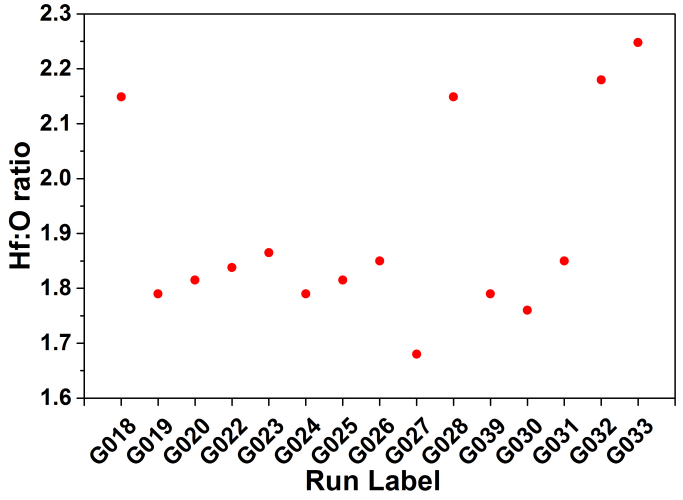
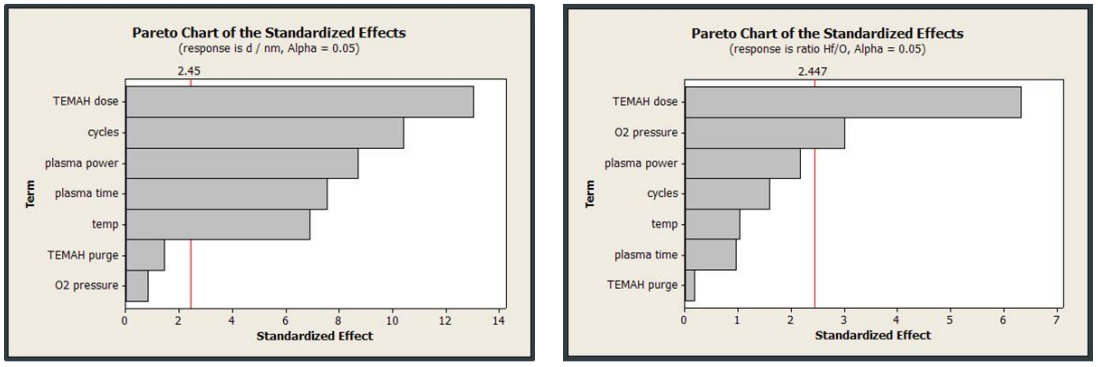


Figure 3.15: Hf:O ratio determined from fitting of XPS core level spectra of Hf 4f and O 1s.

The thickness and Hf:O ratio results were submitted into MINITAB software allowing the main effects to be calculated. This can be displayed in a Pareto chart whereby the effects of each variable is plotted against a standardized effect. The larger the standardized effect, the more this variable will affect the outcome of the process. A typical alpha level of 0.05 was chosen. This means there is a 95 percent chance the result seen is due to the

process and not by chance. The red line indicates a reference line. Any effect that has a larger standardized effect than this shows an important variable. The Pareto charts for thickness and Hf:O ratio are shown in Figure 3.16(a) and Figure 3.16(b) respectively. These graphs show the thickness of the hafnium oxide film is determined mostly by the TEMAH dose time, followed by the number of cycles. The plasma power, plasma time and temperature are also found to be contributing factors on the thickness. The TEMAH purge and pressure during the O_2 steps show little effect on the thickness. The Pareto chart for the Hf:O value shows only two main effects; TEMAH dose time and pressure during the O_2 steps. The remaining variables show little effect on the ratio.



(a) (b)

Figure 3.16: Pareto chart showing main effects for (a) thickness and (b) Hf:O of hafnium oxide via ALD.

After this initial screening run, optimisation through additional runs is performed. The Pareto charts allow the main effects to be determined but do not give information on the ideal variable values. For this, main effect charts can be created and are shown in Figure 3.17 for Hf:O. A steeper gradient of the black lines indicate this variable has a greater effect on the outcome with centre points showing the shape of the change. The thickness of the layer is less important than the Hf:O, as the thickness can be altered by changing the number of cycles, after the Hf:O value has been optimized. Therefore the Hf:O main effects plot results can be used to determine the optimisation run.

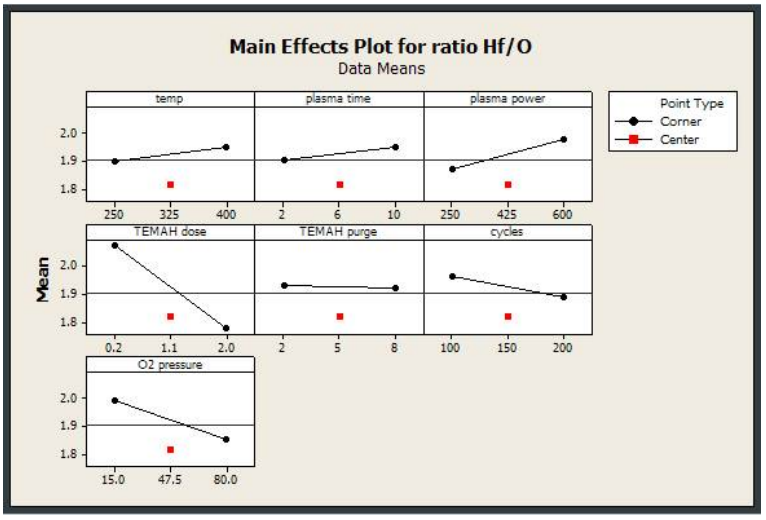


Figure 3.17: Main effect plot for thickness for ALD of hafnium oxide with centre points. Large gradients indicate the parameter has a large effect on the outcome. The centre points allow any curvature in response to be seen, allowing non-linear relations to be determined.

A summary of the chosen parameters for the first optimisation run is shown in Table 3.6, labelled as 'Run 1'. The Pareto charts indicate TEMAH purge time, plasma time, temperature and cycles all have negligible effect on Hf:O ratio. This is verified by the shallow gradients seen in the main effects plot. Therefore the minimum value for TEMAH purge time and plasma time were chosen as optimum to ensure shorter processing time. Due to a very short 2 s plasma time, a higher pressure of 80 mTorr during O_2 and plasma steps was chosen for optimisation runs to ensure enough plasma was being created. Lower temperature runs are more economical and due to the negligible effect of temperature on the Hf:O values, 250 °C was chosen as optimum. 185 cycles were chosen due to the negligible effect on ratio and to ensure thicker layers were deposited, allowing for optimum material characterisation. The plasma power, although slightly below, lies close to the reference line in the Pareto chart and therefore, looking at the main effects plot, 600 W was chosen. The main effect plot for the most important effect for Hf:O ratio, shows a reduction and levelling off of Hf:O ratio with increasing TEMAH time. This indicates a saturation level is reached for hafnium in the layer from the TEMAH source at above 1.1 s. Due to the self-limiting growth of ALD, any runs with TEMAH dose step above 1.1 s will result in excess source being wasted and purged away. Therefore 0.8 s was chosen for the next optimum run.

Previously, wafer pieces were used for the DOE to reduce cost. For optimisation runs, whole silicon 6 inch wafers were used allowing the uniformity to be studied via ellipsometry. The result from the first optimisation run, 'Run 1', shows a non-uniform thickness distribution across the wafer in a concentric circle pattern, with a variation of ∼64 percent and is shown in Figure 3.18(a) along with refractive index variation of ∼9 percent.

Parameter	**Run 1**	**Run 2**	**Run 3**	**Run 4**	**Optimised Run**
T$_{table}$ [°C]	250	250	250	250	250
t$_{plasma}$ [s]	2	2	2	2	2
P$_{plasma}$ [W]	600	600	425	425	600
t$_{TEMAH}$ [s]	0.8	0.8	0.8	2	1.75
t$_{purge}$ [s]	2	2	2	8	8
cycles	500	185	185	100	100
P$_{O_2}$ [mTorr]	80	15	80	15	80
t$_{HfO_x}$ **range (percent)**	64	70	50	6	4
n range (percent)	9	7	13	1	1

Table 3.6: Parameters for Optimisation Runs for hafnium oxide development.

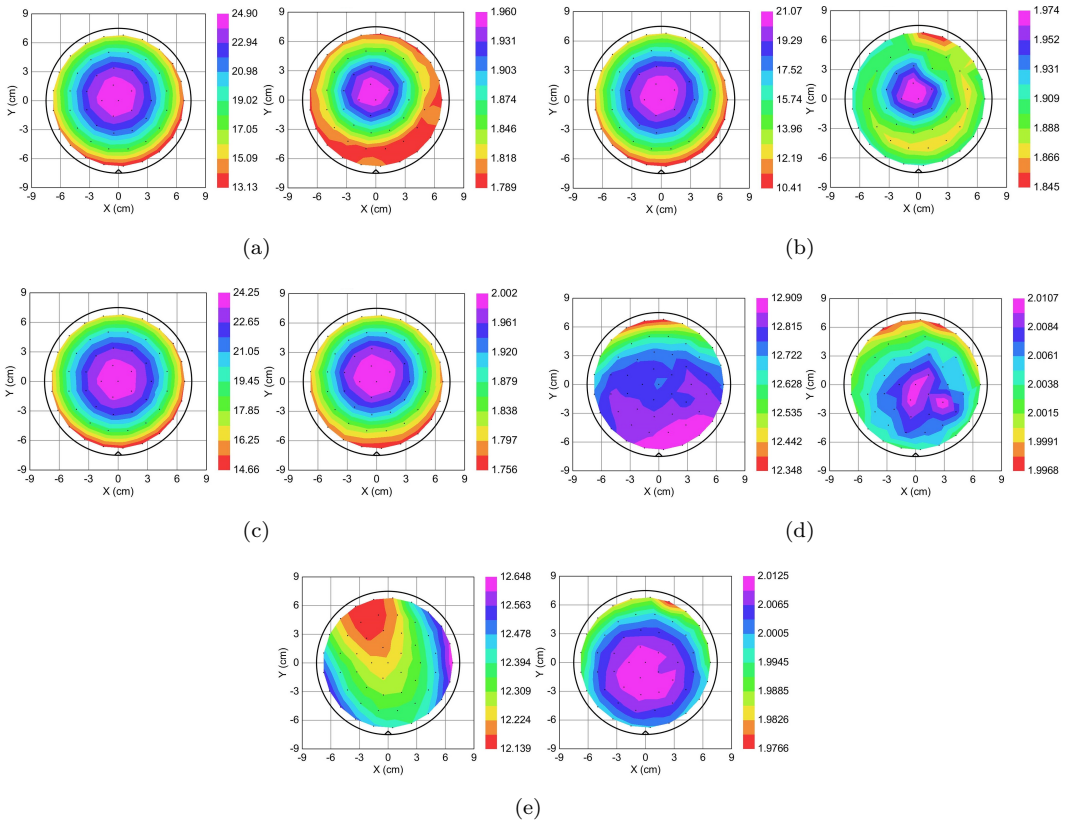
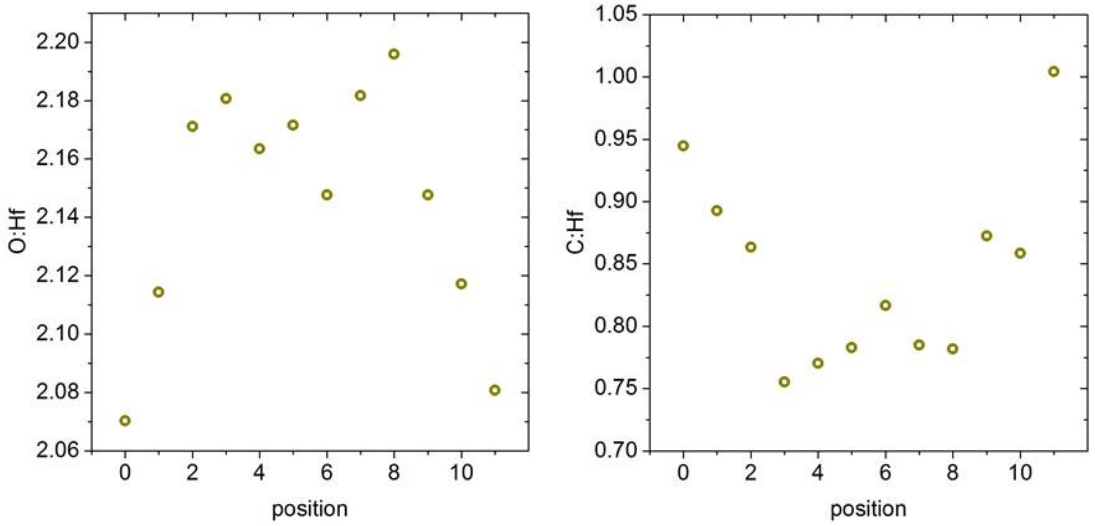


Figure 3.18: X-Y ellipsometry plot showing thickness (nm) on the LHS and and refractive index variation on the RHS across silicon wafer for hafnium oxide, for parameters listed in Table 3.6 as (a) 'Run 1' (b) 'Run 2' (c) 'Run 3'(d) 'Run 4' (e) final 'Optimised Run'.

Due to the geometry of the ALD chamber, the concentric circle pattern of the uniformity suggests this effect is from the oxygen plasma. The oxygen plasma is directed from above the wafer, down onto the centre of the wafer, as shown in Figure 3.1. To investigate this further, XPS was conducted across the wafer at multiple points along the X=0 axis, allowing the variation in oxygen and carbon (TEMAH) to be measured. This is shown in Figure 3.19. Position 0 and 10 refer to the out edges of the wafer, whilst 5 is the

centre midpoint of the wafer. The ratios follow the same trend as the refractive index and thickness variation measured by ellipsometry. The centre of the wafer is thicker with more oxygen present and less carbon (reduced amount of precursor). The edges are thinner, with less oxygen and more carbon. Reduced oxygen and reduced thickness at the edges of the wafer could be caused by the reaction of radicals with any source deposited on the walls of the chamber, resulting in a drop off in concentration gradient towards the edges of the wafer. Also this could explain the increased carbon seen at the edges due to un-reacted TEMAH source still present. An investigation into the oxygen plasma conditions was conducted to reduce the large variation across the wafer.



(a) (b)

Figure 3.19: Elemental ratios of (a) O:Hf and (b) C:Hf, determined from XPS across a 6 inch Si wafer at the X=0 axis for optimisation 'Run 1' described in Table 3.6.

Optimisation 'Run 2' and 'Run 3' investigated the alterations of oxygen plasma conditions; the plasma power was reduced from 600 W to 425 W in run 2, and the oxygen pressure was reduced from 80 mT to 15 mT in run 3. The full parameter values for these runs are shown in Table 3.6. Run 2, with reduced plasma power, resulted in a uniformity of ∼70 percent for thickness and ∼7 percent for refractive index. Run 3, with reduced oxygen pressure, resulted in a uniformity of ∼50 percent for thickness and ∼13 percent for refractive index. This is shown in Figure 3.18(b) and Figure 3.18(c) for Run 2 and Run 3 respectively, confirming altering the plasma power and oxygen pressure does not result in significantly improved uniformity.

As the pareto chart suggested, the most influential parameter for ratio was the TEMAH dose. Therefore the next run, optimisation 'Run 4' had an increased TEMAH dose time, from 0.8 s to 1 s, to see if the uniformity would improve. An increased TEMAH dose should ensure saturation over the whole wafer. The purge time for TEMAH was also increased from 2 s to 8 s to ensure reduction of reactions with oxygen radicals with the

wall of the chamber by reducing source on the walls. The full set of parameters for the next run are listed as 'Run 4' inTable 3.6. The ellipsometry results are shown in Figure 3.18(d). The uniformity showed significant improvement with a uniformity of ∼4 percent for thickness and ∼1 percent for refractive index.

For the previous runs, at lower TEMAH dose rates, it appears the layers were heavily affected by the oxygen plasma or table gradient of temperature from the table beneath. The concentric circle pattern is no longer visible. Instead, the pattern of thickness uniformity occurs as a gradient across the wafer, indicating the variation is caused from the TEMAH source direction. For this run, at higher TEMAH dose rates, this sensitivity to the plasma/temperature has been removed, and the main factor determining uniformity is the TEMAH source. This indicates ALD growth was not attained at lower TEMAH doses. It appears that an increased TEMAH dose time results in a much more reliable deposition of hafnium oxide, within the ALD growth window. This agrees with the pareto chart, indicating TEMAH dose is the most important parameter for this ALD growth.

In order to verify that the oxygen plasma conditions no longer had a main effect on the uniformity, with an increased TEMAH dose, 'Run 4' was repeated but with 80 mTorr pressure and 600 W. No change was seen in uniformity from the previous run, and no concentric pattern was visible. This verifies the increase TEMAH dose time results in a more stable growth window, with little effect from other parameters.

The final set of runs varied the TEMAH dose from 1 s to 2 s in 0.25 s steps, with the remaining parameters as described in the 'Optimised Run' in Table 3.6. A TEMAH dose of 1.75 s resulted in the best uniformity of ∼4 percent for thickness and ∼1 percent for refractive index as shown in Figure 3.18(e). This wafer was diced into 5 pieces, one in the centre and one at north, south, east and west orientation. These parts were measured using XPS and the ratio of each part is shown in Table 3.7. The ratio can be seen to be consistent across the wafer, with small deviations within an acceptable range.

Position on Wafer	**Hf:O**
North	1.90
Centre	1.89
South	1.90
East	1.90
West	1.90

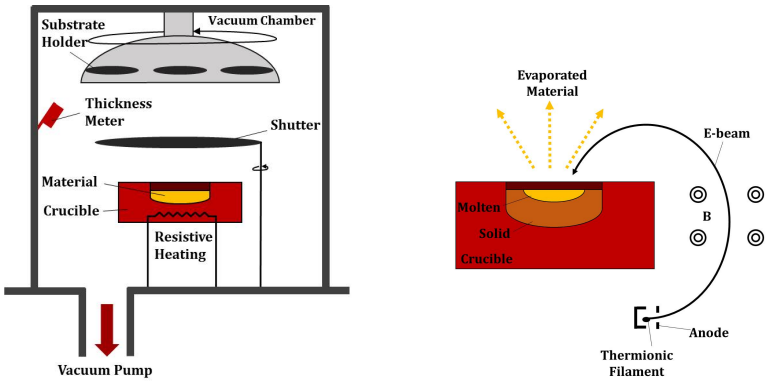
Table 3.7: Parameters for final 'Optmised Run' with increased TEMAH dose and good uniformity.

Therefore, using the DOE and optimisation runs, the final 'Optimised Run' gaining the best uniformity of thickness, along with good stoichiometry was found. The parameters for this is shown as 'Optimised Run' in Table 3.6, giving an average deposition rate of

0.124 nm/cycle and an average Hf:O value of 1.90. The previously calculated monolayer thickness of 3.3 angstroms is greater than the deposition rate of 1.24 $\AA$/cycle and shows that 3 cycles are needed to achieve one monolayer. As explained previously, this deposition rate is slightly higher than reported in literature for the same and other materials due to the use of O_2 plasma. Confirming atomic layer deposition is achieved, and showing higher deposition rates than previously reported, this indicates this recipe is efficient and results in high quality hafnium oxide. This is now the standard recipe used for all hafnium oxide deposition within the University of Southampton Nanofabrication cleanroom facility, used for all future research.

3.2 TiN Development

TiN can be deposited via sputtering at the University of Southampton. Sputtering results in low levels of impurities in the metal and has easy control of the deposition rate. A sputtered layer of material is deposited in a slightly different way to evaporation, a method used for traditional electrodes such as aluminium. Evaporation of aluminium works by heating up aluminium to its evaporation temperature, using a controlled energy source. The samples to be coated are located at the top of the chamber with the target side face down, on a rotating structure. This is situated in a vacuum chamber where the pressure is between 10^{-3} and 10^{-6} mbar. This can be seen in Figure 3.20(a).



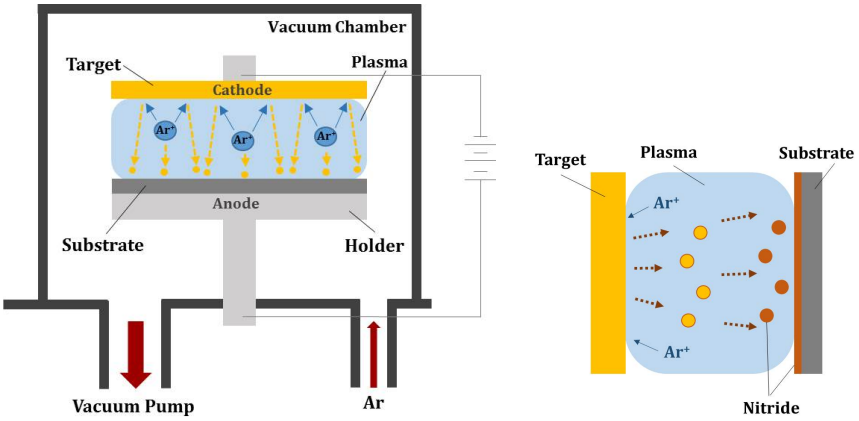
(a) (b)

Figure 3.20: Layout of an electron beam evaporator (a) inside evaporator chamber and (b) of source vaporisation set-up, adapted from [124].

There are two different ways to heat up the source to its evaporation temperature. The more simple way is by a resistive heating element but at Southampton University's Cleanroom Facility, an electron beam is used to assist. In this case an electron beam is directed at the source material, in this case a lump of aluminium, where the energy is converted to heat, vaporizing the material. This material then hits the rotating wafers and is deposited in thin layers, building up over time. The chamber contains sensing devices whereby the thickness of the material can be measured so that the electron

beam will turn off once the desired thickness is obtained. The evaporation and therefore deposition rate can be controlled by the cathode heating supply. This can be seen in Figure 3.20(b).

Sputtering works by a different process. In a sputterer, an argon plasma is created and the Ar^+ ions are then accelerated into the source or target. The argon ions are slowed down by collisions and eject the target atoms backwards. These atoms are then transported to the substrate resulting in a film forming on the substrate. The layout of the sputter chamber can be seen in Figure 3.21(a). This technique is known as non-reactive sputtering and requires a titanium nitride target to sputter TiN layers. This recipes were performed in the Physics cleanroom at the University of Southampton.



(a) (b)

Figure 3.21: Schematic representation of a typical sputtering system (a) inside sputter chamber and (b) reactive sputtering nitride process, adapted from [125].

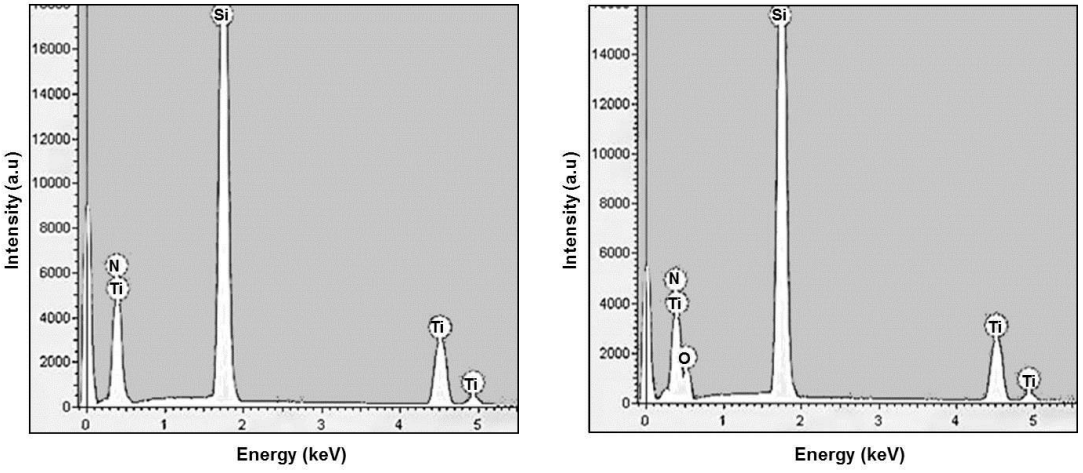
The alternate sputtering technique is known as reactive sputtering. For TiN, a titanium target is used in a nitrogen environment. This results in a more controlled titanium-to-nitrogen ratio, when compared to non-reactive sputtering. This is due to difficulty of creating a titanium nitride target, used in non-reactive sputtering, with equal amounts of nitrogen throughout. The reactive sputtering is so called, due to the fact that the sputtering occurs in a reactive atmosphere. For TiN, a mixture of Argon and N_2 is needed. The compound is deposited by using a titanium target, but this time the sputtering occurs in an nitrogen atmosphere. This can be seen in Figure 3.21(b). The non-reactive sputtering was conducted in the nanofabrication facilities in the ECS cleanroom at University of Southampton.

3.2.1 TiN Sputtering Development

In order to compare the two different sputtering techniques, reactive and non-reactive, two test samples were fabricated on silicon, using electron-dispersive X-ray spectroscopy (EDX), XRD, XPS and sheet resistance measurements. A Zeiss EVO LS25 SEM was

used with an accelerating voltage of 10 kV in order to obtain elemental spectrum EDX data using an Oxford INCAx-act X-ray detector.

EDX, also referred to as EDS, fires electrons at a sample and then measures the X-rays that are produced. The energy of the X-rays are measured and used to produce spectra of the elements that are within the sample. If the electron beam has an energy greater than the binding energy of an inner shell electron, then the inner shell electron will be knocked out. The outer shell electrons will then drop down to the now vacant inner shell, releasing an X-ray. This X-ray will have an energy equal to the energy difference of the two shells. Measuring the energies of the released X-rays will enable a spectrum to be formed, where a database of peaks and elements will identify which peak relates to which element.



(a) (b)

Figure 3.22: EDX spectrum with identified elemental peaks: (a) reactively sputtered TiN on silicon. Silicon, titanium and nitrogen peaks are identified. No oxygen peak is present and (b) non-reactively sputtered TiN on silicon. Silicon, titanium, nitrogen and oxygen peaks are identified.

The EDX elemental spectrum for reactively sputtered TiN is shown in Figure 3.22(a), whilst the non-reactively sputtered TiN spectrum is shown in Figure 3.22(b). These measurements were taken within the same hour as deposition. The element present within the reactively sputtered TiN are titanium, nitrogen and silicon. This silicon peak originates from the silicon substrate below. The elements present within the non-reactively sputtered TiN are titanium, nitrogen, silicon with the addition of oxygen at 23 percent concentration. This suggests the non-reactive technique has deposited a titanium oxynitride layer. The oxygen percentage, calculated using quantitative analysis from these EDX spectrum's, must be taken comparatively and not as an absolute value. This is due to the error that originates from the close proximity of the oxygen peak to the Ti and N peaks in the spectrum, resulting in the limitation of deconvolution of each peak.

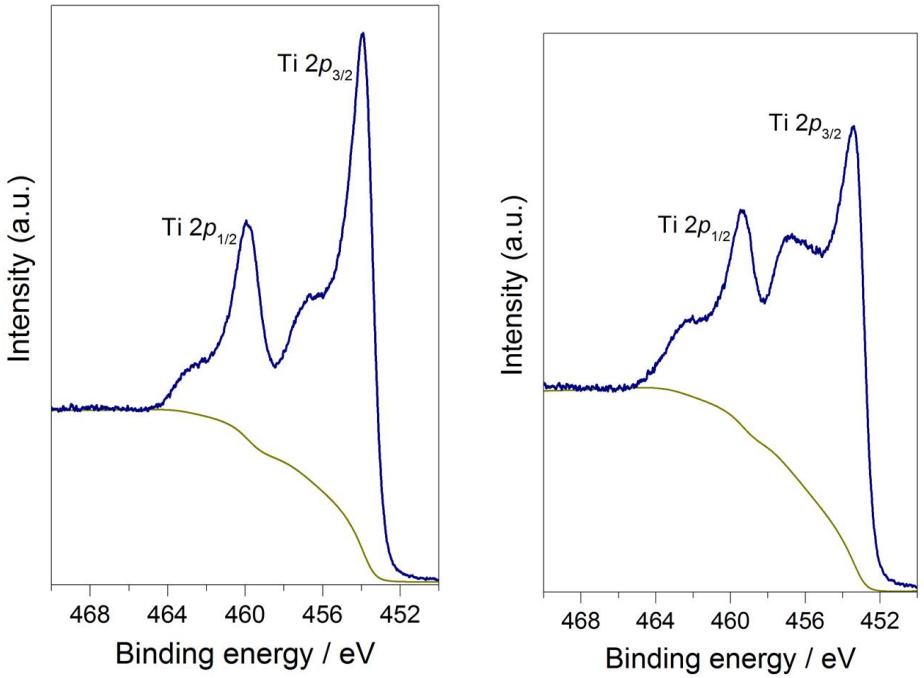


Figure 3.23: Ti2p XPS spectrum for (a) reactively sputtered TiN and (b) non-reactively sputtered TiN. Shirley background shown.

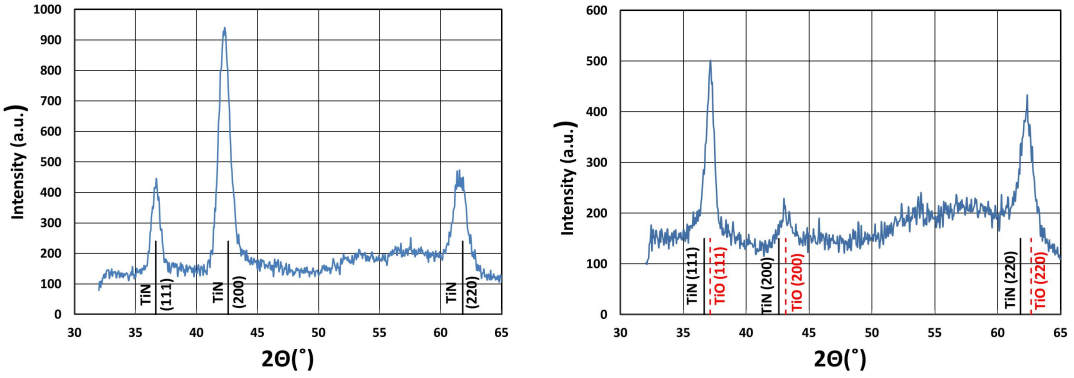
XPS was used to analyse the two TiN/Si samples, scanning titanium, nitrogen and oxygen peak energies. Table 3.8 lists the atomic concentration for each of these elements within the reactively sputtered and non-reactively sputtered TiN layers. Figure 3.23 shows the Ti2p peaks for both the TiN layers, whereby different oxidation states are observed [126]. The non-reactively sputtered Ti2p peaks have a larger intensity ratio between the higher binding energy core levels and the oxidation states. The reactively sputtered Ti2p peaks have a larger intensity ratio between the higher binding energy core levels and the Ti^{3+} state, associated with TiN. The surface sensitivity of XPS measurements has resulted in a 16 percent oxygen baseline for the reactively sputtered TiN. The non-reactive sputtered TiN shows an additional 23 percent on top of this baseline, in agreement with the EDX data.

	Atomic Percentage			
TiN Sputter Technique	**Ti2p**	**N1s**	**O1s**	**Sheet Resistance (Ω sq)**
Reactive	41.28	42.62	16.10	7
Non-reactive	35.34	26.10	38.56	300

Table 3.8: XPS measured atomic concentration of Ti2p, N1s and O1s for two sputtered technique of TiN and sheet resistance measurements.

XRD data was collected for the TiN/Si samples, using grazing incidence Θ=3 ° using a Bruker D8 with GADDs diffractometer (Cu-$K_{\alpha 1}$) for phase identification purposes. The XRD patterns obtained from the reactively sputtered and non-reactively sputtered

TiN layers can be seen in Figure 3.24(a) and Figure 3.24(b) respectively. Stoichiometric titanium nitride can be identified for the reactively sputtered TiN layer whereby the experimental peaks align with the theoretical TiN peak (black lines) as shown in Figure 3.24(a). The non-reactive sputtered TiN XRD patten is more complex to identify due to the similar XRD patterns of titanium oxide and titanium nitride. This is shown by the TiN theoretical peaks shown in black and the theoretical peaks of TiO shown by dashed red lines in Figure 3.24(b). However, due to the high concentration of oxygen found in previous material characterisation techniques such as EDX and XPS, the crystal structure is most likely a mixture of both titanium nitride and titanium oxide.



(a) (b)

Figure 3.24: XRD patterns for TiN/Si samples with (a) reactively sputtered TiN with identified TiN PDF *38-1420 peaks and (b)non-reactively sputtered TiN with identified TiN PDF *38-1420 and TiO PDF *78-0720 peaks.

The sheet resistance measurements for the two TiN layers are shown in Table 3.8. The reactive TiN has a lower sheet resistance compared to the non-reactive TiN indicating a lower concentration of oxygen present in this layer. This is in agreement with EDX and XPS results. To summarise, the material characterisation performed on the sputtering techniques indicates that the reactive sputtering technique results in stoichiometric TiN whilst non-reactive sputtering results in TiO_xN_y. The high oxygen concentration in the non-reactive sputtering could be due oxidation of the TiN target or presence of oxygen in the chamber during deposition.

3.2.2 TiN Etch Development

Following deposition, top electrodes can be created via etching of the top electrode layer. For traditional electrode materials, such as aluminium, wet etching is performed by using an aluminium etchant solution via the chemical reaction as shown in Equation 3.7. The way in which this wet etch works is to first oxidise the aluminium, forming Al_2O_3 by nitric acid. The aluminium oxide then reacts with the phosphoric acid component, forming soluble $AlPO_4$. Hydrogen gas is one of the by-products which can remain on

the surface of the wafers. To overcome this issue, the enchant is agitated through heating and bubbling, preventing the gas from adhering to the surface [127].

$$6H^+ + 2Al \Rightarrow 3H_2 + 2Al^{3+} \tag{3.7}$$

The etch used for titanium nitride has not been developed previously at the University of Southampton. Three main chemicals have previously been reported for etching of TiN: fluorine, chlorine and bromide [128–132]. Fluorine was chosen for the etchant of titanium nitride, in the form of CF_4, using a plasma etch process. Plasma etching is a form of dry etching. In plasma etching, two processes occur simultaneously. Firstly a chemical reaction occurs at the surface of the wafer, due to active neutrals in the plasma. For TiN etch using CF4/O_2, the reaction of active fluorine radicals with the TiN layers produces by-products including TiF_4 and NF_x [133]. At the same time, ions from the plasma (O_2 for the CF4/O_2 TiN etch) are accelerated by an radio frequency (RF) field and bombard the surface of the wafer resulting in physical milling. This releases energy and aids the chemical reactions that occur at the surface. At the University of Southampton, a reactive ion etcher, or RIE, can be used for CF_4 etching. A reactive ion etcher is a plasma etch reactor which exists of a parallel plate diode where one electrode is powered, whilst the other remains grounded. In an RIE, the wafer is positioned on the electrode that is biased [134].

For the development of the TiN etch, a surface profiler was used to measure the step heights before etch, after etch with the resist on and after etch with the resist off. Using this technique, the etching recipe was developed, resulting in an etch rate of 24 nm/min, with a selectivity of 1:5 for TiN:Resist. The parameters of the etch is shown in Table 3.9.

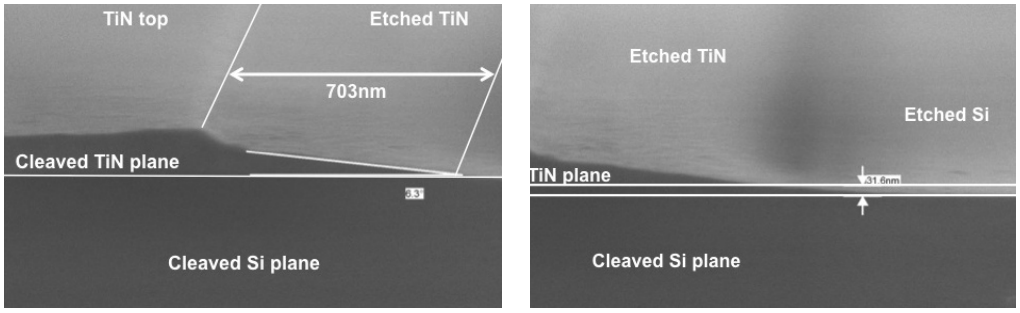
Power [W]	**O_2:CF_4**	**O_2 [sccm]**	**CF_4 [sccm]**	**Pressure [mT]**
200	15	20	100	50

Table 3.9: Parameters for Titanium nitride etch

The profile of the etch was measured using the SEM, using a test wafer with 125 nm TiN. A sloped profile of the side of the etch can be seen in Figure 3.25(a). This slope indicates a poor side-wall profile with a 6 degree slope rather than the optimum 90 degrees. This could be due to limited chemical reaction between the CF_4 and the TiN surface, indicating a physical milling process rather than a chemical etch. This, however, does not pose any problems due to the large device sizes and large spacing between devices used throughout this research. The length of the sidewall is on the scale of hundreds of nanometres, whereas the smallest electrode is 10 μm in length for this research and therefore the dimension of the sidewall is negligible.

There is much conflict in publications for titanium nitride etching using halogen chemistries concerning the etch rate [135]. One group described easy formation of high volatile etch

by products leading to a high etch rate [136, 137], whilst the other reported a slow etch rate, with difficulty obtaining anisotropic etch profiles [138]. For other applications where this profile is inadequate, a different type of etching known as inductively coupled plasma (ICP) plasma etching could be developed to increase the chemical reaction using a higher ion and radical density.



(a) (b)

Figure 3.25: SEM image showing TiN etch features of (a) sidewall profile and (b) an overetch.

Figure 3.25(b) shows the sidewall profile of the titanium nitride etch again, but this time the over-etch of the silicon is shown. The etch has slightly etched into the silicon, by around 30 nm. This will ensure the titanium nitride devices are disconnected from each other and is an acceptable amount of over etch.

Checks can be performed during fabrication of devices to ensure the full thickness of the layer has been etched including microscopy images and resistance measurements before, during and after.

3.3 Summary

A TiN/HfO$_x$ stack was developed using material characterisation to analyse the process parameters.

Hafnium oxide was deposited via ALD using a TEMAH and O_2 plasma. The first development step was done by performing material analysis of an initial recipe, supplied by the ALD tool manufacturer, OIPT. From ellipsometry, a deposition rate of 0.16 nm/cycle was extracted. Comparing this with an estimated monolayer thickness of 0.33 nm for hafnium oxide, this shows over 3 cycles are needed to achieve one monolayer verifying the deposition is within the ALD growth window. This is an efficient growth rate when compared to previously reported ALD recipes due to the use of an O_2 plasma. A thickness range across a 6 inch wafer of 14 percent was measured. This variation in thickness uniformity however can be utilised for electrical measurements of fabricated

devices. From XPS, Hf:O ratio of around 2 was measured near the surface indicating near stoichiometric hafnium oxide.

Following this, an investigation into the table temperature effects on stoichiometry and material properties was conducted. The temperatures chosen were 300 °C, 350 °C and 400 °C with the remaining parameters unchanged from the initial hafnium oxide recipe. Using XRD, cubic crystal structures were measured for hafnium oxide deposited at 300 °C and 350 °C, whilst a monoclinic structure was measured for 400 °C. Using XPS, a Hf:O ratio of 1.78±0.05, 1.99±0.05 and 1.95±0.05 was extracted for 300 °C, 350 °C and 400 °C, respectively. Hence the lowest temperature of 300 °C results in sub-stoichiometric HfO_x.

Finally, a full DOE was conducted resulting in an optimised recipe for stoichiometric hafnium oxide following severe and multiple tool breakdowns. A Plackett-Burmann design was chosen with 3 repeat centre points. The results indicated the TEMAH dose had the largest effect on the Hf:O ratio. A set of optimisation runs then followed until the final optimised recipe was reached. From ellipsometry, a deposition rate for the optimised recipe was extracted to be 0.12 nm/cycle with a thickness range of 4 percent across a 6 inch wafer. This is an efficient growth rate resulting in uniform ALD deposition of hafnium oxide. From XPS, a Hf:O ratio of 1.90 was extracted. Therefore the optimised recipe has been shown to produce $HfO_{1.9}$ at a deposition rate of 0.12 nm/cycle. This recipe is now the standard recipe for all hafnium oxide deposition within the nano-farbication cleanroom.

The TiN development was conducted to investigate the material properties of two sputtering techniques; reactive and non-reactive. Using EDX, XPS, XRD and sheet resistance measurements, large amounts of oxygen are found to exist within non-reactively sputtered TiN indicating the deposition of a TiO_xN_y layer. The same material characterisation showed stoichiometric TiN is deposited for the reactively-sputtered TiN process.

An etch recipe for TiN was developed for the first time at the nano-fabrication cleanroom at the University of Southampton. A dry etch, using RIE, was developed using a mixture CF_4 and O_2. Although a side-wall slope of 6 degrees was obtained, this is acceptable for devices on the scale of micro-meters in size and spacing.

Chapter 4

Radiation Hardness of MOSFET High-k Dielectrics

The CMOS industry is being revolutionised through the use of high-k dielectrics in MOS transistors, due to their ability to achieve the same capacitance as much thinner silicon dioxide devices. This overcomes leakage issues and enables the scaling of devices with MOS capacitor structures, such as MOSFETs, to continue.

The movement towards high-k devices requires space and nuclear industries to investigate the radiation response of these new materials before any devices are purchased. In order for companies within these industries to proceed with using high-k MOS capacitors, a batch of high-k MOS capacitors have been fabricated, irradiated and analysed. By looking at the electronic characteristics of these devices before and after radiation, the effects of the radiation on the high-k layers can be concluded.

In this chapter, the capacitor structures are explained in Section 4.1, followed by the pre-irradiation C-V analysis, in Section 4.2. The irradiation of these devices is discussed in Section 4.3. If these high-k devices result in similar or increased radiation hardness, when compared to silicon dioxide, then these devices can be considered for use in radiation environments.

This work was written as a technical report for AWE ltd.

4.1 Capacitor Structure

High-k MOS capacitors were fabricated. The cross section of a typical capacitor is shown in Figure 4.1. Many capacitors were fabricated simultaneously on a 6 inch wafer, in repeated arrays of different sizes and shapes. In each array, there are various sizes in

circle and square shapes, defined by the metal contact. The top-down view of a typical array of capacitors is shown in Figure 4.2.

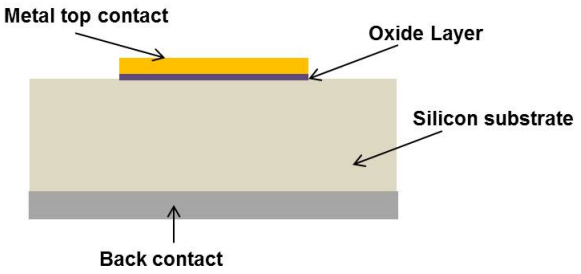


Figure 4.1: Schematic of cross section of typical capacitor.

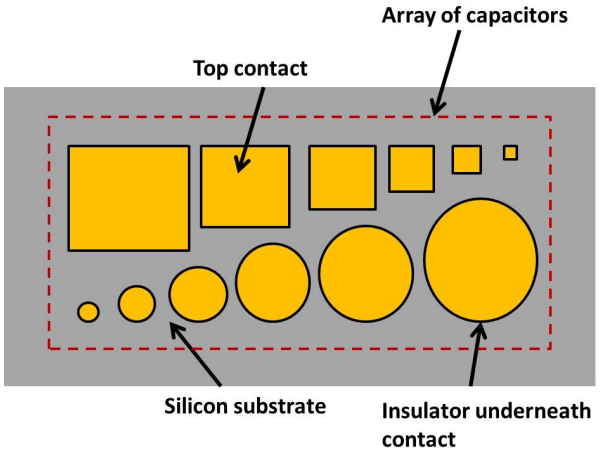


Figure 4.2: Schematic of top-down view of differently sized capacitors defined by top contacts, with the array repeated across whole of wafer.

Many different batches of capacitors were fabricated with varied oxide thicknesss and oxide material types. The different batch splits are de-pictured by showing the various cross-sections in Figure 4.3.

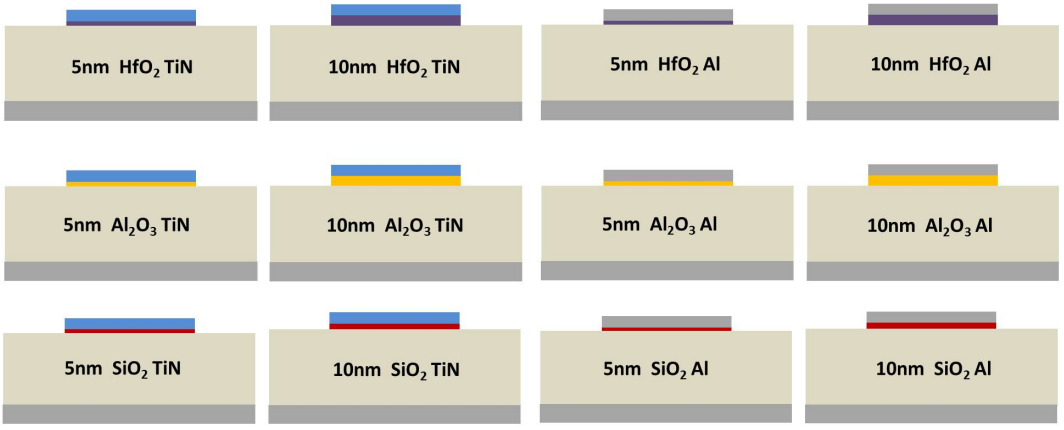


Figure 4.3: Schematic of capacitor cross-sections with oxide materials, thicknesss and top electrode materials labelled.

The two different top electrodes (aluminium and titanium nitride) along with the three different insulator materials (silicon oxide, hafnium oxide and aluminium oxide) provide a variety of interfacial layers, at the top and bottom of the insulator layer. Fabricating and irradiating a selection of insulator and top electrodes, with the silicon dioxide reference batch, allows the radiation impact of the interfacial layers to be studied. Different insulator layer thicknesss enables the bulk oxide traps to be investigated.

The first fabrication step is the deposition of the bottom electrode followed by the deposition of the insulator layer and then the top metal layer. The electrodes are then defined using photo-lithography and etching. An overview of the fabrication processes used for each type of material are briefly described here:

1. Back electrode - aluminium evaporation for all wafers (500 nm)
2. Oxide layer - thermal growth for SiO_2, ALD for high-k dielectrics
3. TiN Top electrode - *Reactively* sputtered followed by dry etch (125 nm)
4. Al Top electrode - Evaporation followed by wet etch (200 nm)

Details of the hafnium oxide and TiN development are discussed in Chapter 3 whilst the remaining processes are well known and previously developed. The hafnium oxide recipe used for the capacitors was the HfO_x recipe, described in Table 3.1.

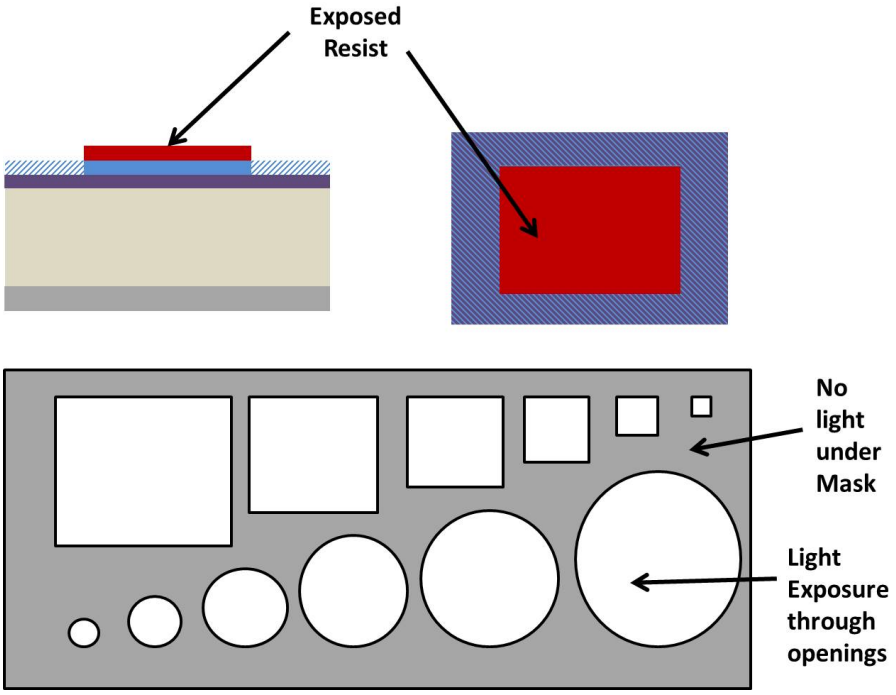


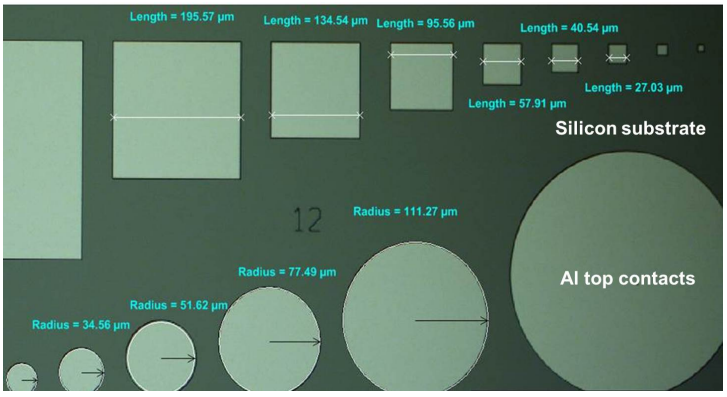
Figure 4.4: Schematic of lithography steps for capacitor layout with a dark field mask resulting in exposed areas of resist acting as etch mask.

An array of different sized capacitors are created on one wafer. The dimensions of the mask are listed in Table 4.1. A negative resist, AZ2070, is used in conjunction with a dark mask where the exposed areas are the circles and squares, strengthening these areas of resist. The other areas of resist are removed in developer, AZ2070. A schematic of the lithography process and mask is shown in Figure 4.4.

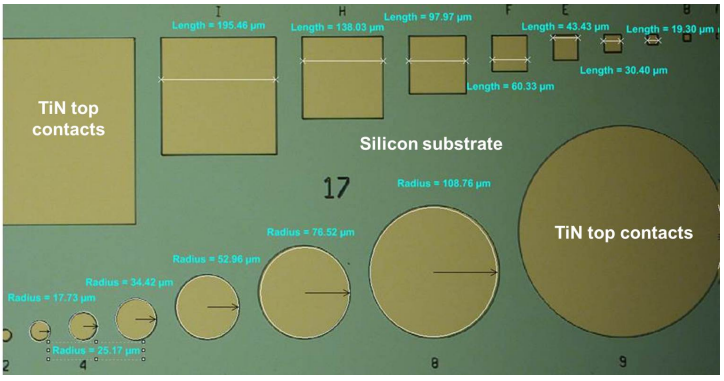
Area [10^{-6}cm^2]	1000	400	200	100	40	20	10	4	2	1
Length of Square [μm]	316	200	141	100	63	45	32	20	14	10
Radius of Sphere [μm]	179	113	80	56	36	25	18	11	8	6
Capacitance [pF]	1726	690	345	173	69	34	17	7	3	2

Table 4.1: Capacitor sizes and expected capacitance for EOT of 2 nm

After the lithography has been conducted, resist remains on top of the metal contact. These resist areas protect the metal gate areas underneath when etching occurs. After the resist is stripped, the capacitors are created as shown in Figure 4.5(a) and Figure 4.5(b) and for aluminium and titanium nitride, respectively.



(a)



(b)

Figure 4.5: Microscope images showing the etched metal contacts of (a) Al and (b) TiN wafers.

4.2 Capacitor Characteristics

An Agilent 4179 high frequency 1 MHz C-V meter is used to measure the capacitance voltage characteristics of the MOS capacitors. The key characteristics of dielectrics, the dielectric constant and thickness, can be extracted from C-V measurements. Current measurements, done in parallel with the C-V measurements, can also be used to extract the leakage current characteristics, an important material property for dielectrics within a MOS capacitor structure.

When using AC signals, the opposition that a circuit or device presents to the AC current is known as impedance. Impedance, Z, is made up of a real and imaginary part. The real part of impedance is the resistance, R. For capacitors and inductors, a phase shift between the voltage and current can occur and this effect is called a reactance, X, and is the imaginary part of impedance. The extracted values of capacitance, inductance and resistance depend on the measurement circuit model. For MOS capacitors with thin oxides, it is best to use a parallel circuit model whereby the series resistance is neglected, as depicted in Figure 4.6.

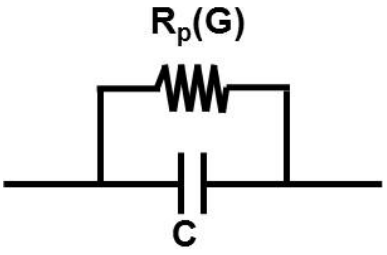
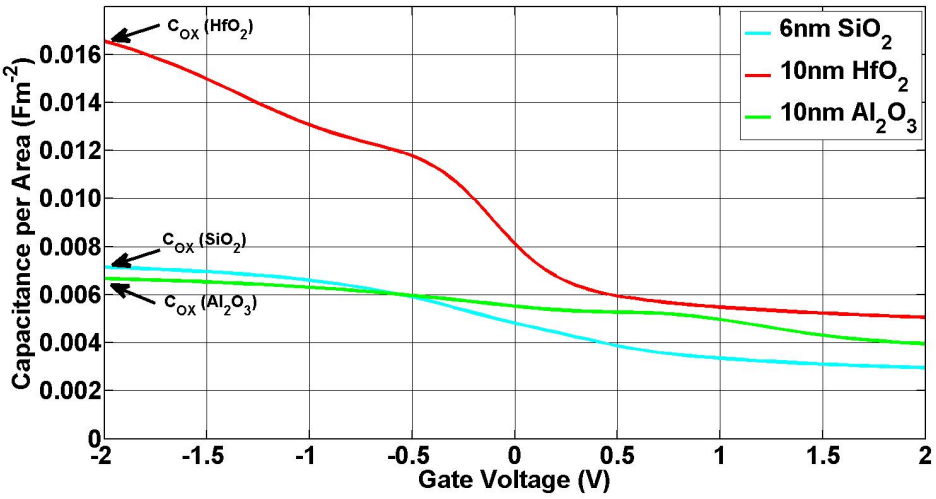


Figure 4.6: Parallel equivalent circuit model diagram for Cp-G measurement mode of a capacitor.

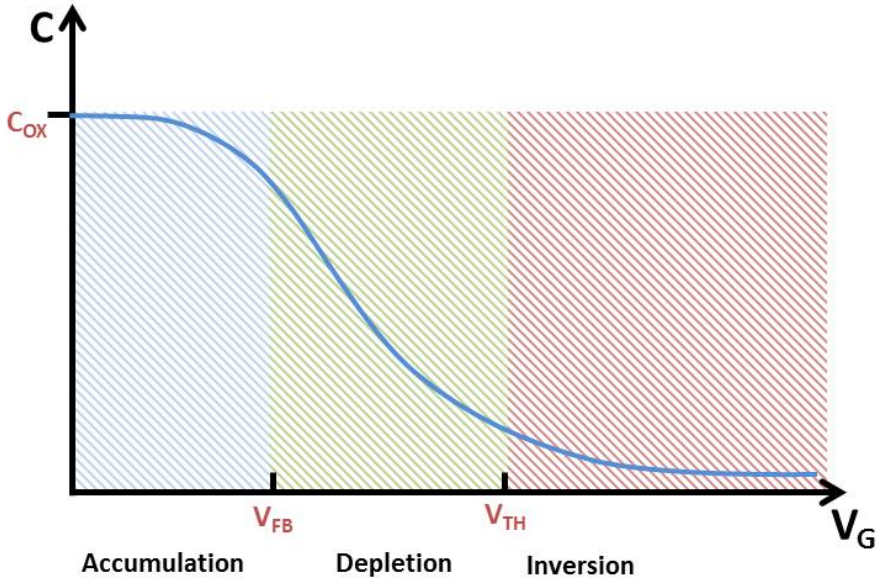
When using the parallel circuit model, it is better mathematically to use the term admittance, Y, which is the reciprocal of impedance. The equation for admittance is shown in Equation 4.1 whereby the real part is shown to be conductance, G, and the imaginary part is shown to be susceptance, B.

$$Y = G + iB \tag{4.1}$$

Typical CV curves are shown in Figure 4.7(a) for capacitors with TiN electrodes, whereby a bias sweep was applied from plus 2 V to minus 2 V, going from inversion through to accumulation. The approximate regions for accumulation, depletion and inversion are depicted in the theoretical schematic shown in Figure 4.7(b). In comparison to the ideal CV curve, a double hump characteristic is seen for the high-k capacitors. This has been attributed to the build up of interface traps [139–142]. The double hump characteristic is not present for SiO_2.



(a)



(b)

Figure 4.7: (a) Experimental capacitance/area as a function of applied voltage for capacitors with a TiN electrode compared to (b) theoretical CV Curves for nMOS Capacitor, with accumulation, depletion and inversion regions highlighted.

The CV curves shown in Figure 4.7(a), will be analysed fully in Section 4.2.1, Section 4.2.2 and Section 4.2.3.

4.2.1 Equivalent Oxide Thickness

Figure 4.8 shows the capacitance per unit area graph for the three different dielectrics, all with TiN electrodes. This graph was plotted for all other types of capacitor, whereby the capacitance value plotted on the y-axis is the maximum capacitance taken from CV measurements, as indicated by the black arrows shown in Figure 4.7(a). This was performed on 12 different wafers, one wafer for each capacitor structure, with four areas on each, resulting in 48 measurements in total.

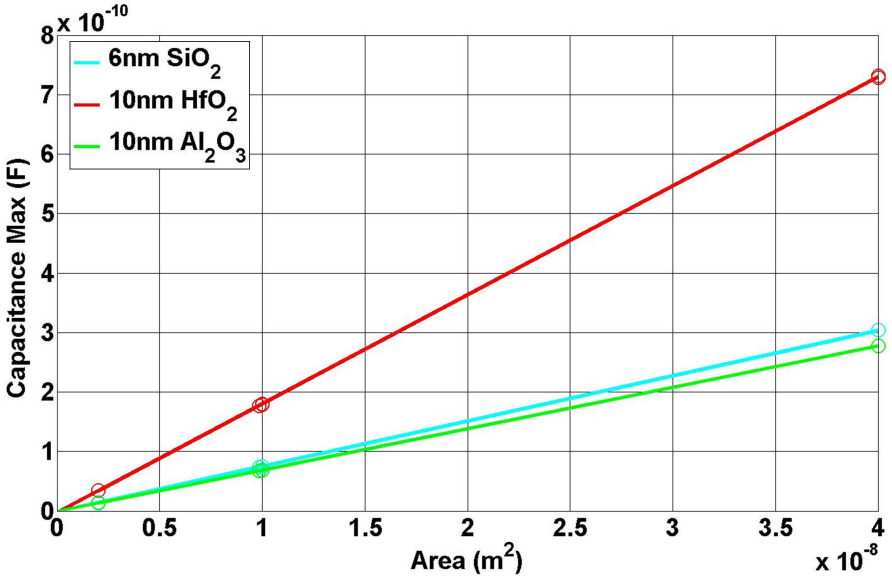


Figure 4.8: Maximum Capacitance as function of gate area voltage for three dielectrics with TiN electrodes. Gradients can be extracted to calculate the EOT, allowing for a comparison of the dielectrics.

The gradients were measured on all capacitance per unit area plots, for all capacitor structures, and can be seen in Table 4.2. The top 6 rows are for TiN contacts whilst the bottom 6 are for Al contacts. For a parallel plate capacitor, the capacitance per unit area is given by Equation 4.2, where t_{high-k} is the physical thickness of the high-k material, ϵ_{high-k} is the dielectric constant of the bulk high-k material and ϵ_0 is the permittivity of free space.

$$\frac{C}{A} = \frac{\epsilon_0 \epsilon_{high-k}}{t_{high-k}} \tag{4.2}$$

However, when fabricating capacitors, the values of ϵ_{high-k} and t_{high-k} are hard to determine, without knowing one of the two values accurately. Also, it assumes a single uniform layer without interface effects, which is usually not the case.

In order to compare the effects of different dielectrics, the term equivalent oxide thickness, EOT, can be introduced, enabling a comparison between capacitance achieved by

high-k materials and silicon dioxide. The theoretical equivalent oxide thickness of each high-k layer can be calculated using Equation 2.25, repeated here for convenience as Equation 4.3, where ϵ_{SiO_2} is the dielectric constant of bulk silicon dioxide. The term $\frac{\epsilon_{high-k}}{t_{high-k}}$ from Equation 4.2 has now been put into a useful form, allowing the dielectric effects to be compared.

$$EOT = \frac{\epsilon_{SiO_2}}{\epsilon_{high-k}} \cdot t_{high-k} \tag{4.3}$$

Theoretically, for a set physical thickness, the higher the ϵ_{high-k} value, the lower the EOT. Therefore the dielectric with the highest ϵ_{high-k} value will result in a lowest EOT and therefore highest capacitance, for a set thickness, enabling the scaling limitation of the silicon dioxide gate dielectric to be overcome.

The theoretical EOTs for the different capacitor structures being investigated in this work are calculated using Equation 4.3 with dielectric constants from literature and the target thickness of the dielectrics layers. This is shown in the first two columns of Table 4.2 for all 12 types of capacitors being investigated. The dielectric constants used for the theoretical calculation were 25 and 9 for HfO_2 and Al_2O_3, respectively [54].

Electrode	**Dielectric**	$\mathbf{t_{ox,theory}}$ **[nm]**	$\mathbf{EOT_{theory}}$ **[nm]**	$\mathbf{C/A_{exp}}$ **[Fm^{-2}]**	$\mathbf{EOT_{exp}}$ **[nm]**
TiN	**SiO_2**	6	6	7.6x10^{-3}	4.53
TiN	**SiO_2**	3	3	8.6x10^{-3}	4.03
TiN	**Al_2O_3**	10	4.30	7.0x10^{-3}	4.97
TiN	**Al_2O_3**	5	2.17	1.24x10^{-2}	2.79
TiN	**HfO_2**	10	1.56	1.83x10^{-2}	1.77
TiN	**HfO_2**	5	0.78	2.44x10^{-2}	1.41
Al	**SiO_2**	6	6	2.6x10^{-3}	13.27
Al	**SiO_2**	3	3	3.3x10^{-3}	10.57
Al	**Al_2O_3**	10	4.30	5.2x10^{-3}	6.67
Al	**Al_2O_3**	5	2.17	7.5x10^{-3}	4.61
Al	**HfO_2**	10	1.56	9.7x10^{-3}	3.56
Al	**HfO_2**	5	0.78	1.1x10^{-2}	3.10

Table 4.2: Equivalent oxide thickness of aluminium oxide and hafnium oxide with TiN and Al contacts. Theoretical EOT is calculated from targeted thickness whilst experimental EOT is extracted from graidents of C/A plots.

The way in which EOT can be extracted experimentally is by taking the gradient of the capacitance-area plot, and dividing it through by ϵ_0, giving the $\frac{\epsilon_{high-k}}{t_{high-k}}$ term, as shown by Equation 4.2. This can then be inserted into Equation 4.3, to give the EOT experimental value. The experimental EOT values for each capacitor type is shown in the last column in Table 4.2.

Table 4.2 can now be analysed allowing comparison not only between theory and experimental EOTs, but also between the capacitor structure types. As the theoretical EOTs suggest, as the physical thickness t_{ox} is reduced, the experimental EOT is also

reduced, for all capacitor types. Therefore in trend of reducing EOT with reducing t_{ox}, the experimental and theoretical values are in agreement.

The experimental values for each electrode type also show agreement with theory whereby the HfO_2 dielectrics have the lowest EOTs, followed by the Al_2O_3 dielectrics with SiO_2 having the largest EOTs. All structures have a higher experimental EOT, except the 6nm SiO_2 with TiN, which has a smaller experimental EOT than calculated theoretically. This anomaly most likely arises from the SiO_2 physical layer being thinner than the target 6 nm thickness.

Looking at capacitors with TiN electrodes, the experimental and theoretical EOTs have similar values for all dielectrics, except the 6nm SiO_2 anomaly previously discussed. Looking at capacitors with Al electrodes, all experimental EOT values are far larger, sometimes double, compared to the theoretical EOT values. As the expected scaling of increasing EOT with increasing permittivity and thickness is seen, this significant difference between experimental and theory must originate from the Al electrode, rather than from the dielectrics.

For both types of electrodes, the HfO_2 shows superior dielectric qualities with the lowest EOT value, even at the thickest 10 nm targeted thickness. This indicates HfO_2 has superior capacitance properties with the potential to replace SiO_2, enabling the scaling limitations of gate dielectrics to be overcome.

The difference between the Al and TiN experimental EOTs, and the difference between theoretical and experimental EOT for Al capacitors indicates that the electrode plays an important role in capacitor properties. This suggests that interfacial layer that forms when the electrodes are deposited on top of dielectrics, play an important role. Section 4.2.2 investigates the interfacial contributions by extracting the dielectric constant and interfacial EOT for each high-k capacitor.

4.2.2 Dielectric Constant Analysis

This equivalent oxide thickness, can be split up into two parts; the EOT originating from the bulk of the oxide, and the EOT originating from the interfaces of the oxide. When an oxide forms on top of a silicon wafer, a reaction will occur producing an interfacial layer. This will also occur when the metal is deposited on top of the oxide, resulting in two interfacial layers, which have different material properties than that of the bulk oxide. These interfacial layers are often on the order of nanometres and therefore, when thick oxides are deposited, the effect from these layers is negligible. For our MOS capacitors, where the oxide thickness is also on the orders of nanometres, these interfacial layers must be taken into consideration. The interfacial layers now form a capacitance of their own and therefore the total capacitance of the oxide is equal to the sum of the reciprocal capacitances, as shown in Equation 4.4.

$$\frac{1}{C_{total}} = \frac{1}{C_{bulk}} + \frac{1}{C_{int}} \tag{4.4}$$

As the equivalent oxide thickness EOT is proportional to the reciprocal capacitance, the effective EOT can be expressed as the sum of the bulk EOT and the interfacial EOT, as shown in Equation 4.5.

$$EOT_{total} = \frac{\epsilon_{SiO_2}}{\epsilon_{high-k}} \cdot t_{high-k} + EOT_{int} \tag{4.5}$$

The equivalent oxide thickness of the interfacial layers can be thought of as independent of the bulk oxide thickness, whereas the bulk EOT obviously scales with the thickness of the oxide deposited. This allows the effect of the two components to be separated by looking at the capacitance of the capacitors with the same gate material, but with different oxide thicknesss. If the differential of Equation 4.5 is taken, with respect to the thickness of the high-k oxide, the dielectric constant of the high-k materials can be found. This is shown mathematically in Equation 4.6.

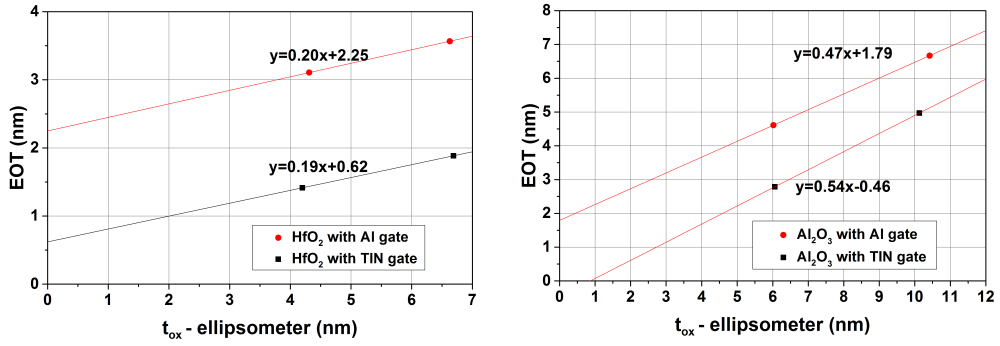
$$\frac{\delta EOT}{\delta t_{high-k}} = \frac{\epsilon_{SiO_2}}{\epsilon_{high-k}} \tag{4.6}$$

When the thickness of the high-k material is set to zero in Equation 4.5, the EOT of the interface is found, which can be thought of as the situation when the bulk oxide is removed, leaving behind the interfacial layers only. This is represented graphically in Figure 4.9(a) and Figure 4.9(b) for hafnium oxide and aluminium oxide, respectively. The equivalent oxide thickness, plotted on the y-axis, is taken from the electrically measured capacitance-area plots, and the physical oxide thickness, is plotted on the x-axis, is found through ellipsometry. Ellipsometry can accurately measure very thin films down to the angstrom scale and therefore can be used to measured our thin oxide layers. The ellipsometry fit for both aluminium oxide and hafnium oxide had an MSE of around 5 indicating a good fit.

high-k, metal gate	$EOT_{int}[nm]$	ϵ_{high-k}
HfO_2, TiN	0.6	20.6
HfO_2, Al	2.2	19.6
Al_2O_3, TiN	0.0	7.3
Al_2O_3, Al	1.8	8.3

Table 4.3: high-k dielectric constant and interfacial EOT extracted from the partitioning of total effective oxide thickness

A linear fit was performed for every pair of thick and thin oxide type, for both types of metal. The gradient of these linear fits were then extracted and can be seen in Table 4.3. Many important conclusions can be drawn from Table 4.3, Figure 4.9(a) and



(a) (b)

Figure 4.9: EOT as a function of ellipsometer measured oxide thickness for (a) HfO_2 and (b) Al_2O_3, with linear fit through two points with the same metal gate. The dielectric constant (gradient) and interfacial EOT (intercept on y-axis) are extracted.

Figure 4.9(b). This shows that the interfacial EOT for the aluminium gated capacitors is more than 2 nm for both the aluminium oxide and hafnium oxide dielectrics, indicating that the aluminium is highly reactive with the oxides, forming a thick interfacial layer. For the 5 nm hafnium oxide capacitor, this interfacial oxide has a greater contribution than that of the bulk hafnium oxide. This is not ideal. The titanium nitride gated capacitors, on the other hand, have interfacial EOTs of less than 0.5 nm, indicating the inert properties of titanium nitride. This theory is verified also by the lack of oxygen found in the reactively sputtered TiN EDX spectrum, as discussed in Chapter 3.

The gradients, and therefore dielectric constants of the high-k materials can also be extracted. Literature suggests bulk aluminium oxide has a dielectric constant of around 9, whilst bulk hafnium oxide has a dielectric constant of around 25 [54]. The dielectric constant extracted from this data for aluminium oxide is in excellent agreement with the literature values. The hafnium oxide dielectric constant is slightly lower than that of the reported bulk value. As the thickness of deposited layers tend towards nm's, the dielectric constants can vary compared to the bulk material values due to the difference in micro-structures [143]. However, the consistency seen for both dielectric constants, across the different types of capacitors in this work, testifies the controlled fabrication process.

From this analysis, it is concluded that TiN HfO_2 capacitors have the smallest overall EOT, seen in Table 4.2 and have one of the smallest interfacial EOT, seen in Table 4.3. This indicates the TiN HfO_2 structure would be a good replacement for the traditional poly-Si/SiO_2 gate structure. In order to measure how good the different dielectrics are working as capacitors, the leakage current needs to be investigated as well. This is done in Section 4.2.3.

4.2.3 Leakage Current

High leakage current indicates poor quality of insulator layers. If the leakage current measured by the C-V system, expressed as the conductance or real part of the admittance, G, is larger than the capacitance, expressed as susceptance or imaginary part of the admittance, B, then the extracted capacitance values are no longer reliable. This is due to the extracted capacitances being subject to artefacts related to the leakage current.

Leakage current versus area can be plotted whereby the gradient gives the current density, J, allowing for a direct comparison between capacitors. This is shown for 10nm aluminium oxide with Al gate in Figure 4.10, for three different gate voltages. This graph is typical for all types of capacitors.

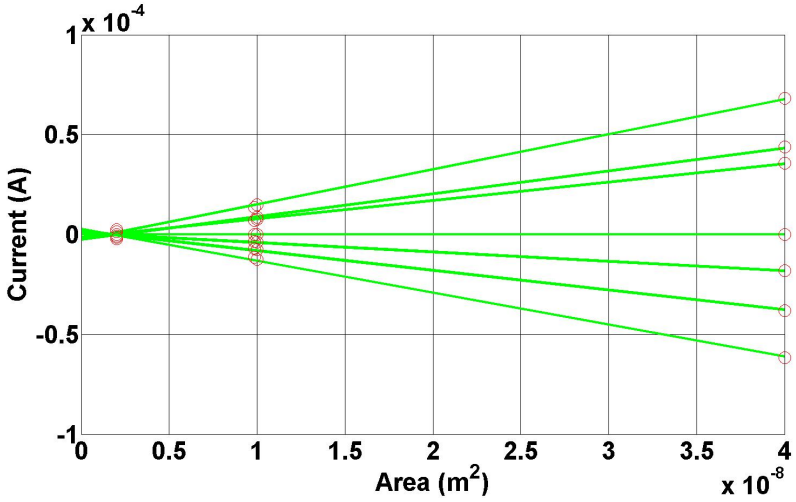


Figure 4.10: Leakage Current as a function of area for 10 nm Al_2O_3 capacitor with Al gates, for different three different gate voltages.

Table 4.4 provides an overview of the leakage current density, alongside the respective capacitance values. From the capacitance per unit area and leakage current densities, the real and imaginary parts of the admittance, conductance G and susceptance (B) respectively, can be found and are also shown in the table. The last column in the table gives the ratio of the susceptance and conductance, where a ratio larger than 1 indicates they have more of a resistive behaviour than a capacitive behaviour. The two wafers, with 3 nm of silicon dioxide, both have a ratio of 1 or larger. All other structures act as proper capacitors indicating a good quality insulator layer.

It must be noted that for leakage currents through thin dielectrics, the current is not usually proportional to the applied voltage, since it is determined by tunneling. Nevertheless, the reason for introducing high-k dielectrics can be seen clearly when plotting the capacitance versus the leakage current, as is shown in Figure 4.11.

high-k	metal gate	t_{ox} [nm]	$C[mF/m^2]$	$J[A/m^2]$	$B[\mu S]$	$G[\mu S]$	G/B
SiO_2	Al	6	2.6	378	655	5	0.01
SiO_2	TiN	6	7.6	2787	1915	37	0.02
SiO_2	Al	3	3.3	57849	821	771	1.00
SiO_2	TiN	3	8.6	426820	2154	5691	2.64
HfO_2	Al	5	11.1	4918	2795	66	0.02
HfO_2	TiN	5	24.4	65693	6138	876	0.14
Al_2O_3	Al	5	7.5	960	1883	13	0.01
Al_2O_3	TiN	5	12.4	7810	3114	104	0.03
HfO_2	Al	10	9.7	1076	2434	14	0.01
HfO_2	TiN	10	18.3	7446	4605	99	0.02
Al_2O_3	Al	10	5.2	1266	1301	17	0.01
Al_2O_3	TiN	10	7.0	30991	1746	413	0.24

Table 4.4: Maximum Capacitance per area and leakage current at -3V gate voltage with corresponding imaginary and real admittance values, along with the ratio of these both. The admittance values are for capacitors sized 4×10^{-4} m^2

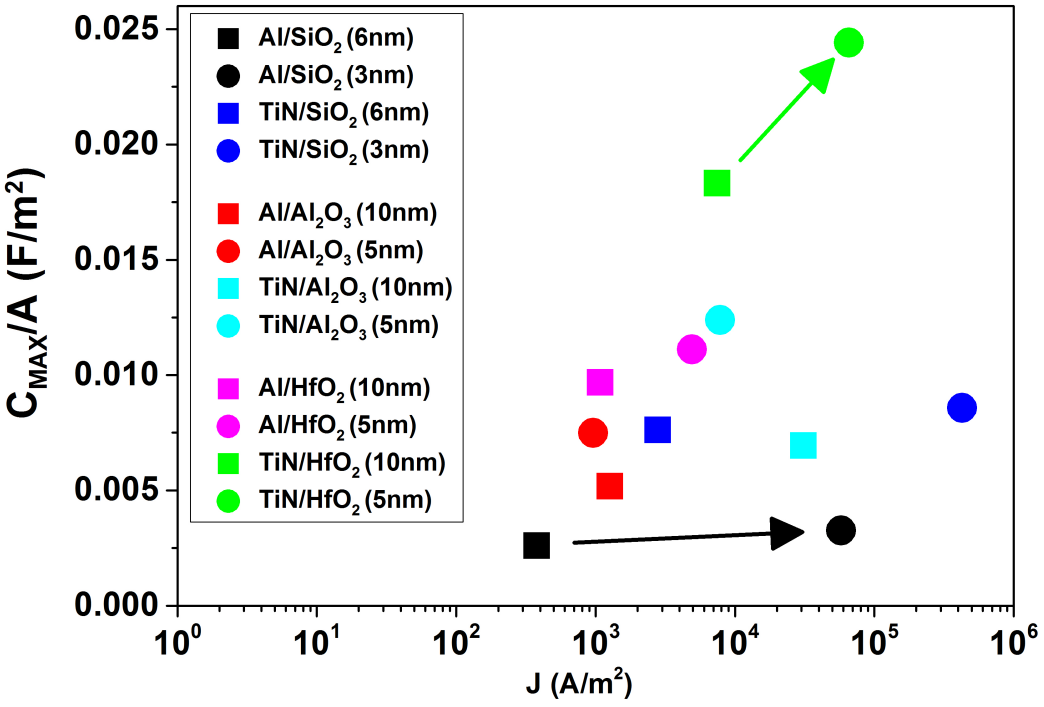


Figure 4.11: Maximum Capacitance per Area as a function of Leakage Current, J, for all capacitor structures

All the different types of capacitors are plotted in a capacitance-leakage plot, whereby the advantages of high-k capacitors is shown clearly. The introduction of high-k dielectrics allows a large increase in capacitance, without a direct increase in leakage current that would occur in silicon dioxide. The 6 nm silicon dioxide film has the lowest leakage current, but also the lowest capacitance. The capacitance can be increased by halving the

oxide thickness, as seen by the 3 nm silicon dioxide film, but the increase in capacitance is only small (around 10 percent), whereas the increase in leakage current is over 2 orders of magnitude. The change in capacitance when going between the thin and thick high-k capacitors is much larger, and the leakage current change is also much smaller, when compared to the silicon dioxide capacitors. The HfO_2 with TiN gate for example, has an increase in capacitance of almost a factor of 10 with the same two orders of magnitude increase of leakage current, as seen by the silicon dioxide capacitor. The thickness of the high-k dielectric film allows for a trade off between capacitance value and leakage current.

4.2.4 TiN/HfO$_x$/Si Capacitor

It was concluded that the structure with the best trade off between leakage current, interfacial layers, capacitance values and high-k value was the hafnium oxide with the TiN top electrode. In order to understand how this capacitor compares with previous devices fabricated by other researchers, Table 4.5 contains the leakage current and accumulation capacitance values taken from a literature, and is compared with our TiN/HfO_2(10nm)/Si capacitor. The devices listed in Table 4.5 have similar structures as our MOS capacitors, however the fabrication process does vary, as do the materials and dimensions. This must be taken into consideration as a direct comparison of the devices might not be applicable.

The TiN/HfO_2(10nm)/Si device fabricated as part of the MOS capacitor batch has a leakage current density comparable to similar devices reported in literature. Although the current density is many orders of magnitude higher than [144], it is of the same order of magnitude as [145] and is an order of magnitude smaller than [146]. The device described in [144] has two aluminium oxide interlayers between the hafnium oxide and titanium nitride, where it is reported that devices without inter layers result in increased leakage current. This is apparent and can be seen when comparing this device with the other devices without interface layers in Table 4.5. For this reason, this leakage current value will be dismissed when compared to the TiN/HfO_2(10nm)/Si device. The device described in this report, TiN/HfO_2(10nm)/Si, shows better or similar levels of leakage current when compared to other high-k MOS capacitors as described in [145–147].

high-k	metal gate	EOT [nm]	J[A/cm^2] at 1V	C$_{accum}$ [μF/cm^2]	Paper Reference
HfO_2	TiN	1.9	0.4	1.8	from this report
HfO_2	TiN	1.7	1×10^{-9}	0.8	[144]
HfO_2	TiN	0.8	10	3	[146]
HfO_2	poly-Si	1.2	0.001	n/a	[147]
HfO_2	TaN	1.0	0.1	n/a	[145]

Table 4.5: Leakage current density and capacitance values from literature review compared to device from MOS capacitor batch

The capacitance per unit area, taken at accumulation, of the devices was only reported in two of the literature review papers in Table 4.5. Unfortunately the other papers do not specify the areas of the devices. Nevertheless, the capacitance/area of the TiN/HfO_2(10nm)/Si device in this report can be seen to be of the same order of magnitude as other devices in the table, with similar structures.

This comparison to literature shows that the TiN/HfO_2(10nm)/Si device fabricated in the MOS capacitor batch has resulted in a high capacitance, low leakage capacitor, with electrical characteristics similar, and in some cases better, than other reported devices. This verifies the success of the fabrication process and indicates deposition of good quality high-k dielectrics.

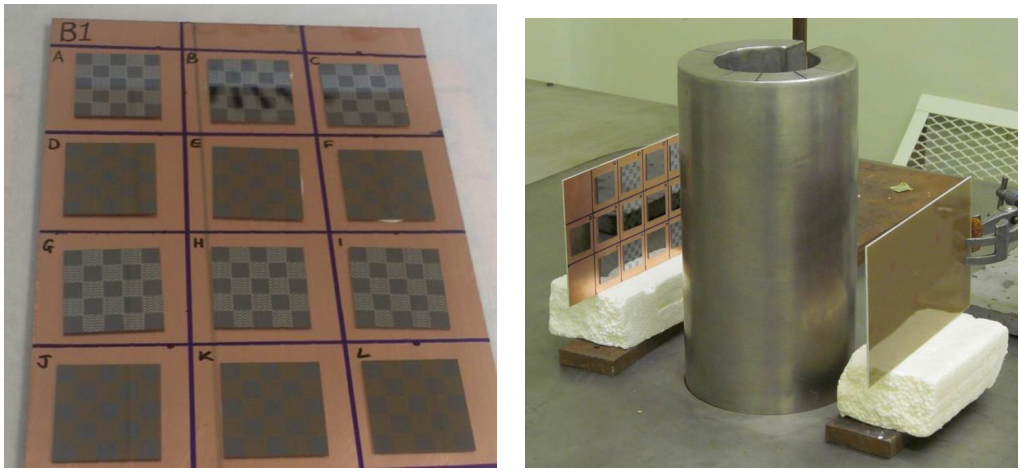
4.3 Irradiation of Capacitors

In order to understand the breakdown and effects of radiation on high-k capacitors, the pre-irradiation C-V curves can be compared to the post-irradiation C-V curves. The irradiation setup is explained first, followed by the C-V analysis performed on the post radiation results.

The irradiation of the high-k metal gate capacitors was conducted at Cranfield University, at the JJ Thomson Irradiation Laboratory. The radiation source is a Cobalt $-$ 60 (Co^{60}) gamma source where the dose rate at the time of radiation was 500 krads(Si)/hr. The dosimetry is certified to +/-5 percent by a dosemeter. The set-up requires the devices to be a set distance in height and laterally away from the source, where the source consists of nuggets of Co^{60}, positioned at different locations in a cylinder.

The MOS capacitor batch consisted of 12 different capacitor types, all to be irradiated to five different doses, ranging from 50 krad(Si) to 3 Mrad(Si). In order to irradiate the capacitors at the varied doses, each wafer was diced up into 2×2 cm^2 pieces. A piece from every wafer, and therefore every type of capacitor, was adhered to a piece of copper coated FR4 board using silver epoxy, one board for each dose. This resulted in 5 boards, one for each dose, each with 12 wafer pieces on it which is shown in Figure 4.12(a). After irradiation, C-V measurements were undertaken on four different sized capacitors that had previously been measured, on each type of capacitor, on each wafer piece that was adhered to each board.

In order to achieve the dose rate of 500 krads(Si)/hr, the boards had to be positioned at a certain height and distance away from the source. The set-up can be seen in Figure 4.12(b), where two boards were positioned at equal distances away. The board were exposed to the source for varying amounts of time. Table 4.6 shows the total dose amounts of each board, along with the time left in the chamber.



(a) (b)

Figure 4.12: Radiation setup showing (a) 12 different capacitor structures diced and adhered to copper covered FR4 board and (b) source layout and board positions.

Board Identification	Dose Rate [rads(Si)/hr]	Irradiation Time	Total Dose [rads(Si)]
1	500k	6 mins	50k
2	500k	15 mins	125k
3	500k	1 hr	500k
4	500k	2 hrs	1M
5	500k	6 hrs	3M

Table 4.6: Radiation Test Parameters

As all the capacitors were adhered across all locations of the board, some on the outer edge, some in the centre, when the board was positioned perpendicular to the source, the outer edges of the board were further away from the source, resulting in a lower dose rate. The source had been modelled by staff at the radiation facility and the variation was found to be negligible.

The capacitors were irradiated, unbiased. Previous work, including radiation of BOX oxides by myself and colleagues, show clear radiation shifts in CV characteristics in the unbiased state [31, 47, 148, 149]. In order to perform biased measurements at the radiation facility, a new, more complex, mask design would be needed resulting in a new and lengthy fabrication process. For both the reasons stated here, it was decided to undertake the radiation in the unbiased state.

Following irradiation, the capacitors were transported back to University of Southampton, where the post irradiation C-V measurements were undertaken. The time between irradiation and measurement was recorded for each capacitor with the time being kept to a minimum, where possible, reducing annealing effects.

4.3.1 Capacitor Analysis

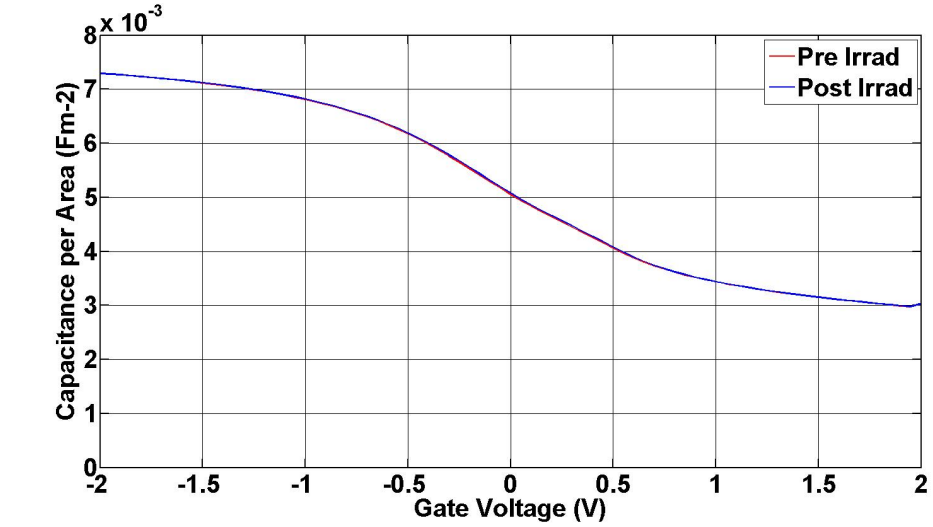
All capacitors were irradiated, followed by C-V measurements using the same set-up as described for the pre irradiation C-V measurements. Comparing with pre-irradiation results, the voltage shift was extracted for each capacitor, where the voltage shift was taken for the aluminium topped capacitors at half the maximum capacitance, whereas the TiN topped capacitors had the voltage shift measured at a quarter of the maximum capacitance. This technique reduced the effect of the double hump, seen in the TiN topped capacitors. It must be noted however that the difference in voltage extraction techniques will not affect the analysis of the results as the extracted parameter is a shift, and not a specific value on the C-V curves.

Typical pre and post radiation C-V curves can be seen in Figure 4.13(a) and Figure 4.13(b), showing the silicon dioxide at 500 krads(Si) and the hafnium oxide at 1Mrad(Si) respectively, both with TiN electrodes. As can be seen, there is little radiation shift observed.

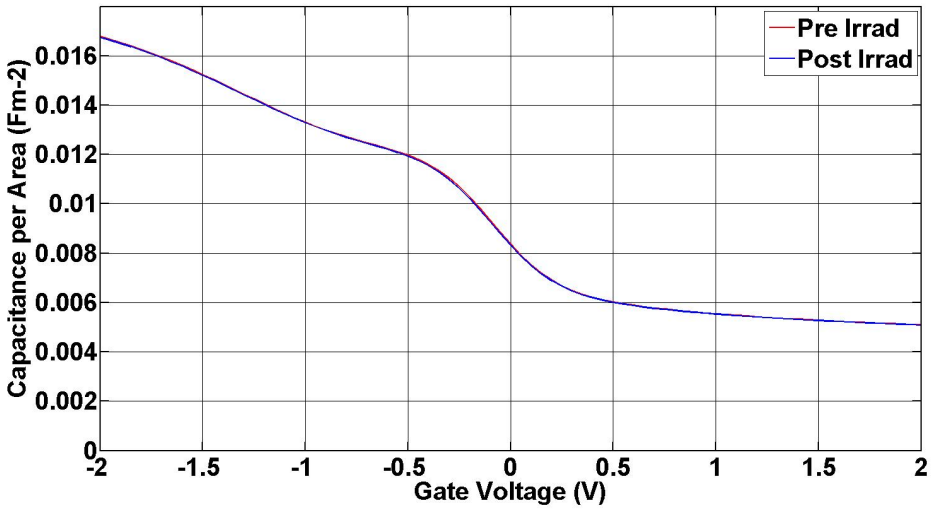
Due to the many capacitors that were measured, the average voltage shift for each dose will be taken across all sized capacitors, for each different type of capacitor structure. The size of the capacitor will not have an affect on the voltage shift due to radiation, enabling this average to be taken. In order to take into account the variability in the measurements of the capacitors and the variability in the measurement tool itself, the standard deviation was calculated for the differently sized capacitors. This results in a standard deviation value for pre radiation, post radiation and an average voltage shift for each capacitor structure type, at the 5 different doses.

The analysis on the thinner oxides was more challenging as many of the capacitors, especially the silicon dioxide 3 nm capacitors, had unreliable C-V curves. At very small thicknesss, the variability across the device and control of the oxide becomes difficult and the type of oxide deposited can be treated more of as an interface, rather than a bulk oxide. A lot of the C-V curves showed non-capacitive behaviour either before and/or after radiation, and many of the capacitors had permanent breakdowns between the pre and post C-V measurements. This limited the amount of data that could be taken for the thin oxides, where the voltage shift and/or a standard deviation value could not be calculated. A comparison between the device structures was unable to be completed for the thinner oxides. Most of the thicker oxides however did not face the same issues as seen in the thinner oxide capacitors, allowing a full analysis to be completed for the different types of structures.

The only type of thick oxide structure that was unable to be analysed was the 6 nm silicon dioxide capacitor with an aluminium electrode. Over half of the capacitors measured with this structure exhibited non-capacitive behaviour. This is most likely due to the reaction between aluminium and silicon dioxide. The EOT of the silicon dioxide



(a)



(b)

Figure 4.13: C-V curves before and after irradiation for the TiN with (a) 6 nm SiO_2 (b) 10 nm HfO_2, irradiated to a dose of 500 krads(Si), with capacitor size=200 $\times$ 200 μm^2.

capacitors with aluminium both show a value of over 10 nm. As mentioned previously, the aluminium showed high reactivity with the oxides. This reaction between the silicon dioxide and aluminium may have resulted in a very thin bulk oxide layer. This is most likely why the capacitors with these structures were no longer capacitive, even with the thicker initial deposited silicon dioxide layer. The high-k capacitors with the TiN electrodes are the most stable capacitors and will provide the best analysis for radiation effects.

The thickest oxide capacitors, with the highest dose will theoretically give the largest

shift and therefore if any radiation effects occur, they will be easily measured in the thicker oxides. Table 4.7 contains the results for the standard deviation and average voltage shifts for 3Mrad(Si) for the three oxide types with TiN electrodes.

high-k	metal top electrode	t_{ox} [nm]	Pre Std Dev [mV] (Pre-rad)	Post Std Dev [mV] (Post-rad)	Average ΔV[mV]
SiO_2	TiN	6	33	119	16
Al_2O_3	TiN	10	23	113	8
HfO_2	TiN	10	89	61	23

Table 4.7: Post 3Mrad(Si) Radiation Shifts for thickest oxides, averaged over 4 varied sized capacitors

The variation in the C-V curves, across the capacitors, is given by the standard deviation before and after the radiation. If this standard deviation is larger than the radiation shift, the radiation shift will not be measurable. Only voltage shifts that are greater than the standard deviation may be taken as true radiation shifts. The results shown in Table 4.7 show that the standard deviation for all types of oxide is greater than the measured shifts. This means the voltage shift measured cannot be treated as a radiation effect; rather it is a result of the measurement tool variation, or general variability seen from one measurement to the next i.e. lifting/placing of the probes etc. Even though the radiation shift cannot be directly measured, these capacitors can be treated as radiation hard with a value of < 120 mV, < 110 mV and < 90 mV for the silicon dioxide, aluminium oxide and hafnium oxide respectively, when irradiated with gamma radiation, at a dose of 3Mrad(Si).

As these capacitors were irradiated to the highest dose, and the radiation shift was smaller than the standard deviation, then theoretically the other total dose values should also follow the same trend. If the radiation shift at 3 Mrad(Si) was smaller than the standard deviation, this should also be the case at 50 krads(Si). Table 4.8 shows the results for the same set of capacitors as Table 4.7, but this time irradiated at the smallest dose of 50 krads(Si).

high-k	metal top electrode	t_{ox} [nm]	Pre Std Dev [mV] (Pre-rad)	Post Std Dev [mV] (Post-rad)	Average ΔV[mV]
SiO_2	TiN	6	39	70	67
Al_2O_3	TiN	10	31	106	57
HfO_2	TiN	10	7	32	92

Table 4.8: Post 50 krads(Si) Radiation Shifts for thickest oxides, averaged over 4 varied sized capacitors

The silicon dioxide and aluminium oxide both show similar results to the 3Mrad(Si) dose, where the standard deviation is larger than the voltage shift seen. The standard deviation is within the same order of magnitude as the 3 Mrad(Si), which is expected due to the standard deviation being unrelated to the radiation effects. These capacitors can be said to be radiation hard up to < 70 mV, < 110 mV for silicon dioxide and

aluminium oxide respectively for up to 50 krads(Si). These results show that there is also no scaling or pattern seen with increasing dose, verifying the shifts seen here are not pure radiation effects. The hafnium oxide device here shows a larger voltage shift than standard deviation, but they are still within the same order of magnitude. This shift can still be treated as an effect of the measurement variations as this value is still at similar levels to the standard deviation seen for the previous set of results, and therefore cannot be definitely identified as a radiation effect.

Table 4.8 and Table 4.7 both show that the hafnium oxide and aluminium oxide capacitors do not show a significant decrease in radiation hardness when compared to silicon dioxide capacitors. This can be explained by using the theory of trapping, used to describe the degradation process in silicon dioxide, described in Section 2.4.1. This theory states that the voltage shift due to oxide traps is dependent on the oxide thickness squared, as shown in Equation 2.22. We can hence conclude the average increase in trapping of holes in the high-k dielectric, as given by f_{ot} in Equation 2.22, is relatively small.

Dose [Mrad(Si)]	high-k	metal top electrode	t_{ox} [nm]	ΔV_{mg}[mV]	Reference
3	HfO_2	TiN	10	<100	this work
10	HfO_2	TiN	10	400	[148]
3	HfO_2	Al	6.8	110	[150]
3	SiO_2	Al	10	30	[150]
3	Al_2O_3	Al	5	8	[150]
3	Al_2O_3	Al	10	450	[149]

Table 4.9: Radiation shifts for variety of devices from literature in comparison to TiN/HfO_x from this work.

When oxide thicknesses tend towards sub-nanometre regimes, as in gate oxides in MOSFETs, the oxide traps and shift due to these become negligible. This is especially true when devices such as SOI MOSFETs are considered. Other, much thicker oxides exist in these structures, including field oxides and the buried oxides (BOX). When these oxides are present, the voltage shifts and effects due to the oxide traps in these other oxides, will be orders of magnitude larger than the effects caused by oxide traps in the nanometre thick gate oxide. Therefore it can be said that at this nanometre regime, high-k MOS capacitors are essentially radiation hard and are as radiation tolerant as the silicon dioxide MOS capacitor. It can be concluded that high-k layers can be considered as a replacement for silicon dioxide layers used as gate oxide replacements in SOI MOSFETs.

Similar experimental set-ups have been conducted and reported in literature where similar doses, oxide materials, oxide thicknesses and top electrode materials were used, where the mid-gap voltage shift was measured. The results from these papers are presented in Table 4.9. As can be seen, the results shown in Table 4.7, fabricated at University of Southampton, have maximum voltage shifts that are similar, or in some cases, smaller

than other reported devices. As stated, the radiation shifts listed for the Southampton capacitors are a maximum value, where the radiation shift could actually be much less than this value, putting the capacitors at a radiation hardness level equal for the worst case scenario or better than the reported devices here.

From these results it can be said that the hafnium oxide capacitor with the titanium nitride electrode is the most reliable and radiation hardened capacitor fabricated in this batch, with a hardness level, to the nearest order of magnitude, of < 100 mV for up to 3 Mrad(Si) gamma radiation.

4.4 Summary

A batch of high-k MOS capacitors were fabricated, with aluminium oxide and hafnium oxide as the insulator layers with a reference silicon dioxide batch. All capacitors had TiN or Al for the top gate electrode. C-V analysis, pre-irradiation, indicated good quality high-k dielectrics had been fabricated. In particular, the capacitor structure with the best capacitive behaviour is the TiN/HfO_2/Si structure, with a total equivalent oxide thickness of 1.8 nm for a physical thickness of 10 nm. The EOT of the interface is found to be 0.6 nm, less than half the total EOT, indicating little reactivity between the metal electrode and the high-k material. The high quality of the TiN top electrode is seen clearly when compared to the much higher interface EOT value of 2.2 nm which is produced when the top electrode is Al.

The leakage current properties of TiN/HfO_x/Si capacitors indicates the high quality of the high-k layer. The change in maximum capacitance between the thin and thick TiN/HfO_2/Si structure gives an increase of capacitance of almost a factor of 10, with only two orders of magnitude increase in leakage current. Comparing this with the silicon dioxide capacitor, doubling the thickness results only in a 10 percent increase in capacitance, with the same increase of two orders of magnitude in leakage current. A trade off between capacitance value and leakage current is possible for the TiN/HfO_2/Si structured capacitor, an important factor in the device output. Comparing the TiN/HfO_2/Si structure with literature showed leakage currents and capacitance values with the same order of magnitude as other similar structures [144–147], verifying the successful fabrication process for high-k dielectrics. The superior capacitive qualities of the HfO_2 capacitors with TiN electrode indicate that the traditional poly-Si/SiO_2 gate structures can be replaced with this HKMG stack, enabling scaling limitations of MOS devices to be overcome. Using TiN/HfO_2 structures will return MOS devices back in line with ITRS roadmap predictions.

All the capacitors were irradiated up to 3Mrad(Si) using a Co-60 source. The high-k MOS capacitors have the same order of magnitude voltage shifts as the silicon dioxide MOS capacitors showing that the high-k materials do not face a reduction in radiation hardness, despite the difference in material and trapping properties. The TiN/HfO_2/Si device is radiation hard to a level of < 100 mV to the nearest order of magnitude, up to 3 Mrad(Si) of gamma radiation. It can therefore be concluded that the high-k MOS capacitors are as radiation hard as the silicon dioxide MOS capacitors. Replacing the gate oxide in devices such as MOSFETs, with these good quality high-k dielectrics will have little reduction in radiation hardness, especially when accounting for the radiation damage caused by the much thicker BOX and field oxides. This means the move towards HKMG can now be realised in radiation environments, enabling companies working in harsh environments to overcome scaling issues.

Chapter 5

Switching Mechanics and Radiation Hardness of HfO_x VCM Resistive Memory

Resistive memory has the potential to become a new type of non-volatile memory with high density, low power and simple metal-insulator-metal structure [151]. Different materials have been used for the dielectric layer but hafnium oxide in particular has shown promising switching characteristics [101–103]. This work will investigate hafnium oxide VCM cells, whereby resistive switching occurs due to the movement of oxygen vacancies. Three different effects have been studied: the effect of TiN stoichiometry on resistive switching in Section 5.2 as published in [152], the effect of HfO_x stoichiometry on resistive switching in Section 5.3 as published in [153] and the radiation effects on varied stoichiometry in Section 5.4 as published in [154].

For metal oxide VCM RRAM, the switching properties have reportedly shown to be affected by the electrode material type [101, 155] and the interfacial layers between the oxide and electrode layers [103, 156, 157]. However, little work has been conducted on investigating the stoichiometry of the electrodes. It has been proposed here that the stoichiometry of the electrodes will directly alter the interfacial layers and therefore the switching properties of resistive memory cells. $TiN/HfO_x/TiN$ memory cells, using electrodes with two different stoichiometries via different sputtering techniques, have been fabricated and analysed. This is shown in Section 5.2.

Previous investigations have also been conducted into the role of the VCM switching material [156]. Further work has been performed, concentrating on role of oxygen ions within metal oxide materials, varying the amount of oxygen that the device is exposed to during deposition [158–160]. $TiN/HfO_x/TiN$ memory cells with different hafnium oxide stoichiometries, have been fabricated and analysed through varying the ALD temperature. This is shown in Section 5.3.

Limitations of current semiconductor memories exist in terms of ionizing radiation hardness. For VCM RRAM cells, the thin layers of oxide could potentially result in radiation hardened memory by process. The varying stoichiometries within this work will enable the ionizing radiation response to be further understood, in relation to oxygen concentration. This is discussed in Section 5.4.

5.1 Resistive Memory Cell Structure

The device structure for resistive memory cells consist of a bottom contact, followed by a dielectric layer, followed by a top contact, forming a MIM structure as shown in Figure 5.1.

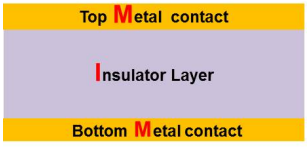


Figure 5.1: MIM structure for RRAM cell.

In order to fabricated RRAM cells from MIM structures, certain requirements need to be met. For fabrication purposes, the MIM structure needs to be constructed on top of a base wafer used for mechanical stability. For this, a silicon wafer is used. Another requirement occurs due to the way these devices are measured electrically, requiring access to both the top and bottom contacts. The final requirement is that multiple RRAM cells are fabricated on the same wafer, resulting in the need for isolation from one RRAM cell to the other. Therefore a mask has been designed allowing for each memory cell to be defined, separate from one another and with access to both contacts, on a silicon base wafer.

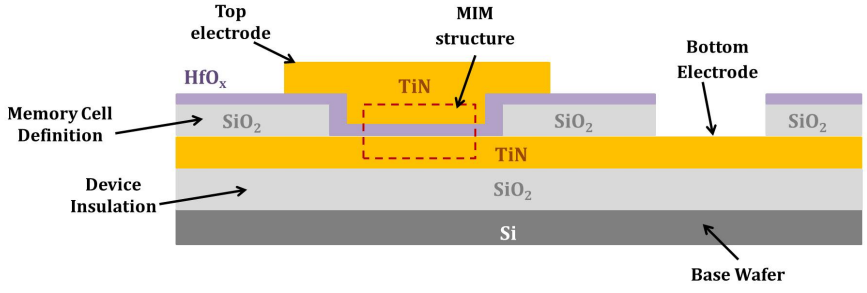


Figure 5.2: MIM structure within RRAM cell structure, with bottom electrode access shown.

The cross-section of a typical RRAM cell is shown in Figure 5.2. The upper silicon dioxide layer is what is used to define and isolate individual memory cells and is also removed in certain areas, to allow access to the bottom electrode. The MIM structure

is created in the silicon dioxide openings as highlighted in Figure 5.2. The lower silicon dioxide layer is used solely as electrical insulation of the MIM structure from the base wafer.

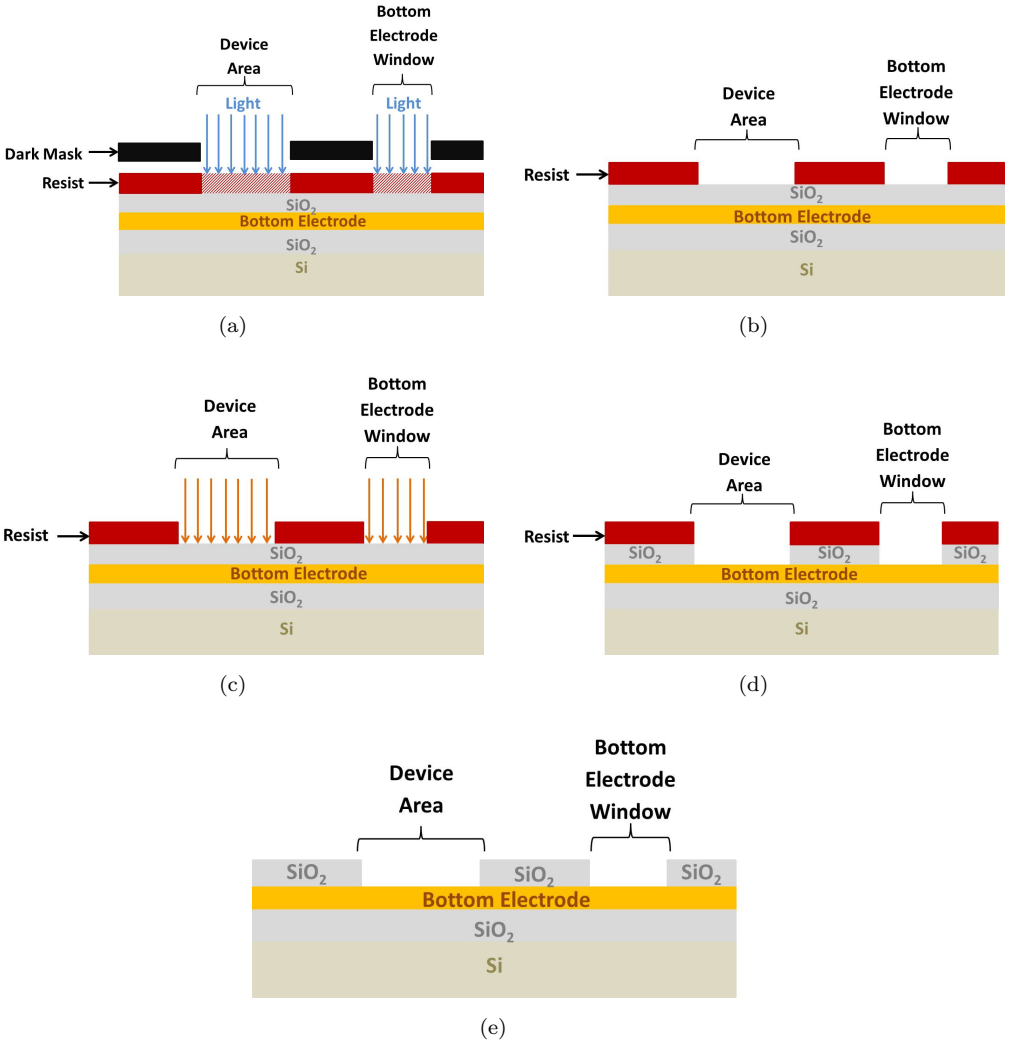


Figure 5.3: Lithography process using first mask to define the RRAM cell areas and access to bottom electrode: (a) resist deposited and patterned on top of silicon dioxide layer (b) resist after lithography showing open areas for the device area and access to the bottom electrode (c) etch of silicon dioxide layer (d) exposed silicon dioxide removed from etch (e) resist stripped leaving RRAM area and bottom electrode window .

In order to fabricate this device layout, the first stage is to deposit the lower silicon dioxide layer followed by the bottom electrode layer. Following this the upper silicon dioxide layer is deposited. It is at this stage that the openings for the RRAM cell areas and access to the bottom electrode is created through removal of certain areas of the silicon dioxide, using lithography as shown in Figure 5.3. Resist is used to define the areas that will be removed through etching, forming the RRAM areas and bottom

electrode access. This lithography mask is designed so that there are various sizes of open areas resulting in various sizes of RRAM cells, ranging from 1 μm to 100 μm.

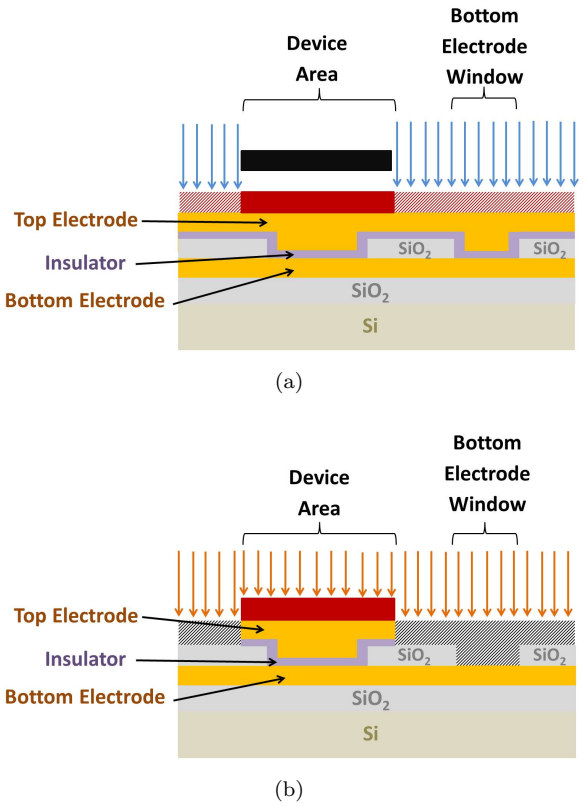


Figure 5.4: Resistive memory cell top contact process showing (a) resist exposure with light mask followed by (b) a dry etch.

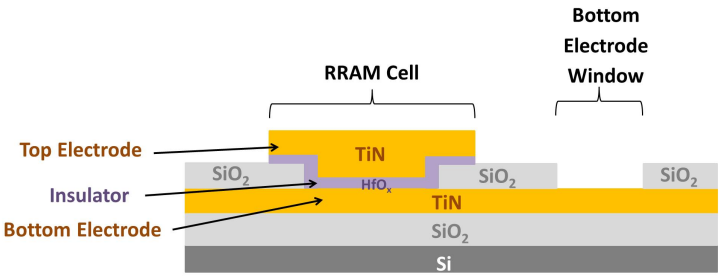


Figure 5.5: Structure of typical memory cell showing RRAM cell area and access to bottom window.

In order to create the MIM structure, hafnium oxide and TiN is deposited over the whole wafer. The next stage is to pattern and etch the top electrode in order to define each individual RRAM cell and gain access to the bottom electrode again. This is done using a second mask. After patterning the wafer, resist remains in the areas above the RRAM cell openings and protects these areas from the following etch. The remaining areas of the wafer, including the window for the bottom electrode access, is etched. This process is shown in Figure 5.4. The result is the RRAM cell structure and access to bottom electrode as shown in Figure 5.5.

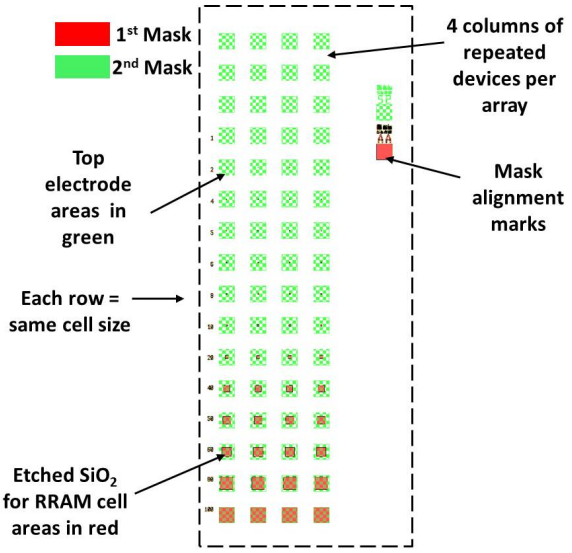


Figure 5.6: RRAM Chip Mask Layout with bottom electrode accessible by two windows (red) and top contact area highlighted (green).

The device layout and the two masks used, the first for the silicon dioxide etch and the second for the top electrode etch, are shown in Figure 5.6. Here, four columns of identical devices can be seen with the rows showing different sizes of RRAM cells. The red areas signify the etched silicon dioxide areas by using the first mask. The green areas signify the top electrode areas by using the second mask.

The I-V RRAM cell measurements are performed using an Agilent B1500 semiconductor analyser with I-V capability, attached to a probing station with a microscope to enable placing of the probes. Two probes are used for the I-V measurements, where one probe is placed on the bottom electrode window and the other is placed on the device top electrodes. DC sweep and pulsed measurements can be performed although the minimum pulsed width was limited to 500 μs. The pulse width and pulse amplitude can be defined by user.

5.2 Effect of Stoichiometry of TiN on Resistive Switching

An investigation was conducted into the effects of the electrode stoichiometry on the switching properties of RRAM cells.

For metal oxide RRAM, with an oxygen vacancy switching mechanism, the switching properties have reportedly shown heavy relation to the electrode material type [101,155] and the interfacial layers between the oxide switching layer and electrodes [103,156,157]. It seems obvious that the stoichiometry of the switching oxide layer is an important factor to the oxygen vacancy switching mechanism, although little work has been done on investigating the stoichiometry of the electrodes.

It is proposed that the stoichiometry of the electrodes will directly alter the interfacial layers and therefore the switching properties of resistive memory cells. This was investigated using two different sputtering techniques for the top TiN electrode.

5.2.1 Resistive Cell Dimensions

Table 5.1 lists the dimensions and processes used for these resistive memory cells. The development and characterisation of the two sputtered techniques for TiN is explained in Chapter 3. The hafnium oxide recipe used was the HfO_x recipe, described in Table 3.1.

Layer	Fabrication Technique	Thickness (nm)
SiO_2 isolation layer	reactively sputtered	500
TiN bottom electrode	reactively sputtered	200
SiO_2 device definition	reactively sputtered	200
HfO_x	ALD (initial HfO_x recipe)	10
TiN top electrode	reactively/non-reactively sputtered	200

Table 5.1: Dimensions and fabrication techniques used to create TiN/HfO_x/TiN resistive memory cell structure for investigation of stoichiometry of top electrode. First layer in the table describes first layer deposited.

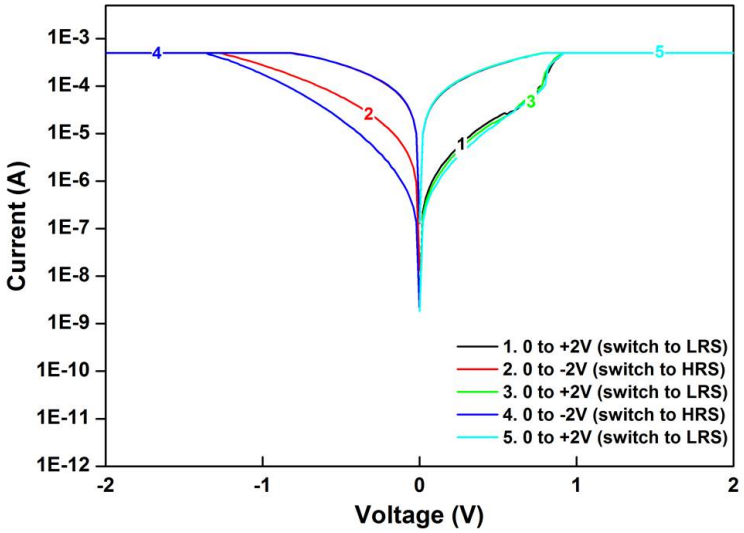
5.2.2 Electrical Characterisation

The TiN/HfO_x/TiN resistive memory cells were electrically measured, at room temperature, using the Agilent B1500A semiconductor analyser system. DC sweep measurements were performed. Typical IV measurements can be seen in Figure 5.7 for reactive and non-reactive sputtered TiN. The reactive sputtered device exhibits bipolar switching with an R_{OFF}/R_{ON} >10, with SET in positive voltage and RESET in negative voltage. The non-reactively sputtered device shows unipolar switching, with R_{OFF}/R_{ON} $\sim 10^3$ but with large variability in sweeps.

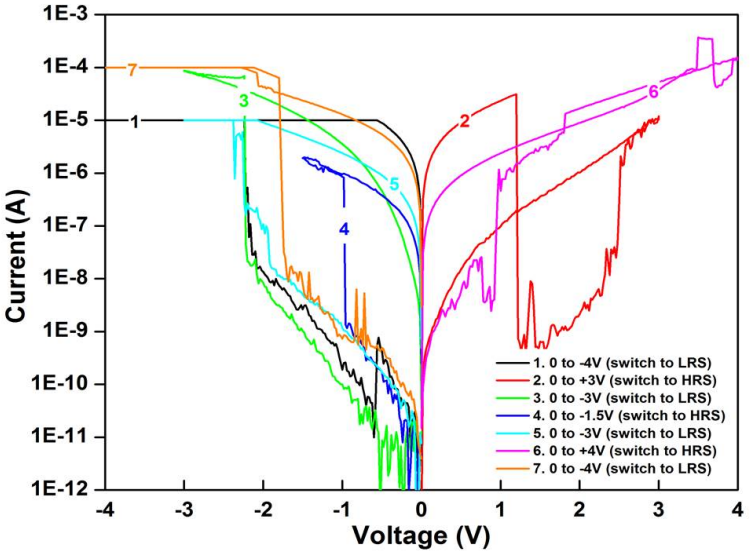
The difference in switching properties seen for these memory cells support the theory of oxygen vacancy related switching mechanism [12]. Table 5.2 summarises the difference of electrode characterisation on Si and Table 5.3 summarises device electrical characteristics for TiN/HfO_x/TiN RRAM cells with different sputtering methods for the top electrode.

Sputter Technique	**Oxygen Percentage**	
	EDX	**XPS**
Reactive	0	16
Non-reactive	23	39

Table 5.2: Material characterisation of TiN/Si samples for two sputtering techniques.



(a)



(b)

Figure 5.7: DC voltage sweep measurements for TiN RRAM cells, at room temperature, showing (a) Reactively-sputtered TiN device showing bipolar behaviour with R_{OFF}/R_{ON} >10. and (b) Non-reactively-sputtered TiN device showing unipolar behaviour with R_{OFF}/R_{ON} $\sim 10^3$. (HfO_x recipe parameters used are: T_{table}=300 $^{\circ}C$, t_{plasma}=2 s, P_{plasma}=250 W, t_{TEMAH}=1.5 s, t_{PURGE}=8 s and P_{O_2}=80 mT.)

The material characterisation was performed on a silicon substrate. When the TiN layers are deposited onto HfO_X, as in the RRAM device case, the reactions will differ depending on the TiN material properties and therefore sputtering technique. The non-reactive sputtering technique deposits titanium oxy-nitride onto the HfO_x resulting in little reaction between the two layers, due to the already oxidized titanium nitride, prior to deposition. The reactively sputtered technique begins with titanium deposition onto

Sputter Technique	**Electrical Characterisation**			
	Behaviour	$\mathbf{R}_{ON}(\Omega)$	$\mathbf{R}_{OFF}(\Omega)$	$\mathbf{R}_{OFF}/\mathbf{R}_{ON}$
Reactive	Bipolar	$2.0\pm0.3\text{x}10^{3}$	$9\pm1\text{x}10^{4}$	$5\pm1\text{x}10^{1}$
Non-reactive	Unipolar	$2\pm1\text{x}10^{6}$	$5\pm3\text{x}10^{9}$	$3\pm2\text{x}10^{3}$

Table 5.3: Electrical characterisation of TiN/HfO_x/TiN RRAM cells for two sputtering techniques.

the HfO_x layer. This titanium layer will most likely oxidized before the nitrogen plasma is introduced to the chamber, resulting in a TiO_xN_y interfacial layer. The formation of this interfacial layer will cause oxygen to be drawn out from the switching layer below, leaving hind an increased number of oxygen vacancies. This increase in oxygen vacancies in the switching layer can explain the reduced R_{OFF} value observed for the reactively sputtered TiN device, along with the bipolar switching behaviour [65].

The non-reactively sputtered electrode will have little reaction with the HfO_x beneath, leading to fewer oxygen vacancies in the switching layer, resulting in a higher R_{OFF} and unipolar switching behaviour. The variability between switches seen in this device is large, as shown by the large standard deviation values in Table 5.3. Despite the large R_{OFF}/R_{ON} ratio and low OFF state current, this device does not show successful repeatable or reliable switching due to large variation in IV characteristics. This variation most probably originates form the uncontrolled deposition technique where the top TiN electrode oxidized during deposition, from an unknown source. This work shows reproducible switching can be achieved using reactive sputtering, despite smaller R_{OFF}/R_{ON}, resulting in more reliable RRAM cells. This investigation also verifies the switching mechanism seen within metal oxides is related to oxygen vacancies and redox-based reactions.

The role of the top electrode and stoichiometry has been investigated. Reactive sputtering will now be used as the top electrode deposition choice. The next batch of RRAM memory cells were fabricated to investigate the effect of stoichiometry of the switching layer.

5.3 Effect of Stoichiometry of HfO_x on Resistive Switching

TiN/HfO_x/TiN resistive RAM cells have been fabricated with stoichiometry of the HfO_x layer altered through control of atomic layer deposition temperature. This work was presented at the Internal Symposium on Circuits and Systems (ISCAS) 2014 and published in the proceedings [153].

Previous investigations into the role of the electrode and insulator material types have been conducted with particular attention paid to the interfacial layers that form between these layers [101, 152, 155, 156]. Other papers have also investigated the role of oxygen

ions within insulator materials, varying the amount of oxygen that the device is exposed to during deposition [158–160]. Improvement in switching properties have been seen for an increase in the number of oxygen vacancies [103, 156, 157].

The stoichiometry of the hafnium oxide layers are altered through changing the table temperature. These temperatures are 300 °C, 350 °C and 400 °C. Sweep and pulsed electrical characterisation were conducted allowing the effects of the stoichiometry on the switching characteristics to be viewed.

Table 5.4 lists the dimensions and processes used for these resistive memory cells. The development and characterisation of the hafnium oxide layers deposited at different temperatures is explained in Chapter 3. The material characterisation has been summarised in Table 5.5. The hafnium oxide recipe used was the initial HfO_x recipe, with parameters listed in Table 3.1, but with a new TEMAH source supply used.

Layer	Fabrication Technique	Thickness (nm)
SiO_2 isolation layer	reactively sputtered	500
TiN bottom electrode	reactively sputtered	250
SiO_2 device definition	reactively sputtered	200
HfO_x	atomic layer deposition	50
TiN top electrode	reactively sputtered	125

Table 5.4: Dimensions and fabrication techniques used to create TiN/HfO_x/TiN resistive memory device structure for investigation of stoichiometry of hafnium oxide. First layer in the table describes first layer deposited.

Characterisation Technique	**ALD Deposition Temperature (°C)**		
	300	**350**	**400**
SEM: HfO_x thickness (nm)	48	50	63
XRD: HfO_x structure	cubic	cubic	monoclinic
XPS: HfO_x, x=	1.78±0.05	1.99±0.05	1.95±0.05

Table 5.5: Material characterisation for HfO_x as a function of atomic layer deposition temperature.

5.3.1 Electrical Characterisation

DC voltage sweep measurements were conducted, at room temperature, using a B1500A semiconductor analyser, using the set-up previously described. Each type of device with varying atomic layer deposition temperature had ten cells measured per area; 5x5 μm^2, 10x10 μm^2, 20x20 μm^2. Therefore there were 30 cells per device type for voltage sweep and another 30 cells for voltage pulsed measurements. The cell with the hafnium oxide deposited at 400 °C did not exhibit switching behaviour. This could be attributed to the monoclinic crystal structure, compared to successful resistive switching seen for cubic structures obtained at 300 °C and 350 °C. This shows agreement with the theory of

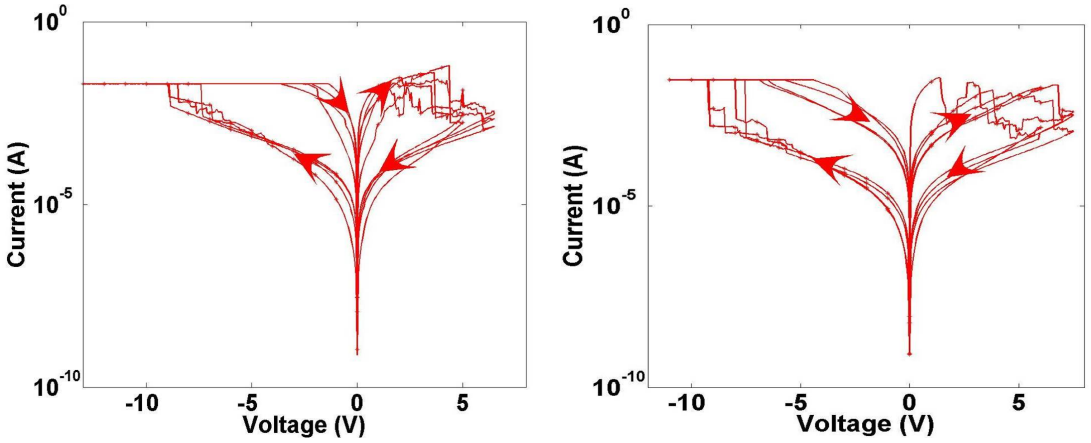
ionic migration whereby oxygen vacancy transport, depends on the crystal structure of the device, resulting in a change in switching characteristics [161].

The favourable crystal structure in terms of optimum resistive switching properties is still unknown. Reliable switching has been reported in monoclinic films [162], whereas it has also been reported in amorphous films with degradation seen when these films were annealed into a monoclinic structure [163]. Further research into effects of crystallization on switching kinetics is needed to fully understand the effects and mechanism.

DC Sweep Parameter	**ALD Deposition Temperature (°C)**	
	300	**350**
Average V_{SET} (V)	-8.4	-8.5
Average V_{RESET} (V)	+3.5	+5.1
Average R_{OFF} (Ω)	$1.8x10^4$	$7.7x10^4$
Average R_{ON} (Ω)	$3.5x10^2$	$1.5x10^3$
Average R_{OFF}/R_{ON}	50	52

Table 5.6: DC sweep results showing switching parameters at different ALD deposition temperatures.

Good switching characteristics were obtained for memory cells with the hafnium oxide layer deposited 300 °C and 350 °C. A current compliance of 20 mA and 30 mA were used for 300 °C and 350 °C, respectively. Forming voltage for a typical 300 °C cell is -18 V and for a typical 350 °C cell is -17 V. Figure 5.8(a) and Figure 5.8(b) show typical switching characteristics with two distinct resistance states for memory cells with deposition temperatures of 300 °C and 350 °C, respectively.



(a) (b)

Figure 5.8: DC sweep measurements for memory cells, at room temperature, with ALD deposition temperature of(a) 300 °C and (b) 350 °C, showing reproducible voltage sweeps with arrows showing direction of sweep. (HfO_x recipe parameters used are: T_{table}=300 °C, t_{plasma}=2 s, P_{plasma}=250 W, t_{TEMAH}=1.5 s, t_{PURGE}=8 s, P_{O_2}=80 mT with a new TEMAH source.)

Table 5.6 shows the R_{OFF} and R_{ON} values for the presented cells, along with the R_{OFF}/R_{ON} values. All other cells exhibit similar electrical characteristics to those shown in Figure 5.8(a) and Figure 5.8(b), with no variations seen with area. The most remarkable thing to note is the memory characteristics are similar even though one type of device is sub-stoichiometric. A box plot can be seen in Figure 5.9 whereby the median, first and third quartiles for V_{RESET} and V_{SET} are displayed. This plot displays the statistics of over 30 cells of each temperature.

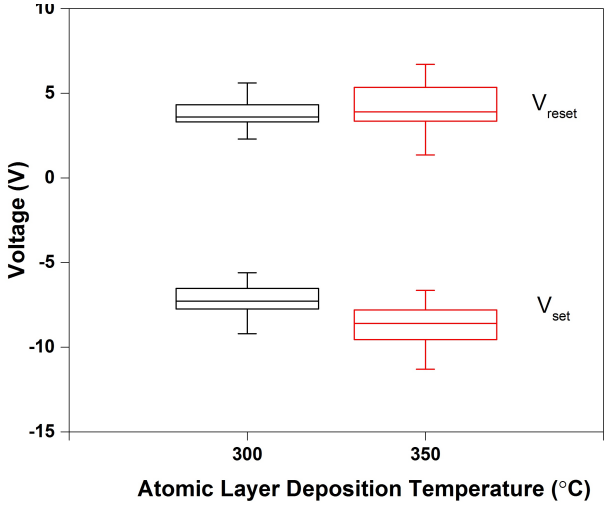


Figure 5.9: Box plot showing median, first and third quartiles. The whiskers show the data points that are beyond the quartiles by 1.5 interquartile range (outliers). This box plot shows the reset and set voltages for 30 memory cells measured at room temperature, of each atomic layer deposition temperature.

Voltage pulse measurements were carried out on cells, at room temperature, using a 50 ms pulse width and a 50 mA current compliance. The switching regime used to switch the 300 °C memory cell was a reset voltage scheme of +2 V, +4 V, +6 V and a set voltage of -10 V. The resistance states were read using a +1 V read. A maximum reset voltage of +7 V was used for the 350 °C memory cell with a set voltage of -12 V. Figure 5.10(a) and Figure 5.10(b) shows successful resistive switching for typical cells for both 300 °C and 350 °C cells with two clear distinctive resistance states, R_{OFF} and $_{ON}$, respectively.

Table 5.7 shows the R_{OFF} and R_{ON} values for a typical device for both the 300 °C and 350 °C memory cell. Little difference are apparent in pulsed or DC sweep measurements between the 300 °C and 350 ° memory cells. The electrical characteristics displayed in Figure 5.10(a) and Figure 5.10(b) are similar for all cells with no variation seen with area. The memory cell characteristics also show insensitivity to stoichiometry.

To summarise, excellent resistive switching has been observed for TiN/HfO_x/TiN memory cells with cubic hafnium oxide. Devices with monoclinic phase hafnium oxide showed no resistive switching suggesting an importance of crystal structure on the switching

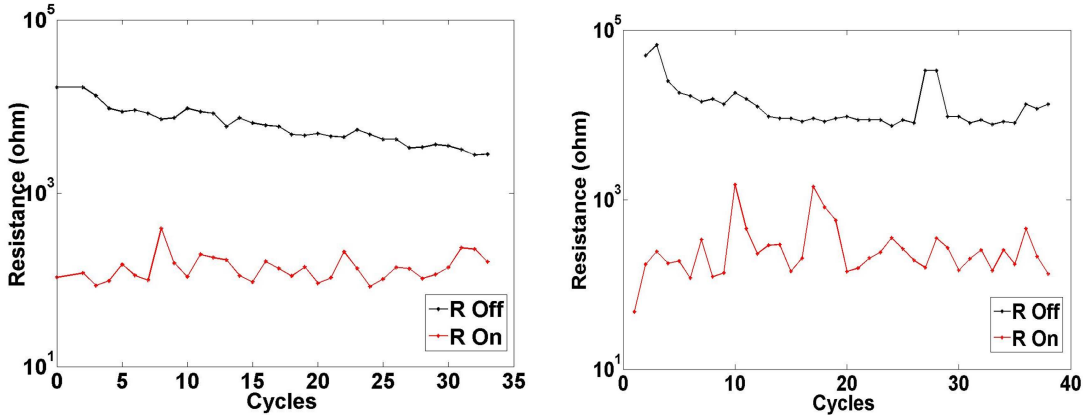


Figure 5.10: Pulsed IV measurements, at room temperature, for memory cells with deposition temperature of (a) 300 °C (average R_{OFF}=6.5x10^3 Ω and R_{ON}=1.4x10^2 Ω) and (b) 350°C (average R_{OFF}=1.5x10^4 Ω and R_{ON}=3.2x10^2 Ω), showing up to 40 switches.

Pulsed Parameter	**ALD Deposition Temperature (°C)**	
	300	**350**
Average R_{OFF} (Ω)	6.5x10^3	1.5x10^4
Average R_{ON} (Ω)	1.4x10^2	3.2x10^2
Average R_{OFF}/R_{ON}	46	47

Table 5.7: Pulsed IV results showing switching parameters at different ALD deposition temperatures.

mechanism. Similar switching mechanism for different stoichiometries is useful for increasing repeatability of memory characteristics, resulting in less stringent fabrication processes.

5.4 Irradiation of TiN/HfO_x/TiN Memory Cells

Current semiconductor memories have intrinsic limitation on radiation hardness capability. Metal oxide resistive RAM however can be considered radiation hardened memory by process due to the simple MIM structure with its thin oxide layer. This is verified by the work conducted in Chapter 4 whereby the HfO_x gate oxide MOS capacitors have high levels of radiation hardness due to the thin oxide layers. Although the RRAM cells are believed to have high levels of radiation hardness, the radiation effects must be fully investigated before RRAM is used as a replacement in nuclear and space industries.

In this work here, memory cells with different stoichiometry are fabricated, radiated and analysed, enabling the oxygen concentration effects on radiation to be studied. The switching mechanism in RRAM is reported to be caused by the rupture and formation of a conductive filament, in close proximity to the interface [164]. In the possibility of radiation induced holes and or oxygen vacancies moving towards the interface, these holes may interact with the conductive filament formation/rupture leading to alterations in switching characteristics. A thick 50 nm oxide is chosen as hence a worst case scenario to ensure even small radiation effects are measurable through the increase in number of trapped holes trapped or oxygen vacancies at the interface. Thick oxides have previously been used to support the general model of memristive electrical switching [165].

The radiation response to varying stoichiometry, previously not investigated, is investigated. This work is published in Transactions on Nuclear Science [154]. DC sweep and pulsed techniques are compared pre and post radiation. Considering the previously reported impact oxide stoichiometry has on switching properties of metal oxide RRAM cells [64, 66, 157], it is imperative the different stoichiometries are studied in relation to radiation.

5.4.1 Radiation Set-up

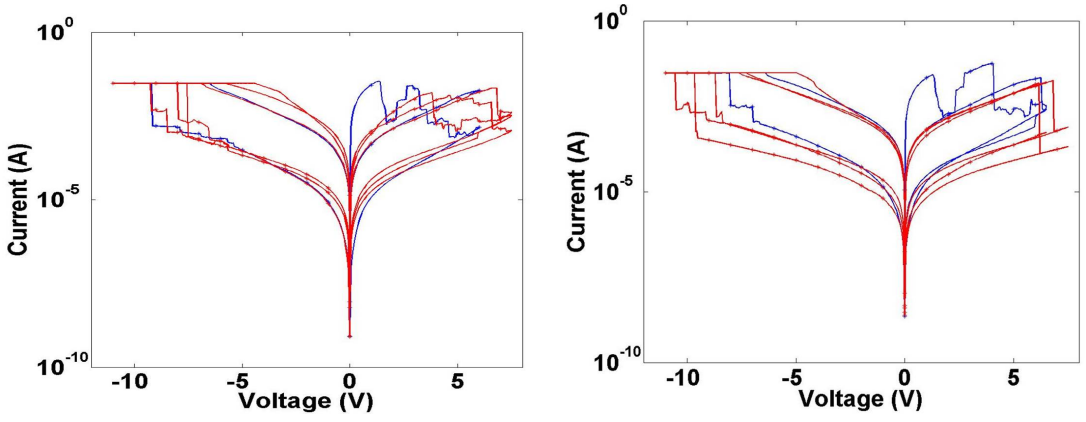
The memory cells used to investigate the radiation effects on the stoichiometry of HfO_x are the same cells as described in Section 5.3. Both DC sweep and voltage pulsed measurements were conducted pre and post irradiation at the University of Southampton. Nine cells per dose were measured for three different areas. The memory cells were left in three states before irradiation, for each area; HRS, LRS and pristine (not previously biased). ^{60}Co source was used for gamma irradiation, at a dose rate of 500 krad(Si)/hr, of memory cells with atomic layer deposition temperature at 300 °C and 350 °C. The memory cells were left floating during irradiation.

The irradiation took place at the military defence academy in Shrivenham, UK. Both type of cell types, for each ALD temperature, were exposed to gamma irradiation in the chamber for different time periods therefore varying the total dose. Four different doses

were chosen: 100 krad(Si), 500 krad(Si), 5 Mrad(Si), 10 Mrad(Si). Cells were also used as a control batch with zero radiation exposure. RRAM cells remain in an unbiased state for the majority of their time within a memory circuit, retaining their R_{OFF} or R_{ON}. The voltage pulse widths is minimal compared to the unbiased state time. For this reason, the memory cells were irradiated in the unbiased state.

5.4.2 Electrical Characterisation

DC sweeps were performed pre and post irradiation, at room temperature. After irradiation, each memory cell was measured again using up to six more voltage sweeps. The post radiation characteristics showed no effect on the area nor the state of the device. DC sweep characteristics pre and post irradiation can be seen in Figure 5.11 for a typical 300 °C and 350 °C memory cell. Table 5.8 displays the switching characteristics for pre and post irradiation for both device types. No change was observed in the set, reset voltage or R_{OFF}, R_{ON} values for any cells, up to the maximum radiation dose of 10 Mrad(Si) within the margin of error seen for the zero dose control batch.



(a) (b)

Figure 5.11: DC sweep measurements for memory cells, at room temperature, with deposition temperatures of (a) 300 °C and (b) 350 °C, before and after 10 Mrad(Si). Pre irradiation is shown in blue and post irradiation is shown in red. (HfO_x recipe parameters used are: T_{table}=300 °C, t_{plasma}=2 s, P_{plasma}=250 W, t_{TEMAH}=1.5 s, t_{PURGE}=8 s, P_{O_2}=80 mT with a new TEMAH source.)

A box plot can be seen for reset and set voltage for both ALD temperatures, in Figure 5.12, whereby no correlation exists for increasing radiation dose. The radiation hardness level is the same for both temperature memory cells, independent of the different stoichiometries, as can also be seen in Figure 5.12.

Pulsed measurements were conducted pre and post irradiation, at room temperature. The memory cells were cycled 20 times before irradiation followed by another 20 cycles post irradiation. The 20 cycles pre irradiation were selected in order to reduce the

DC Sweep Parameter	**ALD Deposition Temperature (°C)**			
	300		**350**	
	Pre	**Post**	**Pre**	**Post**
Average V_{SET} (V)	-7.7	-8.2	-8.0	-9.6
Average V_{RESET} (V)	+3.8	+5.2	+5.2	+6.6
Average R_{OFF} (Ω)	$5.2x10^4$	$3.1x10^4$	$5.1x10^4$	$5.9x10^4$
Average R_{ON} (Ω)	$2.4x10^3$	$2.3x10^3$	$1.4x10^3$	$1.8x10^3$
Average R_{OFF}/R_{ON}	22	14	36	33

Table 5.8: DC sweep results showing switching parameters at different ALD deposition temperatures before and after 10 Mrad(Si).

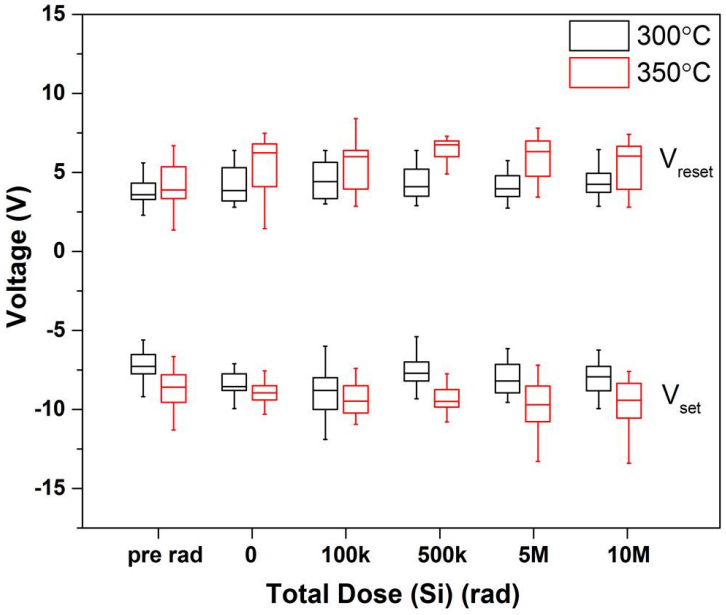


Figure 5.12: Pre and post-irradiation for set and reset voltages for different ALD temperatures, showing negligible effect from up to 10 Mrad(Si) dose radiation. Nine memory cells were measured at room temperature, per dose, per temperature.

effect of decreased R_{OFF}, as seen in Figure 5.10(a) as reported previously by others [101, 166, 167]. The reduction in R_{OFF} is thought to be due to cyclic accumulation of un-recovered defects within the oxide switching layer [168]. Pulsed measurements for 300 °C and 350 °C memory cells can be seen in Figure 5.13 comparing pre irradiation and after 10 Mrad(Si). No change is apparent in terms of switching parameters, within typical cycle to cycle variation.

Table 5.9 displays the R_{OFF} and R_{ON} values for these memory cells, pre and post irradiation. These results are repeatable for all cell sizes and memory cell states, with no correlation seen for area or states. Figure 5.14 displays a box plot for R_{OFF} and R_{ON} values for memory cells per dose for both cell temperatures. Little change up to 10 Mrad(Si) is apparent for both stoichiometries of HfO_x.

Pulsed Parameter	**ALD Deposition Temperature (°C)**			
	300		**350**	
	Pre	**Post**	**Pre**	**Post**
Average R_{OFF} (Ω)	7.7x10^3	5.5x10^3	1.1x10^4	8.0x10^3
Average R_{ON} (Ω)	2.6x10^2	1.8x10^2	3.4x10^2	2.2x10^2
Average R_{OFF}/R_{ON}	30	30	32	36

Table 5.9: Pulsed IV results, at room temperature, showing switching parameters at different ALD deposition temperatures, before and after 10 Mrad(Si).

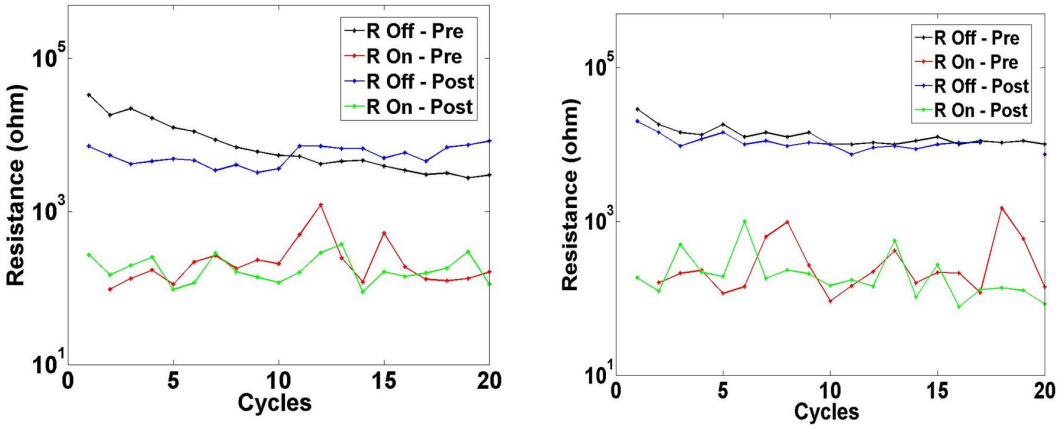


Figure 5.13: Pulsed IV results showing switching parameters at ALD deposition temperature of (a) 300 °C and (b) 350 °C, before and after 10 Mrad(Si).

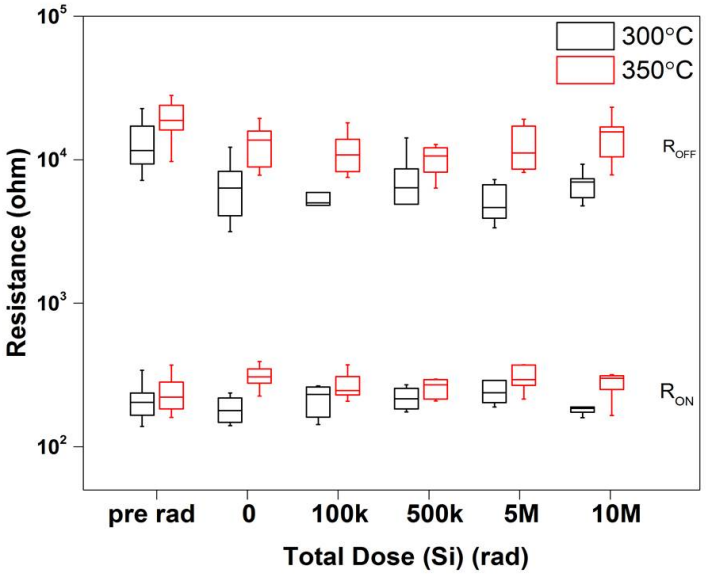


Figure 5.14: Pre and post-irradiation for R_{OFF} and R_{ON} for different ALD temperatures showing negligible effect from up to 10Mrad(Si) dose radiation.

To summarise, gamma radiation tolerance, up to 10 Mrad(Si), was observed for cubic memory cells, independent of stoichiometry with no visible shift seen even with 50nm

thick oxides. This high level of ionizing radiation hardness in agreement with previously reported hafnium oxide memory cells that were radiation hard up to 5.2 Mrad(HfO_x) [97]. A different research group also irradiated TaO_x RRAM cells up to 2.5 Mrad(Si) with no degradation or radiation effects seen, indicating VCM cells inherent radiation hardness [169].

5.5 Summary

TiN/HfO_x/TiN VCM memory cells have been fabricated and measured using pulsed and/or DC sweep techniques.

The first investigation of VCM cells looked at the role of stoichiometry of the top TiN electrode, using two different sputtering techniques; reactive and non-reactive. For reactive sputtering, an interfacial layer forms between the electrode and oxide layer, resulting in bipolar switching behaviour. For the non-reactive sputtering, the electrode deposited is titanium oxy-nitride and therefore further oxidation between the electrode and switching layer does not occur, resulting in unipolar switching. This verifies the theoretical model for metal oxide RRAM based upon oxygen vacancies in redox-based reactions. Due to the higher reproducibility and smaller variation in IV characteristics seen for reactive sputtered TiN electrode memory cells, this fabrication method was chosen for future VCM TiN/HfO_x/TiN cells.

A second investigation was conducted into the role of hafnium oxide layer properties, through altering the ALD deposition temperature. It is shown that monoclinic crystal structure is obtained when the temperature of deposition is at 400 °C, leading to the inability to exhibit resistive switching. Successful bipolar switching was seen for the two lower temperatures, with cubic crystal structure, suggesting crystal structure has a direct effect on the switching mechanism. The memory cells with hafnium oxide deposited at 300 °C and 350 °C exhibit similar switching characteristics even though the 300 °C HfO_x layer is sub-stoichiometric. This could be beneficial, in terms of simplifying the fabrication process, allowing for repeatable memory characteristics without stoichiometric constraints.

Ionizing radiation effects on VCM memory cells have also been investigated, in order to further the understanding of ionized effects in RRAM memory cells. The cubic TiN/HfO_x/TiN memory cells are essentially radiation hard up to 10 Mrad(Si). No radiation shift was measured for both 300 °C and 350 °C memory cells, even with 50 nm thick oxides, which are more sensitive to radiation damage. This shows that the hafnium oxide RRAM cells, and essentially VCM memory cells, have the potential to be used in harsh radiation environments.

Chapter 6

Switching Kinetics and Radiation Hardness of SiC ECM Resistive Memory

Resistive memory, with advantageous high density, low power arrays and simple fabrication process, offers a replacement for conventional semiconductor memories. Electrochemically active memory cells in particular have drawn a lot of attention due to their well understood metallic conductive filament formation with successful switching seen in a multitude of materials and structures.

More recently, SiC has shown great potential as the dielectric, whereby superior state stability [69,71] and ultra-high R_{OFF}/R_{ON} ratios have been reported [73,170]. However these memory cells are reportedly slow in switching, attributed to silicon carbide's high thermal conductivity and ability to act as a diffusion barrier for Cu [71]. Previous work investigated the role of a thermal barrier, inserted into a SiC resistive memory cell structure [80]. This extra layer resulted in a reduction for the time required to switch the device from ON to OFF. The RESET switching kinetics however were not qualitatively investigated and the SET mechanism was never taken into consideration in any form.

Intensive publications into the switching kinetics of oxide-based VCM cells have previously been investigated, including many papers on hafnium oxide [171–174]. Therefore the switching kinetics of VCM cells will not be investigated. However the switching kinetics for SiC based ECM cells have not previously been researched and therefore this work includes investigations into the switching kinetics of Cu/a-SiC/Au memory cells.

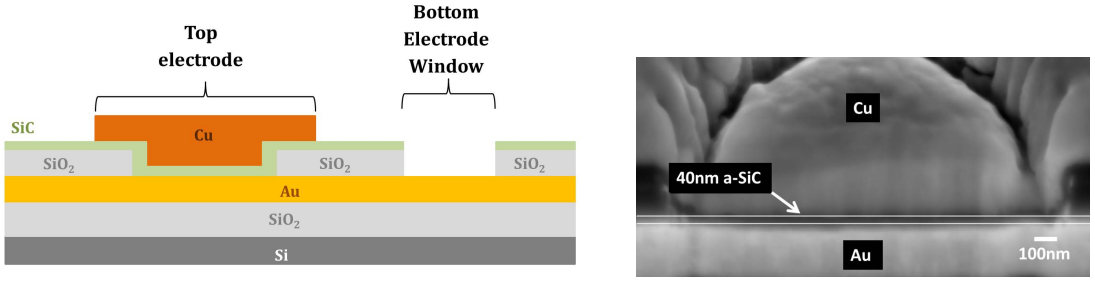
Pulsed measurements are conducted allowing the switching kinetics to be investigated and fitted, using the dielectric's thermal conductivity and resistivity properties, to a numerical model [175]. This enables the identification of the conduction mechanisms

for both SET and RESET. The investigation into the switching kinetics is discussed in Section 6.1.

Cu/a-SiC/Au memory cells memory cells are suitable for use in space and nuclear industry due to silicon carbide's good thermal and state stability [80,176]. These memory cells are irradiated and analysed, using ^{60}Co ionizing radiation up to a total dose of 2Mrad(Si) as discussed in Section 6.2. This dose is an approximate value as would be experienced by electronics in space and nuclear environments [177,178]. This is the first time radiation effects on SiC memory cells have been investigated.

6.1 Switching Kinetics of SiC Resistive Memory

Cu/a-SiC/Au resistive memory cells were fabricated as described in [170]. The same resistive memory cell structure was used as for VCM memory cells, as described in Section 5.1 and is depicted in Figure 6.1(a). An SEM image can be seen in Figure 6.1(b), whereby the thickness of the SiC layer is measured to be 40 nm. The dimensions of the whole structure is given in Table 6.1.



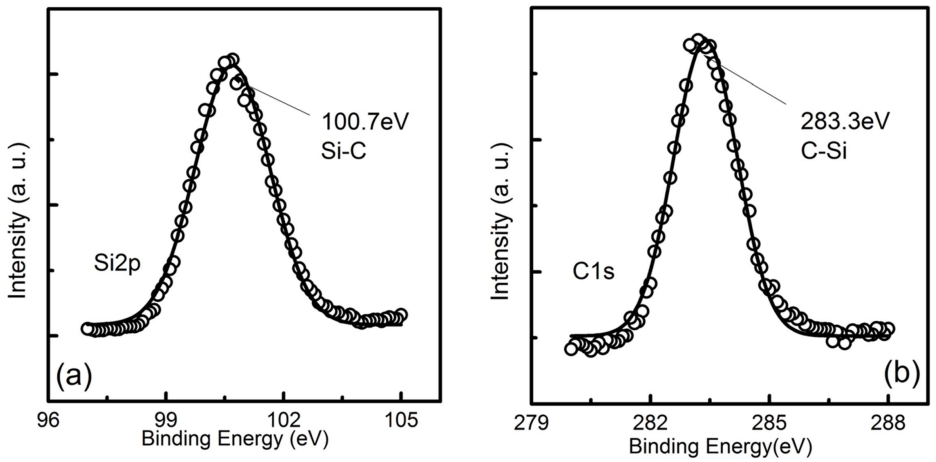
(a) (b)

Figure 6.1: Cu/a-Sic/Au memory cell described by (a) schematic of cell structure and (b) a cross-sectional SEM image.

Layer	Fabrication Technique	Thickness (nm)
SiO_2 isolation layer	thermal oxidation	1000
Au bottom electrode	non-reactively sputtered	300
SiO_2 device definition	reactively sputtered	250
a-SiC	non-reactively sputtered	40
Cu top electrode	non-reactively sputtered	300

Table 6.1: Dimensions and fabrication techniques used to create Cu/a-SiC/Au resistive memory cell structure. First layer in the table describes first layer deposited.

Material characterisation was performed on the SiC layer using XPS and XRD. XPS spectra for Si 2p and C 1s are shown in Figure 6.2(a) and Figure 6.2(b) where stoichiometric a-SiC were identified by peak energies located at 100.7 eV and 283.3 eV, respectively.



(a) (b)

Figure 6.2: XPS spectra for deposited SiC indicating stoichiometric a-SiC with peaks (a) Si 2p and (b) O 1s [69].

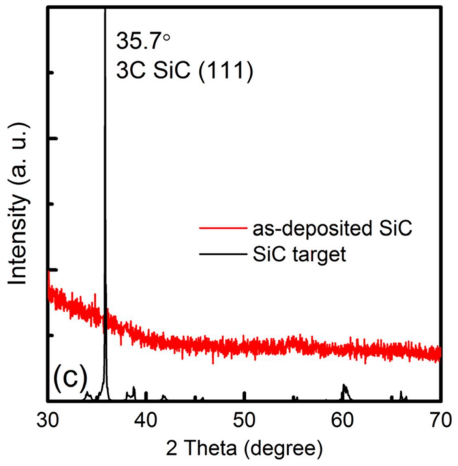


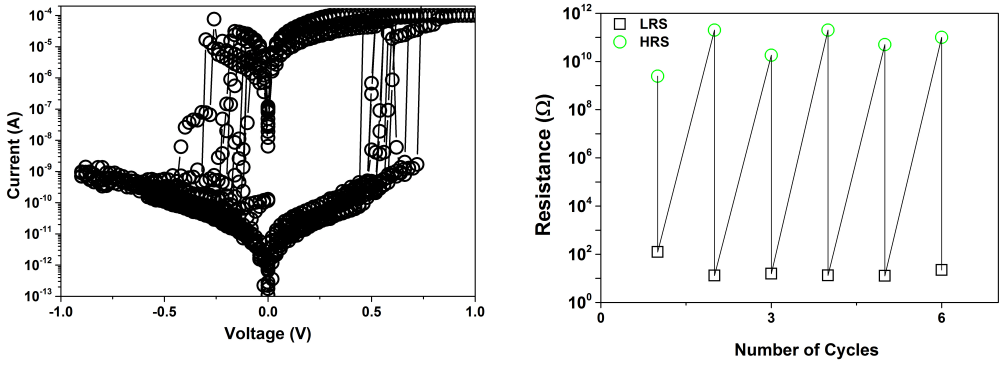
Figure 6.3: XRD spectra for deposited SiC layer and the SiC sputter target used for deposition. Amorphous SiC identified for deposited layer [69].

High resolution XRD spectra, as seen in Figure 6.3, was performed on both the deposited Sic layer and the SiC sputter target used for deposition. The peak seen in the spectra for the SiC sputter target is identified as the 3C-SiC (111) peak, located at 35.7 ° [179]. No peaks are present in the spectra for the deposited SiC layer, indicating amorphous SiC. XRD and XPS both indicate stoichiometric a-SiC is present [69].

6.1.1 Electrical Characterisation

DC sweep measurements were conducted at room temperature using a Agilent B1500A semiconductor analyser, using the set-up previously described. The memory cells were formed, followed by SET and RESET cycles, with a current compliance of 0.1 mA during the SET process. Figure 6.4(a) shows typical I-V characteristics whereby the

SET process occurs under positive voltage and reset occurs under negative voltage. A repeatable switching regime is obtained with V_{SET} ~0.6 V, V_{RESET} ~-0.2 V and R_{OFF}/R_{ON} ~10^7. This high ratio is in agreement with previously reported DC sweeps seen in the same batch of these Cu/a-SiC/Au memory cells, as measured by Le Zhong [73], although reduced SET and RESET voltage amplitude are achieved. This reduced reproducible V_{SET} was achieved through the control of filament formation.



(a) (b)

Figure 6.4: Electrical measurements for Cu/a-SiC/Au memory cell, at room temperature: (a) DC sweeps with repeatable switching regime with V_{SET} ~0.6 V, V_{RESET} ~-0.2 V and R_{OFF}/R_{ON} ~10^7 (b) Pulsed switching with R_{OFF} ~ $10^9 - 10^{11}$ Ω and R_{ON} >10 Ω giving R_{OFF}/R_{ON} ~ $10^8 - 10^{10}$.

Pulsed measurements were conducted on Cu/a-SiC/Au memory cells using a 50 ms pulse width with +8 V, +14 V for the set process and -0.4 V, -0.8 V, -1 V, -1.2 V and -2.5 V for the reset process. Figure 6.4(b) shows an ultra-high ratio is maintained for multiple cycles, with R_{OFF} ~10^9-$10^{11}\Omega$ and a R_{ON} >10Ω, resulting in R_{OFF}/R_{ON} ~10^8-10^{10}. This is, to our knowledge, the highest achieved R_{OFF}/R_{ON} ratio for all types of resistive memory. This exceeds the largest ratio previously reported, for Nb_2O_5 and GeO_x memory cells [180, 181]. The large ratio is a result of a large R_{OFF} value and is thought to originate from the presence of a Schottky barrier at the Cu/SiC interface [170]. The ratio obtained using DC sweep measurements is slightly lower than the ratio obtained using pulsed measurements due to the current compliance limiting the R_{ON} resistance in the DC sweep mode. There was no device area dependency observed for either pulsed nor DC sweep measurements, with areas ranging from 2x2 μm^2 to 80x80 μm^2.

Ultra-high ratios have been achieved for Cu/a-SiC/Au memory cells under pulsed switching, however the switching is slow with a 50ms pulse width. The switching kinetics of Cu/a-SiC/Au memory cells have been investigated and compared to other reported ECM cells from literature. A numerical model has been previously proposed to describe switching mechanism for both SET and RESET in ECM cells [182].

6.1.2 Switching Kinetics Model

Filament growth has been modelled numerically by Ielmini in [182] based upon a physical explanation for universal resistive switching in bipolar RRAM cells. It models the conductive filament growth and dissolution, i.e. SET and RESET, as thermally activated ion migration and discusses how the switching characteristics are affected by migration parameters and experimental set-up. The ion migration is described using a thermally activated hopping model leading to setting the device into the LRS state. This same model is also used to describe the reset process back into the HRS state. Experimental data has been used to verify the numerical calculations, allowing the kinetics of CF formation and dissolution to be studied with regards to experimental measurement conditions and material parameters.

This ion migration model can be used for both types of ionic switching i.e. ECM and VCM. In VCM cells, an applied positive voltage results in field-driven migration of negatively charged oxygen ions through the insulating layer towards the positive electrode (simultaneous to migration of positively charged oxygen vacancies). Nucleation followed by growth forms a conductive filament. The points of nucleation can be at thinner parts of the insulator with enhanced electric field, or in an area of higher concentration of defects, leading to localization of current. A reservoir of ions is needed on the positive electrode, in turn leading to bipolar behaviour.

For ECM cells, the active electrode is modelled as the ion reservoir. This ion reservoir releases the cations for filament growth. Once these cations have nucleated on the inert electrode surface, the filament grows through reduction on the CF surface. For reset, under opposite polarity of applied bias, the ion migration reverses to the active electrode and the filament ruptures.

The kinetics of the SET process have been modelled in [182] based on ion migration through thermally activated hopping. The filament nucleation time is neglected as ion migration is the rate limiting factor. The local temperature of the filament assists the ionic migration, with the filament growth rate given by Equation 6.1 which is proportional to the ion migration rate.

$$\frac{d\Phi}{dt} = Ae^{-\frac{E_A}{kT}} \tag{6.1}$$

ϕ is the CF diameter (assumed constant throughout insulator thickness), k is the Botlzmann constant, T is the temperature of the CF, A is a constant, E_A is the activation energy, given by Equation 6.2, where E_{A0} is the ion hopping energy barrier, q is the elementary charge, V is the applied voltage across the insulator and α is a coefficient for barrier lowering due to applied bias. This barrier lowering causes the positive ions (oxygen vacancies for VCM, metal cations for EMC) in the direction of the E-field.

$$E_A = E_{A0} - \alpha q V \tag{6.2}$$

The model takes into account thermal assistance for ion migration whereby the local temperature T includes effects from Joule heating due to high current densities within the filament during SET. The steady-state Fourier equation, used to calculate local temperature, was solved with boundary conditions i.e. temperature at either electrode were set to room temperature. The CF temperature was estimated based upon the current flowing through the CF or voltage applied over the cell. Using this temperature derivation, and inserting this and Equation 6.2 into Equation 6.1 gives Equation 6.3. This equation can be solved numerically to simulate the filament growth during the SET process. The RESET process models the reduction in filament using the same equation but with a negative sign inserted in the right-hand side.

$$\frac{d\Phi}{dt} = Ae^{-\frac{E_{A0}-\alpha q V}{kT_0(1+\frac{V^2}{8T_0\rho k_{th}})}} \tag{6.3}$$

The SET and RESET process depend highly on the resistivity of the electrolyte layer, along with the thermal conductivity and activation energy. A condition has been proposed in this thesis, resulting in the ability to determine the switching mechanism type using these dielectric properties i.e. thermally assisted ionic motion or ionic motion without thermal contributions. If the product of $\rho k_{th} >> V^2/8T_0$, the filament growth rate equation reduces to Equation 6.4, showing the mechanism is due to ionic motion only, without any thermal contribution. If however $\rho k_{th} << V^2/8T_0$, the filament growth rate equation reduces to Equation 6.5, resulting in thermally assisted ionic motion.

$$\frac{d\Phi}{dt} = Ae^{-\frac{E_{A0}-\alpha q V}{kT_0}}, \qquad \tau_{pulse} \propto e^{\frac{E_{A0}-\alpha q V}{kT_0}} \tag{6.4}$$

$$\frac{d\Phi}{dt} = Ae^{-\frac{E_{A0}8\rho k_{th}}{kV^2}}, \qquad \tau_{pulse} \propto e^{\frac{E_{A0}8\rho k_{th}}{kV^2}} \tag{6.5}$$

Figure 6.5 plots ρk_{th} for a variety of previously reported ECM cells, with a multitude of materials, for both SET and RESET states. A filament size of 5x5 nm^2 was used for all memory cells making them comparable. ρk_{th} for the SET mechanism was calculated using k_{th} of the dielectrics from literature and R_{OFF} from the pulsed switching results, along with the reported dielectric thickness. ρk_{th} for the RESET mechanism was calculated using k_{th} of the metallic conducting filament and R_{ON} from the pulsed switching results, along with the reported dielectric thickness. For the SET process in the Cu/a-SiC/Au memory cells in this work, high thermal conductivity (k_{th}=490 W/mK [183]) along with extremely high R_{OFF} resistance results in an ultra high ρk_{th} value compared to other reported memory cells, resulting in purely ionic motion with

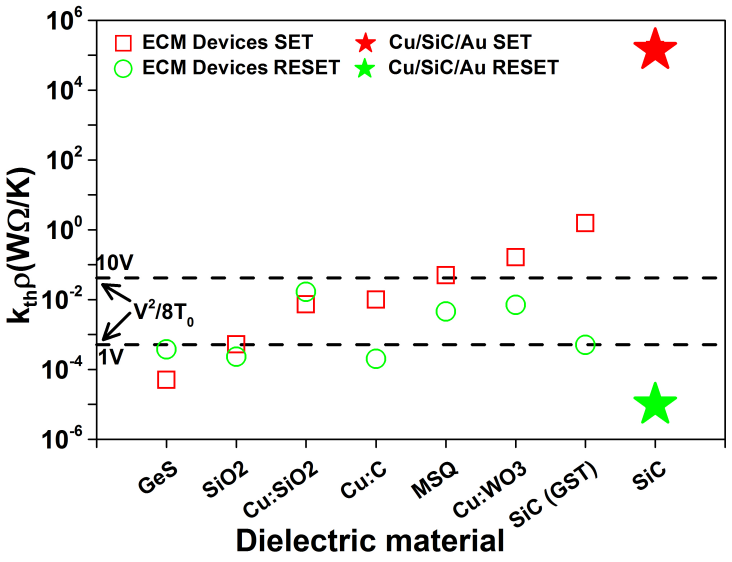
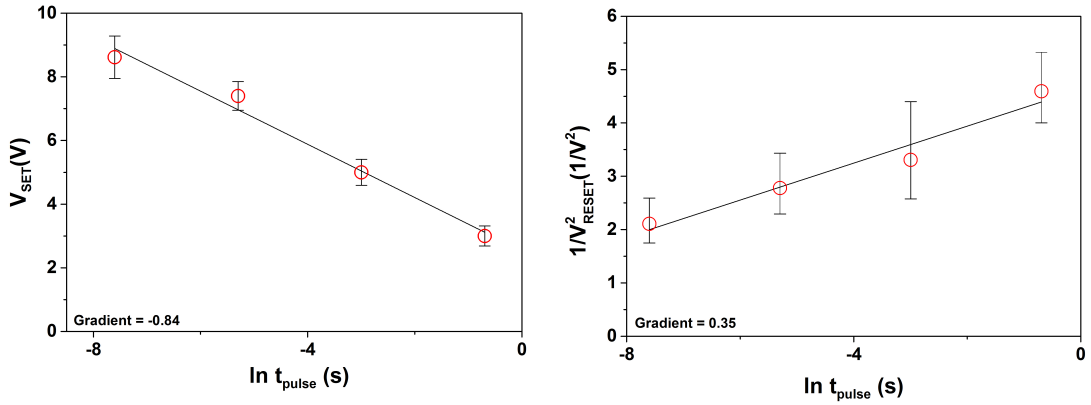


Figure 6.5: Thermal conductivity and resistivity of reported ECM cells compared with Cu/a-SiC/Au memory cells for SET and RESET. Dashed red line determines the switching mechanism; above the line indicates ionic only whilst below indicates thermally assisted ionic motion, at 1 V and 10 V. The SET mechanism for the reported memory cells in this paper is well into the ionic only regime, even at 10 V, due to the high thermal conductivity of the a-SiC dielectric in combination with the high off resistance of these memory cells. The mechanism for RESET is thermally assisted ionic motion shown by the point situated below the 1V line. The references are GeS [72], SiO_2 [79], Cu:SiO_2 [74], Cu:C [77], MSQ [70], CU:WO_3 [81] and SiC(GST) [80].

no thermal contribution. The effective k_{th} is assumed to be lower than the RESET data presented in Figure 6.5, due to out-of-filament heat conduction, pushing the RESET into $\rho k_{th} < V^2/8T_0$ at 1 V and at 10 V of applied bias. This would indicate the RESET mechanisms are due to thermally assisted ionic motion, as in agreement with previously reported literature [64, 80].

A relation has been shown to exist between the RESET state conditions and the SET switching kinetics [173]. In order to investigate this in regards to the SET and RESET mechanism of SiC memory cells in more detail, the switching kinetics were experimentally identified using pulses with varied durations. A selection of pulsed measurements were conducted in order to fit the experimental pulse time dependence on the SET and RESET voltages with the theoretical model.

Figure 6.6(a) shows that Cu/a-SiC/Au memory cells in this work, for the SET mechanism, do indeed have an exponential relation between SET voltage and pulse width. This shows agreement with the model, as seen by Equation 6.4, whereby the SET process in these memory cells are determined by ionic motion without thermal contribution. Using the gradient of Figure 6.6(a), the barrier lowering coefficient, α, is calculated to be 0.02. αqV describes the barrier lowering due to an applied field as shown in Equation 6.2,



(a) (b)

Figure 6.6: Time dependencies for SET and RESET switching: (a) SET time dependence of pulse width with pulse voltage for Cu/a-SiC/Au memory cells. As pulse voltage is increased, time needed to SET device decreases exponentially indicating ionic only motion (b) RESET time dependence of pulse width with pulse voltage for Cu/a-SiC/Au memory cells. Time needed to RESET device decreases exponentially with a $1/V^2$ relation indicating thermally assisted ionic motion. All measurements were conducted at room temperature.

where E_A is the activation energy and E_{A0} is the energy barrier for ion hopping. α can be approximated by $\delta z/2L_{CF}$, where δz is the ion hopping distance between states and L_{CF} is the filament length [184]. Assuming the filament length is equal to the oxide thickness, using α=0.02 results in an ion hopping distance of 1.52 nm being extracted. The large SET voltage required for these memory cells can be attributed to the lack of joule heating contribution, originating from the low resistivity and high thermal conductivity of SiC, in agreement with [173].

Figure 6.6(b) shows that that Cu/a-SiC/Au memory cells in this work, for the RESET mechanism, do indeed have an exponential relation between pulse width and $1/V^2_{RESET}$. This shows agreement with the model whereby the RESET process in these memory cells are determined by thermally assisted ionic motion. The area, and therefore diameter of the conductive filament can be found by measuring the gradient of Figure 6.6(b), which is then defined as g in Equation 6.6, derived from Equation 6.5.

$$g = \frac{8E_{A0}\rho k_{th}}{k} \tag{6.6}$$

Replacing resistivity with RA/l, and rearranging for area, A, then gives Equation 6.7, where l is the length of the conductive filament, assumed to be the SiC thickness.

$$A = \frac{gkl}{8E_{A0}k_{th}R_{ON}} \tag{6.7}$$

Assuming a cylindrical filament, using the area calculated from the gradient, the conductive filament diameter is extracted to be Φ ~4 nm, using k_{th}=401 W/mK and E_{A0}=0.69 eV [185]. This is in good agreement with previously reported diameter sizes for Cu nano-filaments [186].

Although these memory cells are limited by the speed of switching, the high ratio and stability show their potential for use in harsh environments.

6.2 Irradiation of SiC Resistive Memory

The Cu/a-SiC/Au memory cells were irradiated with Co_{60} ionizing radiation up to 2 Mrad(Si). The memory cells were pulsed pre and post irradiation, at room temperature, as can be seen in Figure 6.7 whereby the ultra-high R_{OFF}/R_{ON} was maintained at $\sim 10^9$. The data for pre irradiation in Figure 6.7 is the same as shown in Figure 6.4(b).

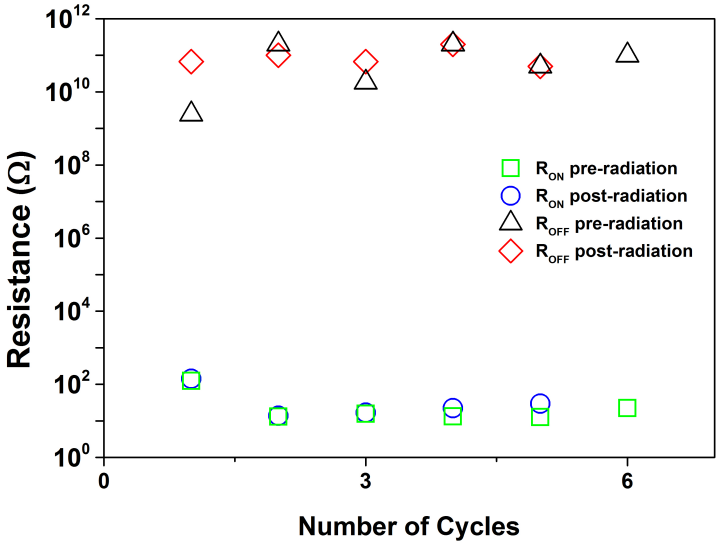
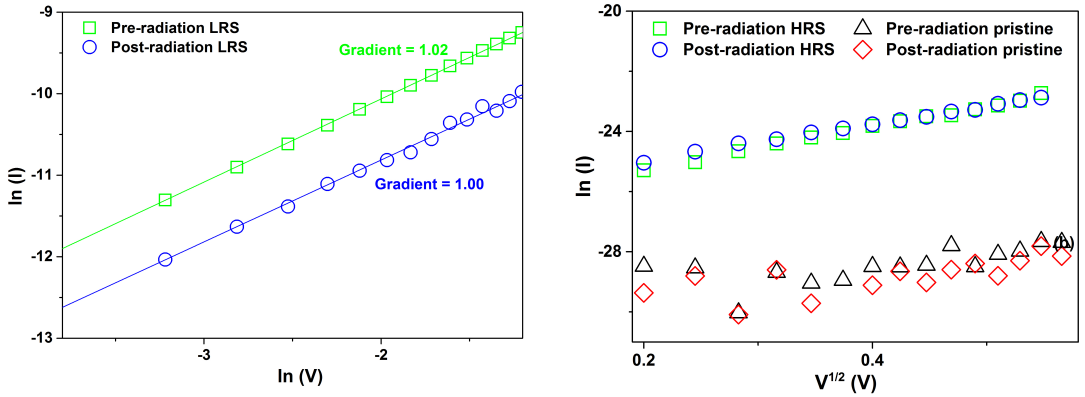


Figure 6.7: Pulsed measurements for Cu/a-SiC/Au device, at room temperature, before and after 2 Mrad(Si) ionizing irradiation. Pre irradiation gives $R_{OFF} \sim 10^9 - 10^{11}$ Ω and R_{ON} >10 Ω giving $R_{OFF}/R_{ON} \sim 10^8 - 10^{10}$. Post irradiation show $R_{OFF} \sim 10^{10} - 10^{11}$ Ω and R_{ON} >10 Ω giving $R_{OFF}/R_{ON} \sim 10^9 - 10^{10}$. Devices shown to be radiation hard up to 2 Mrad(Si).

Along with pulsed measurements, DC sweep measurements were conducted at room temperature allowing the change in conduction mechanism, post irradiation, to be viewed. Previously reported work on the Cu/a-SiC/Au memory cells identified the conduction mechanism for the LRS state to be ohmic conduction, most likely from a Cu filament [73]. This was shown by a linear relation of current and voltage. In order to check the post radiation results, the same measurement was conducted before and after radiation and

then compared. Figure 6.8(a) plots ln(I)-ln(V) for the LRS state of a typical sweep, before irradiation, along with the LRS state of a typical sweep after irradiation. The pre radiation sweep was taken from a sweep as shown in Figure 6.4(a). The linear relation is exhibited for both pre and post radiation, indicating no change in LRS conduction mechanism. A small reduction of LRS current of ~10 μA occurs after radiation, but as this is within cell to cell variation it can not be directly attributed to radiation effects.



(a) (b)

Figure 6.8: IV plots of Cu/a-SiC/Au memory cells showing no radiation change for (a) LRS with a ln(I)-ln(V) showing a linear fit of 1 indicating ohmic conduction and (b) HRS and pristine states with a ln(I)-$V^{1/2}$ plot indicating Schottky emission.

The conduction mechanism for the HRS state in the Cu/a-SiC/Au memory cells has previously been identified as Schottky emission [73], displayed by a linear fit in a ln(I)-$V^{1/2}$ plot. Figure Figure 6.8(b) shows ln(I)-$V^{1/2}$ for typical HRS and pristine sweeps, as displayed previously in Figure 6.4(a) before irradiation, along with typical HRS and pristine sweeps after irradiation. Negligible different is seen post irradiation, with Schottky emission remaining as the conduction mechanism.

These results show there is no noticeable change in conduction mechanism or pulse measurements after 2Mrad(Si) ionizing radiation. This indicates the potential to use Cu/a-Si/Au memory cells in space and nuclear industries. Previously reported hafnium oxide RRAM cells have also shown high ionizing radiation tolerance with negligible change seen in memory cell parameters up to 10 Mrad(Si) as seen in Chapter 5 and work conducted by other groups [78, 97, 154]. This indicates that the radiation sensitive region within of a memory circuit is not the RRAM cell but rather the select device i.e. transistor, whereby larger areas of oxide in transistors (STI and BOX oxides) have previously been identified as highly susceptible to radiation effects [187].

6.3 Summary

ECM cells were fabricated with investigations into the switching mechanism performed. Cu/a-SiC/Au memory cells have shown successful pulsed switching with ultra-high $R_{OFF}/R_{ON} \sim 10^8 - 10^{10}$, the highest published ratio to date, originating from high OFF resistance. The high off resistance and thermal conductivity of these memory cells indicates that, using the condition $\rho k_{th} >> V^2/8T_0$, the switching mechanism for the SET process is due to ionic motion without any thermal contributions resulting in slow switching memory cells. The RESET mechanism, using the condition $\rho k_{th} << V^2/8T_0$, is believed to be due to thermally assisted ionic motion, with agreement in pulse time dependency experiments. The agreement between deduced measurements of these simple memory cells, with extreme parameters, and the numerical model indicates this model works for a full range of memory cell parameters.

These Cu/a-SiC/Au memory cells are shown to be radiation hard up to 2Mrad(Si) with no change seen in ratio of $R_{OFF}/R_{ON} \sim 10^8 - 10^{10}$ or conduction mechanisms, indicating the potential for these memory cells to be used in harsh environments.

Chapter 7

Summary

The reliability of electronics is key in modern day living. Devices are constantly evolving and new structures and new materials are being utilised. Before new materials and new devices are used in space and nuclear industry, the radiation effects must be understood and controlled.

In MOS transistors, radiation can occur in three areas of dielectric, the BOX, STI and gate oxide. Work conducted by my colleagues and I have shown fluorine implants can passivate interface traps, resulting in radiation hardened MOS transistors. However, as high-k dielectrics are being used as replacements for silicon dioxide gate oxides, enabling the scaling of MOSFETs to continue, the radiation effect of high-k dielectrics must be investigated.

In particular, hafnium oxide shows potential for use as gate oxides in MOS transistors, and also switching layers in resistive memories. In order to investigate the radiation effects of hafnium oxide, a high quality TiN/HfO_x stack was developed. A multitude of recipes were developed enabling the stoichiometry of both the TiN layer and the hafnium oxide layer to be controlled. Using three different temperatures for ALD deposition of 300 °C, 350 °C and 400 °C, a Hf:O ratio of 1.78±0.05, 1.99±0.05 and 1.95±0.05 was extracted. The two lower temperatures resulted in cubic crystal structure whereas the highest temperature resulted in monoclinic. Two sputtering techniques were investigated for the top TiN layer, resulting in TiO_xN_y layers deposited using non-reactive sputtering and stoiciometric TiN deposited using reactive sputtering. Finally a standard recipe for $HfO_{1.9}$ with a deposition rate of 0.12 nm/cycle was developed for all future use of hafnium oxide in the University of Southampton nano-fabrication cleanroom.

Following the development of high quality high-k dielectrics, a batch of high-k MOS capacitors were fabricated and irradiated to investigate the damage due to radiation in high-k dielectrics, including silicon dioxide, hafnium oxide and aluminium oxide, with TiN and Al electrodes. C-V measurements verified the high quality TiN/HfO_x stack

using sputtered TiN whereby the interfacial EOT is less than half of the total EOT, for a 10 nm HfO_x layer, indicating little reactivity between the layers. The best capacitors in terms of high capacitance, high dielectric constant and low leakage are the TiN/HfO_2/Si capacitors, with similar electrical characteristics to previously reported hafnium oxide capacitors. The TiN/HfO_2/Si capacitors exhibited superior capacitance performance compared to the reference silicon dioxide capacitors indicating that high quality high-k MOS capacitors have been fabricated, validating the move towards HKMG structures to overcome scaling issues.

Unbiased irradiation results showed the high-k capacitors had the same order of magnitude voltage shifts when compared to the silicon dioxide capacitors, with a shift of < 100 mV seen for up to 3 Mrad(Si) gamma irradiation for the TiN/HfO_2/Si capacitor. The nanometre thickness of these oxides is thought to result in a small amount of radiation damage, concluding that replacing gate oxides with high-k dielectrics does not lead to a significant decrease in radiation hardness of the device. For devices such as MOS transistors, radiation damage in high-k gate oxide will be insignificant when compared to the much larger areas of oxides, like the BOX and STI.

In CMOS technology the scaling of MOSFETs has led to HKMG structures, used to overcome gate oxide leakage. The superior capacitance and leakage current properties shown here for TiN/HfO_2/Si capacitors, and the high levels of radiation hardness it can withstand, indicate HKMG MOS structures can be utilized to overcome scaling issues, even in harsh radiation environments.

Many previous publications show clear measurable radiation effects with devices in the unbiased state, including work performed by myself and colleagues on BOX MOS capacitors [31, 47, 148, 149]. Based on these results, we decided on an unbiased condition for the high k MOS capacitors. In order to perform biased measurements, a new mask and fabrication process would be needed in order to package the devices allowing for biasing in the radiation facility. The time and cost of this meant it was not possible to perform the biased measurements within this work. For future work however, biased measurements of high-k MOS capacitors would be beneficial whereby the yield remaining after recombination would be higher, possibly leading to increased amount of oxide and interface trapped charge. This may result in increased voltage shifts, measurable above the device and sweep variation. The possible increase in radiation effects would also allow other dependencies to be studied including annealing and temperature effects.

A new contender for non-volatile memory, resistive random access memory, has the potential to become an alternative to conventional semiconductor memories. Therefore radiation effect on resistive memory must be investigated. Hafnium oxide in particular has been used as a switching layer showing promising resistive memory cell properties. Hafnium oxide resistive memory cells have been fabricated, measured and analysed using DC sweep and pulsed techniques. Multiple investigations into material effects on

switching mechanism in VCM memory cells were conducted, as were radiation effects. Due to RRAM cells predominantly being in the unbiased state, except for incredibly short reading and switching times, the radiation was performed also in the unbiased state.

Firstly, TiN/HfO_x/TiN memory cells were fabricated, using two sputtering techniques for the top electrode. The non-reactively sputtered TiO_xN_y layer had little reactivity with the hafnium oxide layer below, resulting in unipolar switching (due to lack of interfacial oxide layer) with a R_{OFF}/R_{ON} ratio of 3x10^3, however with large variability in IV sweeps. The memory cell with the reactively sputtered electrode indicated the presence of an interfacial oxygen layer, most likely originating from the reaction of titanium and hafnium oxide, before the nitrogen plasma is introduced. This resulted in bipolar switching. The dependence of switching characteristics on the electrode stoichiometry, verifies the oxygen vacancy based switching model for VCM memory cells. Reactive sputtering was used as the chosen fabrication technique for the TiN electrode in future batches due to the higher reproducibility and smaller variation in IV characteristics.

After the stoichiometry of the electrode had been investigated, the next batch looked into the effect of the metal oxide stoichiometry, within the same TiN/HfO_x/TiN structure. The hafnium oxide layer stoichiometry was altered through changing the atomic layer deposition temperature. Monoclinic stoichiometric hafnium oxide, obtained at 400 °C, did not result in resistive switching. This indicates the importance of crystal structure on the resistive switching mechanism. The two cubic hafnium oxide memory cells, with lower deposition temperatures of 300 °C and 350 °C, resulted in bipolar switching with similar switching characteristics, despite the difference in stoichiometry. This could be beneficial, removing the constraints of stoichiometry for the metal oxide layer in fabrication of VCM cells. These memory cells were irradiated with negligible voltage shift seen, for up to 10 Mrad(Si), even with 50 nm thick oxides, which are more sensitive to radiation damage. This shows the potential use for hafnium oxide RRAM cells in harsh radiation environments and is in agreement with other recent results seen for hafnium oxide MOS capacitors.

Another type of resistive memory, ECM memory has the potential to be radiation hard due to lack of oxide layer. Cu/a-SiC/Au ECM cells were studied, showing successful pulsed switching with ultra-high $R_{OFF}/R_{ON} \sim 10^8 - 10^{10}$, the highest published ratio to date, originating from high OFF resistance. Pulse time measurements were conducted allowing the switching kinetics to be analysed, using a numerical model. The high OFF resistance and thermal conductivity of the Cu/a-SiC/Au memory cells indicates that, using the condition $\rho k_{th} >> V^2/8T_0$, the switching mechanism for the SET process is due to ionic motion without any thermal contributions resulting in slow switching memory cells. The RESET mechanism, using the condition $\rho k_{th} << V^2/8T_0$, is believed to be due to thermally assisted ionic motion, with agreement in pulse time dependency experiments. A conductive filament diameter of ∼4 nm was extracted. The agreement

of the model and experimental data proves this model works for memory cells with a full range of parameters i.e. extremely high OFF resistance states.

The radiation effects of SiC ECM cells are investigated for this first time. These highly stable and thermally reliable Cu/a-SiC/Au memory cells are shown to be radiation hard up to 2 Mrad(Si) with no change seen in ratio of $R_{OFF}/R_{ON} \sim 10^8 - 10^{10}$ or conduction mechanisms, showing potential for these memory cells to be used in harsh environments. VCM hafnium oxide RRAM cells also show high ionizing radiation tolerance with negligible change seen in device parameters up to 10 Mrad(Si) [97, 154]. This indicates that the radiation sensitive region within a memory circuit is not the RRAM device but rather the select device used to address the RRAM cell i.e. transistors. Chapter 4 has shown the gate oxides within transistors are essentially radiation hard due to the small thicknesses used. The other large area oxides within transistors, such as buried oxides and SOI oxides, remain the areas of weakness in terms of ionizing radiation damage.

Traditionally, MOSFETs are used throughout computer architecture in both logic and memory. With the superior electrical properties and high levels of radiation hardness, RRAM is a strong emerging NVM candidate to be used as a replacement for the conventional transistor based memory such as Flash and DRAM. Transistors however may still be used as access devices for RRAM cells and are also still used for logic computations. With the move to high-k metal gate transistors, the superior capacitance/leakage properties and high levels of radiation hardness, indicate that these HKMG MOSFETs are a promising solution to scaling issues regarding the gate oxide thicknesses. However the areas of a transistor still susceptible to radiation effects include the buried oxide and isolation oxide. These large areas of oxide result in the transistor still being the most sensitive region in a circuit to ionizing radiation.

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