

N over N cascode push pull modulator driver in 130nm CMOS enabling 20Gb/s optical interconnection with Mach-Zehnder modulator

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The N over N cascode push-pull modulator driver is demonstrated at 20Gbit/s with IBM 130nm technology. Elec-optical measurement of modulator driver integrated with Mach-Zehnder modulator (MZM) is also presented. This modulator driver achieves 50Ω output impedance matching (for MZM) with on-chip termination. The power consumption of modulator driver is 312 mW and output swing is $3.4V_{pp}$ on differential.

Introduction: In the field of Silicon Photonics, an optical interconnection link using a Mach-Zehnder modulator (MZM) is common and well researched. In the area of electrical modeling, most of these modulators are treated as transmission lines. Previous designs [1], [2] and [3] use a current-mode logic circuit with resistive loads which can generate a high voltage swing at the output with good impedance matching performance, however, the problem is that most of these designs require an external biasing system (such as a biasing tee) to be integrated with an optical modulator. For interconnection applications, the modulator driver design is expected to be low-cost and compact-provide. This paper presents a modulator driver providing 20Gbits/s data rate transmission for a 50Ω MZM at low cost and low power. The modulator driver and MZM are integrated using a multiple die package (bond wires or flip chip), without the need for additional off-chip biasing circuitry.

Circuit description: The top level design of the driver and integration with the MZM is shown in Fig.1. The driver circuit is composed of a number of pre-amplifier and output stages in order to achieve the required gain and fanout. In the pre-amplifier, the first stages (providing the majority of the overall AC gain of the full modulator driver), and the later stages ($2\times$ fanout stages) increase the fan-out of the data signal at the output. All of the pre-drivers are implemented using NMOS common source amplifiers, with inductor and PMOS (gate biased at V_{ss}) loads. The power supply of all pre-driver stages use $V_{dd} = 1.6V$. The final output stage is a cascode N over N amplifier operating with differential inputs. An on-chip termination network is located between the differential outputs and this network adjusts the output impedance to be 50Ω on each single-ended output. With on-chip termination and the push-pull output stage, the complete driver can be directly integrated to a MZM using wire or flip-chip bonding.

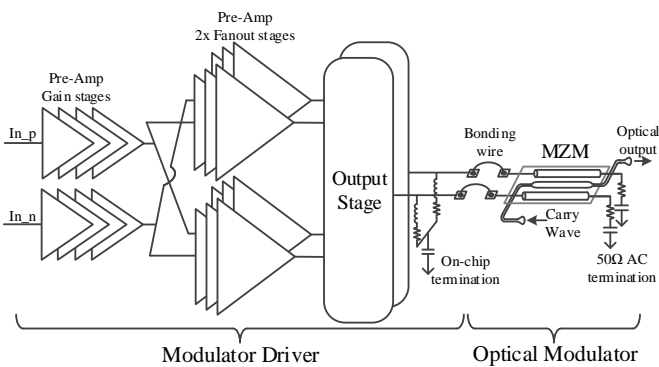


Fig. 1. Top level schematic of driver circuit and optical modulator integration

The schematic of the output stage is shown in detail in Fig.2. An N-over-N cascode push-pull amplifier is used in this design. Unlike conventional push-pull amplifiers [4], an NMOS source follower replaces a conventional PMOS common source amplifier on top branch of the circuit. This modification provides an enhanced bandwidth of the amplifier at the cost of slightly decreasing the output voltage swing. In addition, the load capacitance on an NMOS source follower is much smaller than the equivalent PMOS circuit, thereby ensuring that the

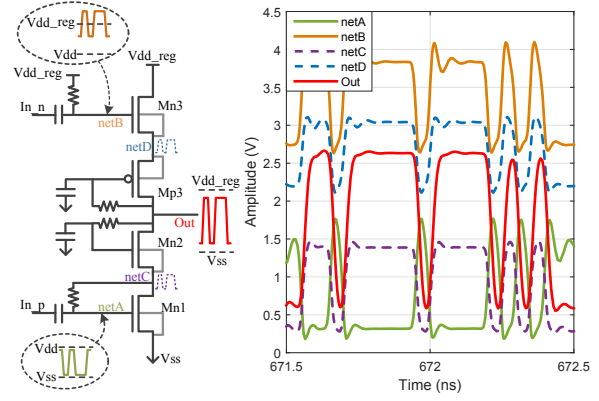


Fig. 2. Output stage (single end) and 20Gb/s waveform on different nets

design is inherently low power due to the reduction of input load capacitance in the output stage, allowing a reduction in the overall power consumption of the pre-driver circuit as a whole.

The resulting behaviour of the output stage is given in Fig.2. The two inputs (netA & B) are differential signals and are re-biased versions of output stage internal signals. The cascode transistors (Mp3 and Mn2) are also self biased in the circuit. The regulated supply (V_{dd_reg}) is 3.3V in this design. The gate of Mn3 (netB) is re-biased onto V_{dd_reg} . The voltage V_{gd} of Mn3 varies in the range $\pm 0.8V$. The signal on the gate (netB) and source (netD) of Mn3 are in the same phase. V_{gs} and V_{ds} are also less than 1.6V in data transmission. Therefore, the voltage differences between the nodes on this transistor (Mn3) are always less than the break-down voltage ($V_{break_down} = 1.6V$ in this process). Table1 shows the dimensions and design details of the output stage circuit.

Table 1: Design detail of the N over N cascode push pull amplifier

Parameter	Value
Mn1	$90\mu m/120nm$
Mn2	$150\mu m/120nm$
Mn3	$150\mu m/120nm$
Mp1	$150\mu m/120nm$
RC on Mn1 & Mp1	$43k\Omega$ & $0.8pF$
RC on Mn2 & Mn3	$95k\Omega$ & $3.2pF$

The frequency response and output impedance with different termination networks are shown in Fig.3. In Fig.3(a), the pass-band gain of the modulator driver is over 40dB and the bandwidth is greater than 11GHz. In Fig.3(b), with on-chip (RC) termination the output impedance is 50Ω in the low frequency band (<1GHz) but reduced at frequencies above this. In the termination network of this design, there is an on-chip inductor added into the circuit. This optimizes the output impedance at higher frequencies. Overall, the output impedance of this design is $50 \pm 3\Omega$ in the data transmitting band of interest until 11GHz.

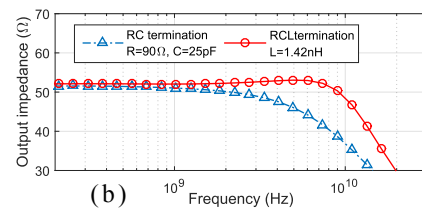
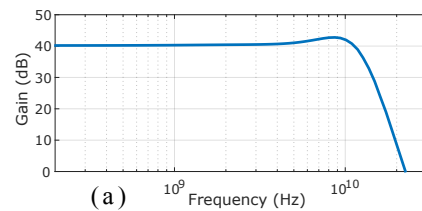


Fig. 3 (a) Frequency response of modulator driver and (b) Output impedance with different termination network

Measurement results: The driver was designed and fabricated using the IBM 130nm CMOS process with the complete chip design including all pads having an area of 0.72mm^2 . The performance of the driver was measured with electrical signal testing and integrated electro-optical testing. The driver circuit integrated with an MAM using bonding wires is shown in Fig.4 where the MZM used is a 1mm long version from [5].

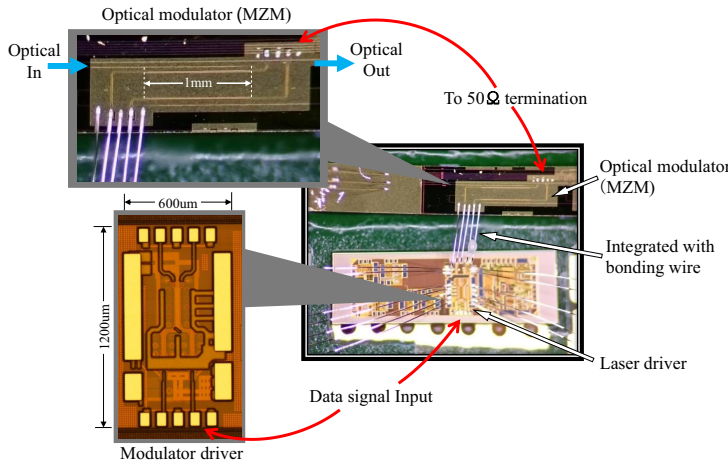


Fig. 4. Modulator driver integrated with optical modulator

The initial results were based on purely electrical testing of the driver where the input signal was a $2^{15} - 1$ differential NRZ pseudo random bit sequence (PRBS) signal and delivered to the driver IC via a coaxial cable and RF probe. The output of the driver was fed into a digital communications analyzer (DCA) with 50Ω input impedance via an RF probe, DC block capacitor and coaxial cable. Light is coupled to and from the MZM by optical fibres during elec-optical testing. A 50Ω AC termination after MZM was provided via a RF probe.

The electrical measurements at 20Gbit/s are shown in Fig.5(a). The single ended eye open-amplitude was measured to be 1.72V and the differential was 3.4Vpp.

The optical measurement results based on the driver connected to a 1mm MZM are shown in Fig.5(b). The optical power is 2.31mW at logic 1 and 0.79mW at logic 0. The measured noise level (NL) of the measurement

set up is $90\mu W$. Optical extinction ratio is given by,

$$ER = 10\log_{10} \frac{P(1) - NL}{P(0) - NL} = \frac{2.3mW - 0.09mW}{0.79mW - 0.09mW} = 5.01dB.$$

Power consumption of modulator driver is 312mW at 20Gbit/s transmitting. Power consumption of the pre-driver stages (1.6V power supply) is 164mW and the output stage (3.3V power supply) power consumption is 148mW.

Conclusion: In this paper, a modulator driver design for 50Ω transmission Mach-Zehnder Modulator has been achieved by exploiting an N over N cascode architecture at the output stage and an RCL termination network. Moreover, compared to previous work (shown in Table2), this driver circuit has been implemented with relatively low power and low cost. Demonstration of the electrical and electro-optical performance shows that this driver is capable of enabling 20Gb/s optical interconnection with MZM.

Table 2: Related work compare

	[2]	[1]	[3]	[6]	this work
CMOS Process	180nm	130nm	45nm SOI	32nm SOI	130nm
Speed (Gbit/s)	10	20	40	30	20
Output swing	6V	7V	4V	2V	3.4V
Power (mW)	600	900	437	—	148
External biasing	Yes	Yes	—	No	No

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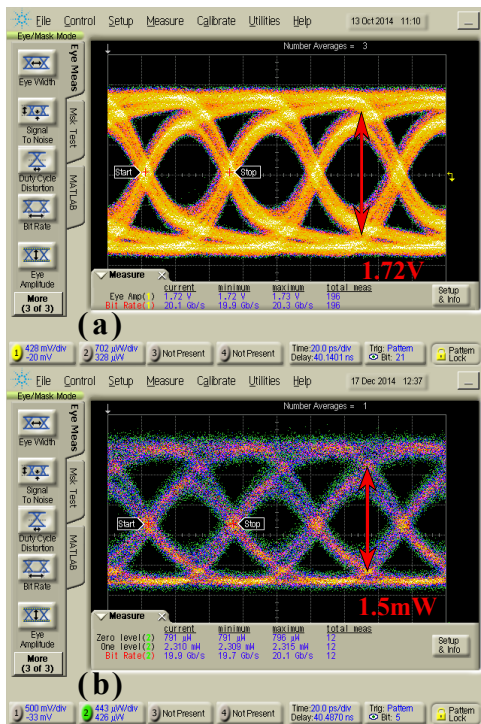


Fig. 5 Modulator driver (a) electrical measurement and (b) optical measurement (integrated with 1mm MZM) at 20Gb/s