University of Southampton

FACULTY OF PHYSICAL SCIENCE AND ENGINEERING

School of Electronics and Computer Science

Sub-micron texturing for photovoltaic antireflection and light-trapping

by

Mehdi Banakar

A thesis for the degree of Doctor of Philosophy

April 2015

UNIVERSITY OF SOUTHAMPTON

ABSTACT

FACULTY OF PHYSICAL, SCIENCE & ENGINEERING
SCHOOL OF ELECTRONIC & COMPUTE SCIENCE

Doctor of Philosophy

SUB-MICRON TEXTURING FOR PHOTOVOLTAIC ANTIREFLECTION AND LIGHT-TRAPPING

by Mehdi Banakar

The photovoltaic solar energy industry has experienced substantial growth over the last few years and this growth has led to manufacturing cost reductions that have brought solar energy to grid-parity in many parts of the world. Grid parity will inevitably lead to further expansions of the industry as uptake of the technology will no longer be subsidy driven. As the industry continues to mature, scientific and technological innovations that reduce the $/Watt cost of solar energy will allow companies to gain a competitive edge and increasingly ensure that solar energy can become affordable for communities in the developing world. Development of antireflection and light-trapping schemes that can help increase efficiency or else decrease material requirements of solar cells are one way that science and technology might contribute to the drive for reduced $/Watt.

Three novel types of sub-micron scale texturing are examined in this work. In each, advanced nanofabrication techniques, specialist characterisation apparatus and complex simulation software are used to gain insight into these new structures.

Sub-micron inverted pyramid structures formed in silicon by a combination of e-beam lithography and a Potassium hydroxide (KOH) etch are found to have a significant antireflective effect. The best structures are found to have a weighted reflectance of 10% when the periodicity is 700 nm, when the spacing between pyramids is as small as possible, and when a thin layer of SiO_2 is added as a antireflection coating. Further reduction of reflectance is only possible by increasing feature size and there appear are no low-reflection sweet spots in sub-micron designs.

Mie Resonator structures were formed in silicon by a combination of e-beam lithography, lift-off and reactive ion etching through a metal hard mask. We have found that the best structures, consisting of arrays of silicon cylinders with diameters of 180nm, heights of 95 nm and periodicity of 500 nm, have weighted reflectance as low as 5.5% and, in fact, better than silicon moth-eye structures. Mie resonator structures seem to provide a very promising antireflective surface that also confer light-trapping effects. The structures be easier to fabricate that moth-eye structures while significantly reducing the silicon wastage associated with micron-scale inverted pyramid technologies that are conventionally used.

Finally, we have carried out an investigation of a self-forming silicon nanowire surfaces that can reduce weighted reflectance to values as low as 0.05% although these are impressive antireflective surfaces that might find application in some optoelectronic systems where scattered light should be reduced, we have concluded that the nanowire structures are unlikely to help solar cell design as increased surface area and surface contamination and damage is likely to greatly increase surface recombination and limit device efficiencies.

In conclusion, it is clear that Mie Resonator structures are amongst the most promising antireflective surfaces and further studies should focus on optimisation of light-trapping and device integration of these structures. The use of Mie resonator structures might eventually allow Crystalline Silicon (C-Si) wafer thickness to decrease to a few microns without reduction in device efficiency.

Contents

List of Figures

List of Table

List of Acronym

1-Methyl-2-pyrrolidon (NMP)

Air Mass 1.5 (AM1.5)

Angle Of Incidence (AOI)

Antireflection (AR)

Antireflection coating (ARC)

Angular Resolved Spectroscopy (ARS)

Back Surface Field (BSF)

Cadmium sulfide (CdS)

Cadmium telluride (CdTe)

Computer aided design (CAD)

Copper indium gallium (di)selenide ($CuInGaSe_2$) (CIGS)

Copper Zinc Tin Selenide (CZTS)

Crystalline Silicon (C-Si)

Direct current (DC)

Discrete Dipole Approximation (DDA)

Double Layer Antireflection (DLAR)

Dye-Sensitised Solar Cells (DSSCs)

Field Emission Scanning Electron Microscopy (FEGSEM)

Finite Difference Time Domain (FDTD)

Gallium Arsenide (GaAs)

Heterojunction with Intrinsic Thin layer (HIT)

Hydrofluoric (HF)

Inductively Coupled Plasma (ICP)

Integrating Sphere (IS)

Internal Quantum Efficiency (IQE)

Inverted Pyramid (IP)

Isopropyl alcohol (IPA)

Light-Trapping (LT)
Low-Pressure Chemical Vapor Deposition (LPCVD)

Maximum current (I_M)

Maximum Power Point (MPP)

Maximum voltage (V_M)

Metal–Oxide–Semiconductor (MOS)

Methyl isobutyl ketone (MIBK)

Methyl methacryllate (MMA)

Microelectromechanical systems (MEMS)

Multicrystalline Silicon (mC-Si)lilapar

Nanopillar (NP)

National Renewable Energy Laboratory (NREL)

Open-Circuit Voltage (V_{OC})

Organic Photovoltaics (OPV)

Physical vapor deposition *(*PVD)

Photon Flux Density (PFD)

Passivated Emitter Rear Locally diffused (PERL)

Passivated Emitter and Rear Cell (PERC)

Perfectly Matched Layer (PML)

Photovoltaic (PV)

Poly Methyl Methacryllate (PMMA)

Potassium hydroxide (KOH)

Polytetrafluoroethylene (PTFE)

Radio Corporation of America (RCA)

Radio Frequency (RF)

Reactive Ion Etch (RIE)

Scanning Electron Microscopy (SEM)

Shockley-Queisser (SQ)

Short-Circuit Current (I_{SC})

Single-Layer Anti-Reflective (SLAR)

University of New South Wales (UNSW)

Vapour-Liquid-Solid (VLS)

Wavelength and Angle Resolved Spectroscopy (WARS)

Weighted Specular reflectance (*WSR*)

Declaration of Authorship

I, MEHDI BANAKAR, declare that the thesis entitled

SUB-MICRON TEXTURING FOR PHOTOVOLTAIC ANTIREFLECTION AND LIGHT-TRAPPING

and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as:

1. *M. Banakar, Stuart A. Boden, Asa Asadollahbaik ,David N. R. Payne, and D. M. Bagnall.* ***Angle-Resolved Reflection Spectroscopy of Sub-Wavelength Surface Mie Resonators.*** In *Solar14: 52nd annual Australian Solar Council Industry Conference & Exhibition, Melbourne, AU, 08 - 09 May 2014.*
2. *M. Banakar, Stuart A. Boden, Asa Asadollahbaik ,David N. R. Payne, and D. M. Bagnall.* ***Angle-Resolved Reflection and Scattering Studies of Sub-Wavelength Surface Mie Resonators.*** In *PVSAT-10: 10th Photovoltaic Science Application and Technology Conference , Loughborough, GB, 23 - 25 Apr 2014.*

3. *M. Banakar, S. Aghdaei, S. A. Boden, I. Sari, and D. M. Bagnall*. ***Silicon nanowires by self-organised reactive ion etching.*** In *8th Photovoltaic Science Applications and Technology Conference, Newcastle upon Tyne, GB, 02 - 04 Apr 2012.*

4. *M. Banakar, O. D. Clark, and D. M. Bagnall*. ***Variable angle spectroscopic ellipsometry used to optimise thin film silicon and ITO layers***. In *5th Photovoltaic Science Applications and Technology Conference, Wrexham, GB, 01 - 03 Apr 2009.*

Signed: ……

Date: …….....

Acknowledgements

This PhD was particularly interesting for me and I have enjoyed the challenges of both the theory and the laboratory work. I cannot thank you all enough, all of those who have supported me and helped me throughout this time.

I would like to express my sincere gratitude to my supervisor, Prof. Darren Bagnall, for his unending guidance, support, enthusiasm and encouragement, throughout the duration of this project. I would also like to thank his family; Sue Gerty and Jos Bagnall, for their kindness and patience and for making me feel welcome, both in Southampton and Sydney. Special thanks must go to Dr Stuart Boden, who gave his time so generously and who supported me during the entire PhD. I would also like to thank the technical staff at the Southampton Nanofabrication Centre, especially Peter Ayliffe for technical help, and Dr Owain Clark and Denny Jack for technical support, training and advice during my fabrication. Also I would like to thank Dr David Payne for his help with FDTD simulation and optical measurements.

Thanks also to Prof. Darren Bagnall's group, including Dr Tristan Temple, Farrah Djidjeli, Dr Steffi Sesuraj, Dr Asa Asadollahbaik, Dr Akhtar Rind, Dr Petros Stavrolakis, Lee J Crudgington, Amirjan Nawabjan, Athanasios Gousiopoulos and in particular, thanks to Dr Michael Pollard for his help with optical measurements.

I would like to thank the students, academics and secretaries, Glenys Howe and Lucia Hewitt, in the Nano Group. Special thanks must go to Dr Ibrahim Sari, Dr Stuart Pearce and Chirenjeevi Krishnan, for their help and fabrication advice and also for their friendship. Thanks are also due in no small way to Dr Sara Aghdaei for all her friendship and support.

I would also like to thank all of my friends for their patience and support, during difficult times.

Finally I would like to thank my family, especially Mum and Dad for their endless love and all the support and encouragement they have given me.

1.Introduction

1.1. Current status of solar energy

In the last few years the photovoltaic (PV) industry has demonstrated year-on-year increases in installation capacity of more than 60% (Figure 1.1) [1] so now there is over 30Giga watt power of installed capacity and a total solar market of over a $100 Billion *per annum.* The total installed capacity PV in Germany is now at such a level that there are times, typically at midday on Sunday in the springtime, when solar energy provides as much as 50.6% of the total electricity that is being consumed (Figure 1.2)[2]. At the same time the cost of solar electricity in $/Watt has decreased to the point at which solar electricity in many regions of the world are comfortably at or below grid parity Figure 1.3.

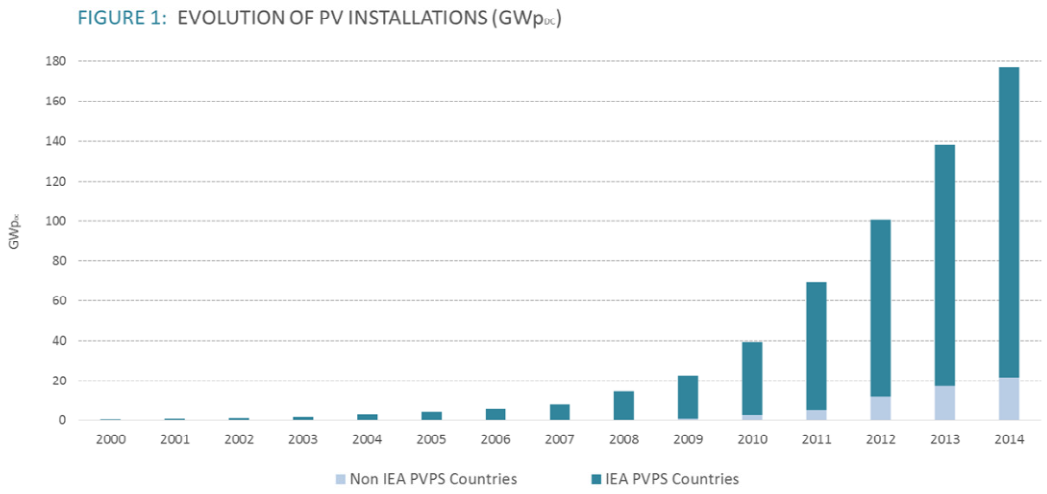


Figure 1.1. Evolution of PV installation [1].

These facts tell us; that solar energy is a very significant and substantial industry, that solar energy is becoming a major component of peak electricity demand and has removed some of the dependence on conventional power plant. Much of the progress over the last 3 decades has been possible as successive governments, most notably in Japan, Germany, and now China and Taiwan [3-5] have been prepared to subsidise the solar industry by feed-in tariffs or other mechanisms, however the reality of grid parity means that ongoing investment in solar can be made on purely economic grounds.

We no longer have to argue for solar because of its green or limitless credentials. As far as the homeowner is concerned the installation of solar panels will provide cost savings over the lifetime of the panels that exceed the cost of installation. That homeowner will still rely upon conventionally provided grid-electricity or else some expensive storage mechanism to get through the winter and the night-time. Electricity companies will still for a little while longer find electricity cheaper to produce using coal or gas and in any case will require a range of conventional and renewable energy sources to guarantee supply and energy security.

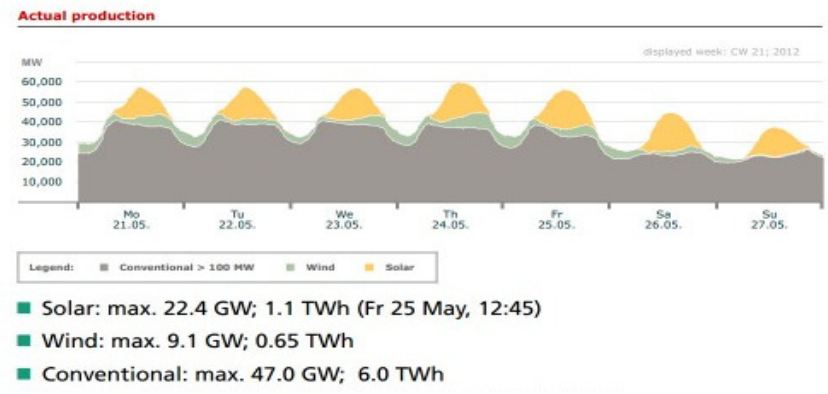


Figure 1.2. Solar Energy contribution to total power Germany for week 21, 2014 [6].

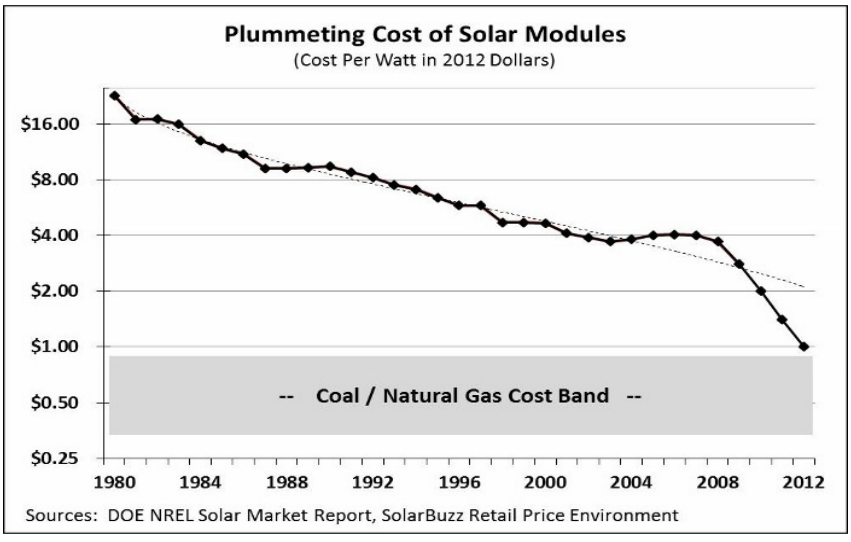


Figure 1.3. Cost of solar module from 1980 to 2012 [7].

Increasingly photovoltaic companies will seek to gain market advantage and improve margins, with huge economic incentives we can anticipate photovoltaics continuing to scale in volume and decrease in cost for many years to come. Modest decreases in production costs or modest improvements in efficiency will be hugely important. Reduced cost will largely come about by scaling, as production volume increases costs can often reduce significantly [8]. Improved efficiency will come about with scientific and technological innovation. In fact, as scaling reduces the cost of the semiconductor device, the fixed costs, known as the balance-of-systems costs become an increasingly important component that is relatively fixed and as a consequence the pay-back time can be substantially reduced by higher efficiencies [9]. Devices with efficiencies less than 10% are probably not economically viable no matter how cheaply they can be manufactured.

Although there are as many as 30 different photovoltaic device technologies, each with special reasons to justify ongoing research it is the *first generation devices* [10] based on either crystalline silicon (C-Si) wafers or multicrystalline silicon (mC-Si) wafers that are, and always have been, the most dominant commercial technology, accounting for as much as 90% of the world PV market [11].

The National Renewable Energy Laboratory (NREL) maintain a chart that plots solar cell efficiency of all the main technologies as a function of year (Figure 1.4)[12].

In the NREL plot it is interesting to note that the bulk of current commercial cells are largely based on ~18% efficient University of New South Wales (UNSW) technologies of the mid 1980's. Although UNSW had refined their approach over many years the current C-Si device record of 25% has been held since 1997 [13, 14] in fact all of the C-Si devices with over 20% efficiency are currently too expensive to mass produce but do have markets for specialist applications.

In fact, all of the device technologies that lie above the C-Si line in figure 4 are currently too costly for most applications. These high-efficiency devices include single-junction Gallium arsenide (GaAs) and a variety of multi-junction devices. With a direct bandgap and excellent transport properties GaAs is in principle a very good semiconductor for photovoltaic devices however GaAs wafers are expensive and processing of GaAs is expensive when compared to silicon, there are no viable single-junction GaAs devices[15].

Third generation solar cells are high-cost high-efficiency devices that might use a range of possible mechanisms to produce efficiencies far greater than can be achieved using conventional single-junction architectures. All the devices that lie above single junction GaAs in the NREL plot are *multi-junction devices* and are the only scientifically proven third generation devices. Although multi-junction solar cells based largely on III-V semiconductors are impressive technological achievements they cannot compete with C-Si for $/Watt even when large lenses or mirrors are used to focus the light of many suns onto the active device.

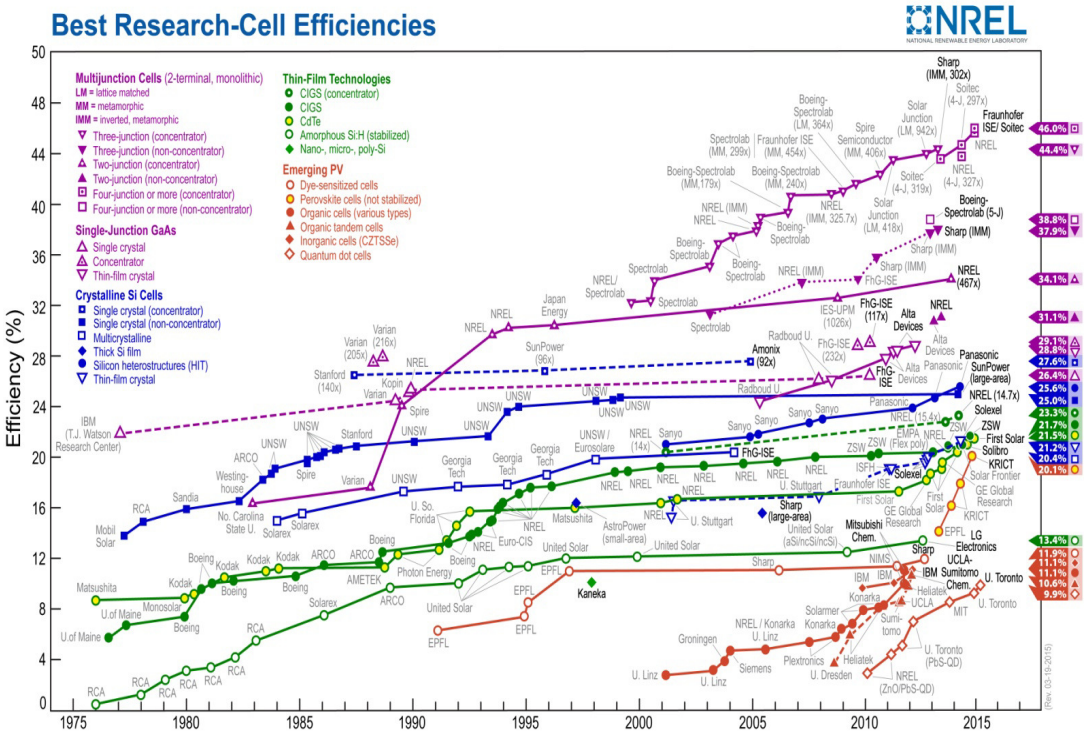


Figure 1.4. NREL maintain a chart that plots solar cell efficiency of all the main technologies as a function of year [12].

All of the devices below mC-Si in Figure 1.4 belong to the *second generation*[10]. These are thin film devices that are generally deposited onto cheap substrates and are in principle much cheaper to manufacture than first generation devices but are always likely to be relatively low in efficiency.

Of the thin film technologies there are three types of device with long research histories: thin film silicon, Cadmium telluride (CdTe) / Cadmium sulfide (CdS) and Copper indium gallium (di)selenide ($CuInGaSe_2$) (CIGS).

The thin film silicon technologies are cheap to produce but have struggled to find stable efficiencies over 10% even when multiple junctions are used, and although small lab-scale CIGS devices have produced efficiencies of 20.3%[16] module efficiencies have proved difficult to maintain over 14% and the complexity of fabrication for a quaternary alloy is perhaps too challenging at low cost [17].

Currently only CdTe devices offer a commercial second generation alternative to wafer silicon, with First Solar claiming a total of over 10 Giga Watt installed worldwide [18]. Figures from 2013 show First Solar producing 2 Giga Watt per year, which represented around 5% of the global photovoltaic production [4].

As yet the relatively new second generation devices: organic photovoltaics (OPV), dye-sensitised solar cells (DSSCs), quantum dot solar cells and copper zinc tin selenide (CZTS).

CZTS solar cells have yet to demonstrate module efficiencies above 10%.

The most exciting of new technologies at this time are the Perovskite devices that have emerged in the last few years to achieve remarkable 20.1% efficiencies [12, 19], it is early days for these devices and although these early efficiencies are impressive, devices are still small area and there are degradation issues [20].

At this time, we can anticipate C-Si devices maintaining and perhaps extending their domination over the next few years with only CdTe at levels or trajectories to mount a significant technological challenge.

For each of these dominant or promising technologies *antireflection* and *light-trapping* schemes are increasingly important. Any device technology must employ an antireflection scheme or else risk losing up to 30% of useful light at the first significant interface. Meanwhile light-trapping schemes can allow for thinner devices and enhanced device properties and cheaper production. Very thin (<20μm) C-Si solar cells produced by kerfless technologies [21] represent one possible future for the mainstream technology, but must be accompanied by advanced antireflection and light-trapping mechanisms. Currently devices are typically etched with KOH to form inverted pyramids with dimensions of 10s of micron. These inverted pyramids provide an antireflective mechanism and also provide light-trapping, but as device thicknesses reduce to just a few microns alternative nanometer scale approaches must be sought.

Diffraction gratings, moth-eye antireflection schemes and plasmonic metal nanoparticles have all been extensively studied as possible mechanisms. In this study we will focus on three systems that have received less attention; nanometre scale inverted pyramids, Mie resonators and nanowire surfaces. Each of these systems are front surface concepts that have the potential to reduce reflection at the same time as scattering and thereby light-trapping.

2.Background and Literature Survey

2.1. Basic Solar Cell Operation

The “textbook” silicon wafer solar cell is a thick block of p-type crystalline silicon with an n-type region at the top of the device. The region of fixed charge (or *depletion region*) that exists on both sides of the *pn-junction*, gives rise to a built-in electric field and an associated *built-in voltage*. The rear of the device is covered by a metal suitable for the formation of an ohmic rear contact, the front contact is formed by another suitable metal patterned into fingers and optimised to maximise efficiency by finding the best trade-off between resistance and shadowing. Areas of the surface that are not covered by metal are covered by a thin transparent layer that both passivate the silicon surface and provide an antireflective coating (Figure 2.1).

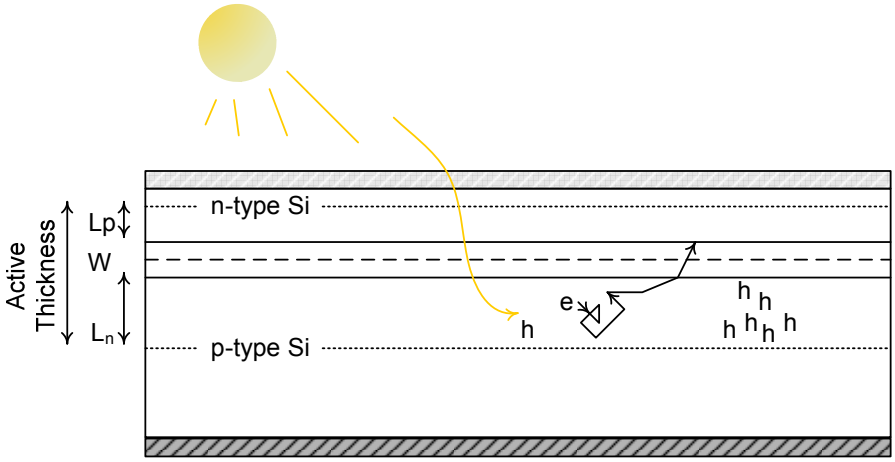


Figure 2.1 Cross section of p-n junction solar cell.

Sunlight enters the device through the top surface of the cell and is absorbed within the silicon. According to the *photovoltaic effect* [22], the spontaneous absorption of a single photon excites an electron from the *conduction band* to the *valence band* creating and *electron-hole pair*. In a solar cell the optically generated minority carriers are the key to the operation of the device. The minority carriers will have a finite *lifetime* and a finite *mobility* that will give rise to an average carrier *diffusion length*. Minority carriers generated within an average diffusion length of the pn-junction’s depletion region will on average diffuse to the depletion region.

Once at the depletion region they will be swept across by the built-in field. At this point the n-type region has one extra electron and the p-type region has one extra hole. The *active thickness* of a solar cell can be defined as the thickness of the depletion region plus the two average diffusion lengths. On average all photons absorbed within this region will provide an excess electron in the n-type region that is free to travel through an external circuit and thereby form part of a *photogenerated current* that is driven by the built-in field.

If the external circuit is a short circuit then the current through the device will be at a maximum short-circuit current (I_{SC}), if the external circuit is removed then the voltage across the device will be at a maximum open-circuit voltage (V_{OC}). The Maximum Power Point (MPP) of the device is found when the load resistance matches the internal resistance of the device, at this point maximum current, voltage (I_M V_M) provides the power output of the device. On an I/V plot (Figure 2.2) the ratio of the two rectangles (I_M V_M) /($I_{SC}V_{OC}$) define the *fill factor* and the device efficiency is the ratio of electrical power out to optical power in. In an ideal solar cell the efficiency of the cell would be 100% and every incident photon would produce an electron in the external circuit and there would be a *quantum efficiency* of 1 for every wavelength.

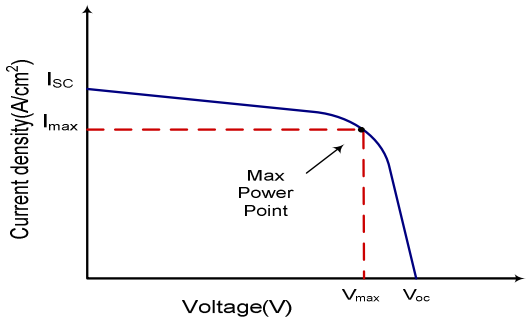


Figure 2.2. Text book I-V Curve of a solar cell.

Of course, real solar cells are far from ideal and actual efficiencies for single junction devices are in the range 0 to 28%. The limits to efficiency are to a large extent fundamental. Sunlight is broadband and in part diffuse (Figure 2.3), photons with energy much greater than the bandgap of silicon can only generate a single electron-hole pair and photons with energy less than the bandgap can not generate any electron-hole pairs. In 1966, Shockley and Queisser [23] carried out a fundamental study of the

thermodynamics of photovoltaic devices and showed that the maximum efficiency achievable by a single junction silicon solar cell would be 31% [24, 25] and that the best efficiency for any single junction solar cell made from any semiconductor would be 38%[24]. These *Shockley-Queisser* (*SQ*) *limits* are already disappointing to members of the public, and yet Shockley and Queisser did not concern themselves with the avoidable efficiency losses that render mankind's best effort silicon solar cell only 25.6% efficient [19].

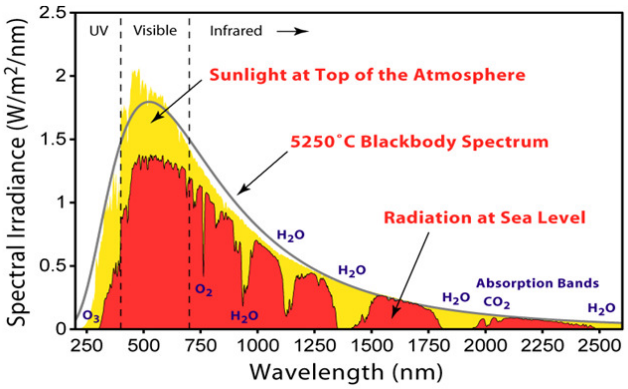


Figure 2.3. Spectral irradiance at top of atmosphere and at sea level, compared to black body spectrum for 5250°C.

These avoidable losses include: absorption in the devices surface layers, reflection, contact-shadowing, front-surface recombination, bulk-recombination, rear-surface recombination, series resistances, shunt resistances and material issues that affect the shape of the I/V curve and thereby the fill-factor that include non-ideal dark currents and non-ideal ideality factors. Every solar cell design must pay very close attention to all of these issues in order to achieve good efficiency values.

2.2. Recombination Losses

Very small defect or impurity concentrations in the silicon can dramatically reduce carrier lifetimes and increase bulk recombination rates, so the starting wafer must be carefully produced and must be expensive *solar-grade* material. Equally all processing of the wafer must be performed with close regard to possible contamination and thermal processes.

The most significant defects for a silicon solar cell are the front and rear surfaces. Here dangling bonds create mid-gap energy levels that cause significant surface recombination. The surface recombination velocity (*S*) is a measure of surface recombination and can be as high as 10,000 cms^{-1} for untreated surfaces [26, 27]. Since high-energy photons in the UV and blue spectral regions are absorbed close to the surface of a cell high front-surface recombination velocities lead to low quantum efficiencies at the short wavelengths, whereas high rear-surface recombination velocity is one factor that leads to lower quantum efficiencies at the longer wavelengths[26]. High-efficiency devices require both front and rear surface passivation that can reduce *S* to values as low as 1 cms^{-1}. There will always be some surface recombination, so, in general complex surfaces that might, for instance, reduce reflection should not increase the surface area or damage the surface or make the surface less easy to passivate.

Bulk or surface recombination are collectively considered as failures in *carrier collection* and can be mitigated by ensuring that photon absorption and thereby carrier generation takes place as close as possible to the device junction. Making a thin device is a good strategy provided there is not a significant reduction in absorption as a result.

2.3. Electrical Losses

Electrical losses include series resistance, shunt resistance and non-optimum shape to I/V curves reflected by the fill-factor and the ideality factor.

Series resistance results in a reduction in the output voltage at the maximum power point. It needs to be as small as possible, but will have contributions from the ohmic contacts, the resistance of front surface finger design and bus-bars.

Shunt resistance results in a reduction of the current at the maximum power point. It needs to be as high as possible but can be reduced from optimal values by defects that propagate through a solar cell or conductive coatings that extend around the edges of a solar cell.

Classically, the shape of the I/V curve for a diode is determined by the doping levels and minority carrier concentrations that lead to a *dark current*, or *saturation current* under reverse bias.. In practical solar cells, particularly modules, the shape of I/V curves are non-optimum because of device non-uniformities or variations of properties from device to device.

2.4. Optical Losses

Shadowing, caused by metallic front contacts is difficult to avoid for conventional devices. The finger like contacts are designed to minimise shadowing while trying to also minimise series resistance, a compromise between the two must be found and this compromise represents an unavoidable loss in practical terms. Some new generations of C-Si devices have all contacts on the rear surface to remove shadowing losses[28].

The main focus of this work will be on designs that can minimise reflection and transmission losses. One of the challenges with photovoltaics is the broadband nature of sunlight, high-efficiency silicon devices must utilise photons with wavelengths ranging from 350 nm to 1200 nm, coming from all angles of incidence and with all possible polarisation states. Optical losses for a laser source could be practically zero as photonic technologies can provide near perfect designs, the best broadband designs will always represent a compromise that accept losses at each end of the useful solar spectrum.

One of the main aspects to this study will be an investigation of *reflection losses*. According to Snell's law, equation (2.1) [29], polished silicon surfaces will reflect as much as 30% of useful incident light.

$$R = \left| \frac{n_2 - n_1}{n_2 + n_1} \right|^2 \qquad \textbf{(2.1)}$$

Any practical device must employ some form of antireflection scheme. Most simply this should be a textured surface or a single-layer antireflection coating. More complex schemes, discussed in section 2.7.1 can reduce reflection to less than 1% for most of the useful spectral range, though often the complexity of these schemes adds cost to device manufacture that cannot always be accommodated.

Transmission losses are most significant for long-wavelength light close to the band-edge. Although near-band-edge photons can in principle generate a useful electron hole pair absorption coefficients become too low. Silicon with its indirect bandgap is particularly problematic and a few hundred microns of silicon is not enough to absorb all of the light available. Simple designs can ensure that light that might be transmitted is reflected from the rear surface and the path-length effectively doubled, even better

designs would deflect light in such a way that the light is trapped by total internal reflection and path-lengths are enhanced by factors of up to 50 times[30, 31]. Light-trapping is essential for high-efficiency silicon devices and is the second consideration for this work. A review of light-trapping techniques is provided in section 2.7.

2.5. Crystalline Silicon Solar Cells

The commercially dominant photovoltaic technologies are based on silicon wafers, crystalline silicon (C-Si) produces the most efficient of these devices. Although the University of New South Wales (UNSW) Passivated Emitter Rear Locally diffused (PERL) cell has achieved a world record of 25% [13] as long 15 years ago, the very best commercial C-Si module efficiencies are 22.9% [32] and are more typically in the range 17-20%[33]. Multi-Crystalline silicon (mC-Si) wafers are much more cheaply produced, they can still provide modules up to 18.5% efficient but are more typically sold as modules in the 10-14% range [3]. Both C-Si and mC-Si devices are commercially competitive although the reducing C-Si costs and level balance-of-systems costs are increasingly favouring C-Si devices.

Most commercial cells are based on variants of Back Surface Field (BSF) [34] or more complex Passivated Emitter and Rear Cell (PERC) designs [35], most commercial C-Si cell technologies share many common features:

(1) cells are typically based on p-type wafers with a shallow n-type region close to the surface that is formed by diffusion of phosphorous. The use of a p-type substrate makes use of the higher electron mobility. Although there is increasing interest in n-type wafers, so far they have only found commercial use in 'heterojunction' or 'Heterojunction with Intrinsic Thin layer (HIT)' cells [36, 37].

(2) The regions in close contact to the front or rear contacts are heavily doped to ensure a low-resistivity ohmic contact is formed. In the case of simple cells the whole of the rear surface is directly contacted to the back of the wafer with the whole of the rear surface heavily doped (p^+).

(3) The front contacts are typically a fine "finger-like" structure of silver produced by screen printing. Though increasingly the cost of silver is leading a technological

push to alternatives such as the electroplating of copper. The rear-contacts are typically plated copper or aluminium that covers the whole rear surface[38].

Most commercial cells use a Potassium hydroxide (KOH) etch to provide a micron-scale inverted pyramid texturing with a passivating single-layer anti-reflective (SLAR) coating of SiO_2 or Si_3N_4 to minimise reflection. This same inverted pyramid scheme also deflects light as it enters the silicon and thereby extends the path-length and enables a degree of light-trapping (Figure 2.4) [39].

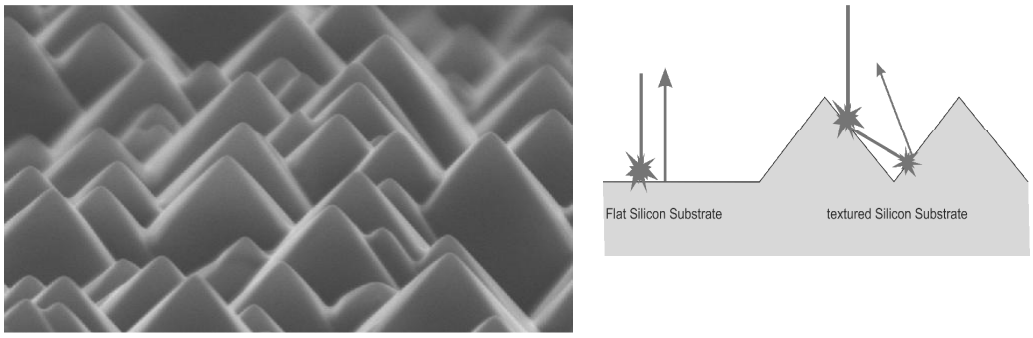


Figure 2.4. Scanning Electron Microscope (SEM) image of a textured silicon surface and schematic illustration of AR mechanism [39].

More expensive designs and techniques can be used to increase the efficiency of these typical devices. Using 'buried contacts' on the front surface allows for reduced series resistance and reduced shadowing [40, 41]. One of the major losses of efficiency for these basic devices remains recombination at the rear surface, so passivating the rear surface and then locally diffusing the heavily doped regions and contacting and thereby reducing the metal-silicon contact area can lead to improvements as demonstrated in UNSW's PERC cells [42]. Finally, lithographic definition of the front surface inverted pyramids with a double layer antireflection (DLAR) coating can replace the random texturing and SLAR with further antireflection and light-trapping enhancement [43]. This front surface is perhaps the most striking feature of the PERL cell and not only provides low reflectance it also increases absorption lengths by ensuring that most of the absorbed light is directed obliquely into the device. This careful optical design [5] reduces optical losses to less than 5% of all incident light.

The world-record holding Passivated Emitter, Rear Locally-diffused (PERL) cell (Figure 2.5) [4] embodies all of the improvements described, however, the additional

front and rear surface patterning required is much too expensive for commercial devices to utilize at this time.

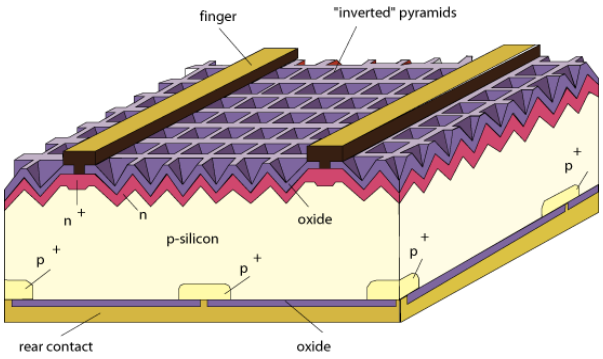


Figure 2.5. Passivated Emitter, Rear Locally-diffused (PERL) cell [4].

2.6. Future developments of C-Si device technologies

Over the next few years we can expect a continual drive towards higher efficiency and cheaper C-Si devices. The UNSW PERL cells already illustrates what is possible in terms of higher efficiency, however innovative techniques must be found to allow PERL-like devices to be produced without significant cost increases.

Meanwhile, with material cost a concern, we can expect that low-cost alternatives to silver and reduced silicon usage will increasingly provide a second set of research aims.

While silicon in itself is not expensive, the high-crystallinity, high-purity silicon that is required for solar cells is expensive and the manufacture of silicon wafers is one of the most significant cost components of a cell. There are considerable silicon related cost reductions to be found if, (1) the number of wafers per ingot can be increased by being able to utilise thinner wafers, (2) if the kerf and other waste silicon produced during diamond wire cutting and polishing processes can be reduced, (3) if the silicon lost during surface texturing can be reduced.

We can anticipate a move to the use of thinner wafers and so-called *kerfless* technologies, where cells are constructed in wafers that are 20 µm thick or less [44].

Such cells would be brittle but flexible, they would require enhanced light-trapping but preferably from nano-scale rather than micron-scale features. As well as providing improved utilisation of silicon, these ultra-thin silicon devices are also likely to have a larger V_{OC} [45] providing that light-trapping is good enough to maintain the I_{SC}.

In anticipation of the realisation of these industrial trends, this work has focussed on the fabrication, characterisation and modelling of sub-micron antireflection and light-trapping structures.

2.7. Anti-Reflection and Light-Trapping

A range of different antireflection (AR) and light-trapping (LT) techniques are commonly used or else have been intensively studied [46, 47]. Some techniques only confer an anti-reflection effect while others offer both anti-reflection and light-trapping. In this section each of the main classes of technique are discussed and both the merits and disadvantages of each considered.

2.7.1. Single Layer Anti-Reflective (SLAR) Coatings

The simplest AR technique is the single layer coating. This technique is an interference based technique in which the single layer in question sits on the surface of the silicon and has a refractive index somewhere between that of silicon and air. In order to minimise reflection for a given wavelength there should be destructive interference between light reflected from the front surface of the SLAR and the front surface of the silicon. This destructive interference has the effect of favouring transmission into the underlying cell over reflection. Typically Si_3N_4 layers of around 50 to 85 nm (depending on the exact composition of the silicon nitride) will provide an optimum AR effect at the same time as providing excellent passivation to the silicon surface.

Boden and Bagnall [48] carried an extensive theoretic study of the best SLAR materials and thicknesses by considering the performance in terms of I_{SC} for a fixed, coated cell over the course of a whole day. Showing that TiO_2 could provide the most effective SLAR With only a 4.6% loss compared to a perfect antireflection coating (ARC), and compared to a bare silicon surface with 2 nm of native oxide that would have a 19.5% loss of I_{SC}. The best Si_3N_4 layer was found to have an 8.4% loss when compared to a perfect ARC. Even bearing in mind this 8.4% figure, it is clear that the invention of

even a perfect ARC will not revolutionise photovoltaics, but PV technology is an incremental field of endeavour and every fraction of a percent gain is important provided it can be afforded.

Table 2-1 Optimized parameters for SLARs at an EVA-silicon in an encapsulated solar cell (d_{opt} is optimized) [48].

SLAR for encapsulated cell	Opt. d (nm)	JscAve (mA/cm2)	% Loss
Ideal ARC	–	22.36	0
TiO2	62.49	21.34	4.6
ZnS	65.08	21.25	5.0
TiOx	66.68	21.17	5.3
LPCVD Si_3N_4	77.45	20.76	7.1
RPECVD SiNx #2	75.56	20.47	8.4
RPECVD SiNx #3	67.92	20.34	9.0
RPECVD SiNx #1	84.64	20.06	10.3
RPECVD SiNx #4	59.11	19.58	12.4
RPECVD SiNx #5	51.30	18.92	15.4
CcO2	74.25	18.87	15.6
Bare Si with 2 nm native oxide	–	18.00	19.5

JscAve is the predicted average short-circuit current produced in a coated cell over a whole day. "% loss" is the percentage reduction in JscAve if replacing an ideal ARC (i.e. 100% transmission for all angles and wavelengths).

The study indicates that the best SLAR coatings will still suffer a loss of power of around 5%. This is a relatively small but nevertheless an avoidable loss.

The success of SLAR is limited by parasitic absorption in the SLAR and the fact that reflectance can only be minimised at a single wavelength. This wavelength can be optimised considering the Internal Quantum Efficiency (IQE) of the cell and Air Mass 1.5 (AM1.5), but there will always be losses as you move away from the central wavelength.

2.7.2. **Double-Layer Anti-Reflective (DLAR) coatings**

DLARs can allow tuning for two central wavelengths and provide more design freedom albeit at additional expense.

Boden and Bagnall [48] extended their study to find an optimum DLAR design and found that the best performing DLAR was a SiN_x/TiO_2 combination that could provide only 3.45% of lost I_{SC} when compared to a perfect ARC.

Table 2-2 Optimum parameter for DLARs in an encapsulated cell [48].

DLAR (L1/L2)	Opt. d_1 (nm)	Opt. d_2 (nm)	J_{scAve} (A/m^2)	% loss
Ideal	–	–	22.36	0
SiN_x #1/TiO_2	66.111	56.13	21.59	3.45
Si_3N_4 /TiO_2	51.34	48.61	21.55	3.64
ZnS/TiO_2	27.85	38.83	21.37	4.42

Layer 1 is the top layer, next to air. J_{scAve} is the predicted average short-circuit current produced in a coated cell over a whole day. ''% loss'' is the percentage reduction in Js_{cAve} if replacing an ideal ARC (i.e. 100% transmission for all angles and wavelengths). Only DLARs with predicted performances greater than the best SLAR

Both SLAR and DLAR coatings can provide significant improvement over a bare surface, reducing reflection losses from around 20% to around 4%. The best results are clearly for optimised DLAR schemes but these schemes are more expensive to implement as they require the deposition of two materials. Neither SLAR or DLAR confer any light-trapping effects.

2.7.3. **Inverted pyramids**

Most commercial C-Si solar cells utilise micron-scale inverted pyramid texturing combined with a SLAR to achieve the most cost-effective antireflection scheme. A relatively simple KOH process can be used to reveal <111> facets of silicon to provide a texture of "inverted pyramids" with a 54.7º slope [49]. KOH etching is an anisotropic process which is most commonly used for the etching of silicon. The KOH etch has a strong preference of crystallographic orientation, therefore the etch rate for (100) plane is significantly faster than on the (111) plane [50]. Using KOH solution on a wafer with the (100) plane at the surface will result in the formation of inverted pyramids (IP).

Figure 2.6 shows the effect of KOH on the Si crystallographic orientation. These pyramids might be 5 to 10µm wide and can be understood and modelled by simple ray-tracing. Light incident on the cell will typically meet silicon sloped at 54.7º to the vertical, much of the light will be absorbed at this point, however some light will be reflected, because of the geometry of the design the reflected light will most-likely incident upon the silicon for a second time and in fact, light can endure multiple reflections [51]. The overall result is extremely low reflectance even if the silicon is not coated. This reflectance can be further reduced by adding a SLAR (tuned to $d\cos(54.7)$ for the 54.7º angle).

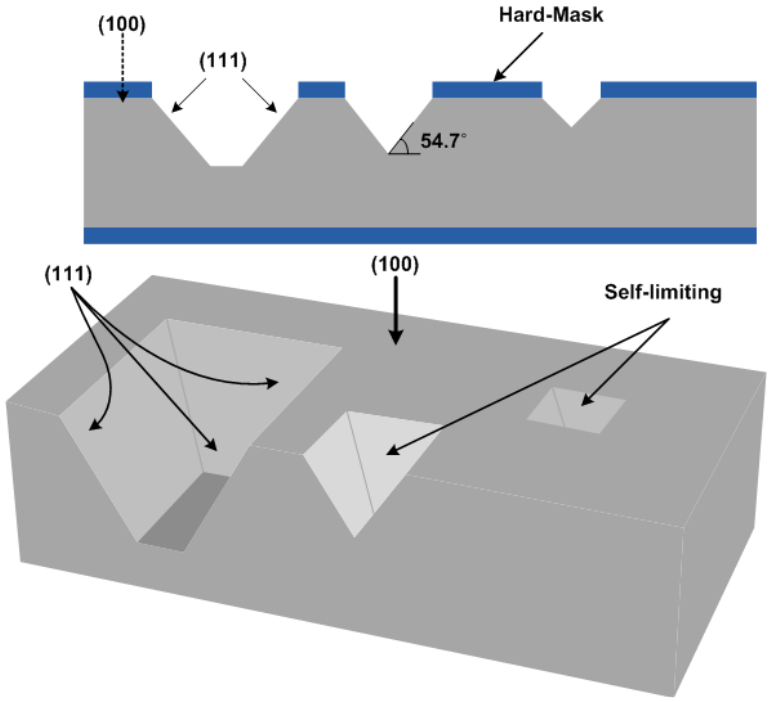
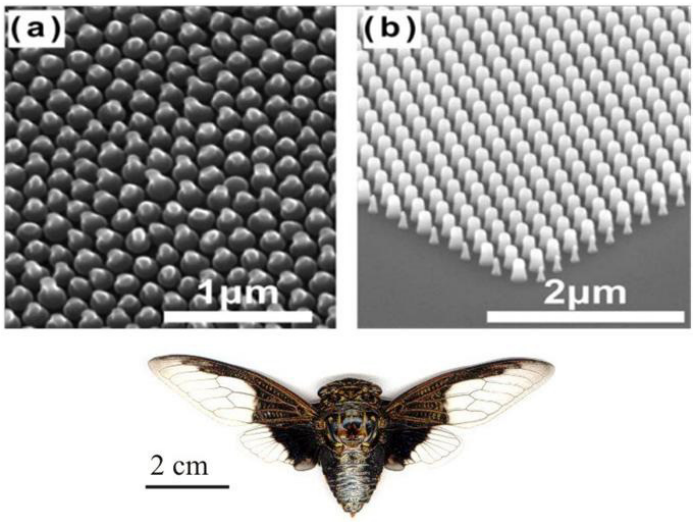


Figure 2.6. Diagram of example of (100) and (111) planes in a Si wafer with a (100) surface.

2.7.4. **Moth-eyes**

The "moth-eye" anti-reflection methodology is a biomimetic technique inspired by the nanoscale structures observed on the eyes and wings of some species of moth (Figure 2.7) [52]. Moth-eye surfaces confer broadband anti-reflection properties that are in general better than SLAR and DLAR coatings and on a par with inverted pyramids. Moth-eye surfaces have the advantage of requiring no additional material depositions as they are simply features etched into the surface of the primary absorber and at the same time need only be 200-500 nm in height.

The disadvantages include the requirement of nanoscale patterning that must be lithographically defined or self-organised, the strong dependence of reflectivity on the exact shape of the nano-features and the increase of surface area that increases surface recombination. At the same time, whereas inverted pyramids confer some light-trapping effects the sub-wavelength nature of moth-eyes ensures that all light is transmitted without scattering or diffraction so there are no light-trapping benefits to the structure.



(c)

Figure 2.7. SEM image of a moth found on transparent part of its wings(a) , (b) SEM image of artificial moth eye array on silicon and (c) Cryptotympana Aquila [53].

The mechanism responsible for moth-eye AR can be simply understood by considering the sub-wavelength features of the surface as an *effective medium* with a gradual change of refractive index, from that of air to that of silicon, for example. The photon cannot resolve individual features and experiences only a gradual change of refractive index and this results in reduced reflection. Moth-eyes are broadband with reflection only increasing at short wavelengths when the wavelength is similar to the feature size or periodicity and light is scattered or diffracted at longer wavelengths when the thickness of the effective medium is comparatively small.

Detailed modelling and experimental studies by Boden and Bagnall at the University of Southampton illustrated how the effective medium understanding of the moth-eye surface is overly simplistic and showed how modelling of the structures show more complicated dependences than can be explained by effective medium approximations [54, 55].

Boden and Bagnall [55] went on to show how moth-eye surfaces can outperform optimised SLAR and DLAR coatings (Table 2-3), but did not extend their study to inverted pyramid surfaces.

Table 2-3 Optimum parameter for SLARs, DLARs and optimized moth-eye.

Ar Scheme	J_{scAve} (A/m^2)	% loss
Ideal AR coating	22.36	0
TiO_2 SLAR	21.34	4.6
SiN_x/TiO_2 DLAR	21.59	3.5
Optimized moth-eye (period=312nm)	22.22	0.62

Performance of encapsulated cell (EVA-silicon interface) employing various AR schemes. JscAve is the predicted average short-circuit current produced by the cell over day. ''% loss'' is the reduction in JscAve compared to an ideal AR coating (100% transmission for all angles and wavelengths).

Overall moth-eye AR is an interesting mechanism but has not been adopted onto the active semiconductor layers in any commercial photovoltaic technology. However, AR effects similar to the moth-eye scheme have been conferred on the cover-glass of PV modules (BP Saturn) by the incorporation of silica beads onto the glass surface [56].

Moth-eye structures have been realised on crystalline silicon wafer solar cells [57], but were found to produce less efficient devices because the additional processing steps or increased surface area negated any beneficial AR effects. Even if moth-eyes could allow a more efficient devices, wafer silicon PV is not likely to adapt moth-eye AR in the near- or medium-term as KOH etching for the creation of highly effective inverted pyramids remains relatively inexpensive and as yet there are no cost-competitive routes for large-area moth-eye patterning, even self-assembled nanosphere or nanoimprint lithography would probably be too expensive and too difficult to implement at the rates required by the PV industry.

2.7.5. **Plasmonics**

Over the last few year plasmonic antireflection and light-trapping has been extensively investigated. Metal nanoparticles can have a strong interaction with light when the wavelength corresponds to the resonance of the particle. This resonance determines the degree of interaction and scattering cross-section and the direction and magnitude of scattering. The resonance is determined by the type of metal, the surrounding medium, the size and shape of the particles and the photonic environment of the particles. There are three principle plasmonic mechanisms that can benefit photovoltaics (Figure 2.8) [58], the first two are based on localised plasmon polaritons (LPPs) that can cause a local field enhancement that can increase absorption in the immediate vicinity of the particles, or benefit by directional scattering and thereby light-trapping. The third mechanism is based on propagating plasmons.

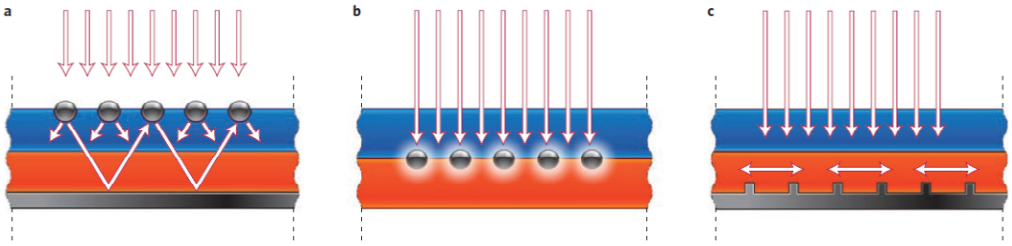


Figure 2.8. Plasmonic light-trapping mechanisms for thin-film solar cells, a, Light trapping as a result of scattering from metal nanoparticles at the front of the solar cell. Light is preferentially scattered and b, Light trapping as a result of the excitation of localized surface plasmons in metal nanoparticles implanted in the cell and c, Light trapping as a result of the excitation of surface plasmon polaritons at the metal/semiconductor interface[58].

The most successful of these mechanisms is the directional scattering approach that can also confer antireflection properties if light is preferentially scattered into the region of high-refractive index.

The challenge with all of these approaches is that the metal nanoparticles will almost always induce some parasitic absorption. Parasitic absorption is especially likely at short wavelengths, so placing particles at the surface of a solar cell is always likely to be to the detriment of cell performance. Placing particles at the back of a cell avoids the short-wavelength parasitic losses and allows the design to specifically address high-angle scattering for the difficult near band-edge photons that most require light-trapping [59]. Careful design of the shape, size and distribution of metal nanoparticles in back-reflector designs are the most promising way forward but so far success has been limited with only modest gains of thin film solar cell efficiencies being reported [60].

2.8. Aims of this Work

Professor Bagnall's group at Southampton University has had many years of experience in the fabrication, characterisation and modelling of a variety of antireflection and light-trapping schemes for photovoltaics including Single Layer Anti- Reflective (SLAR) and Double Layer Anti-Reflective (DLAR) coatings [48], 'moth-eye' biomimetic structures [53, 55] and plasmonics [59, 61, 62]. In this study we decided to utilise this collective experience and capability to investigate 3 alternative approaches to anti-reflection and light-trapping, namely *sub-micron inverted pyramids* (chapter 4), *Mie Scatterers* (chapter 5) and *nanowires* (chapter 6). In each case we are able to utilise the Southampton Nanofabrication Centre to fabricate samples and state-of-the-art characterisation such as wavelength and angle resolved spectroscopy (WARS) [63] and modelling capability including Rigorous Coupled Wave Analysis (RCWA), and *Finite Difference Time Domain* (FDTD), (chapter 3).

3.Fabrication and Characterization Techniques

A wide range of fabrication, characterisation and simulation techniques have been used throughout this work. In this chapter we describe the main tools and techniques that have been used.

3.1. Fabrication Techniques and Tools

3.1.1. Reactive Sputtering

Many silicon device process flows require the rapid deposition of thin film silicon dioxide and silicon nitride. These dielectric layers are commonly used for isolating components and structures from each other within a circuit design, to form the gate insulator within Metal–Oxide–Semiconductor (MOS) transistors. As we have seen in section 2.7 silicon nitride are often used as passivation and antireflective layers in PV, it is also often used for *hard masking* during localised doping processes such as diffusion, ion implantation and during etching processes. In this work silicon nitride layer has been used extensively for hard masking of regions during etching processes[64].

In this investigation, the deposition of dielectric materials is performed using reactive sputtering. Sputtering is a deposition process whereby atoms are ejected from a solid target material due to bombardment of the target by excited energetic particles. A glow-discharge plasma is created within an atmosphere of argon, which creates a region of highly energetic argon ions. These ions are accelerated towards the copper cathode which is bonded to the sputtering target, resulting in the ejection of the target atoms. These are then deposited on the substrate surface.

The Leybold Optics Helios Reactive Sputtering system[65], is configured for surface coating of dielectric, metallic and plastic substrates (flat or slightly curved) by means of cathode sputtering under vacuum. The principle features of sputtering are illustrated in the Figure 3.1.

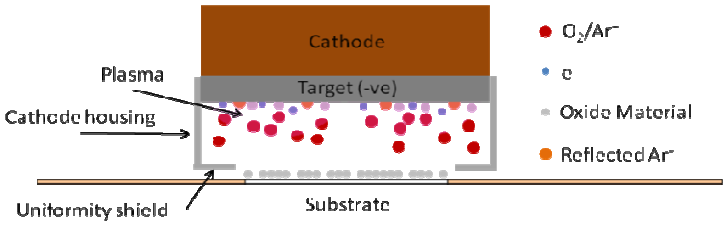


Figure 3.1. Schematic illustrating the principles of reactive sputtering in Leybold Optics Helio[65].

3.1.2. E-Beam Lithography

On many occasions throughout this work electron-beam lithography has been used to transfer a nanostructure design onto a sample. E-Beam Lithography uses a beam of focused electrons to expose a resist which is sensitive to electrons. The e-beam lithography technique allows the definition of sub-micron features down to 20nm or less, with the flexibility to freely repeat or optimise the designs. In this work, the JEOL JBX 9300FS is configured to define patterns generated using Tanner L-Edit [66].

The generated pattern data from the L-edit software is imported into the lithography software tool Beamer, which prepares the defined patterns for verification and optimization. The software also reduces the impacts of adverse effects that may occur due to beam positioning between shapes, filling shapes with "shots" on a discrete grid, field position dependent aberrations, stitching between field proximity, and process effects. At the final stage the software optimises the data for exposure and formats data for processing by the e-beam system.

3.1.3. Evaporation LAB 700

The deposition of chromium for metal lift-off processing has been performed using the Leybold Optics LAB700 e-beam evaporator. This system consists of a large vacuum chamber maintained at room temperature, which is pumped to a vacuum level of 10^{-5} to 10^{-7} mBar. An electron beam source is directed to a crucible containing chromium granules which are heated to melting point by the beam. This causes the material to vaporize and condense on the substrate which is suspended above. The substrate rotates within a planetary substrate mount inside the chamber to ensure a uniform coating, the thickness of which is determined using a crystal sensor mounted adjacent to the substrate (Figure 3.2). The large distance between the crucible and the substrate leads to

highly directional deposition (little side wall coverage) making it suitable for the lift-off process[67].

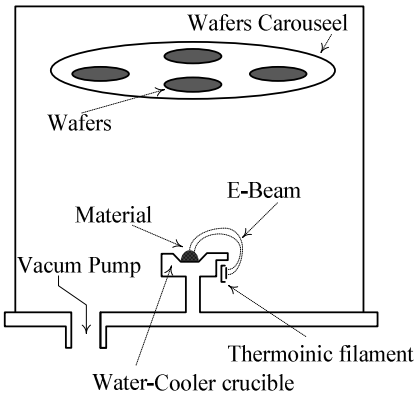


Figure 3.2. Sketch of Lab 700 chamber system.

3.1.4. **Reactive Ion Etching**

After e-beam patterning, regions of silicon nitride layers must be etched. The Reactive Ion Etch (RIE) [68] capacitive plasma-etching system places the sample to be etched on top of one of two parallel electrodes. The plasma is generated at the standard 13.56MHz, and will create an ion density of around 10^{10} cm^{-3}.

Within the plasma, electrons and ionized molecules are highly mobile. As a positive Radio Frequency (RF) cycle is applied to the electrode, the electrons accelerate towards it, while a negative bias causes them to be repelled and attracted to the grounded chamber walls. The reverse occurs to the positively-charged ionized molecules. As the electrons are much lighter and therefore more mobile, greater numbers of them are attracted towards the electrode than ionized molecules. The electrons enter the positively-biased electrode, and this causes a net negative Direct current (DC) bias to be generated between the electrode and the grounded chamber. The region around the electrode therefore becomes depleted of electrons and becomes positively charged.

The applied electric field therefore accelerates the positive molecules towards the negatively charged electrode, which collide with the sample placed on top. The method of etching is either *sputter etching*, in the case of non-reactive process gases such as argon; *reactive ion etching* with the use of reactive chemical etchants such as CF_4, SF_6, and CHF_3.

3.1.5. KOH Etching

Section 2.7.3 described how inverted pyramid structures can be readily formed by the use of a potassium hydroxide (KOH) etch.

In this work, the KOH solution was produced by dissolving reagent grade pellets of KOH in de-ionized water to a concentration of 40 wt.%. Table 3-1 illustrates the etch rate of KOH for a selection of silicon crystallographic planes, at concentrations of 30 – 50% at 70°C. Concentration is measured by a specific gravity hydrometer, and maintained using a re-condensing lid and recirculation pump. The solution is held in a temperature-controlled bath at 70°C. Polytetrafluoroethylene (PTFE) holders suspended samples in the etching bath. Oxygen was bubbled through the solution to discourage the build-up of hydrogen on the surface of the wafer, which can affect surface morphology [50, 69].

Table 3-1 Etch rates of KOH to Si planes at 70°C [50].

Si Planes	Rates at Different KOH Concentration (μm/min)		
	30%	40%	50%
(100)	0.797	0.599	0.539
(111)	0.005	0.009	0.009

3.1.6. Inductively Coupled Plasma (ICP) Etching

Inductively Coupled Plasma (ICP) etching offers several advantages over a conventional RIE system. There are two RF generators, one remote generator which creates the gas plasma and another which controls the RF field which directs the ions towards the sample surface. This allows separate control over the ion plasma density and the wafer bombardment energy through the two controls.

The advantages of this arrangement are the ability to form a plasma with a very high ion density ($>10^{11}$ cm^{-3}), while applying a much lower ion acceleration field on the substrate surface. This allows for much higher etching selectivity, greater etch rates, and lower surface damage compared to a high-power RIE etch, and provides much greater process flexibility [70].

The ICP tools have access to 6 gases including C_4F_8, SF_6, Ar and O_2, the list of the gases with MFC (Mass Flow Controller) is presented in Table 3-2.

Table 3-2 List of the gases available to the ICP system with MFC gas flow.

Gas	MFC Max (sccm)
C4F8	50
CHF3	50
CF4	50
SF6	50
Ar	100
O_2	100

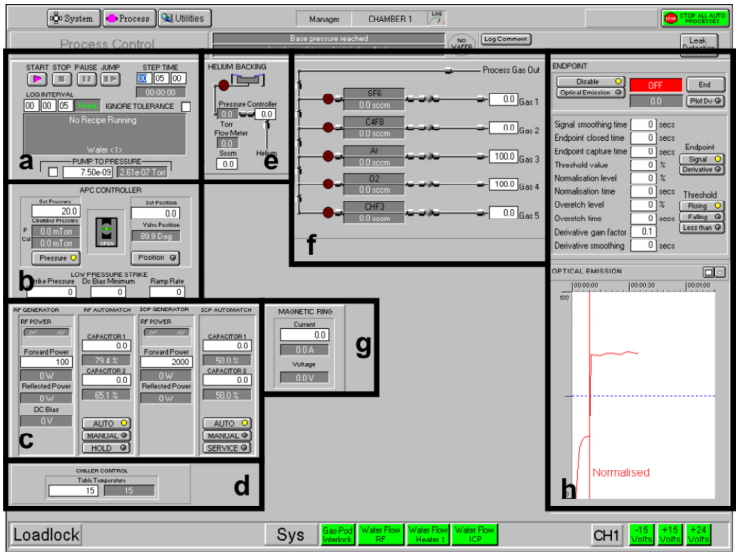


Figure 3.3. The process chamber control screen with highlighted detail (a) Recipe step process information, (b) APC control, (c) ICP and platen RF power/tuning (d) platen temperature (e) helium rear side cooling flow and abort limit (f) actual and desired gas flows (g) DC electromagnet current (plasma confinement) and (h) OES endpoint detection.

The ICP tool is fully automated and control is by a PC2000 user interface running on PC. Figure 3.3 shows a screen shot of the process chamber control screen with highlighted detail for a typical process.

3.2. Optical Characterisation Techniques and Tools

3.2.1. Reflectance Probe

A reflectance probe technique has been used to measure the reflectance spectra (Figure 3.4). The Ocean Optics probe delivers light from a white light source (HL-2000 tungsten-halogen, Ocean Optics) to the sample through six optical fibres. A central optical fibre collects a proportion of light reflected from the sample and delivers this to a spectrometer (USB4000, Ocean Optics). Bare silicon is used as a reflectance standard and a theoretical reflectance spectrum was used to provide absolute reflectance (R_{sam}) as a function of wavelength (λ) (Equation (3.1).

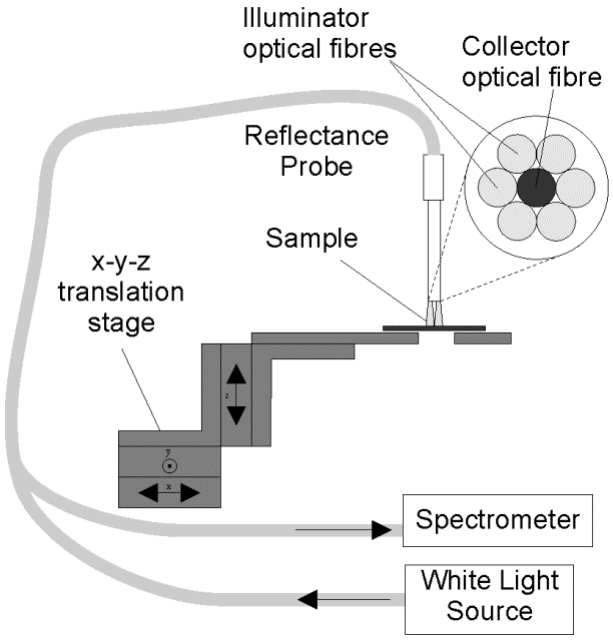


Figure 3.4. Schematic of reflectance probe measurement [46].

$$R_{sam} = \frac{I_{sam}(\lambda) - D(\lambda)}{I_{sta}(\lambda) - D(\lambda)} \times R_{sta}(\lambda) \qquad (3.1)$$

Here, I_{sam} and I_{sta} are the reflected intensities from the sample and standard, respectively, D is the dark intensity and R_{sta} is the theoretical reflectance of the standard (polished Si) [46].

3.2.2. **Integrating Sphere**

The measurement of optical reflectance is primarily performed using an Integrating Sphere (IS)[66]. This apparatus consists of a spherical chamber with the internal surfaces coated in a highly reflective Polytetrafluoroethylene (PTFE) material, which results in a homogenous distribution of optical radiation by means of multiple reflections from the sphere surfaces.

The sphere can be configured in a variety of arrangements for the measurement of transmission, reflection, absorption and total integrated scatter. A radiation source is directed at the input aperture, on which a sample can be located for measurements of transmittance, or on the rear port from which measurements of reflectance can be made. Measurements are normalised from a reference with no sample mounted and are performed within a dark cabinet to exclude all other light sources.

Measurements of diffuse transmittance and reflectance can additionally be performed, using a light trap apparatus which serves to eliminate zero-order (specular) transmission, so that only the diffuse radiation remains. For transmission, the light trap is mounted at the output port, which excludes light transmitted between the centre of the input port and the edges of the output port, whilst for reflection the light trap is mounted on a third observation port and the angle of the sample at the output port is adjusted accordingly which present it in Figure 3.5.

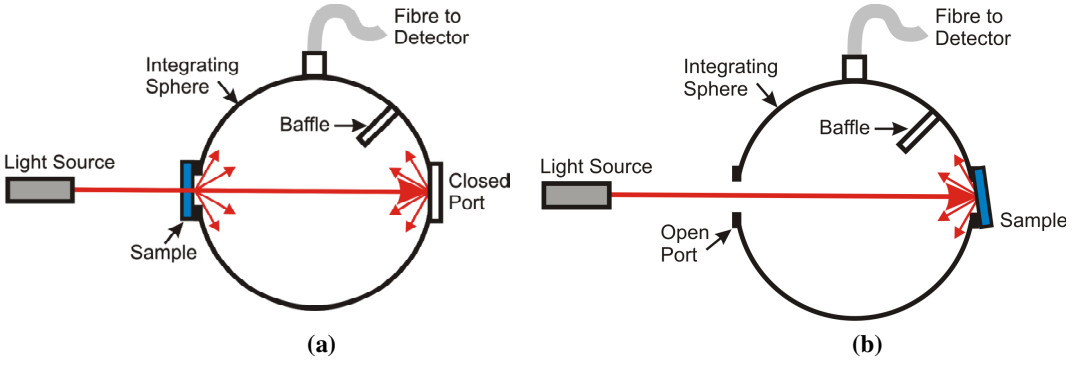


Figure 3.5. Integrating sphere set to measure (a) transmission and (b) reflection [66].

Hemispherical reflectance spectra of samples at an angle of incidence of 8° were measured using the integrating sphere (RTC-060-SF, Prolite Labsphere) and a supercontinuum laser (Fianium SC450). This technique enables the collection of both diffuse and specular reflected light from a sample mounted on the rear port. A fibre is used to couple a proportion of this light to a spectrometer (BTC112E, B&W TEK, Inc.) for spectral analysis.

3.2.3. **Angular Resolved Spectroscopy (ARS)**

A more detailed assessment of the transmittance and reflectance of a particular sample can be gained using an angle resolved scattering technique. A bespoke apparatus for the wavelength-dependant measurement of angular reflectance has been assembled at Southampton [66, 71]. The sample is illuminated at normal incidence using a laser source, and spectra are then recorded at angle intervals from the normal Figure 3.6.

The angular resolved technique provides a representation of scattering into a single two dimensional plane, perpendicular to the sample surface. For the case of randomly textured surfaces, scattering is roughly isotropic and the two dimensional `in plane' measurement is likely to provide similar results for all azimuth rotations of the sample.

The apparatus consists of; a Fianium supercontinuum white light laser covering wavelengths from 450 nm to 1800 nm, computer controlled motorized stages (Newport), a visible spectrometer (BWTEK), and a set of polarisers and focusing lens provided by THOR Labs.

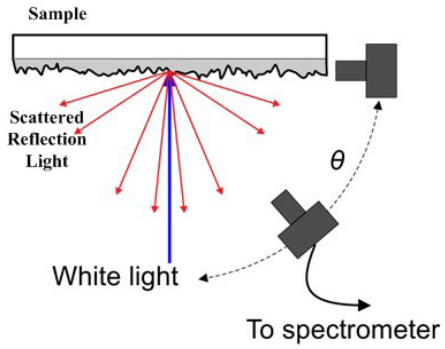


Figure 3.6. Schematic of experimental arrangement for ARS measurement.

The maximum continuous wave equivalent power of the laser over the visible spectral range is 289 mega watt. Using such a high-power saturates the output spectral signal, providing reduced information of absorption properties of the sample and in some cases may even damage the sample. It is therefore necessary to accurately control the laser power output to obtain suitable low-power intensity with required polarisation without modifying the spectral shape. For this purpose two Glan-laser polarisers are utilized due to their high damage threshold, wide field of view (~40º), high extinction ratio (100,000:1) and a broad operating spectral range of 350 nm to 2300 nm.

The laser power and incident polarization state can be controlled by adjusting the angle between the two polarisers. The polarised white light is then guided through an iris diaphragm (via a periscope) which blocks out the stray beams associated with partial back reflected beams from the polarizers.

In assuring the precision of the optical measurement, automated computer controlled stages are as important as laser power stability. Three high precision motorized linear stages and three motorized rotary stages which have a minimum incremental motion of 0.1μm and 0.005º, respectively are used. These stages are controlled by an XPS Universal High-Performance Motion Controller/Driver, provided by Newport, These high precision motorized stages enable samples to be rotated in θ and ϕ as well as moved in the X, Y and Z directions (Figure 3.7).

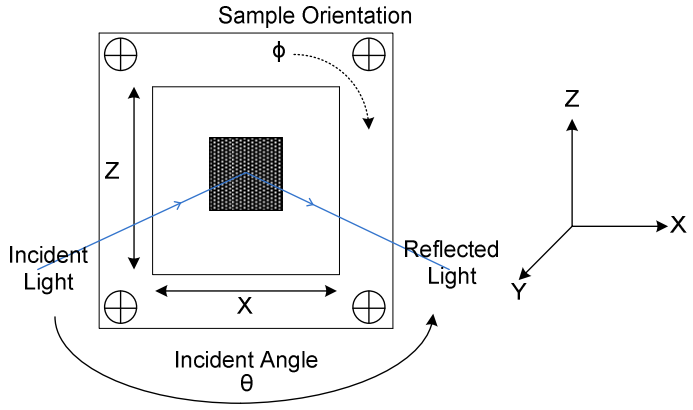


Figure 3.7. Sample stage XYZ and definition of Incident Angle and sample orientation [72].

The polarised white-light laser then illuminates samples mounted on the stage, and the reflected laser light is collected via mini integrating sphere and into an optical fibre probe attached to the collector arm in order to ensure that the reflected light enters directly into the optical fibre and into spectrometer. The spectrometer BTC112E (BWTEK Inc., USA) is used which can measure from 350 nm to 1050 nm wavelength with resolutions of 0.2 nm to 4 nm[73]. The spectrometer is connected to a computer and is controlled by LabVIEW software which also records and selects all measurement parameters such as start and stop incident angles, step size, integration times, start and stop stage rotation angle and XYZ positions. The measured spectral data is then saved

to a specified folder path. Once completed, a signal from the spectrometer is fed back to the motion controller so that the next scan step can continue, this minimizes acquisition delays and speeds up scans. These cycles occur continuously until the stop incidence angle is reached. The main feature of this program is that spectra can be continuously monitored whilst moving the collector arm across the full incident angle range. By monitoring in real-time, the spectral characteristics can be optimized. To align the system, a standard polished Si wafer is measured for P and S polarisation, where, with reference to the measurement plane, p-polarisation represents vertical oscillation of the incident electric field and s-polarisation is horizontal oscillation of the electric field).

Figure 3.8 shows the Specular reflectance for three different wavelength and compared with theory, for both P and S polarisation.

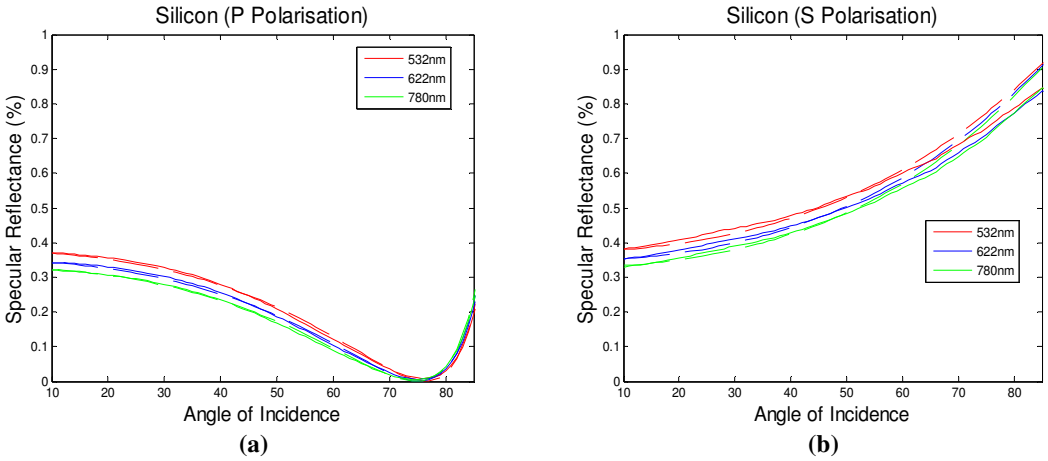


Figure 3.8. Specular reflectance at 532, 622 and 780 nm, the dotted line represents measurement and the solid line represents theory (a) *P*-polarisation and (b) *S*-polarisation.

The reflectance from silicon for *P* and *S* polarisations across the 450-1000 nm wavelength range and the angle range of 10-85˚are shown in Figure 3.9. The theoretical values are calculated from the Fresnel equation (2.1).

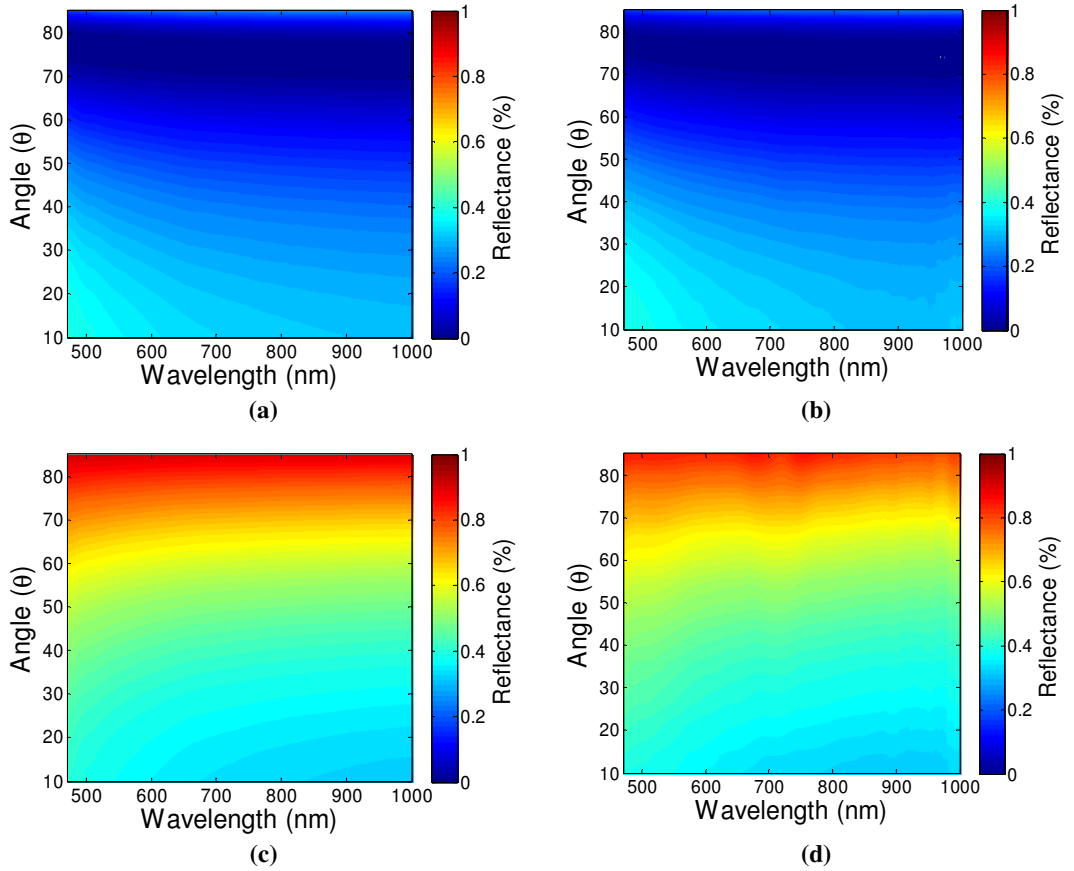
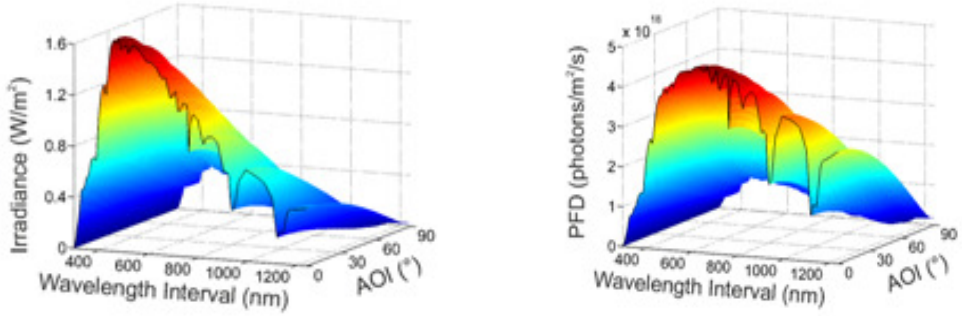


Figure 3.9. Reflectance of silicon , (a) P polarisation-experimental (b) P polarisation-theoretical (c), S polarisation-experimental (d), S polarisation-theoretical.

3.2.4. **Weighted reflectance**

The weighted reflectance value provides an indication of how well an anti-reflective structure would perform over the course of a day, if used on a fixed position solar cell. The irradiance value is evaluated for the angle of incidence (AOI) from 0° to 90°, based on the Photon Flux Density (PFD) solar spectrum data, as illustrated in Figure 3.10. Values are obtained from the *SPCTRAL2* model provided by the National Renewable Energy Laboratory (NREL)[74], which allows the input of parameters including date, time and angle. In this example spectra from times 06:08 to 12:08 at the equator on the vernal equinox are calculated, which provides irradiance data for AOI from 0-90˚. Further details can be found in previous publications[46].



(a) **(b)**

Figure 3.10. From solar spectrum, (a) Irradiance and (b), Photon flux density [46].

The weighted reflectance (R_w) is calculated using equation (3.2), where *PFD* is the AM 1.5 solar spectrum in the form of photon flux density, in units of photons $m^{-2}s^{-1}$. $R(\lambda)$ is the measured hemispherical reflectance of the sample.

$$R_W = \frac{\sum R[(\lambda) \times PFD(\lambda)]}{\sum (PFD(\lambda))} \qquad (3.2)$$

Angular resolved specular reflectance spectra were collected using the angular reflectance spectroscopy (ARS) system. Collecting data over a wavelength range of 450–1000 nm and an angle of incidence range of 5-83° enables a figure of merit termed the weighted specular reflectance (*WSR*) to be calculated from equation (3.3).

$$R_W(\theta) = \frac{\sum_\lambda [R(\lambda,\theta) \times PFD(\lambda,\theta)]}{\sum_\lambda [PFD(\lambda,\theta)]} \quad \textbf{(3.3)}$$

Where $R(\lambda,\theta)$ is the average of the s and p polarisation specular reflectance values of a sample measured using the reflectometer system. The WSR is then calculated by averaging over all angles of incidence to give a single percentage figure of merit.

3.3. Simulation

Modelling the operation of photonic structures is an important stage in the design process. Much can be learnt and understood about optical systems by using analytical calculations; Fresnel equations can be used for straightforward interfaces, transfer matrix methods can be used for multiples of interfaces [75, 76], and ray-tracing methodologies can be used for micron-scale textures [77]. However, it is difficult if not impossible to use wholly analytical techniques to accurately predict the operation of complex or nanostructured systems [46]. In the case of nanostructured designs it is certainly necessary to use more complex modelling methods, in this work we have used the semi-analytical technique of *Rigorous Coupled-Wave Analysis* (RCWA) and the computational method known as *Finite Difference Time Domain* (FDTD) modelling. RCWA is performed using GD-Calc [78] and FDTD using Lumerical [18].

3.3.1. Rigorous Coupled Wave Analysis

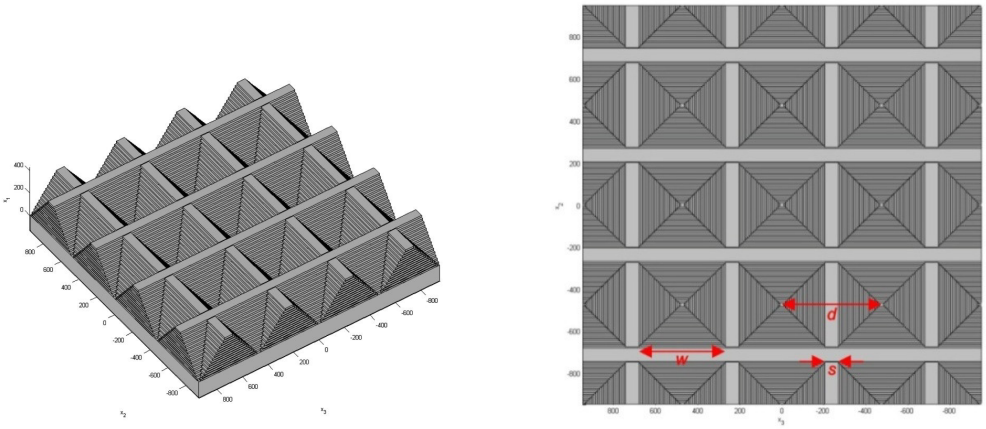
Rigorous Coupled Wave Analysis (RCWA) is a semi-analytical technique based on Floquet's Theorem [79] that can be used to solve scattering for periodic structures. It is essentially a Fourier-space technique in which fields are represented as the sum of spatial harmonics. Structures are represented in layers, with staircase approximations used to represent curves and solutions are found by matching boundary conditions at each interface between layers.

3.3.2. **GD-Calc**

Simulations were performed using the software package GD-Calc on models of sub-micron inverted pyramid arrays in silicon. These simulations will support an experimental investigation into the optical properties of structures fabricated in silicon using electron beam lithography and KOH wet etching.

The inverted pyramid structure is defined in GD-Calc using a "staircase" approximation, with a series of blocks arranged in layers or strata on top of a semi-infinite substrate. A 3D rendering of the structure is shown in Figure 3.11. The base width of the pyramids, *w*, and the period of the array, *d1*, can be specified. This fixes the size of the flat areas between the pyramids, *s*. The angle of the pyramid facet is fixed at 54.7° which is the angle between the <111> and <100> planes of the silicon lattice. This also fixes the pyramid depth, h, at (equation (3.4).

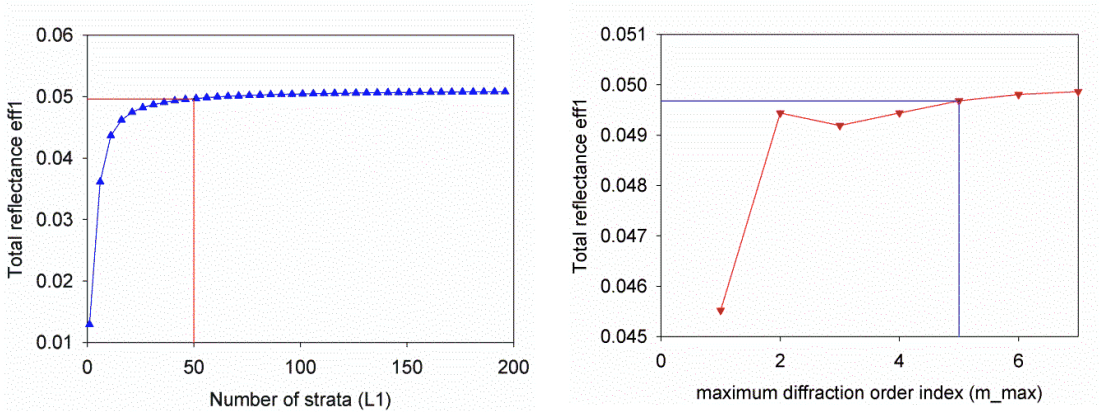
$$\mathrm{h} = \frac{1}{2} w \tan\left(54.7^{\circ}\right) = \left(\frac{w}{\sqrt{2}}\right) \qquad \textbf{(3.4)}$$



(a) **(b)**

Figure 3.11. (a) Three dimensional rendering of inverted pyramid structures defined in GD-Calc, with 15 strata; (b) top down view of the pyramids, defined with 30 strata, showing the base width, w, spacing, s, and period, d of the array.

Convergence tests were carried out for 500 nm wavelength on the number of strata, (L1) and the diffraction order truncation limit, (m_max). The results are shown in Figure 3.12, where the values of L1 = 50 and m_max = 5 are identified as parameters for which sufficient convergence is achieved. These parameters are used for the reflectance spectra simulations described throughout this work.



(a) **(b)**

Figure 3.12. (a) Convergence test for the number of strata, L1, with m_max=5; (b) convergence test for the diffraction order truncation limit, m_max, with L1 = 50.

3.3.3. **Finite Difference Time Domain**

Finite-difference time-domain (FDTD) [80] is a method of numerical analysis that has been used to study material and periodic structures over many years. The method is in the general class of *grid-based differential numerical modelling* methods. FDTD was first established by Yee in 1966 [81] as 3D solution to the time-dependent Maxwell's equations. Yee's algorithm locates electric field (E) and magnetic field (H), components at the centre of a grid with each electric field (E) line having four magnetic field components (Figure 3.13).

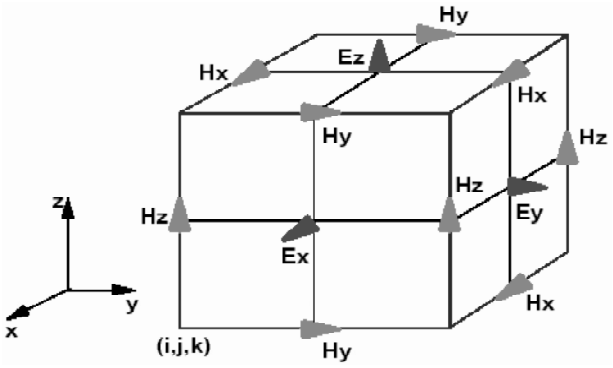


Figure 3.13. Illustration of Yee's spatial grid [82].

This way the discretised time-dependent Maxwell equations results in finite-difference equations that can be solved for a given instant in time. Software, typically solves electric field and then magnetic field components for each discrete volume in the mesh, then leapfrogs to the adjacent volumes while applying appropriate boundary conditions. The algorithm repeats this process many times until a steady-state convergent and contiguous solution is found. As with RCWA curved structures have to be rendered by staircase approximations and this represents a compromise in accuracy. FDTD is a very powerful technique, for modelling of complex periodic structures but can be very time consuming for disordered structures. A particularly powerful part of FDTD is the techniques ability to provide 3D maps of field intensity within a structure and this in turn provides valuable insight into photonic mechanisms.

3.3.4. **Lumerical FDTD Solutions**

The simulation program FDTD solutions by Lumerical solutions Inc., can be used to accurately simulate sub-wavelength photonic and optical devices and can be used in many applications such as integrated optics, nanoparticles scattering, plasmonics, solar cells and many more. Lumerical allows design and optimisation in 2D and 3D TCAD context and add sources and monitors to simulation. It has the ability to run parallel simulations in any available computer resource to obtain normalized transmission or reflection simulations, diffracted order from gratings and other periodic structures and many other features, the results can be readily analysed. Lumerical can run parameter sweeps. and has a conformal mesh FDTD simulator which makes simulation runs faster and allows more accurate results than a stair case mesh.

In the design each material is allocated a different colour (Figure 3.15). The FDTD object is the simulation region. The boundary conditions for an object can make simulations simpler by selecting periodic or symmetrical boundaries. For the majority of simulations used in this study, periodic boundaries have been used for the vertical sides of the simulation region, and Perfectly Matched Layer (PML) boundaries for the horizontal sides of the simulation region.

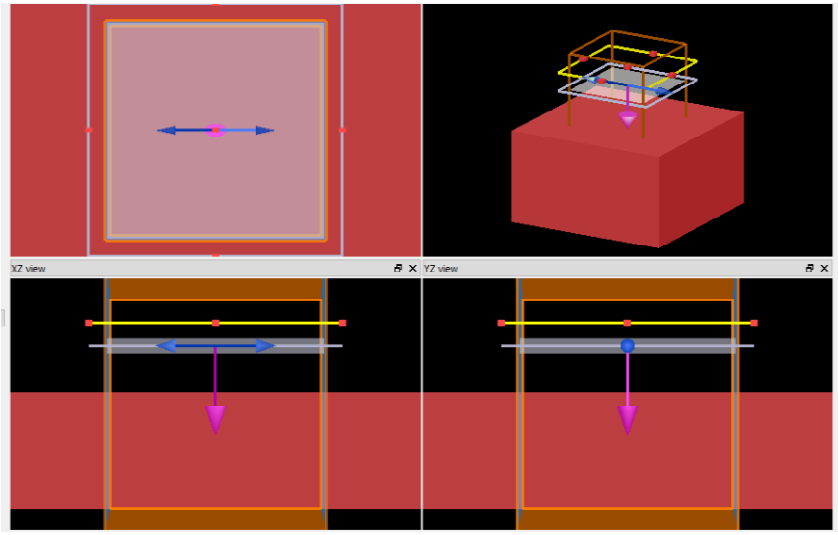


Figure 3.14. Lumerical FTDT solution Window.

The source object simulates the incident light, for all of the simulations in this study, a plane wave source with wavelengths in the range 440-1100 nm was used in order to simulate a solar source. Monitors collect data and are represented in the Lumerical display by yellow boxes or lines. Two different types of monitor have been used in these simulations; movie monitors create an animation of the simulation.. Frequency-domain power monitors measure several properties, including transmission T and electric field E.

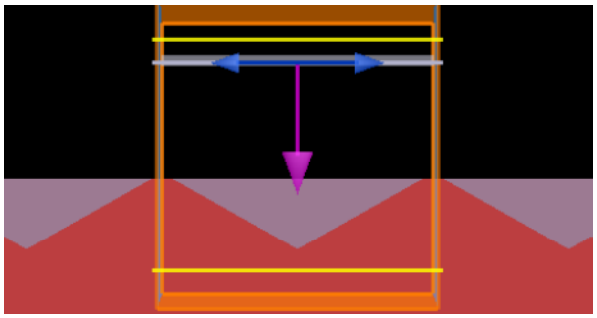


Figure 3.15. Material is allocated a different colour for typical Inverted Pyramid Structure.

Example results of the top length optimisation of inverted pyramid arrays, can be seen in Figure 3.16, which show the reflection, transmission and absorption as a percentage of incident light, respectively.

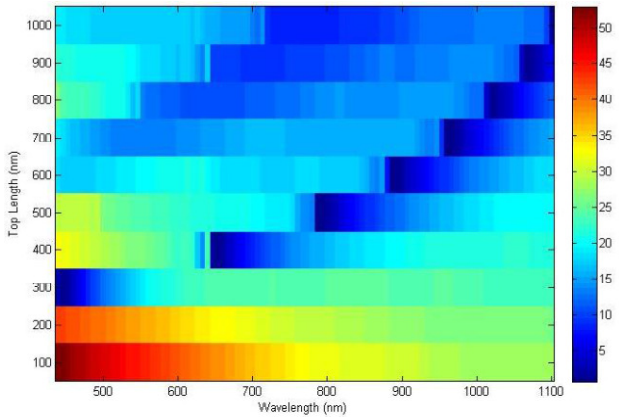


Figure 3.16. Simulation of Top Length Optimisation.

In this work RCWA (GD-calc) has been used to model inverted pyramid arrays, however, RCWA was found unsuitable for modelling the Mie Resonator structures. For both inverted pyramid and Mie Resonator structures we have worked with Dr David Payne (a Post-Doctoral member of Prof. Bagnall's group at Southampton University, and now UNSW) in order to develop FDTD simulations in a timely manner and thereby allow some additional analysis in this work.

4.Submicron Pyramidal AR Structures

4.1. Introduction

Random micron-scale inverse pyramid texturing with a single layer coating is the most common antireflection (AR) scheme used in commercial C-Si photovoltaics in particular the formation of the inverted pyramid structure is the first step in the fabrication of the high-efficiency '*PERC*-like' solar cells that are beginning to dominate C-Si production [83]. The inverted pyramid scheme is a very effective AR scheme with less than 1% reflection for much of the useful spectral range. Relying on the natural faceting of silicon revealed by a KOH etch it is a relatively inexpensive and quick scheme that allows production at an industrial scale.

The PERL cell which held the record for single junction silicon cell efficiency for many years (section 2.5), developed by Green *et al*, at UNSW [84] took AR performance a step further by using lithographic stages to produce regular arrays of carefully optimised inverted pyramids and double layer coatings. This PERL methodology is a much more expensive process that does not confer sufficient efficiency savings to justify the additional expense of production for mainstream commercial cells and so is not likely to be adopted in the near future, if ever. Both the random inverted pyramids and the ordered inverted arrays have features typically of the order 10 microns, so neither scheme is suitable for very thin devices. Multi-crystalline wafer technologies, currently around half of wafer silicon cell production cannot utilise KOH etch because of the random orientation of facets, so in the case of mC-Si alternative texturing methods are used [85].

To date, there has been relatively little work carried out on the fabrication or characterisation of ordered arrays of sub-micron scale inverted pyramids. The work in this chapter details the manufacture, characterisation and modelling of ordered arrays of sub-micron inverted pyramids.

Whereas the optical behaviour of standard inverted pyramid textures can be understood and modelled by simple ray-tracing techniques it is clear that submicron inverted pyramids arrayed with wavelength-scale periodicities are going to behave very

differently. Firstly, we can expect sub-wavelength aspects of the designs, that cannot be resolved by the incident wavelengths, to provide an effective graded refractive index in a manner similar to the moth-eye scheme. Secondly, we can hope that the periodic features could produce diffractive effects that will provide an opportunity for light-trapping. When compared with moth-eye surfaces it is clear that the regular faceting and self-limiting nature of inverted pyramids might offer more reproducibility, however, the effectiveness of the moth-eye scheme is very dependent on profile of the nanoscale features [55], so it is likely that there exists fewer options for optimization in the case of the nanoscale inverted pyramids. As with moth-eyes it is likely that sub-micron inverted pyramid arrays cannot be simply understood by diffraction modelling or graded refractive index and in fact, robust RCWA or FDTD modelling is likely to be required in order to understand the system.

4.2. Background Literature

In the literature, Sun *et al*, [86] were amongst the first to report [87-89] experimental results on the fabrication of sub-wavelength Inverted Pyramids (IP) , using silica particles of different sizes to create a shadow mask (Figure 4.1).

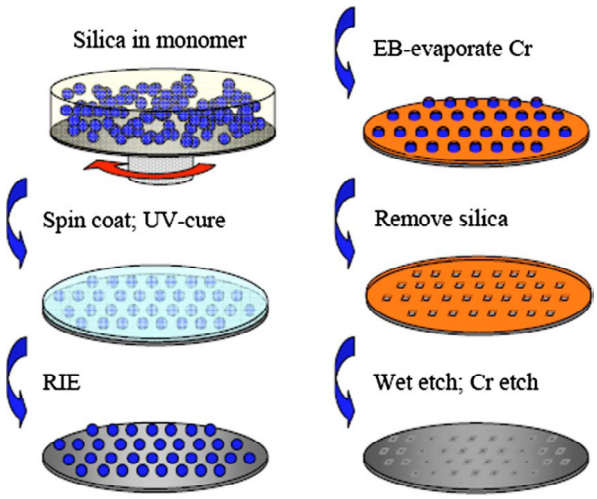


Figure 4.1. Process step for submicron inverted pyramid arrays using shadow mask by spinning nano silica[86].

Silica spheres, 320 nm in diameter, were chosen as templates using spin coating and UV-curing, this was followed by RIE to remove the monomer. Then Cr is deposited to

form a hard mask and in the final step, the wet etch using KOH solution at 60°C for 90s and 120s was carried out. This process achieved the formation of IP arrays with sizes of 300 nm and 360 nm (etch times of 90 s and 120 s, respectively) which are shown in Figure 4.2.

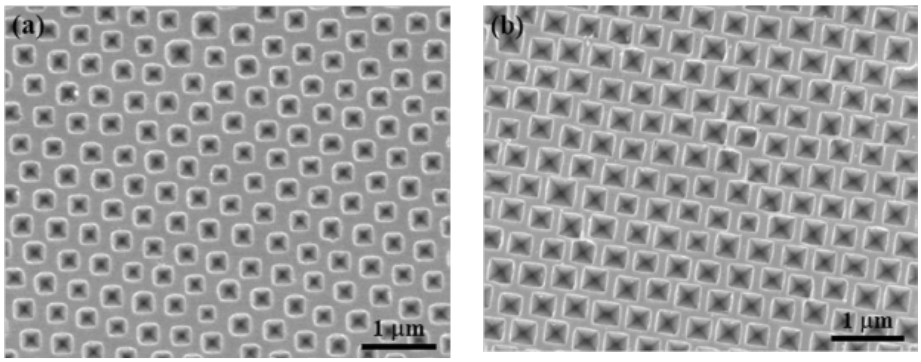


Figure 4.2. SEM Image of inverted nanoscale pyramid arrays, (a) 300 nm and (b) 360 nm [86].

The optical results of Sun *et al*, (Figure 4.3), show how the texture produced by the 120s etch reduces the reflectance significantly when compared to bare Si, both in simulation and experiments. While these reductions are encouraging for textures that still contain considerable flat regions, the 10% reflectance at wavelengths of 600 nm and greater is not particularly remarkable. It is clear already in the results of Sun *et al* that it is often a challenge to match simulated and actual results, particularly when, in this case the features are of a similar size as the wavelength. In this case the mismatch between experimental results and the RCWA simulations at 400 nm is attributed to assumptions made about the 'effective refractive index' of the structures.

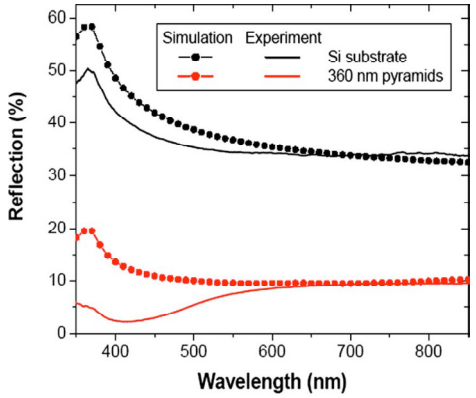


Figure 4.3. Experimental (solid) and RCWA-modelled (dotted)specular optical reflectivity at normal incidence. Black: bare (100) silicon wafer. Red: 360 nm size pyramids templated from 320 nm silica spheres [86].

Sun *et al,* reported that with decreasing pyramid size in their experiments, the reflection was increased (Figure 4.4). As with moth-eye structures, it is clear that as wavelength-scale feature size is reduced the effective thickness of the AR region is reduced, this will inevitably reduce the effectiveness of the AR unless alternative diffractive or scattering mechanisms come into play.

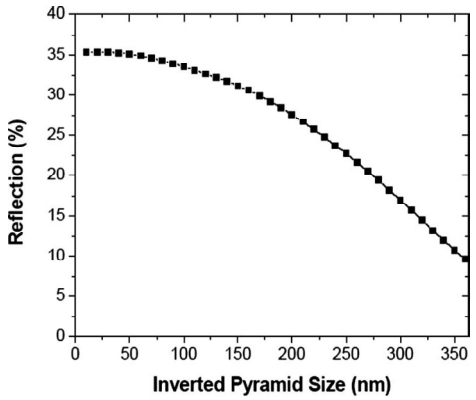


Figure 4.4. RCWA-simulated normal-incidence optical reflection at λ=600 nm vs inverted pyramid size. The 320 nm silica spheres are used as templates [86].

In very recent work Senthuran *et al* [90] have fabricated inverted nanopyramid arrays without a mask by utilizing interference lithography and a subsequent dry and then KOH etches. Figure 4.5 compares the reflectance of bare Si with surfaces textured with inverted pyramid arrays of two different sizes, with and without the additional dual ARCs. The total reflection at normal incidence for 700 nm pyramids was below 10% over the entire visible range and enhanced further with the addition of a standard dual ARC (MgF_2/ZnS) on top of the structure.

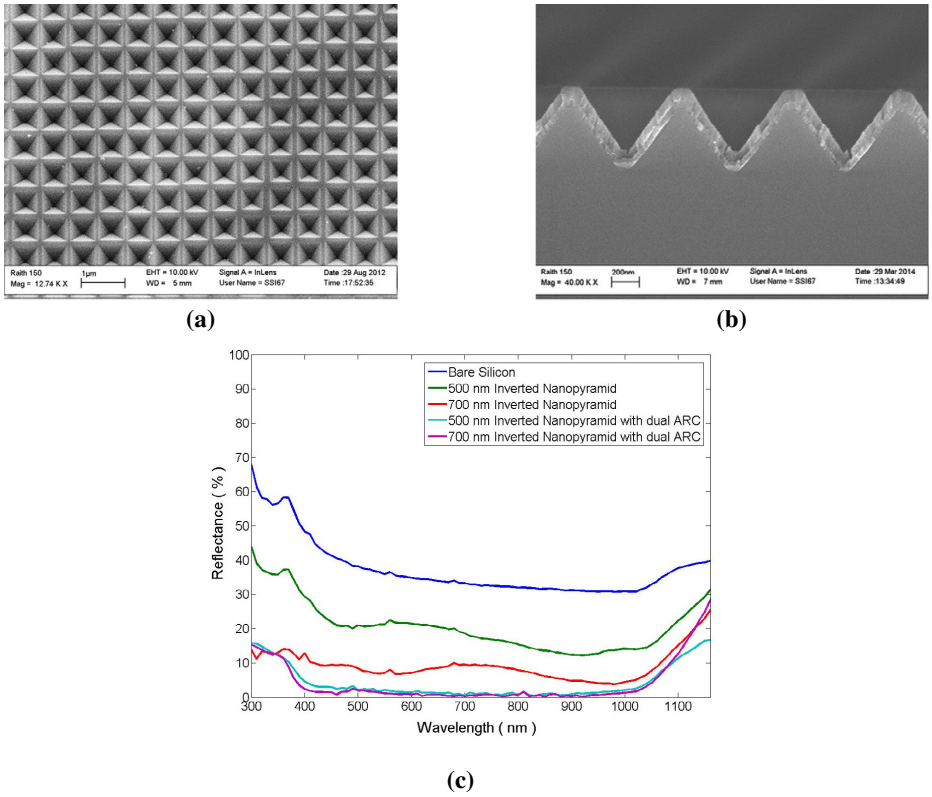


Figure 4.5. SEM images of (a) 700 nm inverted nanopyramids (b) cross sectional view of inverted nanopyramids with conformal dual ARC (c) Comparison of reflectance between bare Si, Si surface textured with inverted nano-pyramid arrays and Si surface textured with inverted nanopyramid arrays with dual ARC [90].

These two examples from the literature demonstrate that sub-micron scale inverted pyramid arrays can confer a broadband AR effect and so could be useful in enhancing the performance of silicon solar cells. To fully realize the potential of this AR scheme, the feature size and periodicity should be optimized for broadband performance across the whole solar spectrum.

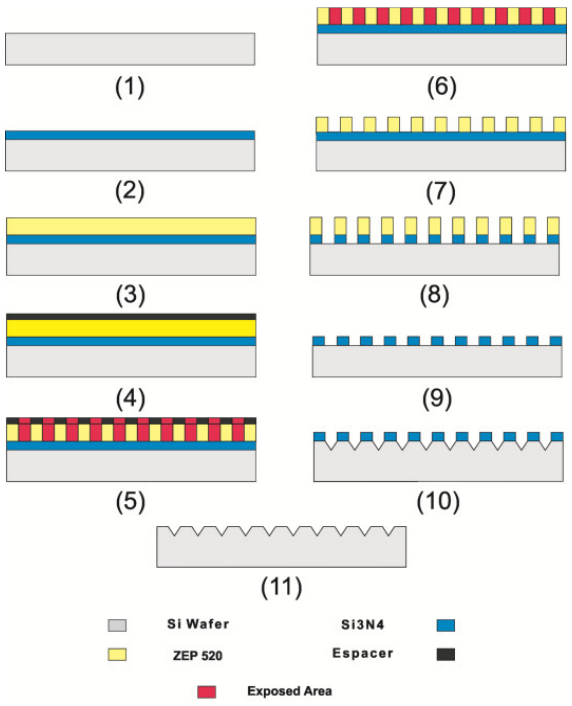
4.3. Fabrication of Inverted Pyramids

I have developed electron beam lithography and wet etch processes to fabricate inverted pyramid (IP) arrays in silicon with a high degree of control over the size and uniformity of array features. I use measurements from these samples to explore how the antireflective properties of the IP arrays vary with period. I also use the experimental

results to validate an implementation of the rigorous coupled wave analysis simulation technique and then show how this can be used to further explore variations in feature size and shape with a view to optimizing the structure.

The initial aim of this work was to produce regular square arrays of submicron inverted pyramids with pyramid base widths in the range 200 nm to 500 nm, in step sizes of 100 nm. In this section, each process step is described along with issues experienced during development of the fabrication processes. The final successful fabrication process is finally detailed.

The process for fabrication of IP arrays on silicon is presented in Figure 4.6. This process was established after discussion with a number of experienced researchers and technical staff working in the Southampton Nanofabrication Centre. Some experience gained on the fabrication of inverted nanopyramids by Dr Hitoshi Sai during a summer research secondment in Southampton in 2012 was particularly valuable (unpublished). The following sections provide details on each of these steps in turn.



1. Clean 150 mm standard p type Si wafer
1. Deposit 150 nm Si_3N_4 on Si wafer
2. Spin ~400 nm of Az250A resist
3. Spin Espacer resist
4. E-beam exposure
5. Remove Espacer
6. Develop resist
7. Remove exposed Si_3N_4
8. Remove resist
9. Wet etch with KOH
10. RCA clean
11. Remove Si_3N_4

Figure 4.6. Process steps for the fabrication of submicron inverted pyramids arrays on silicon.

4.3.1. **Substrate selection and wafer cleaning**

The starting material was a standard single side polished, 6 inch p-type silicon substrate with 600 µm thickness and (100) orientation. Before the start of any processing the silicon wafers were cleaned using Radio Corporation of America (RCA) clean, RCA1 (for 5 min at 40 °C) solution to remove any organic contaminants, following that, RCA2 (5 min at 40 °C) was used to remove any ionic contamination[91, 92], then to remove any oxide layer, a Hydrofluoric (HF) 7:1 solution was used [93]. Cleaning was completed by rinsing and drying the Si wafers.

4.3.2. **Silicon nitride mask formation**

Initially, *Low-Pressure Chemical Vapor Deposition (LPCVD)* furnace (TS6603, Tempress Systems) was used to form the Si_3N_4 layer on the Si wafer, however at the KOH etching stage, the layer of Si_3N_4 would peel off after a short period of time (Figure 4.7). In an attempt to resolve this issue the thickness of Si_3N_4 was increased, however this did not to solve the problem. The common issue of peel off using this process is due to the mismatching of the lattices of Si_3N_4 with Si, leading to residual stress in the thin film and resulting in delimitation [94].

The next action was to thermally grow 5-10 nm of SiO_2 as an intermediate adhesion layer to hopefully improve adhesion between the Si and Si_3N_4 however the nitride mask was still found to delaminate during the KOH etch.

As described in section 3.1.1 plasma assisted reactive magnetron sputtering system deposition was available as an alternative Si_3N_4 formation technique. This deposition was known to produce dense and smooth thin films and so a trial was conducted to determine whether the Helios system could be used to deposit an adherent nitride film capable of withstanding the KOH etch process without delaminating.

Si_3N_4 was deposited using the standard recipe on the Leybold Helios sputtering tool (section 3.1.1.1) to a thickness of 150 nm on both sides of the wafer. Deposition on both sides of the wafer was necessary to protect the rear of the silicon wafer from KOH etching. An exposed rear surface would deplete the KOH solution of hydroxide ions,

and adversely affect the etch rate and reproducibility on the front side. Our first and all subsequent experiments showed the magnetron sputtering to provide Si_3N_4 suitable to act as a hard mask during KOH etching with no delamination.

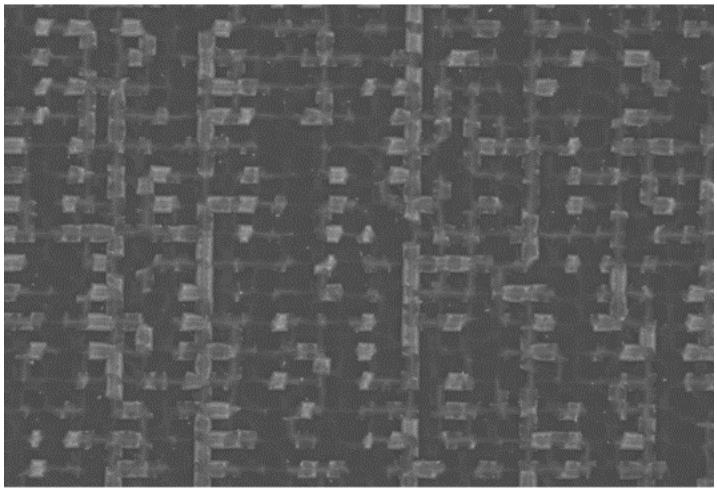


Figure 4.7. SEM of the surface of an etched wafer showing that the furnace grown Si_3N_4 mask has delaminated during the KOH etch.

4.3.3. **Resist Spinning**

Electron beam lithography was used to define the sub-micron square array etch mask in the Si_3N_4. The e-beam responsive resist chosen was *ZEP520A (From ZEON Co.)* [95] as this is a positive resist with high resolution and resistance to dry etching that would allow the defined pattern to be transferred to the underlying Si_3N_4 layer. A standard recipe as outlined in Table 4-1 was used to spin *ZEP520A* resist layers onto the Si_3N_4 coated wafer which was then baked at 180°C for 180 seconds.

Table 4-1 Spin recipe details for Resist ZEP520A

	speed (rpm)	time (s)	acceleration (rpm)
Spin recipe details for ZEP520A	0-3370	0.1	2000
	3370	0.1	0
	3370	180	0
	3370-0	5	1200

A layer of conductive resist *E-Spacer 300Z* [96] was then spun onto the *ZEP520A* in order to avoid beam deflection and pattern distortion that can result from negative charge build up on the Si substrate surface during E- Beam lithography. Table 4-2 provides the spin recipe details for E-Spacer 300Z.

Table 4-2 Spin recipe details for E-spacer 300Z.

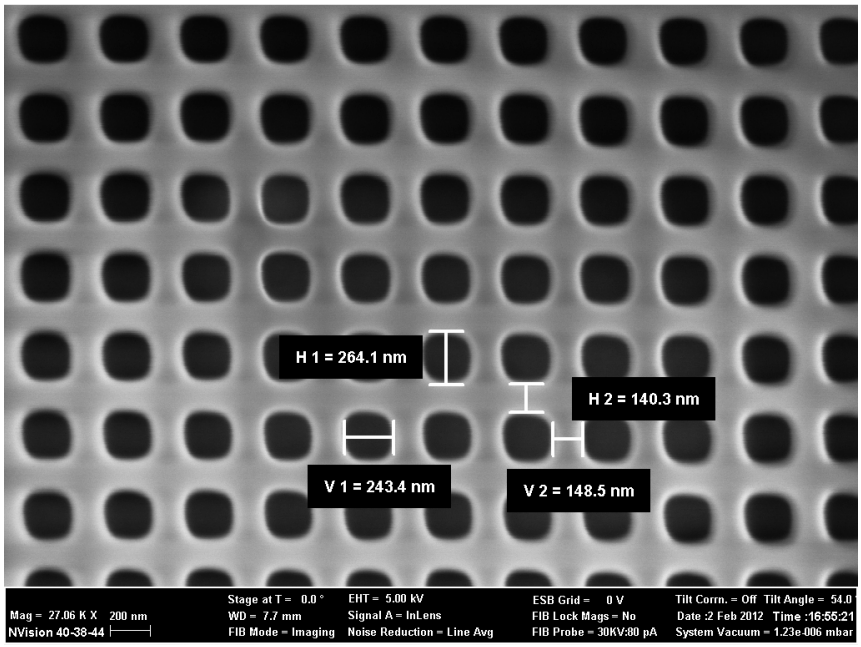
Spin recipe details for E-Spacer 300Z	speed (rpm)	time (s)	acceleration (rpm)
	0-2000	0.1	2000

4.3.4. **E-beam Exposure and Development**

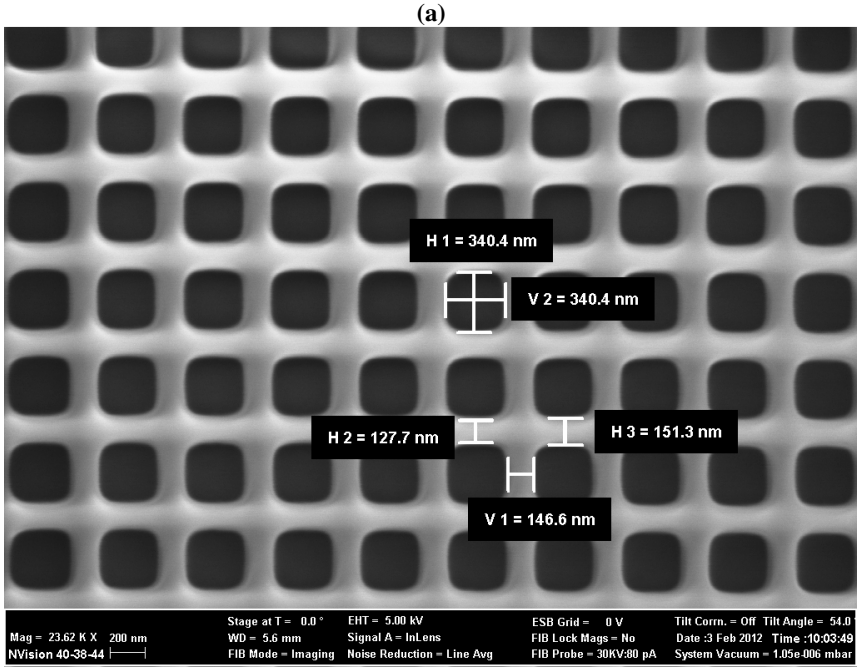
L-edit, which is a computer aided design (CAD) software program from Tanner EDA, has been used to generate arrays. Each array is 1cm by 1 cm, with a 0.5 cm gap between each array to allow for dicing and handling. The standard designs of square patterns with sides of 200, 300, 400 and 500 nm were drawn in L-Edit, then converted using software (Beamer from GenIsys GMBH) to a format which is compatible with the E-beam lithography tool. The standard base dose used for the pattern was 195 $\mu C/cm^2$.

After exposure E-Spacer *300Z* was removed by rinsing with DI water for 1 min with gentle pressure and then blow-drying using a nitrogen gun. Developer *ZED-N50 (From ZEON Co.)* [95] was used as the development solution for the *ZEP520A* after E-beam exposure. The sample was soaked in ZED-N50 for *90s* and then rinsed with Isopropyl alcohol (IPA) for *30s* to remove the resist from the exposed areas.

Scanning Electron Microscopy (SEM) images of patterns successfully formed in the resist are shown in Figure 4.8. As was expected the resist pattern shows significant curvature for such small designs. The pattern that is targeting the formation of squares with 200 nm sides, is close to actually producing circles with radi of 200 nm. This curvature in the resist pattern was largely expected to be preserved in the Si_3N_4 layer, however the KOH etch would expected to restore to a square pattern in the silicon.



(a)

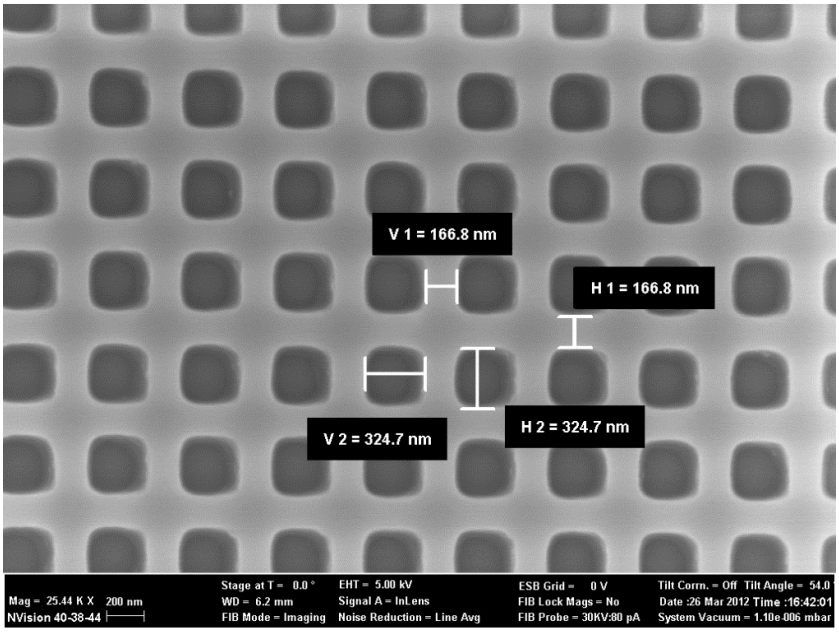


(b)

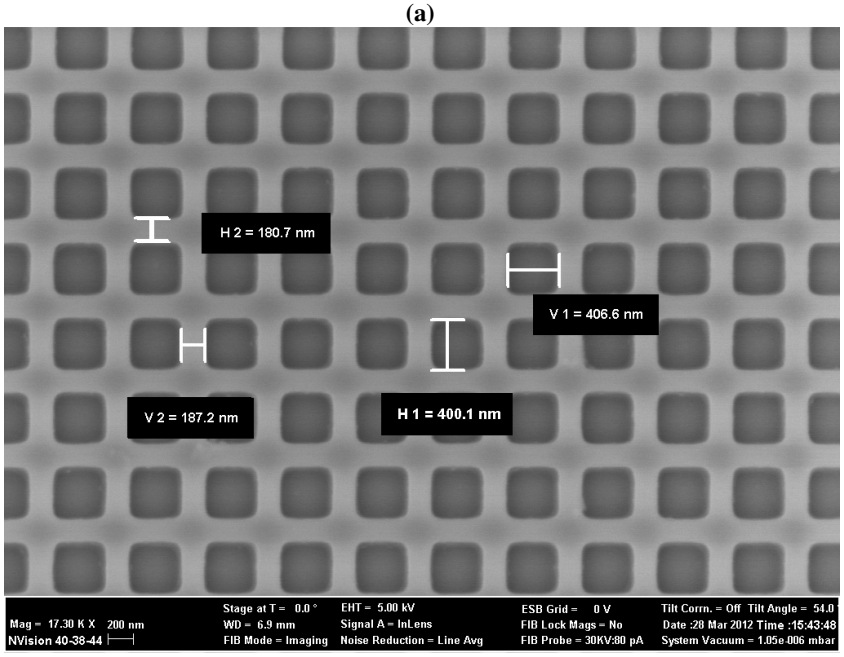
Figure 4.8. Top down SEM images of square array patterns in resist: (a) width designed as 200 nm, (b) width designed as 300 nm.

4.3.5. **Dry etch pattern transfer into Si_3N_4 mask**

Reactive Ion Etching (RIE) was used to transfer the pattern in the resist to the underlying Si_3N_4 layer. The standard recipe was employed with an etch time of 8 min (see section 3.1.4). SEM images of patterns successfully transferred into Si_3N_4 mask layer (before resist removal) are shown in Figure 4.9.



(a)



(b)

Figure 4.9. SEM images of patterns etched into the Si_3N_4 mask layer (before resist strip): (a) squares designed with 200 nm side (b) squares designed with 300 nm side.

4.3.6. **Removing Resist**

There are a few methods to remove *ZEP520A* resist: One such method is to use a solvent remover such as 1-Methyl-2-pyrrolidon (NMP) at 80°C for a couple of hours. A quicker method is to use an O_2-plasma *asher* for 5-10 min. For this work, the plasma asher technique was chosen. SEM images of patterns after resist removal are shown in Figure 4.10.

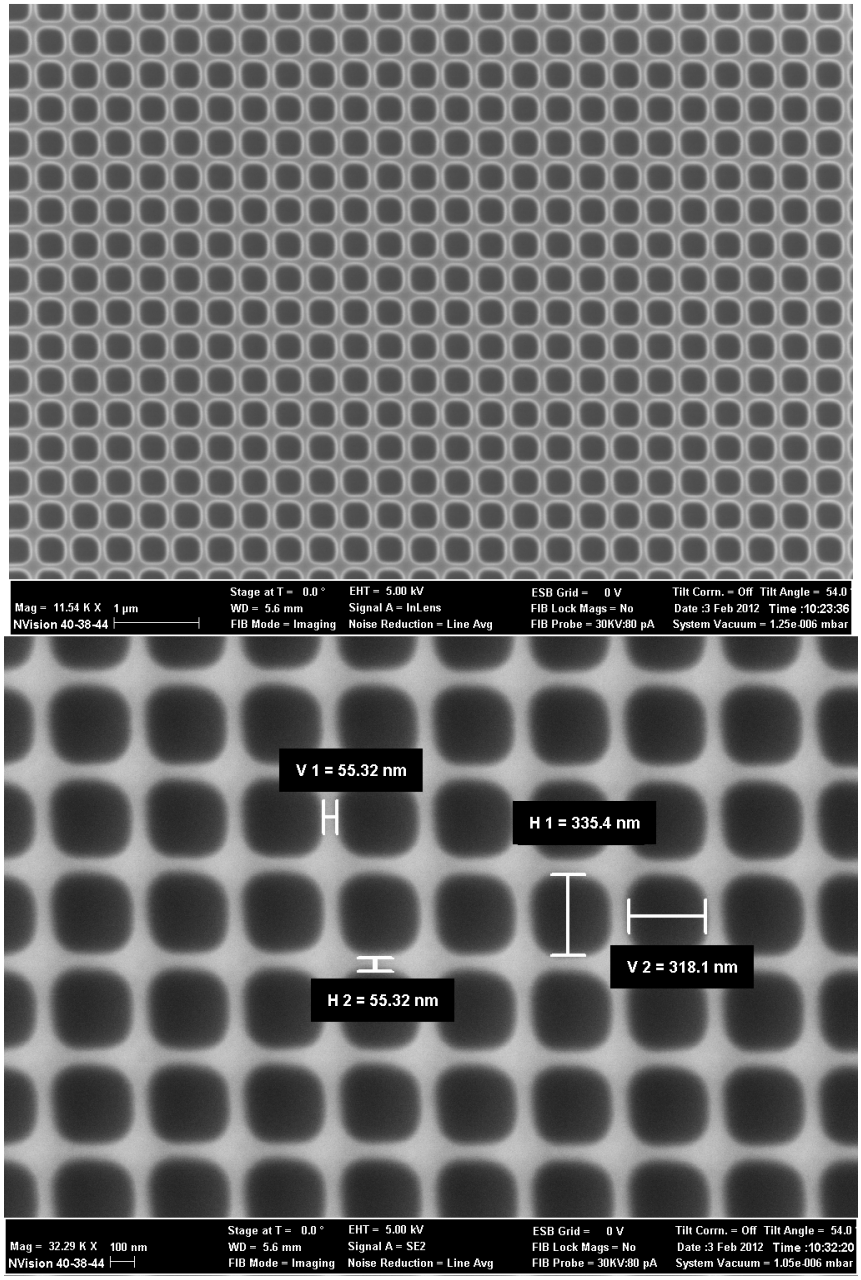


Figure 4.10. SEM images of samples with 200 nm width sample after resist removal.

4.3.7. **Wet etch using KOH solution**

Etching in KOH solution (see section 3.1.5) was used to form the ordered inverted nanopyramid arrays through the Si_3N_4 mask. Initially, the standard process at *70°C* was used but the etch rate was found to be very slow at this temperature. The SEM image in Figure 4.11 shows the resultant texture after etching for 1 hour at *70°C*. The image shows only a small amount of silicon etching was achieved in just a few windows.

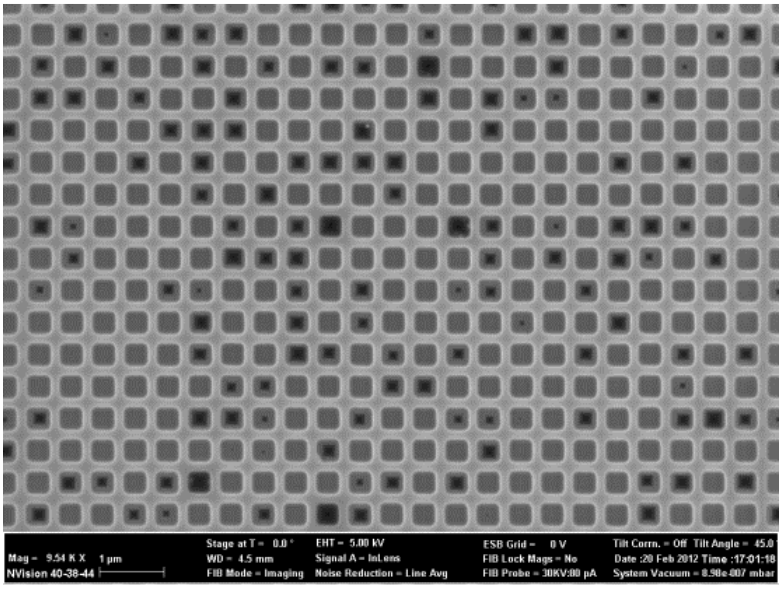


Figure 4.11. SEM image of etching for 1 hour at 70°C.

The KOH temperature was increased to 80°C and this was found to greatly enhance the etch rate. The etch time was then optimized by etching samples for 1, 2 and 3 minutes and then by imaging the resulting surfaces using SEM. The results for 1, 2 and 3 minute etching times are presented Figure 4.12, along with accompanying schematics illustrating the extent of the etching for each sample imaged. The sample etched for 3 minutes shows fully formed pyramids.

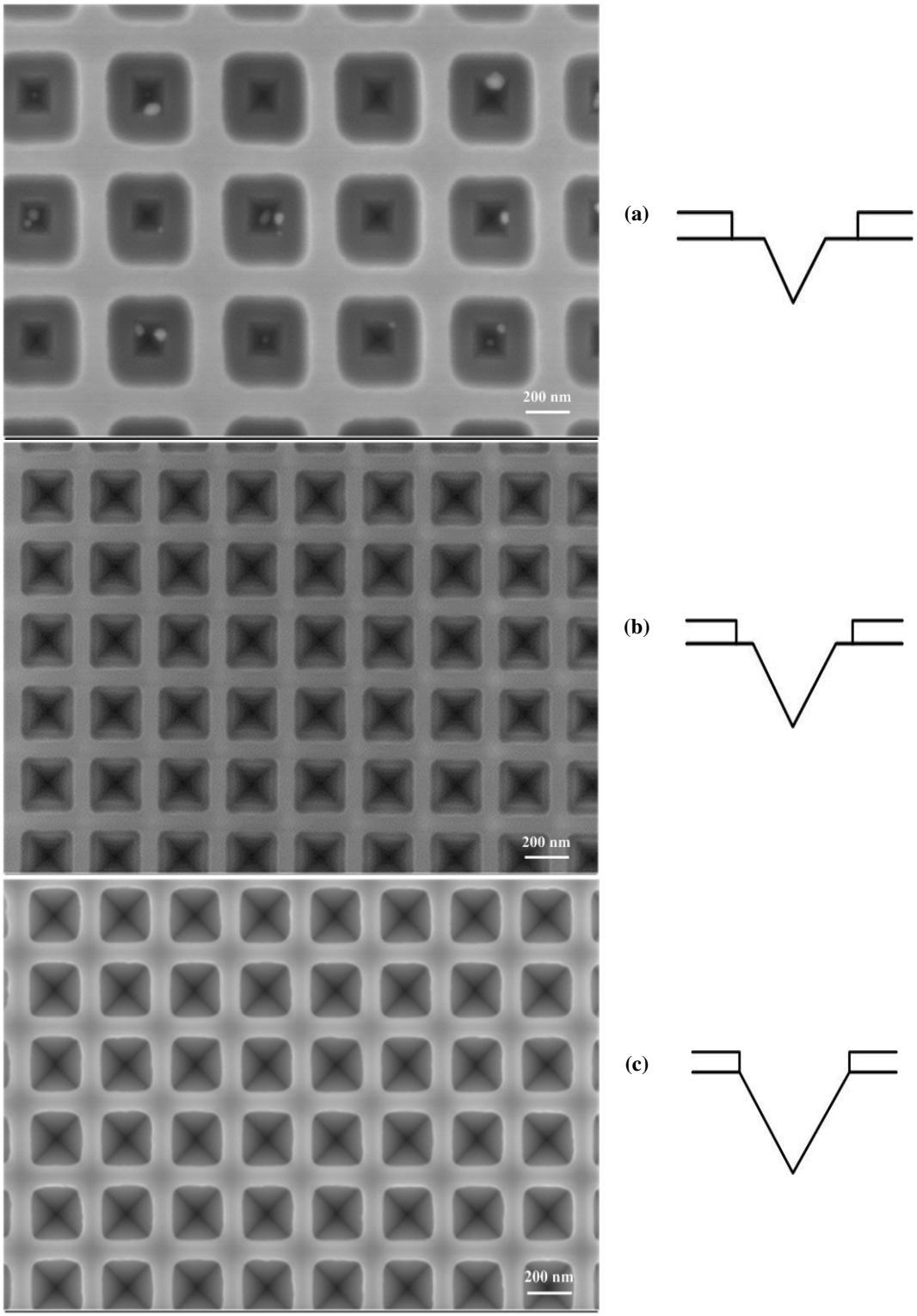


Figure 4.12. SEM images of samples etched in KOH at 80°C for (a) 1 min, (b) 2 min and (c) 3 min. Schematic diagrams illustrating the extend of the etching for each imaged sample are included. alongside each image.

Immediately after etching, some samples were observed to contain small particles inside the IPs (Figure 4.13). The samples were therefore cleaned again using a standard RCA clean to remove any possible metal or organic contamination.

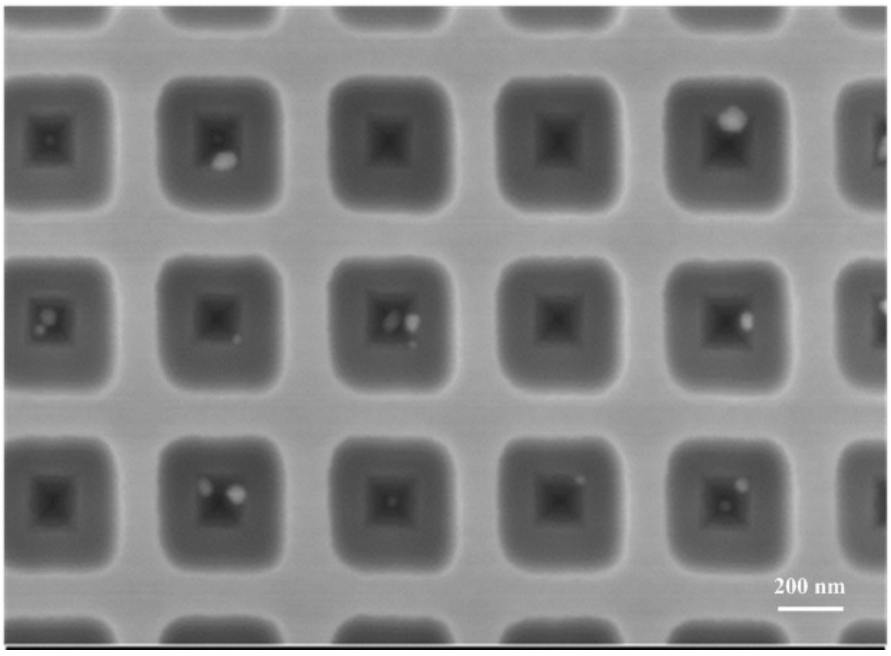
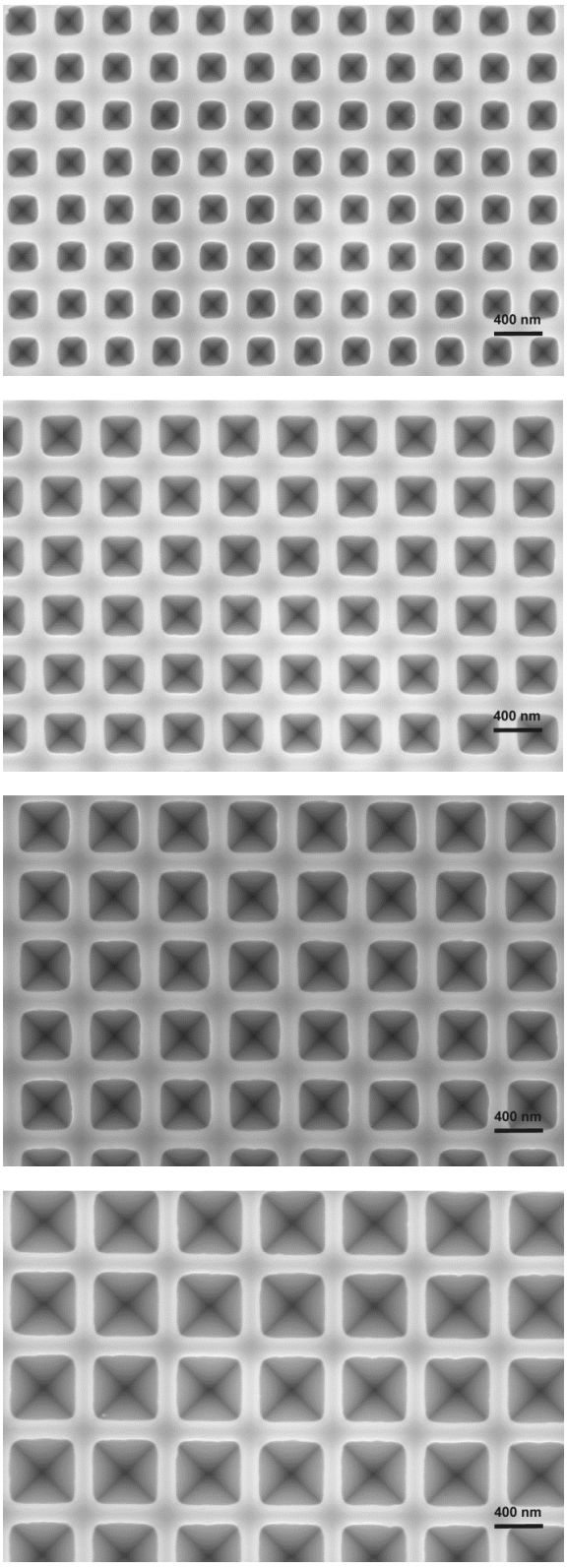


Figure 4.13. SEM image of invert pyramids arrays taken immediately after KOH etching showing possible iron contamination from KOH tank.

SEM images of fully formed patterns of IP arrays, etched using the optimized recipe and then RCA cleaned are shown in Figure 4.14 (top down images) and Figure 4.15 (sample tilted to *25°*).



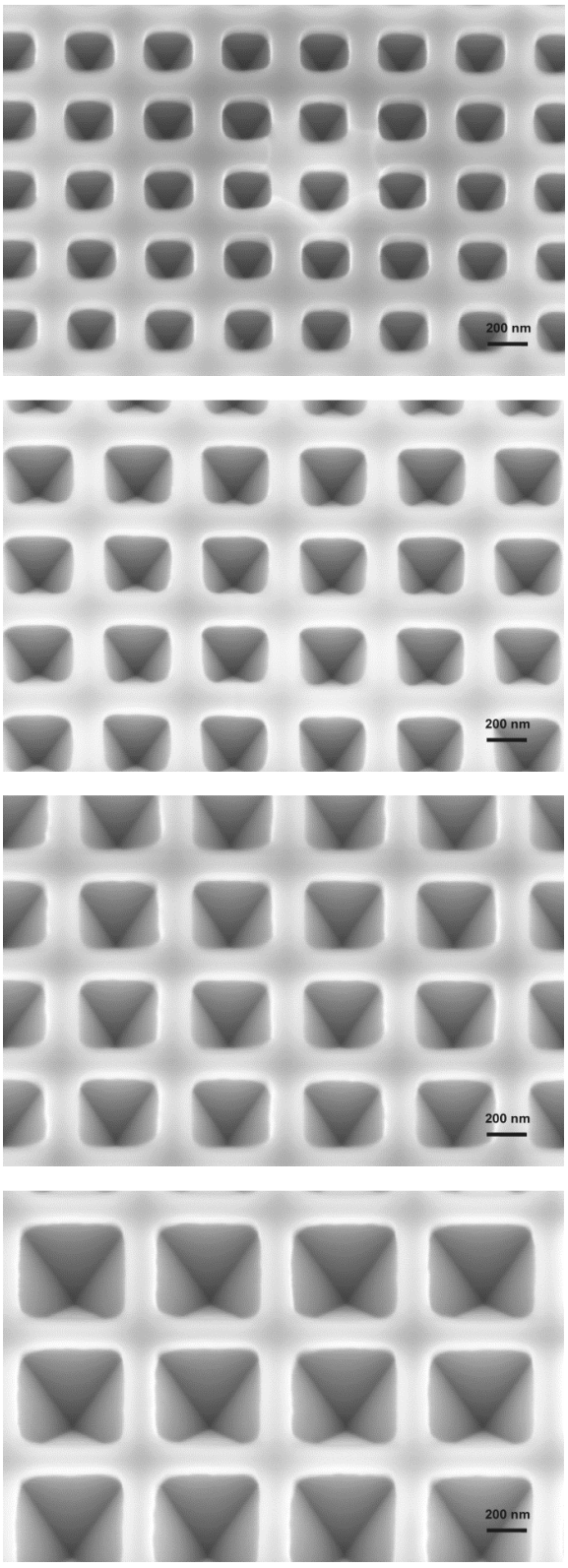
(a) 200 nm

(a) 300 nm

(a) 400 nm

(a) 500 nm

Figure 4.14. Top down SEM images of post KOH etched samples with 4 widths defined.



(a) 200 nm

(b) 300 nm

(c) 400 nm

(d) 500 nm

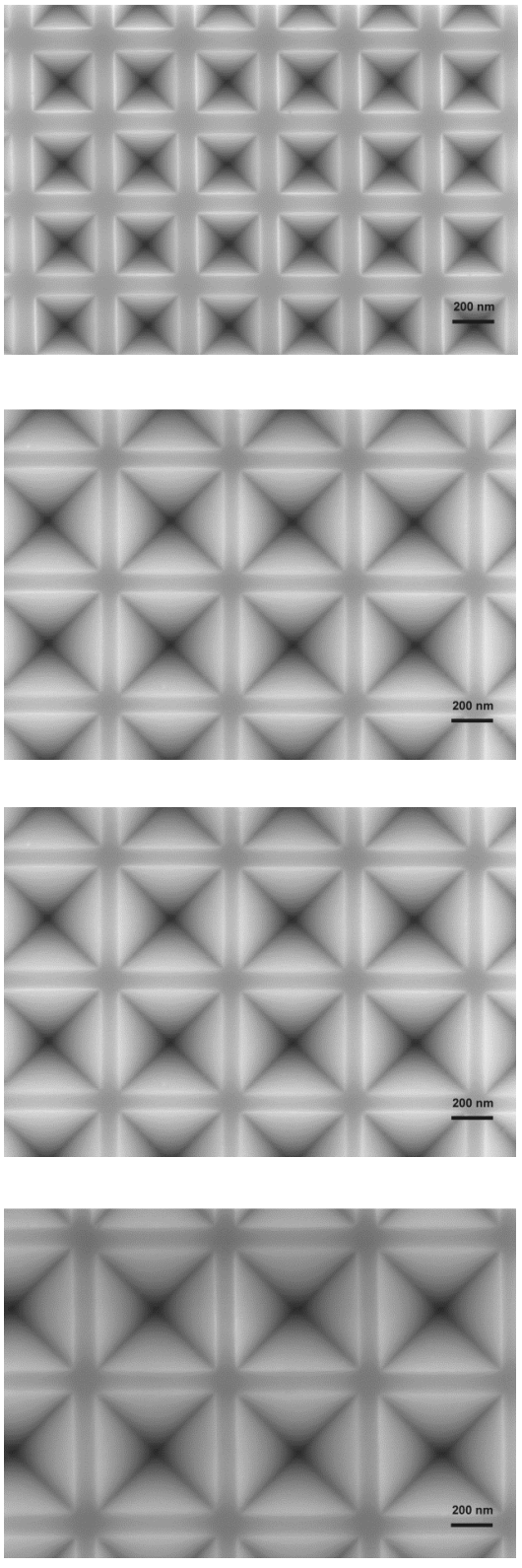
Figure 4.15. SEM images post-KOH etch with samples tilted to 25° and designed square sides defined.

The images in Figure 4.15 shows that only the <111> facets of the inverted pyramids are exposed and that those facets extend beyond the edges of the mask and that they taper down to a point. These results confirmed that 3 minutes was a sufficient time to expose just <111> facets for all of the structures in this range of designs, once only <111> facets are left the etch will continue but at approximately $1/100^{th}$ the rate as the <111> plane is slowly removed, undercutting the mask [97].

4.3.8. **Removal of Si_3N_4**

There were at least two techniques available for the removal of the Si_3N_4 hard mask, dry etching using the RIE tool, or wet etching using HF. In this work, the wet etch option was chosen to avoid any surface damage or increased surface roughness that may have resulted from a dry etch process. To remove the nitride layer from the textured samples, the samples were placed in HF (7:1) for 60 min. SEM images of fully formed patterns of IP arrays following removal of the Si_3N_4 mask are shown in Figure 4.16, SEM images of the samples taken at a tilt of 35°.

Measurements of the feature dimensions were carried out on the SEM images of the successfully fabricated samples. Table 4-3 presents measured values of base width (w), period (d) and flat spacer width (s) (see Figure 4.17 for an explanation of the terms dimensions) together with the square array dimensions from the E-beam mask design. The measurements reveal that the KOH etch undercuts the Si_3N_4 mask by 50-60 nm on each side, resulting in IPs with smaller flat spacer widths and larger base widths than the corresponding dimensions of the E-beam mask. This undercutting is to be expected in a wet-etch technique and could be exploited to further reduce the flat spacer width and perhaps improve the AR effect. This process of undercutting the mask could in principle continue to the point where the mask was completely undercut, and although this might be a desirable outcome for the final optical design, leaving no flat areas would also lead to mask delamination.



(a) 200 nm

(b) 300 nm

(c) 400 nm

(d) 500 nm

Figure 4.16. Top view SEM images of samples after the removal of Si_3N_4.

Table 4-3 Design and fabricated values of w, d and s.

Sample Name	Si Pyramid **Designed**			Si Pyramid **Fabricated**		
	w (nm)	s (nm)	d (nm)	w (nm)	s (nm)	d (nm)
Batch1-Si-S1	200	200	400	305 (+/-10)	94 (+/-10)	398 (+/-5)
Batch1-Si-S2	300	200	500	415 (+/-10)	74 (+/-10)	497 (+/-5)
Batch1-Si-S3	400	200	600	515 (+/-10)	78 (+/-10)	598 (+/-5)
Batch1-Si-S4	500	200	700	594 (+/-10)	96 (+/-10)	698 (+/-5)

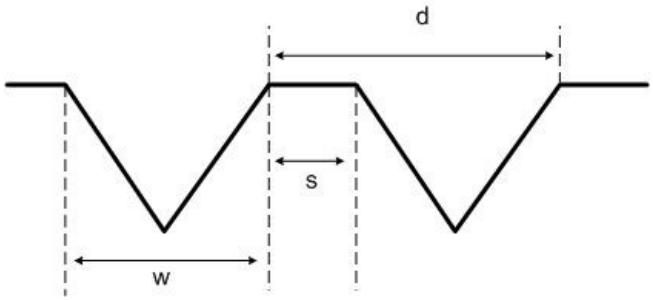


Figure 4.17. Diagram of IPs showing the base width (w), period (d) and flat spacer width, s, of the array.

4.4. Integrating sphere measurements

The integrating sphere (IS) technique was used (see section 3.2.2) to measure the total hemispherical reflectance from each of the samples using p polarization and an angle of incidence of 8°. The results are presented in Figure 4.18 and show that texturing a Si surface with IP arrays confers an AR effect. The nanostructured surfaces are significantly less reflective than bare silicon with the reflectivity typically in the 5% to 25% range from 400 nm to 1000 nm, the best sample is the one with the largest features has less than 15% reflectance in the wavelength range of 550nm to 870nm. The reflectance minimum is seen to be tunable, with the spectral region of lowest reflectance moving from longer wavelengths as the period of IP arrays is increased. Specifically, the wavelength of minimum reflectance it found to be 450 nm for the sample with 400 nm periodicity, 560 nm for 500 nm, 675 nm for 600 nm and, 790 nm for 700 nm periodicity. Similar behaviour was reported by Boden and Bagnall for subwavelength structured moth-eye arrays in silicon [53] and it suggests that the antireflective properties of submicron scale texturing can be tailored for a given application depending on the wavelength range of interest.

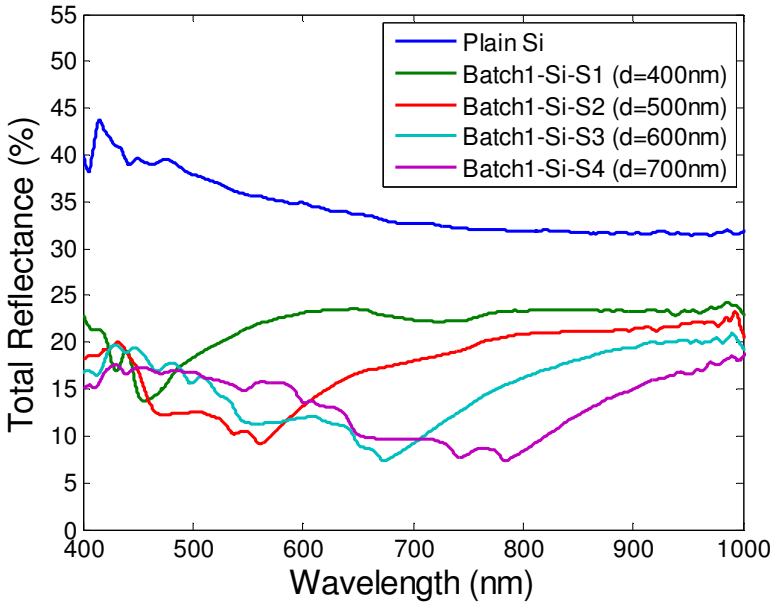


Figure 4.18. Total reflectance measurements from Integrating Sphere for samples along with plain. Si.

Using the IS measurements, average reflectance, R_{ave}, across the wavelength range was calculated for each sample and the results are presented in Figure 4.19. We can see that our analysis suggests an decrease in R_{ave} with increasing array period and feature size.

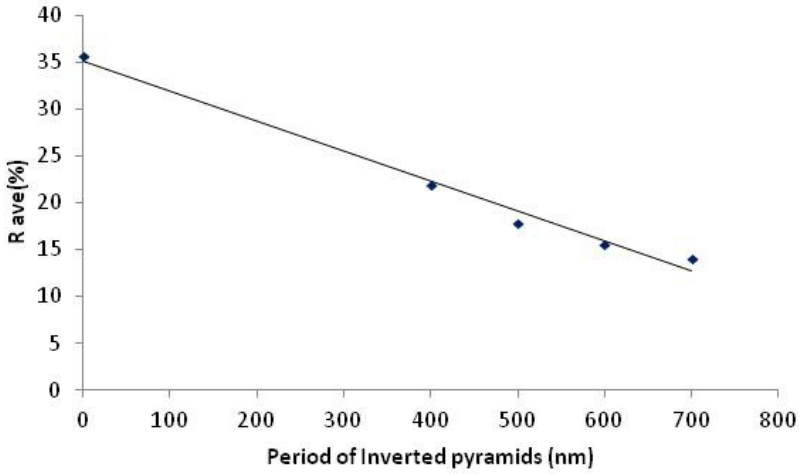


Figure 4.19. Plot of R_{ave} *Vs* IPs arrays from IS measurement.

The weighted reflectance (R_w) was calculated using equation (4.1), where *PFD* (λ) is the AM 1.5 solar spectrum in the form of photon flux density, in units of photons $m^{-2}s^{-1}$ and $R(\lambda)$ is the reflectance measured using the IS technique.

$$R_w = \frac{\sum_{\lambda} R(\lambda) \times PFD(\lambda)}{\sum_{\lambda} PFD(\lambda)} \qquad \textbf{(4.1)}$$

The weighted reflectance is plotted against period of the pyramidal arrays in Figure 4.20, which shows a similar trend as for average reflectance.

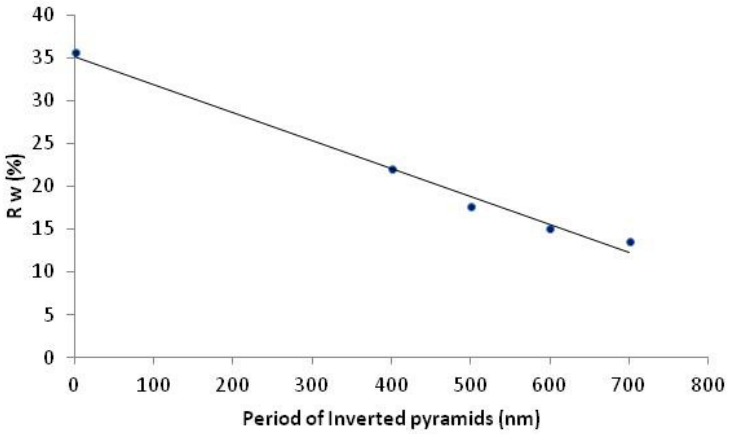


Figure 4.20. R_W plot *Vs* period of IP arrays, calculated from IS measurements.

The IS reflectivity measurements on the submicron-scale IP arrays reveal that the texturing confers some AR effect which is tunable with the period of the array. The total AR effect is found to be significant when compared to a plain silicon surface, but it is not as effective as moth-eye textures or many single layer AR coatings.

Since fabrication of such arrays over areas sufficiently large to enable optical characterization is time consuming and expensive, we decided to investigate the use of numerical simulation to further optimize the design and explore the effects of dimension tuning.

4.5. RCWA Modelling

4.5.1. Model validation with experimental results

Rigorous Coupled Wave Analysis with the commercial software package, GD-Calc, implemented in Matlab as described in section 3.3.1 was used to simulate the reflectance spectra of regular square arrays of IPs in silicon. The inverted pyramid design with base width (w), period (d) and flat region spacing (s) can be specified in a rendering of the model, allowing trends to be explored and feature dimensions optimized.

Firstly, in order to validate the simulation technique, it is important to make sure that results match well to measured reflectance spectra, this way we can then be confident that the simulation results are an accurate representation of what would be found if we were to fabricate and measure such samples.

The values of w, d and s for sample Batch1-Si-S1, listed in Table **4-3**, were used as inputs into the GD-Calc model and the reflectance spectrum at normal incidence was calculated. An SEM image of the pyramid array on this sample, taken at a tilt angle of 25 degrees, is presented in Figure 4.21 (a). The corresponding 3D rendering of the model of this surface in GD-Calc, at the same tilt angle, is shown in Figure 4.21 (b). It is clear from comparing the two images that most of the structural features observed in the SEM image are reproduced in the GD-Calc model.

GD-Calc was then used to simulate the reflectance spectrum over the wavelength range from 400 nm to 1000 nm for both s and p input polarisation. An angle of incidence of 8° was chosen to match the angle of incidence used during the integrating sphere measurement. The resulting spectrum for Batch1-Si-S1 for p polarisation is plotted in Figure 4.22, along with the measured reflectance spectrum from this sample. The simulated p-polarization spectrum matches well to the experimental reflectance spectrum. The simulation program calculates spectra for s and p polarization simultaneously. The spectrum for s polarization and the spectrum for the average of s and p are also plotted in Figure 4.22 for completeness.

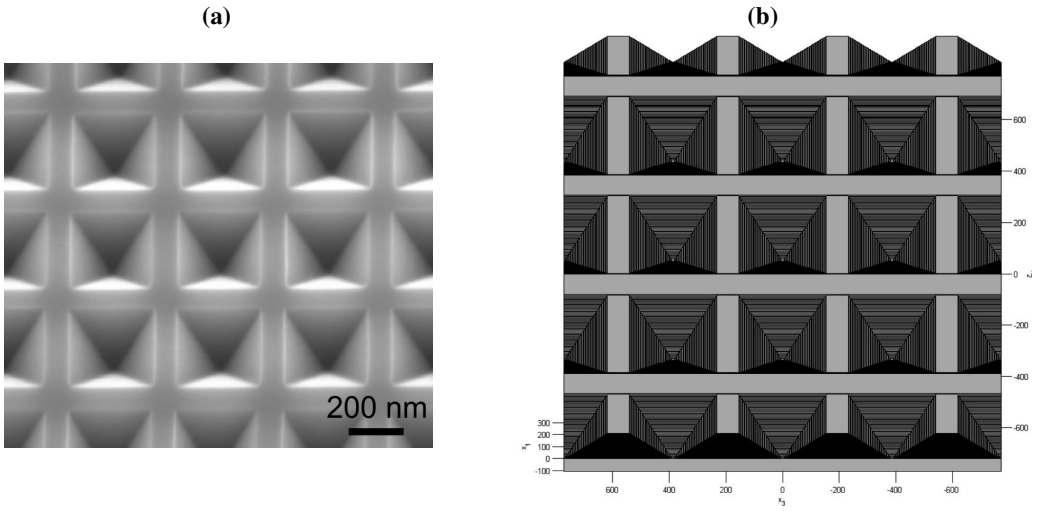


Figure 4.21. Batch1-Si-S1 (a) SEM image, 25° tilt, (b) 3D rendering of GD-Calc model, also 25° tilt.

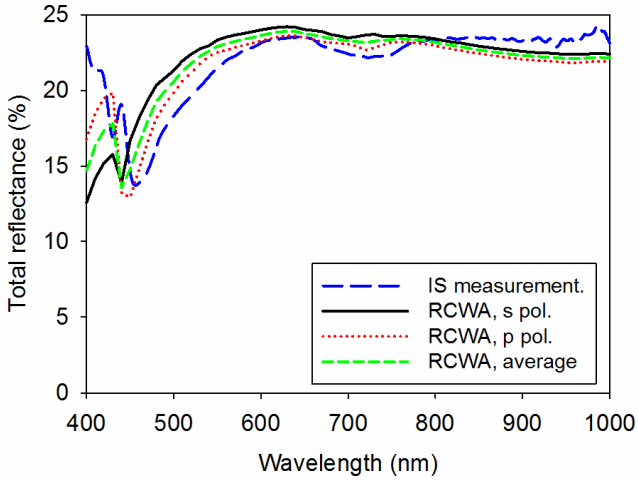


Figure 4.22. Calculated s and p-polarised reflectance spectra from RCWA simulation of sample Batch1-Si-S1 at an angle of incidence of 8°, plotted with the reflectance spectrum from the sample measured using the integrating sphere technique.

Similar RCWA simulations were performed for the other 3 samples in Batch 1. The resulting calculated reflectance spectra for p-polarization at 8°, plotted with the spectra from the integrating sphere measurements are shown in Figure 4.23. Simulation results obtained using the Finite Difference Time Domain (FDTD) method are also included for comparison [98]. Again, the simulation data matches well to the experimentally determined properties of the samples fabricated in Batch 1, and to the results from the independent FDTD simulations. This demonstrates that the RCWA technique, implemented in GD-Calc can be used to accurately predict the properties of our silicon IP arrays and so can be used with confidence to explore the effects of varying structural parameters of the array.

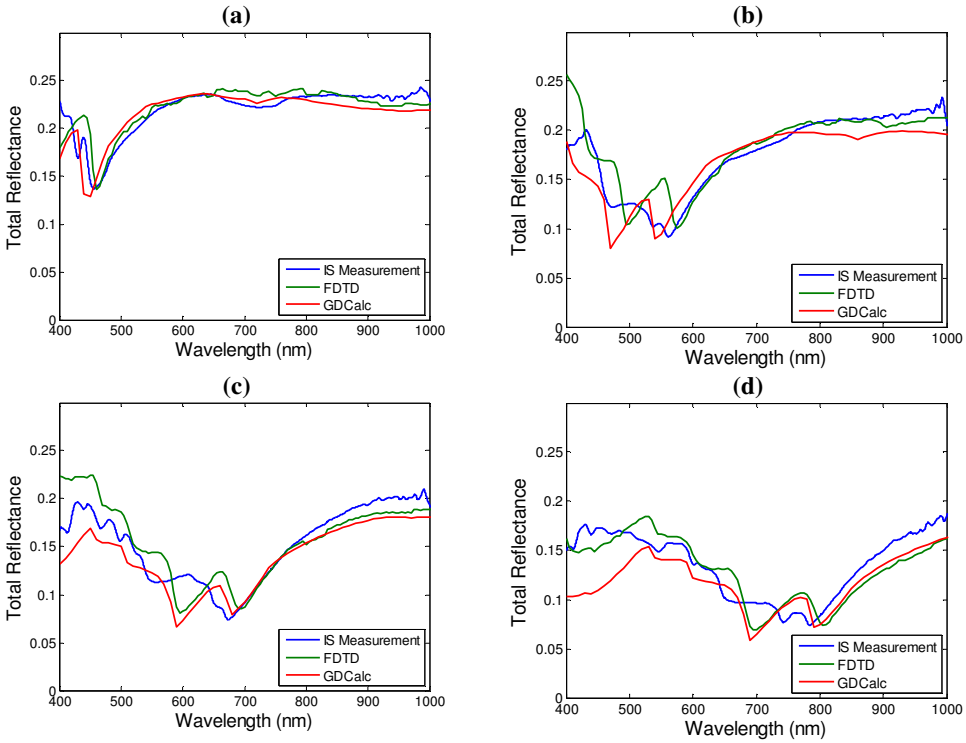


Figure 4.23. Simulated and measured reflectance spectra for IP arrays in silicon from Batch 1 (a) S1, d=400 nm, (b) S2, d=500 nm, (c) S3, d=600 nm, (d) S4, d=700 nm.

4.5.2. **Simulating flat region reduction**

The SEM images of the samples made in Batch 1 reveal that they contain considerable flat areas between the IPs. In micron-scale pyramidal arrays, this is detrimental to the AR properties of the texturing because any flat areas typically, though not always, represent a missed opportunity for AR effect. Therefore, it is necessary to minimize the flat spacer area for micron-scale AR pyramidal textures. The RCWA modelling technique validated in the previous section can now be used to investigate the extent to which removal of the flat areas in our submicron-scale pyramid arrays can reduce reflection even further. The results from this could then be used to inform the design of the next batch of IP arrays.

The RCWA method was used to simulate reflectance spectra of a silicon IP array with periods of 400 nm, 500 nm, 600 nm and 700 nm, for various flat spacer widths from 0 to 100 nm (see Figure 4.24).

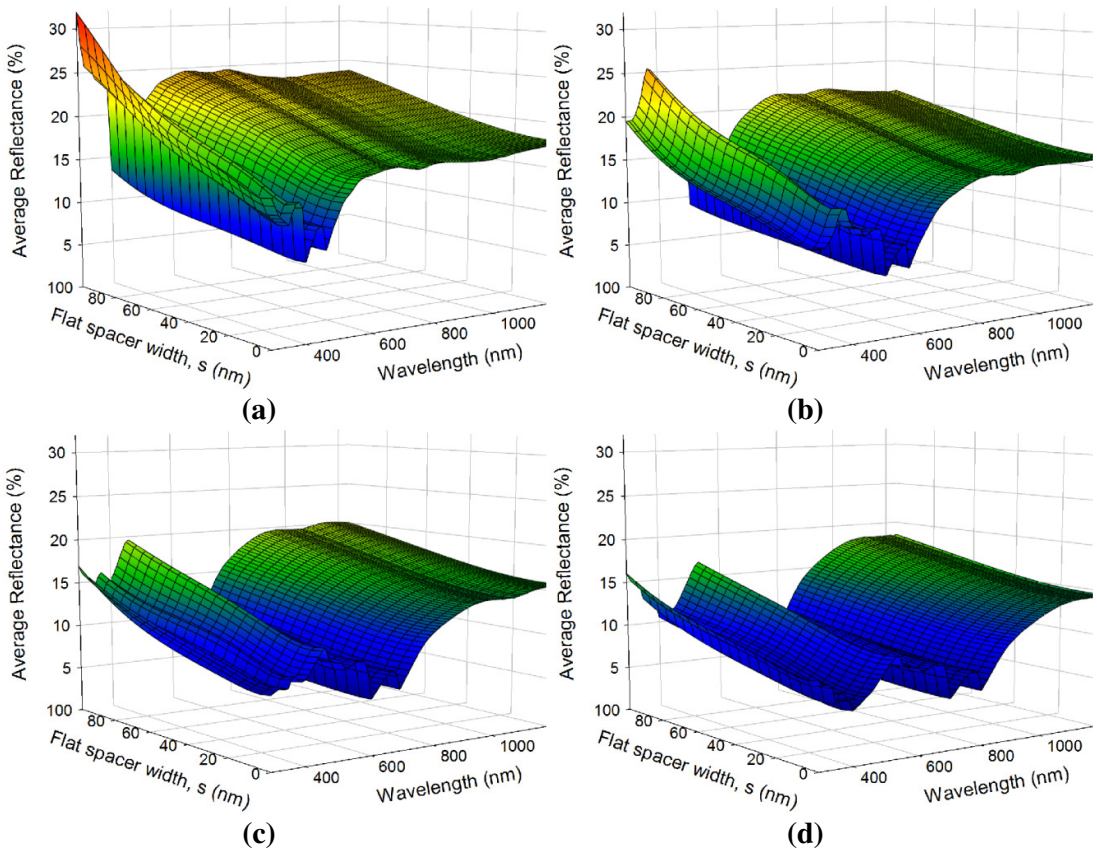


Figure 4.24. Plots of RCWA simulation results showing reflectance (average of s and p) vs. wavelength and flat spacer widths for different array periods, d: (a) d=400 nm, (b) d=500 nm, (c) d=600 nm, (d) d=700 nm (b).The angle of incidence is 8°.

The spectra were then averaged across the wavelength range from 300 nm to 1240 nm to determine the mean spectra reflectance versus flat spacer width for each period (Figure 4.25).

The simulation shows that spacer widths of <10 nm give the lowest mean spectral reflectance. As seen in Table 4-3, the flat spacer widths of the samples fabricated in Batch 1 were approximately 70-90 nm, i.e. far from the optimum range predicted by the RCWA simulations. The simulations predict a reduction in mean reflectance of approximately 25% (e.g. from ~13.5% to 10 % absolute for the 700 nm period array) if the pyramids are fabricated with a flat spacer width of less than 10 nm.

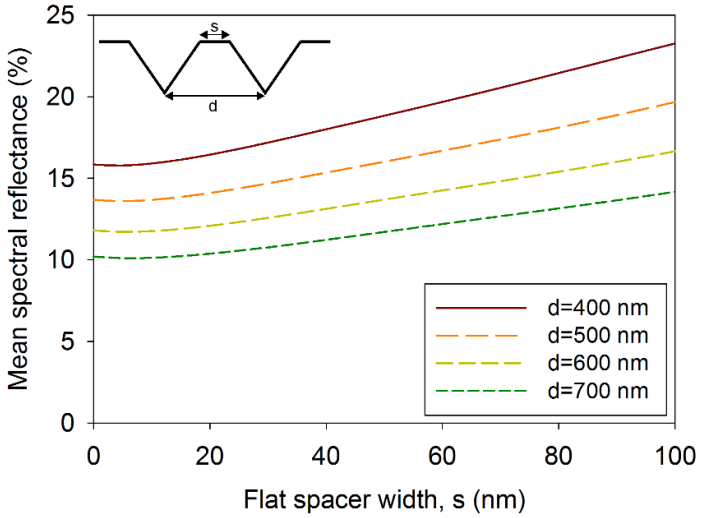


Figure 4.25. Plot of the mean spectral reflectance versus flat spacer width, extracted from the data shown in Figure 4.24, for various array periods.

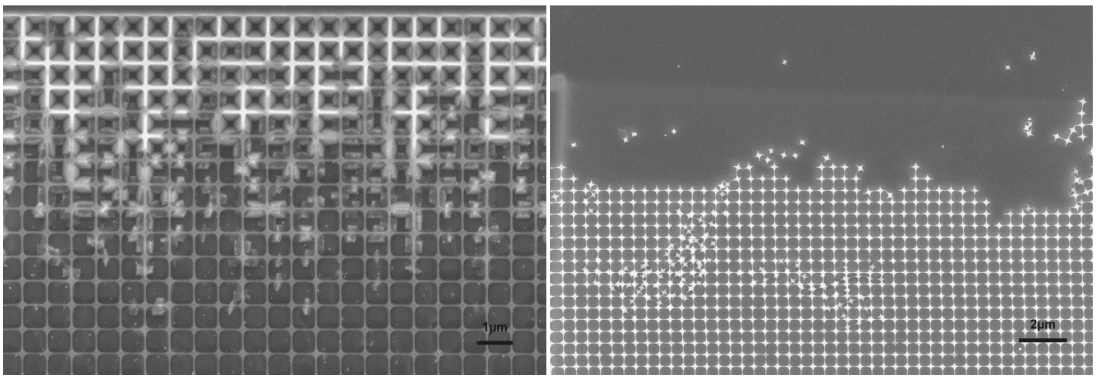
Figure 4.24 and Figure 4.25 also show the extent of the AR opportunities with uncoated IP designs at this 'sub-wavelength scale', the simulations in Figure 4.24 show how spectral features only change gradually with periodicity, and spacer width. Although there are design sweet-spots for specific wavelengths, Figure 4.25 shows there are no design parameters that confer a significant broadband AR effect. Once the space width is reduced it seems that the only way to improve on 10% mean spectral reflectance is to increase the size of features or to add an AR coating, both of these measures move away from the main aims of this work, i.e. to find sub-wavelength alternatives to AR coatings and micron-scale texturing.

The following section describes the fabrication and characterization of a second batch of pyramidal arrays in silicon, with the aim of minimizing the flat spacer width and therefore further improving the AR properties.

4.6. Minimizing the flat spacer width of IP arrays

The simulations in section 4.5 show that IP array spacer widths of <10 nm give the lowest mean spectral reflectance. To minimize the flat spacer widths of inverted nanopyramid arrays, an investigation focused on KOH etching time was carried out. The etch rate of <100> crystallographic planes in silicon is higher than that of <111> planes with KOH solution[50]. Therefore by increasing the etch time, undercutting of the mask will occur, leading to expansion of the base width of IPs and concurrent reduction of the flat spacer width. As we have seen, the first set of samples were fabricated with a 3 minute etch in KOH solution resulting in flat spacer widths of around 70-90 nm (batch 1, described in Table 4-3). A second experimental set of samples were produced with etch times of 4, 5 and 6 minutes.

Inspection of the samples etched for 5 and 6 minutes however, showed the mask to begin to delaminate from the surface as can be seen in the SEM images in Figure 4.26. Here, complete undercutting of the hardmask has occurred in some areas, causing the mask to lift off the surface, exposing the surface completely to the KOH solution.μ



(a) **(b)**

Figure 4.26. SEM images of samples etched in KOH at 80°C for (a) 5 min and (b) 6 min.

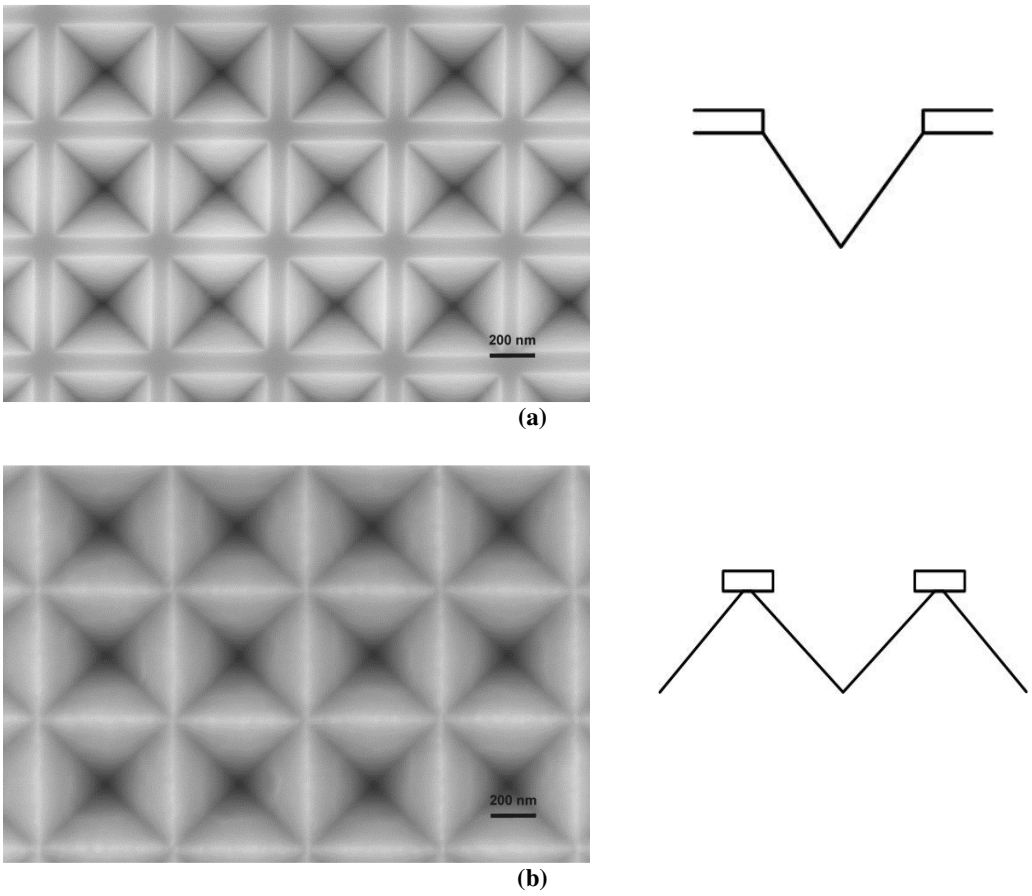


Figure 4.27. SEM images of samples etched in KOH at 80°C for (a) 3 min and (b) 4 min. With schematic illustration of the profile.

The etch time of 4 minutes at 80°C was found to lead to a decrease in spacer width to approximately 20-30 nm, as shown in the SEM images in Figure 4.27. Our second complete sample set for optical characterisation 'Batch 2' were formed with a 4 min KOH etch, SEM images are shown in Figure 4.28 after removal of the Si_3N_4 by HF solution. Measurement of the feature dimensions was carried out on the SEM images of the samples. Table 4-4 presents measured values of base width (w), period (d) and flat spacer width (s) together with the square array dimensions from the e-beam design. The measurements reveal that the KOH etching undercut the Si_3N_4 mask by 70-80 nm on each side. Although not in the optimum region (below 10 nm), the spacer widths of Batch 2 samples are considerably smaller than those of the original sample set and so should lead to an improvement in the AR effect.

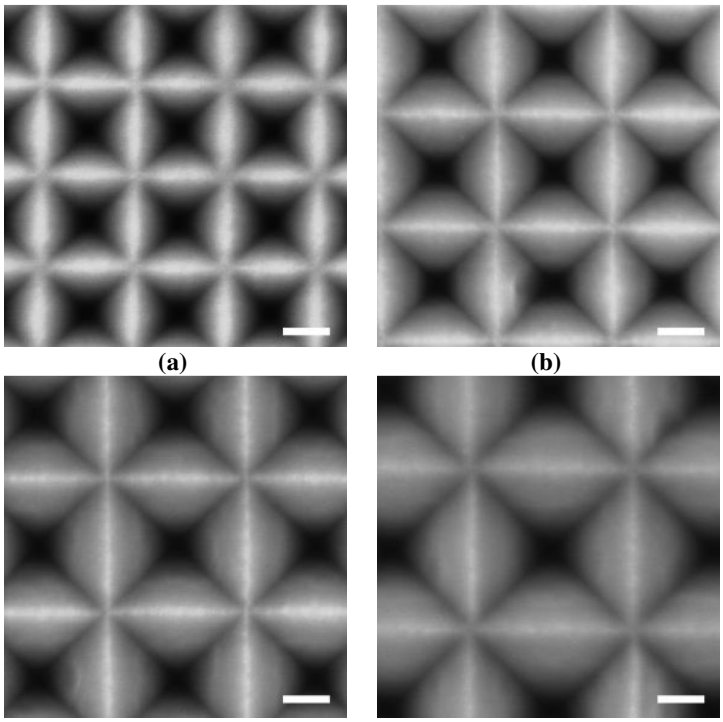


Figure 4.28. Top view SEM images of Batch2-Si, with designed square widths of (a) 200 nm, (b) 300 nm, (c) 400 nm and (d) 500 nm. The scale bars in all images are 200 nm.

Table 4-4 Design values of w, d and s, also measured from SEM images of experimental samples.

Sample Name	Si Pyramid design			Si Pyramid Fabricated		
	w(nm)	s(nm)	d(nm)	w(nm)	s(nm)	d(nm)
Batch2-Si-S1	200	200	400	354(+/-10 nm)	34(+/-10 nm)	401(+/-5 nm)
Batch2-Si-S2	300	200	500	466(+/-10 nm)	24(+/-10 nm)	502(+/-5 nm)
Batch2-Si-S3	400	200	600	567(+/-10 nm)	33(+/-10 nm)	601(+/-5 nm)
Batch2-Si-S4	500	200	700	657(+/-10 nm)	36(+/-10 nm)	703(+/-5 nm)

4.6.1. **Optical Measurements**

The integrating sphere (IS) technique was used (see section 3.2.2) to measure the total hemispherical reflectance from all of the batch 2 samples, using p polarization and an angle of incidence of 8°. Sample Batch1-Si-S4, the sample from Batch 1 that exhibited the best AR effect, was chosen for comparison with the corresponding sample from Batch 2 (Batch 2-Si-S4, 700 nm period). The reflectance spectra from these two samples are plotted in Figure 4.29. Comparing the weighted means of two spectra reveals that by reducing the flat spacing width, the AR effect is improved by ~1%. This is perhaps a surprisingly modest gain considering the reduction of flat surface area, but we have to remember that the photon cannot resolve these features and the whole surface acts as an effective media.

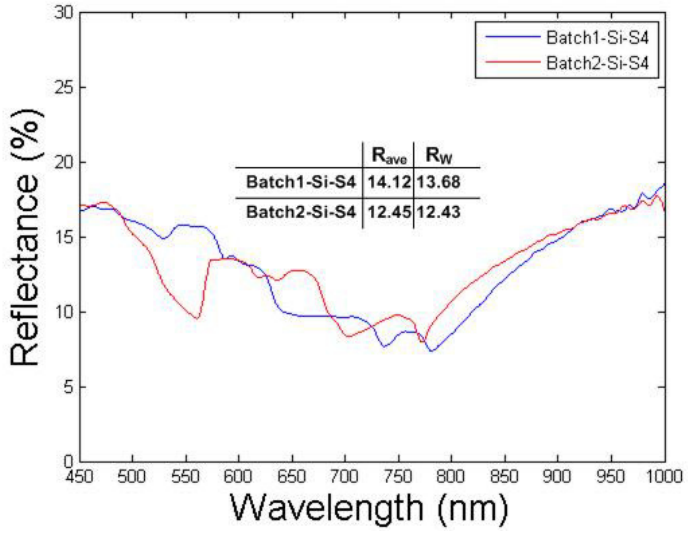


Figure 4.29. Reflectance spectra from IP array samples with 700 nm period from Batch 1 and Batch 2-Si-S4. The mean reflectance (R_{ave}) and weighted mean reflectance (R_w) values for each sample are given in the embedded table.

Angular resolved specular reflectance spectra were collected using a custom built motorised θ-2θ angular reflectance spectroscopy (ARS) system (see section 3.2.3) from all of the samples, using s and p polarization over a wavelength range of 450–1000 nm and an angle of incidence range of 5-85°. Spectra for the average of s and p have been calculated from equation (4.2), where R_s and R_p are the measured reflectance spectra for s and p polarization as defined in chapter 3.

$$R_{average} = \frac{(R_s + R_p)}{2} \qquad (4.2)$$

The reflectance spectra for s and p polarization from Batch 2-Si-S4, for a range of angles of incidence, along with the average of s and p polarisations for same sample are presented in Figure 4.30.

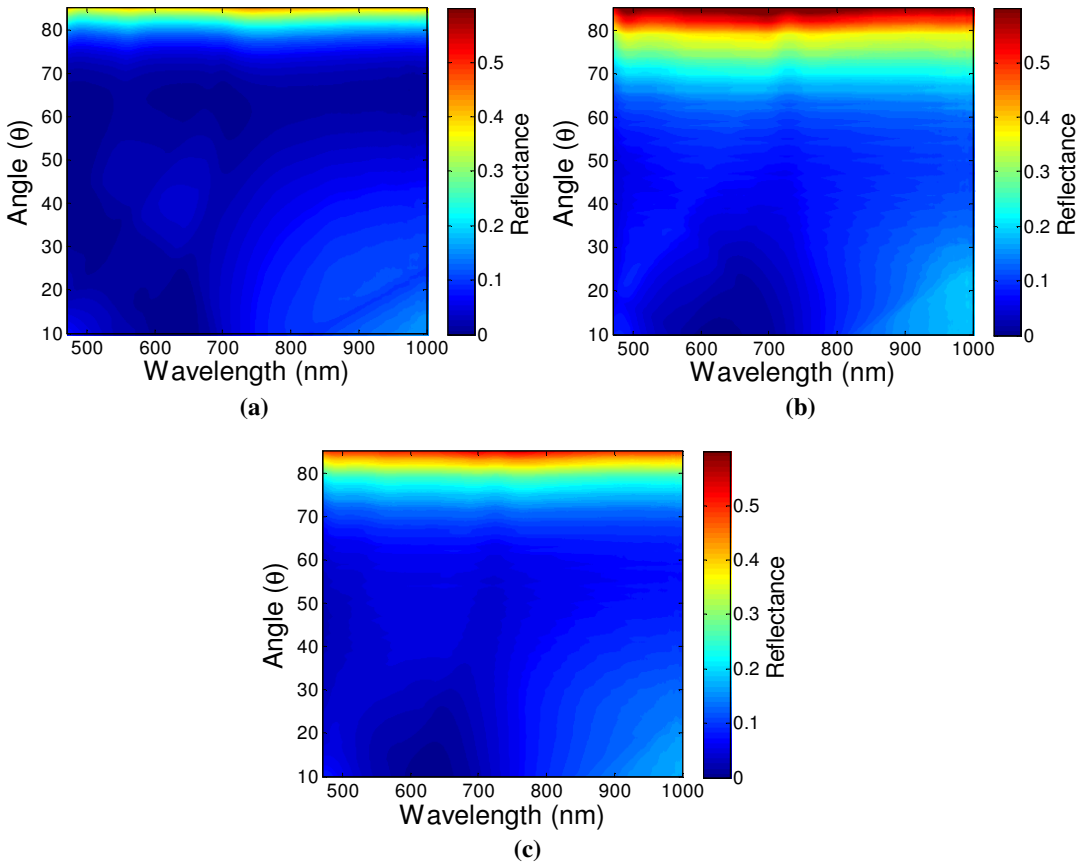


Figure 4.30. Reflectometer measurement results of inverted nanopyramid arrays, Batch2-Si-S4 (w=652 nm, s=36 nm and d=703 nm): (a) R_p input polarisation, (b), R_s input polarisation and (c) average of s and p polarisation.

The reflectance vs wavelength and angle of incidence data (average of s and p) for all of the batch 2 samples are presented in Figure 4.31, demonstrating the antireflective effect of the IP arrays over broad ranges of wavelength and angle.

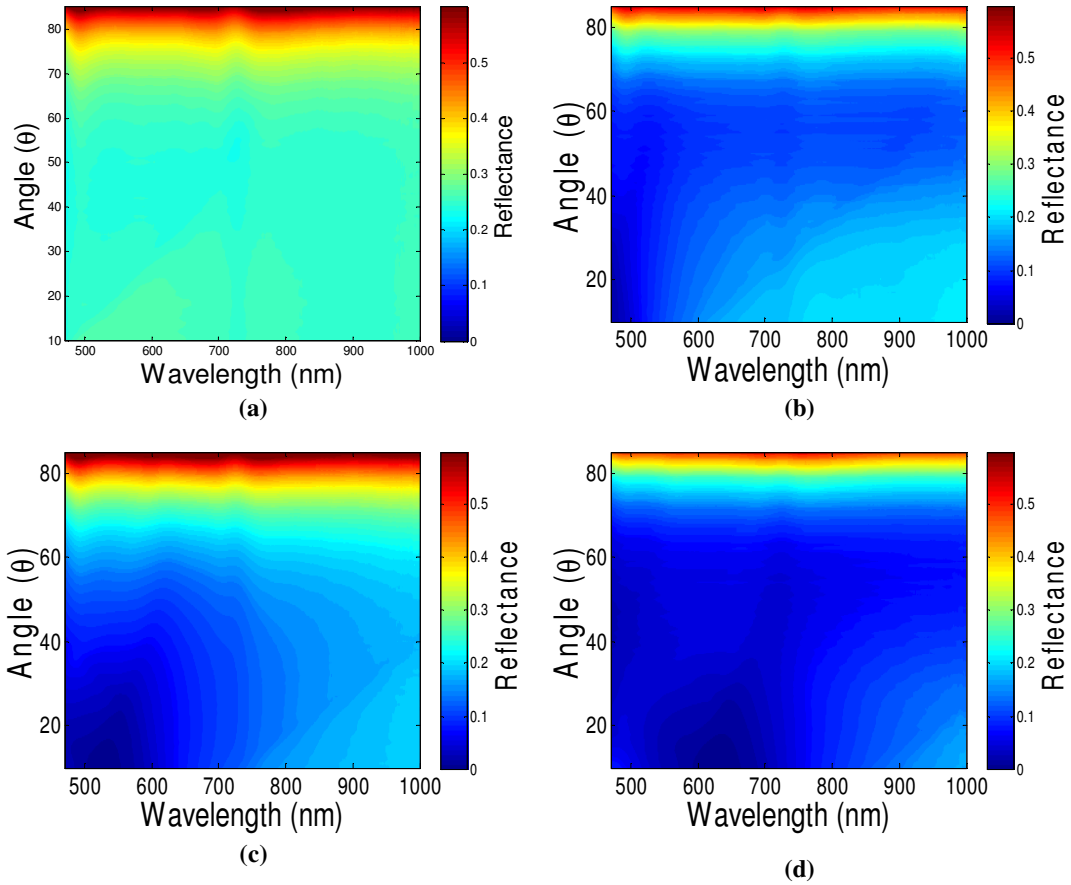


Figure 4.31. Average reflectance of (R_s and R_p) for Batch 2-Si-1-S4, (a) 400 nm, (b) 500 nm, (c) 600 nm, and (d) 700 nm.

Collecting data over a wavelength range of 470–1000 nm and an angle of incidence range of 5-85° enables the weighted specular reflectance (WSR) to be calculated. This gives an indication of how well the AR structure would perform over the course of a day if used on a fixed mounted solar cell. R_w is calculated using equation (4.3), (see section 3.2.4) and $R_{ave}\ (\lambda, \theta)$ is the measured reflectance.

$$R_W = \frac{\sum_{\lambda,\theta} R_{ave}(\lambda,\theta) \times PFD(\lambda,\theta)}{\sum_{\lambda,\theta} (PFD(\lambda,\theta))} \qquad (4.3)$$

The results of calculated R_{ave} and R_w are presented in Table 4-5.

Table 4-5 R_{ave} and R_W value determent from ARS mesurments.

Sample Name	R_{ave} (%)	R_W (%)
Batch2-Si-S1	29	27
Batch2-Si-S2	21	18
Batch2-Si-S3	17	14
Batch2-Si-S4	14	9

From the ARS measurements, average reflectance, $R_{ave,}$ and weighted reflectance, R_w, are plotted against period of the pyramidal arrays in Figure 4.32, showing a near-linear decrease in R_{ave} and R_w with increasing array period.

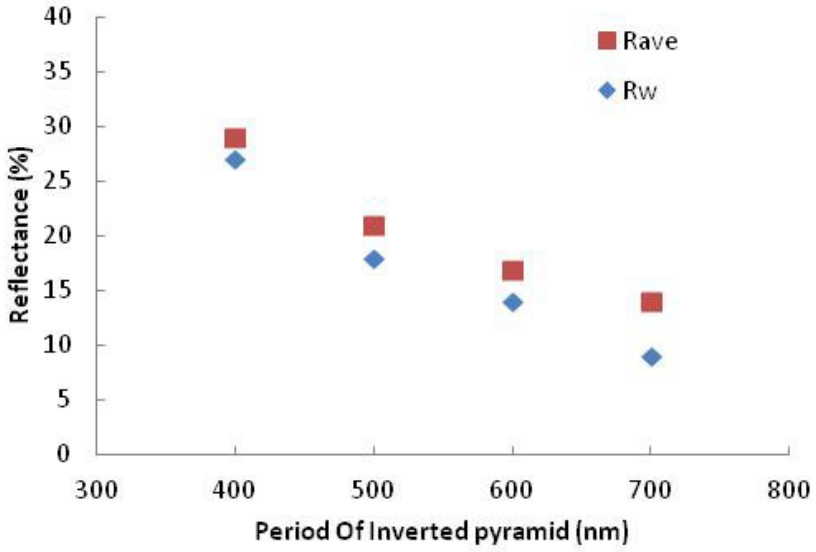


Figure 4.32. Reflectance from ARS measurements *Vs* Period of IP from for all Batch 2-Si samples.

4.7. Preliminary Oxide investigation

Micron-scale pyramidal texturing schemes are often coated with a single or double layer antireflection thin film coatings (SLAR or DLAR) to further enhance the AR effect. In this section, we describe a preliminary investigation into whether a thin layer of SiO_2 can enhance the AR effect conferred by our submicron scale IP arrays. The Leybold Helios sputtering system was used (see Section 3.1.1) to deposit 70 nm of SiO_2 on top of the IP array samples fabricated in Batch 1.

4.7.1. **Optical measurements**

The IS technique was used to measure the total hemispherical reflectance from all of the Batch 1 samples coated with the SiO_2 layer (Batch1-SiO_2) and the weighted reflectance, R_w was calculated using equation (4.1), and compared with R_w calculated from Batch 1-Si samples (i.e. IPs without coating). The results are presented in Figure 4.33 and show that adding a SLAR coating of SiO_2 to the Si surface with IP arrays decreases the AR further.

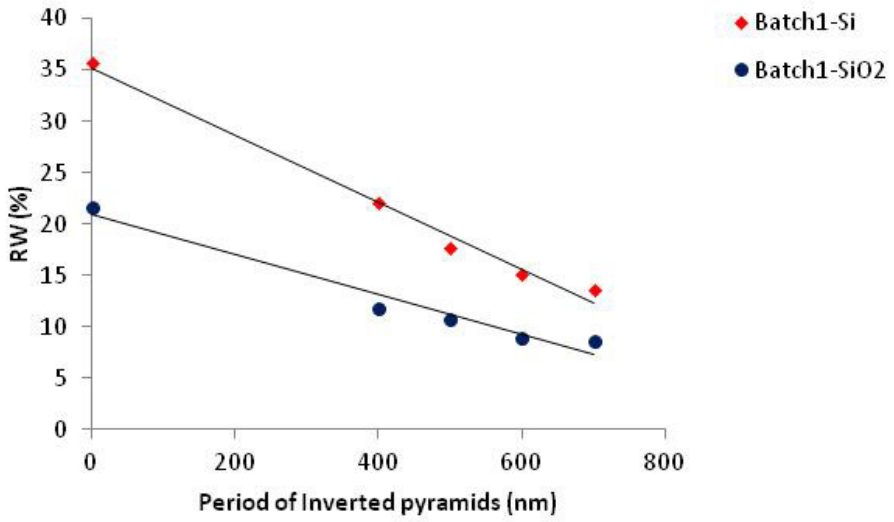


Figure 4.33. Calculated R_w from IS measurements for all IP samples in Batch 1, with and without a 70 nm thick layer of SiO_2.

The samples fabricated in Batch 2 were also coated with 70 nm of SiO_2 and then measured by ARS. Average reflectance was calculated from equation (4.1). The spectra for s and p polarization from Batch 2-SiO_2-S4 along with the average of s and p for same sample and the spectra average of Batch 2-Si-S4 are presented in Figure 4.3.

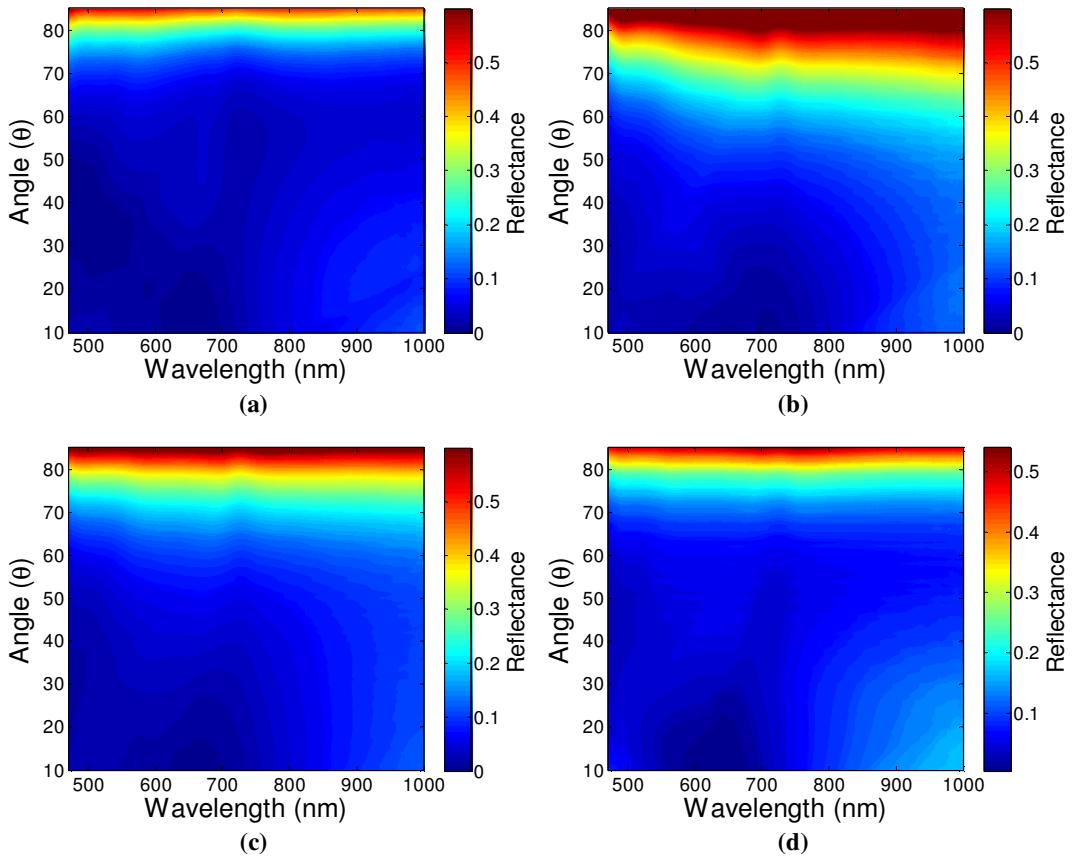


Figure 4.34. ARS measurement of inverted nanopyramid arrays, Batch2-SiO2-S4 (w=663 nm, s=29 nm and d=700 nm) (a) p polarisation, (b) s polarisation, (c) average of s and p and (d) and average of Batch2-Si-S4 (w=663 nm,s=29 nm and d=700 nm).

From the ARS measurements, the average reflectance, R_{ave} and the weighted reflectance, R_w for Batch 2-SiO2 samples were calculated and the results are presented in Table 4-6.

Table 4-6 R_{ave} and R_w values for Batch2-SiO_2 samples.

Sample Name	R_{ave} (%)	R_W (%)
Batch2-SiO_2-S1	31.68	25
Batch2-SiO_2-S2	20.65	17
Batch2-SiO_2S3	16.29	11
Batch2-SiO_2-S4	11	8.5

The results from Table 4-6 are plotted in Figure 4.35, showing that adding a SLAR coating of SiO_2 to the Si surface with IP arrays enhances the AR further.

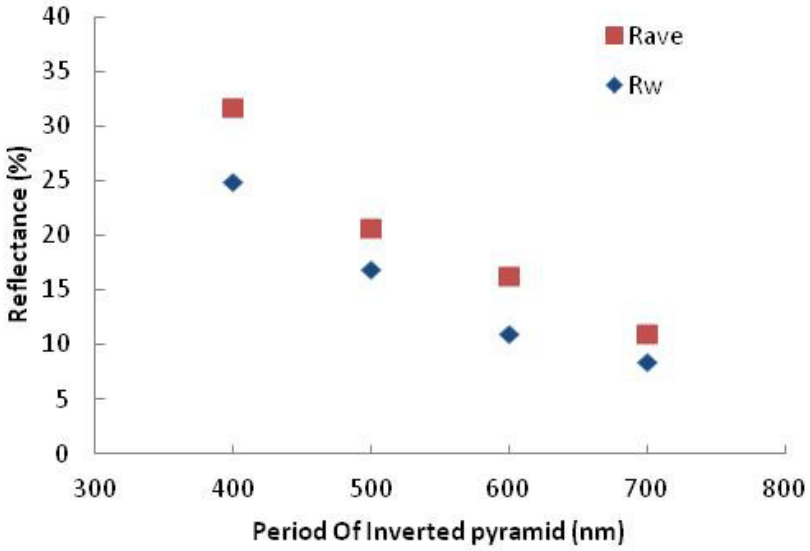


Figure 4.35. Reflectance from ARS measurements *Vs* Period of IP from for all Batch2-SiO_2 samples.

The calculated R_{ave} and R_w from IS and ARS measurements for Batch 2-Si-S4 and Batch 2-SiO-S4 samples presented in Table 4-7 show that adding a SLAR of SiO_2 to the Si surface with IP arrays decrease the reflectance. R_{ave} and R_w measured by IS and ARS show ~ 3-4% improvement when the oxide layer is added to the IP array.

Table 4-7 R_{ave} and R_w values calculated from both IS and ARS measurements for Batch2-Si-S4 and Batch2-SiO-S4.

	Batch2-Si-S4		Batch2-SiO_2-S4	
	R_{ave} (%)	R_w (%)	R_{ave} (%)	R_w (%)
IS	12.45	12.43	8.51	8.46
ARS	14	9	11	8.5

4.8. Conclusion

Antireflective inverted nanopyramid arrays have been fabricated in silicon substrates and their performance in reducing reflectance of the solar spectrum has been analysed. The results demonstrate that IP arrays can confer effective AR to a silicon surface. The spectral position of the reflection minimum can be tuned by varying the period of the array. Reducing the flat spacer area has been shown through modelling and confirmed by experiment to result in a modest decrease in the average and weighted average reflectance of the textured surface. Adding a 70 nm SiO_2 layer has also been shown through experiment to confer an additional antireflective effect.

Further optimisation, both experimentally and through numerical modelling, could be used to further reduce reflection from designs of inverted pyramid structures. It should be possible to reduce the spacer width, and optimisation of the SLAR coating material and thickness could still improve performance. However, it is clear that significant improvements to AR can only really be managed through increasing the periodicity of the design and building bigger and thicker features. Although it might be interesting to find the optimum feature size and periodicity this would be moving away from our main purpose of finding a sub-wavelength texturing system that could be applied to very thin photovoltaic devices, to this end our attention was drawn to *Mie Resonator Arrays*.

5.Mie resonator arrays

The development of low-cost techniques that can minimize reflection of semiconductor surfaces is important in maintaining efficiency improvements for a whole range of photovoltaic technologies. In this chapter we investigate a relatively new antireflective scheme based on subwavelength *Mie resonators* and compare to sub-wavelength 'moth-eye' arrays. We show that correctly designed Mie resonator arrays have the potential to outperform moth-eye arrays and reduce reflectance to low levels over a wide range of illumination angles and spectral conditions experienced by a fixed solar cell over the course of a day.

5.1. Introduction

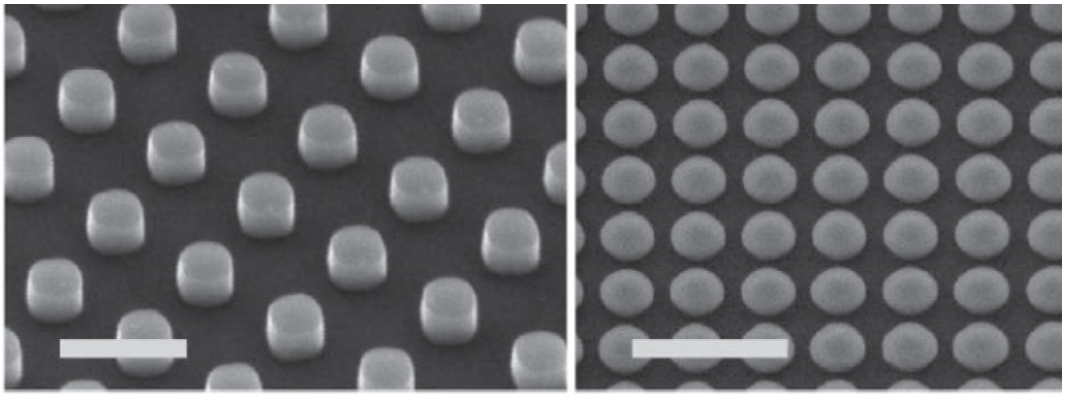
In addition to traditional thin film antireflective coatings (ARCS) [48, 99], reflection from a silicon surface can be reduced by a range of texturing schemes. These include micron-scale pyramidal features [100, 101] and the more recently developed *sub-wavelength structures*, which can be further subdivided into two distinct classes: The biomimetic 'moth-eye' schemes of closely packed, tapered pillars [53, 86, 102-104] and *Mie resonator arrays*, recently described by Spinelli *et al.*[105] consisting of relatively sparse arrays of short cylindrical pillars (Figure 5.1) [106].

Mie Scattering [107], occurs when light is scattered by particles of a size comparable to the wavelength of light whereas *Rayleigh Scattering* accounts for scattering by particles much smaller than the wavelength of the light. Mie scattering is a powerful and important physical phenomenon that can accurately predict the angular scattering of light due to metal nanoparticles in a solar cells [47] as well as explain the existence of rainbows [108]. In cases where Mie Scattering is important, incident light will correspond to a resonant dipole (or higher order mode) in the particle and light will be strongly scattered radially with an angular distribution that reflects the nature of the particle and its surrounding media [47]. As a result of this Mie scattering can be exploited to strongly scatter specific wavelengths of light in particular directions and the size and shape of the particle can be changed to tune the effect to the wavelength of interest. The second important feature of Mie scattering is that the size, nature and shape of the particle also determines the optical cross-section which at resonance can be

significantly larger than the physical size of the particle. As a consequence of these two features, scattering by low coverages of metallic or dielectric particles have been extensively studied. Classic *Mie Theory* describes the scattering of light by a homogenous sphere and is based on specific solutions of Maxwell's equations. Analytical solutions can also be found for spheroids [109] however, for more complex structures Discrete Dipole Approximation (DDA) codes or FDTD modelling is commonly used [110, 111].

Spinelli *et al*,[105] formed their Mie Resonator arrays Figure 5.1 by a *soft-imprint* process with the capability of patterning large areas which is low cost and potentially compatible with solar cell manufacturing. In this technique, a pattern moulded in a rubber Polydimethylsiloxane stamp with a master Si wafer which was patterned and prepared using electron beam lithography or optical interference lithography techniques. They Spin-coat a layer of sol-gel (details of the sol-gel were not supplied by the Authors) on the Si wafer, using the fabricated master stamp to transform the patterns into a sol-gel layer. The sol-gel acts as a hard mask layer for formation of Mie resonator arrays pattern on Si using RIE process.

A master template with a 4×4 mm^2 array of 250 nm diameter, 150 nm high and 450 nm pitch was fabricated on a 4-inch Si (100) wafer using electron beam lithography and etching. The pattern in the sol-gel was transferred to the Si wafer with a two-step RIE Process. In the first step a combination of N_2 and CF_4 gas was used to etch through the sol-gel layer, and in the second step N_2 and Cl_2 gases were used to etch the Si wafer. After the dry etch RIE process, the sol-gel mask was removed with diluted HF and finally layers of different thicknesses of Si_3N_4 were grown on the top of samples using low-pressure chemical vapour deposition (LPCVD).



(a) **(b)**

Figure 5.1. (a) Scanning electron microscopy image taken under an angle of 40° of a bare Si NP array (scale bar represents 500 nm) and (b) a Si NP array coated with a 60-nm-thick Si_3N_4 layer (scale bar represents 1 µm) [105].

The study by Spinneli, working in the group of Albert Polman [105] not only introduced the concept of Mie resonator arrays, but also provided a very detailed account of the optical properties of their samples with a number of diameters, heights and periods. The study used both Mie Theory and FDTD simulations to show how the dielectric nanoparticles can act as a cavity with a high quality-factor (Q=10) and with well-defined resonance as determined by the dimensions of the nanoparticle (Figure 5.2). When a cylinder of similar diameter is attached to a substrate the resonances are found to broaden and a *leaky channel* into the substrate is formed that confers beneficial AR effects to the structure. Even with the leaky channel the resonance enhances the scattering cross-section by a factor of four so, as with plasmonics a relatively low feature density is sufficient to provide effective AR.

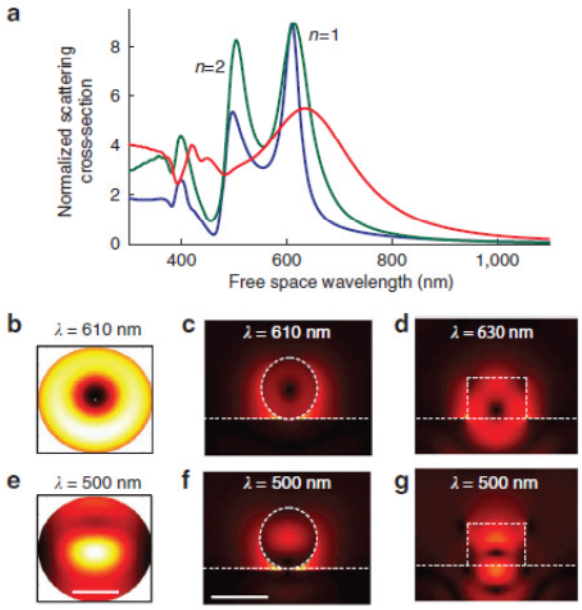


Figure 5.2. Mie scattering on a Si wafer. (a) Scattering cross-sections, normalized to geometrical cross-section, for a Si sphere in air (blue), a Si sphere on a Si substrate (green) and a Si cylinder on a Si substrate (red). 1st and 2nd order Mie resonances indicated. (b–g) E-field intensity (colour scale) in a cross-section of the particle for a sphere in air (b,e), a sphere on substrate (c,f) and a cylinder on substrate (d,g), for Mie modes of first (b–d) and second (e–g) order. Wavelengths used for calculations indicated in each panel. Plots for a sphere in air are calculated with Mie theory; particles on a substrate are simulated. Scale bar in e is 50 nm, and refers to b and e. Scale bar in f is 150 nm and refers to c,d,f and g [105].

Spinelli *et al*, provide a detailed account of the weighted reflectance (Figure 5.3) and specular reflectance for a range of angles of incidence (Figure 5.4) from Mie resonator structures. Their *total reflectance spectroscopy* technique shows an average reflectivity of only 1.3% over the 450–900 nm spectral range and the strongly reduced reflectivity is observed for a broad range of angles of incidence up to ± 60°. Overall Spinelli *et al*, have shown that dielectric Mie-scattering can be as effective as plasmonic scattering without some of the challenges inherent with plasmonics. For example, there are no parasitic losses similar to those that occur in metal nanoparticles and there is potentially no need for any new materials within a photovoltaic structure. Patterning of the substrate or a dielectric layer is sufficient to achieve excellent results with, as a consequence little compromise of surface recombination rates. Perhaps the one remaining drawback of the Mie resonator AR scheme is the additional complexity of the process, although Spinelli *et al*, have demonstrated whole-wafer nano-imprint lithography this is still more complex and significantly more costly than a random pyramid etch.

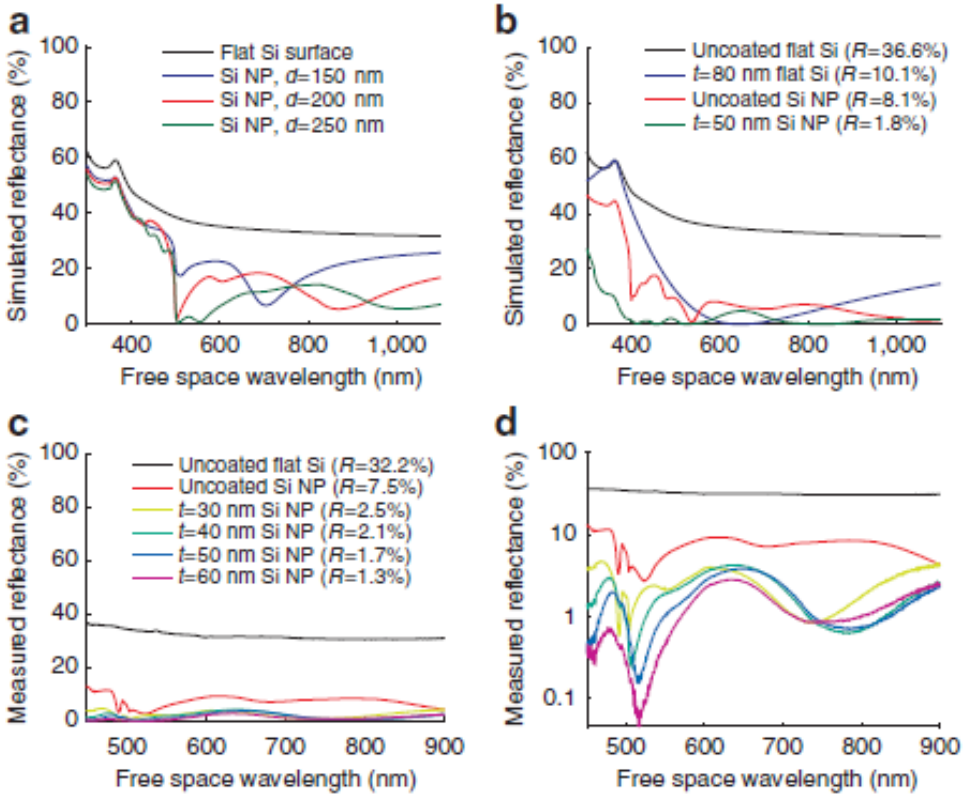


Figure 5.3. Ultra-low reflectivities. (a) Simulated reflection spectra from a regular square array of Si NPs spaced by 500 nm, with a height of 150 nm. (b) Simulated reflection spectra for a bare flat Si substrate a flat Si substrate coated with a standard Si_3N_4 antireflection coating (t = 80 nm), a Si surface with bare Si nanostructures on top and a Si surface with Si nanostructures on top coated with an optimized Si_3N_4 layer (t = 50 nm). (c) Measured total reflectivity of a bare Si wafer, an uncoated Si Nanopillar (NP) array and four Si NP array coated with Si_3N_4 layers of different thicknesses, (d) The same reflectivity data plotted in logarithmic scale [105].

As we have seen the Mie resonator structures operate through the coupling, by preferential forward scattering, of resonant Mie modes into an underlying substrate. Tapered moth-eye structures, conversely, operate through a graded index mechanism which removes the step change in refractive index at an interface [53]. It has been shown by experiment and simulation that both types of subwavelength AR structure have the potential to improve on widely-used thin film coatings and micron-scale texturing for the reduction of reflectance in photovoltaic devices, thereby leading to more efficient solar cells. Inspired by the work of Spinelli *et al,* and with the nanofabrication skills available in Southampton, coupled to a strong background in optical characterisation of moth-eye surfaces in particular, we decided to take a closer look at the Mie resonator structures in order to gain additional insight and attempt optimization of the structures.

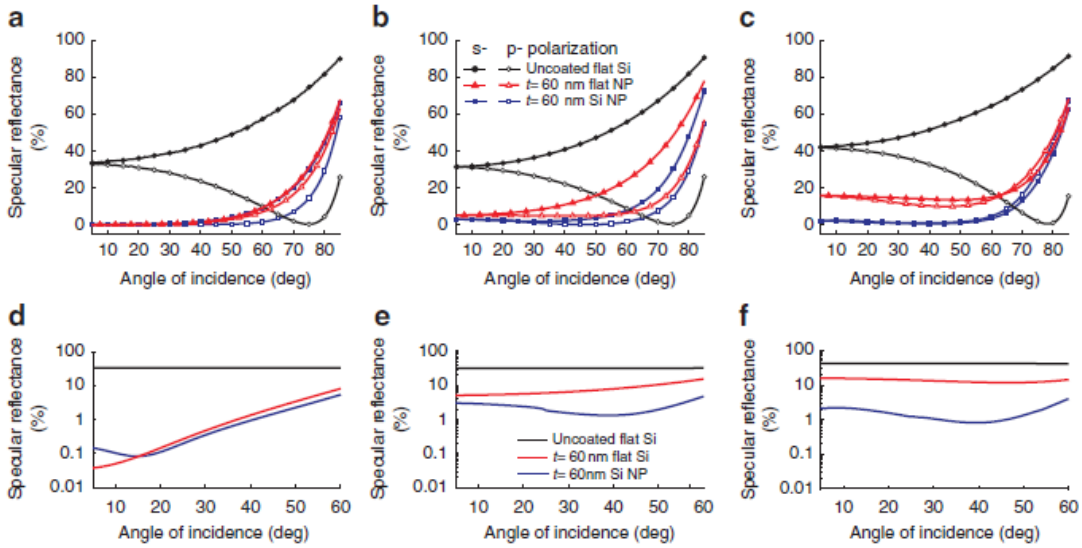


Figure 5.4. Angle resolved reflectivity. Specular reflectivity measured as a function of Angle Of Incidence (AOI), for wavelengths of 514 nm (a,d), 632 nm (b,e) and 405 nm (c,f). Panels in the top row show results for s- (solid symbols) and p-polarized (open symbols) incident beam, whereas the bottom row show an average of s- and p-polarizations, plotted on a logarithmic scale. In each graph, reflectivities from a bare Si wafer (black lines), a 60-nm standard Si_3N_4 coating (red) and a coated NP array (blue) are shown [105].

5.2. Initial Design

This sections, presents the fabrication and optical characterization of silicon Mie resonator arrays, with a focus on the application of these arrays as antireflective schemes for silicon solar cells. Structures with a range of periods, heights and pillar diameters are investigated, firstly using an integrating sphere system for near-normal incidence reflectance measurements and then with an angular reflectance spectroscopy system. The results are compared to similar results from; an uncoated flat silicon surface, several thin film ARCs, and a silicon moth-eye array.

My initial designs were based on those described by Spinelli et *al*. [105] but with a wider range of parameters. My aim was to produce arrays of silicon resonators carved into a silicon surface. In my experimental design I set out to make 21 different samples each with arrays of different diameter, period and height (Table 5-1). Each sample would be 1 cm x 1 cm in area with a 0.5 cm gap between each array to allow dicing and handling.

Table 5-1 Mie Resonator Sample Designs Values of diameter (d), period (p) and height.

Sample	Lateral Design		Height (nm)		
	d (nm)	p (nm)	Set1	Set2	Set3
D1	250	500	100	150	200
D2	250	450	100	150	200
D3	225	450	100	150	200
D4	200	400	100	150	200
D5	150	500	100	150	200
D6	125	500	100	150	200
D7	100	500	100	150	200

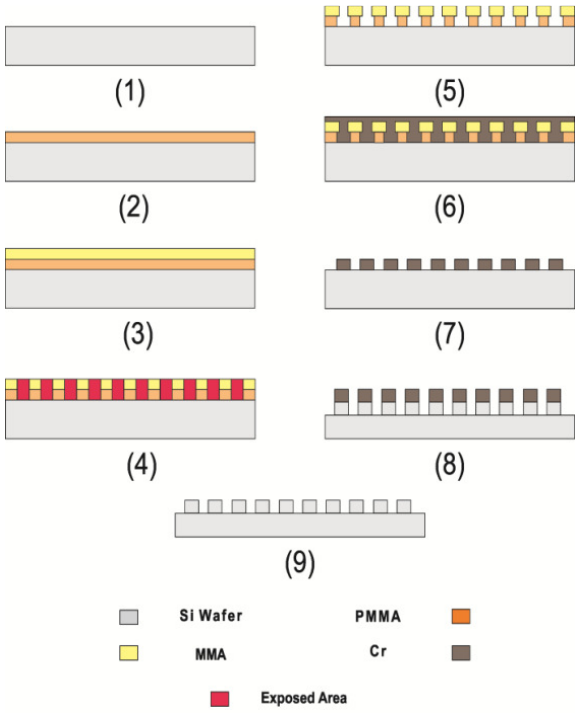
5.3. Fabrication of Mie resonator arrays

The process for fabrication of the Mie scattering arrays on silicon is presented in

Figure 5.5. The principle aim of the process design is to define a pattern in chromium and then to use the patterned chromium as a hard mask during the subsequent etching of silicon.

There are two lithographic methods that can be used to define a metal pattern on a surface. It is possible to deposit the metal, deposit and pattern the resist and then remove

any unrequired metal by etching. Alternatively, in the *lift-off* approach [112], the metal is deposited on top of the patterned resist, then the metal on the resist is lifted-off to leave behind the desired pattern. In general lift-off is good for small island features where most of the metal is not required, whereas the 'metal first' approach is good for removing relatively small amounts of metal from an otherwise continuous metallic layer. The lift-off technique was clearly going to be the best approach for this work. The following sections provide details on each of these steps in turn.



1. Clean 150 mm standard p type Si wafer
2. Spin MMA resist
3. Spin PMMA resist
4. E-beam expose
5. Develop
6. Deposit 50 nm Cr on Si wafer
7. Lift-Off
8. Dry etch with ICP
9. Remove Cr

Figure 5.5. Process steps for the fabrication of Mie resonator arrays.

5.4. Substrate selection and wafer cleaning

The starting material was a standard single side polished, 6 inch p-type silicon substrate with 600 µm thickness and (100) orientation. Before the start of any processing the silicon wafers were cleaned using RCA1 (for 5 min at 40°C) solution to remove any organic contaminants, following that, RCA2 (5 min at 40°C) was used to remove any ionic contamination [91, 92], then to remove any oxide layer, a HF 7:1 solution was used [93]. Cleaning was completed by rinsing and drying the Si wafers.

5.4.1. **Resist spinning**

In order to get the best results from a lift-off process at a nanoscale it is often found helpful to use two resists in a *bi-layer* structure [113, 114]. By making the lower of the two resists slightly more sensitive to the exposure process it is possible to undercut the upper resist bi-layer of Methyl Methacryllate (MMA) 8.5 (300 nm) and Poly Methyl Methacryllate (PMMA) 495 (150 nm) resist have been used in this work, both resists are E-beam responsive and positive. When the metal layer is deposited the undercut in the resist profile ensures that the metal cannot form a continuous film and independent particles are formed on the substrate, this then allows the lift-off to proceed without having to 'rip' the metal film.

In this work a MMA/PMMA bi-layer process has been used which was developed by the Nano Research group, at the University of Southampton [115].

In this process the MMA is spun coated first as this is more sensitive to electron beam exposure, the MMA is then soft-baked at 150°C for 3 minutes and allowed to cool for 5 minutes at room temperature. PMMA is then spin-coated as the second layer and that in turn is soft-baked at 180°C for 3 minutes. The MMA/PMMA spin details are provided in Table 5-2, the targeted total thickness of the bi-layer was 400nm.

Table 5-2 MMA/PMMA resist spin recipe details.

Spin recipe details	speed (rpm)	time (s)	accel (rpm)
	0-500	5	100
	500-5000	2	2250
	5000	45	0
	5000-100	1	4900
	100-0	1	0

5.4.2. **E-beam Exposure and Development**

L-edit software was used to design arrays of circles with the range of diameters and periods described in Table 5-1. It is satisfactory to use hexagon patterns in designs instead of circles because resists and metals will generally round to form circles, and circles are data intensive in both L-edit and e-beam processing. Hexagonal designs with six different diameters (d) in the range 100 to 250 nm and three different periods (p) of

400, 440 and 500 nm were defined in L-Edit. L-Edit files were then converted using Genesis software to a format which is compatible with the E-beam tool.

The standard proximity corrected base dose for e-beam patterning in the Southampton system was 650 μCcm^{-2}, however, it was necessary to carry out process optimisation of the e-beam process. To do this a series of tests were carried out to determine the appropriate e-beam dose-level for my designs since the size of the pattern will be effected by the dose-level.

I decided that optimisation of the e-beam stage could be most effectively achieved by optimising to the size of the metal circles (rather than holes in a resist). So during these experiments the processes described in sections 5.4.3 and 5.4.4 were also carried out.

In order to ascertain the appropriate dose, a dose level range of values between +100% and -25% of the dose of 650 μCcm^{-2} was chosen. For these tests the pattern area was designed to be 3mm by 3mm for each design. The reduced area was important to reduce write-times but needed to remain large enough to make sure that proximity effects were not significantly changed. Figure 5.6 shows how increasing the dose level increases the size of the metal particles. With decreasing dose level the edges of the features become less well defined. Figure 5.6 shows the effect of the dose tests for samples with 230nm diameter, the average diameter with dose level is plotted in Figure 5.7.

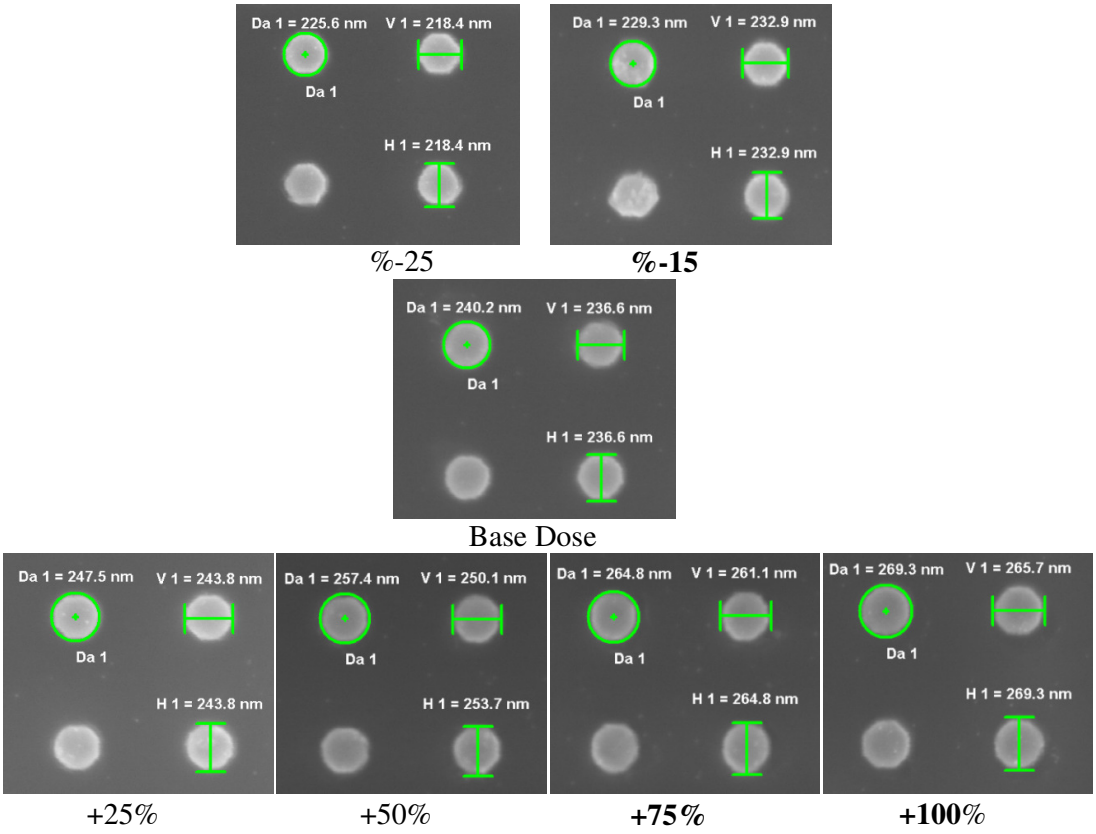


Figure 5.6. SEM of dose test for a sample with 230 nm diameter.

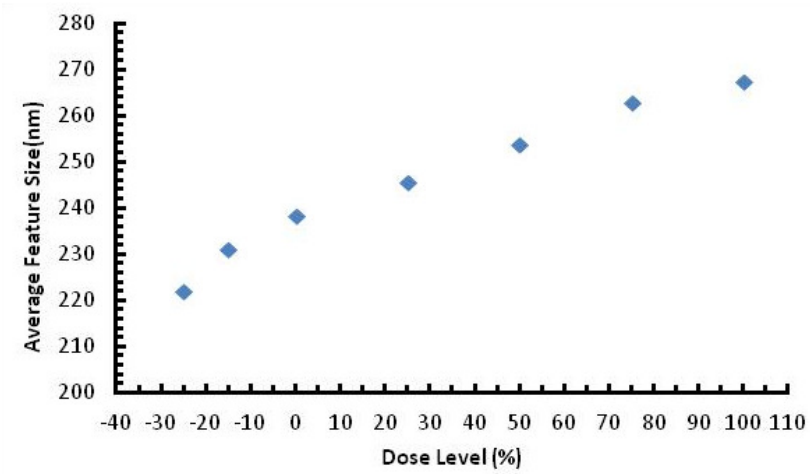


Figure 5.7. Diagram of average diameter aligned with dose level.

In some cases decreasing the dose level causes incomplete exposure of some areas of the resist. As a result Cr deposits on thin residual areas of resist and then delaminates in the lift-off step (Figure 5.8).

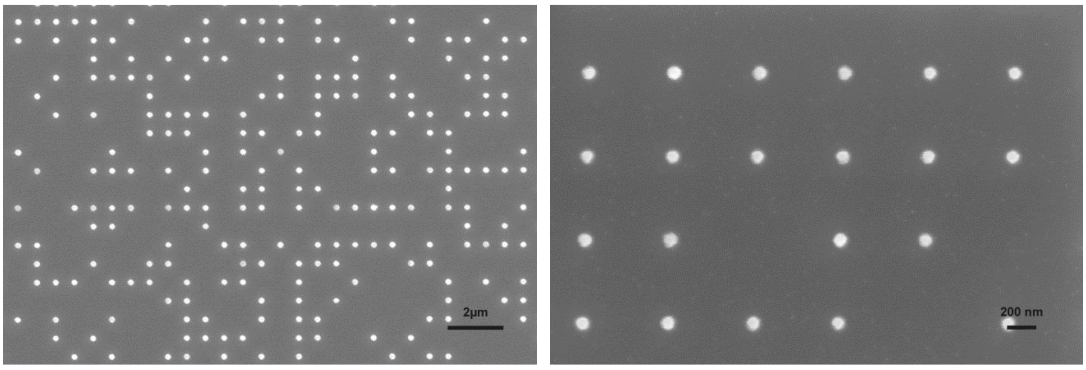


Figure 5.8. SEM Image showing the effect of low dose level.

These experiments confirmed 650 μCcm^{-2} as a suitable dose level for sample sizes required, though this dose tended to form circles a little larger than the targeted diameters, the dose was necessary to ensure all the circles were sufficiently exposed. For three sets of samples (D2, D6, D7) the Cr diameters were much greater than intended so we decided to redo the three samples, however, during this time the e-beam chamber had been replaced and the dose had to be increased by 25% in order to achieve the desired results.

5.4.3. **Cr hard mask formation**

To remove the areas of the bio-layer resist exposed by the electron beam the wafers were submerged in Methyl isobutyl ketone (MIBK):IPA solution (2:1) for 90 seconds, and then rinsed in IPA for 30 seconds [116]. The concentration of MIBK in the solution had a significant effect on the resist sensitivity, for lower sensitivity the MIBK concentration can be reduced [117].

After the development process, Cr is deposited using a standard recipe on the Lab700 Physical Vapor Deposition *(*PVD) which has been optimized at the University of Southampton. The electron-beam evaporator tool (Lab 700) is highly directional as required by this lift-off process (see section 3.1.3). The process was set to ensure a non-critical thickness of 50 nm of Cr on the wafer.

5.4.4. **Lift-off**

Lift-off was carried out by wafer submersion in *n-methylpyrrolidone* (NMP) at 60°C to leave a hard mask of chromium disks on the silicon surface [117]. An SEM image of successful pattern formation is shown in Figure 5.9.

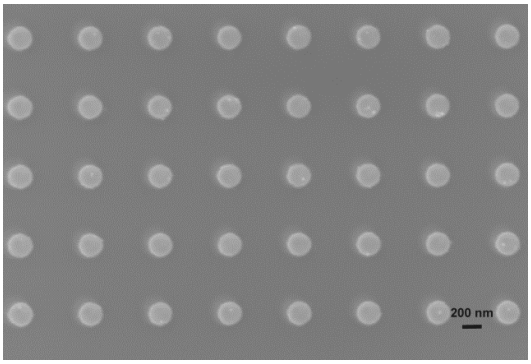
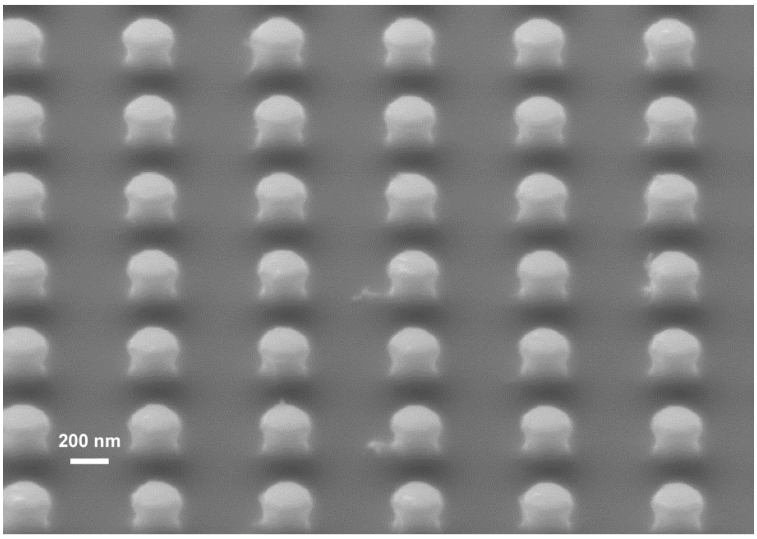


Figure 5.9. SEM image of typical design after lift-off process.

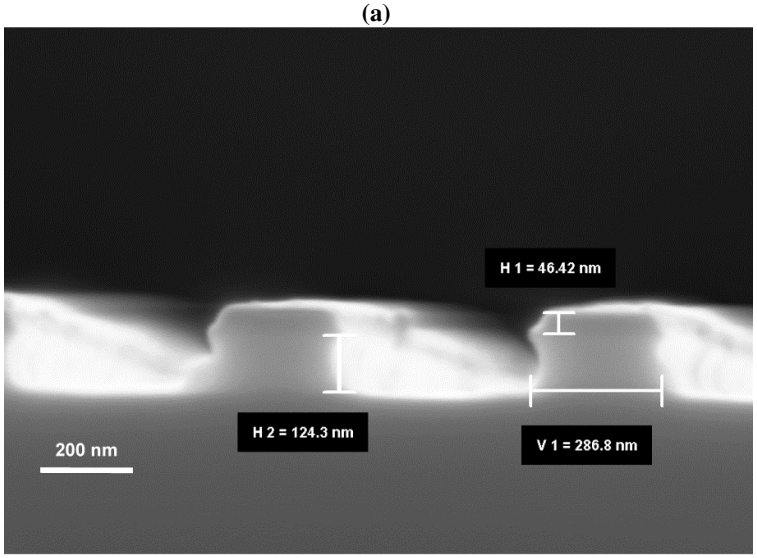
5.4.5. **Dry etch using ICP tool**

Samples were diced to 1cm x 1cm chips and ICP Etching (section 3.1.6) was carried out to form the silicon Mie scattering arrays.

In the first experiments each sample was attached to a carry wafer bonded by photo resist, however, this methodology was found to form an undercut beneath the Cr mask and so could not achieve a vertical profile (Figure 5.10).



(a)



(b)

Figure 5.10. SEM images a typical sample showing an undercut.

First investigations to prevent this undercut issue, concentrated on changing the ICP etching parameters, e.g. gas, temperature and chamber pressure however none of these removed the problem. After some discussions it became apparent that a build-up of charge on the sample was potentially causing the undercut to occur and that the charge build-up was due to the insulating nature of the photoresist used to bond the sample to the carry wafer.

Different bounding techniques were examined, carbon tape was used at first but this did not solve the issue, the next set of experiments were based on a new *crystal bonding* technique.

Crystalbond™ '555' is a commercially available temporary wafer mounting product designed to provide high-bond strength and easy removal [118]. To apply Crystalbond 555, the carry wafer is heated to 80°C on a hot plate and a small amount of Crystalbond is applied by direct contact on to the wafer location where sample is too be bound, then the sample is carefully lowered onto that location while ensuring that all of the Crystalbond is covered. The Crystalbond manufacturers had not provided data on the vacuum suitability of the product but report that users had found the product suitable [118]. Figure 5.12 shows SEM images of Mie resonator structures produced using the crystal bond technique, smooth vertical sidewalls are seen to be produced.

In this work we were keen to investigate the effect of different feature heights as well as different period and diameter. The three heights targeted were 100, 150 and 200 nm.

A standard recipe used by the Nano Group at the University of Southampton was designed to yield an etch rate of approximately 1nm per second. In this study we adopted these standard parameters but carried out calibration exercises to ensure that the relatively shallow etches required could be accommodated. The standard ICP parameters are presented in Table 5-3.

Table 5-3 Nano Group standard ICP parameters.

SF_6 gas flow	25sccm
C_4F_8 gas flow	50 sccm
Ar gas flow	27 sccm
RF Power	50 W
Chamber pressure	15 mTorr
Chamber temperature	15 C˚

In order to calibrate the etch rate a series of etches were carried out under the standard conditions with etch times of 30 to 200 seconds (Figure 5.11).

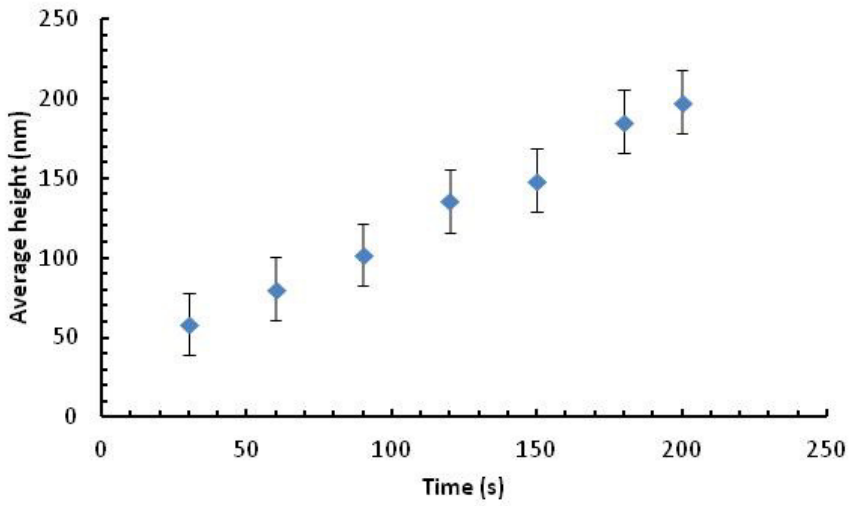


Figure 5.11. Diagram of average height aligned with dose level.

Figure 5.11 shows that for short etch times and shallow etches the etch rate is linear and that there is considerable variability in etch rate associated with plasma strike variations. As a result of these studies 90, 150 and 200 seconds were selected as suitable etch times for the 100, 150, and 200 nm heights required.

These are all rather short etches compared to typical Microelectro mechanical systems (MEMS)-like features that the ICP tool was typically used to produce so repeatability and control was an issue. In order to maximise reproducibility it was found necessary to precondition the ICP tool by cleaning the chamber and run the recipe once, without the sample, for 15 minutes.

I was very keen to be able to compare samples of different periods and diameters but exactly the same heights so the second important step was to etch all of the samples with the same target height at the same time. To achieve this all relevant samples (typically 7 samples in total) were attached to one carrier wafer. Figure 5.12 presents SEM images of features at each height along with a schematic diagram.

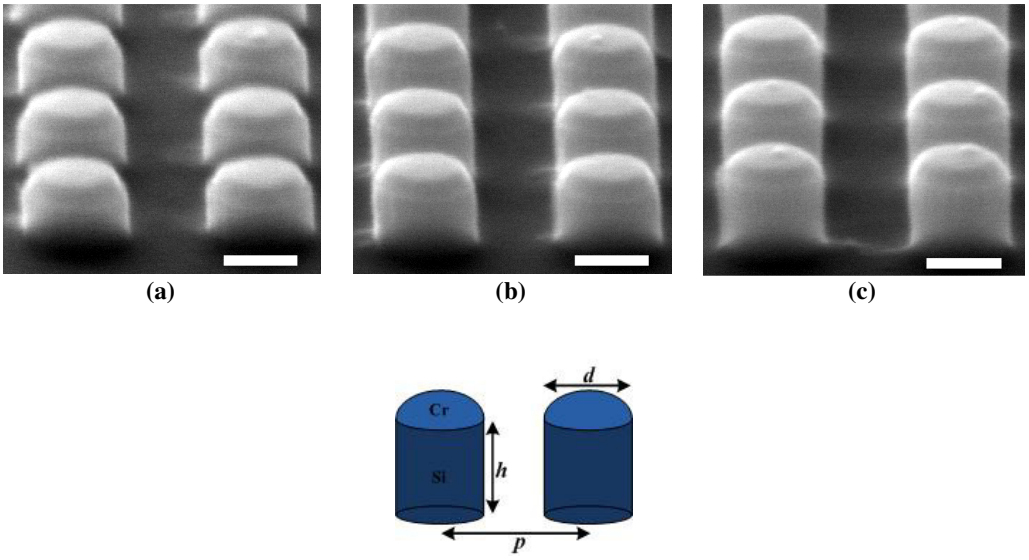


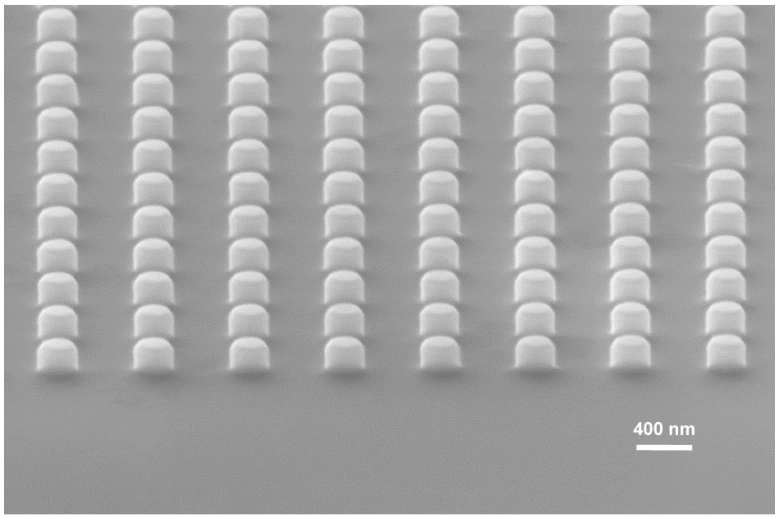
Figure 5.12. SEM images of samples etched in ICP for various heights: (a) 100nm, (b) 150 nm and (c) 200 nm scale bars are 200 nm. (d) A schematic diagram of features indicating key design parameters.

5.4.6. **Removal of Chromium**

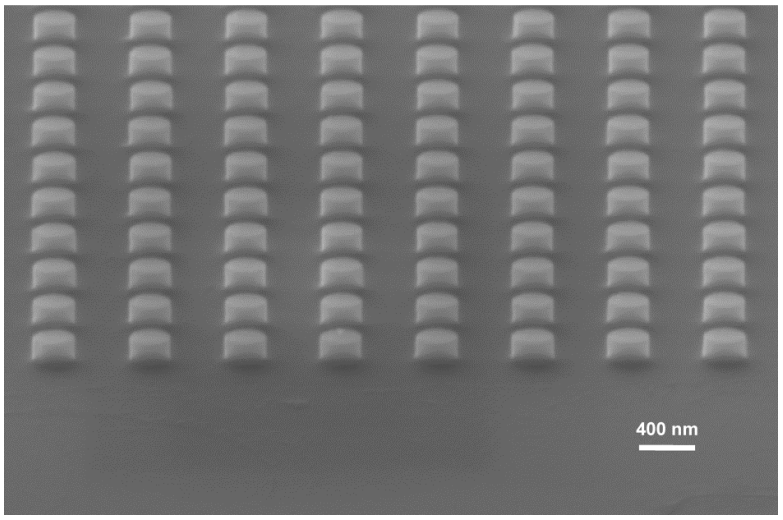
To remove the Chromium, a ready to use chromium etchant CR-7 from Cyanth Corporation [119] was used. Samples were immersed in CR-7 for 10 min then rinsed with DI water and dried using a N_2 gun.

5.5. Mie Scattering Fabrication Results

SEM images of fully formed patterns of Mie scattering arrays following removal of the Cr mask are shown in Figure 5.13.



(a)



(b)

Figure 5.13. SEM image of a typical Mie resonator arrays sample, (a) before Cr strip and (b) after Cr remove, scale bar is 200 nm.

Measurements of the feature dimensions were carried out on the SEM images. Table 5-4 presents measured values of diameter (d), period (p) and height (h), (see Figure 5.14 for an explanation of these dimensions).

Table 5-4 Designed and measured values of p, d and h. measured from SEM images of experimental samples all values are rounded to nearest 5nm to reflect experimental accuracy.

L-Edit Design Number	Sample Number	L-Edit		SEM Measurement (+/5 nm)		Average Height (+/5 nm) (targets were Set1=100 nm, Set2=150 nm and Set3=200 nm)		
		Periodicity (P)	Diameter (D)	Periodicity (p)	Diameter (D)	Set1	Set2	Set3
D1	S1	500	250	500	280	95	145	195
D2	S2	450	250	450	280	95	145	195
D2(b)	S3	450	250	450	300	95	145	195
D3	S4	450	225	450	250	95	145	195
D4	S5	400	200	400	220	95	145	195
D5	S6	500	150	500	200	95	145	195
D6	S7	500	125	500	125	95	145	195
D6(b)	S8	500	125	500	180	95	145	195
D7	S9	500	100	500	120	95	145	195
D7(b)	S10	500	100	500	140	95	145	195

Samples (b) replaced originals with 25% increased dose see text

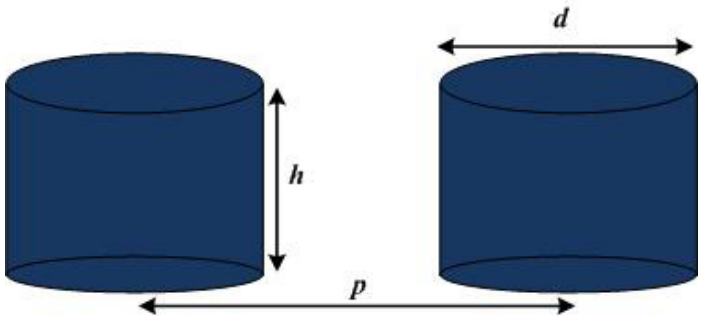


Figure 5.14. Diagram of Mie resonator arrays showing the diameter (d), period (p) and height (h) of array.

5.6. Optical Characterisations

My fabrication efforts were rewarded with a consistent set of 21 different 1cm x 1cm samples ready for optical characterisation by Integrating sphere and angular resolved spectroscopy systems (Table 5-5).

Table 5-5 Samples available for optical characterisation.

L-Edit Design Number	Samble Number	SEM Measurement (+/5 nm)		Average Height (+/5 nm)		
		Periodicity (p)	Diameter (D)	Set1	Set2	Set3
D1	S1	500	280	95	145	195
D2	S2	450	280	95	145	195
D4	S5	400	220	95	145	195
D5	S6	500	200	95	145	195
D6(b)	S8	500	180	95	145	195
D7	S9	500	120	95	145	195
D7(b)	S10	500	140	95	145	195

In addition to the set of Mie Resonator samples we obtained an antireflective silicon moth-eye sample with 400 nm feature height and a periodicity of 280 nm. This moth-eye sample was the best of many fabricated in an extensive study by Stuart Boden at Southampton University [46], although we believe slight improvements may be possible, it is the best moth-eye reported and an excellent benchmark sample to use in this work.

5.6.1. Integrating sphere measurements

The integrating sphere (IS) system (described in section 3.2.2) was used to measure the total hemispherical reflectance from all of 21 samples. Measurements were taken using p-polarized source and an angle of incidence of 8°. The results gained are presented and compared to equivalent measurements for uncoated flat silicon in Figure 5.15.

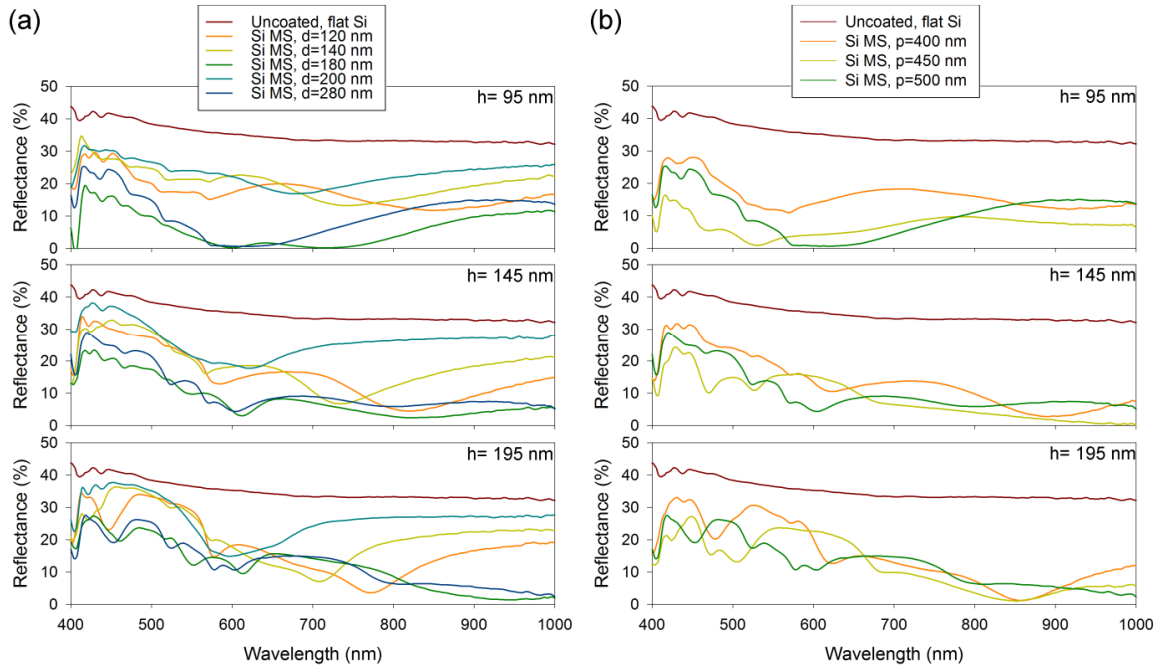


Figure 5.15. Hemispherical reflectance spectra from Si Mie resonator arrays with heights of 95 nm, 145 nm and 195 nm collected using the integrating sphere method. The spectrum for uncoated, flat silicon is also shown for comparison: (a) The period is 500 nm and the diameter is varied from 120- 280 nm; (b) p is varied from 400- 500 nm and the d/p ratio held at 0.55[120].

Figure 5.15 confirms that texturing a Si surface with Mie resonator arrays confers a significant AR effect for each of the designs. All samples show a reduction in reflectance when compared to the uncoated un-textured silicon surface. Visual analysis of the results suggest that the best performing samples are those with the shortest features (h=95 nm), though we can also see that the reflectance of longer wavelengths is reduced most for the tallest structures (h=195 nm).

It is clear that we might expect tuneable spectral features to appear as a result of Mie resonances within the features, as a result of diffraction (particularly at short wavelengths) and perhaps interference as a result of the two surfaces presented by the structure. The experimental data shows, often rather complex characteristics and it is challenging to separate out the different types of feature. A strong feature is observed to move with diameter for samples with feature height h=195 nm, but other than this most samples simply demonstrate broad minima in the visible wavelengths, though arguably all three samples with h=145 nm and the d/p ratio of 0.55 might exhibit minima at wavelength beyond the range studied here.

Trying to define 'the best' sample requires more than simple visual inspection of the graphs, it certainly requires a careful consideration of the application in mind. Our application is for photovoltaics, so, as with the inverted pyramid samples of chapter 4. We have sought to gain further insight into the suitability of Mie resonator arrays for photovoltaic applications by analysing their average reflectance, R_w, weighted to the AM1.5 solar spectrum. The weighted reflectance (R_w) was calculated using equation (5.1), where $PFD(\lambda)$ is the AM 1.5 solar spectrum in the form of photon flux density, in units of photons/m^2/s and $R(\lambda)$ the reflectance measured using the IS technique.

$$R_{\mathrm{W}} = \frac{\sum[R(\lambda)\times PFD(\lambda)]}{\sum(PFD(\lambda))} \qquad \textbf{(5.1)}$$

The results of this analysis (shown in Figure 5.16) reveal that the period, height and diameter of Mie resonator arrays can be tuned to achieve an antireflective effect that can exceed those of traditional optimised thin film antireflective coatings. Furthermore, the best Mie resonator sample in this measurement set (p=500 nm, d=180 nm, h=95 nm) exhibits an R_w of only 5.5%, outperforming even the silicon moth-eye structure which has an R_w=6.4%. This is further highlighted in the plot in Figure 4a, which compares the hemispherical reflectance spectra of thin film ARCs, the silicon moth-eye sample and the best Mie resonator array.

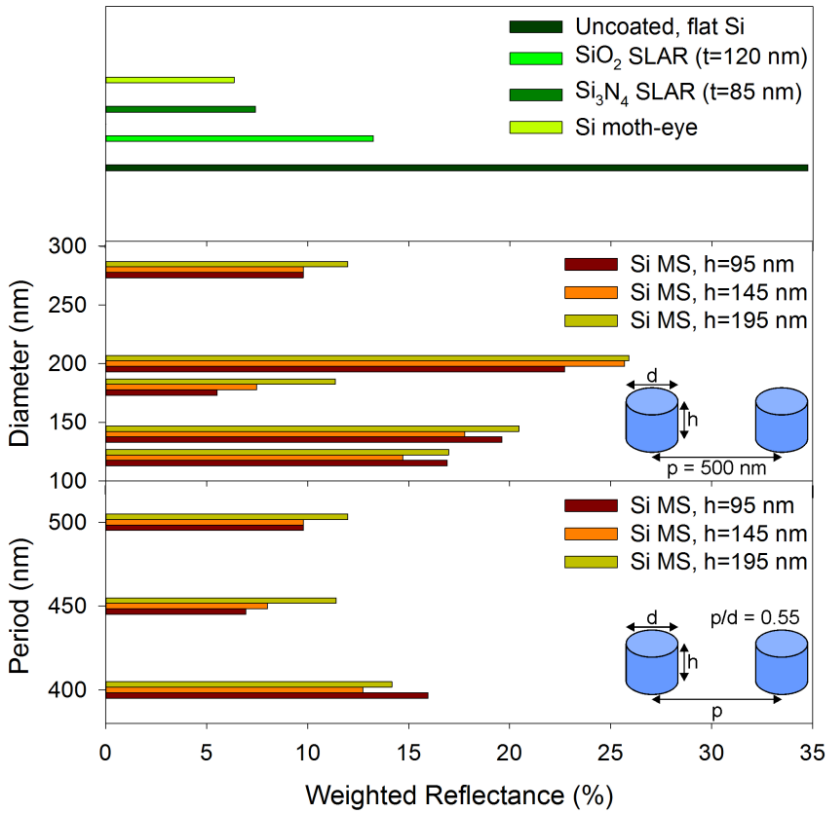


Figure 5.16. Weighted reflectance, R_w, of the silicon Mie resonators Mie resonator arrays calculated from the integrating sphere reflectance spectra shown in Figure 5.15. The R_w values of uncoated, flat silicon, two types of thin film single layer antireflective coating (SLAR), with optimum thicknesses, and the silicon moth-eye structure are included for comparison[120].

The SEM images of the two types of subwavelength antireflective (the moth-eye sample in Figure 5.17 (b) and the best Mie resonator arrays sample in Figure 5.17(c) illustrate that in addition to a lower reflectance the Mie resonator arrays benefit from a shorter feature height and a lower packing density. This is potentially advantageous when considering the relative ease of passivating the silicon surface to keep surface recombination low and also incorporating other layers into a PV device. This also adds to the potential for scaling the patterning to larger areas using nano-imprinting techniques, both in terms of the expense of producing the master stamp and also the ease of printing the pattern.

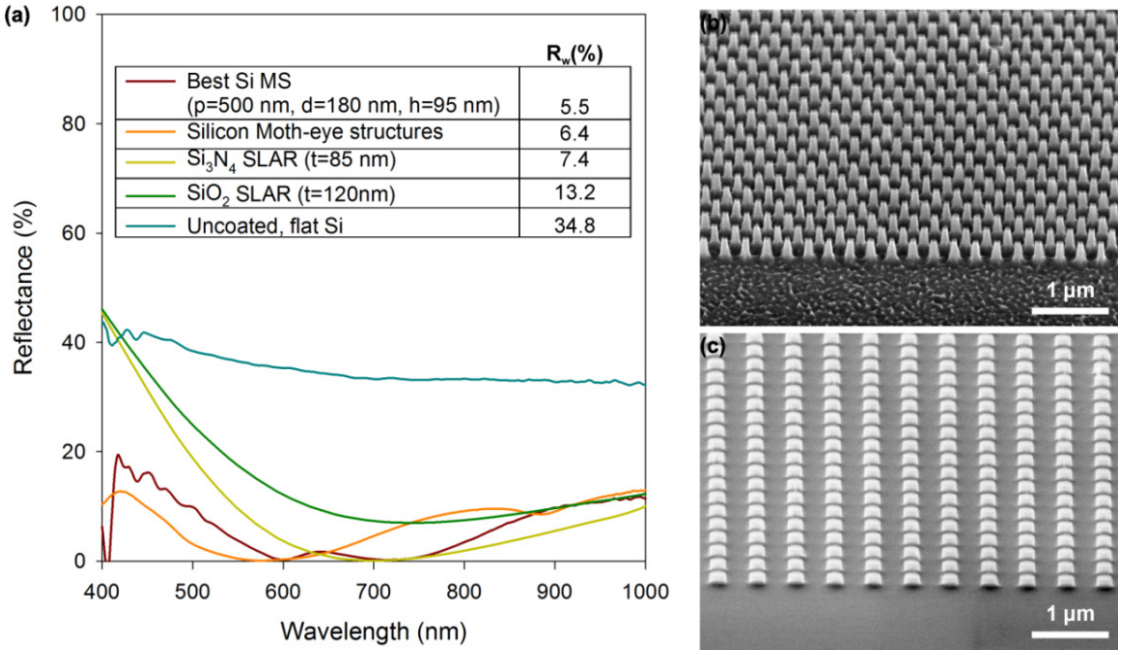


Figure 5.17. (a) Hemispherical reflectance spectra from integrating sphere method for the best performing Mie resonator arrays and a silicon moth-eye structure. The legend gives the calculated weighted reflectance (Rw). Spectra from optimised SLARs and uncoated flat silicon are included for comparison; (b) SEM image of silicon moth-eye sample; (c) SEM image of best performing Mie resonator sample[120].

5.6.2. **Angular Reflectance Spectroscopy**

Angular resolved specular reflectance spectra were collected using a custom built motorised θ-2θ angular reflectance spectroscopy (ARS) system (see section 3.2.3) from all of the samples, using s and p polarization over a wavelength range of 450–1000 nm and an angle of incidence range of 5-85°. Spectra for the average of s and p have been calculated from equation (5.2) where R_s and R_p are the measured reflectance spectra for s and p input polarization.

$$R_{average} = \frac{(R_s + R_p)}{2} \qquad (5.2)$$

The reflectance spectra for s and p polarization from (p=500 nm, d=180 nm, h=95 nm), for a range of angles of incidence, along with the average of s and p for same sample are presented in Figure 5.18.

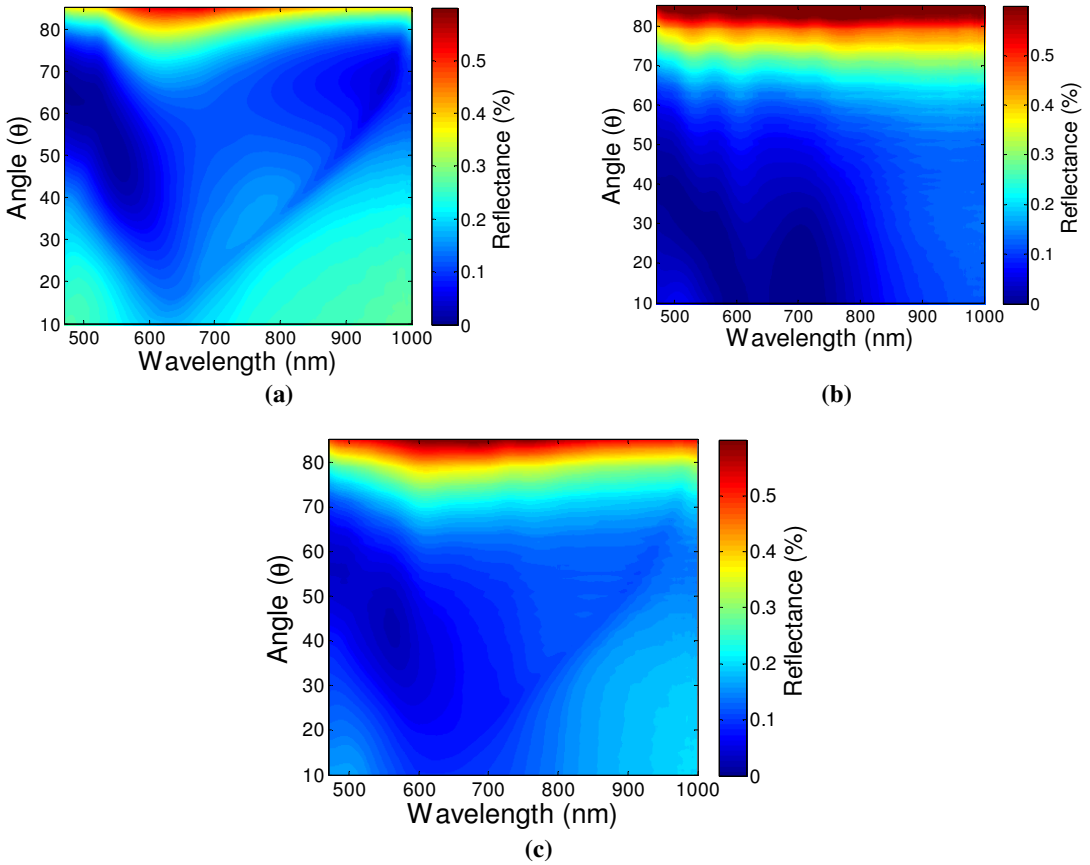


Figure 5.18. Reflectometer measurement results of Mie resonator arrays, sample (p=500 nm, d=180 nm, h=95 nm): (a) R_p input polarisation, (b), R_s input polarisation and (c) average of s and p polarisation.

A similar analysis to IS measurement can be performed on reflectance data from the angular reflectance spectroscopy (ARS) data collected on each of the fabricated samples to yield weighted reflectance values that take into account angular in addition to spectral variations throughout a day. It is important that antireflective surfaces for solar cells perform well for light over a wide range of incident angles as well as over a broad wavelength range because both angular and spectral illumination conditions vary considerably over the course of a day. Collecting data over a wavelength range of 470–1000 nm and an angle of incidence range of 5-85° enables a figure of merit termed the weighted specular reflectance (WSR) to be calculated. Firstly, R_w is calculated using (equation (5.3)), (see section 3.2.4) where $PFD\ (\lambda,\theta)$ is the AM 1.5 solar spectrum in the form of photon flux density, in units of photons/m^2/s and $R_{ave}\ (\lambda,\theta)$ is the

reflectance have been measured and calculated. The resulting WSR values are plotted in Figure 5.19.

$$R_W = \frac{\sum_{\lambda,\theta} R_{ave}(\lambda,\theta) \times PFD(\lambda,\theta)}{\sum_{\lambda,\theta} (PFD(\lambda,\theta))} \quad (5.3)$$

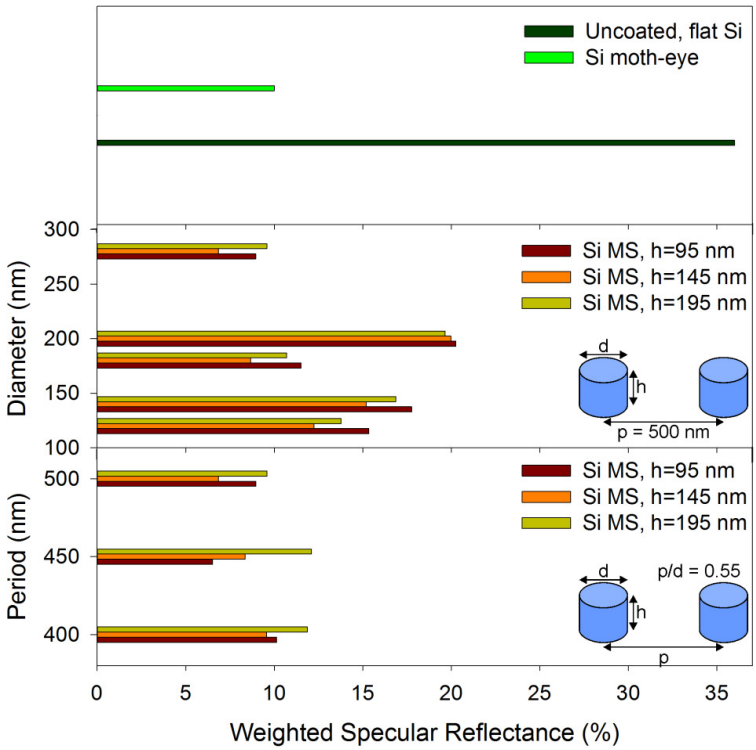


Figure 5.19. Weighted specular reflectance, WSR, of the silicon Mie resonator arrays calculated from angular reflectance spectroscopy method. The WSR values of uncoated, flat silicon and the silicon moth-eye structure are included for comparison[120].

The WSR data again demonstrates that the Mie resonator arrays structures with carefully specified dimensions can outperform the thin film SLARs and even the silicon moth-eye array. Interestingly, the best performing Mie resonator arrays sample when the full angular analysis is performed is not the same as the structure that produced the best R_w. The lowest WRS is exhibited by the sample with p=450 nm, d = 250 nm and h=95 nm, SEM images of which are presented in Figure 5.20. This gives a WRS of only

6.5% whereas the sample with the lowest R_w from the integrating sphere exhibits a relatively poor WRS of 11.5%. This indicates that it is important to characterize full angular and wavelength performance when developing optimum Mie resonator antireflective surfaces. For example, it is likely that in the case of a concentrator system where solar cells will experience only a limited angular variation in incident light throughout a day, the Mie resonator arrays with the best near-normal incidence AR performance (i.e. the sample with the lowest R_w, shown in Figure 5.20 should be used. For non-concentrator, non-tracking devices, the Mie resonator arrays that perform Mie resonator arrays best over the full angular range (i.e. the sample exhibiting the lowest WRS, shown in Figure 5.20) should be employed.

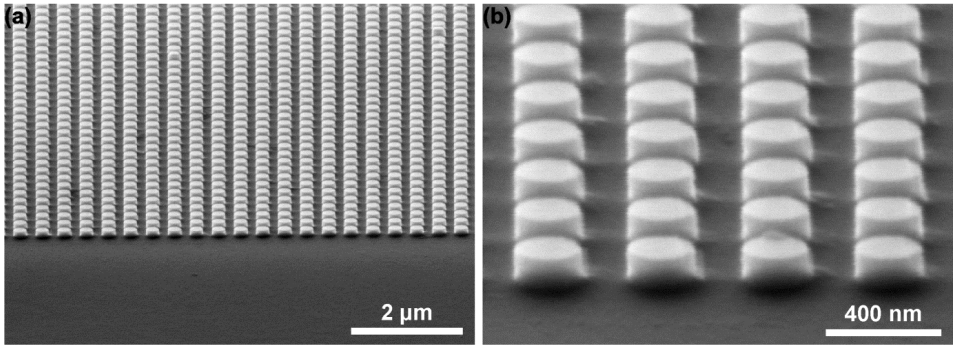


Figure 5.20. SEM images, taken at an angle of 54°, of the best performing (lowest WSR) silicon Mie resonator array based on angular reflectance spectroscopy (period = 450 nm, diameter= 250, height = 95 nm).

The performance of the Mie resonator arrays compared to the moth-eye sample is even more impressive when the full angular characteristics are considered, with the moth-eye sample giving a WSR of 10% compared to the 6.5% of the best Mie resonator. The ARS data from both types of subwavelength antireflective structure are displayed in Figure 5.21. The samples show contrasting behaviour, with the low reflectance region of the Mie resonator sample occurring in the angular range 20-40° and at short wavelengths whilst that of the moth-eye sample occurs at normal incidence. These characteristics are not presently fully understood but confirm fundamentally different AR mechanisms and behaviour for the two different subwavelength structures.

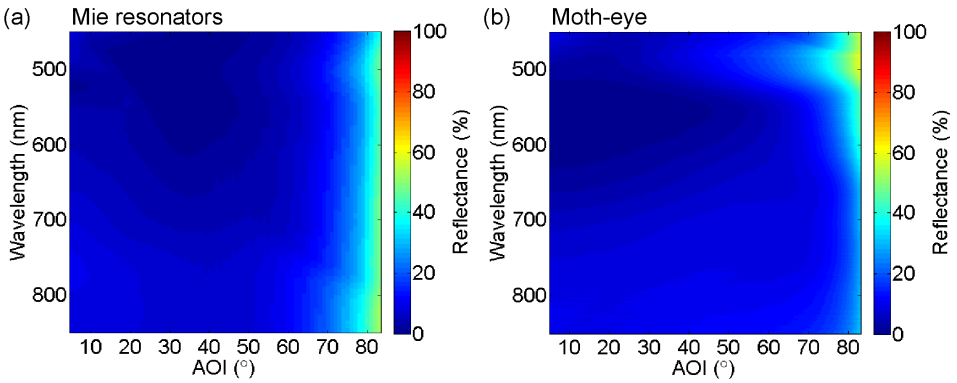
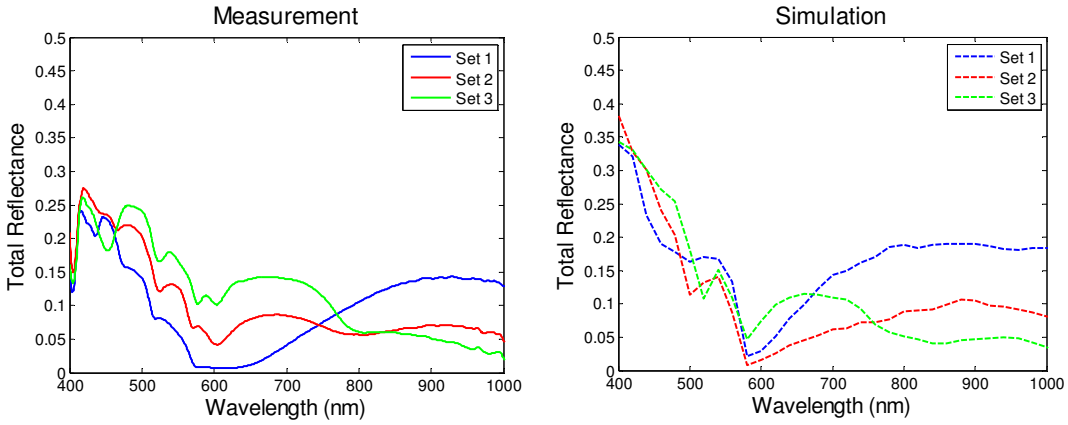


Figure 5.21. (a) Angular reflectance spectra (average of s and p incident polarisations) for (a) best performing silicon Mie resonator array, and (b) silicon moth-eye.

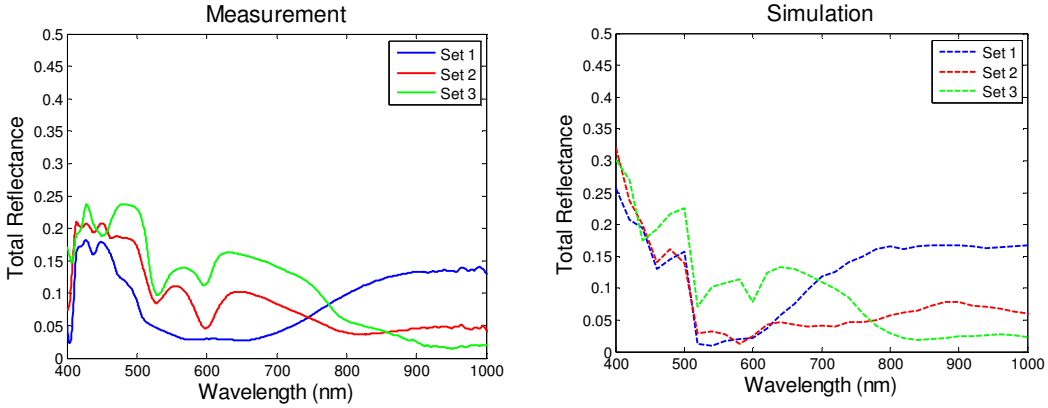
5.7. FDTD Simulation

FDTD has been used as described in section 3.11.2, this work has been conducted in collaboration with Dr David Payne who has, over a number of years acquired the skills required to model complex nanostructures using Lumerical and FDTD. This work is part of a paper in preparation [121].

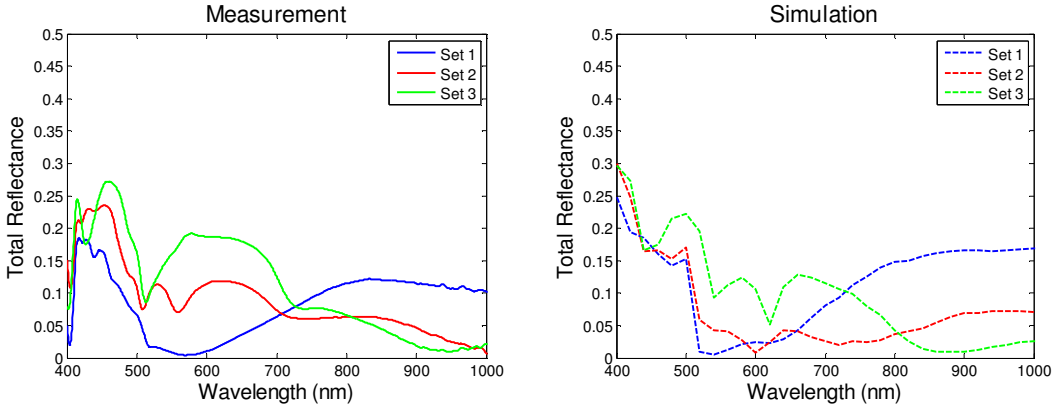
Figure 5.22 shows comparison between measurements and simulation results for sample designs S1, S2 and S3 for each of the three cylinder heights.



(a)



(b)



(c)

Figure 5.22. IS Measurements and simulation results for (a) S1 (P=500 nm, d=280 nm), (b) S2 (P=450 nm, d=280 nm, and (c) S3 (P=450 nm, d=300 nm). (Set 1=95 nm, Set2=145 nm and Set3=195 nm) [121].

Clearly a little more work is required, however the simulations show reasonable agreement for many of the samples. This to some extent validates the FDTD model that has been used. If this model is adjusted to match the best sample reported by Spinelli and Polman [105], (with a period of 450 nm, a height of 150 nm and diameter of 250 nm) 'the Polman design' and then we model absorption in a 1µm slab of silicon in

which the Polman design is on the front surface and a SiO_2 and silver back-reflector is on the rear, we find a 1.35x enhancment in the absoption when compared to a planar surface (Figure 5.23).

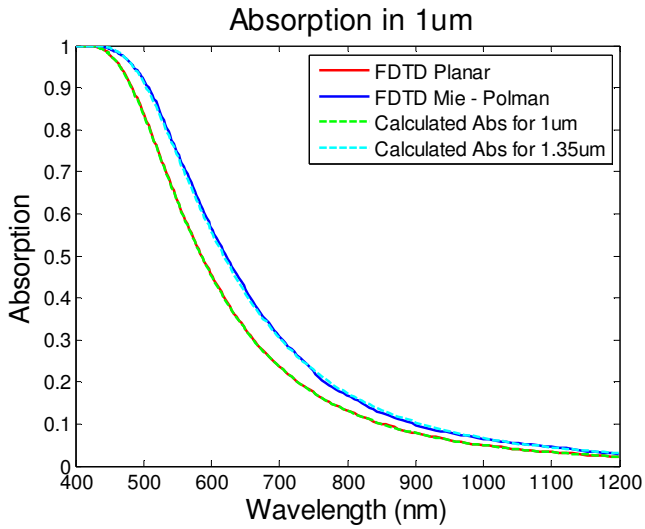


Figure 5.23. Evidence of light-trapping in a FDTD model of a 1µm silicon solar cell with the optimum design of Spinelli and Polman[105] optimum design (p= 450 nm, h= 150 nm and d=250 nm) [121].

This preliminary results clearly shows that the Mie resonator structure provides some light scatter and enhances the optical path length. While this is not a huge enhancement, this effect it is in addition to the anti-reflection enhancement, leading to a significant overall absorption enhancement.

5.8. Conclusions

Antireflective Mie resonator arrays have been fabricated in silicon substrates and their performance in reducing reflectance of the solar spectrum has been analysed and compared to the performance of a silicon moth-eye array. The results demonstrate that Mie resonators can confer effective AR to a silicon surface, the best of the structures are found to outperform silicon moth-eye structures, especially when the angular and spectral changes in incident sunlight over a day are taken into account. Furthermore, the performance of the Mie resonator arrays is shown to be highly dependent on the dimensions and spacing of the constituent pillars and that the optimum design is different when considering wavelength and incident angle changes over a day compared to simply considering the AM1.5 spectrum. Further investigation is required, both

experimentally and ideally through numerical modelling to optimize the design of these structures and implement them into a solar cell fabrication process in order to realise the full potential of this promising new antireflective method.

6.Silicon Grass (Black Silicon)

6.1. Introduction

Nanowires, formed by bottom-up vapour-liquid-solid (VLS) techniques [122] or by top-down etching techniques [123], can create antireflective (AR) structures by assisting multiple reflections between or within wires, or by inducing gradual changes of refractive index like moth-eye AR schemes[53]. Nanowires can also enhance absorption and modify bandgaps as a result of quantum confinement if the dimensions are small enough.

Within photovoltaics, nanowire solar cells and devices have received much attention over the last few years. Core-shell nanowires can form individual nanoscale solar cells [124], or be connected in arrays to form bulk-heterojunction solar cells [125]. Ordinary photovoltaic devices could use nanowires to improve AR or else enhance absorption, they can also be used to provide a textured substrate [126-128]. Use of nanowires for any of these applications has the potential to be rewarding but is also likely to be challenging; there will always be a level of disorder in any fabrication process that is not completely lithographic. Large aspect ratios will increase surface area and this is likely to increase surface recombination. Those large surface areas are also more likely to be harder to fully passivate and are more likely to contain impurities. Carriers generated within nanowires might be hard to extract unless the junction is contained within the wire. As a result there will always be mechanical uncertainty and challenges with conformality of subsequent growth.

In my research I am primarily interested in the AR properties of nanowires and their use as a textured substrate for thin film silicon solar cells[129]. In this chapter I describe the fabrication and characterisation of self-organised “silicon-grass” nanowires formed by reactive ion etching (RIE) in a process similar to that reported by Pezoldt *et al*, [130], which is based on the “Black Silicon Method” by Jansen et al [131].

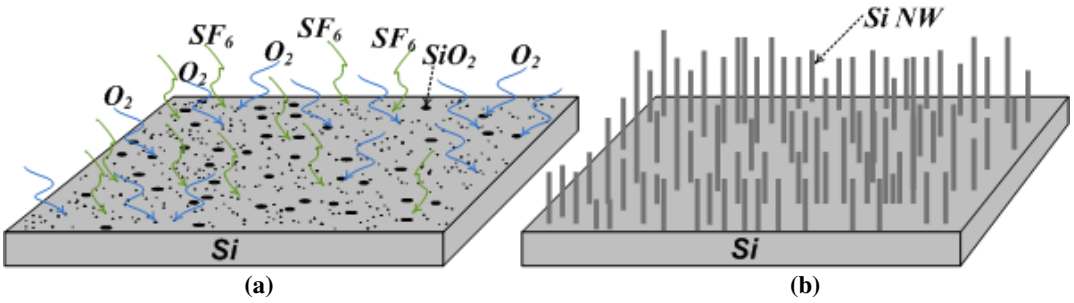


Figure 6.1. Schematic of the mechanism of formation of random wires by dry etching using SF_6/O_2. (a) Si substrate with native oxide on top at start of process and (b) formation after Ar treatment.

The nanoscale features form without the need for a lithographically defined mask and so the process is relatively cheap and scalable compared to other nanoscale texturing technologies. The formation of the wires is based on local and regenerating oxide masking. Initially the surface is covered with native oxide that forms a hard mask layer that is not removed homogeneously, but is perforated in regions where the oxide is thin. The relatively unmasked spots are etched and needle like structures are formed, depending on the degree of isotropy of the etch process (Figure 6.1). The directed ion bombardment in RIE, though, removes silicon as well as the adsorbed film. With the right choice of plasma parameters the regeneration of the adsorbed masking layer during the etch is just sufficient to maintain a kind of randomly perforated mask [132]. I describe the conditions for optimized nanowire formation and present reflection spectra at normal incidence, from which I extract an average reflectance, weighted to the AM 1.5 solar spectrum, as a figure of merit for AR performance under sunlight.

6.2. Sample Fabrication

2 cm×2 cm sections of a p-type silicon wafer were used as starting materials for the formation of nanowire textures. Following an RCA clean, the samples were loaded into the reactor chamber (STS LPX Pegasus de-coupled ASE ICP DRIE), details of which are described by Pezoldt *et al*, [130]. Mixed mode etching (etching and simultaneous passivation) proceeds with an SF_6/O_2 plasma whereby the etch time and the oxygen flow rate can be varied to control the resulting surface texture. Process parameters are shown in Table 6-1.

Table 6-1. Process parameters for fabrication of "silicon-grass" nanowires.

SF_6 gas flow	60 sccm
O_2 gas flow	85,95,105 sccm
Platen Power	50 W
Chamber pressure	15 mTorr
Chamber temperature	20 C˚
Process time	20,30,60 sec

6.3. Sample Characterization

Samples were cleaved to allow cross-sectional scanning electron microscopy (SEM) to be carried out. SEM was performed with a Carl Zeiss NVision40 FIB equipped with a Gemini Field Emission Scanning Electron Microscopy (FEGSEM) column. The beam energy was 20 keV. The samples were mounted vertically in the SEM and tilted by 10° so that the images were captured at 80° from the normal to the surface. The height of the nanowire features was obtained as an average of several measurements taken directly from the cross-sectional SEM images while accounting for the sample tilt.

The plasma etching process creates a dense array of high aspect ratio, vertically aligned nanowires, (Figure 6.2 and Figure 6.3) the height and density of which can be controlled by varying the etch time and O_2 flow rate [130, 131].

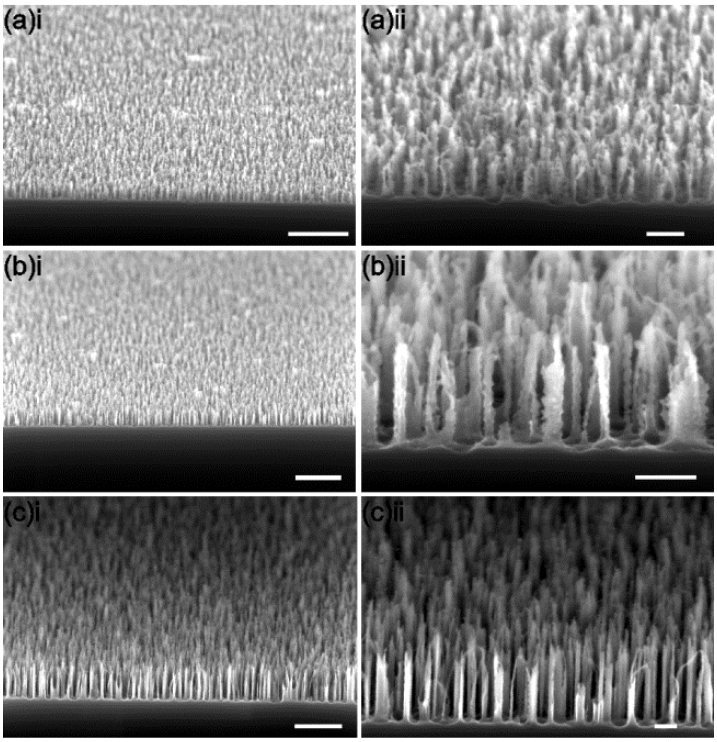


Figure 6.2. SEM images of textured silicon surfaces etched for the following times: (a) 20s (b) 30s and (c) 60 s. The oxygen flow rate was 85 sccm. The scale bars are (i) 2 µm and (ii) 400 nm.

The average height is proportional to the etching time (Figure 6.4). Increasing the oxygen flow rate increases the apparent density of the nanowires as seen using SEM (Figure 6.3), whilst decreasing the average height (Figure 6.4). It is clear from the plot in Figure 6.4 that the range of etch times selected had a larger effect on the average height than the range of O_2 flow rates tested.

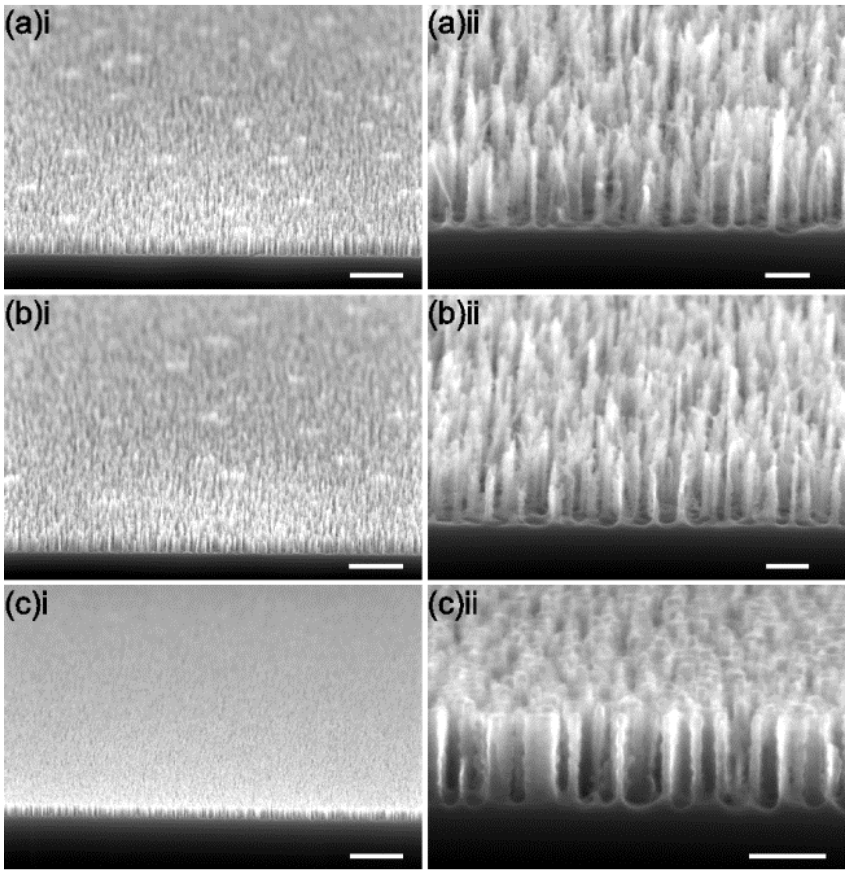


Figure 6.3. SEM images of textured silicon surfaces etched for 30 s, using an oxygen flow rate of (a) 80 sccm, (b) 95 sccm and (c) 105 sccm. The scale bars are (i) 2 µm and (ii) 400 nm.

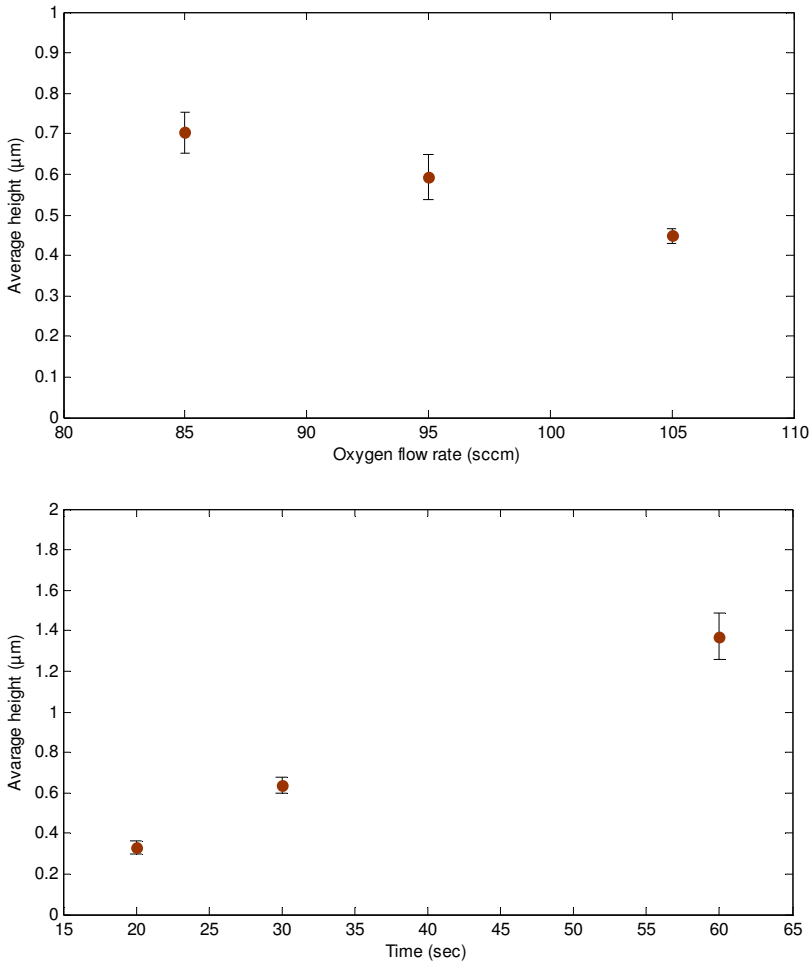


Figure 6.4. Plot of average nanowire height vs. oxygen flow rate and etch time.

6.4. Optical Characterisation

Spectral reflectance measurements demonstrate that all samples have an AR effect, with the reflectance decreasing with increased etch time (Figure 6.5) and oxygen flow rate (Figure 6.6).

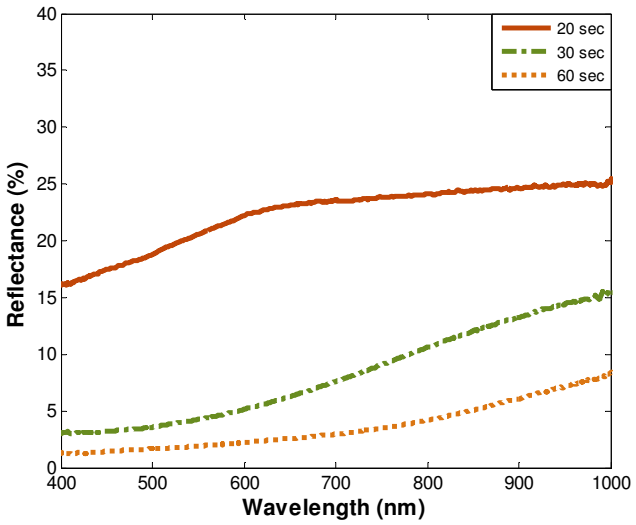


Figure 6.5. Reflectance probe measurements showing the reflectance spectra for textured silicon surfaces etched with an oxygen flow rate of 85 sccm for various times.

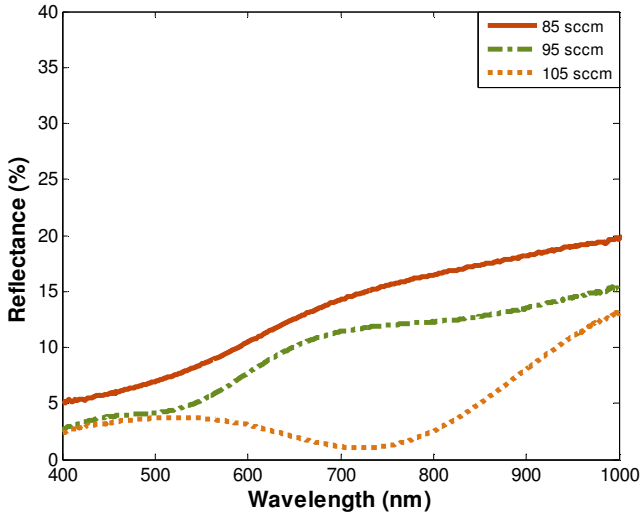


Figure 6.6. Reflectance probe measurement results showing the reflectance spectra for textured silicon surfaces etched for 30 s, and various oxygen flow rates.

To quantify this behaviour in terms of the texture applicability to PV, the average reflectance weighted to the AM1.5 solar spectrum (R_w) was calculated and plotted as a function of etch time and oxygen flow rate (Figure 6.7). As the etch time is increased,

the nanowire feature height increases, reducing reflectance by increasing the region over which the effective refractive index is graded. The same trend is not seen with O_2 flow rate where the height is seen to decrease but the reflectance also decreases. Here, the improved AR effect due to the increase in feature density appears to more than compensate for the decrease in height.

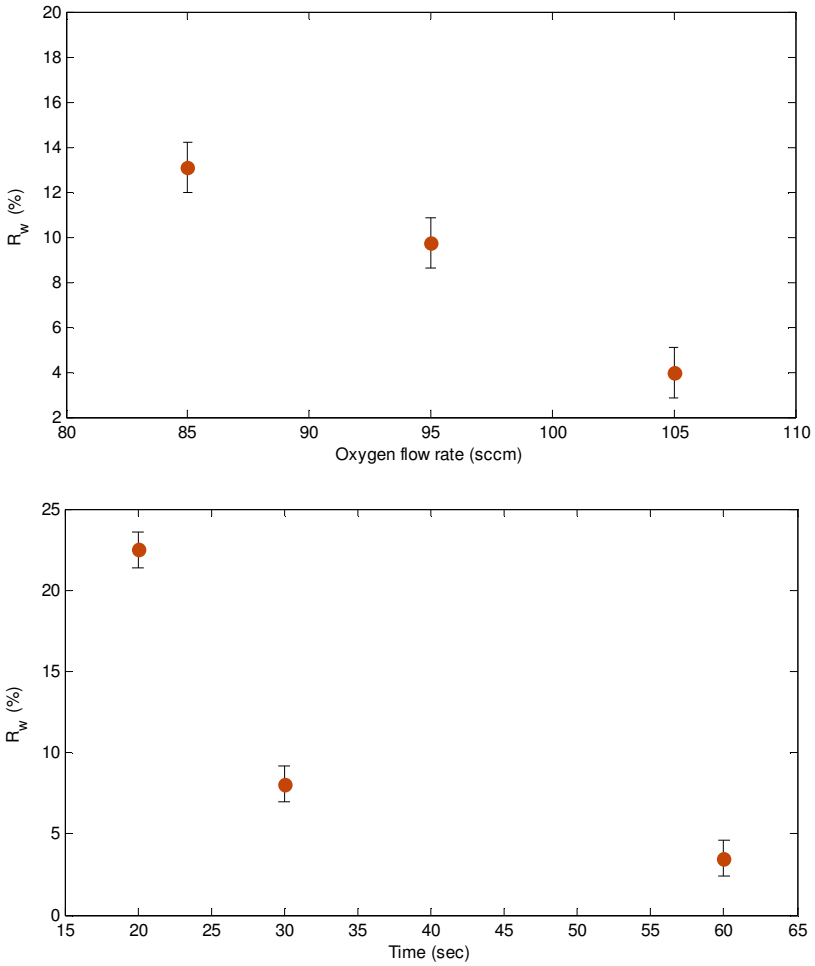


Figure 6.7. Average reflectance, weighted to the AM1.5 solar spectrum, as a function of etch time and oxygen flow rate.

6.5. Argon treatment

A 3 minute Ar plasma treatment can be used to modify the appearance of the nanowire features as seen in the before (a) and after (b) SEM images in Figure 6.8. The Ar treatment will smooth the side of the nanowires, resulting in tapered features. From an effective medium viewpoint, this step alters the effective refractive index profile from air to silicon. The measurements of specular reflectance over a range of wavelengths and angles of incidence (Figure 6.9) show that the AR performance improves after argon treatment as the tapering creates a graded index profile that is closer to optimum. The R vs. λ and θ maps clearly demonstrate the broadband nature of the AR effect and the wide angular range over which it operates compared to bare polished silicon. The weighted average reflectivities of the surfaces shown in Figure 6.8 are 0.13% ±0.08 (without Ar treatment) and 0.05%±0.02 (with Ar treatment).

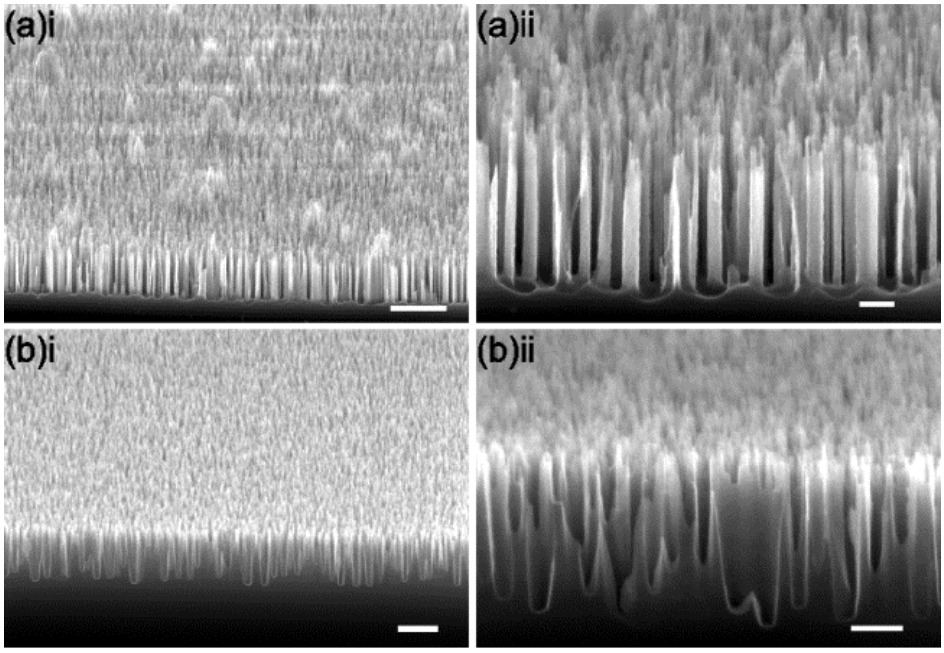


Figure 6.8. SEM images of textured silicon surfaces etched using an oxygen flow rate of 100 sccm for 2 mins; (a) without and (b) with a 3 minute Ar treatment. The scale bars are (i) 2 µm and (ii) 400 nm[129].

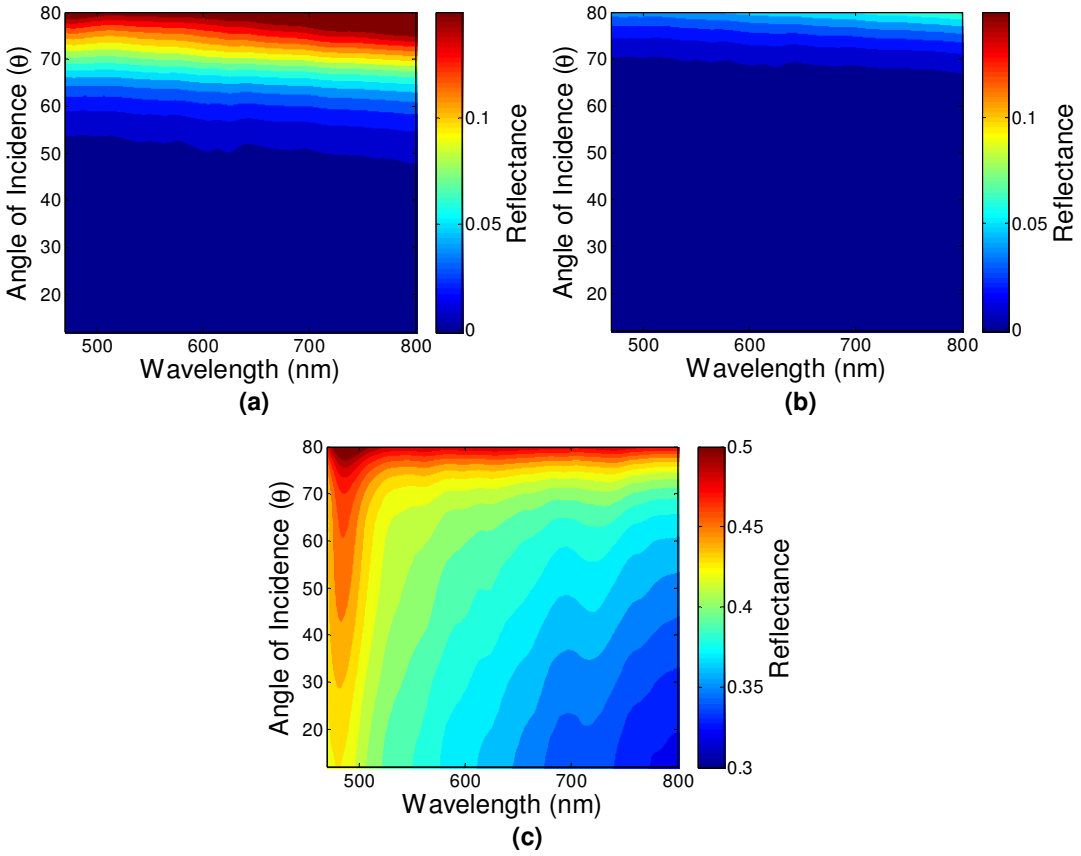


Figure 6.9. Measured specular reflectance as a function of wavelength and angle of incidence for the textured silicon samples shown in Figure 6.8, (a) without and (b) with a 3 minute Ar treatment. (c) Results from a bare polished silicon sample for comparison (note scale change)[129].

6.6. Conclusions

Highly effective nanowire-type AR surfaces were fabricated in silicon using a self-masking SF_6/O_2 dry etch process. The resulting structures were characterized by SEM, reflectance probe and angular dependent reflectometry. Reflectance decreased with both etch time and oxygen flow rate due to the morphological changes induced by varying these parameters. An argon plasma etch was employed to taper the nanowire features, resulting in a weighted average reflectance of only 0.05%.

Future work will include a full characterization of the specular and diffuse components of reflected light by wavelength and angle resolved spectroscopy (WARS).

7.Conclusions and Future Work

7.1. Conclusions

There are currently a large number of photovoltaic technologies under investigation; however devices based on silicon wafers (C-Si or MC-Si) are by far the dominant technology with only First Solar and their CdS/CdTe devices breaking the monopoly. Although there appear to be exciting new technologies emerging at regular intervals, most recently with the Perovskites for example, with ever-decreasing cost and the reality of grid-parity C-Si and MC-Si technologies look set to remain the dominant technologies for the foreseeable future.

At the same time, it is clear that efficient and low-cost photovoltaic systems must take proactive measures to reduce surface reflections or else squander up to 30% of the incident power. It is also clear that light-trapping is also an important feature of most high-efficiency devices, that can confer one or two percent to device efficiency especially for relatively thin devices.

A number of inexpensive antireflection schemes, including single-layer coatings, double-layer coatings, and micron-scale texturing can be utilised to reduce reflection losses to very acceptable levels, typically with weighted reflectance less than 10% and very low reflectance at the central spectral ranges. C-Si and MC-Si devices make use of highly effective micron-scale texturing schemes in conjunction with single-layer antireflective coatings, that not only significantly reduce reflection but also confer some light-trapping.

It seems unlikely that any new antireflection or light-trapping technology would replace these schemes in the near future, however, as the industry seeks to reduce costs technological progress will slowly but surely reduce material wastage and with time C-Si and MC-Si wafers are likely to become thinner and thinner. Eventually, when wafers are only a few 10's of microns thick the micron-scale textures will no longer be practical and light-trapping will become more important. At this point alternative antireflective and light-trapping schemes may be sought. This study has investigated 3 relatively novel surface texture schemes compatible with future thin wafer technologies and with the potential to both reduce reflection and enhance light-trapping.

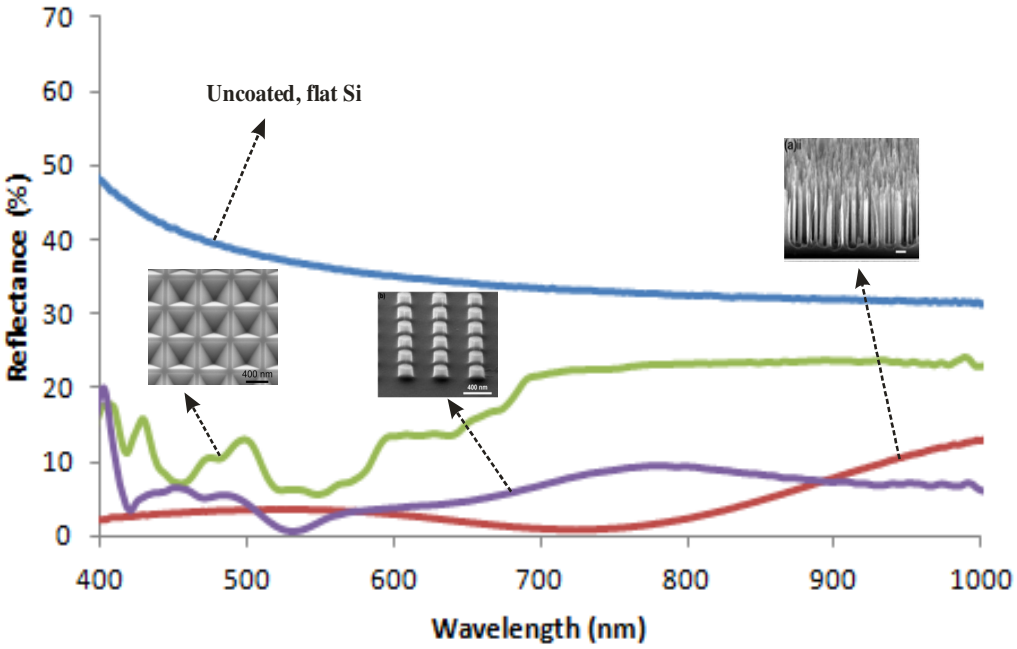


Figure 7.1. Reflectance spectra from nanoscale inverted pyramids , Si Mie resonator arrays , and nanowire structure arrays.

Reflectance spectra from the best example from each of the texture schemes investigated are presented in Figure 7.1.

I have found that nanoscale inverted pyramids can significantly reduce reflection, however, the effectiveness of the scheme has been found to be almost linearly dependent on feature size, with the smallest features fabricated (400nm periodicity) I found a relatively high weighted-reflectance (>22%) that could be reduced by around 10% with the addition of a single layer antireflective coating. My characterisation and RCWA simulations suggest that there is no design sweet-spot and that acceptable weighted-reflectance values might only be realised by increasing the periodicity and feature dimensions to at least 1 micron. There was no evidence that the use of sub-wavelength structures conferred any effect similar to the effective medium effects seen in the case of optimised moth-eye structures. Although we expect sub-wavelength inverted pyramids to confer some light-trapping benefits it is clear that the short-comings in reflectance reduction render the scheme fundamentally inappropriate, even if cheap fabrication methodologies could be found. Mainstream device technologies

would not move to thinner wafers if that led to a 10% increase in reflection and a corresponding loss in efficiency.

Mie resonator structures have been found to be a much more promising proposition. I have fabricated an excellent set of samples using a combination of e-beam lithography and reactive ion etching, and then used advanced characterisation capabilities in order to confirm that optimised Mie resonator structures can confer excellent antireflective effects with the best structures able to reduce the weighted reflectance to less than 7%. I have found that our best Mie Resonators outperform our best moth-eye structures. Samples produced in this work have been used to validate FDTD simulations that have already confirmed that Mie resonators can provide a light-trapping effect and a 35% enhancement in absorption. Conventional moth-eye structures cannot confer light-trapping and so it seems to me that Mie resonator structures are fundamentally better than moth-eye structures in terms of antireflection and light-trapping. At the same time, I note that the profile of the nanoscale moth-eye features are difficult to reproduce and the effectiveness of the structures are strongly dependent on profile whereas the Mie resonators are simple cylinders and much more readily produced and reproduced. Mie resonators could be a strong candidate system for future ultrathin photovoltaics, though further investigation is required on the light-trapping capabilities.

Finally, we have taken a look at a self-organised surface nanowire structure that can confer the most impressive antireflection effects. Nanowires have the potential to provide multiple external reflections and light-trapping, but add great complexity and significant surface area to devices. The approach also induces surface damage that will increase surface recombination. It is clear that it would be challenging to make good use of these nanowire structures in any kind of practical device, however it is also clear that the kind of surface I have demonstrated could be used in situations where the principle objective is to reduce glare from surfaces or minimise laser reflections in optoelectronics.

7.2. Further works

The most promising areas for future work would be in an extension of the Mie resonator investigations. The reflectance results I have obtained illustrate very complex spectral dependences on the diameter, height and periodicity of the structures. A much larger sample set and much more extensive use of FDTD would allow improved insight into the optical mechanisms at work and their key dependences, ought to be possible to determine optimal designs for a range of different antireflection applications. It should also be possible to carry out more extensive FDTD investigations into the light-trapping potential of these structures and optimise for both antireflection and light-trapping for specific devices and well defined spectral conditions. My studies have also focussed on silicon-only structures, further work might consider alternative dielectric materials and single layer (passivation) coatings within the Mie resonator framework. Ultimately, it is likely that Mie resonators might provide the best front surface antireflective and light-trapping structure, but ultimate light-trapping might require a second rear-surface structure, perhaps based on Mie or plasmonic scattering mechanisms, if this kind of double-texture scheme can be successfully demonstrated then the next challenge would be to demonstrate fabrication methodologies that can produce suitable structures at low cost and with high throughput and yield, such a demonstration could provide the opportunity for the photovoltaics industry to significantly reduce silicon usage while maintaining efficiency and thereby help to ensure that the cost of solar energy continues to decline and the benefits of cheap, low-carbon electricity generation can be felt by all members of the world community.

8.References

[1] IEA-PVPS.0. *A Snapshot of Global PV*. Available: http://www.iea-pvps.org/fileadmin/dam/public/report/technical/PVPS_report_-_A_Snapshot_of_Global_PV_-_1992-2014.pdf (2014, April).

[2] B. Burger.*Electricity production from solar and wind in Germany in 2013*. Available:http://www.ise.fraunhofer.de/en/downloads-englisch/pdf-files-englisch/news/electricity-production-from-solar-and-wind-in-germany-in-2013.pdf (2014, Jan).

[3] E. ProSun.*Export subsidies are illegal under WTO and EU rules*. Available:http://www.prosun.org/en/fair-competition/trade-distortions/subsidies.html, (04 April).

[4] J. Mayer.*Electricity Production and Spot-Prices in Germany 2014*. Available: http://www.ise.fraunhofer.de/en/downloads-englisch/pdf-files-englisch/data-nivc-/electricity-spot-prices-and-production-data-in-germany-2014.pdf, (2014, 04 April).

[5] *"EPIA Global Market for Photovoltiacs 2014-2018" http://www.epia.org/news/publications/ June 2014*.

[6] N. Reserch. *Annual Solar PV Installed Capacity and Revenue by Region, World Markets: 2011-2020*. Available: http://www.navigantresearch.com/wp-assets/uploads/2013/07/MD-SMF-13-Executive-Summary.pdf, (2013, 16 Jan).

[7] G. Munro.*Price of Solar Plummets-here's the proof* Available: http://efergy.com/blog/price-of-solar-plummets-heres-the-proof/#, (2013, April).

[8] V. F.T. Moore, 232, (1959), "Economies of Scale: some statistical Evidence," *Quarterly Journal of Economics,* vol. 73, p. 4, 1959.

[9] J. Ondraczek, "Are we there yet? Improving solar PV economics and power planning in developing countries: The case of Kenya," *Renewable & Sustainable Energy Reviews,* vol. 30, pp. 604-615, Feb 2014.

[10] M. A. Green, "Third generation photovoltaics: Ultra-high conversion efficiency at low cost," *Progress in Photovoltaics,* vol. 9, pp. 123-135, Mar-Apr 2001.

[11] A.Jäger-Waldau. *PV Status Report 2008*. Available: http://www.eurosfaire.prd.fr/7pc/doc/1299661785_lbna23604enc_001.pdf, (2008, 04 April).

[12] NREL. *Research Cell Efficiency Records*. Available: http://www.nrel.gov/ncpv/images/efficiency_chart.jpg, (2015, 05 April).

[13] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, "Solar cell efficiency tables (version 43)," *Progress in Photovoltaics,* vol. 22, pp. 1-9, Jan 2014.

[14] T. Markvart and L. Castañer. *Practical handbook of photovoltaics fundamentals and applications*. Available: http://www.sciencedirect.com/science/book/9781856173902, (2003).

[15] R. Szweda, *Gallium Arsenide, Electronics Materials and Devices. A Strategic Study of Markets, Technologies and Companies Worldwide 1999-2004*, 3 ed.: Elsevier, 2000.

[16] P. Jackson, D. Hariskos, E. Lotter, S. Paetel, R. Wuerz, R. Menner*, et al.*, "New world record efficiency for Cu(In,Ga)Se-2 thin-film solar cells beyond 20%," *Progress in Photovoltaics,* vol. 19, pp. 894-897, Nov 2011.

[17] (2012, 04 April). *Potovoltaics:Technologies, Cost, and performance*. Available: http://www1.eere.energy.gov/solar/pdfs/47927_chapter4.pdf

[18] Available: http://www.firstsolar.com/en/about-us, (April).
[19] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, "Solar cell efficiency tables (Version 45)," *Progress in Photovoltaics,* vol. 23, pp. 1-9, Jan 2015.
[20] M. A. Green, A. Ho-Baillie, and H. J. Snaith, "The emergence of perovskite solar cells," *Nature Photonics,* vol. 8, pp. 506-514, Jul 2014.
[21] A. Lochtefeld, L. Wang, M. Carroll, J. S. Han, D. Stryker, S. Bengtson*, et al.*, "15%, 20 Micron Thin, Silicon Solar Cells on Steel," *2013 Ieee 39th Photovoltaic Specialists Conference (Pvsc),* pp. 1364-1365, 2013.
[22] A. Einstein, "Concerning an Heuristic Point of View Toward the Emission and Transformation of Light," *American Journal of Physics,* vol. 33, March 1905 1905.
[23] W. S. a. H. J. Queisser, "Detailed Balance Limit of Efficiency of p-n Junction Solar Cells," *Journal of Applied Physics* vol. 32, p. 510, 1960 1960.
[24] G. L. Araujo and A. Marti, "Absolute Limiting Efficiencies for Photovoltaic Energy-Conversion," *Solar Energy Materials and Solar Cells,* vol. 33, pp. 213-240, Jun 1994.
[25] J. Nelson, *The Physics of Solar Cells*, illustrated, reprint ed. vol. 2: Imperial College Press, 2003.
[26] H. Mackel and A. Cuevas, "Determination of the surface recombination velocity of unpassivated silicon from spectral photo conductance measurements," *Proceedings of 3rd World Conference on Photovoltaic Energy Conversion, Vols a-C,* pp. 71-74, 2003.
[27] C. C. B. O. Kolbesen, L. Fabry, M. Bersani, D. Giubertoni, G. Pepponi, *Analytical Techniques for Semiconductor Materials and Process Characterization 6* The Electrochemical Society, 2009.
[28] M. D. Lammert and R. J. Schwartz, "Interdigitated Back Contact Solar-Cell - Silicon Solar-Cell for Use in Concentrated Sunlight," *Ieee Transactions on Electron Devices,* vol. 24, pp. 337-342, 1977.
[29] A. I. Lvovsky, "Fresnel Equations," in *Encyclopedia of Optical Engineering*, ed. Department of Physics and Astronomy, University of Calgary, Calgary, Alberta, Canada: Taylor & Francis 27 Feb 2013.
[30] E. Yablonovitch and G. D. Cody, "Intensity Enhancement in Textured Optical Sheets for Solar-Cells," *Ieee Transactions on Electron Devices,* vol. 29, pp. 300-305, 1982.
[31] E. Yablonovitch, "Statistical Ray Optics," *Journal of the Optical Society of America,* vol. 72, pp. 899-907, 1982.
[32] J. Zhao, A. Wang, F. Yun, G. Zhang, D. M. Roche, S. R. Wenham*, et al.*, "20,000 PERL silicon cells for the '1996 world solar challenge' solar car race," *Progress in Photovoltaics,* vol. 5, pp. 269-276, Jul-Aug 1997.
[33] J. Zhao, A. H. Wang, and M. A. Green, "24.5% efficiency PERT silicon solar cells on SEH MCZ substrates and cell performance on other SEH CZ and FZ substrates," *Solar Energy Materials and Solar Cells,* vol. 66, pp. 27-36, Feb 2001.
[34] J. G. Fossum, "Physical Operation of Back-Surface-Field Silicon Solar-Cells," *Ieee Transactions on Electron Devices,* vol. 24, pp. 322-325, 1977.
[35] A. W. Blakers, A. Wang, A. M. Milne, J. H. Zhao, and M. A. Green, "22.8-Percent Efficient Silicon Solar-Cell," *Applied Physics Letters,* vol. 55, pp. 1363-1365, Sep 25 1989.

[36] e. a. M. Taguchi, ". Improvement of the conversion efficiency of polycrystalline silicon thin film solar cell," presented at the Proceedings of the Fifth Photovoltaic and Solar Energy Conference, PVSEC, 1990.

[37] Y. Tsunomura, Y. Yoshimine, M. Taguchi, T. Baba, T. Kinoshita, H. Kanno*, et al.*, "Twenty-two percent efficiency HIT solar cell," *Solar Energy Materials and Solar Cells,* vol. 93, pp. 670-673, Jun 2009.

[38] C. M. Chong, S. R. Wenham, and M. A. Green, "High-Efficiency, Laser Grooved, Buried Contact Silicon Solar-Cells," *Applied Physics Letters,* vol. 52, pp. 407-409, Feb 1 1988.

[39] B. Dale, Rudenberg, HG, "High efficiency silicon solar cells," presented at the Proceedings of the 14th Annual Power Sources Conference, 1960.

[40] D. Jordan, Nagle, JP, "Buried contact concentrator solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 2, pp. 171-176, 1994.

[41] S. R. Wenham, C. B. Honsberg, and M. A. Green, "Buried Contact Silicon Solar-Cells," *Solar Energy Materials and Solar Cells,* vol. 34, pp. 101-110, Sep 1994.

[42] Z. J. Wang, P. Y. Han, H. Y. Lu, H. Q. Qian, L. P. Chen, Q. L. Meng*, et al.*, "Advanced PERC and PERL production cells with 20.3% record efficiency for standard commercial p-type silicon wafers," *Progress in Photovoltaics,* vol. 20, pp. 260-268, May 2012.

[43] B. S. Richards, "Comparison of TiO2 and Other Dielectric Coatings for Buriedcontact Solar Cells: a Review," *PROGRESS IN PHOTOVOLTAICS: RESEARCH AND APPLICATIONS,* vol. 12, pp. 253–281, 2004.

[44] D. M. Powell, M. T. Winkler, H. J. Choi, C. B. Simmons, D. B. Needleman, and T. Buonassisi, "Crystalline silicon photovoltaics: a cost analysis framework for determining technology pathways to reach baseload electricity costs," *Energy & Environmental Science,* vol. 5, pp. 5874-5883, Mar 2012.

[45] E. Yablonovitch, T. Tiedje, and H. Witzke, "Meaning of the Photo-Voltaic Band-Gap for Amorphous-Semiconductors," *Applied Physics Letters,* vol. 41, pp. 953-955, 1982.

[46] S. A. Boden, "Biomimetic Nanostructured Surfaces for Antireflection in Photovoltaics," Doctor of Philosophy, FACULTY OF PHYSICAL SCIENCE AND ENGINEERING,ECS, University of Southampton, 2009.

[47] T. L. Temple, "Optical properties of metal nanoparticles and their influence on silicon solar cells," Thesis (Ph D) - University of Southampton, School of Electronics and Computer Science, 2009, Original typescript,, 2009.

[48] S. A. Boden and D. M. Bagnall, "Sunrise to Sunset Optimization of Thin Film Antireflective Coatings for Encapsulated, Planar Silicon Solar Cells," *Progress in Photovoltaics,* vol. 17, pp. 241-252, Jun 2009.

[49] M. Green, "Slicon solar cells advanced principles and practice," *Center for photovoltaic devices and systems,* 1995.

[50] I. Virginia Semiconductor. *Wet-Chemical Etching and Cleaning of Silicon* Available: http://www.virginiasemi.com/pdf/siliconetchingandcleaning.pdf, (April 2015).

[51] S. R. W. a. M. A. G. P. Campbell, "LIGHT TRAPPING AND REFLECTION CONTROL WITH TILTED PYRAMIDS AND GROOVES," presented at the 20th IEEE Photovolt,1988.

[52] S. Beeby and N. White, *Energy Harvesting for Autonomous Systems*: Artech House, 2014.

[53] S. A. Boden and D. M. Bagnall, "Tunable reflection minima of nanostructured antireflective surfaces," *Applied Physics Letters,* vol. 93, Sep 29 2008.
[54] S. A. B. a. D. M. Bagnall, "Nanostructured biomimetic moth-eye arrays in silicon by nanoimprint lithography," *Proc. SPIE* vol. 7401, pp. 74010J–74010J–12, 2009.
[55] S. A. Boden and D. M. Bagnall, "Optimization of moth-eye antireflection schemes for silicon solar cells," *Progress in Photovoltaics,* vol. 18, pp. 195-203, May 2010.
[56] A. G. Aberle, "Thin-film solar cells," *Thin Solid Films,* vol. 517, pp. 4706-4710, Jul 1 2009.
[57] F. Jiao, Q. Y. Huang, W. C. Ren, W. Zhou, F. Y. Qi, Y. Z. Zheng*, et al.*, "Enhanced performance for solar cells with moth-eye structure fabricated by UV nanoimprint lithography," *Microelectronic Engineering,* vol. 103, pp. 126-130, Mar 2013.
[58] H. A. Atwater and A. Polman, "Plasmonics for improved photovoltaic devices (vol 9, pg 205, 2010)," *Nature Materials,* vol. 9, pp. 865-865, Oct 2010.
[59] T. L. Temple, G. D. K. Mahanama, H. S. Reehal, and D. M. Bagnall, "Influence of localized surface plasmon excitation in silver nanoparticles on the performance of silicon solar cells," *Solar Energy Materials and Solar Cells,* vol. 93, pp. 1978-1985, Nov 2009.
[60] R. S. A. Sesuraj, D. M. Bagnall, and H. S. a. M. Kondo, "Plasmon_enhanced Light-trapping in Microcrystalline silicon solar Cells," presented at the 6th World Conference on Photovoltaic Energy Conversion (WCPEC), Kyoto, Japan, 2014.
[61] T. L. Temple and D. M. Bagnall, "Broadband scattering of the solar spectrum by spherical metal nanoparticles," *Progress in Photovoltaics,* vol. 21, pp. 600-611, Jun 2013.
[62] T. L. Temple and D. M. Bagnall, "Optical properties of gold and aluminium nanoparticles for silicon solar cell applications," *Journal of Applied Physics,* vol. 109, Apr 15 2011.
[63] D. N. R. Payne, S. A. Boden, O. D. Clark, A. E. Delahoy, and D. M. Bagnall, "CHARACTERIZATION OF EXPERIMENTAL TEXTURED ZnO:Al FILMS FOR THIN FILM SOLAR CELL APPLICATIONS AND COMPARISON WITH COMMERCIAL AND PLASMONIC ALTERNATIVES," *35th Ieee Photovoltaic Specialists Conference,* pp. 1560-1564, 2010.
[64] M. Scherer, "Magnetron sputter-deposition on atom layer scale," *Vakuum in Forschung und Praxis,* vol. 21, p. 6, 2009.
[65] S. Pearce, "Leybold Helios Pro XL Sputterer DV05 Work Instructions," in *Work Instruction*, ed. Unvirsity Of Southampton: Nano Fabrication center 2012.
[66] D. N. R. Payne, "The Characterization and Enhancement of Light Scattering for Thin Solar Cells," Doctor of Philosophy Prf Darren M. Bagnall, University of Southampton, FACULTY OF PHYSICAL SCIENCES AND ENGINEERING, ECS, 2014.
[67] J. C. Gerbedoen, A. Aliane, A. Giguere, D. Drouin, R. Ares, and V. Aimez, "All evaporation submicron lift-off lithography process with negative e-beam QSR-5 resist," *Microelectronic Engineering,* vol. 103, pp. 123-125, Mar 2013.
[68] H. Jansen, H. Gardeniers, M. deBoer, M. Elwenspoek, and J. Fluitman, "A survey on the reactive ion etching of silicon in microtechnology," *Journal of Micromechanics and Microengineering,* vol. 6, pp. 14-28, Mar 1996.

[69] J. P. Cotter, I. Zeimpekis, M. Kraft, and E. A. Hinds, "Improved surface quality of anisotropically etched silicon {111} planes for mm-scale optics," *Journal of Micromechanics and Microengineering,* vol. 23, Nov 2013.

[70] M. D. Henry, "ICP ETCHING OF SILCON FOR MICRO AND NANOSCALE DEVICES " PhD, CALIFORNIA INSTITUE OF TECHNOLOGY 2010.

[71] S. A. B. A. Asadollahbaik, M. D. B. Charlton, D. N. R. Payne, S. Cox, and D. M. Bagnall, "Reflectance properties of silicon moth-eyes in response to variations in angle of incidence, polarisation and azimuth orientation," *Opt. Express,* vol. 22, p. A402, 2014.

[72] M. F. A. Muttalib, S. Z. Oo, and M. D. B. Charlton, "Experimental measurement of photonic/plasmonic crystal dispersion, applied to the investigation of surface Plasmon dispersion for SERS sensing applications," *Integrated Optics: Devices, Materials, and Technologies Xvi,* vol. 8264, 2012.

[73] I. B&WTEK. *Glacier X , spectrometerBTC112E* Available: http://bwtek.com/products/glacier-x/, (April, 2015).

[74] R. E. B. a. C. J. Riordan. (1986) Simple Solar Spectral Model for Direct and Diffuse Irradiance on Horizontal and Tilted Planes at the Earth's Surface for CloudlessAtmospheres.
Available:http://rredc.nrel.gov/solar/pubs/spectral/model/, (April, 2015).

[75] L. A. A. Pettersson, L. S. Roman, and O. Inganas, "Modeling photocurrent action spectra of photovoltaic devices based on organic thin films," *Journal of Applied Physics,* vol. 86, pp. 487-496, Jul 1 1999.

[76] M. Shtein, P. Peumans, J. B. Benziger, and S. R. Forrest, "Micropatterning of small molecular weight organic semiconductor thin films using organic vapor phase deposition," *Journal of Applied Physics,* vol. 93, pp. 4005-4016, Apr 1 2003.

[77] A. W. Smith and A. Rohatgi, "Ray Tracing Analysis of the Inverted Pyramid Texturing Geometry for High-Efficiency Silicon Solar-Cells," *Solar Energy Materials and Solar Cells,* vol. 29, pp. 37-49, Feb 1993.

[78] K. C. J. GD-Calc.. Available: http://software.kjinnovation.com/, (April, 2015)

[79] T. Weiss, N. A. Gippius, S. G. Tikhodeev, G. Granet, and H. Giessen, "Efficient calculation of the optical properties of stacked metamaterials with a Fourier modal method," *Journal of Optics a-Pure and Applied Optics,* vol. 11, Nov 2009.

[80] A. Taflove, "Application of the Finite-Difference Time-Domain Method to Sinusoidal Steady-State Electromagnetic-Penetration Problems," *Ieee Transactions on Electromagnetic Compatibility,* vol. 22, pp. 191-202, 1980.

[81] K. Yee, "Numerical solution of initial boundary value problems involving Maxwell's equations in isotropic media," *IEEE Transactions on Antennas and Propagation,* vol. 14, p. 6, 1966.

[82] R. M. Yang Hao, *FDTD Modeling of Metamaterials: theory and application*, illustrated ed.: Artech House, 2008.

[83] S. C. Baker-Finch and K. R. McIntosh, "Reflection of normally incident light from silicon solar cells with pyramidal texture," *Progress in Photovoltaics,* vol. 19, pp. 406-416, Jun 2011.

[84] M. A. Green, "The Path to 25% Silicon Solar Cell Efficiency: History of Silicon Cell Evolution," *Progress in Photovoltaics,* vol. 17, pp. 183-189, May 2009.

[85] J. M. Shim, H. W. Lee, K. Y. Cho, J. K. Seo, J. S. Kim, E. J. Lee*, et al.*, "17.6% Conversion Efficiency Multicrystalline Silicon Solar Cells Using the Reactive Ion Etching with the Damage Removal Etching," *International Journal of Photoenergy,* 2012.

[86] C. H. Sun, W. L. Min, N. C. Linn, P. Jiang, and B. Jiang, "Templated fabrication of large area subwavelength antireflection gratings on silicon," *Applied Physics Letters,* vol. 91, Dec 3 2007.

[87] A. Mavrokefalos, S. E. Han, S. Yerci, M. S. Branham, and G. Chen, "Efficient Light Trapping in Inverted Nanopyramid Thin Crystalline Silicon Membranes for Solar Cell Applications," *Nano Letters,* vol. 12, pp. 2792-2796, Jun 2012.

[88] M. S. Branham, W. C. Hsu, S. Yerci, J. Loomis, S. V. Boriskina, B. R. Hoard*, et al.*, "15.7% Efficient 10-mu m-Thick Crystalline Silicon Solar Cells Using Periodic Nanostructures," *Advanced Materials,* vol. 27, pp. 2182-+, Apr 1 2015.

[89] H. Sai, T. Matsui, K. Saito, and M. K. a. I. Yoshida, "Photocurrent enhancement in thin-film silicon solar cells by combination of anti-reflective sub-wavelength structures and light-trapping textures," *PROGRESS IN PHOTOVOLTAICS: RESEARCH AND APPLICATIONS,* vol. 23, 2015.

[90] S. Sivasubramaniam and M. M. Alkaisi, "Inverted nanopyramid texturing for silicon solar cells using interference lithography," *Microelectronic Engineering,* vol. 119, pp. 146-150, May 1 2014.

[91] W. Kern, "The Evolution of Silicon-Wafer Cleaning Technology," *Journal of the Electrochemical Society,* vol. 137, pp. 1887-1892, Jun 1990.

[92] H. Mishima, T. Yasui, T. Mizuniwa, M. Abe, and T. Ohmi, "Particle-Free Wafer Cleaning and Drying Technology," *Ieee Transactions on Semiconductor Manufacturing,* vol. 2, pp. 69-75, Aug 1989.

[93] M. Itano, F. W. Kern, M. Miyashita, and T. Ohmi, "Particle Removal from Silicon-Wafer Surface in Wet Cleaning Process," *Ieee Transactions on Semiconductor Manufacturing,* vol. 6, pp. 258-267, Aug 1993.

[94] R. T. Bhatt and A. R. Palczer, "Effects of thermal cycling on thermal expansion and mechanical properties of SiC fibre-reinforced reaction-bonded Si3N4 composites," *Journal of Materials Science,* vol. 32, pp. 1039-1047, Feb 15 1997.

[95] ZEON,CO. (2003). *ZEP520A*. Available: http://www.nanophys.kth.se/nanophys/facilities/nfl/resists/zep520a-7-2.pdf

[96] G. F. Iriarte, J. G. Rodriguez-Madrid, and F. Calle, "Fabrication of sub-100 nm IDT SAW devices on insulating, semiconducting and conductive substrates," *Journal of Materials Processing Technology,* vol. 212, pp. 707-712, Mar 2012.

[97] K. Sato, M. Shikida, Y. Matsushima, T. Yamashiro, K. Asaumi, Y. Iriye*, et al.*, "Characterization of anisotropic etching properties of single-crystal silicon: Effects of KOH concentration on etching profiles," *Mems 97, Proceedings - Ieee the Tenth Annual International Workshop on Micro Electro Mechanical Systems,* pp. 406-411, 1997.

[98] D. N. Payne, "unpublished work".

[99] J. Zhao and M. A. Green, "Optimized Antireflection Coatings for High-Efficiency Silicon Solar-Cells," *Ieee Transactions on Electron Devices,* vol. 38, pp. 1925-1934, Aug 1991.

[100] P. C. a. M. A. Green, "Light trapping properties of pyramidally textured surfaces," *J. Appl. Phys,* vol. 62, p. 243, 1987.

[101] J. Zhao, A. Wang, P. Altermatt, and M. A. Green, "24 Percent Efficient Silicon Solar-Cells with Double-Layer Antireflection Coatings and Reduced Resistance Loss," *Applied Physics Letters,* vol. 66, pp. 3636-3638, Jun 26 1995.
[102] C. G. Bernhard, "Structural and functional adaption in a visual system," *Endeavour,* vol. 26, pp. 79–84, 1967.
[103] Y. Kanamori, M. Sasaki, and K. Hane, "Broadband antireflection gratings fabricated upon silicon substrates," *Optics Letters,* vol. 24, pp. 1422-1424, Oct 15 1999.
[104] K. Hadobas, S. Kirsch, A. Carl, M. Acet, and E. F. Wassermann, "Reflection properties of nanostructure-arrayed silicon surfaces," *Nanotechnology,* vol. 11, pp. 161-164, Sep 2000.
[105] P. Spinelli, M. A. Verschuuren, and A. Polman, "Broadband omnidirectional antireflection coating based on subwavelength surface Mie resonators," *Nature Communications,* vol. 3, Feb 2012.
[106] F. J. Bezares, J. P. Long, O. J. Glembocki, J. P. Guo, R. W. Rendell, R. Kasica, *et al.*, "Mie resonance-enhanced light absorption in periodic silicon nanopillar arrays," *Optics Express,* vol. 21, pp. 27587-27601, Nov 18 2013.
[107] C. F. Bohren and D. R. Huffman, *Absorption and scattering of light by small particles*: Wiley, 1983.
[108] J. S. Bouillard, S. Vilain, W. Dickson, G. A. Wurtz, and A. V. Zayats, "Broadband and broadangle SPP antennas based on plasmonic crystals with linear chirp," *Scientific Reports,* vol. 2, Nov 20 2012.
[109] S. Asano and G. Yamamoto, "Light-Scattering by a Spheroidal Particle," *Applied Optics,* vol. 14, pp. 29-49, 1975.
[110] E. M. Purcell and Pennypac.Cr, "Scattering and Absorption of Light by Nonspherical Dielectric Grains," *Astrophysical Journal,* vol. 186, pp. 705-714, 1973.
[111] B. T. Draine and P. J. Flatau, "Discrete-Dipole Approximation for Scattering Calculations," *Journal of the Optical Society of America a-Optics Image Science and Vision,* vol. 11, pp. 1491-1499, Apr 1994.
[112] Z. Cui, *Nanofabrication: Principels, Capabilities and Limits*: Springer, 2009.
[113] M. Hatzakis, "Pmma Co-Polymers as High-Sensitivity Electron Resists," *Journal of Vacuum Science & Technology,* vol. 16, pp. 1984-1988, 1979.
[114] H. J. Levinson and M. A. McCord, *Handbook of Microlithography, Micromachining, and Microfabrication* vol. 1: Hardcover 1997.
[115] u. w. Yudong Wang.
[116] U. Peter Ayliffe.
[117] R. S. A. Sesuraj, "Plasmonic Mirror for Light-trapping inThin Film Solar Cells," Doctor of Philosophy, FACULTY OF PHYSICAL AND APPLIED SCIENCES,ECS, UNIVERSITY OF SOUTHAMPTON, 2014.
[118] http://www.crystalbond.com/. (April, 2015).
[119] K. R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing - Part II," *Journal of Microelectromechanical Systems,* vol. 12, pp. 761-778, Dec 2003.
[120] M. Banakar, S. A. Boden, A. Asadollahbaik, D. N. R. Payne, and D. M. Bagnall, "Angle-Resolved Reflection Spectroscopy of Sub-Wavelength Surface Mie Resonators," presented at the In Solar14: 52nd annual Australian Solar Council Industry Conference & Exhibition, , Melbourne, AU, 2014.
[121] M. Banakar, D. Payne, and D. M. Bagnall, " Work in preparation," 2015.

[122] R. S. W. a. W. C. Ellis, "VAPOR-LIQUID MECHANISM OF SINGLE CRYSTAL GROWTH," *Appl. Phys. Lett,* vol. 4, p. 89, 1964.
[123] K. J. Morton, G. Nieberg, S. F. Bai, and S. Y. Chou, "Wafer-scale patterning of sub-40 nm diameter and high aspect ratio (> 50 : 1) silicon pillar arrays by nanoimprint and etching," *Nanotechnology,* vol. 19, Aug 27 2008.
[124] M. M. Adachi, M. P. Anantram, and K. S. Karim, "Core-shell silicon nanowire solar cells," *Scientific Reports,* vol. 3, Mar 26 2013.
[125] M. D. Kelzenberg, S. W. Boettcher, J. A. Petykiewicz, D. B. Turner-Evans, M. C. Putnam, E. L. Warren*, et al.*, "Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications," *Nature Materials,* vol. 9, pp. 239-244, Mar 2010.
[126] B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu*, et al.*, "Coaxial silicon nanowires as solar cells and nanoelectronic power sources," *Nature,* vol. 449, pp. 885-U8, Oct 18 2007.
[127] M. D. Kelzenberg, D. B. Turner-Evans, B. M. Kayes, M. A. Filler, M. C. Putnam, N. S. Lewis*, et al.*, "Photovoltaic measurements in single-nanowire silicon solar cells," *Nano Letters,* vol. 8, pp. 710-714, Feb 2008.
[128] L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, and J. Rand, "Silicon nanowire solar cells," *Applied Physics Letters,* vol. 91, Dec 3 2007.
[129] M. Banakar, S. Aghdaei, S. A. Boden, I. Sari, and N. u. T. D. M. BagnallSilicon nanowires by self-organised reactive ion etching. In 8th Photovoltaic Science Applications and Technology Conference, GB, 02 - 04 Apr 2012, "Silicon nanowires by self-organised reactive ion etching," presented at the In 8th Photovoltaic Science Applications and Technology Conference

Newcastle upon Tyne, GB, Apr 2012.
[130] T. K. J. Pezoldt, M. Stubenrauch, and M. Fischer, "Black luminescent silicon," *Physica Status Solidi (C),* vol. 8, pp. 1021-1026, 2011.
[131] H. Jansen, M. Deboer, J. Burger, R. Legtenberg, and M. Elwenspoek, "The Black Silicon Method .2. The Effect of Mask Material and Loading on the Reactive Ion Etching of Deep Silicon Trenches," *Microelectronic Engineering,* vol. 27, pp. 475-480, Feb 1995.
[132] M. Schnell, R. Ludemann, and S. Schaefer, "Plasma surface texturization for multicrystalline silicon solar cells," *Conference Record of the Twenty-Eighth Ieee Photovoltaic Specialists Conference - 2000,* pp. 367-370, 2000.