An RRAM biasing parameter optimiser

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***Abstract*—Research on memory devices is a highly active field and many new technologies are being constantly developed. However, characterising them and understanding how to bias for optimal performance is becoming an increasingly tight bottleneck. Here we propose a novel technique for extracting biasing parameters conducive to desirable switching behaviour in a highly automated manner, thereby shortening process development cycles. The principle of operation is based on first: applying variable amplitude, pulse-mode stimulation on a test device in order to induce switching multiple times, next: collecting data on how pulsing parameters affect the device's resistive state and finally: choosing the most suitable biasing parameters for the application at hand. The utility of the proposed technique is validated on $TiOx$-based prototypes, where we demonstrate the successful extraction of biasing parameters that allow operation of our devices both as multi-state and binary resistive switches.**

***Index Terms*—RRAM, memristor, characterisation, testing**

I. Introduction

Resistive Random Access Memory (RRAM)-based memory is a very promising candidate in the search for the 'more than Moore' memory technology that could drive the industry beyond the scaling limit of NAND flash. Many attractive properties have already been demonstrated in RRAM devices: simple, two-terminal architecture [1], extreme scalability (down to $4F^2$/cell in planar arrays, 2D and even higher density in 3D arrays) [2], [3], non-volatile storage with long retention times [4], high cycling endurance [5], low write and read energies [6] and potential of achieving single-device multi-level memory.

As RRAM matures the drive to develop a process that reliably delivers all of the aforementioned benefits in a single array intensifies. The road towards achieving this goal will involve significant effort in terms of process development: a systematic exploration of a vast fabrication parameter space (materials specification, fabrication recipe variables, geometry specification etc. [7]–[9]) through successive process optimisation steps entailing 'prototyping, testing and tuning'.

In order to accelerate the process development cycle it is imperative that automated testing routines are developed, such as the ones shown in [10] (generalised marching test assessing device switchability under given biasing conditions) and [11], [12] (tests for finding switching voltages for devices exhibiting abrupt switching). In this work we report on a novel testing routine that is capable of automatically extracting sets of biasing conditions suitable for operating RRAM arrays either as binary or as multi-level memory cells; a biasing parameter optimiser. Our optimiser draws inspiration from the Incremental Step Pulse Programming techniques used in the flash industry [13] and employs programming pulse ramps interspersed with read-out sequences in order to determine the effects of pulse amplitude and duration on the resistive state (RS) of the target device in an automated manner.

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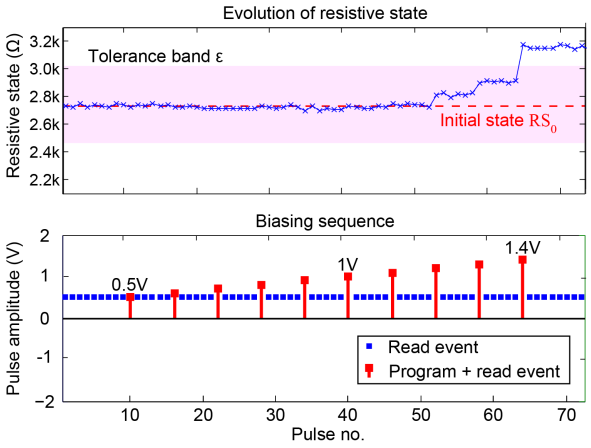

Fig. 1. Example of resistive switching under a pulse train ramp stimulation. Read events are $0.5\,V$ pulses. Program events consist of a $100\,\mu s$ programming pulse followed by a read pulse. RS exits the tolerance band (in this case $\pm 10\%$) after the last programming pulse at $1.4\,V$ via 'RS overshoot'.

Section II details the conceptual basis and function of the optimiser, section III details the implementation specifics and experimental set-up whilst section IV shows measured results from in-house fabricated $TiOx$ devices that validate our approach. Section V contains a discussion on the practical operation of the optimiser and the effects of running parameter choices with section VI concluding the paper.

II. Optimiser description

The optimiser algorithm works on the concept of repeatedly inducing switching in a target device and collecting information on the effects of biasing conditions on RS throughout the process. Switching is achieved by applying progressively more invasive input waveforms to the device under test (DUT). Each time switching is achieved, the last set of input biasing parameters used are saved. A record is also taken of whether DUT RS has switched towards higher or lower resistance. Voltage pulsing stimulation is used as square-wave pulses are easy to generate, can be described sufficiently well by only two parameters (T, V_b) (pulse duration and amplitude respectively) and were found to allow better control of DUT behaviour as opposed to the more traditional voltage sweeping technique.

A. Definitions and assumptions

In order for the optimiser to find appropriate switching parameters automatically, a quantitative definition of 'switching' is required. A DUT is considered to have successfully switched

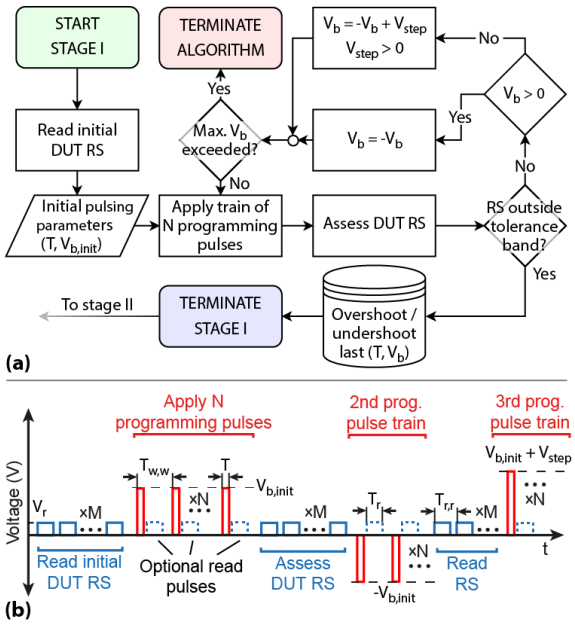

Fig. 2. Initialisation phase of optimiser algorithm. (a) Flow chart. Initial pulsing parameters (T, V_b) are user-defined. Successful (blue) and unsuccessful (red) termination conditions are highlighted. (b) Waveform generated during initialisation phase. Parameter descriptions are shown in table I.

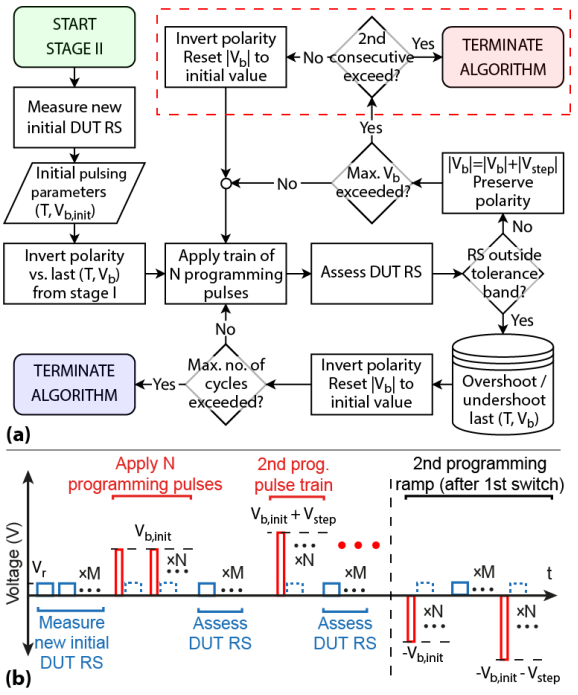

Fig. 3. RS cycling phase of optimiser algorithm. (a) Flow chart. Initial parameters (T, V_b) same as in stage I (Fig. 2). Successful (blue) and unsuccessful (red) termination conditions are highlighted. (b) Waveform generated during RS cycling phase. Parameter descriptions are shown in table I.

from an initial state RS_0 when its RS has exited a specified tolerance band ε (in % of RS_0) around RS_0. If the DUT has switched towards lower (higher) resistance the switching event is termed an 'undershoot' ('overshoot') as shown in Fig. 1.

Optimum operation of the optimiser relies on two assumptions: 1) When biased by a sequence of progressively higher magnitude voltage pulses of suitable polarity, a working DUT will eventually experience a measurable fractional change in its resistive state (RS). 2) The DUTs feature a threshold below which the effects of pulsing on RS are negligible. The first assumption effectively states that there must be biasing conditions (sufficient voltage and suitable polarity) that induce switching as per our quantitative definition above for some value of ε. The second assumption implies that assessments of DUT RS can be carried out via non-invasive 'read' pulses.

B. Algorithm description

The optimiser routine is carried out in two stages: an 'initialisation' stage and an 'RS cycling' stage. In the initialisation stage (I) the system reads the initial RS of the DUT (RS_0) and then applies a succession of programming pulse trains (N pulses/train) of fixed duration, increasing amplitudes and alternating polarities (Fig. 2). DUT RS is assessed between every pair of programming trains. In normal operation this continues until the RS exits the user-defined tolerance band. The alternating polarity of the incoming stimulation pulses ensures that a functioning DUT will be forced to exhibit a sufficient change in RS regardless of initial state and with minimum voltage stress throughout the test. The algorithm terminates unsuccessfully if the maximum allowed bias voltage fails to elicit switching with both polarities.

Notably we can use M read pulses for each assessment of DUT RS in order to obtain both an estimate of RS value and the associated measurement uncertainty. Moreover, each of the N pulses that constitute a programming pulse train can be individually followed by optional read pulses in order to collect more information at the cost of run time (see Fig. 2(b)).

In the RS cycling stage (II), the system applies a succession of incremental step pulse train ramps (ISPTRs). Each ramp consists of stimulation pulse trains of fixed duration and increasing amplitudes at fixed polarity, but successive ramps alternate polarity (Fig. 3). At the beginning of each ramp, DUT RS is measured and RS_0 is reset. In turn, RS is read between each pair of pulse trains. Progressively stronger pulse trains are added to each ramp until DUT RS exits the user-defined tolerance band. Upon switching, pertinent data is saved and the next ramp is initiated. The user decides how many ramps are to be applied during the RS cycling stage. ISPTRs are emitted with alternating polarities because the system is designed to work optimally with bipolar devices, in which case successive ISPTRs are expected to cause DUT RS to oscillate. If an ISPTR reaches the maximum allowed programming voltage and the DUT does not switch, the ISPTR's polarity is considered unable to switch the device at its given state. The optmiser will attempt to apply ramps in both polarities before deeming a DUT unswitchable altogether and terminating unsuccessfully (see Fig. 3(a)).

III. Implementation

The experiment was performed on stand-alone RRAM device arrays of TiO_{2-x} as described in [14]. The optimiser was implemented on an instrument previously described in [15], [16]. In our current implementation of the optimiser

algorithm, there is a total of 12 key parameters, eight of which are controllable by the user. These are summarised in table I, where user-controllable parameters lie below the red line.

TABLE I
OPTIMISER PARAMETER LIST.

Parameter	Description	Units
V_r	Read pulse voltage (fixed $0.5\,V$)	V
T_r	Read pulse duration (automatically set)	μs
$T_{r,r}$	Interval between successive read operations	μs
$T_{w,w}$	Interval between successive write operations	μs
$V_{b,init}$	Initial/minimum programming pulse voltage	V
V_{step}	Voltage step	V
V_{max}	Maximum allowed pulse voltage	V
M	No. of read pulses per RS assessment	-
N	No. of programming pulses per train	-
T	Programming pulse duration	μs
ε	Minimum fractional RS change vs initial state required for successful switching	%
C	No. of switching cycles in RS cycling stage	-

The testing system automatically attempts to optimise read-out time as a function of the RS value being read. Timing between successive reads and successive writes is not under user control in the current optimiser implementation. Instead, pulses are sent as soon as the system is ready to source them. Future implementations will grant that control as DUT behaviour and results may be affected by timing choices (e.g. $T_{w,w}$ may affect DUT behaviour through possible thermal effects [17] and $T_{r,r}$ will affect algorithm results in samples exhibiting noticeable RS volatility [18]).

IV. EXPERIMENTAL RESULTS

In order to validate the optimiser algorithm, a series of tests were ran on a total of 22 randomly selected DUTs, during which we gradually refined our choices of user-controlled parameter values. In this section we present results from three runs executed on three separate devices, which were deemed to showcase interesting behaviour. The user-controlled parameter settings for each run are summarised in table II.

TABLE II
USER-CONTROLLED PARAMETER SETTINGS FOR OPTIMISER RUNS.

Parameter	DUT 1	DUT 2	DUT 3	Units
$V_{b,init}$	0.5	0.5	0.5	V
V_{step}	0.1	0.05	0.1	V
V_{max}	4.0	2.5	4.0	V
M	5	5	5	-
N	10	10	1	-
T	100	100	100	μs
ε	10	15	10	%
C	25	25	25	-

A. DUT 1 test:

DUT 1 was subjected to the optimiser routine with the intention of finding biasing parameters that operate the device in the analogue switching regime. We define this as the biasing regime whereby applying stimulation in the form of identical pulse trains will cause the device to 'SET' (move towards lower resistive state) or 'RESET' gradually, i.e. RS will change in small steps as the pulses arrive. To that end the number of programming pulses per train was set to $N = 10$ and the RS tolerance band to the relatively small value of $\varepsilon = 10\,\%$. The voltage step was kept at $V_{step} = 0.1\,V$ as the initial optimiser runs indicated that our test devices respond to such bias voltage increments with a comfortably moderate change in RS switching rate (e.g. see Fig. 4(c1)). This choice of parameters was expected to allow the DUT to exit the tolerance band as a result of a succession of small RS increments/decrements caused by a multitude of identical pulses.

Our prototype devices support analogue switching with DUT 1 constituting a good example of a well-behaved device operating clearly in analogue, bipolar switching regime as shown in Fig. 4. Stage I of the optimiser ends when positive polarity pulsing causes the DUT to undershoot its RS tolerance band. Stage II then successfully cycles DUT RS 25 times. Notably, RS oscillates within a relatively tight range throughout the test run (see panel (a1)). Overshoots and undershoots follow each other in strict alternating succession whilst the voltages at which switching occurs (the 'switching voltages') seem to be relatively stable throughout the duration of the test run. Plotting the normalised change in RS (the 'switching rate' ΔR) as a function of the voltage employed in each pulse train (V_b) we notice a clear trend towards obtaining SET transitions under positive voltage bias and RESET under negative. The curvature of the $\Delta R(V_b)$ characteristic justifies our choice of $0.1\,V$ as a reasonable V_{step} value for exploring the bias voltage space (i.e. the x-axis of panel (b1)). If we consider the switching rate as a function of both bias voltage and initial state we obtain the figure in panel (c1) (the 'switching surface'), which reveals no observable link between switching rate and initial RS within the operating RS range the device traverses during the test run ($1.8\,k\Omega - 2.8\,k\Omega$).

In order to validate our methodology, DUT 1 was subjected to a further set of pulse trains (250 pulses/train) following the optimiser test run. Successive pulse trains featured opposite polarities whilst amplitudes were determined based on the set of switching voltages collected during the preceding optimiser run (Fig. 4(b1)). In this case we used the minimum magnitude over- and undershoot switching voltages in order to ensure that we obtain slow, gradual switching and visit many intermediate resistive states. Results are shown in Fig. 5. The chosen stimulus conditions indeed operate DUT 1 in the desired analogue switching regime for both SET and RESET directions. Notably, the device reacts to the pulse trains with a progressively saturating RS response.

B. DUT 2 test:

DUT 2 was subjected to a similar test as DUT 1, but this time we sampled the bias voltage space in steps of $V_{step} = 50\,mV$. Furthermore, the tolerance band was set to $\varepsilon = 15\,\%$. The obtained results are shown in Fig. 4, middle panels. We observe that in principle DUT 2 also shows clear bipolar operation with RS oscillating within a relatively narrow range of values (panel (a2)) whilst over- and undershoot events follow each other in strict alternating succession. Switching voltages for this device are consistent, however, the plot of

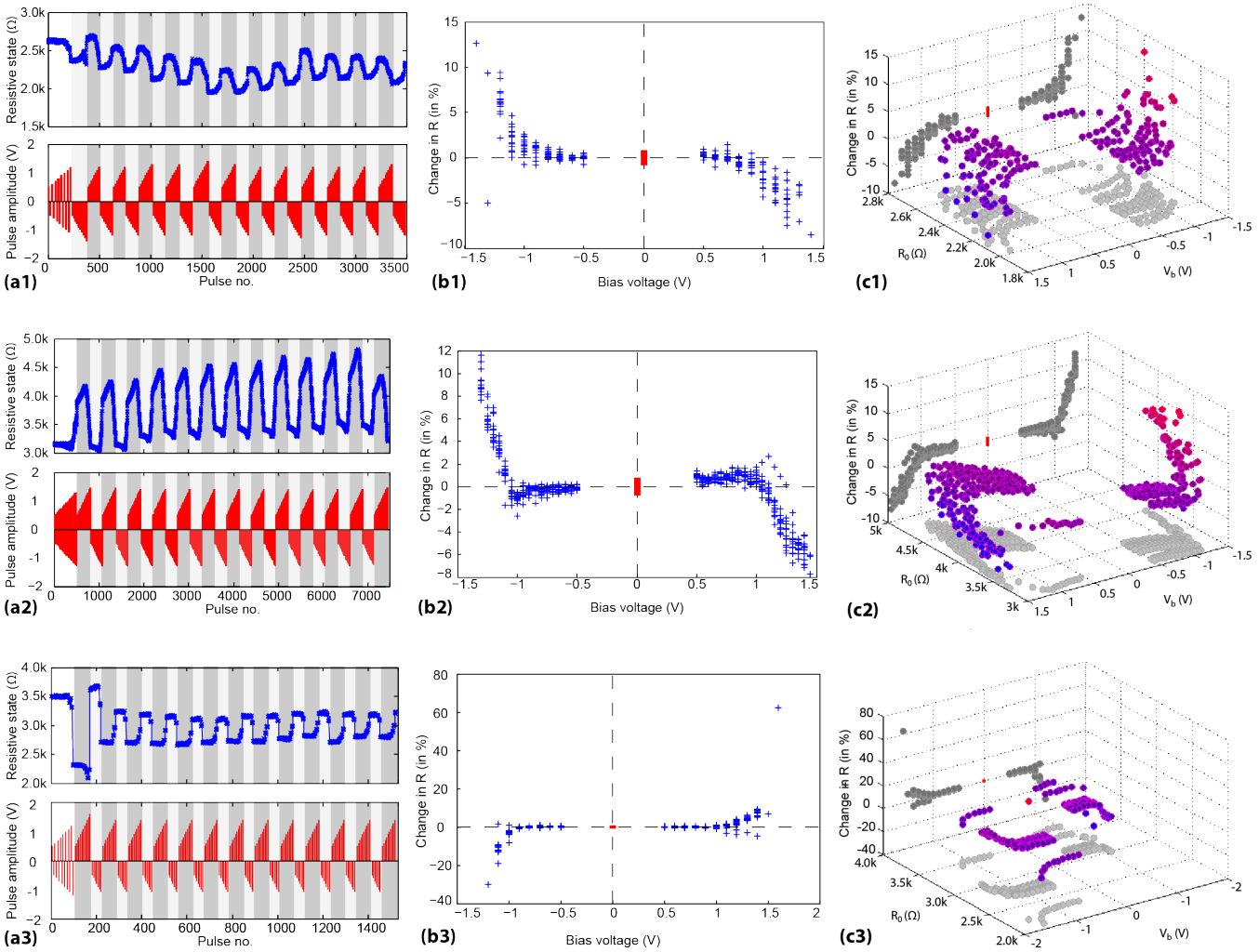

Fig. 4. Optimiser test run results. Top panels: DUT 1. (a1) Evolution of DUT RS with input pulses. Top trace: RS measurements. Bottom trace: Programming pulse sequence. Gray shading highlights DUT reaction to successive ISPTRs during the RS cycling phase of the algorithm. (b1) Normalised change in RS ('switching rate') recorded after application of each train of programming pulses as a function of pulse voltage ($\Delta R(V_b)$). The red bar denotes the largest min-max range of RS values recorded during a single DUT RS assessment operation - a conservative estimate of confidence limits (normalised to final, average reading). DUT 1 exhibits 'SET'-type transitions (towards lower RS) under positive voltage bias and 'RESET'-type under negative bias. (c1) 'Switching surface' of DUT 1, i.e. $\Delta R(V_b, R_0)$ where R_0 the DUT RS before application of each programming pulse train. Red bar as in (b1). Projections of the data-points on the (R_0, V_b) and $(\Delta R, V_b)$ planes are shown in light and dark gray respectively; the latter corresponding to sub-figure (b1). Middle panels (a2,b2,c2): DUT 2. Two distinct bipolar operation regions are observed: one for pulses with $|V| <\approx 1V$ featuring SETs at negative voltages and another one for stronger pulses exhibiting SETs at positive voltages. Bottom panels (a3,b3,c3): DUT 3. The effect of stimulation is heavily concentrated on the last pulse in each ISPTR.

switching rate vs. programming pulse train voltage (panel (b2)) reveals two distinct regions of bipolar operation. The first region concerns pulse voltages of magnitude below $\approx 1\,V$ and features mild SET transitions at negative voltage and RESET at positive. The second region surrounds the first and features markedly stronger SET/RESET transitions triggered by the opposite polarities vs. region 1. It is pulses belonging to region 2 that cause DUT RS tolerance band exits in both directions during the test run. This would not have necessarily been the case had ε been set to a lower value. Finally, the full switching surface figure (panel (c2)) shows little dependence of the switching rate on initial RS within the test-specific operating RS range of DUT 2 ($3\,k\Omega - 5\,k\Omega$).

C. *DUT 3 test:*

DUT 3 was subjected to the optimiser routine with the intention of finding biasing parameters that operate the device in the binary switching regime. We define this as the biasing regime whereby the device can be repeatedly toggled between two distinct resistive state ranges after application of single-pulse stimulation (typically dubbed the High Resistive State (HRS) and Low Resistive State (LRS) ranges). To that end the number of programming pulses per train was set to $N = 1$ with the tolerance band remaining at $\varepsilon = 10\,\%$ and voltage step at $V_{step} = 0.1\,V$. This choice of parameters was expected to facilitate switching via single-pulse events under the rationale that the rapid increase in biasing voltage caused by the low value of N would concentrate the effect of each ISPTR on the final, strongest pulse. ε was kept low in this work since our

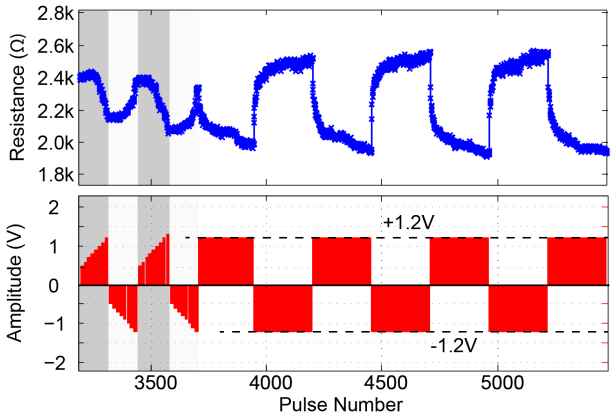

Fig. 5. Behaviour of DUT 1 immediately after completion of optimiser run in Fig. 4, top panels. Top trace: DUT RS measurements. Bottom trace: Programming pulse sequence. Gray shading indicates the last few cycles of the preceding optimiser run. Subsequently the device was biased with $+1.2\,V$ and $-1.2\,V$ pulse trains (250 pulses/train); parameters chosen based on the results from Fig. 4(b1). DUT 1 shows good analogue switching behaviour.

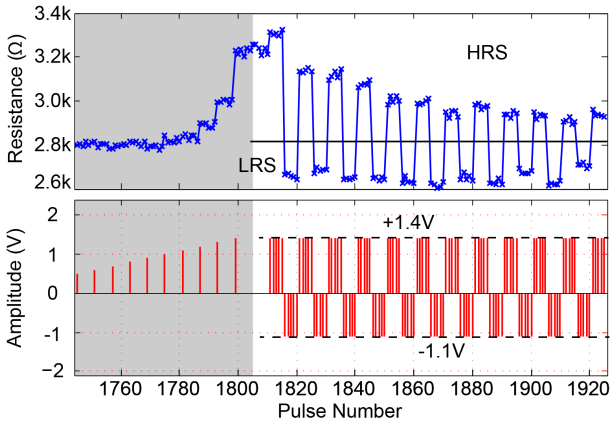

Fig. 6. Behaviour of DUT 3 immediately after completion of optimiser run in Fig. 4, bottom panels. Top trace: DUT RS measurements. Bottom trace: Programming pulse sequence. Gray shading indicates the last cycle of the preceding optimiser run. Subsequently the device was biased with $+1.4\,V$ and $-1.1\,V$ pulse trains (5 pulses/train); parameters chosen based on the results from Fig. 4(b3). DUT 3 shows clear binary switching behaviour. Solid horizontal line in top trace marks a possible threshold between two distinct, High Resistive State (HRS) and Low Resistive Range (LRS) ranges.

devices operate most reliably when not forced to repeatedly undergo large changes in RS. Nevertheless, depending on the application ε can be adjusted to better match the desired minimum acceptable ON/OFF ratio. Finally, V_{step} was not changed as we wished to obtain a bias voltage value not far in excess of what is strictly necessary in order to elicit binary switching in our DUT.

Results for DUT 3 are shown in Fig. 4, bottom panels. The effects of the stimulation protocol are clearly visible in panel (a3). DUT RS can be observed to exit the specified tolerance band via significantly more abrupt RS transitions than DUT 1 and DUT 2, although still in a distinctly bipolar fashion. Switching voltages remained stable during this stimulation protocol, although for this particular device SET transitions were elicited by negative voltages; opposite to DUTs 1 and 2. Devices of opposite switching voltage polarities can be routinely found in our samples although the behaviour of DUTs 1 and 2 is significantly more common. Panel (b3) confirms the 'anti-polar' behaviour of DUT 3, as does the switching surface of panel (c3).

In order to validate our methodology, DUT 3 was subjected to a further set of pulse trains (5 pulses/train) of alternate polarities following the optimiser test run; similarly to DUT 1. Amplitudes were chosen based on the measured switching voltages seen in Fig. 4(b3). In this case we chose the most frequent values of $1.4\,V$ and $-1.1\,V$ for overshoots and undershoots respectively as they remained stable throughout most of the optimiser run. Results are shown in Fig. 6. The chosen stimulus conditions successfully operate the device in the binary switching regime for both SET and RESET transitions. It is always the first pulse in the train that delivers the most impact on DUT RS indicating that the RS response is saturating in nature, much like for DUT 1 (Fig. 5). At these voltages, however, a single pulse of $100\,\mu s$ duration suffices to drive the device to the limits of its range.

D. *Fixed parameters:*

All tests were carried out with programming pulses lasting $100\,\mu s$. This value was chosen because it allows for relatively short testing times with good pulse-width control. We have kept it fixed throughout this work in order to concentrate our study on the effects of pulse amplitude as an RS switching driver. The selected number of read pulses per RS assessment operation ($M = 5$) was deemed sufficient given our instrument's precision whilst the number of switching cycles during the RS cycling stage of the optimiser was set to $C = 25$ in order to observe the distribution of switching voltages and uncover any trends as the device is repeatedly cycled. The minimum programming pulse voltage was maintained at $V_{init} = 0.5\,V$, i.e. the read-out pulse amplitude in order to ensure that each ISPTR starts from a non-invasive voltage level. Finally, the maximum allowable voltage was set to $V_{max} \geq 2.5\,V$ as it was observed that our test devices tend to routinely switch at $< 2\,V$. Notably, the specific value used did not impact the execution of the optimiser tests as no switching voltage ever exceeded a magnitude of $1.6\,V$. Finally, optional read-out pulses followed each programming pulse (as explained in section II-B and shown in Fig. 2(b)) in all tests, although the resulting data is not used in the present work.

V. Discussion

The proposed optimiser simplifies the problem of finding suitable switching parameters for RRAM devices to the less complex problem of finding user-controllable parameters that allow the system to automatically determine said parameters. To that end our approach is designed to make use of as few assumptions as possible: no assumptions are made on whether the initial DUT RS is 'high' or 'low', what input signal polarity is required to elicit RS change in either SET or RESET direction, what 'flavour' of switching the device is capable of exhibiting (analogue or binary) etc. Results from

section IV validate the approach and confirm the usefulness of the system for our $TiOx$-based devices; devices exhibiting non-volatile, bipolar switching characteristics for which the current implementation of the optimiser is tailored to extract the most relevant results.

RRAM device behaviour is affected by biasing history. For that reason all extracted switching voltages (which drive the biasing sequence) will reflect the effects of a whole series of programming pulses on the DUT. However, the key information lies in the switching rate plots (Fig. 4(b,c)) rather than the switching voltages themselves. From there it is possible to see what bias voltage on average corresponds to the desired switching rate, how tight the bias voltage-switching rate link is and how much it depends on initial RS.

The user-controlled parameters (notably ε, V_{step} and N - see table I) should be set such that bias voltages corresponding to the desired switching rates are recorded as quickly as possible and at minimal voltage stress on the DUT. If ε is too large, ISPTRs have a chance of reaching destructively high voltages before switching is acknowledged and captured switching rate values run a higher risk of exhibiting a dependence on DUT RS. Excessively small values, on the other hand, will lead to false switching detection as a result of measurement uncertainty. Large values of V_{step} tend to sample the bias voltage space too sparsely (x-axis in Fig. 4(c1)) and increase the risk of applying unnecessarily large voltages on the DUT whilst excessively low values may cause the DUT to reach switching before desirably high switching rates are recorded and unduly prolong testing time. Overly large values of N similarly slow down testing and tend to cause switching before high switching rates are reached, although having $N > 1$ helps see the cumulative effects of a succession of identical pulses and reveal any dependencies of switching rate on DUT RS.

VI. Conclusions

In this work we have presented an algorithm capable of providing crucial information on the switching behaviour of RRAM devices in a highly automated manner. The system is designed to work with as few assumptions as possible in order to provide meaningful results in the broadest possible scenarios, although it is optimised to work with bipolar, non-volatile devices. The utility of the proposed routine is validated through tests on $TiOx$-based RRAM samples, whereby switching parameters for analogue and binary operation are successfully extracted with minimal effort, time cost and voltage stress on each respective DUT. Furthermore, information collected throughout each test run is automatically compiled into 'switching rate' and 'switching surface' plots that allow an overview of DUT behaviour at a glance. Finally, some practical guidelines on how to operate the system for optimal time/voltage stress/result relevance performance are shared.

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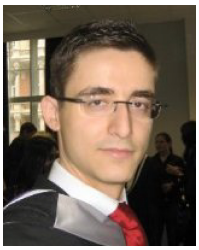

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