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FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Electronics and Computer Science

MICROFABRICATED PAUL TRAPS FOR LEVITATING AND SHUTTLING OF IONS AND CHARGED PARTICLES

by

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ABSTRACT

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Trapped ions in Paul traps (radio frequency ion traps) are a promising candidate for the realization of a quantum computer. To date, experimental demonstrations of quantum computing and information processing with trapped ions have been limited to small numbers of quantum bits (qubits). The most prominent challenge to realise ion-trap quantum computation is to scale the system and control a large number of trapped ions coherently. Surface-electrode ion trap designs which are amenable to various microfabrication techniques offer a path to achieve this.

In this work, design, fabrication and key operations of two types of surface-electrode ion traps, i.e. a Y-junction trap and a two-dimensional (2D) hexagonal lattice trap developed towards scaling ion-trap architectures, are presented. The steps involved in the fabrication of the ion-trap devices included photolithography, wet etch (hydrofluoric acid etch) and dry etch (deep reactive ion and inductively coupled plasma etching), and metal evaporation. The devices were fabricated on SOI substrates with different buried oxide thicknesses (i.e. 5 μm and 10 μm) and different metals for the trap electrodes (i.e. gold and aluminium). An extremely high-breakdown voltage up to 1 kV was measured in vacuum for the SOI-built test devices with a 10 μm-thick buried oxide formed by oxide film-to-oxide film bonding process. This is attributed to the deep V-shaped undercut profile of the buried oxide layer which resulted in a large breakdown path length, and so mitigating surface breakdown effects. Owing to the V-shaped undercut profile, the surface breakdown voltage was improved by 15% for the devices fabricated on SOI substrates with a 10 μm-thick buried oxide.

In the first experiment, the demonstration of ytterbium ($^{174}Yb^{+}$) ion trapping in the 2D hexagonal lattice trap is achieved with a relatively long lifetime of a laser-cooled ion up to 90 minutes and ≤ 5 minutes without cooling in ultra-high vacuum system. The 2D lattice trap design allows for reliable trapping of 2D ion lattices, rudimentary shuttling between lattice sites and deterministic introducing of defects into the ion lattice. Based on all these abilities, such a 2D lattice trap with the predicted reduction of lattice spacing down to 32 μm can be configured as a versatile architecture for 2D quantum simulations with trapped ions. In the second experiment, microparticle trapping in the 2D lattice trap, performed in air, is achieved with the longest trapping lifetime of 60 minutes. Both gold and aluminium-coated electrodes also lead to comparable trapping performances. Furthermore, the *in situ* levitation of microparticles is successfully demonstrated at the maximum levitation height of 30 μm. This ability provides additional control on the trapping height which increases the overall functionality of the 2D lattice trap.

List of Contents

List of Figures

List of Tables

Declaration of Authorship

I, Hwanjit Rattanasonti, declare that the thesis entitled "*Microfabricated Paul traps for levitating and shuttling of ions and charged particles*", and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research.

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List of Publications

[1] R. C. Sterling, **H. Rattanasonti**, S. Weidt, K. Lake, P. Srinivasan, S. C. Webster, M. Kraft, and W. K. Hensinger, "Fabrication and operation of a two-dimensional ion-trap lattice on a high-voltage microchip," *Nat. Commun.*, vol. 5, p. 3637, Apr. 2014.

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[3] **H. Rattanasonti**, R.C. Sterling, P. Srinivasan, W.K. Hensinger and M. Kraft, "Wet etching optimization for arbitrarily shaped planar electrode structures," in *MME2010 21st Micromechanics and Micro systems Europe Workshop : Abstracts*. University of Twente, Transducers Science and Technology, Enschede, The Netherlands. ISBN 978-9081673716, pp. 305-308, Sep. 2010.

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Definitions and Abbreviations

AC	Alternating Current
ADRE	Aspect Ratio Dependent Etching
APC	Automatic Pressure Control
BDRB	Banded Double-Ring Electrodynamics Balance
BEM	Boundary Element Method
BHF	Buffered Hydrofluoric Acid
BOE	Buffered Oxide Etch
BOX	Buried Oxide
CCD	Charge-Coupled Device
CPO	Charged Particle Optics
DC	Direct Current
DI	Deionized
DRIE	Deep Reactive Ion Etching
EBC	Electrodynamics Balance Chamber
EDB	Electrodynamic Balance
ESI	Electrospray Ionization
FDM	Finite Difference Method
FEM	Finite Element Method
FNA	Fuming Nitric Acid
GND	Ground
HARS	High-Aspect Ratio Structure
HF	Hydrogen Fluoride, Hydrofluoric Acid
ICP	Inductively Coupled Plasma
IPA	Isopropyl Alcohol
IQT	Ion Quantum Technology
LIT	Linear Ion Trap
MEMS	Microelectromechanical Systems
OIPT	Oxford Instruments Plasma Technology
ORC	Optoelectronics Research Centre
PCB	Printed Circuit Board
PETEOS	Plasma Enhanced Tetraethylorthosilicate
PECVD	Plasma Enhanced Chemical Vapour Deposition
PR	Photoresist
QCCD	Quantum Charged-Coupled Device
QIP	Quantum Information Processing
QIT	Quadrupole Ion Trap
QMF	Quadrupole Mass Filter
Qubit	Quantum Bit
RIE	Reactive Ion Etching
RF	Radio Frequency
RMS	Root Mean Square

SEIT	Surface-Electrode Ion Trap
SEM	Scanning Electron Micrograph
SNC	Southampton Nanofabrication Centre
SOI	Silicon-on-Insulator
SOQ	Silicon-on-Quartz
SOS	Silicon-on-Sapphire
STS	Surface Technology Systems
TDME	Time Multiplexed Deep Etching
3D	Three-Dimensional
2D	Two-Dimensional
UCL	University College London
UHV	Ultra-High Vacuum
VLSI	Very-Large-Scale Integration

V_{AC}	AC voltage
g	Acceleration of gravity
Ω	Angular frequency
Q, z	Charge
Q/m	Charge to mass ratio
U	DC voltage
ρ_m	Density of the medium
ρ_p	Density of the particle
k	Dielectric constant
b	Dimensionless drag coefficient
η	Dynamic viscosity of the fluid
$\omega S_E(\omega)$	Electric field noise
V_{bd}	Electrical breakdown voltage
C_D	Empirical drag coefficient
F_D	Friction force (or drag force)
κ	Geometric factor
$\dot{\bar{n}}$	Heating rate
h, d	Ion-electrode distance, ion height, trap height
ν	Kinematic viscosity of fluid
Kn	Knudsen number
m	Mass
λ	Mean free path of the fluid
ϕ	Potential field
ψ	Pseudopotential
ε	Ratio of a secondary to a primary AC voltage
Re	Reynolds number
V_{RF}	RF voltage
f_{osc}	Scanning frequency
$\omega/2\pi$	Secular frequency of ion (charged particle) motion
C_C	Slip correction factor

$S_E(\omega)$	Spectral density of electric field noise
R_p	Spherical object dimension in radius
D_p, $\varnothing$	Spherical object dimension in diameter
a	Stability parameter q
q	Stability parameter a
D	Trap depth
$\Omega/2\pi$	Trap driving frequency
ε_0	Vacuum permittivity constant
u	Velocity of the object relative to the fluid

Chapter 1

Introduction

1.1 A brief history of charged particle confinement

Earnshaw's theorem states that a collection of point charges cannot be maintained in an equilibrium configuration solely by the electrostatic interaction of the charges. This was originally formulated for electric forces and first proven by Samuel Earnshaw in 1829. In later years, it was also proven by other physicists that not only a static set of electric charges but also magnetic diploes (e.g. a permanent magnet), electric dipoles and steady currents are governed by Earnshaw's theorem [1]. As a consequence, the stable levitation of matter in a free space using electrostatic, magnetostatic or gravitational forces, or any combinations thereof, to generate a three-dimensional potential well necessary for trapping (i.e. a minimum of the potential, a saddle point) is not possible without other mechanical, feedback control or dynamic forces. However, this did not stop scientists from trying to find a loophole in the levitation techniques which are not ruled out by Earnshaw's theorem. In the twentieth century, levitation became the active field. A series of theoretical works and experimental studies were carried out and published. Physicists have successfully demonstrated several design techniques of levitation using a variety of physical means to counter gravity and to violate or escape the restrictions underlying Earnshaw's theorem.

A number of levitation schemes (e.g. electrostatic, magnetic, electromagnetic, acoustic, aerodynamic, optics) have been developed over the years. In more recent times, the novel quantum levitation has been demonstrated using the Casimir force to achieve stable levitation of nano-objects. With different physical principles, these levitation methods have their own relative advantages and disadvantages, making it difficult to precisely gauge the scope of each technique. One of the most well-known levitation procedures called the Millikan oil droplet experiment (MODE) was performed originally by Robert Millikan in 1906. Millikan started his work in attempting to measure the electron charge and continued for several years until the crucial first article was published announcing the measurement of the electronic charges on single droplets in 1913 [2]. For part of this work, he was awarded in the Nobel Prize in Physics in 1923 "*for the work on the elementary charge of electricity and on the photoelectric effect*". Since then, the Millikan condenser or electrostatic balance became the basis for a wide variety of physical studies of matter (e.g. aerosols, colloids, metals, alloys, semiconductors, bio-particles, protein droplets) and enabled modern single-particle levitations to a broad range of applications, such as the study of physical properties, biochemistry, biology, pharmaceutical, mass spectrometry and quantum computing, many years later.

In the early 1950s, the principle of electrodynamic balance (EDB) of charged particles by an alternating current (AC) quadrupole configuration was first discovered by Paul and co-workers [3], [4]. They invented two novel ion traps that function both as an ion storage device and as a mass spectrometer [5]. The invention of the ion trap technique was recognised by the award of the 1989 Nobel Prize in Physics, half jointly to Wolfgang Paul and Hans Dehmelt. The quadrupole ion trap was initially used by the Physics community led by Dehmelt at the University of Washington to study the properties of atomic ions. As a storage device, ions were trapped by the formation of a trapping potential when applying appropriate voltages to the electrodes of the ion trap. The quadrupole ion trap applied a direct current (DC) voltage to two endcap electrodes and a radio frequency (RF) oscillating electric field to the ring electrode to create a saddle-shaped field to trap ions at the centre of the trap. This ion trap was also operated as a mass filter using a mass-selective-stability mode of operation in which only ions of one particular m/z value (mass m and z charge) can be

trapped at a time. To address this limitation, Stafford and his colleagues [6] at Finnigan MAT developed the mass selective instability mode in which all ions generated were stored while mass analysis was performed and sequentially ejected from the trap. This new technique incorporating the use of a helium damping gas of 1 mTorr improved the mass resolution and led to the development of a commercial ion trap mass spectrometer [7]. The quadrupole mass filter with four hyperbolic rods was capable of operating in an analogous manner to a conventional quadrupole ion trap with a ring electrode and two endcaps. In later works, the circular-shaped electrodes were found to be applicable and simpler in terms of design and assembly compared to the hyperbolic-shaped electrodes. The quadrupole mass filter with four circular rods arranged in similar form to the hyperbolic-shaped quadrupole ion trap attracted more interest in the field of mass spectroscopy.

The ion trap techniques established in the 1950s for ion spectroscopy were further developed for manipulating aerosol particles for *in situ* analysis. This certainly opened up the study of the chemical physics or aerocolloidal particles. Shortly after the first introduction of the quadrupole ion trap, a major advance in microparticle levitation was investigated by Straubel [8] in 1956. A single charged droplet or particulate was suspended stably in a "*Straubel trap*" which is the simplest design of a particle trap with a modification of the Millikan condenser and the implementation of EDB. The trap consists of two flat plates (endcaps) of an original Millikan apparatus and the additional AC electrode in a ring shape located at the middle plane between the flat plates [9], [10]. In an EDB, a particle (in the size range 0.1-100 μm) can be held stationary by a combination of AC and DC electric fields. A charged particle experiences an electrostatic force (DC potential) applied to the endcaps for balancing the gravitation and drag forces of the particle and a time-varying force (AC potential) applied to the ring for focusing the particle to the centre of balance [11].

Many other EDB configurations to suspend charged particles (i.e. charged dust, ions, and electrons) in dynamic equilibrium were proposed years after due to their high desirability for being able to chemically characterise particles in a variety of particle sizes ranging from small scales in nanometre to large scales in sub-millimetre. The electrodynamics balance chambers (EBCs) were used to study a wide range of particle sizes from a few microns

presented in Straubel's work [9], [10] and Wuerker's work [12], and to suspend sub-millimetre droplets (>750 μm in diameter) in a banded double-ring electrodynamics balance (BDRB) presented in Jacko and Reed [13]. Historically, levitation of particles this large has never been accomplished using only electrodynamic suspension. The necessary condition for the proper operation of electrodynamic trapping systems depends upon finding appropriate electrode configurations which create sinusoidal time-varying forces whose strengths are in first order proportional to the distance from the centre of the trap. In 1959, Weurker et al. [12] developed the electrodynamic suspension system for trapping iron and aluminium dust particles with diameters of a few microns using the electrode configuration similar in form to conventional quadrupole ion traps. Later, in 1983, Weiss-Wrana [14] introduced a particularly useful adaptation of Straubel's EDB called "*the double-ring configuration*" by replacing the middle ring with two parallel rings located above and below the middle. In the late 1980s, this EDB device was employed in Davis et al. [15] to measure the radioactivity of single aerosol particles. A few years later, Ray and Souyri [16] and Davis et al. [17] showed that the double-ring configuration can be adapted and simplified by applying both AC and DC bias voltages to the middle rings and eliminating the endcaps.

Numerous electrodynamic balance (EDB) techniques reviewed in Davis [18] and Krieger et al. [19] have proven to be a useful experimental tool and used in numerous studies on atmospheric aerosol microparticles and microdroplets in different processes and applications including characterisation of physical, chemical and optical properties, thermodynamic properties, evaporation and condensation, and chemical reactions. The versatility of the classical EDB systems has been demonstrated over decades. Right up to the late 1990s, the use of EDB systems was expanded to the biological, medical, and pharmaceutical research fields [20], [21]. The increasing complexity in these studies continues to push the technological limits of experimental tools for handling and analysing samples simultaneously. In recent years, a new EDB design called a coaxial double cylindrical EDB coupled with Raman system allowing *in situ* characterisation both of physical and chemical changes of the levitated inorganic particles was presented [22].

1.2 Ion-trap technology for quantum computing

The first ion storage device (trapping device) was invented by Kingdon [23] in 1923. The "*Kingdon*" trap consists of a thin wire (central electrode) surrounded by a metal cylinder (outer electrode) with flat endcap electrodes enclosing the trapping volume. In the Kingdon trap, there is no potential minimum to store the ions. However, ion confinement in this trap is achieved by employing "*orbital trapping*" in a purely electrostatic field. A direct current (DC) voltage is applied between the central wire and the cylinder producing a radial logarithmic potential between these two electrodes. An axial motion along the central electrode is also governed by the field curvature produced by the endcaps. The first application of a Kingdon trap as a mass spectrometer (analyser) occurred in 1981 when Knight [24] introduced a modified-geometry Kingdon trap called "*The ideal Kingdon trap*" that provided a harmonic axial potential in addition to the radial logarithmic term. The outer electrode was modified to a barrel-like form and symmetrically split into halves in a close form to the endcaps of the quadrupole ion trap (QIT). Later, the variations in the Kingdon trap geometry towards the development of the "*orbitrap*" from a purely electrostatic field to a quadro-logarithmic field (a near-ideal quadrupole field) included (i) using two parallel wires for the central electrodes [25], (ii) superimposing an AC voltage on the DC potential (the dynamic Kingdon trap) for improving trap efficiency [26], and (iii) applying the ideal Kingdon trap to determine Mass-to-charge (m/z) ratio from the frequency of harmonic ion oscillations along the central electrode [27], [28].

It was not until the early 1950s that Paul and his colleagues developed an ion-trap device based on the electrodynamic balance (EDB) of a quadrupole-type configuration called the *"Quadrupole ion trap* (QIT)*"* also known as the *"Paul trap"* [29]. Ion trapping in Paul traps is governed by a combination of a sinusoidal radio frequency (RF) electric field at frequency ~1 MHz, and static DC electric fields. In its classical form, the Paul trap exists in two configurations (i.e. 3D and 2D linear form) which function both as an ion storage device in which gaseous ions can be trapped for a period of time and as a mass filter (spectrometer) of selective m/z ratio, and all of this operates at a pressure of 1 mTorr of helium buffer gas. The first device was the quadrupole ion trap (QIT) comprising two hyperbolic electrodes with

their foci facing each other (endcaps) and a hyperbolic ring electrode halfway located between the endcaps. The second device called the quadrupole mass filter (QMF) consists of four hyperbolic rods with two pairs of electrodes set diagonally across from each other and driven by a radio frequency (RF) potential with an opposite polarity. Following the pioneering work of Paul et al. [29], the first high vacuum magnetron trap, also called "*Penning trap*" using a strong homogeneous magnetic field to confine particles radially and a quadrupole electrostatic potential to confine the particles axially was invented by Hans Dehmelt in 1959. In the early development of ion traps, they have been mainly used as ion store for investigation of the charge, mass and spin of trapped particles. More recently, ion traps have been found to be more useful instruments in wide-ranging applications in many fields of physics such as mass spectrometry [30]–[32], atomic clocks [33], a useful system for studying elements of quantum dynamics [34], quantum teleportation [35], nuclear physics [36], cosmology [37], and as a very promising tool for building quantum computer [38]–[40] with the advent of laser cooling [41], [42] and laser spectroscopy [43]. In particular, during the past two decades, the most impressive progress of trapped ions has been made in a new field of quantum computing where physics and computer science have been combined.

In this new field, the use of quantum technologies to develop future quantum computers has become attractive for two compelling reasons. First, the advancement in semiconductor technology towards the development of smaller and faster logic-gate devices for conventional computers is achieved by reducing the size and increasing density of transistors on integrated circuit (IC) chips. According to a trend known as Moore's Law, this technology is, however, moving towards its demise and is expected to reach its fundamental limits (the inevitable quantum-mechanical atomic and nuclei limits) due to the fact that the quantum effects will dominate the behaviour of the device once transistors become smaller and are built nearly on the atomic/nucleus scale [44]. This opens up a new era of quantum computing. The field of quantum computing based on the quantum mechanical processes was initiated by the work of Manin [45] in 1980. In later years, a number of key advances have been made in the theory of quantum computation. In 1982, Benioff [46] and Feynman [47] contributed to the early development of theoretical framework for a "quantum computer" – that is, a computer that

takes advantage of certain fundamental quantum mechanical phenomena for the operations on data. During the same period, a very important discovery of a theory of an "*universal quantum computer*", also a quantum Turing machine, was made by Deutsch [48] in 1985. Within this research venue, scientists have developed a significant volume of theoretical and experimental works for realising quantum computing (QC), and more generally in quantum information processing (QIP). In quantum regime, a number of elements such as atoms, ions, electrons or photons can be used to store the basic unit of quantum information called quantum bit (qubit) which can be expressed by quantum mechanics using the principles of superposition and entanglement [38], [49]. Unlike a classical bit which can store only a single value of either 0s or 1s as conventional computers do, a quantum bit has more than two possible states; 0, 1 and a combination of two states that obeys the superposition principle resulting in each qubit being able to store two values simultaneously. The combination of quantum superstition and quantum entanglement of multiple qubits makes quantum computation enormously powerful as the amount of information carried by qubits expands exponentially compared to that of classical computation.

To build a real quantum computer, current efforts are being made in finding suitable physical implementations for quantum bits. Prototypes of quantum computing and information processing have been realised in various physical systems including trapped ions [50]–[52], neutral atoms [53]–[57], optical photons [58]–[60], nuclear magnetic resonance (NMR) in molecules [61], [62], silicon-based nuclear spins [63], nitrogen-vacancy colour centre (or NV-centre) in diamond [64], electron spins (using GaAs quantum dot [65], [66] and InAs Nanowire [67]) and superconducting electrical circuits (i.e. Josephson junctions [68], [69]). So far trapped ions seem to be the most promising candidate by meeting most of the requirements for a functional quantum computer outlined by DiVincenzo's criteria [70].

"*Trapped ions*" as a viable quantum computing candidate were first proposed by Cirac and Zoller [50] in 1995, and demonstrated experimentally shortly afterward by Monroe and co-workers [51] in 1997. The ion trap technology becomes a promising candidate as a scalable architecture for the practical implementation of large-scale quantum computers. Proof-of-principle experiments of quantum computing using one qubit or a small number of qubits have

already been demonstrated [71]–[74]. One of the remaining challenges towards realising a useful quantum information system is that of scaling up these fundamental architectures to a large number of qubits. To build a large-scale quantum computer, Kielpinski and co-workers [75] proposed a "quantum-charged couple device" (QCCD) architecture consisting of a large number of interconnected ion traps in 2002. This ion-trap device can be constructed by an integrated array of linear RF Paul ion traps, divided into the ion storage region (memory region) and the interaction region for logic operations. Such a device is capable of doing logical operations by generating entanglement between any pair of ions by shuttling the ions out from the storage zone into the entanglement zone, and bringing them back to complete the algorithm [75]. To achieve all this, the QCCD architecture requires arbitrary two-dimensional control of trapped ions that may consist of four key protocols: linear shuttling, corner (or junction) shuttling, separation and recombination. Many ion-trap schemes have since been proposed. These include the use of networks of interconnected ion traps [75], [76], the implementation of segmented trap electrodes and junctions in linear trap arrays such as symmetrical three-dimensional multilayer ion traps [73], [77]–[79] and, in particular, asymmetric planar trap geometries (or surface-electrode ion trap) offering ease of fabrication and true scalability [71], [80]–[85]. The quest to drastically increase the number of trapped ions (qubits) to hundreds or thousands requires new methods allowing for reliable and reproducible construction of more complex ion-trap structures with a high density.

The microfabrication technology offers very promising route towards the realisation of scalable platforms for quantum computing due to several advantages demonstrated in novel microfabricated ion-trap designs. Microtraps can be constructed from various material choices of substrates, metals and dielectrics. In micro- and nanofabrication, the pattern transfer process (e.g. photolithography, e-beam lithography and etching) offers the ability to create arbitrary electrode geometries and small trap dimensions ranging from a micrometre down to nanometre scale. A high resolution process greatly benefits the miniaturisation of critical dimensions (e.g. trap junctions [73], [86], and operation regions [71], [87]). Several novel fabrication techniques have been employed to retain good optical access for experimental operation and detection (e.g. high aspect ratio through-silicon etching for backside ion loading

slots [71], [73], [87], [88], angled backside slots for through-wafer laser access [89], recessed-wire bonding pads [71]. Furthermore, the complexity of electrode wiring in a large-scale ion-trap system can be alleviated using the implementations of vertical interconnect access (via) connections or the integrations of micro optics (e.g. optical fibres [89], waveguide [90], and micro-mirrors [91]) to enhance photon collection efficiency, and control electronics [81] on the same device.

The prospect of building a practical quantum computer underlies many novel designs of the surface-electrode ion traps (SEITs) that utilises fabrication techniques [71], [73], [87], [92] which have the potential benefit of constructing the next generation miniaturised, truly-scaled, and complex quantum-computing devices. This is due to the fact that the ion-trap structures at the sub-micrometre level can be achieved by exploiting photolithographic techniques. Furthermore, structures with complex electrode geometries can be achieved and produced with high precision of specified design patterns with minimal imperfection controlled in fabrication process leading to high performance devices. The implementation of surface-electrode ion traps with microfabrication techniques have presented strong growth and become an active area of research in less than a decade as evidenced in a body of literature.

1.3 Thesis overview

The research work based on the design, optimisation, fabrication, and operation of surface-electrode ion traps (SEITs) towards progress in quantum computing and quantum simulations is presented. The work aims at the construction of a two-dimensional (2D) array of ion traps using the microfabrication techniques. The experimental setup and realisation of the proposed microtraps in two different regimes - (i) ion trapping in ultra-high vacuum and (ii) charged particle trapping in air - are demonstrated. This thesis is constructed as follows:

Chapter 2 introduces the principle of electrodynamic balance for charged particles followed by the description of quadrupole ion traps as an ion storage device and a mass spectrometer. The revolution of ion-trap quantum technology is highlighted. This chapter presents a review of published works on the challenges and prospects of novel ion-trap

geometries associated with the attempt to achieve large-scale ion-trap quantum computing and information processing by exploiting many microfabrication techniques. In addition to investigating ion traps for charged particle trapping, experimental demonstrations and techniques used in recent surface-electrode ion traps are benchmarked.

Chapter 3 describes the relevant theories of ion trapping in quadrupole fields. The motion of trapped ions in quadrupole ion traps is first derived by a full treatment involving the Mathieu's equation and stability parameters followed by the pseudopotential approximation. A subsequent topic presents the derivation of motion of charged particle in air associating with drag force by Stokes' law and drag effect on the stability of the Mathieu's equation.

Chapter 4 provides analytical and numerical models for surface-electrode ion traps to gain detailed insight of operation and trapping mechanisms of ions and microparticles in the proposed traps including i) a surface-electrode ion trap with Y-shaped junction and ii) a two-dimensional (2D) hexagonal lattice trap. The use of computer modelling software called "*bemsolver*" to simulate electric potentials in the physical trap geometries and Mathematica computations to calculate trap properties, i.e. pseudopotential, trap depth, secular frequency, trap point and escaping point, are presented. The determination of damping effect to the stability parameters when microparticles are suspended in a quadrupole ion trap at atmospheric pressure (in air) is also described.

Chapter 5 describes the overall fabrication process flows used to construct the microtrap prototypes on Silicon-On-Insulator (SOI) substrates. The full descriptions of the fabrication processes including wet chemical etching, deep reactive ion etching (DRIE), hydrofluoric acid (HF) etching, and inductively coupled plasma (ICP) etching is also provided. A subsequent improvement of the fabrication processes aims to reduce numbers of steps and to eliminate the surface damage, defects and contamination that may arise during an initial evaluation process. The effort is employed to develop a more mature process with greater device quality.

Chapter 6 provides a brief introduction to the construction of the ion-trap experimental apparatus (e.g. ion sources, vacuum system, optical system, trap electronics and control system). The experiment results demonstrate the fundamental operations of ytterbium ($^{174}Yb^{+}$)

ion trapping and rudimentary shuttling in the fabricated 2D hexagonal lattice trap. The electrical characterisation of surface flashover in a vacuum is investigated. In addition, the ability to control ion lattice distribution and to deterministically introduce defects into the ion lattice are demonstrated.

Chapter 7 and 8 are devoted to the experimental setup and realisations of a 2D hexagonal lattice trap in ambient air including a reliable trapping and three-dimensional (3D) control over the glass microspheres' motion (i.e. a 2D shuttling between lattice traps and levitation to different trap heights by means of a secondary AC electric field). In addition, the experiments of the electrical breakdown test, the secular frequency measurement and the charge-to-mass ratio (Q/m) approximation are presented.

Chapter 9 summarises the key results, accomplishments and concluding remarks from this research work. In addition, a future research recommendation based on the knowledge and experience gained from this research work is discussed.

Chapter 2

Radio frequency (RF) Paul traps in quantum computation

In the efforts toward the realization of a large-scale ion-trap quantum computer based on the fundamental concept of Cirac-Zoller [50] later extended to a proposal of quantum charge-coupled device (QCCD) architecture [75], the ion trap has become a promising scalable platform for quantum computing, and is being actively researched. The implementations of linear radio frequency (RF) or "*Paul*" trap arrays have been successfully demonstrated of achieving scaling up of the numbers of quantum bits (qubits) and performing basic quantum operations. This chapter provides a brief introduction to the importance of ion traps for quantum computing (QC) and quantum information processing (QIP) in Section 2.1. In scaling up ion traps to host a large number of qubits, the generic evolution of RF Paul traps from conventional ion-trap geometries (i.e. hyperbolic surfaces) to the new generation of 2D arrays is presented in Section 2.2.

Microfabrication technologies and material sciences have become key enables and drivers for making miniaturised and scalable ions traps become realistic for future quantum computers. In this respect, much of the literature review in Sections 2.3 and 2.4 has been devoted to the various fabrication techniques, trap operation and performance assessment of symmetrical multi-layer traps and asymmetric ion traps (also called surface-electrode ion traps), respectively. In addition to basic ion-trap operations, the levitation scheme by a shift of the RF nil point (i.e. the minimum of the RF potential or the position of a trapped ion) is outlined in Section 2.5.

2.1 Radio frequency (RF) Paul traps

Since the first demonstration of charged particle trapping in RF quadrupole fields in the early 1950s, quadrupole trap technology is still in widespread use not only in ion mass spectrometry and aerosol research but also in the substantial progress towards ion-trap quantum information processing (QIP). With the combination of the basic technology for trapping and cooling ions, scientists have used trapped ions for storing quantum information (qubits) and demonstrated theoretical key concepts [38], [50], [52] and building block of quantum computing methodologies and architectures such as a quantum charged-coupled device (QCCD) architecture proposed by Kielpinski et al. [75]. There have been many pioneering works being done both theoretically and experimentally by several ion-trap research groups around the world attempting to characterize this technology and its need to make a quantum computer a reality in near future.

The implementation of the basic quantum-computation elements, quantum bits (or "*qubits*"), remains a technical challenge. Several physical realisations of qubits have been proposed. One of the most promising approaches is based on storing each qubit in the electronic state of an ultra-cold trapped ion which is manipulated by laser irradiation, as proposed by Cirac and Zoller [50] in 1995. Furthermore, the ion-trap scheme satisfies the basic requirements for a quantum computer as outlined by DiVincenzo [93] in 2000:

(1) A scalable physical system with well characterised qubits.

(2) The ability to initialise the state of the qubits to a simple fiducial state.

(3) Long relevant decoherence times, much longer than the gate operation time.

(4) A universal set of quantum gates (e.g. single-qubit rotations and the controlled NOT gate (or CNOT)).

(5) A qubit-specific measurement capability.

(6) The ability to interconvert stationary and flying qubits.

(7) The ability to faithfully transmit qubits between specified locations.

Most of these requirements have been demonstrated experimentally over the past decades. More recently, the significant progress and outstanding challenge is the scaling of trapped ions to hundreds or thousands of qubits and beyond. There are indeed many atomic ion trap architectures that have been proposed for the realization of large-scale quantum information systems [52], [75], [94]–[96] and quantum simulations [72], [97]–[100]. In the quest for greater trap efficiency, it is necessary to operate with arrays of many ions which can be made to interact with one another in different combinations according to the requirements of any particular algorithm such as quantum gate operation requiring ion separation and combination or a two-dimensional (2D) movement protocol in order to interchange the position of two ions. One way of achieving the separation and recombination operation is to divide the traps into segments [80], [101]. A 2D movement called shuttling can be achieved in trap architectures having junction structures [73], [78], [86], [102]. Recent works have been successful in demonstrating trapped ions with small number of zones, in the order of 10 so far [102] and controlled entanglement of 14 calcium-ion quantum bits (qubits) [103].

2.2 Geometric evolution of RF Paul traps towards a large-scale quantum computer

The prominent and fundamental idea to use ion traps for quantum computer began essentially with the Cirac-Zoller proposal for a scalable quantum computer based on a string of trapped ions, which was confined in a single trap and interacted with laser beams [50]. This system was considered as a good starting point for quantum operations and was demonstrated experimentally shortly afterward by Monroe et al. [51]. However, manipulating a large number of ions in a single trap presents immense technical difficulties due to the addition of individual ions to the string results in undesired vibration mode, decreased trap strength, and less efficient sideband laser cooling and coherence. Therefore, Rowe et al. [104] considered the implementation of Kielpinski's approach [75] called quantum charge-coupled device (QCCD) architecture to build a simple linear ion trap with control electrode segments that enables the movement of ions between two locations, the separation of ion pairs

in a single trap into two separated traps, and their recombination in a separated zone to complete the algorithm. This was a first step towards a realisation of a multi-zone linear trap where only a small number of ions are confined in the zones that are used for implementing quantum operations.

However, one of the remaining challenges of trapped ion quantum computation is to scale up this physical system to accommodate a large number of qubits. To construct a large-scale quantum computing and information processing, more complex electrode topologies and structures and greater trap efficiencies are desired. Among several RF Paul trap electrode configurations, two approaches have emerged as possible candidates for scaling a large array of interconnected ion traps with more enhanced electrode configurations which are potentially amenable to microfabrication. The original proposal was a symmetric three-dimensional (3D) multi-layer structure with electrodes surrounding the ions (see Figure 2.1(d-e) for a three-layer trap and a two-layer trap, respectively). Since the early 2000's, this geometry has been used to realised interconnected linear traps with segmented electrodes [54, 56, 81] and more complex structures with junctions (i.e. T-junction [102], X-junction [78]) allowing basic quantum operations.

While multi-layer traps which are considered as a near-ideal 3D geometry of a conventional Paul trap (four-hyperbolic rods, see Figure 2.1(b)) offer a high trap depth and stiff confinement, most multi-layer traps require manual assembly and alignment. This remaining issue can be resolved by the emergence of an asymmetric ion trap also called a surface-electrode ion trap (SEIT) with the trapped ions residing above a planar array of electrodes as shown in Figure 2.1(f). This new ion-trap geometry was proposed by Chaiverini et al. [80] in 2005, and first experimentally demonstrated by Pearson et al. [83] in 2006. The major advantage of the surface-electrode configuration over a 3D multi-layer trap is that it is amenable to microfabrication and relatively simple to scale them up to large arrays since all electrodes lie in a single plane. Later, several achievements of ion-trap-based quantum systems exploiting microfabricated surface-electrode ion traps have been demonstrated. These include the ion separation and recombination process in the segmented traps [80], [101], and the shuttling operation in the junction traps [73], [78], [86], [102]. In a particular

application like quantum simulators, simulations of coupled ion lattices with local control over ion interactions which is most probably implemented in a formation of two-dimensional (2D) trapping geometries [72], [98], [105]–[108] is of particular interest. However, lattice trap arrays cannot be made by placing individual traps next to each other in a sense of scalability because the electric fields generated by individual trap sites can overlap and distort. Therefore the electrode geometries for individual traps must be optimised and designed in complex fashion to generate desired ion-trap arrays as discussed by Siverns et al. [109].

Microfabricated surface-electrode ion traps become intriguing as a promising tool not only for applications in quantum information technology with trapped ions but also for other applications. For example, a planar ring electrode as shown in Figure 2.1(g) which close resemble a "*Paul-Straubel*" trap (a single ring electrode with two parallel metal plates [9], [110]), was also designed and optimised for mass spectrometry [111] and quantum simulations [90], [112]. In the following sections, the efforts which were devoted mainly to the construction of variants of ion-trap configurations (i.e. choice of materials, fabrication methods and techniques) to be suitable for large-scale fabrication along with the advantages and disadvantages based on the experimentally demonstrated trapping performance are discussed in detail. Particularly, the surface-electrode traps and their recent progresses and techniques used for realisation of 1D and 2D arrays of microfabricated ion traps for quantum computation and simulation experiments are also highlighted.

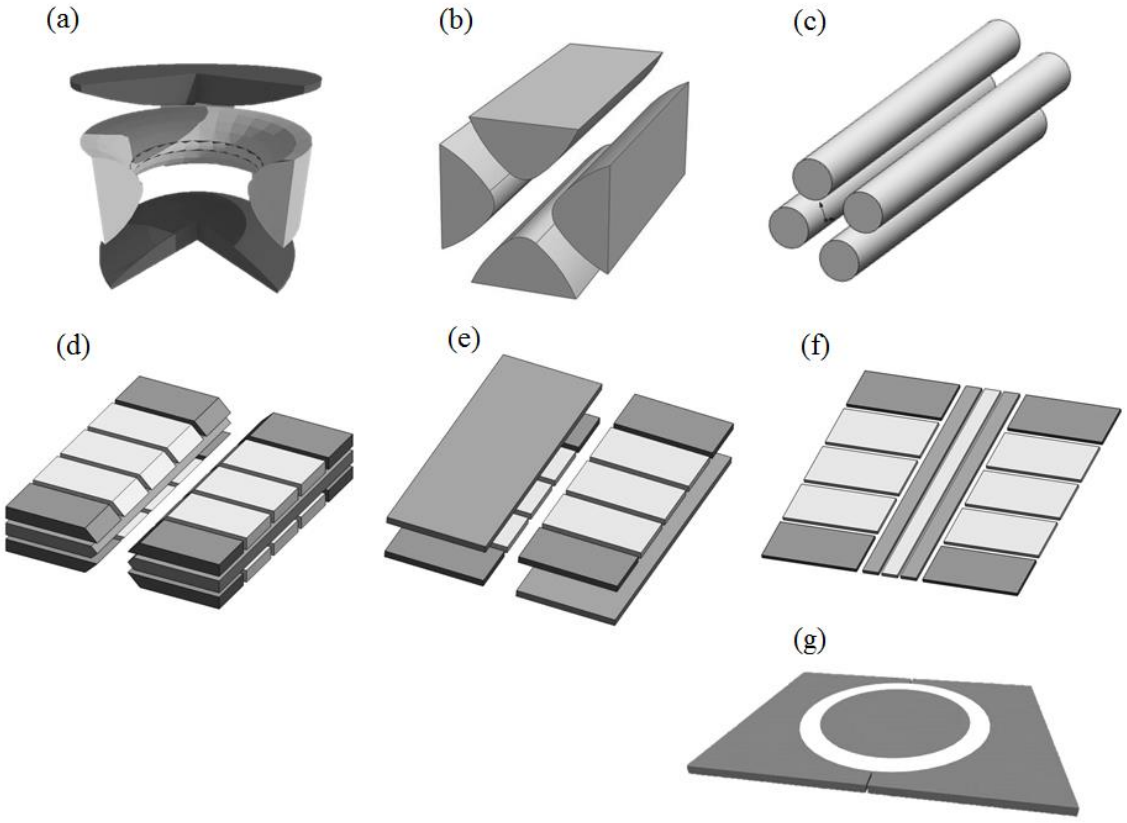


Figure 2.1 – RF Paul ion-trap configurations. (a) A 3D quadrupole trap with a hyperbolic ring electrode and two endcaps. (b) A 2D quadrupole ion trap with four-hyperbolic electrodes (quadrupole mass filter). Both (a) and (b) are the original RF Paul traps [29]. (c) A four-rod trap with circular-shaped electrodes (a typical geometry for mass spectrometry applications). (d) A three-layer linear ion trap [102], (e) A two-layer linear ion trap [104]. (f) A five-wire design of a surface-electrode trap [80]. (g) A single planar ring electrode trap [84]. (Figure modified from ref. [113].)

2.3 Symmetric three-dimensional (3D) multi-layer traps

Symmetric three-dimensional (3D) multi-layer traps can be thought of as a closed form of an idealised linear ion trap geometry (or a four-rod linear trap) because an ion is trapped by symmetrically surrounding electrodes. The difference is that although electrode structures are made of neither hyperbolic shaped electrodes nor four-rod assembly, they now can be implemented using more complex topologies including segmented DC electrodes and interconnected traps with junctions. In 2002, Rowe et al. [104] proposed a two-layer linear ion trap where ions can be stored and moved between two trap zones named *"a dual linear trap"*

(see Figure 2.2). This trap is considered the first implementation of a scalable quantum computing system using a series of interconnected ion traps to demonstrate some of the elements such as the transfer of an ion back and forth between two distinct traps, and the separation of two ions initially held in one trap into two different traps. This trap was constructed from a stack of two 200 μm-thick alumina wafers. The trap electrodes were formed using laser-machined slots and gold traces of 0.5 μm thickness by the evaporation using a shadow mask technique on alumina substrates followed by a 3 μm electroplated gold layer. The outer control electrodes were electrically isolated with a 10 μm gap. The two trap wafers were isolated by 360 μm-thick alumina pieces mounted to a wafer stack holder. Therefore manual assembly and alignment was required for this trap.

The study of the motional ambient heating suggested that the reduction of heating rate by a factor of $\approx$ 100 observed in the dual linear trap compared to the other two traps presented in [114], which have a comparable ion-electrode distance in the range 200-270 μm. The heating rate found in a dual linear trap was approximately 1 quantum per 10 ms at the ion's secular frequency $\omega_z/2\pi = 2.9$ MHz (the ion motional frequency in the axial z direction in an RF trap). Having a complete coating of the electrode substrates with gold and the implementation of shielded electrode prevents the deposition of ion flux on the electrodes over time, resulting in a significant reduction in the heating rate compared to the other two traps with the absence of these two features with the measured heating rate of 1 quantum per 100 μs. This result suggests that lowering heating rate appears to be related to the integrity of the trap electrode surfaces.

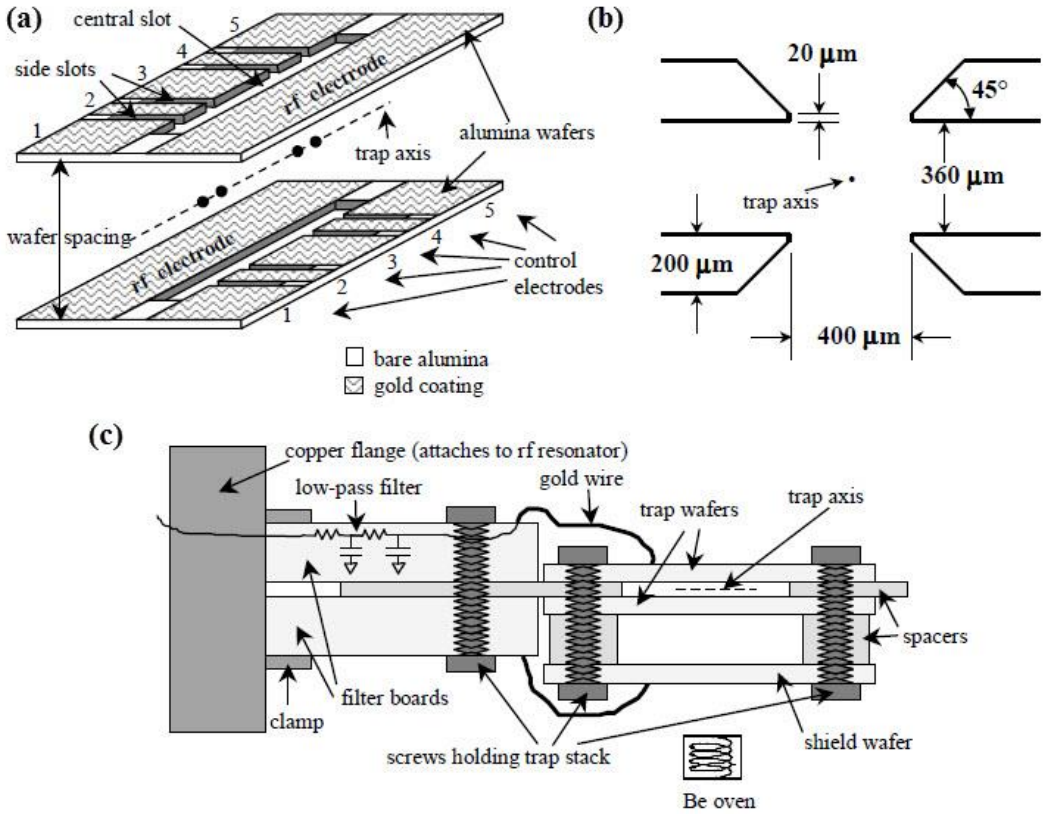


Figure 2.2 – Schematic of a two-layer linear ion trap with double trapping zones. (a) The wafer-stack implementation with segmented control electrodes. (b) Ion-electrode distance is about 270 µm. (c) Trap assembly, electrical connections, and ion loading. (Figure from ref. [104].)

In 2005, Wineland et al. [101] demonstrated an extension of Rowe's work from two-trapping zones to six-trapping zones using a similar process to construct the trap. This work explored several experimental demonstrations of quantum operations associated with the entanglement between ions located in different zones. It was essentially to have relatively narrow control (DC) electrodes to facilitate the separation of a group of ions into subgroups and transfer them to an entanglement zone. This trap confined $^{9}Be^{+}$ ions and showed the optimised separation time of 200 µs with minimal the ion heating of approximately 1 quantum at the secular frequency $\omega_z/2\pi = 3$ MHz. Although increasing gate speed and facilitating ion separation can be achieved by the use of smaller traps, the fidelity of entanglement and ion loss becomes more prone to the increasing of ion motional heating in smaller traps. This is due to the fact that the electric-field fluctuations originating from

the surface of the trap electrodes is much stronger in smaller traps. Therefore, it is important to consider the scaling of the heating rate ($\dot{\bar{n}}$) which is inversely proportional to d^{-4}, the ion-electrode distance (d) [114] and the gate operation time (or gate speed) to the ion's motional frequencies which are inversely proportional to the square of the trap dimensions, $\omega \propto d^{-2}$ [114]. For miniature linear trap arrays with small trap dimensions, it appears that new methods of trap construction are needed instead of the use of laser-machined electrode geometries which have a size limitation to a width of around 20 μm. To overcome this problem, Wineland exploited the advantage of MEMS fabrication techniques to construct a single-zone, two-layer linear ion trap similar to the design presented by Rowe et al. [104]. In his work, the electrodes with features as small as 5 μm were formed in boron-doped silicon wafers using the photolithography and silicon deep reactive ion etching (DRIE) process. This trap, a Si-Glass-Si structure, consists of two layers of silicon anodically bonded via a borosilicate glass spacer. However, the structure required manual alignment by hand with the aid of a microscope. Later, Britton et al. [87] experimentally demonstrated trap operations using the miniaturised trap proposed by Wineland. $^{24}Mg^{+}$ ions were confined in this trap with typical operating conditions at RF potential $V_{RF} = 125$ V at $\Omega_{RF}/2\pi = 67$ MHz. The ion lifetime with laser cooling (a technique to cool trapped ions to a very low temperature by removing momentum from them through the interaction with laser light) was of several hours; lifetime without laser cooling was 20 seconds. This was the first miniaturised two-layer linear trap utilising a commercial silicon substrate with a smaller ion-electrode distance of 122 μm which is approximately half of the previous designs [101], [104]. The interelectrode spacing was significantly reduced to 6 μm. The heating rate of trapped ions in this microtrap was not reported but can be predicted to increase by at least a factor of 16 compared to that of a dual trap according to the d^{-4} scaling law.

Two-layer linear ion traps demonstrated in [87], [101], [104], [114] require manual assembly and alignment of the trap electrodes and the insulator layer. This inherent drawback of multi-layer traps may render some issues more pronounced when scaled the arrays with a large number of interconnected ion traps resulting imperfection from the manual alignment. For these reasons, Stick et al. [77] proposed a GaAs/AlGaAs heterostructure which no longer

needed manual assembly or alignment. The trap shown in Figure 2.3 was fabricated from four alternating layers of two GaAs layers (highly doped 3×10^{18} e/cm^{-3} with 2.3 μm thickness) and two AlGaAs layers (4 μm thickness) which were epitaxially grown on a 200 μm-thick GaAs substrate. The ion-electrode distance was significantly decreased to 30 μm in this trap. The backside-etch removed a 200 μm-thick GaAs substrate for optical access through the chip. The cantilevered GaAs electrodes were formed after a series of dry and wet etch procedures. The electrodes were electrically isolated from each other by an inductively coupled plasma (ICP) etch. Selective wet etch undercut of the AlGaAs insulator layer (~ 15 μm away from the tips of the cantilevered electrodes shown in Figure 2.3(a)) using a hydrofluoric acid demonstrates the benefit of dielectrics shielding by minimising the exposure of insulating surfaces leading to unwanted stray fields near trapped ions.

This trap operated at very low voltage due to the fact that breakdown strength of a 4 μm-thick AlGaAs layer limits the RF voltage that can be supplied to the trap. The AC voltage applied between top- and bottom-cantilevered electrodes was 11 V at RF drive frequency $\Omega_{RF}/2\pi = 14.75$ MHz prior to breakdown, but the static DC voltage up to 70 V was applied to the trap without observing breakdown. For $V_{RF} = 8$ V at $\Omega_{RF}/2\pi = 15.9$ MHz, the axial secular frequency ($\omega_z/2\pi$) and radial secular frequencies ($\omega_{x/y}/2\pi$) were measured to be 1.0 MHz and 3.3-4.3 MHz, respectively. The stability parameter q of 0.62 and the trap depth (a minimum energy required to trap ions) of 0.08 eV were reported. The measured heating rate along the axial dimension was also high at $1.0 \pm 0.5 \times 10^6$ quanta per second. This corresponded to a resonant electric field noise level of 2.0×10^{-8} (V/m)^2/Hz. The source of the observed heating is unclear but may be related to several factors associated with fluctuating patch potentials on the electrode surface, the mechanical motion of the cantilevered electrodes to the ion, and the interaction between atomic ions and solid-state materials used which were new to ion trap application; this needs further investigation. Nevertheless, the major advantage of a doped gallium arsenide (GaAs) heterostructure is the elimination of manual assembly needed in the previous designs. In addition, the selective undercut of an insulator layer in this trap also provides an effective shielding of the dielectric material from the trapped ions.

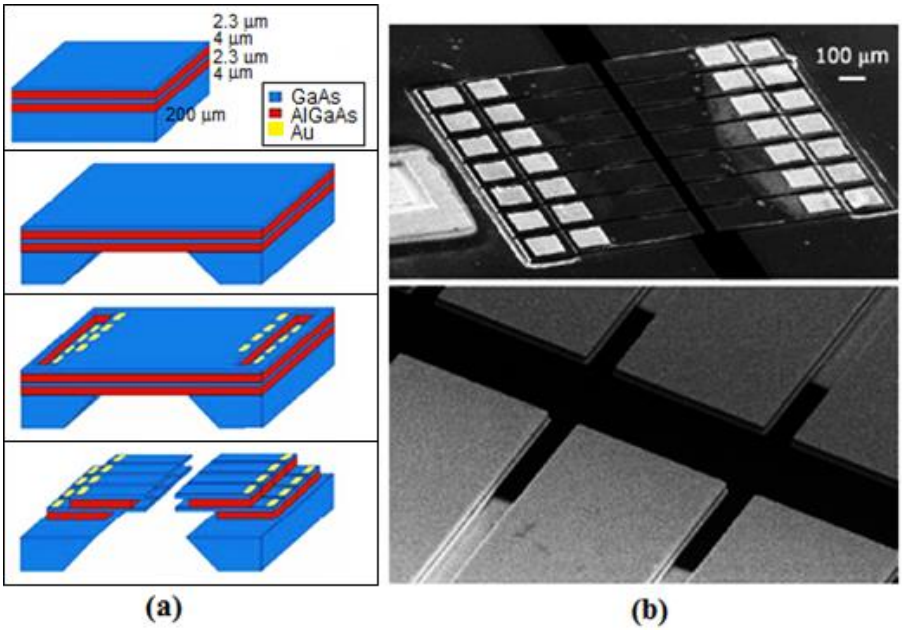


Figure 2.3 – A GaAs/AlGaAs heterostructure trap. (a) Schematic of the fabrication process of four alternating AlGaAs and GaAs epitaxial grown layers on GaAs substrate. (b) SEM images of the GaAs/AlGaAs trap chip with seven-axial segments (28 DC electrodes). Inset shows a close-up image of the central trap region. (Figure from ref. [77].)

Another approach that requires no manual assembly was called a planar silica-on-silicon technique, developed by Brownnutt et al. [79]. The trap electrodes which were constructed as shown in Figure 2.4 are of gold-coated silica and spaced by a highly doped silicon layer in a monolithic structure. The fabrication processes include thermal oxidation of Si wafer on both sides, inductively coupled plasma (ICP) etch of SiO_2, evaporation of gold on SiO_2 with lithographic patterning of electrode structures, series of isotropic wet etch of silicon to create open trench and selective undercut, and wet etch of the gold between the DC segments. Furthermore, the non-standard technique called "*Shadow evaporation*" of gold to coat the edges and surface of SiO_2 near the undercut similar to the technique used in Rowe et al. [104] was presented. This microfabricated trap appears to have specific advantages over the high aspect-ratio GaAs trap which is the first monolithic microfabricated trap demonstrated by Stick et al. [77]. For the same conditions (trap size d = 30 µm, RF voltage V_{RF} = 8.0 V, trap drive frequency $\Omega_{RF}/2\pi$ = 15.9 MHz), apart from the spacer thickness (40 µm-thick silicon) which is ten times thicker than that of the GaAs trap (4 µm-thick

AlGaAs), the silica-on-silicon trap has the trap depth of 0.60 eV which is seven times deeper than that of the GaAs trap (0.08 eV). In addition, it used metallic electrodes and a low-loss dielectric, resulting in significantly lower heating. The surface breakdown was also reported at the maximum AC electrical field of 5 V/μm of the RF-DC electrode gap of 50 μm which was sufficient for normal operating conditions (≤ 250 V) used in the experiments. Together with trap structural design, material properties and the process of silica-on-silicon fabrication technique, this trap has proven its scalability and efficiency to create ion trap on a chip containing large 2D arrays of trapping segments with many qubits. In this work, this suggests that the ion-electrode distance down to 90 μm can be achieved using the silica-on-silicon fabrication techniques proposed, and even in relatively small ion-electrode distance, about 20 μm is possible with further process development.

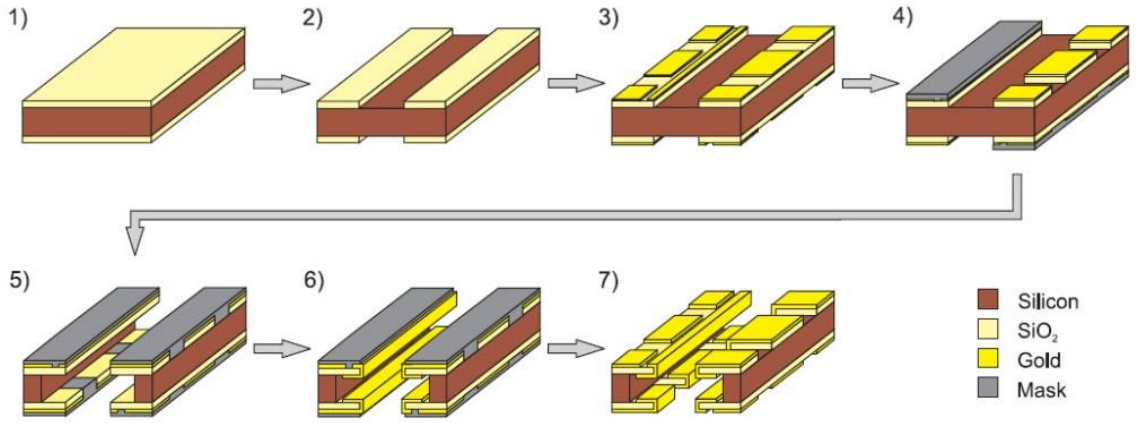


Figure 2.4 – Schematic of the fabrication process of monolithic ion trap chip based on planar silica-on-silicon techniques. (1) Thermal oxidation of Si wafer (15 μm-thick SiO_2 on both surfaces, (2) ICP SiO_2 etch to create a central slot, (3) Evaporation of gold electrodes on SiO_2, (4) ICP SiO_2 etch of to create segmented DC electrodes, (5) Isotropic wet etch of Si to create a cantilever structure, (6) "*Shadow evaporation*" of gold on the exposed SiO_2, and (7) Wet etch of the gold between the segmented DC electrodes and a further wet etch of Si. (Figure from ref. [79].)

For two-dimensional (2D) separation/recombination and shuttling protocols that transport ions between interaction zones through junction, a three-layer linear trap array with T-junction using thin laser-machined polished alumina substrates was first demonstrated by

Hensinger et al. [102]. A construction of the 24-control electrodes on the top and bottom substrates was achieved by photolithography and wet-chemical etching. The metal electrodes were formed by depositing 15 nm of titanium followed by 400 nm of gold on an alumina substrate using the electron beam evaporation. The three substrates formed in "*Control-RF-Control*" sequence seen from the cross-sectional diagram of this trap in Figure 2.5(c) were separated by thin alumina spacers and were held together via rectangular alumina mount bars as shown in Figure 2.5(a). The T-junction trap consists of 11-trapping zones, a-k, located at the trap centre - see Figure 2.5(b). Laser-cooled cadmium ($^{111}Cd^{+}$) ions were confined in this T-junction trap with the ion lifetime of several hours.

For the shuttling protocol, the RF voltage amplitude of 360 V at $\Omega_{RF}/2\pi = 48$ MHz was applied to the central layer electrode obtaining a transverse secular frequency of $\omega_z/2\pi =$ 5.0 MHz. Three key shuttling protocols consisting of linear shuttling, corner turning, and separation/recombination of two ions were experimentally demonstrated. Linear shuttling and corner-turning operations were reported to attain nearly perfect efficiency of 98% over a wide range of speed. The kinetic energy gain during the corner-turning protocol was estimated to 1.0 eV by numerical simulation. The separation operation appeared to be less efficient compared to the shuttling. The separation time took about 10 milliseconds and carried out with a success rate of only 58%. The separation and recombination achieved a success rate of 82%. The success rate for the whole process of linear shuttling, corner turning, and separation/recombination is 24%, mainly limited by the separation and recombination efficiency which was suspected to a very weak trap during separation and large control electrodes in the separation zone ($\approx$ 400 μm). The optimisation of the control electrode dimension should improve the separation and recombination efficiency.

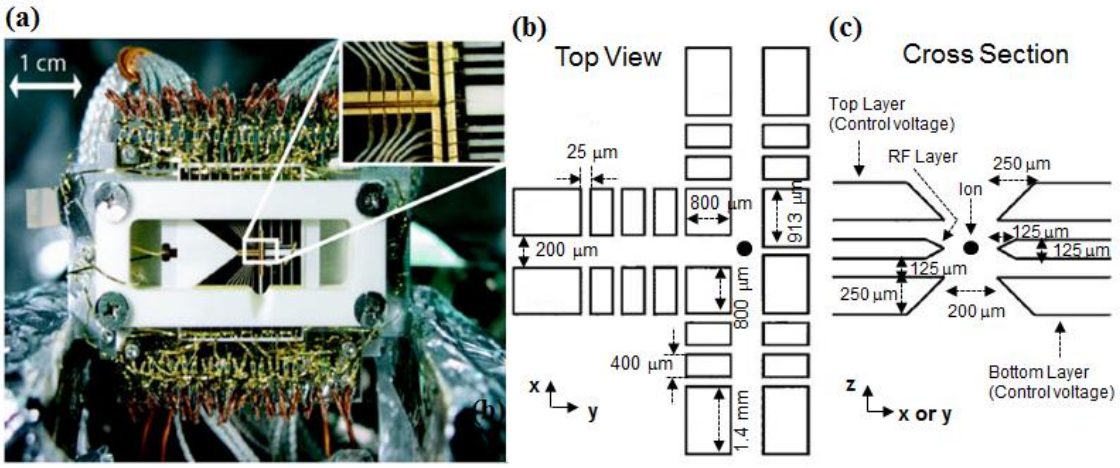


Figure 2.5 – A T-junction trap array with 24 control (DC) electrodes, 11 trap zones. (a) Photograph of the T-junction trap assembly with electrical connections. Inset shows the trapping array near T-junction. (b) Top view of the trap layout from showing the T-shaped central slot of 200 μm and the interelectrode gap of 25 μm. (c) Cross-section view of a three-layer linear trap configuration when look through the trap axis. (Figure from ref. [102].)

Following the success of universal shuttling protocols implemented in T-junction trap with $^{111}Cd^{+}$ ions [102], a two-layer X-junction trap array with many more number of 46-control electrodes and 18-trapping zones was proposed by Blakestad et al. [78]. The X-junction trap also presented a greater success rate of 99% when shuttling $^{9}Be^{+}$ ions through a junction with ion kinetic energy gain less than 10^{-7} eV. The radial confinement was controlled by the RF voltage amplitude of 200 V at $\Omega_{RF}/2\pi = 83$ MHz. With two diagonal bridges forming the X-shaped junction generated by a two-layer electrode design, the RF electrodes were connected across the junction as shown in Figure 2.6. These bridges produced high pseudopotential barriers ≈ 0.35 eV as reported. Unfortunately, high pseudopotential barriers near the junction region makes the confinement at the junction sufficiently weak, and stable ion shuttling through the junction more difficult as a result. Thus the use of narrower segmented control electrodes (~ 100 μm wide) near the junction was suggested.

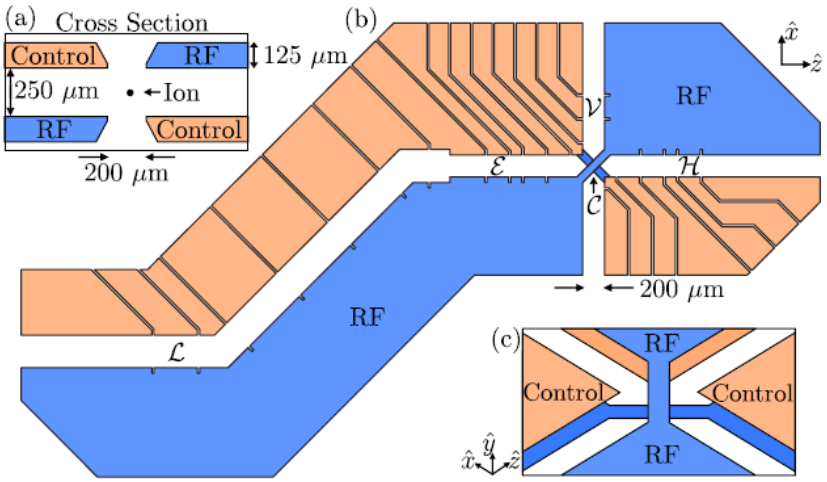


Figure 2.6 – Schematic of the X-junction trap array constructed on two laser-machined alumina wafers with gold-coated electrodes. (a) Cross-section view of a two-layer linear trap with segmented control electrodes. (b) Top view of the trap electrode layout (c) A close-up of RF bridges formed at the intersection. (Figure from ref. [78].)

Even though these symmetrical 3D multi-layer ion-trap arrays apparently offer the advantages of a high trap depth, a stiff confinement, a low RF loss, a shield of the dielectrics and good open optical access, they require the addition of manual assembly and alignment. With this constraint, they are not suitable for scaling to large arrays of microtraps. Moreover, the potential field near the junction expected to exhibit a large variation is rather complicated and highly sensitive to imperfect alignment of electrodes during trap construction. To eliminate the need for manual assembly and alignment, a 3D trap geometry with a scalable fabrication process exploiting a monolithic fabrication techniques was demonstrated in a GaAs/AlGaAs trap [77] and a silica-on-silicon trap [79]. However other technical issues were shown in these 3D monolithic ion-trap chips. For example, the GaAs/AlGaAs trap suffered from a relatively low breakdown voltage and significantly high anomalous heating rate. A customised fabrication process was required in a silica-on-silicon technique. To achieve truly-scalable ion-trap architectures and to facilitate creation of more complex electrode structures, the deformation of a symmetric 3D multi-layer ion trap to an asymmetric ion trap also called a surface-electrode ion trap (SEIT) was proposed by Chiaverini et al. [80] in 2005.

A SEIT configuration which has all electrodes residing on a single plane on a substrate and where the ions are trapped above the trap surface offers a significantly greater simplicity of fabrication but still preserves the basic physics of the required trapping potential (i.e. a quadrupole field) similar to a 3D trap configuration. This newly developed geometry is more amenable to a standard semiconductor and MEMS microfabrication. Due to their promises, the realisations of SEITs have become an active area of research and have seen significant progress made by ion-trapping research groups, which is discussed in the following sections.

2.4 Asymmetric surface-electrode ion traps

An asymmetric ion trap also called a surface-electrode ion trap (SEIT) was first introduced by Chiaverini et al. [80]. This trap is a deformation of the standard 3D quadrupole geometry into a planar geometry that has all the electrodes on a single plane. A linear RF Paul trap consisting of four parallel linear electrodes was deformed by moving one control electrode and one RF electrode onto the same plane of the remaining two electrodes (see Figure 2.7(a-b)). This symmetric "*four-wire*" geometry (RF-control-RF-control) appears to be promising but the implementation of junctions and segmented DC electrodes for shuttling purposes might not be suitable. An alternative approach proposed was a "*five-wire*" geometry with its basic electrode layout shown in Figure 2.7(c). While the centre electrode is maintained at RF ground, the outer control electrodes which can be segmented for the axial confinement are used for DC compensation. The RF voltage is applied at the two RF electrodes to provide the radial confinement. In a five-wire surface geometry with equal width of two RF electrodes, the principal axes of the trap using control fields are perpendicular and parallel to the plane. To efficiently laser-cool the trapped ions along all three principal axes of motion, each principal axis is required to be angled with the electrode plane since the laser beam orientation can only have a small angle with respect to this plane. The rotation of the principal axis in a symmetric five-wire design can be done by breaking its symmetry either by DC voltages or by geometry. With the latter approach, the principal axes can be tilted using unequal width of RF electrodes. Previous ion-trap designs such as T-junction or X-junction traps employing

a 3D multi-layer structure can also be adapted to the five-wire planar design. The difference is that the ions are confined above the electrode plane instead of being symmetrically surrounded by electrodes. A SEIT structure offers a simple fabrication with only a few fabrication steps required and added-benefit for rapid turnaround time in both design and fabrication process.

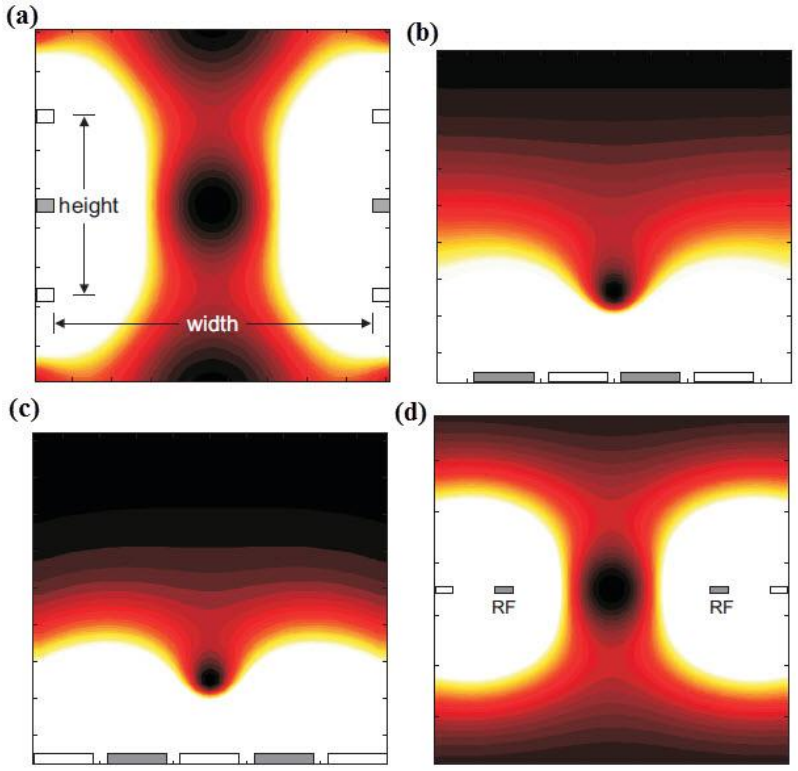


Figure 2.7 – Pseudopotential plots of linear ion-trap geometries with the local potential minimum (black dot). RF potential is applied to the grey electrodes and the white electrodes are held at RF ground. (a) A three-layer structure. (b) A four-wire planar geometry. (c) A five-wire planar geometry. (d) A planar geometry with the local minimum in the electrode plane. (Figure from ref. [80].)

Planar electrode geometries can be made by patterning metal onto an insulating substrate using standard semiconductor technologies or various MEMS-based microfabrication methods. Since the fabrication procedure for the planar trap is straightforward, electrical circuitry elements or optical systems may be integrated directly on the trap chip [81], [90]. Another potential benefit of a surface-electrode configuration is that the location and strength

of the trapping region may be altered by varying the electrode structure in one plane only. However, a SEIT design has an inherently lower trap depth by a factor of approximately 30-200 (depending on electrode geometries) than those of a conventional quadrupole trap with a similar trap size [80]. One possible solution is the integration of a loading or reservoir trap of a more standard design containing deeper trap depth to help in the initial ion-loading process [83]. It was also found that the trap depth was increased by adding a planar top electrode with a 100 V DC bias over the trap which was primarily used for shielding stray fields from the trap. Although current trap designs must be reduced in size and have dense arrays of trapped ions to accommodate large numbers of qubits, there may be an ultimate limit to how small linear RF Paul traps can be made.

Chaiverini explained that scaling beyond an ion-electrode distance (d) of tens of nanometres may become impossible due to the reduced trap depth, even using a conventional quadrupole trap [80]. However a surface-electrode ion-trap configuration can be used to produce a broad range of geometries such as multiplexed linear traps with segmented DC electrodes [81], [87], junction traps [86], planar point traps [89], [90], [112], [115], multiple-ring electrode traps [111], and two-dimensional (2D) arrays of lattice traps [83], [107], [108], [116]. SEITs have been widely used in many applications in quantum computation and information processing, quantum simulation, and mass spectroscopy. In this regard, the implementation of surface-electrode configurations that has been carried out in much recent ion-trap research is further discussed in detail. This area of work has been thriving over the last decade and has led to the innovative development of microfabrication techniques. Advances in various surface-electrode ion trap architectures and fabrications are fundamentally motivated by one common goal of building a scalable, high-speed, and robust ion-trap system in which a quantum computer can be realized. Choices of fabrication processes for microfabricated ion-trap chips in various applications were extensively reviewed in Hughes at al. [117].

2.4.1 Printed circuit board structures

A surface-electrode ion trap (SEIT) can be simply built using a low-cost printed circuit board (PCB) material. Besides its low cost and broad availability of the PCBs, the main benefit of a PCB trap is the ease of fabrication in building-up prototypes with fast turnaround times based on a standard PCB manufacturing. The PCB structure yields a great potential for scaling and optimising microstructural trap arrays with various combinations of trap geometries, dimensions and materials. To construct a SEIT with a PCB, it is important to choose a PCB with the right characteristics for a fundamental ion-trap operation (i.e. a high voltage RF signal at a few MHz and a vacuum environment). This includes a high breakdown voltage, a low RF loss tangent, and an ultra-high vacuum compatibility. A single-layer PCB process is suitable in fabricating linear electrode geometries [83], [84], [118] but more complex topologies with isolated electrodes [107], [108], [112] require a two-layer PCB process to connect trap electrodes with the external power sources without blocking optical access for lasers. Next, selecting a suitable metal-coated PCB is also important and most published works use copper because commercial PCBs are generally pre-coated with a thick copper layer (15-18 μm). In addition, a thin-metal plating (a few micrometres) such as tin or gold coating on the surface of copper traces can prevent oxidation or corrosion on copper. There are several vacuum PCB substrate types such as FR-4 epoxy glass [111], GML-1000 [83], Rogers 4350B (a microwave laminate with better vacuum compatibility than GML-1000) [84], [112], [118] that were used for fabricating surface-electrode traps.

The advantage of PCB-traps is a fast and reliable fabrication. However, PCB processes commonly allow for specifically minimum feature size and drill size, typically ranging within the order of tens to hundreds of micrometres. For example, in some cases, the drill size can be varied from < 0.1 mm [118] or even larger at 0.5-1.0 mm [83], [84]. Having the copper traces and gaps of greater than 50 μm limits further success in miniaturisation of one-dimensional (1D) or two-dimensional (2D) arrays of ion-traps. For instance, a 2D ion lattice with an ion-ion separation in order of few tens micron is required to create a strong Coulomb interaction and to be capable of performing quantum simulations [107], [115], [116]. Another disadvantage found in a PCB-trap is charging effects inducing a build-up of stray charges on the dielectric

surfaces between the electrode strips that may degrade the performance of the trap. Such unwanted stray fields will push trapped ions away from the nil of the RF trapping field, hence, the ions experience the excess micromotion which causes decoherence in the system and degrade the fidelity of the quantum operations. Normally the Cu-electrodes are several micrometres in thicknesses ($\approx$ 15 μm) and the interelectrode spacing ranges from 50-850 μm depending on the milling process. Because of a rather large interelectrode spacing, these slots can be milled into the substrate [83], [84], [113] to avoid charge effects by removing the exposed dielectrics near the trap region. Another solution is to have sufficiently large ion-electrode distance but this also decreases the trap depth.

Pearson et al. [83] demonstrated two types of surface-electrode ion traps constructed from PCB substrates. The trap configurations consist of multi-zone linear ion traps formed in four straight arms joined at the intersection (Figure 2.8(a)) and a two-dimensional Paul trap array (Figure 2.8(b)). The electrodes are tin-coated copper, and the substrate is GML-1000 (a microwave laminate). The first trap is based on a symmetric five-wire design with equal electrode width (two RF rails and a centre control electrode) of 1.27 mm and the interelectrode spacing of 0.89 mm. The ion height (ion-electrode distance) is approximately 1.7 mm from the numerical computation. The second trap is a 2D lattice trap geometry with a lattice spacing (ion-ion separation) of several millimetres. Although the prototype traps were not fabricated with the optimum relative sizes of the trap electrodes due to the limitation in the PCB technology as explained above, the multi-zone linear ion trap with four arms was proven to be capable in demonstrating the fundamental movement operations required in multiplexed trap architecture including a linear shuttling, corner and junction shuttling, a separation/recombination of ion pairs. Since SEITs have very shallow trap depth in the order of 1% of that of multi-layer traps with comparable dimensions, an ion-loading mechanism is very important. In this regard, a four-rod Paul trap was used as a reservoir of ion in the loading zone because of its deeper trap depth. Pearson used these microtraps to confine charged aminopolystyrene spheres of 0.44 μm in diameter in a rough vacuum environment. With a similar design of the 2D trap arrays shown in Figure 2.8(b) scaled to

smaller lattice spacing (ion-ion distance) well below 100 μm, a 2D array of trapped ions can be satisfactory for quantum simulation schemes described by Porras and Cirac [105], [119].

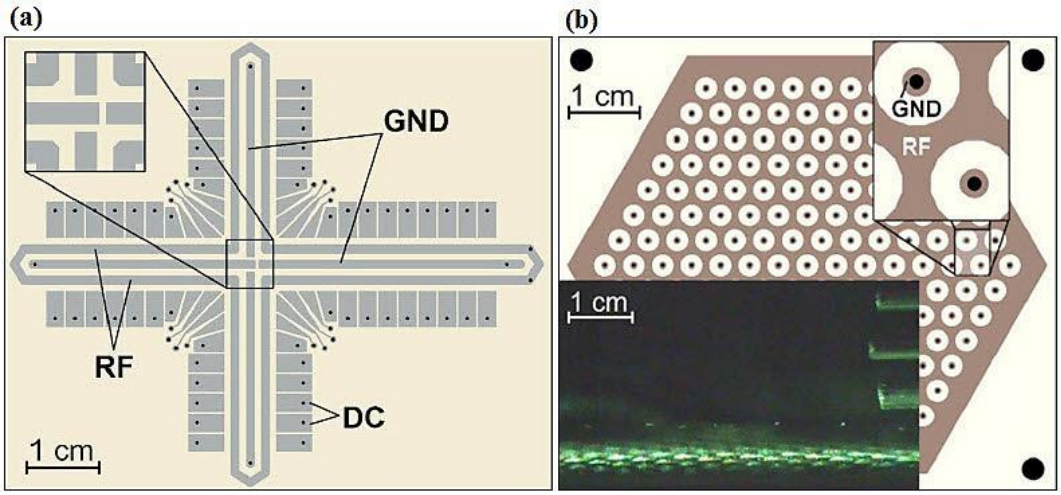


Figure 2.8 – A surface-electrode ion trap fabricated on a printed circuit board (PCB) with tin-coated copper electrodes. (a) Top view of a five-wire surface-electrode trap made up of four straight arms jointed at a cross intersection. (b) Top view of a two-dimensional Paul trap array. Bottom inset: Imaging of seven microspheres trapped above a 2D hexagonal lattice trap. (Figure from ref. [83].)

A 4×4, 16-site ion-trap array with addressable RF electrodes called *"Folsom"*, a design of Kump et al. [107], [108], was also made of a PCB technology (a vacuum compatible PCB RO4350b). The electrodes were formed with 18 μm-thick Cu, electrically isolated by a 50 μm gap using an etching process, and then plated with 10 μm of gold. This trap structure consists of 16 circular trapping sites, 400 μm in diameter and 1.5 mm away from each other. The trap was designed to determine the functionality of addressable RF electrodes between the trapping sites in transporting pairs of ions into a close proximity, which in turn meant that the ion-ion distance was dynamically reduced. Another useful feature of the addressable, tuned RF electrode was to rotate the principal axes of motion that enables laser cooling in all three dimensions. The use of separate adjustable electrodes (having isolated electrodes) requires vertical interconnect access (via) to be integrated into the electrode structure. For this reason a PCB technology with two layers was chosen where the top side is the trapping electrodes

and the bottom is for fan-out, allowing the electrodes to be connected to the external electronics. The experiment was conducted in air using the first prototype, a 2×2 addressable trap array, using dust particles. The main aim was to characterise the trap performance in comparison with the numerical simulation. Through the optimisation, the next generation trap comprising a 16-site ion-trap array with tuneable RF electrodes was experimentally demonstrated as shown in Figure 2.9. A cloud of laser-cooled $^{40}Ca^{+}$ ions was initially confined approximately 400 μm above the surface with an applied RF voltage of approximately 210 V at $\Omega_{RF}/2\pi = 10.7$ MHz resulting in the radial secular frequency $\omega_{x,y}/2\pi = 680$ kHz. The laser-cooled ion lifetime was approximately 10 minutes. The shuttling scheme was investigated by reducing the amplitude of RF voltage (same phase as the initial trapping) applied to the adjustable RF electrode. Reducing the applied RF voltage by about 5 dB, a pair of trapped ions in two distinct traps connecting to the adjustable RF electrode was displaced approximately 40 μm in either x or y direction. The laser-cooled ion lifetime was only a few seconds during the shuttling operation. This was attributed to variations of cooling power over the shuttling range and the excess micromotion due to the phase difference between the primary RF electrode applied to the circular-trapping electrode and the adjustable RF electrode [112], [120]. One particular interesting characteristic of this trap is the need for a negative DC voltage to be applied to the circular-trapping electrodes to maintain stable trapping. Beginning with -1 V at the initial trapping, more strongly negative DC voltage was required up to -6 V over the course of the one-year experimental period. The main issue of this trap was a significantly high ion heating of 2.5 K/ms corresponding an electric-field noise level of $\approx 5.0 \times 10^{-8}$ $(V/m)^2/Hz$ which was much larger than the anomalously high heating rate of the GaAs/AlGaAs trap (approximately $1 \pm 0.5 \times 10^{6}$ quanta per second corresponding an electric-field noise level $\approx 2.0 \times 10^{-8}$ $(V/m)^2/$ Hz) described earlier. The authors suspect that one potential cause of significantly high heating rate in this trap is related to the technology used to construct this trap. Importantly, the study of ion-motion heating reported by Kumph et al. [108] offered the first data obtained from a gold-plated-on-copper PCB array trap since the investigation of heating effects in a PCB trap has not been reported to date.

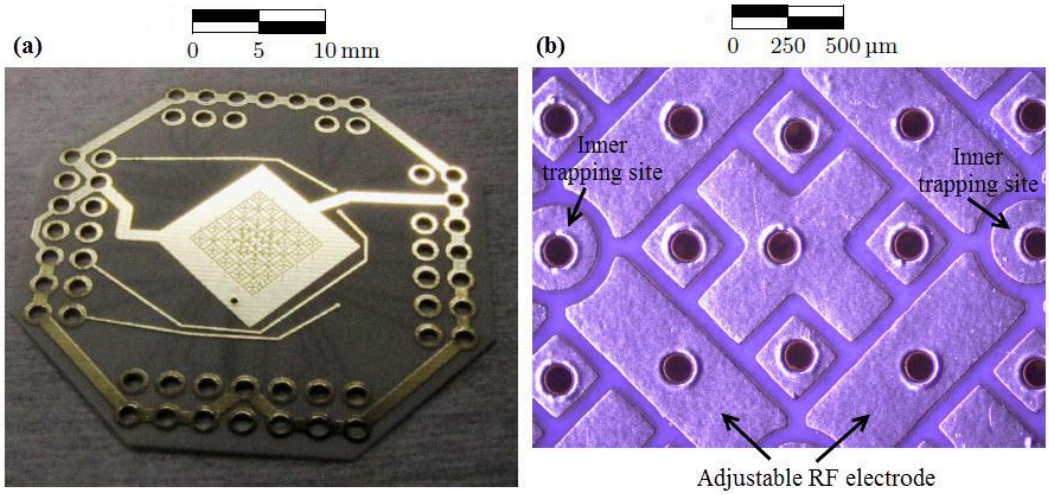


Figure 2.9 – A 2D array of ion traps called "*Folsom*" consisting of 16 circular trapping sites. (a) Photograph of the "*Folsom*" trap with gold-plated-on-copper electrodes fabricated on a PCB material. (b) A close-up image of the centre electrode structure after plating with 10 µm of gold. The inner 2×2 array has individually adjustable RF electrodes between trapping sites (Figure from ref. [108])

2.4.2 Monolithic structures

Wineland and Britton [82], [101] presented a micrometre-scale ion trap fabricated from a bulk boron-doped silicon substrate using MEMS fabrication techniques. The electrodes were formed by a photolithographic patterning and Si etching using DRIE (Bosch process). This trap required no additional metallisation process. However, the trap's configuration requires a structural support by anodic bonding of the silicon wafer to a glass substrate (a 7070 glass substrate) resulting in the cantilevered silicon electrodes as shown in Figure 2.10. An absence of insulator layer at the direct line of sight of trapped ions benefits for a reduction of RF fields penetrating into the glass layer which may create unwanted surface charges. With a 100 µm-thick silicon substrate and a 5 µm interelectrode gap, the ratio of the ion height to interelectrode gap obtained from this trap is sufficiently large to minimize the stray field effects. This trap achieved confining of 12 ions in a linear chain with a relatively strong axial component of the RF pseudopotential. Nevertheless the heating rates of trapped ions were not reported in this study.

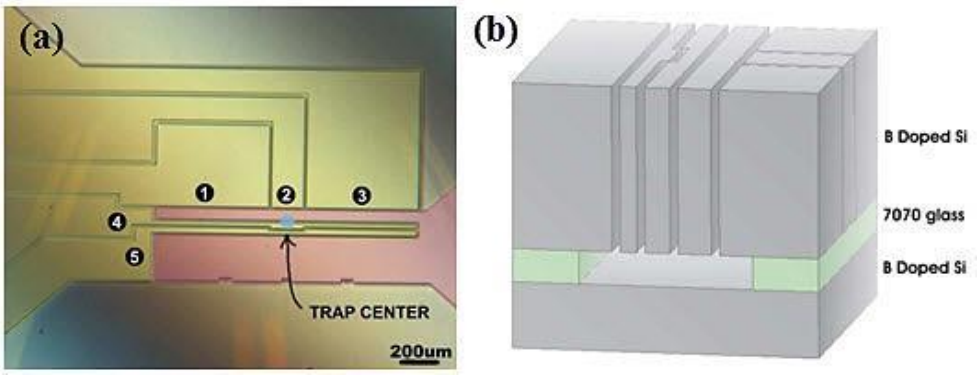


Figure 2.10 – A surface-electrode ion trap fabricated from a bulk silicon. (a) False-colour microscope image of the trap structure from top view (yellow = DC/GND electrode, pink = two RF rails). (b) A cross-section diagram shows a structural support of the top silicon electrodes and the silicon substrate by anodic bonding a 7070 glass substrate. (Figure from ref. [82], [101].)

2.4.3 Conductive structures on insulating substrate

Conductive trap electrodes can be simply formed on top of an insulating substrate. From this literature review, there were three different techniques have been commonly used to fabricate the SEITs including i) metal wet etch [85], ii) thick metal deposition/electroplating followed by wet etch on a seed-layer [81], [121], [122], and iii) thin metal deposition with a lift-off process [90]. The fabrication is straightforward based on standard MEMS fabrication. This trap structure offers a wider variety of choices of low RF-loss insulating substrates (e.g. quartz, fused silica, sapphire, Pyrex, alumina ceramic) and noble conductive electrodes (e.g. gold, silver, copper, aluminium). A combination of material choices and ease of fabrication makes the structure more attractive and amenable to complex electrode geometries. However, the problem of charging effects on the exposed dielectric substrates exhibit in this trap structure but is considered to have less impact compared to those of PBC-traps. This is due to the interelectrode spacing being reduced to as small as few microns in size using the photolithography process. In this structure, the ion height was decreased to less than 100 μm while the heating rate remains sufficiently low, as reported in Seidelin et al. [81].

In fact, the microfabricated SEIT was first demonstrated by Seidelin et al. [81] in 2006 using a conductive structure on substrate technique. A five-wire, one-zone linear trap with gold electrodes fabricated on a fused quartz substrate was successful in confining individual laser-

cooled $^{24}Mg^{+}$ ions at a low ion height of ≈ 40 μm above the surface. In Figure 2.11, this trap contains a low-pass filter, consisting of a resistor and capacitor, on each control electrode which requires a double photolithographic patterning step. Resistors and traces were fabricated using a lift-off process with metal (Ti/Au) evaporation. Resistors were fabricated directly on the quartz substrate, a low RF loss material. Traces were fabricated on top of the copper seed layer. The 6 μm-thick gold electrodes near the trapping region were electroplated onto the copper seed layer followed by an etching process to isolate electrodes and traces. The use of a thick gold-plating layer near the trapping region is to reduce the impact of the stray charge build-up on the exposed dielectric areas located at the bottom of the electrode gap. Therefore, the higher the coating of the gold electrode, the larger the distance between the trapped ions and the dielectric surfaces. With the operating parameters of this trap, the amplitude of the RF drive potential is approximately 103.2 V at $\Omega_{RF}/2\pi$ = 87 MHz and the static potentials are less than or equal to ± 5V. The numerical simulation of RF pseudopotential suggests the trap depth of 177-193 meV. Experimentally, the secular frequencies of trapped ions are about 2 MHz and 17 MHz for the axial and radial confinements, respectively. The author suspects that the cause of the heating rate of 4.8 ± 0.4 quanta/ms was from Johnson noise [114] in the resistance of the built-in RC filter and anomalous heating but it was thought to be sufficiently small for high fidelity quantum operations [123].

Another five-wire surface-electrode design constructed using even simple fabrication process with a single-step etch was proposed by Labaziewicz et al. [85]. This trap was fabricated on a single crystal quartz substrate, a high thermal conductivity material at cryogenic temperature. The electrode layers were formed by 10 nm titanium (Ti) as an adhesion layer, followed by 1 μm silver (Ag). After the photolithography, the exposed areas were etched away using NH_3OH:H_2O_2 Ag etch, followed by HF Ti etch. The microtrap operated at an applied RF voltage of 250 V at $\Omega_{RF}/2\pi$ = 26 MHz. The ion height in this trap is about 150 μm above the electrode surface. In Figure 2.12(b), the imperfection geometry from the etching process with multiple sharp points at etched side-walls induced emitting electron when applying a voltage > 100 V, resulting in stray electric fields. To smoothen rough

electrode sidewalls, the trap was annealed in a vacuum oven at 10^{-5} Torr, at 720-760 °C for one hour. The high temperature was for reflowing the silver. As the result, no field emission points for voltages up to 750 V across a 10 μm-wide gap was observed on the annealed trap as shown in Figure 2.12(c).

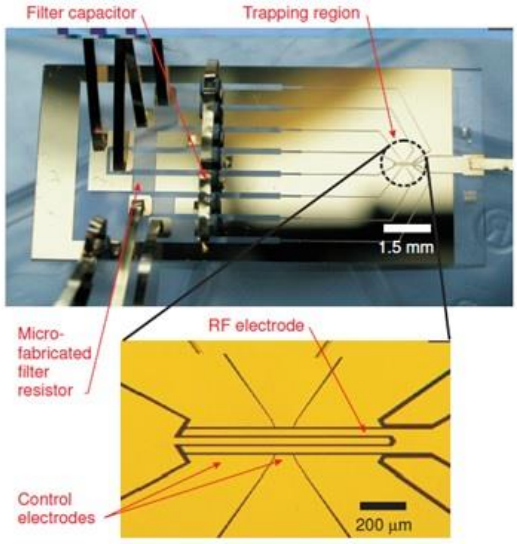


Figure 2.11 – A five-wire, one-zone surface-electrode trap chip with integrated electronics components. The 6 μm-thick gold electrodes were fabricated on a fused silica substrate. Inset is a close-up image of a single trapping site with segmented control electrodes. (Figure from ref. [81].)

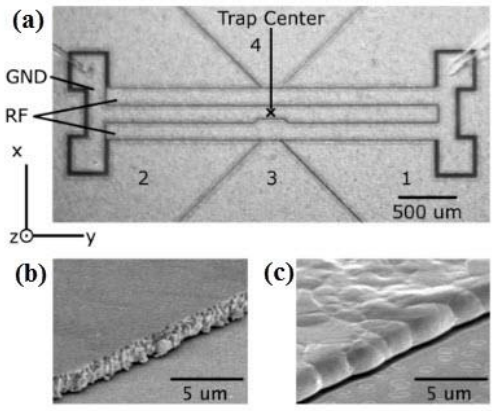


Figure 2.12 – A five-wire, one-zone SEIT fabricated on a quartz substrate with Ti/Ag electrodes. SEM images at (a) the trap centre, (b) the trap electrode sidewall before annealing, and (c) the sidewall after annealing at 760 °C for 1 hour, to improve a rough edge after metal-wet etching. (Figure from ref. [85].)

Unlike other five-wire SEITs with asymmetric RF electrodes rotating the principal axes of the trap, Allcock et al. [121], [124] proposed a new method, a "*six-wire*" design. Splitting the central axial control electrode located in between two RF electrodes in turn creates a six-wire SEIT but retain the effective form of quadrupole field as in the case of conventional RF Paul traps. The electrode layout is shown in Figure 2.13(a). One advantage of six-wire geometry is that it does not require one of RF electrodes to be larger than the other (required in asymmetric five-wire geometry) which can lead to large capacitive coupling and high losses when the trap is driven in RF range. Also the large capacitance and resistance of the RF electrode will degrade the quality factor (Q-factor) of the RF resonator. In this trap, the ions are trapped at 145 μm above the trap surface as shown in Figure 2.13(b). Interelectrode spacing is varied from 5 μm at the centre trap region beneath the trapped ions to minimise the exposed dielectric area, and then increased to 10 μm in the area further away from the trapping region and to 15-25 μm at the peripheral trap. This trap was fabricated on a polished single-crystal quartz substrate similar to that of Labaziewicz et al. [85]. The trap electrodes were structured by first depositing a 15 nm titanium layer as an adhesion promoter followed by an evaporated 200 nm silver seed layer. Then the electrode pattern was transferred using a photolithography with a negative photoresist followed by electroplating of a thick gold layer ≈ 2.4 μm [125]. To complete building-up of trap electrodes, the Ag/Ti seed layer was etched away using a lift-off process. A brief overview on the fabrication step is shown in Figure 2.13(c). Later, Daniilidis et al. [122] demonstrated asymmetric SEITs with various trap sizes (ion-electrode distances) between 125 and 500 μm with interelectrode spacing of 10 μm and electrode thickness of 5 μm. The fabrication process is similar to Allcock's work [121] but differs slightly in terms of choices of materials: i) a sapphire substrate, and ii) an evaporated 100 nm gold layer as a seed layer for the subsequent 5 μm gold electroplating.

The conductive structures on the insulating substrate has also been used in building different SEIT geometries such as the planar ring trap of Jiang et al. [90]. This ring trap integrated an on-chip waveguide for optical detection into the same trap using a double-size standard lithography alignment technique. The fabrication started with patterning electrode

configuration on both sides of a Pyrex wafer followed by the metal depositions of 50 nm Cr and 500 nm Au using an evaporator. To form the completed electrodes, the photoresist was removed by a lift-off process. Then the waveguide fabrication was constructed on a wafer top size using a 200 μm-thick layer of SU-8. For this ion trap, a backside ion loading slot was created by making the centre through-wafer hole of 1 mm in diameter using the mechanical drilling. Experimentally, the on-chip optical waveguides with various configurations were characterised and mainly used for the particle secular motion detection.

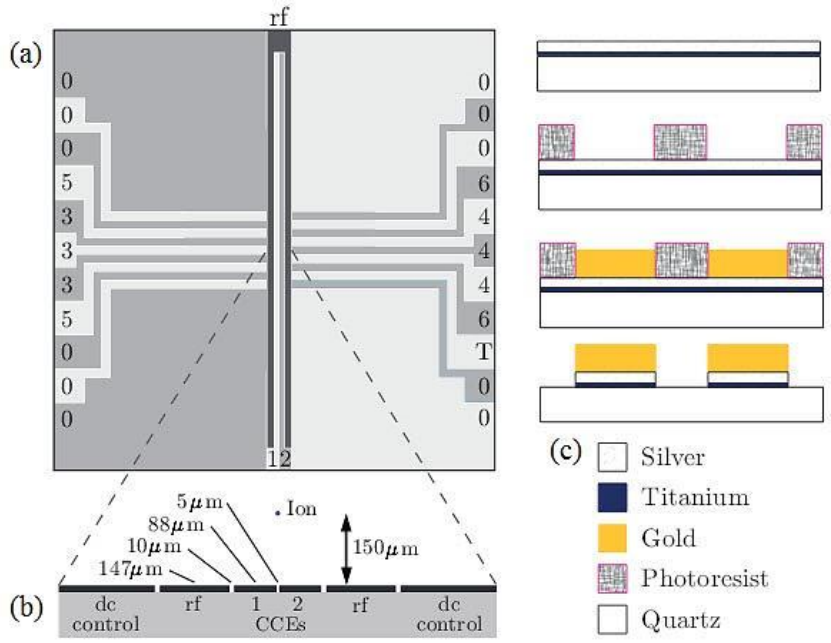


Figure 2.13 – A six-wire SEIT with gold-coated electrodes fabricated on quartz substrate. (a) Top view of trap layout. (b) Cross-section structural diagram shows electrode dimension and gap variation from the centre trap (ion position) to the periphery with an ion-electrode distance of 150 μm. (c) Fabrication steps (see text) (Figure from ref. [121].)

2.4.4 Silicon-On-Insulator (SOI) structures

In 2009, Britton et al. [87] first demonstrated the use of a commercial Silicon-On-Insulator (SOI) substrate to fabricate the SEIT containing 45 electrodes as shown in Figure 2.14. The substrate is a commercially available SOI with a Si resistivity of 5-20 × 10^3 Ω.cm.

The process started with photolithographic patterning of trap electrodes on the Si device layer. The exposed Si layer was etched to create electrically isolated islands of silicon electrodes using anisotropic etching, the Bosch process DRIE. Then a 3 μm thermal buried oxide layer was removed by an isotropic wet-etching, exhibiting a lateral undercut about 2 μm which in turn provides shielding of the dielectric exposure from the trapped ions. A series of conductive layers including 10 nm Al, 10 nm Ti and 1 μm Au were deposited on the silicon to make conductive electrodes. To lower the electrode resistance, the metal deposition step performed at the end of the process can be done without requiring an additional mask. The trap as shown in Figure 2.14(a) composed of two different trap regions: one with bare silicon electrodes and another with gold-coated electrodes that are of benefit to the study of ion-motion heating associated with the electrode material.

The SOI traps reveal the main advantage over the other SEITs by demonstrating that, the thicker Si device layer that is used, the more efficient the shielding of dielectric surfaces is due to a high aspect ratio trap relative to the height-to-width aspect ratio of the electrode thickness (100 μm) and the interelectrode spacing (4 μm). Also the backside ion loading slot can be made using a single process of a deep Si DRIE from the backside (a handle Si layer). However, a thin buried oxide layer can results in a larger capacitance between the RF electrodes and ground than those of the anodically bonded traps. This can cause ohmic heating and can degrade the RF resonator quality factor. Similarly, a larger capacitance between the control DC electrodes and ground can cause intrinsic micromotion; hence a SOI trap with thick oxide is necessary.

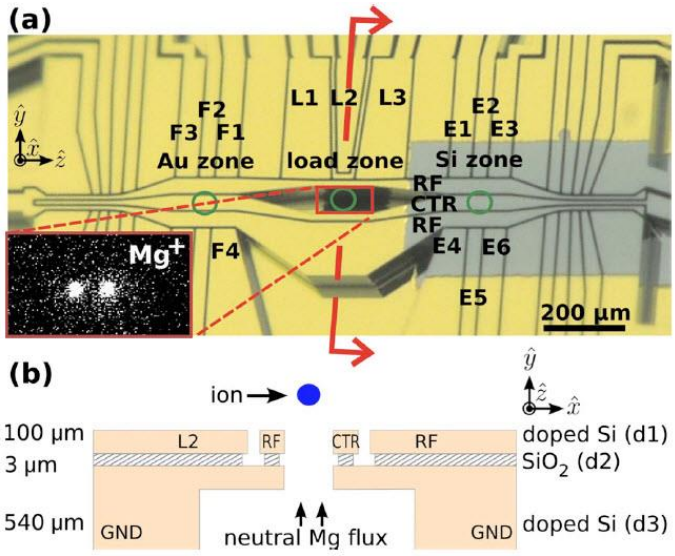


Figure 2.14 – A multi-zone surface trap fabricated from a SOI wafer. (a) Trap geometry with a loading zone (L1-L3) and two trap zones with Au coating (F1-F6) and bare silicon (E1-E6). Inset: Imaging of two trapped Mg^+ ions. (b) Trap structure in cross-section near the loading zone. (Figure from ref. [87].)

2.4.5 Conductive structures on insulator with ground layer

Recent works aim to develop more complex asymmetric surface-electrode ion trap structures which require several numbers of process steps and high reliability. The use of the standard VLSI (very-large-scale integration) fabrication techniques seems promising for truly scaling ion-trap array structures in the future. With that idea, Leibrandt et al. [88] proposed the initial traps fabricated using aluminium which is a common VLSI material with low resistivity. In Figure 2.15(b), a 1 µm thick of the first aluminium layer (M1) was deposited directly on the Si substrate acting as a ground plane to prevent RF loss in the Si substrate followed by a 0.4 µm of silicon nitride (Si_3N_4) layer. The second metal layer (M2) of a 1 µm-thick aluminium being the layer of the DC control electrodes was deposited onto the Si_3N_4 layer. Then the M2 layer was coated by a 10 µm-thick plasma-enhanced tetraethyl orthosilicate (PETEOS) SiO_2 film (with a dielectric constant of 4.0, high breakdown voltage and low current leakage) [126]. The third metal layer (M3) of a 1 µm-thick aluminium was constructed on top of the thick oxide to form RF electrodes.

In this particular trap structure, a thick insulator layer is necessary to increase the breakdown voltage and reduce the capacitance coupling between the RF electrodes (M3) and the DC electrodes (M2) [77], [80]. Overhanging of metallised RF electrodes on the dielectric layer and residing of the metallized DC electrodes underneath the trap position are beneficial in shielding exposed dielectric surfaces that are in direct line of sight from trapped ions. However, the problem of using aluminium (a material compatible with VLSI technology) to form electrodes is an oxide film formed instantaneously on aluminium contacts in air or with UV irradiation resulting in unwanted charge build-up on the electrode surfaces. This could degrade the trap performance. Thus it was suggested that the standard metallisation such as a tungsten (W) or titanium/tungsten (Ti/W) layer in the order tens of micrometres could be additionally deposited on top of the aluminium electrodes to improve the surface integrity for ion trapping.

The experiment was performed at room temperature (300 K). Ions were confined above the trap surface ≈ 60-79 μm by the RF voltage range 140-370 V at drive frequencies $\Omega_{RF}/2\pi$ = 32-52 MHz. This trap encountered several issues including a shorter ion lifetime of 30-120 seconds than the expected values between one and five minutes at such low vacuum pressure (6.7×10^{-9} Pa), electrical shorts between the DC electrodes (M2) and the ground plane (M1) through a 0.4 μm-thick Si_3N_4 or shorts through the Si substrate, and some unidentified reliability issues. Despite these issues, the ion heating rate at room temperature was relatively low, 7 ± 3 quanta/ms at the secular frequency $\omega/2\pi$ = 1.6 MHz corresponding to a spectral density of electric field noise of $8 \pm 3 \times 10^{-11}$ $(V/m)^2/Hz$ for the ion height of 60 μm above the trap surface. Problems of short ion lifetime and electrical shorts between layers were suspected to be related to its structure: i) local outgassing from the 10 μm-thick SiO_2 layer degrades the ion lifetime and ii) crack in a brittle and thin nitride (Si_3N_4) layer underneath the wire-bonding pads where the electrodes hit the ground plane or through the Si substrate. The authors suggests that the mechanical defects found may be fixed by replacing Si_3N_4 (dense structure, hard, high stress level, and cracks readily) with oxide which is more robust insulator. The reason behind choosing nitride instead of oxide, commonly used as an insulator layer in many ion traps, was to have the relatively high capacitance of control electrodes to

ground (thin nitride insulating layer with high dielectric constant) and much lower capacitance of RF electrodes to ground. The former issue can be solved by using a capacitor divider to suppress RF pickup on the DC control electrodes. Nevertheless, the trap performance was significantly improved at cryogenic testing (6 K). The ion lifetime was increased to 4.5 ± 1.1 hours and the heating rate was reduced below 220 ± 30 quanta/s at a trap frequency $\omega/2\pi$ = 540 KHz (a spectral density of electric field noise of 10 ± 1 × 10^{-13} $(V/m)^2/Hz$ for the ion height of 79 μm).

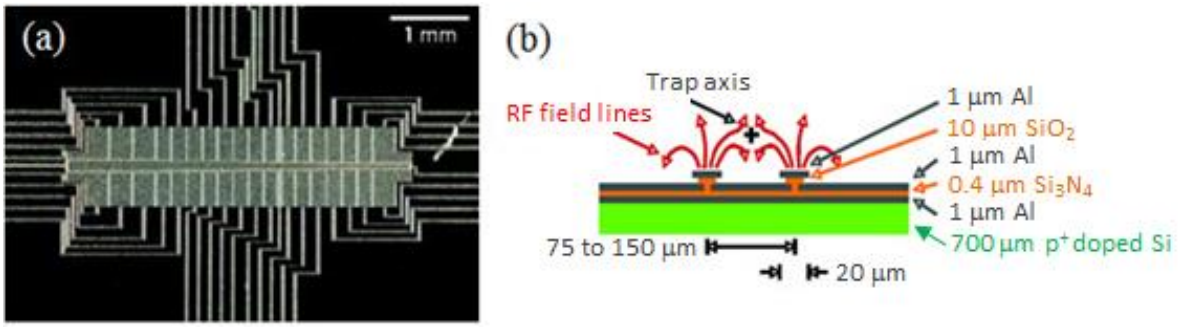


Figure 2.15 – A multi-zone surface-electrode ion trap fabricated on insulator with a ground layer. (a) The trap electrode layout. (b) Schematic cross-section of the trap structure fabricated on the Al, SiO_2 and Si_3N_4 layers, compatible materials with CMOS technology. (Figure from ref. [88].)

Stick et al. and Mount et al. [71], [92] presented the surface-electrode ion trap called the *"Sandia Thunderbird"* trap which is a symmetric six-wire geometry consisting of dual inner DC electrodes, RF electrode rails and segmented outer DC electrodes (Figure 2.16(b)). The trap geometry is similar to a six-wire design of Allcock et al. [121], [124] (splitting a centre control electrode) but the fabrication techniques used are different (see detail in Section 2.3.3). This trap was fabricated using standard VLSI technologies similar to Leibrandt et al. [88] but with the additional via (vertical interconnect access). The trap electrodes in Figure 2.16(a) were constructed between two metal layers: the top metal plane (M2) forming the top electrode layer used to supply the trap voltages and the lower metal plane (M1) acting as a ground plane to prevent RF coupling into the silicon substrate. A thick oxide layer (9-14

μm) between M1 and M2 compared to a thinner oxide layer decreases the capacitance between the RF electrodes and ground resulting in an increase of RF generator quality factor. These silicon dioxide pillars electrically separating the two metal layers were fabricated by multiple layers of plasma-enhanced chemical vapour deposition (PECVD). A hole through the SOI substrate was made over the entire trapping region to allow for the backside ion-loading to avoid the issue of shorting between electrodes by deposited materials from the natural atomic flux when loading ions from the side. The outer DC electrodes were electrically connected to the recessed bond pads by via to the electrical plane M1 which in turn revolved the obstruction of the wire-bond ribbons above the trapping plane.

The traps were operated at RF voltage amplitude range 50-200 V at a wide range of RF drive frequencies $\Omega_{RF}/2\pi \approx$ 27-43 MHz. Ca^+ ions were confined $\approx$ 80 μm above the top electrode layer (M2). The ion lifetime was in the order of several hours (> 10 hours) with laser cooling and as long as 20 minutes without cooling. Linear shuttling of a single ion over 10-electrode length ($\approx$ 770 μm) was demonstrated with high success rate, 10^6 times without ion loss. Further investigation of quantum protocols such as separation and recombination of ion chains including the motion heating rate of the $^{171}Yb^+$ ions in this trap were presented by Mount et al. [92]. The trap depth was found to be $\approx$ 86 mV corresponding to an applied RF voltage of 220 V at drive frequency $\Omega_{RF}/2\pi = 27.8$ MHz. The breakdown voltage of 300 V was reported. The electric-field noise power of this trap system was found to be $\omega S_E(\omega) = 6.3 \times 10^{-4}$ V^2/m^2 corresponding to the heating rate $\dot{\bar{n}} = 0.8 \pm 0.1$ quanta/ms at a radial secular frequency $\omega/2\pi = 2.1$ MHz.

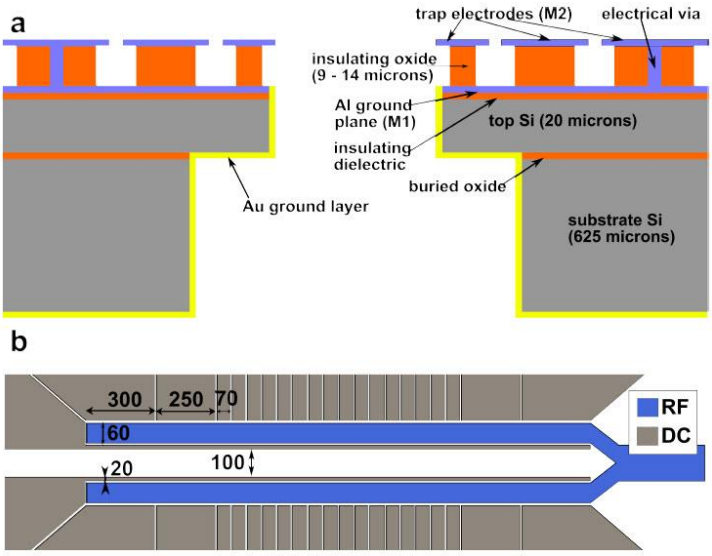


Figure 2.16 – A symmetric six-rail design named the "*Sandia Thunderbird*" trap with two metal layers and the use of via. (a) Schematic cross-section of the trap structure comprising a silicon substrate, oxide layer and aluminium electrodes. (b) The trap layout with the loading slot. (Figure from refs. [71], [92].)

Unlike the use of a linear centre-electrode geometry at the junction region [83], Moehring et al. [86] proposed a SEIT with the implementation of a Y-shaped junction. The optimised Y-shaped junction was designed to minimise the magnitude of pseudopotential in the junction region as a function of electrode geometry. The fabrication techniques used to build the Y-junction trap were similar to the previous work of Stick et al. [71]. Calcium (Ca^+) ions were trapped 70 μm above the trap plane. The applied RF voltages were varied between 25-165 V for trapping in the loading zone and 85-120 V for shuttling through the junction, at a fixed RF drive frequency $\Omega_{RF}/2\pi = 43$ MHz. The ion lifetime was reported to be in several hours when the ions were Doppler-cooled, and about 1 minute without cooling. The junction shuttling was successful in performing 10^6 round-trip transports in each path of the Y-junction without ion loss. One interesting junction-shuttling routine observed in the Y-trap was a minimal voltage adjustment required only on the centre electrode at low DC voltage amplitude of - 0.5 V. Ions were shuttled in the linear regions and junction regions using a small number of the segmented DC electrodes and survived these routines with and without Doppler cooling during shuttling. More complex shuttling routines into each leg of junction were demonstrated without ion loss over an hour for Doppler-cooled multiple ions.

Separation and recombination of two ions was observed hundreds of times without error. The optimised junction electrode of the Y-junction trap experimentally demonstrated a robust ion-trap system capable of performing a reliable linear and junction shuttling including ion chain separation and recombination with or without Doppler cooling during shuttling.

In recent work of Wright et al. [73], the SEIT with X-junction demonstrated the modification of the RF electrode shape near the junction to increase trapping strength and reduce ion heating rate during transport. The X-junction trap was also fabricated with similar materials and techniques used by Stick et al. and Mount et al. [71], [92] as discussed above. Instead, this trap was fabricated with three layers of patterned aluminium (Al) electrodes and in the absence of via. The bottom Al layer (M1) normally grounded prevents the RF electric field loss in Si substrate. The middle metal layer (M2) forms the patterned RF, centre electrode and outer control electrodes including the integrated on-chip capacitors for minimising RF pickup on the control electrodes. The additional M3 layer is a top ground layer to define the boundary of the control electrodes. The ion-loading slot (50×50 μm) was etched through one of the centre electrodes as shown in Figure 2.16(b), not the entire trap region as presented in the *"Sandia Thunderbird"* trap [71], [92].

The trap was operated with an applied RF voltage of 128 V at frequency $\Omega_{RF}/2\pi$ = 58.55 MHz, suggesting a trap depth of 29 meV. The ion lifetime was observed for several hours while continuously Doppler-cooled and dropped to five seconds when the cooling laser was off. Wright succeeded in performing high fidelity junction shutting between two legs (≈ 400 μm in total distance) with the success rate of at least 99.8% (departure) and at least 93% (return) from 106 round-trips. The ion heating was pronounced after transporting the ion back and forth through the junction after 85 round-trips; at time, about 34 milliseconds without Doppler cooling. The main source of the ion heating was found to be dominated by cumulative heating effects and potentially caused by electrical noise on the RF and control potentials in association with the digital-to-analog converter (DAC) control system. Another issue found during the experimental characterisation of the junction was a potential barrier located at the junction centre causing unstable trapping and shuttling through the junction. This unwanted potential barrier was believed to be as a result of an incomplete etching of

the oxide layer leaving the residual dielectrics which can be charged up and generate stray electric fields.

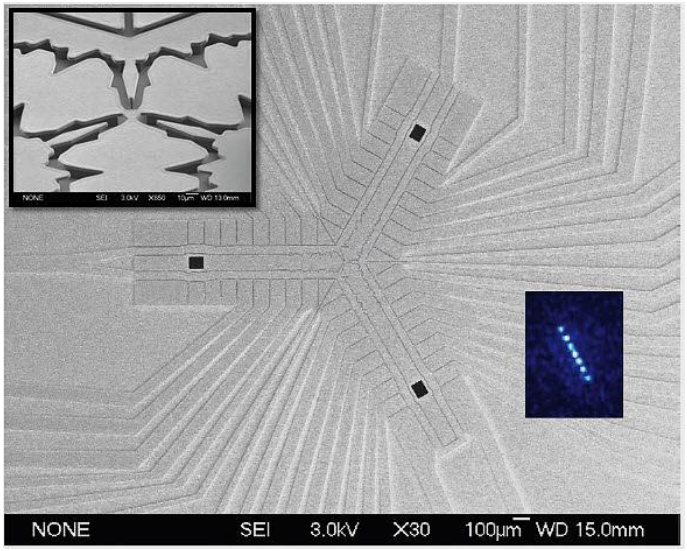


Figure 2.17 – SEM image of a five-wire design with Y-shaped junction. Insets show close-up images of the modified shape of the centre control electrode and the RF rails at the junction region (top inset) and imaging of a linear chain of seven trapped ions (bottom inset). (Figure from ref. [86].)

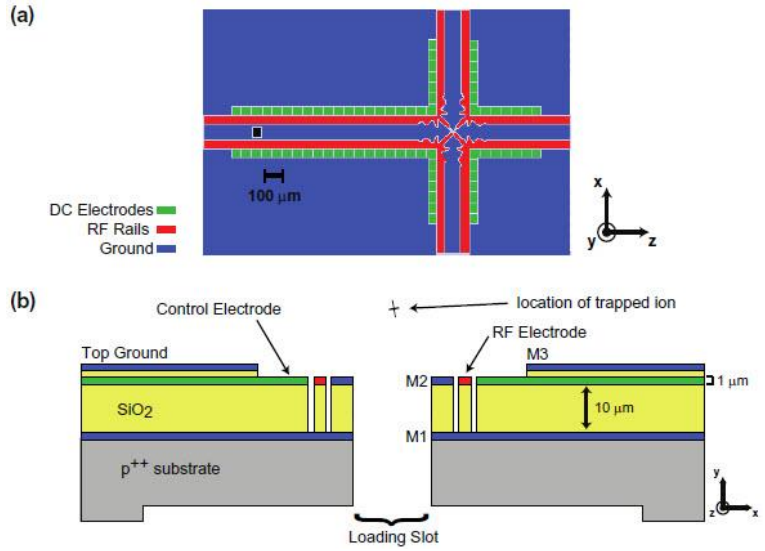


Figure 2.18 – A surface-electrode X-junction ion trap with three metal layers. (a) Top view of trap layout. (b) Cross-section structural diagram at the loading zone comprising a Si substrate, a SiO_2 insulating layer and three layers of aluminium electrodes. (Figure from ref. [73].)

2.5 Experimental demonstrations of surface-electrode ion traps

Table 2.1 presents the experimental demonstrations of various surface-electrode ion trap geometries utilising both atomic ions and microparticles to assess the trap design and performance. Besides the basic ion-trap and quantum operations for QIP, one unique operation of interest in SEITs, the levitation scheme by means of RF nil shifting, was first demonstrated in a single planar ring trap with ions [89], [112]. Normally, trapped-ion experiments have to be conducted in ultra-high-vacuum (UHV) conditions in order to be securely trapped, well isolated from the environment, and efficiently laser-cooled trapped ions when performing quantum operations and also other quantum phenomenon studies. However, there have been a small number of experiments carried out in a rough vacuum with macroscopic ions [83], [116] and at atmospheric pressure with charged microparticles [90], [107], [111]. The use of microparticle experiment is primarily suitable for a proof of principle, study of trap properties and functionalities during the trap design and optimisation phase. Microparticle trapping in ambient air reduces the demand and the cycle time for the design, set-up and implementation of an experimental apparatus compared to those of atomic ion trapping experiments. In microparticle traps, the vacuum system and optical laser cooling system are not required. With its advantages, the microparticle trap normally acts as a prototype setup for the further development and optimisation of the microfabricated ion traps. Variants of microparticles have been used such as diamond [90], [111], and dust particles (lycopodium spores) [107]. The simplest charging technique used is based on the triboelectric effect (also known as triboelectric charging) in which certain materials become electrically charged after they come into friction contact with a different material. For example, crystals of diamond (10 and 25 μm in diameter) are charged by pushing them from a Teflon tube with a Teflon-insulated wire [111] or rubbing diamond particles (1.5 μm to 150 μm in diameter) against a Teflon sheet using a brush [90]. The triboelectric effect, however, is not very predictable because the polarity and strength of the charges produced differ according to the materials, surface roughness, temperature, strain, and other properties. Therefore, a more reliable charging technique called Electrospray ionization (ESI) system was used to generate charged-aminopolystyrene nanospheres [83], [107]. In addition, typical operating condition of 200-300 V

at a frequency range from a few hertz to several kilohertz are easy to synthesise by using a function generator and high-power amplifier generating various amplitudes and frequency range, or auto-transformers to generate the target voltage range with a fixed frequency, 50 Hz or 60 Hz. The monitor system can also be setup with a green laser light or HeNe laser beam used to illuminate trapped microparticles. The scattered light should be easy to observe with video monitoring of the trapped particle through a charge-coupled device (CCD) camera [83], [111]. In one particular trap design with integrated waveguides, a 650 nm laser diode was used to excite the particle and the scattered light from the trapped particle was collected by the on-chip waveguides and detected using an external photodiode [90].

The principal drawback of studies using microscopic charged particles to investigate trap properties in air is that, unlike atomic ions, these trapped particles are not identical. Since the mass of a particle and the amount of electric charge carried by a particle are not fixed, charge-to-mass ratio (Q/m) is not the same for every particle leading to a large variation in the experimental results. Without reliable techniques to measure or quantify mass and electrostatic charge on microparticles, this is more difficult in analysing the results of an experiment with too many uncontrolled parameters.

Table 2.1 - Summary of various SEITs with their operations in a vacuum system and atmospheric pressure (ambient air) with various types of ions and charged microparticles.

Trap design	Materials	Trap dimensions	Ion trap		Microparticle trap		Key performances
			Ion	Operating condition	Particle size (diameter)	Operating condition	
2D array traps (multiple traps) [60], [87]	PCB Cu	Lattice space = 3 mm Gap = 0.18 mm Ion height = 1 mm	-	-	0.44 μm spheres[1]	400 V 1 kHz 10^{-1} Torr	Trapping of microsphere array
Planar ring traps: single ring and 3-ring configuration [83]	2-layer PCB Cu	Ground electrode = 2.0 mm, RF electrode = 3.5 - 8.6 mm (in diameter)	$^{129}Xe^+$	190-380 V 2.80 MHz 7×10^{-6} Torr	25 μm diamonds	700 V 60 Hz 760 Torr	Large operating range, trapping ions and particles $m/z \sim 10^2$ - 10^9
2D array traps 6×6 lattice traps [91]	Stainless steel mesh	Lattice space = 1.67 mm Gap = 0.18 mm Ion height = 1 mm	$^{88}Sr^+$	300 V 7.70 MHz 7×10^{-10} Torr	0.44 μm spheres[1]	300 V 1960 Hz 1 Torr	First experiment presents 2D lattice of ions.
A planar point Paul trap (a single trap) [84], [90]	2-layer PCB Cu	Ground electrode = 1.1 mm RF electrode = 5.9 mm (in diameter) Gap = 0.1 mm Ion height = 960 μm	$^{88}Sr^+$	360 V 8.07 MHz (300 K)	-	-	Trapping of single ions and 2D planar ion crystals. Ion height varies 200-1000 μm.
				250 V 6 MHz Cryogenic 8 K	-	-	Integrated light source to directly drive the qubit transition of $^{88}Sr^+$
SEIT with segmented ground electrodes (a single trap) [89]	Quartz/Au MEMS fabrication	n/a Ion height = 30 μm	$^{24}Mg^+$	50 V 45 MHz	-	-	Integrated optical fibre to collect fluorescence light from the ion. Ion height varies 30-100 μm.
A planar one-hole ring trap (a single trap) [85]	Pyrex/Au MEMS fabrication	Ground electrode = 1.0 mm (in diameter)	-	-	1.5-150 μm diamonds	100-750 V 100-700 Hz 760 Torr	Integrated on-chip waveguide to detect particle position.
2D array trap 2×2 lattice traps [78]	PCB Cu	Lattice space = 1.5 mm	-	-	Dust particles[2]	230 V 50 Hz 150 V_{DC} 760 Torr	Pair-wise interactions of particles in a 2D array. Ability to merge the two spherical traps into one linear Paul trap.
2D array traps 4×4 lattice traps [79]	PCB Au/Cu	Lattice space = 1.5 mm Ion height = 400 μm	$^{40}Ca^+$	105 V 10 MHz	-	-	Extended work of [78] with ions but observed high heating rate.

Note: [1] 0.44 μm diameter aminopolystyrene spheres, [2] Dust particles (Lycopodium spores)

2.6 Summary

Fabrication of microscopic ion traps has utilised a wide variety of materials and techniques. A symmetric three-dimensional (3D) multi-layer linear ion trap with segmented electrodes presents great advantages of deep trap depth and good optical access similar to conventional quadruple RF Paul traps. The 3D linear traps were demonstrated in two different forms: a two-layer trap and a three-layer trap. The concept of trap construction is achieved by patterning electrodes on insulating wafers and mounting them together with an insulating spacer. Variants of multi-layer linear traps containing small numbers of trapping zones to multi-trapping zones and more complex electrode configurations with the implementation of junctions (i.e. T-junction, X-junction) were proposed and have been successful in demonstrating the fundamental operations required for quantum computing [78], [87], [101], [102], [104]. The successful trapping of ions in the order of 10 in a small number of zones was also demonstrated [52]. Most fabrication techniques utilised in multi-layer linear traps require manual assembly of electrodes and the insulator spacers. This inherent drawback may raise more issues when scaled to arrays with a large number of interconnected ion traps resulting in imperfections from the manual alignment. This structure is also difficult to scale for more complex trap topologies, and even for a large-scale ion-trap quantum computing system. To achieve a true scalability in a 3D multi-layer linear trap structure, a monolithic approach instead of a stacking approach needs to be followed. In attempting to eliminate the manual assembly step, the further development of 3D multi-layer linear trap using GaAs/AlGaAs heterostructure [77] and the silica-on-silicon technique [79] has been demonstrated. However, the GaAs/AlGaAs trap suffered from very low breakdown voltage $\approx$ 8 V and significantly high anomalous heating. The silica-on-silicon trap offers a significant improvement over the GaAs/AlGaAs trap and was proven to be scalable to large 2D arrays of trapping segments with many qubits. Nevertheless, it requires a series of fabrication steps and the non-standard techniques (i.e. shadow evaporation).

In the quest for a more simplified fabrication, a new ion-trap design is needed. The new approach of a linear RF Paul trap design was proposed using the geometric transformation of a symmetric 3D multi-layer structure (trapped ions surrounded by electrodes) into

an asymmetric planar structure with ions residing above a planar array of electrodes. A planar trap structure also known as a surface-electrode ion trap (SEIT) offers a simplification in fabrication, amenability for a variety of trap geometries, scalability to a large number of trapping and operating zones to accommodate large number of qubits, and miniaturization of trap sizes. With the idea of trap electrodes lying in a single plane similar to VLSI architecture design, various fabrication methods including standard PCB manufacturing, MEMS fabrication and VLSI fabrication techniques have been widely used for construction of SEITs. Several SEIT designs have been proposed including PCB traps [83], [84], [107], [108], [111], [112], [115], bulk-silicon trap with an anodic bonding glass spacer [82], [101], conductive structures on insulating substrates [81], [85], [89], [118], [121], conductive structures on SOI substrate [87] and more complex trap structures built with multi-metal layers [71], [73], [86], [88], [92]. Furthermore, these techniques has been utilised with various choices of substrates such as low RF-loss insulator substrates (e.g. quartz, fused silica, sapphire, Pyrex, alumina), compatible semiconductor materials (e.g. Si, Si_3N_4, SiO_2, SOI wafer) and also different type of conductive electrodes (i.e. Au, Ag, Cu, Al). In addition, several attempts to integrate on-board electronics [81] and micro-optical devices (e.g., light source [89], [115], waveguide [90]) were made to enhance the ion motional control and detection, and, in particular, that of secular frequency measurement. Even though SEIT geometries are prone to low trap depth and high heating rate [80], [114], many works still successfully demonstrated stable trapping with sufficient ion lifetime (with laser cooling) and high success rate in performing basic quantum operations in 2D arrays of microtraps with junctions [71], [73], [86], [127]. Surface-electrode ion traps have proven to be useful tools not only for a scalable quantum computing and information-processing system but also for other potential applications in quantum simulation [107], [108], [116], mass spectrometry [111], [128], micro- and nanoparticle manipulations [90] and pressure gauge sensing [83]. Nevertheless the critical issue of motional ion heating rates limiting the fidelity of quantum operations has impeded progressing in developing a large-scale quantum computer with trapped ions. Since an anomalous heating is not easily to explain and because it is difficult to identify its sources, experimental results of heating rate studies suggest that the dependency of ion-electrode distance (scaling $\bar{n} \propto d^{-4}$), trap frequency, electrode

surface materials and temperatures dominates the motional ion heating compared to thermal Johnson noise estimation (i.e. electrode resistance or connecting electronic components) [114]. Due to the fact that the studies of ion heating rate are normally carried out during the experimental phase, not by modelling or simulation, a careful consideration of scaling ion-electrode distance and choosing materials, fabrication technique and benchmarking is essential.

Chapter 3

Theory of charged particle trapping

This chapter provides an overview of the theoretical aspects relating to the design of charged particle trapping systems. First, the principle of electrodynamic trapping of charged particles using a combination of static (DC) and oscillating (AC) electric fields corresponding to the quadrupole system is outlined. To understand how radio frequency (RF) Paul traps confine charged particles or ions, the physics or the particle dynamics in quadrupole electric fields is described by the well-known Mathieu's differential equations. The complete solutions of the Mathieu's equation and the stability diagrams are first derived to provide insights on the ion trajectory stability. In complex ion-trap geometries, the pseudopotential approximation is used to derive the pseudopotential well, trap depth and secular frequencies in the relation of operating parameters. Subsequent topics include the motion of charged particles in ambient air associated with Stokes' Law and the effect of damping (drag effect) on the stability diagram of the Mathieu's equation.

3.1 Trapping of charged particles in quadrupole electric fields

Earnshaw's theorem [1] demonstrates that particle confinement cannot be achieved by using static electric or magnetic fields alone. Wolfgang Paul and Hans Dehmelt found a method to overcome this by the use of oscillating electric fields, since Earnshaw's theorem

strictly applies only to static fields. The principle of electrodynamic balance (EDB) using a combination of static (DC) and oscillating (AC) electric fields to trap charged particles in quadrupole trap configurations was first introduced by Paul and his colleagues [29]. The three-dimensional (3D) quadrupole ion trap (QIT) is the device that functions both as an ion store and as a mass spectrometer of large mass range resolution and high sensitivity. Figure 3.1 shows a conventional 3D QIT consisting of three hyperbolic electrodes. One is the ring electrode positioned symmetrically between the two endcaps. The dimension is the radius of the ring electrode in the central horizontal plane and is the separation of the two endcaps measured along the trapping axis.

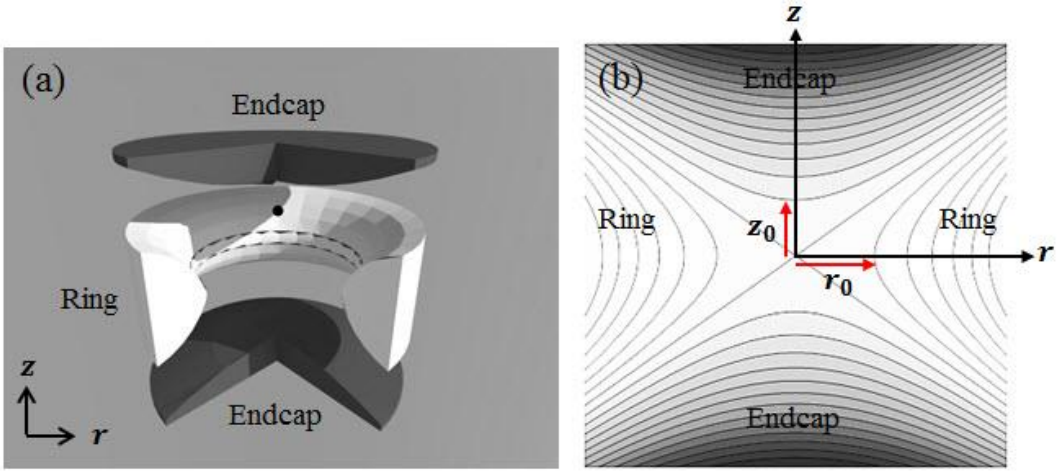


Figure 3.1 – A conventional 3D quadrupole ion trap (QIT). (a) Schematic cross-section of a 3D QIT consisting of a hyperbolic ring electrode and two hyperbolic endcaps. (b) Equipotential lines of the quadrupole electric field in the rz-plane. (Figure modified from ref. [128].)

Another trap configuration of the RF Paul traps is a two-dimensional (2D) quadrupole ion trap which composes of four-hyperbolic shaped electrodes linearly extended in the y-direction as shown in Figure 3.2(a). However, the most commonly used trap is the quadrupole mass filter with four circular rods as shown in Figure 3.2(b) because it is easier to build compared to the hyperbolic configuration. Each pair of opposite rods is connected electrically and the applied potentials on the pairs of rods are out-of-phase with each other, such that

a 2D quadrupole field is established in the xy-plane but the potential along the z-axis is zero. While travelling along the z-axis, trapped particles will also oscillate in the xy-plane under the influence of electric fields generated by these four rods as shown in Figure 3.2(c). The trapping potential in conventional RF quadrupole ion traps has the shape of a saddle surface and oscillates with an angular frequency Ω around the z-axis as shown in Figure 3.3. Under the appropriate trapping parameters, charged particles establish stable trajectories inside the trap when trapped at a local minimum of the pseudopotential (RF nil) as shown in Figure 3.3(c).

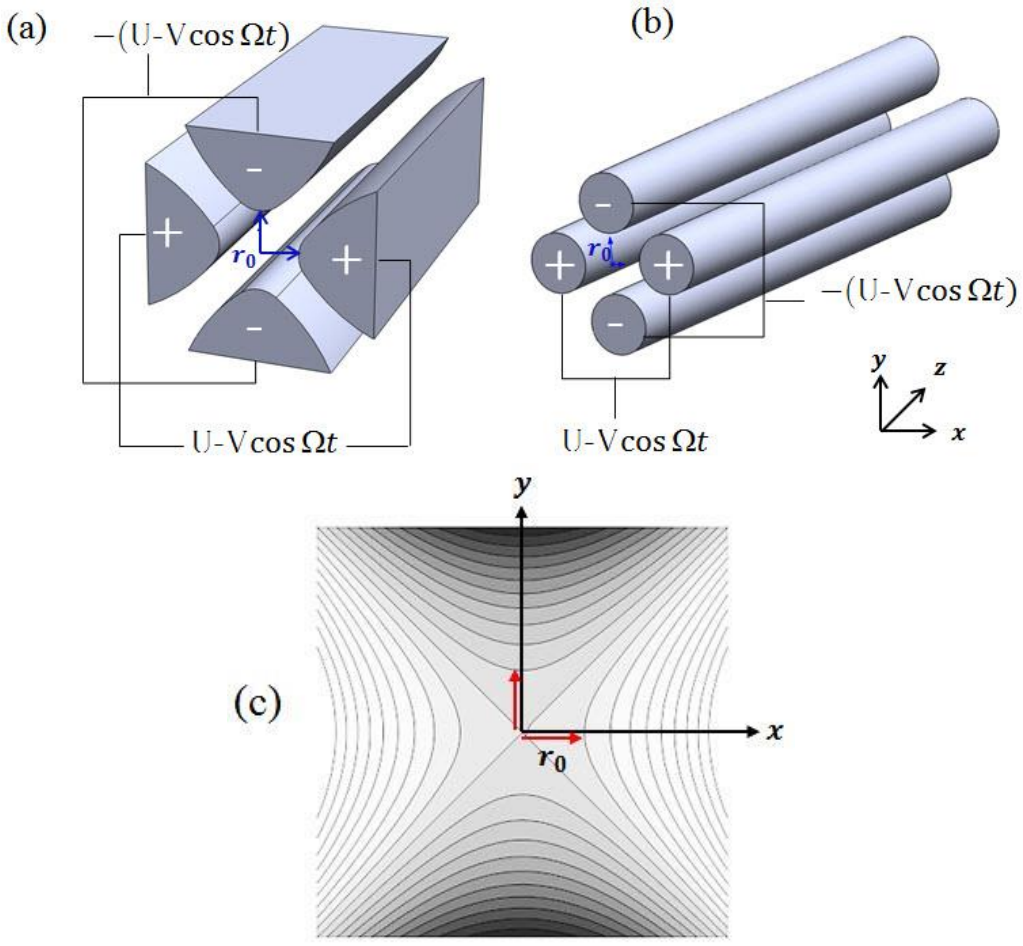


Figure 3.2 – Schematic cross-section of two-dimensional (2D) QITs for the mass spectrometer. (a) A hyperbolic-shaped electrode structure. (b) A circular-shaped electrode structure. (c) Equipotential lines of a quadrupole field in the xy-plane. (Figure modified from ref. [29].)

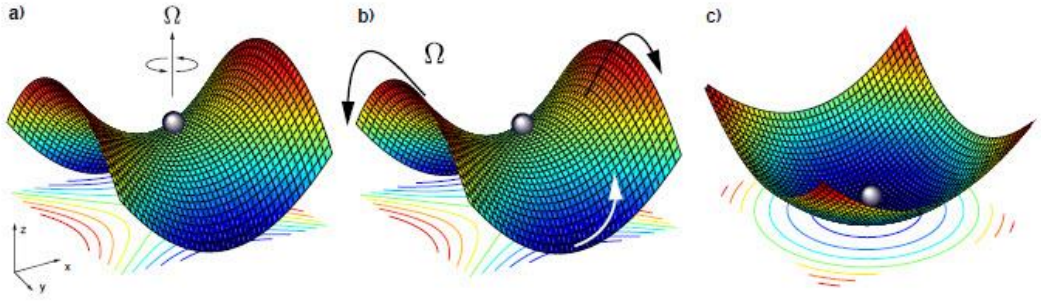


Figure 3.3 – The RF potential used for trapping charged particles in conventional QITs. Illustration of Equation (3.2) - (a) forms the quadrupole electric fields in the shape of a saddle surface and oscillates with an angular frequency Ω around the z-axis, and (b) oscillates with a time-dependence t. (c) An effective potential (a time-averaged pseudopotential approximation) provides a local minimum (RF nil) at the centre of trap and trapping potential along both x and y directions. (Figure from ref. [129].)

3.2 The motion of charged particles in RF Paul traps

In this section, the motion of charged particles in RF Paul traps (or QITs) is discussed. The derivation of the equations of motion for charged particles confined in RF Paul traps can be treated in two ways: i) the complete solution of the Mathieu's differential equation, and ii) the simplified solution of an effective potential (also called quasi-, pseudo- or ponderomotive potential) approximation [16]. The often used term "*pseudopotential*" is presented throughout the thesis.

3.2.1 2D and 3D quadrupole potential fields

The following derivations are based on the theoretical analysis presented by Paul [86] and March [128]. Beginning with the conventional quadrupole ion traps (QITs) presented in Figure 3.1 and Figure 3.2, the trap generates a 3D parabolic potential Φ which can be written in a general term as

$$\Phi(x,y,z) = \frac{\Phi_0}{2r_0^2}(\alpha x^2 + \beta y^2 + \gamma z^2)\,. \tag{3.1}$$

The potential Φ must satisfy the Laplace condition: $\nabla^2\Phi_{x,y,z} = 0$ and must be true with a condition that $(\alpha + \beta + \gamma) = 0$. To satisfy these two conditions, there are two simplest ways chosen in practice following expressions in March [128].

For a 2D quadrupole ion trap (QIT) with $\alpha = -\beta = 1$ and $\gamma = 0$, a 2D potential distribution in the xy-plane is expressed as

$$\Phi(x, y) = \frac{\Phi_0}{2r_0^2}(x^2 - y^2)\,. \tag{3.2}$$

For a 3D quadrupole ion trap (QIT) with $\alpha = \beta = 1$ and γ = -2, a 3D potential distribution in the cylindrical coordinates (r, z) can be written in

$$\Phi(r, z) = \frac{\Phi_0(r^2 - 2z^2)}{R_0^2}. \tag{3.3}$$

where $R_0^2 = r_0^2 + 2z_0^2$, r_0 and z_0 is the distance from the trap centre to the electrode surface in the r and z directions.

Equation (3.2) is the expression for the potential often found in any standard stability analysis and often used as the starting point. To examine the equations of motion of a single particle confined in a 2D QIT subjected to the potential given by Equation (3.2), the component of ion motion in the x-direction ($y = 0$) is considered first and the other directions can be treated analogously. Then Equation (3.2) gives

$$\Phi(x, 0) = \frac{\Phi_0}{2r_0^2}x^2\,. \tag{3.4}$$

When considering a particular case of a single ion or charged particle with mass m and charge Q, the equation of motion of a single particle in three dimensions can be derived from the Newton's second law of motion and Lorentz force on a charged particle in an electric field,

$$m\ddot{\vec{r}}(x, y, z) = Q\vec{E} = -Q\nabla\Phi\ . \tag{3.5}$$

From Equation (3.5), the electric field at the point (x , $y = 0$) can be derived using Equation (3.2) as

$$\left(\frac{d\Phi}{dx}\right)_y = \frac{\Phi_0}{r_0^2}x\,, \tag{3.6}$$

and the force acting on the particle (F_x) is given by

$$F_x = -Q\left(\frac{d\Phi}{dx}\right)_y = -Q\frac{\Phi_0}{r_0^2}x\,, \tag{3.7}$$

and

$$m\left(\frac{d^2x}{dt^2}\right) = m\ddot{x} = -Q\frac{\Phi_0}{r_0^2}x\,. \tag{3.8}$$

If the applied voltage is given by the combination of a DC voltage U and an AC voltage V oscillating with an angular frequency Ω_T, then the potential is

$$\Phi_0 = U + V\cos\Omega_T t\ . \tag{3.9}$$

Equation (3.9) is substituted into Equation (3.8) for the component of ion motion in the x-direction first. A similar approach is then applied to other directions (y and z). The decoupled equations of motion of a single particle (or ion) with a charge Q and mass m are

$$\ddot{x} + \frac{Q}{mr_0^2}(U + V\cos\Omega_T t)x = 0\,, \tag{3.10}$$

$$\ddot{y} - \frac{Q}{mr_0^2}(U + V\cos\Omega_T t)y = 0\ , \tag{3.11}$$

$$\ddot{z} = 0\ . \tag{3.12}$$

The solution of the equation of motion for the axial direction as shown in Equation (3.12) explains that a trapped particle follows a constant velocity along the z-axis.

Following an approach that is similar to the 2D QIT described above, the equations of motion in a 3D QIT can be obtained by solving Equation (3.3). Then its equations of motion are

$$\ddot{r} + \frac{2Q}{m(r_0^2 + 2z_0^2)}(U + V\cos\Omega_T t)r = 0 \tag{3.13}$$

and

$$\ddot{z} - \frac{4Q}{m(r_0^2 + 2z_0^2)}(U + V\cos\Omega_T t)z = 0 \tag{3.14}$$

3.2.2 Solutions to Mathieu's equation and stability diagram

To facilitate solutions of the equations of motion governing the stability of particle trajectory in QIT, it is convenient to write the equations in dimensionless form using the canonical or standard form of Mathieu's differential equation [130],

$$\frac{d^2u}{d\zeta^2} + (a_u - 2q_u \cos 2\zeta)u = 0\,, \tag{3.15}$$

where u is a displacement, ζ is a dimensionless parameter equal to $\Omega_T t/2$, and a_u and q_u are additional dimensionless stability parameters.

Considering the decoupled equations of motion of a single charged particle in a 2D QIT, the classical equations of motion shown in Equation (3.10) and (3.11) can be generalised into the standard form of Mathieu's equation in Equation (3.15) following the expressions described by Wineland et al. [131]. Thus,

$$\frac{d^2x}{d\zeta^2} + (a_x - 2q_x \cos 2\zeta)x = 0 \tag{3.16}$$

$$\frac{d^2y}{d\zeta^2} + \left(a_y - 2q_y \cos 2\zeta\right)y = 0 \tag{3.17}$$

with the following substitutions,

$$a_x = -a_y = \frac{4QU}{mr_0^2\Omega_T^2}; \quad q_x = -q_y = \frac{-2QV}{mr_0^2\Omega_T^2}; \quad \zeta \equiv \frac{\Omega_T t}{2}. \tag{3.18}$$

In addition, the relationship of the Mathieu's stability q parameters of the cylindrically symmetric 3D QIT is found that $q_x = q_y$ since $\alpha = \beta = 1$. The same treatments used in a 2D quadrupole trap stability analysis can be applied to derive a_z and q_z trapping parameters which are used frequently in discussions of the stability diagram of a 3D QIT in the case that $\alpha = \beta =$ -1 and $\gamma =$ -2. Following solutions of Mathieu's equation derived by Jones [130], the equations of motion of a particle in a cylindrically symmetric 3D QIT are:

$$\frac{d^2z}{d\zeta^2} + (a_z - 2q_z \cos 2\zeta)x = 0 \tag{3.19}$$

Case 1: $r_0^2 = 2z_0^2$

$$a_z = \frac{-8QU}{mr_0^2\Omega_T^2}; \quad q_z = \frac{4QV}{mr^2\Omega_T^2} \tag{3.20}$$

$$a_r = -a_z/2,\ q_r = -q_z/2 \text{ and } \zeta = \Omega_T t/2$$

Case 2: $r_0^2 \neq 2z_0^2$

$$a_z = \frac{-16QU}{mR_0^2\Omega_T^2}; \quad q_z = \frac{8QV}{mR^2\Omega_T^2} \tag{3.21}$$

$$a_r = -a_z/2,\ q_r = -q_z/2 \text{ and } \zeta = \Omega_T t/2$$

where $R^2 = r_0^2 + 2z_0^2$.

The Mathieu equation can be solved by using the Floquet theorem which can be found in greater detail of theoretical analysis in other references [130]–[132]. The solutions to Mathieu's equations are of two types - (i) periodic but unstable and (ii) periodic and stable. The stability diagram can be derived to describe the regions of stability and instability in terms of the dimensionless Mathieu parameter a and q as graphically illustrated in Figure 3.4. For a 2D QIT, the stability region in which the axial and radial stability overlap means that a particle of a given mass-to-charge ratio can be stably trapped within the area of shaded regions, labelled x-stable and z-stable as shown in Figure 3.4(a). The shaded regions labelled "*A*" and "*B*" shown in Figure 3.4(b) are referred to a region of stable trajectories in both r and z directions simultaneously in a 3D QIT. The region A is of the greatest importance and the first stability region to be considered at this time. As for the stability diagrams shown in Figure 3-5, the first stability region of the conventional 2D and 3D quadrupole ion traps has its stability boundary at $q = 0.908$ (with $a = 0$). For ions having values of the stability parameter $q_z > 0.908$ which is the maximum stability parameter (q_{max}) in the mass-selective instability mode [6], trapping efficiency will falls off gradually and ions will be ejected. However, The quadrupole ion trap can be operated in a stability region at a much higher q value than that is normally used in the region A (with $q < 0.908$), according to the detailed analysis of the quadrupole mass filter operating in higher stability regions [133], [134].

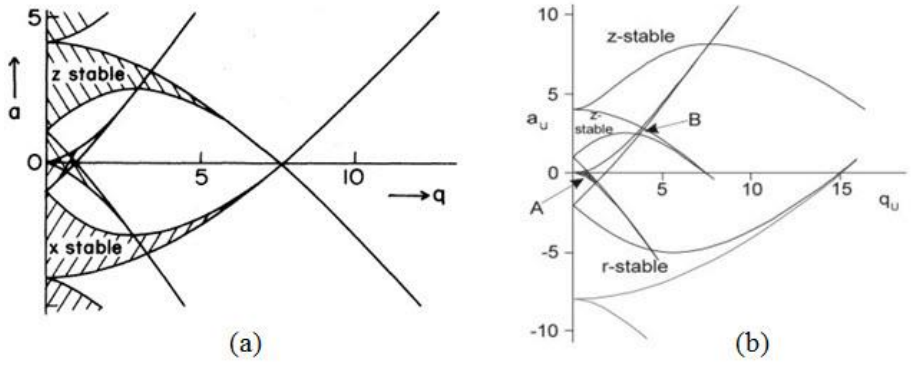


Figure 3.4 – The Mathieu stability diagram in (a,q) space. (a) A 2D quadrupole ion trap. (b) A 3D quadrupole ion trap. The overlapping regions labelled A and B present the stable trapping in both r and z directions simultaneously. (Figure from refs. [29], [128]).

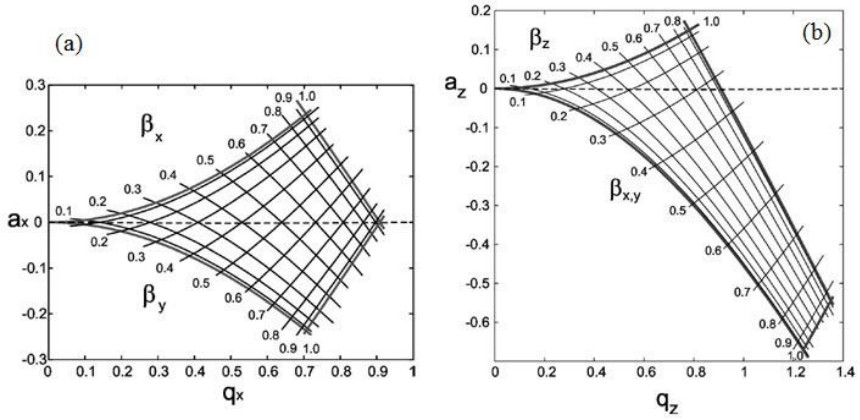


Figure 3.5 – The stability diagram of the first stability region. (a) A 2D linear quadrupole ion trap. (b) A 3D quadrupole ion trap. (Figure from ref. [34]).

From the solutions of two dimensionless parameter a and q derived above (see Equations (3.18), (3.20) and (3.21)), it is clearly seen that the stability of particle motion depends upon the mass (m) and charge (Q) of a particle, the size of the trap (r_0, z_0), the oscillating frequency (Ω_T /2π) and amplitude of the applied RF voltage, and the amplitudes of the applied DC (U) voltage. In Figure 3.5, the first stability region of the stability a - q plot can be used to determine whether the system is stable (trapped) or unstable (particle loss). In order to keep the experimental setup as simple as possible,

the operating conditions are usually treated with $V_{DC} = 0$ resulting in $a = 0$. In this case, the boundary trajectories of particles are given by the stability q parameter for $q < 0.908$. Equation (3.21) with $q_z = 8QV/mR^2\Omega_T^2$, gives a particle charge-to-mass (Q/m) limitation as

$$\frac{Q}{m} < \frac{0.908}{2}\frac{z_0^2}{V_{AC}}\Omega_T^2; \ \ with\, r_0 = z_0. \tag{3.22}$$

This upper limit of charge-to-mass (Q/m) ratio is inversely proportional to the oscillating AC voltage amplitude. In the study of microscopic particles, it is important to have Q/m ratio smaller than those of atomic ion species. Therefore, the driving frequency $\Omega_T/2\pi$ used in microparticle trapping can be kept much lower than the radio frequency in the range of megahertz or gigahertz needed for ion trapping.

For $q \ll 1$, following the derivations in Splatt [132] the motion of the trapped ion in the x-axis is written as

$$x(t) = x_0 \cos\omega_x t\left[1 + \frac{q_x}{2}\cos\Omega_T t\right] = 0 \tag{3.23}$$

where x_0 is the amplitude of the motion in the radial direction, ω_x is the secular frequency, q_x is the stability parameter in the x-direction and Ω_T is the drive frequency.

In Equation (3.23), it can be seen that the complete particle motion is governed by two superimposed components; first, a large amplitude, slow "*secular motion*" at the trap frequency ω_x, and second, a small amplitude, fast "*micromotion*" synchronously with the applied RF frequency Ω_T. The amplitude of micromotion is zero at the trap centre and is proportional to the displacement of the trapped particle from the RF nil point. Increasing the stability parameter q_x near the boundary of trap stability at $q_{max} = 0.908$, the amplitude of micromotion is largely expanded as shown in Figure 3.6. Typically, the amplitude of the micromotion is relatively small to sustain the trapped particle close to the trap centre. Such behaviour is desirable as it minimises the velocity and position uncertainty of the particle and maximises the laser coupling.

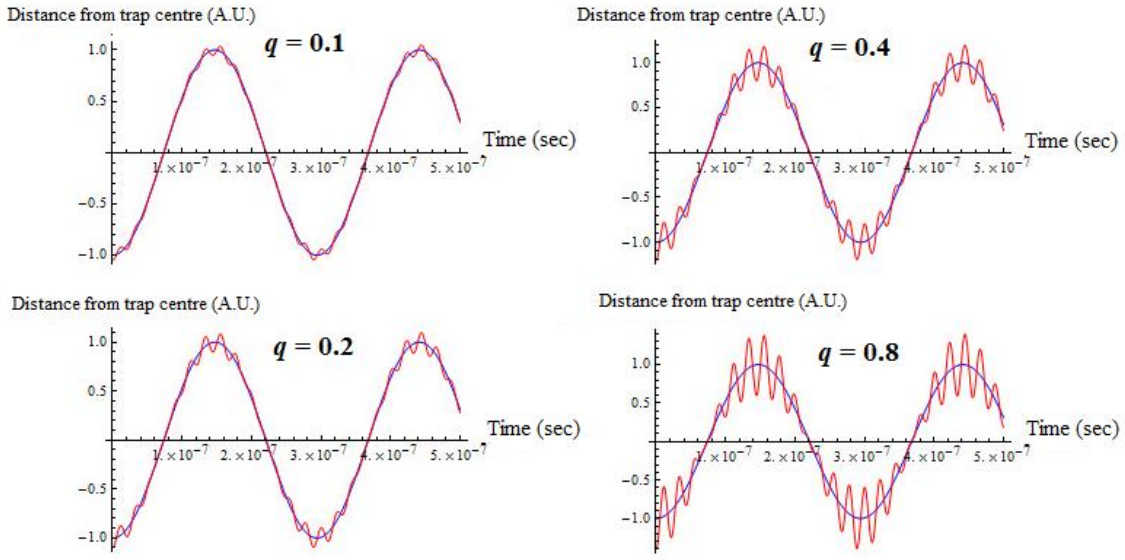


Figure 3.6 – A completed description of the ion's motion consisting of the secular motion (in blue) given by $\cos(\omega_x t)$ and the fast micromotion oscillating at Ω_T (in red) which is superimposed on top of the slower secular frequency ω_x with variation of the stability $q_x \rightarrow q_{max} = 0.908$. (Figure simulated using the Mathematica script in Appendix A.)

3.2.3 Pseudopotential approximation

The equations of motion for a particle confined in RF Paul traps can be treated in two ways. The first model is the completed solutions of Mathieu's differential equation discussed in the previous section. The second model is the solutions of pseudopotential approximation which is used as the simplified descriptions for any complex ion-trap systems. The numerical solutions of Mathieu's equation provide insights on the ion trajectory stability, while the pseudopotential approximation is more straightforward and convenient to analyse trap design and optimisation because it is dependent on the magnitude of the electric field only, not on the particle trajectories inside the trap. By using pseudopotential approximation, trap properties such as the pseudopotential well, trap depth, and secular frequencies corresponding to the given frequency and voltage can be evaluated. Following the pseudopotential approximation model described in Dehmelt [5], Sterling [135] and Madsen [136], an effective potential as the average potential that acts on a particle moving in one dimension in a rapidly oscillating electric field of the form is written as

$$E(z) = E_0(z)\cos(\Omega_T t) \tag{3.24}$$

where $E_0(z)$ is the spatial dependence of the electric field. The dynamic of a trapped particle in an oscillating field is derived by the Newton's second law of motion and Lorentz force law as

$$F_z(z,t) = m\ddot{z} = QE(z)$$

$$= QE_0(z)\cos(\Omega_T t). \tag{3.25}$$

Then the particle displacement along the z-axis as a function of time t is derived by integrating Equation (3.25) twice, and the solution is,

$$z(t) = -\frac{QE_0(z)}{m\Omega_T^2}\cos(\Omega_T t) + z_0. \tag{3.26}$$

With the initial condition $z(0) = z_0$ and $\dot{z}(0) = 0$, the time-average of the force in Equation (3.26) reveals that the average force felt by the particle is zero. This is evident from the $\cos(\Omega_T t)$ term, which is not satisfactory for maintain stable trapping. Now consider an inhomogeneous field in which the electric field is non-uniform and $\partial E_0(z)/\partial z \neq 0$. This will change the particle orbit and the force felt by the particle of $E_0(z)$, while the time dependence remains the same at $\cos(\Omega_T t)$. With small perturbation of the field, the electric field can then be expanded around the centre trap point z_0 following the expression in Sterling [135]:

$$E_0(z) \approx E_0(z_0) - \frac{\partial E_0(z_0)}{\partial z_0}\left(\frac{QE_0(z_0)}{m\Omega_T^2}\cos(\Omega_T t)\right). \tag{3.27}$$

Now substitute Equation (3.25) with Equation (3.27), and the equation of the force on the charged particle in the inhomogeneous electric field becomes

$$F_z(z,t) = QE_0(z_0)\cos(\Omega_T t) - Q\cos(\Omega_T t)\left(\frac{\partial E_0(z_0)}{\partial z_0}\frac{Q\,E_0(z)}{m\Omega_T^2}\cos(\Omega_T t)\right)$$

$$= QE_0(z_0)\cos(\Omega_T t) - \left(\frac{\partial E_0(z_0)}{\partial z_0}\frac{Q^2E_0(z)}{m\Omega_T^2}\right)\cos^2(\Omega_T t). \tag{3.28}$$

By averaging the force on the particle in Equation (3.28) over one period, the $\cos(\Omega_T t)$ term averages to zero, and the $\cos^2(\Omega_T t)$ term averages to 1/2. These yield the average force on the particle as

$$\bar{F}(z) = -\frac{Q^2 E_0^2}{2m\Omega_T^2}\frac{\partial E_0(z)}{\partial z}$$

$$= -Q\frac{\partial \psi(z)}{\partial z}. \tag{3.29}$$

where the pseudopotential $\psi(z)$ is defined by following the expression in Madsen [136] as

$$\psi(z) = \frac{QE_0^2(z)}{4m\Omega_T^2}. \tag{3.30}$$

From Equations (3.29) and (3.30), the result can be generalised to three dimensions following the expression in Dehmelt [5], so that the average force on a particle is

$$\bar{F}(x,y,z) = -Q\nabla\psi(x,y,z), \tag{3.31}$$

where the pseudopotential ψ is given as

$$\psi(x,y,z) = \frac{QE_0^2(x,y,z)}{4m\Omega_T^2} = \frac{Q|\nabla V_{RF}\,(x,y,z)|^2}{4m\Omega_T^2}. \tag{3.32}$$

Then, Equations (3.31) and (3.32) can be used to determine the effective motion of a particle confined by a trapping field. The particle motion in the pseudopotential can be approximated as the secular harmonic motion with the secular frequency described in Wineland et al. [131] and Madsen et al. [137],

$$\omega_{p,x}^2 = \frac{Q^2}{4m^2\Omega_T^2}\frac{\partial^2}{\partial x^2}\,(|\nabla V_{RF}(x,y,z)|^2) \tag{3.33}$$

3.3 The motion of microparticles in RF Paul traps as a function of damping

When a charged particle is trapped stably in a RF Paul trap, the particle's motion consists of a slow harmonic motion called the secular motion and a low-amplitude, high-frequency motion called the micromotion. However, when aerosol particles or micro- and nanoparticles are confined in a closed environment (e.g. in air or background gas), the effects of airflow patterns and the forces acting on particles (e.g. the external force, drag force, gravitational force), influence on the behaviour of the particles. To determine a particle motion

in a gas or mostly common operation in ambient air, the review of Stokes' Law and its breakdown in the regime of very small or large particles is presented in this section for better understanding of the motion of the particle of interest in damped microparticle ion traps.

3.3.1 Drag force on Stokes' Law

In fluid mechanics, the determination of Stokes' Law describes the motion of a small spherical object in a viscous fluid. The law, first developed by George G. Stokes in 1851, is derived by considerations of the force acting on a sphere at very small Reynolds numbers Re (e.g. very small particles) by solving the Navier-Stokes equations. The total drag force exerted by fluid on a spherical particle is derived as

$$F_D = 6\pi\eta R_p u\,, \tag{3.34}$$

which is called Stokes' Law [138] where

F_D is the friction force (or the total drag force exerted by the medium on the sphere),

η is the dynamic viscosity of the medium (Pa.sec or kg/ms),

R_p is the radius of spherical object (in m), and

u is the velocity of the sphere relative to the fluid (m/s).

From Equation (3.34), it can be seen that the drag force is proportional to the particle radius. In addition, Stokes' Law applies the following assumptions in the consideration of the behaviour of a particle in a fluid and the validity of Stokes' law [138]. These include

(i) laminar flow which is defined as a condition where fluid move particles along in smooth paths,

(ii) rigid spheres with smooth surfaces and homogeneous (uniform in composition) material, and

(iii) particles do not interfere with each other, and not in compressed air or gas systems.

In such a case, Stokes' Law is only valid for non-turbulent flow with low Reynolds numbers. So the Reynolds number of the flow must be calculated first in order to determine whether the use of Stokes' Law (Equation (3.34)) to calculate the drag force is applicable.

3.3.2 Reynolds number

To understand particle trajectories in air or gas flow, the determination of the gas flow patterns interacting to the particle whether it is smooth or turbulent is needed. The Reynolds number (Re) is a dimensionless parameter used to determine the flow pattern characteristics by the ratio of inertial force to viscous forces in a fluid, and to predict the flow pattern in different fluid flow situations such as a liquid (or gas) flowing in a pipe, channel or similar, or a very small object (e.g. blood cells, aerosol particles etc.) flowing in fluid. The classification of the different flows can be distinguished by the definition of the Reynolds number. In general, a flow can be laminar, turbulent or transition in nature. For the flow passing through a small spherical object, the Reynolds number (Re) can be defined based on the sphere's dimension [138] as

$$Re = u_0 D_p/\nu = 2\rho u_0 R_p/\eta \ , \tag{3.35}$$

where the terminal velocity v is given by

$$u_0 = \frac{g D_p^2 (\rho_p - \rho_m)}{18\,\eta}, \tag{3.36}$$

u_0 is the velocity of the object relative to the fluid (m/s),

η is the dynamic viscosity of the fluid (Pa.S or N.s/m^2 or kg/m.s),

ν is the kinematic viscosity of fluid ($\nu = \eta/\rho$, m^2/s),

ρ_m is the density of the medium (g/cm^3 or kg/m^3),

ρ_p is the density of the particle (g/cm^3 or kg/m^3),

R_p, D_p is the spherical object dimension in radius and in diameter, and

g is the acceleration of gravity (9.81 m/s^2).

3.3.3 Knudsen number

Another determination of dimensionless parameter associated with the nature of the suspending medium (fluid) relative to a particle dimension is the Knudsen number (Kn). Since aerosol particles are small (typically in nanometre scale), the particle size is often comparable to the distance of the surrounding medium molecules travelling between collisions with other gas molecules referring to the mean free path (λ). The Knudsen number (Kn) is given by [138],

$$Kn = \lambda / D_p \ , \tag{3.37}$$

where λ is a mean free path of the fluid (in metre) which is the average distance travelled by a molecule before collision with another gas molecule, and D_p is a particle size in diameter. The gas-particle interaction can be classified into different regimes depending on the particle size compare to the mean free path of fluid. Using Equation (3.37), the flow regimes are defined as below.

(i) If the particle size is much larger than the mean free path, $Kn \ll 1$ is classified to the continuum regime and the drag force is valid by Stokes' Law.

(ii) If the particle size is significantly smaller than the mean free path of gas molecules resulting in $Kn \gg 1$, then it is called the free molecule or kinetic regime.

(iii) For any intermediate particle size range between these two regimes, it is called the transition regime which is typically $0.1 < Kn < 3$.

3.3.4 The empirical drag coefficient and slip correction factor

For small Reynolds number ($Re \ll 1$) and small Knudsen number ($Kn \ll 1$), the drag force in Equation (3.34) obeys Stokes' Law. Otherwise the drag force determined by the Stokes' Law becomes inaccurate either because it is under-estimated (large Re) or is over-estimated (large Kn). Therefore, more accurate solutions of drag force over the entire range of the Reynolds number and Knudsen number regimes can be obtained by introducing the terms called an empirical drag coefficient C_D and a slip correction factor C_C. Beyond the Stokes

region the expressions of the empirical drag coefficient and the slip correction factor are required. To account for the accurate drag force for each range of Reynolds number, Flagan and Seinfeld [138] suggested the expression of the drag force of Stokes' Law from the experimental results in term of an empirical drag coefficient C_D,

$$F_{drag} = \frac{\pi}{8} C_D \rho D_p^2 u^2 , \tag{3.38}$$

where

$$C_D = \begin{cases} \dfrac{24}{Re} & Re < 0.1\ (Stokes'Law) \\ \dfrac{24}{Re}\left(1 + \dfrac{3}{16}Re + \dfrac{9}{160}Re^2 \ln 2Re\right) & 0.1 < Re < 2 \\ \dfrac{24}{Re}(1 + 0.15Re^{0.687}) & 2 < Re < 500 \\ 0.44 & 500 < Re < 2 \times 10^5. \end{cases} \tag{3.39}$$

When a particle diameter ($2R_p$) approaches the same order as the mean free path λ of the suspending fluid (i.e. air $\lambda = 65$ nm), the Knudsen number becomes large in turn and the drag force is found to be over-estimated by Stokes' Law prediction in Equation (3.34). Thus an empirical slip correction factor is introduced to correct Stokes' Law for a progressively lower-than-predicted drag force as Kn increases when R_p gets smaller and smaller (non-continuum regime),

$$F_{drag} = \frac{6\pi\eta R_p V}{C_C} \tag{3.40}$$

where C_C has the general form

$$C_C = 1 + Kn\left[\alpha + \beta exp\left(-\frac{\gamma}{Kn}\right)\right]. \tag{3.41}$$

Many theorists investigated the values of parameters α, β, γ based on Milikan's original values corrected with the improved values of mean free path for gas molecules in dry air. Allen and Raabe [139] fully re-evaluated the Millikan's results using oil drops and micrometre-size polystyrene spheres. Even though there are several analyses for the slip correction factors, the maximum difference in the different set of parameters (α, β and γ) is found to be $\approx$ 2% over the Kn range of 0.001 to 100. These reviews give options to choose

a different set of parameters (α, β and γ) based on Kn range and the particle size of interest. For this work, the set of parameters from the work of Allen and Raabe [139] and Hutchins et al. [140] are the most suitable for the experimental work with solid spherical particles of diameter ranging from 1 μm or larger. The value of the slip correction in the air at 289 K and 1 atm as a function of particle diameter was experimentally investigated by Flagan and Seinfeld [138]. For a particle with a diameter range between 5-20 μm, drag force can be accurately defined by Stokes' Law as shown in Table 3.1.

Table 3.1 - The values of the slip correction C_c and drag coefficient C_D in air at 289 K and 1 atm as a function of particle diameter. (Table modified from ref. [138].)

D_p(μm)	Kn	C_C
0.01	13.02	22.7
0.05	2.60	5.06
0.1	1.30	2.91
0.5	0.26	1.337
1	0.13	1.168
5	0.03	1.034
10	0.01	1.017

D_p(μm)	Re	C_D
20	0.02	1.00
60	0.04	1.06
100	2	1.24
300	20	2.17

3.3.5 Damping effects on the Mathieu's equation and stability diagram

For any experiments performed under atmospheric pressure, the motion of particles in the trap is strongly dampened by the surrounding air flow. The drag force is always presented unless the particle is confined in a vacuum system. To calculate the drag force exerted by a medium (fluid or gas) on a particle, the equations of motion in Equation (3.21) is derived by including the damping (or drag) effects on the Mathieu's stability given by Spann et al. [141], Pearson et al. [60], Flagan and Seinfeld [60], and Winter and Ortjohann [142],

$$\frac{d^2u}{d\zeta^2} + b\frac{du}{d\zeta} + (a_u - 2q_u\cos 2\zeta)u = 0. \tag{3.42}$$

In an electrodynamic balance, the equation of motion in the axial direction associated with the gravity force mg and the drag force F_D is

$$m\frac{d^2z}{dt^2} = F_D - mg. \tag{3.43}$$

The expression of the drag force F_D under Stokes' Law is given by

$$F_D = 6\pi\eta R_p u. \tag{3.44}$$

The drag effect term ($b\frac{du}{d\zeta}$) accounts for friction and depends linearly on the velocity u, where b is the dimensionless drag coefficient [141], [142] expressed as

$$b = \frac{9\eta}{\rho R_p^2 \Omega_T} = \frac{12\pi\eta R_p}{m\Omega_T} \tag{3.45}$$

where R_p is the radius of spherical particle with the density of particle ρ and the viscosity of medium η.

In any non-Stokes' Law regime that has a large Reynolds number Re and Knudsen number Kn, the dimensionless drag coefficient (damping constant) can be derived by introducing the terms called an empirical drag coefficient C_D of Re and a slip correction factor C_C of Kn [83], [142],

$$b = \frac{12\pi\eta R_p\, C_D}{m\Omega_T}\ , \qquad b = \frac{12\pi\eta R_p}{C_C m\Omega_T}. \tag{3.46}$$

Winter and Ortjohann [142] investigated the stability under a strongly damped system and numerically derived the Mathieu's equation with damping term using a numerical Runge-Kutta method. The particle of interest was anthracene dust particles with 30 μm in diameter and density ρ = 1.28 g/cm^3 with η (air) = 1.8 $\times 10^{-4}$ P. Using Equation (3.45), the dimensionless drag coefficient is equal to b = 1.8. Figure 3.7 shows the resultant stability studies of which the maximum parameter q (or q_{max}) increases with the dimensionless drag coefficient b. As seen, the limit of stability from q_{max} = 0.908 (for undamped conditions or in a vacuum, b = 0), extends to q_{max} = 2.13 (for b = 1.8). In this case, the damping effect increased the limit of stability by a factor of 2. Winter and Ortjohann [142] also found the relationship of damping constant and particle dimension as $b \sim R_p^{-2}$, suggesting that the smaller particle has the larger stability range with the same specific charge. Pearson et al.

[60] also studied the effect of drag force on the stability parameter by deriving the slip correction factor of 44 nm diameter particles trapped in a surface-electrode trap. The result showed that the maximum stable Mathieu parameter q at $a = 0$ increase from $q_{max} = 0.908$ at $b = 0$ to $q_{max} = 1.05$ at $b = 0.45$ which was considered to be only a small effect of air drag on the trap stability. However, the speed of macroscopic ion motion in the shuttling experiment was significantly affected by air drag despite the fact that the trap stability was not affected by damping.

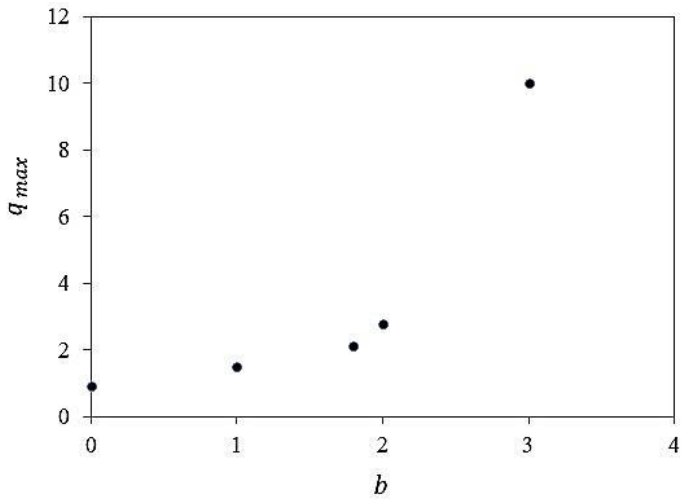


Figure 3.7 – The maximum stability parameter q_{max} for obtaining bound motion in the quadruple ion trap in dependence on the dimensionless drag coefficient (damping constant) b defined by Equation (3.45). (Figure from ref. [142].)

3.4 Summary

The principle of electrodynamic confinement of charged particles using a combination of static (DC) and oscillating (AC) electric fields corresponding to the 2D and 3D quadrupole ion-trap configurations (RF Paul traps) is described. The equations of motion for a charged particle or an atomic ion confined in RF Paul traps can be treated in two ways: as the completed solutions of the Mathieu's differential equation, or as the solutions of the pseudopotential approximation. The numerical solutions of the Mathieu's equation provide insights the ion trajectory and stability, while the use of the pseudopotential approximation is more practical for the optimization of the trap design. Trap properties such as the pseudopotential well depth and the secular frequencies corresponding to the trap parameters (i.e. trap size, stability) and the operating conditions (i.e. the drive voltages and frequencies) can be defined using the numerical simulations for the pseudopotential approximation as will be presented in Chapter 4.

The study of microparticle trapping in RF Paul traps as a function of damping (drag force) is examined by Stokes' Law associated with the Reynolds number and the Knudsen number. When the value of the evaluated Reynolds number or Knudsen number is too large for Stokes' Law analysis to be valid, the adjustment for Stokes' Law by introducing the terms called the empirical drag coefficient and the slip correction factor is required for the accurate determination of the drag force on the particles. Then the derivation of the Mathieu's equation and the maximum stability parameter q for charged particles under the damping of the air is described. The relationship between the dimensionless drag coefficient (damping constant b), the maximum value of the Mathieu stability q parameter (q_{max}), and the particle size can be used to indicate the degree of the air drag effect on the trap stability and the experimental demonstration of microparticle trapping aimed to be conducted in ambient air as will be described in detail in Chapter 8.

Chapter 4

Analytical models and numerical simulations of surface-electrode ion traps

Working towards the realisation of scalable ion-trap architectures for quantum computing and information processing reviewed in Chapter 2, the mathematical tools are normally used for the design and optimisation of the proposed trap geometry. The electric field curvature and potential of the prototype geometry, in particular the design of arrays of surface-electrode ion traps (SEITs), can be analysed both analytically and numerically. First, the analytical model for calculating the electrostatic fields and relevant trap parameters of a basic SEIT layout in the gapless plane approximation proposed by House [143] is described. This model is suitable for relatively simple trap structures with rectangular shaped electrodes such as a four-wire and a five-wire geometry [80]. For arbitrary configurations containing more complex trap geometries, the numerical simulation is commonly used instead. A description of the two most commonly used numerical methods for ion-trap numerical simulations - finite element method (FEM) and boundary element method (BEM) - is outlined. Design considerations for the SEIT designs are discussed. In this work, the BEM is chosen for the comprehensive trap simulations of the proposed SEITs including a Y-junction trap and a 2D hexagonal lattice trap designed by the collaborators at the Ion Quantum Technology (IQT) group, the University of Sussex. The simulation results presented in this thesis were carried out using the "*bemsolver*" software package [144], [145]. This was followed by a detailed numerical analysis of the computed electric fields in the proposed traps using Mathematica

functions. The aim of the use of analytical models and numerical simulations is to obtain insightful information of trap design characteristics and to find a range of experimentally suitable parameters for different operations (e.g. trapping, shuttling, and levitation). Also the analytical prediction of the drag effect to the stability Mathieu's equation when suspending microparticles in ambient air derived in previous chapter (refer Section 3.3) is evaluated with more specific test cases against the experimental conditions discussed in Chapter 8.

4.1 Analytical models for surface-electrode traps

The design of surface-electrode ion traps (SEITs) can be studied analytically using the analytic model developed by House [143]. This model determines the electric potential generated by a series of electrodes residing in a single plane solving the Laplace equation in three dimensions with Dirichlet boundary condition. House's model assumes that an electrostatic field is created by a set of conducting electrodes whose upper surfaces are in the plane $y = 0$, extend infinitely in the x- and z-dimensions, and with infinitely small gaps between electrodes. This assumption is also known as the gapless plane approximation. Figure 4.1(a) presents a drawing of a SEIT configuration in the xy-plane with two RF electrodes and a central electrode that are assumed to be infinitely long in the z-dimension. Two RF electrodes are separated by a central electrode and surrounded by control electrodes which are segmented in the z-dimension. The voltages applied to the individual electrode define the potential $\emptyset(x, 0, z)$ which satisfies the boundary condition [143]:

$$\phi(x,0,t) = \begin{cases} 0 & , \quad x < -c, \\ V_{RF}\cos(\Omega t), & -c < x < 0, \\ 0 & , \quad 0 < x < a, \\ V_{RF}\cos(\Omega t), & a < x < a + b, \\ 0 & , \quad x > a + b. \end{cases} \tag{4.1}$$

The surface-electrode configuration in Figure 4.1 has the potential field,

$$\phi(x,y,t) = \frac{V_{RF}}{\pi}\left[\arctan\left(\frac{a+b-x}{y}\right) - \arctan\left(\frac{a-x}{y}\right) - \arctan\left(\frac{x}{y}\right) + \arctan\left(\frac{c+x}{y}\right)\right]\cos(\Omega_{RF}t). \tag{4.2}$$

The 2D pseudopotential well of a five-wire design with RF electrodes of equal width ($b = c$) obtained from Equation (4.2) is graphically illustrated in Figure 4.1(b). In SEITs, the position of the local minimum or RF nil is where a charged particle (or an ion) will be trapped. The trapping position is located at a distance h (ion height) above the surface in the y-direction and x_0 in the x-direction. In the absence of any static potential, the pseudopotential well depth (also called trap depth) defined as the amount of energy needed for an ion to escape from trap region can be represented by the difference between the pseudopotential at the "*RF nil*" (typically zero) and the "*turning point*", also called the "*escape point*" as shown in Figure 4.2. The position of the RF nil point where ions are trapped and the turning point where ions escape from the trapping potential and be ejected, can be found by calculating where the gradient of the pseudopotential is zero.

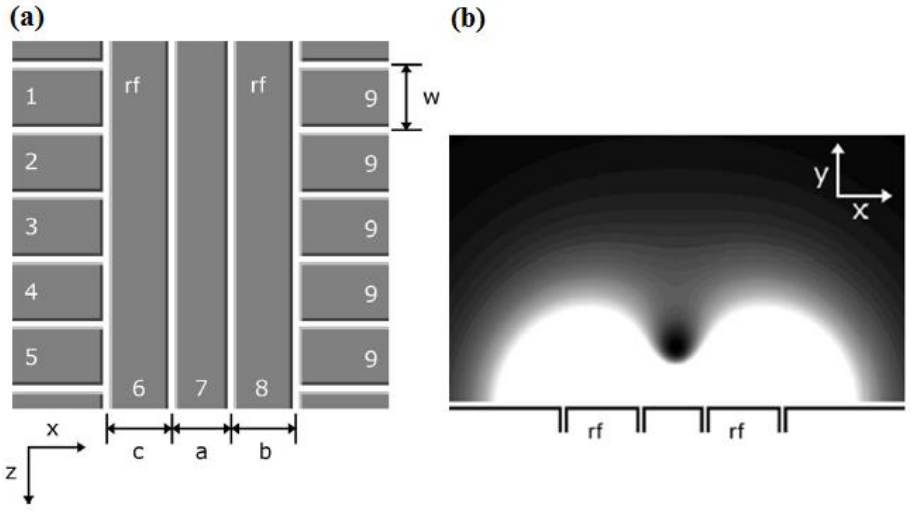


Figure 4.1 – The five-wire electrode configuration used in House's analytical models for electrostatic potential fields in surface-electrode traps. (a) The electrode layout in the xz-plane. (b) Illustration of the pseudopotential well with the local minimum representing the ion position above the centre electrode located between two RF electrodes. (Figure from refs [143].)

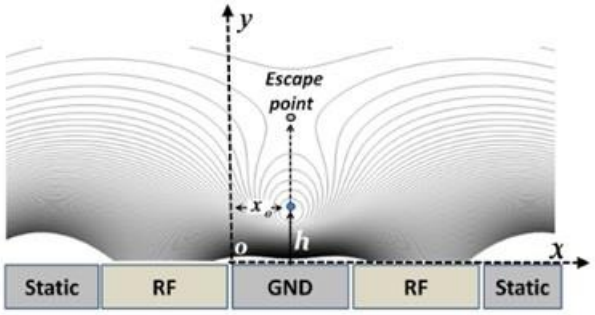


Figure 4.2 – Illustration of the pseudopotential well created by the electric fields of a symmetric five-wire design. The trapping position is located at (x_0, y_0) coordinate with a distance h above the surface. The positions of the trapped ion and turning point (or escape point) can be calculated using Equation (4.3) and (4.4) respectively. (Figure from ref. [146].)

In the xy-plane, an ion is confined at the trapping point where the absolute value of the peak RF electric field is minimal. The coordinates of the trapping point (x_0, y_0) are given by

$$x_o = \frac{ac}{(b+c)}$$

$$y_o = \frac{\sqrt{abc(a+b+c)}}{b+c}. \tag{4.3}$$

The pseudopotential at the escape point is normally used to calculate the depth of pseudopotential well (trap depth) (D). The coordinates of the escape point (x_E, y_E) are approximated to be

$$x_E = \frac{a}{2}$$

$$y_E = \frac{\sqrt{2ab + a^2 + 2(a+b)\sqrt{2ab + a^2}}}{2}. \tag{4.4}$$

Nizamani and Hensinger [146] also derived the trap depth for a given ion height h obtained from Equation (4.3) and the geometric factor κ based on the House's model,

$$\psi_E = \frac{QV_{RF}^2}{\pi^2 m \Omega_{RF}^2 h^2}\,\kappa, \tag{4.5}$$

where κ is given as

$$\kappa = \left[\frac{2\sqrt{abc(a+b+c)}}{(2a+b+c)\left(2a+b+c+2\sqrt{a(a+b+c)}\right)}\right]^2. \tag{4.6}$$

The Mathieu parameter q (with $a = 0$) obtained from the second derivatives of the field at the centre trapping point are

$$q_{11} = -q_{22} = \frac{-4QV_{RF}}{\pi m\Omega^2}\frac{a^2(b^2-6bc+c^2)+a(b+c)(b^2-6bc+c^2)-bc(b+c)^2}{(a+b)^2(a+c)^2\sqrt{abc(a+b+c)}}$$

$$q_{12} = -q_{21} = \frac{-4QV_{RF}}{\pi m\Omega^2}\frac{(b-c)(2a+b+c)}{(a+b)^2(a+c)^2}. \tag{4.7}$$

These analytical expressions can be used to compute the ion height, trap depth and stability parameter q for the proposed Y-junction trap in comparison with the numerical simulation in Section 4.4.2. However, House's model is limited only to SEITs with a rectangular shape. Any complex structures like junctions or 2D lattices still rely on the numerical simulations to solve the electric potentials and other relevant trap properties.

4.2 Numerical methods for surface-electrode traps

Calculations of the secular frequencies and trap depths require detailed knowledge of the potentials and electric fields near the trap axis. There are several primary forms of numerical method commonly used for solving various physics problems (e.g. electromagnetic fields, heat transfer, and mechanical stress). In ion trapping application, solutions of second-order differential equations of electric potentials (Laplace's equation) in Equation (3.32) can be numerically solved by various methods. The three most common uses of numerical methods for ion-trap simulations include the Finite Difference Method (FDM), the Finite Element Method (FEM), and the Boundary Element Method (BEM). Of these three methods listed above, the FDM is straightforward to implement but the calculations require very fine grid spacing resulting in greater computational resources than other methods. The FDM and FEM are

volume-discretisation methods which determine the electric fields of electrodes by constructing a "*mesh*" over the modelled volume of interest. Therefore, the entire domain mesh is required and the solution of entire domain point is calculated respectively.

In BEMs, a mesh of the boundary is required and the solution on the boundary is calculated. The calculation is based on charge distributions on electrodes which need to be meshed into a set of smaller triangular or rectangular segments. When the surface charge distribution is known, the electric fields and potentials can be simulated. The reduction in size of mesh is by one dimension resulting in the need for less time-consuming and less computation resources by using BEM analysis. This is considered to be a significant advantage for ion-trap simulations solving electrode surface only (2D matrices) instead of the entire trapping volume (3D matrices). The BEM analysis has proven to be more efficient and accurate for modelling ion-trap arrays due to no discontinuities while the solutions found from FDM or FEM often involve discontinuous potentials at the edges of electrodes [129].

There are several commercial software packages implemented with these three methods: COMSOL Physics (FEM), Anasofts Maxwell 3D (FEM), Charged Particle Optics - CPO 3D (BEM), SIMION (FDM). Other non-commercial programs such as the BELA program (a two-dimensional finite element electrostatic package) [83] and the bemsolver software package written for the open source [129], [135] were also used in the design and optimisation of SEITs. In the following, the use of bemsolver to simulate the electrostatic fields of the physical ion-trap geometries followed by the data analysis of pseudopotentials and trap characteristics obtained from Mathematica notebooks are demonstrated in the following sections.

4.2.1 Bemsolver (ROOT C^{++} compiler)

All trapping potential simulations presented in this work were performed using the "*bemsolver*" software package developed by Singer et al. [144] and the main scripts and executable files are supplied as supplementary online material [145]. The bemsolver is a numerical tool that uses the boundary element method (BEM) to generate the electric potentials of individual electrodes. The bemsolver has one significant advantage over the CPO

with its ability to import the electrode structure from a .dxf file format directly. This allows ion-trap geometries to be drawn in computer-aided design software (e.g. AutoCAD, TurboCAD, and SolidWorks). It is important that the electrode geometry is drawn using four-sided 3D Polylines, and for each individual electrode, a unique layer must be assigned. An electrostatic simulation involves calculating the potential of the "*electrode basis functions*" with one volt (1 V) applied to one of the electrodes while the others remain at ground. This process is repeated for each electrode, thereby producing a set of electrode basis functions that describes the spatial properties of the potential produced by each electrode. The solution for an arbitrary set of potentials on the control (DC) electrodes is then a linear combination of these one-volt solutions. The simulated potential of each electrode is sampled by a grid of points in space, and exported to a file that can be used for further analysis. The output format contains a set of coordinates of (x, y, z) followed by the extracted potential values. Figure 4.3 shows a meshed 3D drawing of Y-junction electrode geometry (in .dxf format) initially constructed by Sterling. Each individual electrode is assigned to a unique layer used to simulate the electrode basis functions.

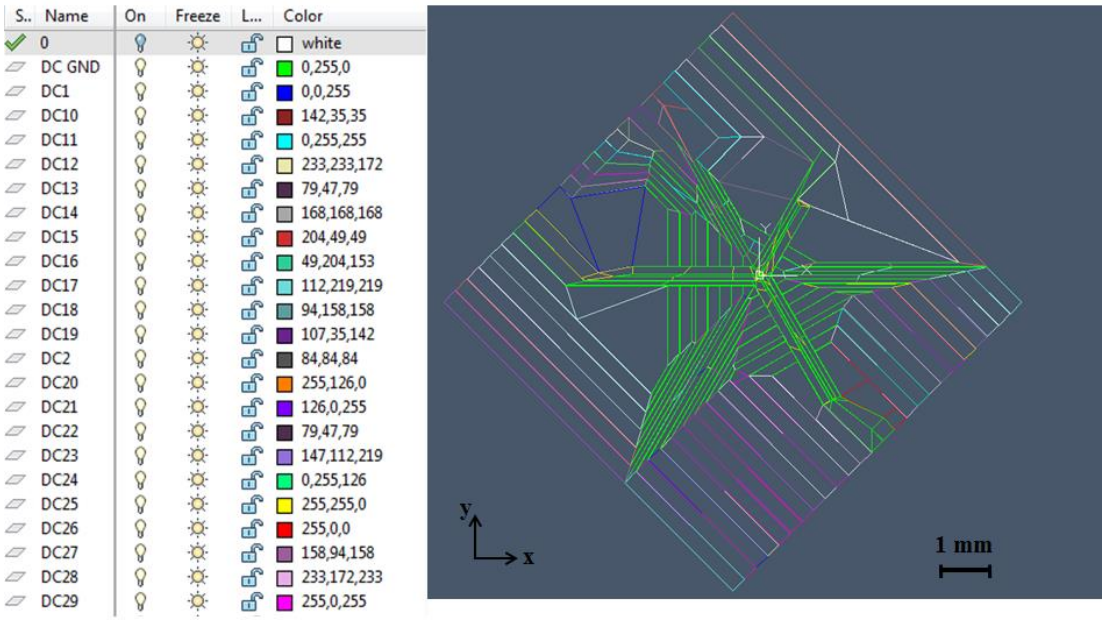


Figure 4.3 – A drawing of Y-junction electrode geometry in 3D Polylines. Each electrode is assigned to a unique layer using Solidworks and TurboCAD.

4.2.2 Pseudopotential approximation by Mathematica analysis

After completing the numerical simulations of the electrode basis functions using bemsolver, the simulated data are imported to a mathematical analysis program called Mathematica. The pseudopotential of the prototype trap is computed by combining the potentials of the electrode basis functions using Equation (3.32). With this method, a variety of trap designs cad be evaluated with minimal simulation time while retaining the simplicity of only using one set of electrode basis functions. The data extracted from bemsolver has the format of x, y, z position followed by the computed potentials. The raw data of x, y, z position are in millimetre scale by default, so this must be converted to metre scale for any subsequent analysis. To compute the pseudopotential, the data points of the electrode basis functions are first interpolated using the Mathematica "*Interpolation*" function. The interpolation functions of both RF(x, y, z) and DC(x, y, z) presenting the RF and DC electrode basis functions can now be substituted in Equation (4.8). The total pseudopotential, $\psi(x, y, z)$ is then given by

$$\psi(x,y,z) = \frac{Q}{4m\Omega_T^2}\left|\frac{\partial\left(V_{RF}RF(x,y,z)\right)}{\partial x} + \frac{\partial\left(V_{RF}RF(x,y,z)\right)}{\partial y} + \frac{\partial\left(V_{RF}RF(x,y,z)\right)}{\partial z}\right| + Q(V_{DC1}DC1(x,y,z) + V_{DC2}DC2(x,y,z) + \cdots), \tag{4.8}$$

where V_{RF} and V_{DC} are the amplitude of the voltages applied to RF and DC electrodes respectively.

To calculate the secular frequencies and trap depth, the RF nil point and the turning point are defined first by calculating the gradient of the pseudopotential Equation (4.8) with respect to x, y, z coordinates using "*dervx, dervy, dervz*" terms in Mathematica function for Equation (4.9).

$$f_{turn}(x,y,z) = \frac{\partial\psi(x,y,z)}{\partial x} + \frac{\partial\psi(x,y,z)}{\partial y} + \frac{\partial\psi(x,y,z)}{\partial z} \tag{4.9}$$

At the RF nil and turning points, the $f_{turn}(x, y, z)$ function is equal to zero and can be solved by using "*FindRoot*" function to find the position where the values of $f_{turn}(x, y, z)$ are equal to zero, which will provide the position of the RF nil or turning points. For example,

the FindRoot functions based on the initial guess values of 75 μm and 150 μm provide more accurate values of the ion height at 74.8058 μm and the turning point at 148.894 μm.

$$\text{FindRoot}\left[f_{turn}(x,y,z),\{\{x,0\},\{y,0\},\{z,75\times10^{-6}\}\}\right]$$

FindRoot function will return the RF nil point as {-0.00116006, -0.0000116237, 0.0000748058}.

$$\text{FindRoot}\left[f_{turn}(x,y,z),\{\{x,0\},\{y,0\},\{z,150\times10^{-6}\}\}\right]$$

FindRoot function will return the turning point as {-0.00111715, -0.0000130626, 0.000148894}.

To find the trap depth (D), the pseudopotentials at the RF nil and turning points need to be determined using Equation (4.8) and the computed ion height and turning point in the x, y, z coordinates obtained from the FondRoot solutions above. The trap depth is then equal to $D = \psi_{Turning}(x,y,z) - \psi_{RF\,nil}(x,y,z)$. Following the expression in Equation (3.3), the secular frequencies ($\omega_{x,y,z}$) can be approximated by calculating the second derivate of Equation (4.8), and divide the result by the ion (particle) mass m.

$$\begin{aligned}\omega_x &= \left(\frac{Q^2}{4m^2\Omega^2}\frac{\partial^2\psi(x,y,z)}{\partial x^2}\right)^{1/2}\\ \omega_y &= \left(\frac{Q^2}{4m^2\Omega^2}\frac{\partial^2\psi(x,y,z)}{\partial y^2}\right)^{1/2}\\ \omega_z &= \left(\frac{Q^2}{4m^2\Omega^2}\frac{\partial^2\psi(x,y,z)}{\partial z^2}\right)^{1/2}.\end{aligned} \tag{4.10}$$

Evaluating Equation (4.10) corresponding to the resultant RF nil position obtained from the FindRoot function will give the three secular frequencies (along the principal axes of the pseudopotential). The Mathematica notebook used to evaluate the trap parameters including the pseudopotential, trap depth, secular frequencies, trap height, escape point and stability q parameter can be found in Appendix A.

4.2.3 Simulation of a five-wire rectangular electrode geometry

At first, initial simulations are carried out to investigate the suitability of the bemsolver software for analysing trapping potentials. Figure 4.4 shows the simplified geometry used in the first set of simulations to compare the numerical method using bemsolver and Mathemetica software with the analytical model by House [143] described in Section 4.1. A basic five-wire SEIT used in this study consists of two-symmetrical RF electrodes ($b = c =$ 120 μm) and a centre ground electrode ($a = 100$ μm) located in between these two RF electrodes and two DC control electrodes at the outer edges. Using House's analytical model, this trap geometry gives the ion height y_0 of 92 μm and the escape point (turning point) y_E of 170 μm above the surface. The geometric factor κ is found to be ≈ 0.015. Assuming the trapped ion is a single ionized strontium atom $^{88}Sr^+$ (similar to House's) with a charge $Q = 1.6 \times 10^{-19}$ C and mass $m = 1.46 \times 10^{-25}$ kg and the RF voltage $V_{RF} = 300$ V at frequency $\Omega_{RF}/2\pi = 50$ MHz, the trap depth is calculated to be ≈ 0.184 which corresponds to the stability parameter $q = 0.23$.

Next, the potential inside the trap is numerically calculated using bemsolver. The resultant potential fields are then used to compute the pseudopotential and other trap parameters by Mathematica functions. The FindRoot functions provide the ion height of 95 μm and the escape point of 176 μm. The trap depth can be calculated by finding the difference of pseudopotentials between the RF nil and escape points. The results of House's model analytical analysis and the numerical simulation using bemsolver and Mathematica are summarised in Table 4.1. This shows that both methods produce similar results and are suitable to determine the trapping potential, trap height and trap depth of the basic SEIT geometries. However, the small deviation of the ion position is due to the fact that the simulated five-wire trap geometry contains 10 μm gaps between electrodes similar to the realistic geometries, and the analytical solutions are based on the gapless plane approximation. In Figure 4.4, the trap point and the escape point obtained from the numerical simulation are marked by white cross marks at 95 μm and 176 μm above the electrode surface.

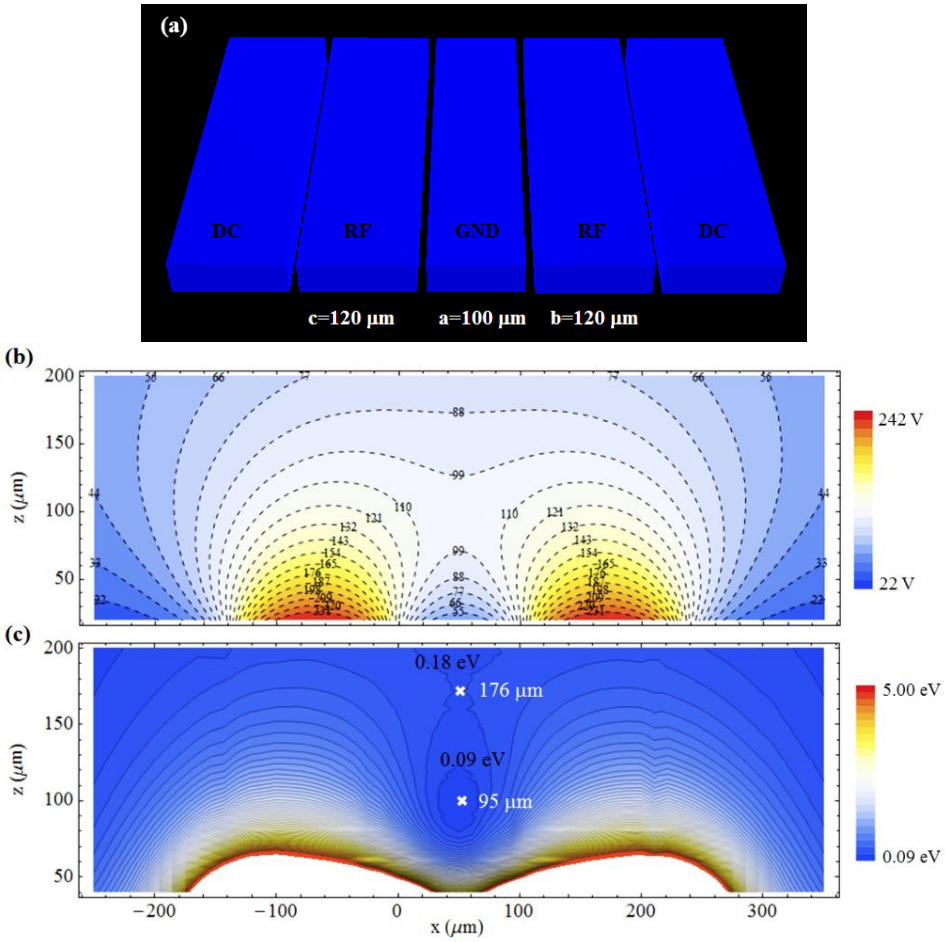


Figure 4.4 – Simulation of a five-wire design with equal RF electrode width. A RF voltage V_{RF} = 300 V at frequency $\Omega_{RF}/2\pi$ = 50 MHz is applied to the RF electrodes. (a) Electrode layout. (b) A 2D contour plot of RF potential. (c) A 2D contour plot of RF pseudopotential with the ion height at 95 µm and the escape point at 176 µm above the surface. Trap depth is estimated to be ≈ 0.18 eV.

Table 4.1 - Comparison of the analytical (House's model) and numerical results of a five-wire SEIT design with an equal width of RF electrodes.

Electrode Dimension (µm)	Analysis mode	Trap position (x_0, y_0) (µm)	Escape position (x_E, y_E) (µm)	κ Factor -	Trap depth (D) (eV)
a=100 b=120 c=120	Analytical calculation	(50.00, 92.20)	(50.00, 169.66)	0.015	0.184
	Numerical simulation	(50.26, 94.41)	(51.70, 175.84)	-	0.180

$^{88}Sr^{+}$ trapping parameters: RF voltage = 300 V at frequency $\Omega_{RF}/2\pi$ = 50 MHz

4.3 Design of surface-electrode ion traps

In this work, two designs of surface-electrode ion trap (SEIT) array were proposed by Robin Sterling, a former PhD. student at the Ion Quantum Technology (IQT) group, the University of Sussex. First, a Y-junction trap array is based on an asymmetric five-wire trap design with outer segmented DC control electrodes and a Y-shaped junction allowing ions to be transported through the trap arrays. With its ability, the experimental realization of scalable ion-trap quantum computation consisting of four key protocols: linear shuttling, corner (or junction) shuttling, separation and recombination of two or more ions can be achieved in a Y-junction trap. Second, a 2D hexagonal lattice trap is capable of trapping individual ions in a 2D lattice with the ion-ion interacting via the Coulomb force. This makes a 2D lattice trap an ideal candidate for quantum simulations of coupled spins and condensed matter physics.

Trap layout and analytical and numerical simulations of the proposed traps are described in following sections. In the design process, the electric fields of the desired surface-electrode patterns with 3D geometry were simulated using a software package called bemsolver along with the numerical methods of solving the equations and visualising using Mathematica. The simulation results provide insightful information of trapping parameters required for successful operations during the experimental investigation particularly in the initial trials of microparticle loading and trapping with unknown charge-to-mass (Q/m) value.

4.4 A Y-junction trap

4.4.1 Trap design

The design of a Y-junction surface-electrode ion trap is based on a five-wire design with two RF electrodes of unequal widths. For a symmetric five-wire design with equal RF electrode widths as shown in Figure 4.5(b), one of the radial principal axes is perpendicular to the trap surface, which makes that axis difficult to Doppler cool as the cooling laser requires a component of the laser beam to be parallel to the motional axis of trapped ion and to cool

it. Thus a rotation of the principal axis is required for effective laser cooling and can be done by breaking the symmetry of two RF electrodes with unequal width as presented in the proposed Y-junction trap. Furthermore, the addition of a ground electrode between the narrow RF electrode and the segmented DC electrodes results in the uniform trapping fields of pairs of static DC voltages applied at both sides (Figure 4.5(c)).

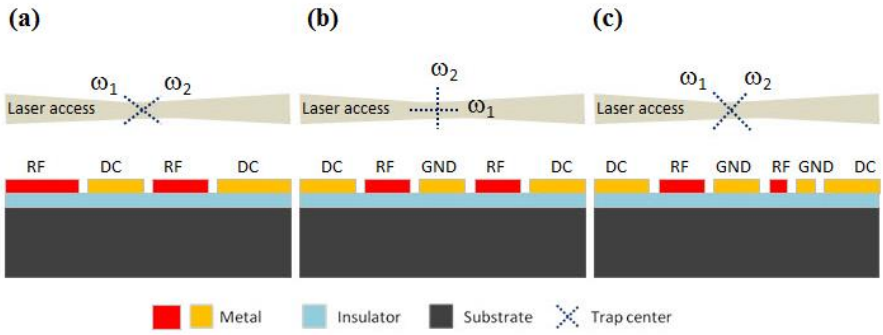


Figure 4.5 – Comparison of the radial principal axes in different surface trap geometries. (a) A four-wire design. (b) A symmetric five-wire design. (c) An asymmetric five-wire design with unequal width of two RF electrodes resulting in a rotation of the principal axis for effective laser cooling.

As shown in Figure 4.6, the Y-junction trap consists of two RF electrodes, two ground electrodes and 44-segmented DC electrodes. Two RF electrodes are asymmetrically designed with widths of 100 μm and 200 μm, along with the central ground and extra ground electrode with a width of 60 μm and 100 μm respectively. This asymmetrical geometry allows a rotation of the principal axis required for effective laser cooling of an ion. To avoid the heating issue, the ion height (RF nil point) h is chosen to be greater than 70 μm. The trap is considered to have three main operating regions: Y-junction (shuttling through the junction), combination and separation (quantum gate operations), and ion storage. To implement successful adiabatic shuttling protocols, it is important to have a smooth shuttling path through the junction. Hence, the RF geometry at the Y-junction region was modified to minimize the RF potential barrier discussed in detail in the doctoral work of Sterling [135]. In addition, a more comprehensive discussion of the optimization of electrode configurations and the arrangement

of static DC electrodes for fast shuttling operation is presented in Nizamani and Hensinger [146].

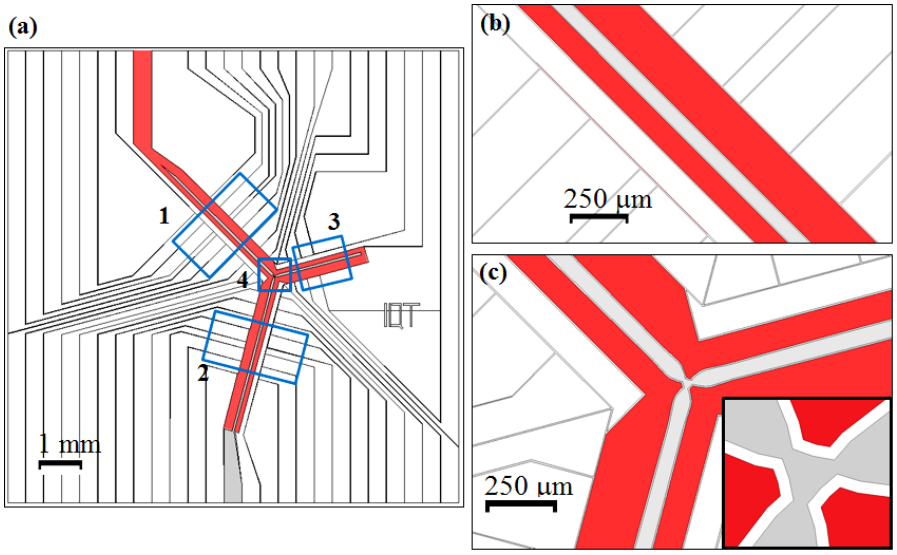


Figure 4.6 – Schematic of the proposed Y-junction surface-electrode ion trap. (a) The entire ion-trap array with four operating regions: ion separation/recombination (zones 1 and 2), ion storage (zone 3) and Y-junction (zone 4). (b) A close-up view of interaction region with narrow DC control electrodes (in white) for separation/recombination. RF electrodes with unequal width (in red) and a centre ground electrode (in grey). (c) A close-up of a Y-junction region. Inset shows the modified RF electrode geometry at the junction to reduce the RF potential barrier. (Figure modified from ref. [135].)

4.4.2 Simulations of the Y-junction trap

The Y-junction trap is assumed to trap $^{171}Yb^{+}$ with the applied RF voltage of 300 V at drive frequency $\Omega_{RF}/2\pi = 50$ MHz, where the numerical simulation gives the trap depth of 176 meV with the stability parameter $q \approx 0.60$ (based on the derivation of an ideal 2D quadrupole ion trap in Equation (3.18)). This trap structure yields the ion height of 75 µm and the escape point at 150 µm above the electrode surface. The radial secular frequencies are $\omega_x/2\pi \approx 4.14$ MHz and $\omega_z/2\pi \approx 4.26$ MHz. Figure 4.7 (a, b and c) shows the trapping region evaluated in this case. The contour plots of the computed potentials and pseudopotentials in the xz-plane at the centre of the top linear section of a five-wire geometry and the RF nil line

at 75 μm above the surface along the y-axis close to the Y- junction centre are shown in Figure 4.7 (d, e and f respectively).

The same data set of electrode basis functions from bemsolver is also used for microparticle trapping. A single microparticle confined in the Y-junction trap is initially assumed to have a size of 20 μm, mass of 20×10^{-9} kg and surface charge of 1.6×10^{-14} C based on the analysis in Yang et al. [147]. This provides a charge-to-mass ratio (Q/m) of 8×10^{-4} C/kg. Due to a much smaller Q/m ratio of the microparticle compared to the ions normally in the order of 10^5 C/kg, microparticle trapping requires the drive frequencies to be in the order of a few hundred up to thousands of hertz compared to ion trapping which typically operates with drive frequencies in the order of 10-100 MHz. For an applied AC voltage (V_{AC}) of 300 V at frequency $\Omega_{RF}/2\pi$ = 2685 Hz and $Q/m = 8 \times 10^{-4}$ C/kg, the trap depth is computed to be 0.088 eV. Upon this trapping condition, the stability Mathieu parameter q is estimated to be 0.30. With decreasing drive frequency to 1900 Hz, the trap depth is increased to 0.144 and the stability parameter q is shifted to 0.60. It can be seen that the trapping parameters used for confining charged microparticles are quite different from those required for ion trapping in the same trap. This is due to the fact that charged particles either have much lower charge or much greater mass those of ions. With a small value of charge-to-mass ratio (Q/m), the confinement of charged particle thus requires a much lower drive frequency for retaining a large AC voltage applied to RF and a small stability parameter q at the same time. Furthermore, the motion of charged particles in the trap region is also noticeably affected by gravity and requires a static electric field to either pull or push them upwards to stably rest at the RF nil point (see further discussion in Chapter 9). The two-dimensional (2D) RF pseudopotential contour plots in the xz-plane of Yb^+ ion trapping in megahertz and charged microparticle trapping in kilohertz are presented in Figure 4.8

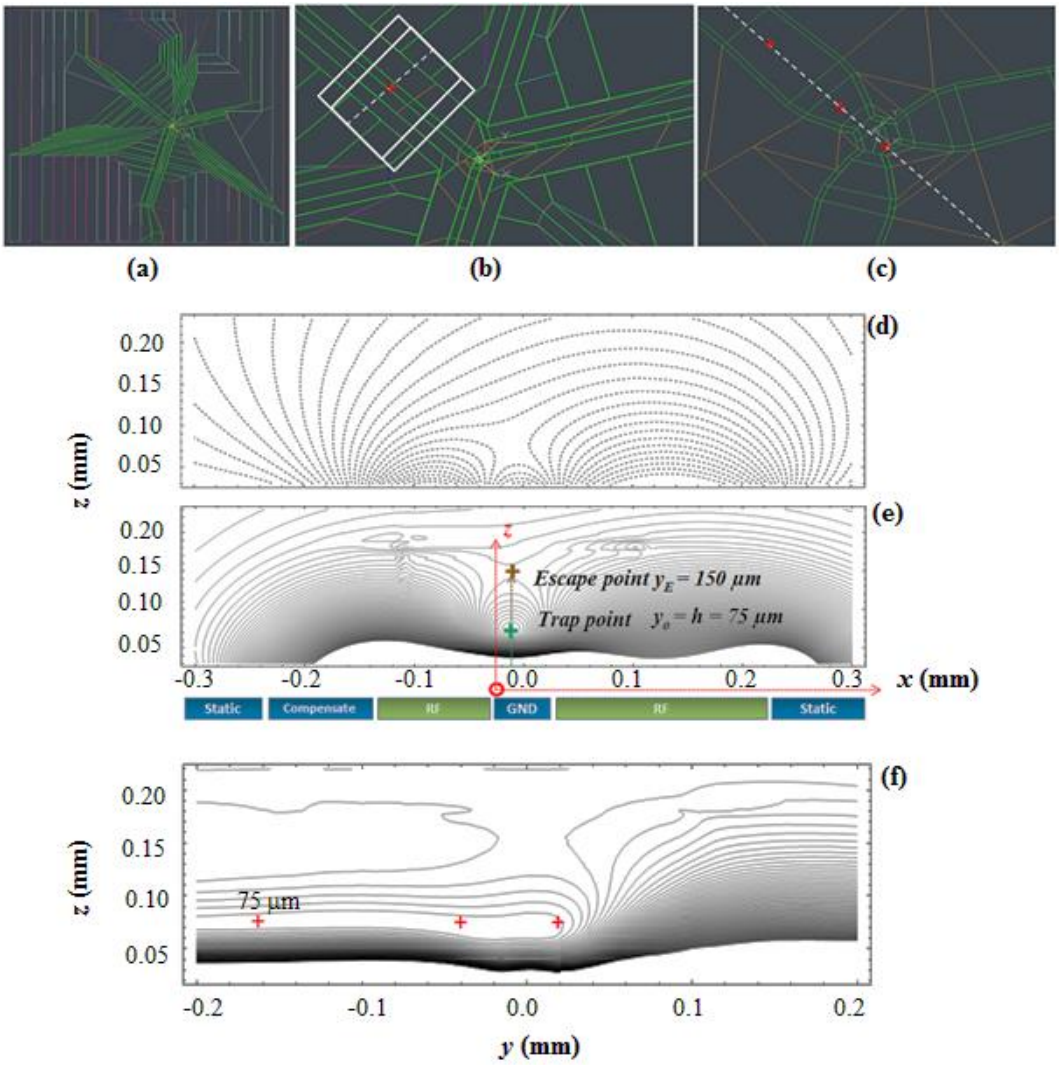


Figure 4.7 – Simulation of the Y-junction trap with the operating parameters: V_{RF} = 300 V at $\Omega_{RF}/2\pi$ = 50 MHz for $^{171}Yb^{+}$ ions. Trap drawings show (a) the entire trap chip and (b-c) the upper linear region used to simulate RF pseudopotentials in the xz-plane and the yz-plane, respectively. (d) A 2D contour plot of the trapping potential with the saddle point. (e-f) 2D contour plots of RF pseudopotential in the xz-plane with the ion height (RF nil point) at 75 μm and the escape point at 150 μm above the surface, and in the yz-plane closed to the junction region and the RF nil line at 75 μm along the y-axis.

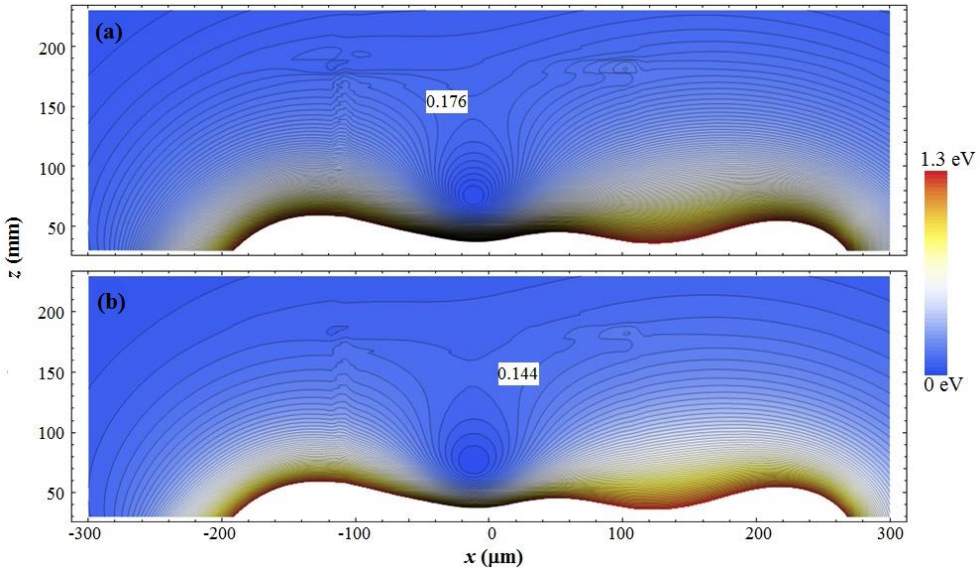


Figure 4.8 – 2D contour plots of pseudopotential in the Y-junction trap for: (a) $^{171}Yb^{+}$ ion, V_{RF} = 300 V at frequency $\Omega_{RF}/2\pi$ = 50 MHz giving the trap depth = 0.176 eV and the stability parameter q = 0.60. (b) A single charged microparticle at a given $Q/m \approx 8 \times 10^{-4}$ C/kg, V_{AC} = 300 V at frequency $\Omega_{RF}/2\pi$ = 1900 MHz giving the trap depth = 0.114 eV and the stability parameter q = 0.60.

4.5 A two-dimensional (2D) hexagonal lattice trap

4.5.1 Trap design

A two-dimensional (2D) lattice trap is based on the concept of a three-dimensional (3D) ring Paul trap which can be transformed to a planar array of ring traps by moving the top ground endcap to infinity and keeping the RF ring electrode and the ground endcap beneath it. A 2D lattice RF plate was first introduced by Clark et al. [116]. This design has a hole diameter of 1.14 mm and hole spacing of 1.67 mm and is supported by a printed circuit board. Furthermore, this millimetre-scale lattice trap was used to trap $^{88}Sr^{+}$ ions and to demonstrate the strength of interactions between microparticles with a diameter of 0.44 μm in different trapping sites. Instead of the circular lattices [116], other lattices such as hexagonal and rectangular were evaluated in Siverns et al. [109].

A 2D hexagonal lattice traps shown in Figure 4.9 contains arrays of hexagonal wells arranged in a honeycomb fashion allowing for trapping of 2D ion lattices which could be useful for quantum simulations of coupled spin system. This ion-trap topology is based on a single RF electrode unlike other works [106]–[108], [148] using multiple independent RF electrodes. The trap consists of 29 trapping sites arranged in a triangular shape. Each trapping site is surrounded by up to six nearest neighbours. The ion-ion distance of 270.5 μm measured from the centre of two adjacent lattices is significantly smaller than Clark's design of 1.67 mm. The hexagonal lattice regions are embedded in a large single RF electrode. The micromotion compensation (DC) electrodes are placed outside the RF electrodes.

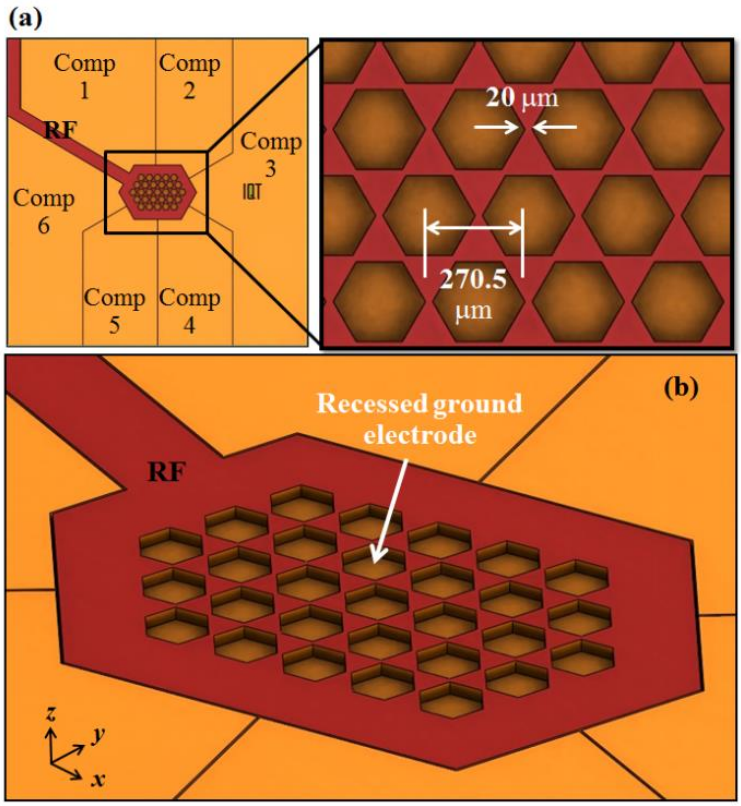


Figure 4.9 – Schematic of the proposed 2D hexagonal lattice trap. (a) The entire ion- trap array with a single RF electrode (red) and six compensation electrodes (orange). Inset shows the ion-ion distance of 270.5 μm. (b) The 2D lattice trap contains 29 trapping sites. The recessed ground electrode is 40 μm below the top electrode surface. (Figure modified from ref. [135].)

4.5.2 Simulations of particle trapping in a 2D lattice trap

Simulations for a 2D hexagonal lattice trap presented in the following sections are mainly focused on the trapping conditions of microparticles used in the experiments described in Chapter 8. With an applied AC voltage V_{AC} = 300 V at frequency $\Omega_{RF}/2\pi$ = 1190 Hz corresponding to the trap depth = 0.11 eV and the stability parameter q = 0.60, the three secular frequencies $\omega_{x,y,z}/2\pi$ are calculated to be 28, 26 and 58 Hz respectively. The ratio of the radial to the axial frequency is found to be $\omega_{x,y}/\omega_z \approx 0.5$ similar to those of surface-electrode ring electrode geometry reported by Kim et al. [112]. The pseudopotential plots in the z-axis of a single hexagonal pseudopotential well as shown in Figure 4.11 illustrates that the particle is trapped at 117 μm above the trap surface with the escape point at 247 μm. The pseudopotential plots of the x-axis and y-axis are symmetric. Pseudopotential simulations extended to multiple lattices in the x-axis and y-axis illustrate the RF potential barrier of 0.30-0.35 eV between the adjacent lattice sites. 3D pseudopotential contour plots of a single lattice (Figure 4.11(d)) and multiple lattices (Figure 4.11(a)) show that the pseudopotential minimum (RF nil) locates at the centre of all individual lattices and the pseudopotential well increases significantly towards the electrode surface.

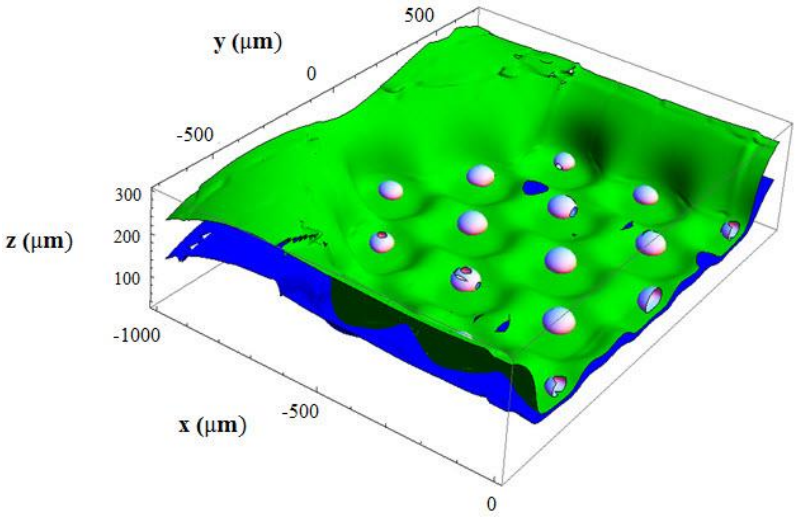


Figure 4.10 – A 3D contour plot of pseudopotential from half of the 2D trap array with V_{AC} = 300 V at $\Omega/2\pi$ = 1190 Hz. The equipotential surface corresponds to: white = 0.05 eV, green = 0.50 eV and blue = 1.0 eV. The circular dots (white) represent the particle's position at the pseudopotential minimum.

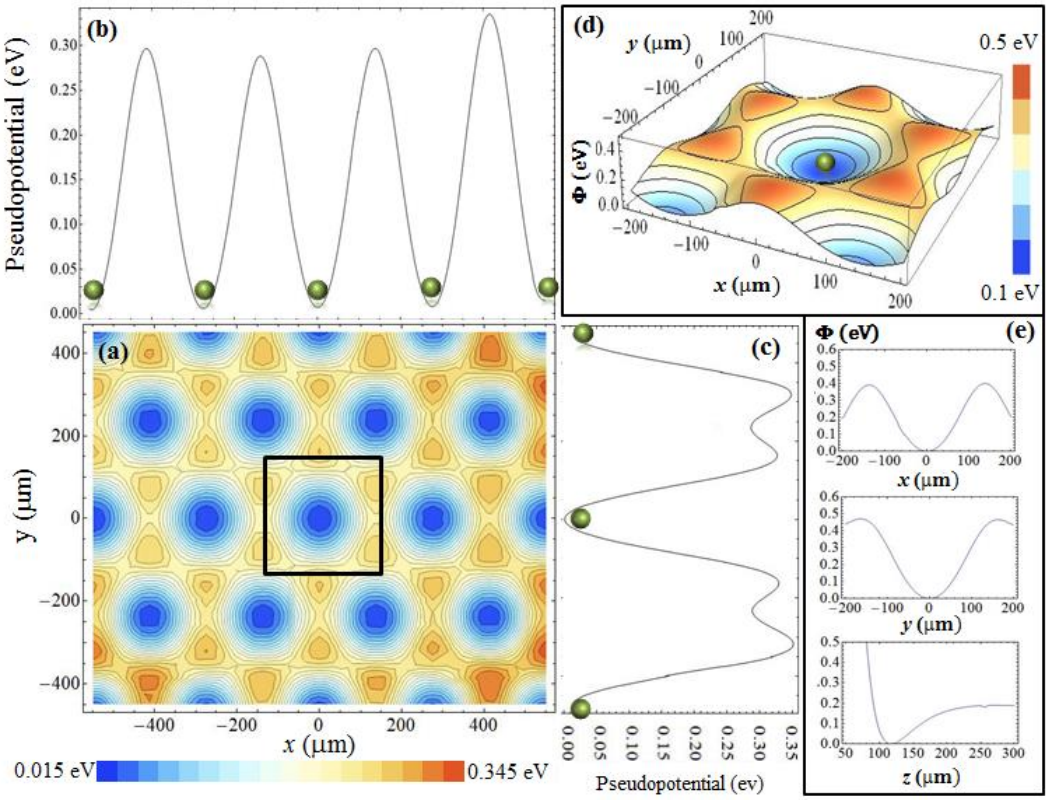


Figure 4.11 – Simulation of the 2D hexagonal lattice trap. (a) 2D contour plots of pseudopotential in the xy-plane at z = 117 μm (trap height) over the central 11 trap sites with V_{AC} = 300 V at $\Omega/2\pi$ = 1190 Hz, $Q/m \approx 8 \times 10^{-4}$ C/kg, stability parameter $q \approx 0.60$, and trap depth = 0.18 eV. (b-c) Pseudopotential plots in the x-axis with five lattice sites, and in the y-axis with three lattice sites. Green dots depict trapped particles at the pseudopotential minimum (RF nil). Insets: (d) A 3D pseudopotential well of a single lattice site. (e) Pseudopotential plots in three axes. The pseudopotential plot in the z-axis indicates the ion height at 117 μm, the escape point at 250 μm from the surface.

4.5.3 Simulations of shuttling scheme

One of the key requirements for quantum information processing is to have a well-controlled 2D transport (a process called "*shuttling*") of ions among an ion-trap array or to different trapping zones in a junction trap. To achieve this, the uses of array trap architectures [78], [102] and large scale ion traps [75] have been proposed. In linear ion traps, shuttling can be done by using the segmented DC electrodes on the trap array so that the pseudopotential well holding one ion or more ions moves in a controlled way. Shuttling can also be used for a new way of realizing gate operations [149] by moving ions in and out of the laser beam instead of addressing the beam onto the ion.

In a 2D hexagonal lattice trap, a rudimentary shuttling between neighbouring lattices can be achieved by lowering the RF voltage to minimise the RF potential barrier between adjacent lattice sites as much as possible without loss of particle due to the much lower trap depth. Otherwise particles will have enough energy to escape the reduced pseudopotential well. Now the charged particle can be transported to the adjacent lattice by applying a control (DC) voltage to the compensation electrodes surrounding the RF electrode. To control the shuttle direction, DC voltages with the same polarity as the charged particle are applied, resulting in a repulsive force in the same direction as the applied electric field. For example, a charged particle is initially trapped with an applied AC voltage of 300 V at frequency $\Omega_{RF}/2\pi = 700$ Hz corresponding to the trap depth of 0.10 eV and the stability parameter $q = 0.30$. The pseudopotential barrier between adjacent trap sites in Figure 4.12 is reduced from 0.28 eV to 0.10 eV (which is roughly equal to the initial trap depth) by decreasing the AC voltage from 300 V to 180 V. The equipotential lines (contour) of the 2D pseudopotential plot in the xy-plane are separated by 0.1 eV (0 to 1.0 eV from the inner ring to the outer ring) as shown in Figure 4.13. The inner ring at 0.1 eV represents the depth of pseudopotential well. Once the RF voltage is reduced, the 0.1 eV-equipotential line of each trapping site starts expanding until it merges with those of neighbouring traps at the RF voltage between 180 V and 200 V. However, the pseudopotential well of the outermost lattice traps remain separate due to the inhomogeneity of the electric field curvature of individual lattices. Therefore, the RF voltage needs to be lowered to about 160-170 V for shuttling a particle at the peripheral lattices.

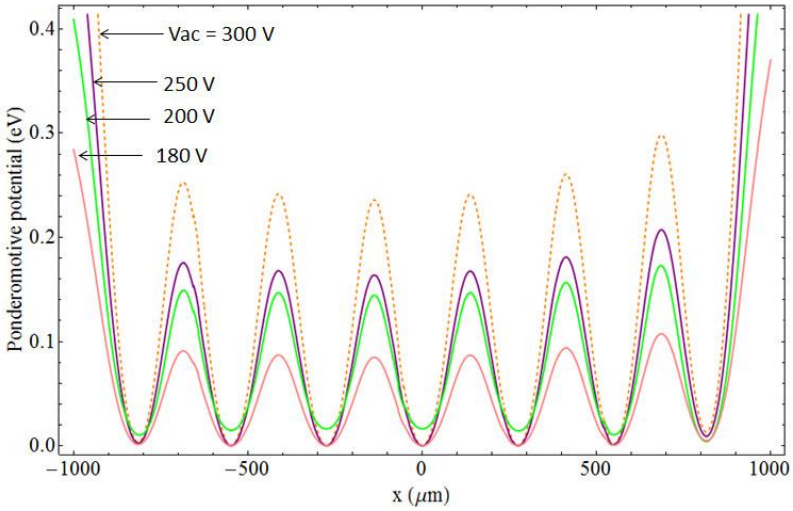


Figure 4.12 – A pseudopotential plot in the x-axis simulated from the centre trap array containing seven lattices. The pseudopotential well barrier is reduced from its initial value of 0.26 eV (at V_{RF} = 300 V) to 0.10 eV after reducing V_{RF} to 180 V.

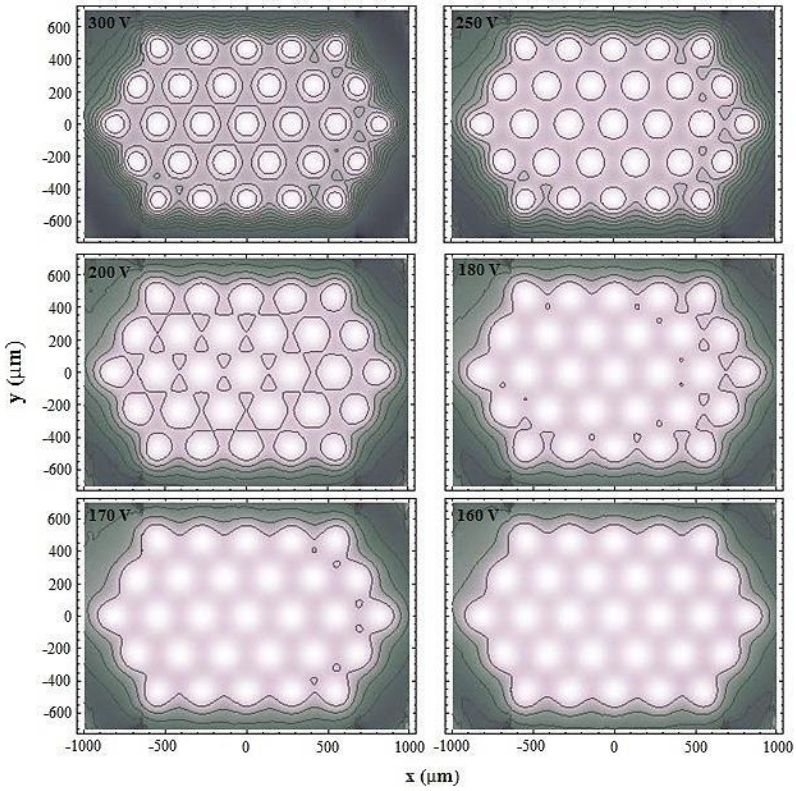


Figure 4.13 – 2D contour plots of the pseudopotential in the xy-plane at z = 117 μm with a varying RF voltage for shuttling operation. The contour lines are from 0 V to 1 eV with 0.10 eV step. The optimum RF voltage resulting in the 0.1 eV-equipotential line of each lattice to be completely merged is 180 V (except for the outermost lattice traps which require further reduction to 160 V).

4.5.4 Simulations of levitation scheme

In the context of this thesis, levitation stands for the displacement of particle height by shifting the RF nil point perpendicularly to the electrode surface plane. Followed the *in situ* levitating technique demonstrated by Kim et al. [112] in a planar ring electrode trap, particle height can be adjusted by altering the amplitude and phase of the AC voltages applied to the inner and outer ring electrodes. To shift the RF nil point without introducing excess micromotion, it is important to have a phase difference between two RF voltages either in-phase ($\theta = 0°$) or the out-of-phase ($\theta = 180°$) for moving the RF nil point toward or away from the electrode surface, respectively. Other phase shift will result in unwanted micromotion. A new particle height can be adjusted upon the magnitude of the ε ratio which is the ratio of the secondary AC voltage (V_{AC2}) applied to the inner ring electrode to the primary AC voltage (V_{AC1}) applied to the outer ring electrode (typically the RF electrode).

The following simulations illustrate the pseudopotential of a particle at various heights which is achieved by applying the additional secondary AC voltage to the recessed electrode of a 2D hexagonal trap. The initial simulation of the recessed electrode connecting to the ground ($\varepsilon = 0$) suggests that a particle is trapped at 117 μm with the escape point at 247 μm above the surface. For a fixed primary AC voltage $V_{AC1} = 300$ V, the variation of the secondary AC voltages V_{AC2} (a varying ε ratio) results in the new particle heights and escaping points numerically simulated and shown in Figure 4.14. It is clearly seen that the in-phase mode ($\varepsilon > 0$) lowers the particle height while the out-of-phase mode ($\varepsilon < 0$) increases the height. The variation of particle height is in the range of 50-150 μm from various ε values within ± 0.75, as illustrated in Figure 4.15. However, more care is needed with the effect of RF nil shift associated with the altered trap depth and stability parameter q at the same time. In Figure 4.16, the simulation shows that the out-of-phase regime (increased particle height) is limited by the lowered trap depth and a decline of the pseudopotential barrier from the trapping position towards the escape point. The in-phase regime is limited by the rapid decline in the stability q parameter and the trap depth at $\varepsilon = +0.40$. In particular, the range of $\varepsilon > +0.30$ where the particle height is lowered towards the electrode surface shows that the pseudopotential well is no longer valid according to the parameter q at the boundary of

the first stability region, $q_{max} = 0.908$. It is noticed that the trap depth abruptly drops to zero and the particle height is also beyond the initial escape point. This incident can be used to determine the instability trajectory or the particle loss. To keep the pseudopotential valid and avoid the parameter q reaching the stability limit, the drive frequency can be increased by some sacrifice in the reduced trap depth. The variation of ε value between $-0.75 < \varepsilon < +0.40$ results in the shifting of particle height up to 33 μm in upward direction and 20 μm in downward direction from the initial particle height at 117 μm ($\varepsilon = 0$). Within this ε range, the levitation is still achievable without suffering from much of a decrease in the trap depth ($\geq$ 0.1 eV) and the trap stability parameter $q < 0.908$.

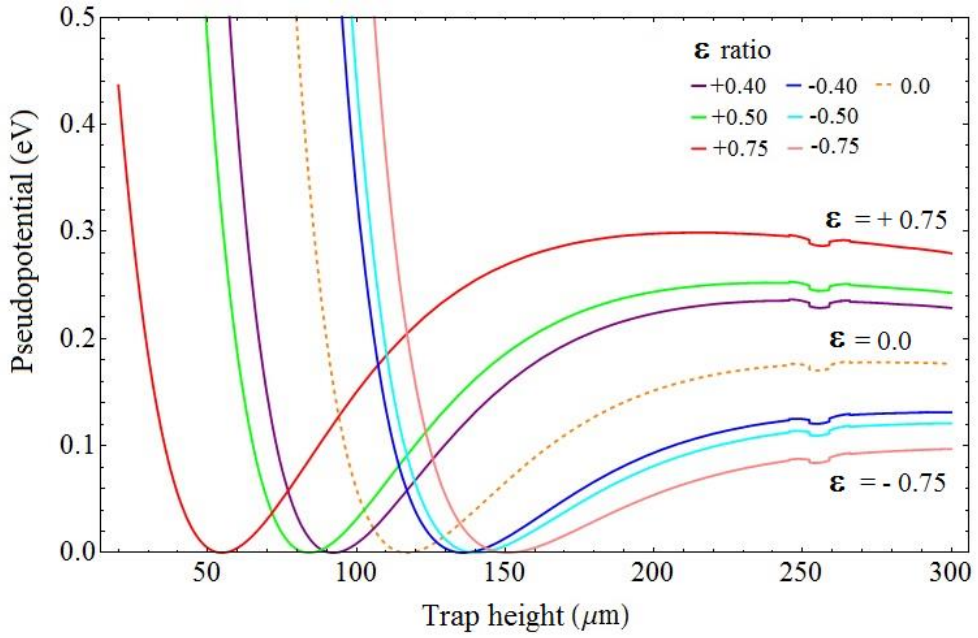


Figure 4.14 – Variation of pseudopotentials along the z-axis with the shifting of particle height (RF nil) corresponding to various ε values, the ratio of the secondary to primary AC voltages ($\varepsilon = V_{AC2}/V_{AC1}$). Under the initial operating condition, $V_{AC1} = 300$ V at frequency $\Omega/2\pi = 1190$ Hz, $V_{AC2} = 0$, the particle height is 117 μm where $\varepsilon = 0$ (dash line). With ε ratio range of ± 0.75, the particle height ranges between 55-150 μm.

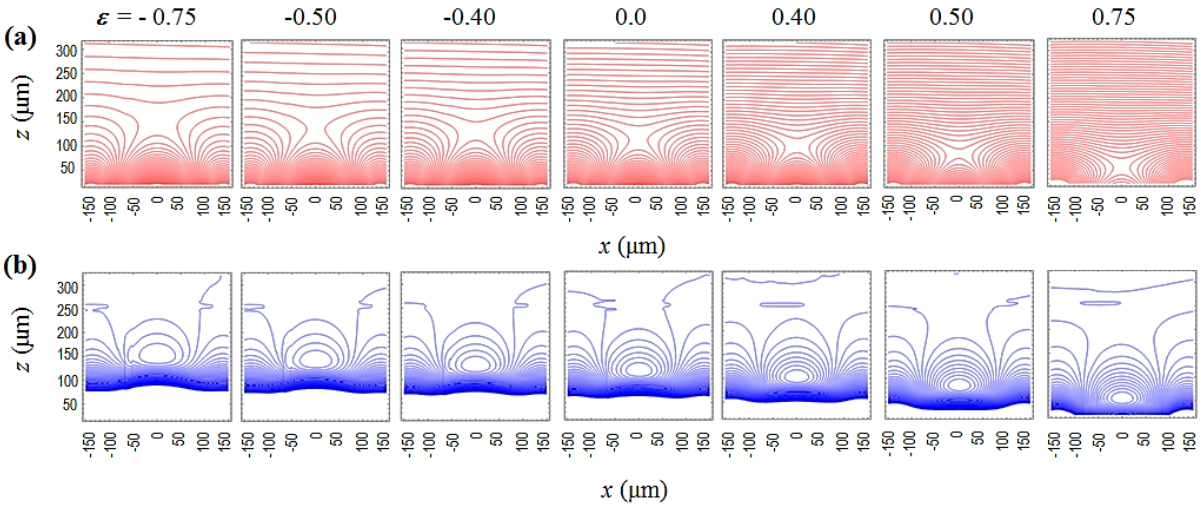


Figure 4.15 – Simulation of particle levitation in the 2D lattice trap. 2D contour plots of RF potential and pseudopotential in the xz-plane shows particle height ranging between 55 μm and 150 μm within $\varepsilon = \pm 0.75$. (a) The RF potential contour shows the saddle point (RF nil) shifting towards the surface where $\varepsilon > 0$ (in-phase) and in a reverse direction where $\varepsilon < 0$ (out-of-phase). (b) 2D contour plots of the pseudopotential show the shift of the pseudopotential minimum.

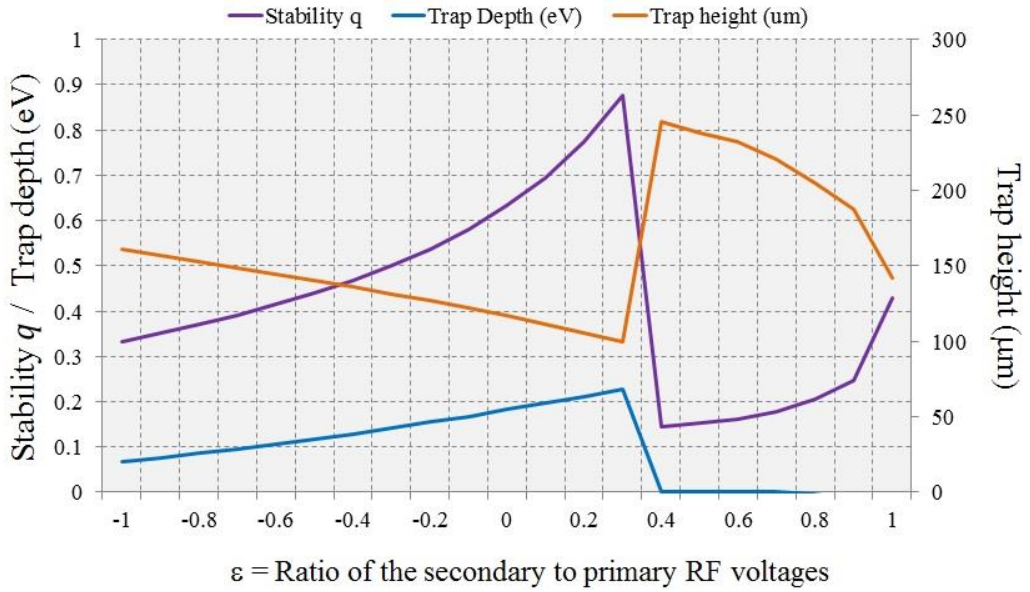


Figure 4.16 – The variation of particle height, trap depth and stability parameter q corresponding to the altered secondary AC voltage (V_{AC2}) at various ε values within ± 1.0. For the given RF voltage V_{AC1} = 500 V at $\Omega/2\pi$ = 1532 Hz, and a particle with a given Q/m ratio ≈ 8×10^{-4} C/kg, the cut-off region of the levitation is shown within the in-phase mode $\varepsilon \geq +0.4$ where the computed trap parameters become invalid.

4.6 Analysis of damping effect of the particle motion in air

Trapping of small particles under low pressure or atmospheric pressure, the motion of trapped particles in air can either be weak damping that does not significantly affect the trap stability or strong damping by any significant air flow that can eject particles out of the trap. By variation of air pressure, temperature and particle size, the degree of damping the particle motion in the trap can be different. From previous studies of damping force to the regions of stability in the QIT as discussed in Section 3.3.5, the maximum Mathieu parameter q ($q_{max} = 0.908$, $a = 0$) is altered due to the dimensionless friction coefficient b. The shift of the stability boundary makes the determination of the charge-to-mass ratio (Q/m) employing the "*boundary ejection*" method (or a mass-selective instability scan [83]) less precise. In this regard, damped microparticle motion subjected to a specific experimental condition is needed to evaluate whether it has a significant influence on the trap stability. First, the experimental condition is determined as to whether it obeys Stokes' Law. The Reynolds number (Re) is calculated using Equation (3.35), $Re = u_0 D_p/\nu = 2\rho u_0 R_p/\eta$. Next, the Knudsen number (Kn) is obtained using Equation (3.37), $Kn = 2\lambda/D_p$ where the mean free path for gas molecules in dry air $\lambda = 67.3$ nm [139]. Next, the empirical drag coefficient C_D and the slip correction factor C_C required for any test condition that does not follow Stokes' Law are computed using Equations (3.39) and (3.41) respectively. The sets of parameters (α, β, γ) reported in Allen and Raabe [139], Hutchins et al. [140] and Kim et al. [150] are the most suitable for the derivation of solid spherical particles that range from 1.00 μm in diameter or larger. The computed C_C values from these three sets of parameters (α, β, γ) are well correlated. Thus the set of parameters ($\alpha = 1.165, \beta = 0.483$ and $\gamma = 0.997$) from Kim et al. [150] is used in the following analysis.

The drag effect term ($b\,\frac{du}{d\xi}$) in Mathieu's equation shown in Equation (3.42) accounts for the damping effect associated with the dimensionless drag coefficient b which can be calculated using Equation (3.45) and (3.46). It can be seen that the dimensionless drag coefficient b depends particle size and mass, fluid viscosity and density, drive frequency and the addition of an empirical drag coefficient and a slip correction factor for any case falling beyond Stokes' range. Table 4.2 shows the study of the dimensionless drag coefficient b as a function of drive

frequency ($\Omega_T/2\pi$) ranging between a low frequency 50/60 Hz (for particle trapping) up to 10 MHz (a typical frequency range for ion trapping) for two different types of particles with various particle sizes from 50 nm to 300 μm in diameter. Anthracene dust particles (a density of 1280 kg/m^3) presented in the previous study of Winter and Ortjohnn [142] is selected in comparison with the soda lime glass microspheres (a density of 2400-2600 kg/m^3) which is the choice of particles used in the experiments described in Chapter 8. This numerical result suggests that Stokes' Law is only valid for the particle dimension between 10 μm and 20 μm in diameter. For the rest of the particle sizes, Stokes' Law is not applicable which requires the additional term of the empirical drag coefficient C_D for large Reynolds number (Re) or Slip correction factor C_C for large Knudsen number (Kn). Since the dimensionless drag coefficient b of the particles is inversely proportional to mass m and drive frequency $\Omega_T/2\pi$, increasing of mass and frequency results in $b \to 0$ where there is no damping effect similar to the undamped systems (i.e. in vacuum). A weak damping is found in large particles like 300 μm but is more pronounced when the particle size is reduced to sub-micron scale across the driving frequency range. This implies that trapping nanoparticles in air at atmospheric pressure has a large impact from the damping effect.

In particular, the dimensionless drag coefficient b of the microparticles with a diameter of 30 μm trapped in the 2D lattice trap operating at a drive frequency range of 500-1000 Hz is found to be as small as $b \approx 0.05$-0.09. Trapping of the selected microparticles in air within this frequency range or higher will result in the drag (damping) term $b < 1$, which is considered to exhibit only a small effect of air damping on the stability boundary. Additionally, the theoretical data analysis by Winter and Ortjohnn [142] (see Figure 3.7) also shows no significant shifting of the stability parameter q at $b \approx 0.1$. Therefore the stability boundary $q_{max} = 0.908$ is also valid for the determination of charge-to-mass ratio (Q/m) described in Chapter 8 (see Section 8.3.7).

Table 4.2 – Calculation of the dimensionless drag coefficient b derived from Equation (3.45) with and without the empirical drag coefficient C_D of Re, the slip correction factor C_C of Kn and variation of drive frequencies. (a) Anthracene dust particles used in previous work [142]. (b) Soda lime glass microspheres used in the present experiments.

(a)

Density of Particle = 1.28 g/cm^3						Dimensionless drag coefficient b					Dimensionless drag coefficient b with C_D of Re and C_C of Kn				
D_p(µm)	Re	Kn	C_{D1}	C_{D2}	C_C	50Hz	500Hz	1KHz	1MHz	10MHz	50Hz	500Hz	1KHz	1MHz	10MHz
300	69.86	0.00	1370.20	3.77	1.00	0.02	0.00	0.00	0.00	0.00	0.07	0.01	0.00	0.00	0.00
100	2.59	0.00	2.10	1.29	1.00	0.16	0.02	0.01	0.00	0.00	0.21	0.02	0.01	0.00	0.00
60	0.56	0.00	1.11	1.10	1.00	0.45	0.04	0.02	0.00	0.00	0.50	0.05	0.02	0.00	0.00
30	0.07	0.00	1.01	1.02	1.01	1.79	0.18	0.09	0.00	0.00	1.79	0.18	0.09	0.00	0.00
20	0.02	0.01	1.00	1.01	1.01	4.03	0.40	0.20	0.00	0.00	4.03	0.40	0.20	0.00	0.00
10	0.00	0.01	1.00	1.00	1.02	16.11	1.61	0.81	0.00	0.00	16.11	1.61	0.81	0.00	0.00
1	0.00	0.13	1.00	1.00	1.16	1611.44	161.14	80.57	0.08	0.01	1392.96	139.30	69.65	0.07	0.01
0.5	0.00	0.27	1.00	1.00	1.32	6445.78	644.58	322.29	0.32	0.03	4894.96	489.50	244.75	0.24	0.02
0.2	0.00	0.67	1.00	1.00	1.86	40286.10	4028.60	2014.30	2.01	0.20	21683.21	2168.32	1084.16	1.08	0.11
0.1	0.00	1.35	1.00	1.00	2.88	161144.00	16114.44	8057.22	8.06	0.81	55990.69	5599.08	2799.54	2.80	0.28
0.05	0.00	2.69	1.00	1.00	5.03	644578.00	64457.80	32228.90	32.23	3.22	128045.40	12804.54	6402.27	6.40	0.64

(b)

Density of Particle = 2.60 g/cm^3						Dimensionless drag coefficient b					Dimensionless drag coefficient b with C_D of Re and C_C of Kn				
D_p(µm)	Re	Kn	C_{D1}	C_{D2}	C_C	50Hz	500Hz	1KHz	1MHz	10MHz	50Hz	500Hz	1KHz	1MHz	10MHz
300	141.97	0.00	6432.22	5.52	1.00	0.01	0.00	0.00	0.00	0.00	0.05	0.00	0.00	0.00	0.00
100	5.26	0.00	5.65	1.47	1.00	0.08	0.01	0.00	0.00	0.00	0.12	0.01	0.01	0.00	0.00
60	1.14	0.00	1.22	1.15	1.00	0.22	0.02	0.01	0.00	0.00	0.30	0.03	0.01	0.00	0.00
30	0.14	0.00	1.03	1.04	1.01	0.88	0.09	0.04	0.00	0.00	0.90	0.09	0.05	0.00	0.00
20	0.04	0.01	1.01	1.02	1.01	1.98	0.20	0.10	0.00	0.00	1.98	0.20	0.10	0.00	0.00
10	0.01	0.01	1.00	1.00	1.02	7.93	0.79	0.40	0.00	0.00	7.93	0.79	0.40	0.00	0.00
1	0.00	0.13	1.00	1.00	1.16	793.33	79.33	39.67	0.04	0.00	685.76	68.58	34.29	0.03	0.00
0.5	0.00	0.27	1.00	1.00	1.32	3173.30	317.33	158.67	0.16	0.02	2409.82	240.98	120.49	0.12	0.01
0.2	0.00	0.67	1.00	1.00	1.86	19833.20	1983.32	991.66	0.99	0.10	10674.83	1067.48	533.74	0.53	0.05
0.1	0.00	1.35	1.00	1.00	2.88	79332.60	7933.26	3966.63	3.97	0.40	27564.71	2756.47	1378.24	1.38	0.14
0.05	0.00	2.69	1.00	1.00	5.03	317330.00	31733.00	15866.50	15.87	1.59	63037.60	6303.76	3151.88	3.15	0.32

$Re << 1$ and $Kn << 1$ (Stokes'law) | $0.1 < Re < 2$, applies C_{D1} | $2 < Re < 500$, applies C_{D2} | $0.1 < Kn$, applies C_C

4.7 Conclusion

The analytical models and numerical simulations of two different types of surface-electrode ion trap (SEIT) designs, (i) a five-wire design with Y-shaped junction (a Y-junction trap) and (ii) a two-dimensional (2D) hexagonal lattice trap (a hexagonal trap) have been utilised in gaining insight into electrodynamic trapping mechanism for both atomic ions and charged microparticles. Two other mechanisms worth mentioning are a rudimentary shuttling of the particles in the 2D lattices and dynamics of levitating particles in the air damping which have also been investigated. The analytical model for electrostatic fields in SEITs (i.e. a four-wire and a five-wire design) based on the gapless plane approximation proposed by House [143] was initially used to evaluate the Y-junction trap. It is found to be convenient to compute the relevant trap parameters such as pseudopotential well, trap depth, trap height and stability parameter q analytically. However, this analytical model is limited only to SEITs with a rectangular shape. Therefore, the numerical simulation method is needed for investigating more complex structures such as a junction region or 2D lattice traps.

Trapping with $^{171}Yb^{+}$ ions and charged microparticles (with the charge-to-mass (Q/m) ratio in range of 10^{-4}-10^{-3} C/kg) in the proposed traps are evaluated numerically using "*bemsolver*" simulation tool (the boundary element method) to simulate the electric potential of individual electrodes in the physical trap geometries. With "*the electrode basis functions*" obtained from the bemsolver, the pseudopotential, secular frequencies and trap depth corresponding to the trapping height and escaping point are numerically analysed by solving its first-order and second-order derivative equations using the mathematical analysis program called "*Mathematica*". Based on these, trap heights of 75 μm (showing a good correlation to the analytical result of the gapless-plane approximation) and 117 μm above the surface are estimated for a Y-junction trap and a 2D lattice trap, respectively. The summary of trap characteristics obtained from this numerical study is provided in Appendix A (Table A.1). By comparing ion- and microparticle-trapping conditions for identical traps using numerical simulations, it is realised that the appropriate driving frequency ($\Omega_T/2\pi$) strongly depends on the charge Q and mass m of the particles. Under typical operating conditions with an applied AC voltage in a range of 200-600 V, this suggests a driving frequency ($\Omega_T/2\pi$) of 30 MHz to

100 MHz for ion trapping and 500 Hz to 3.5 kHz for microparticle trapping, corresponding to the stability parameter $q \leq 0.60$. The numerical simulations provide decent estimations of trap characteristics and is found to be very useful in finding stable operating points in combination of AC/DC voltages, drive frequencies and stability parameters prior to the experimental measurements.

The determination of air damping to the stability boundaries of the Mathieu's equation when suspending microparticles in a quadrupole ion trap is presented. The drag coefficient b of the realistically experimental conditions employed in the experimental studies discussed in Chapter 8 was found to be small as $b = 0.05$-0.10 which exhibits only small drag effect (weak damping) and has no significant effect on the shift of the stability boundary of the first stability region. Therefore, the ideal stability boundary $q_{max} = 0.908$ with $a = 0$ is still eligible for the numerical calculations of microparticle trapping parameters (in air) and the charge-to-mass ratio (Q/m) approximation presented in the experimental works.

Chapter 5

Fabrication of surface-electrode ion traps

In this chapter, the development of fabrication for surface-electrode ion traps (SEITs) including a Y-junction trap and a 2D hexagonal lattice trap is presented. First an introduction to Silicon-On-Insulator (SOI) technology is given. In particular applications, the development of SEITs based on SOI fabrication technology for trapped ion quantum systems and its beneficial characteristics are highlighted. Following that, the determination of SOI substrate specification based on both the electrical and structural properties of the proposed traps are described. The fabrication of the microtraps with three different process flows was developed and demonstrated. The specific advantages and drawbacks of each process flow as related to the trap geometries and dimensions are discussed. A detailed and in-depth description of fabrication processes including a standard photolithography, deep reactive-ion etching (DRIE), hydrofluoric acid (HF) etching, inductively coupled plasma (ICP) etching and metallisation is also presented. This chapter concludes with a discussion on the fabrication challenges, outcomes and recommendations for further improvement in future fabrication.

5.1 Silicon-On-Insulator (SOI) technology

A Silicon-On-Insulator (SOI) is a semiconductor wafer technology that was initially developed for improving performance, power consumption and reliability of integrated circuits

(ICs) that could not be achieved with traditional bulk silicon techniques. Since faster speed and less switching power are an intrinsic advantage of SOI transistors due to their lower capacitance, SOI technology has already been proven in the IC marketplace and has been widely used as a promising new material in the fabrication of micro- and nano-electromechanical systems (MEMS/NEMS), photonics and biotechnological (lab-on-a-chip) devices [151].

The SOI structure consists of a layer of single crystalline silicon separated from the bulk substrate by a thin layer of insulator. Depending on the type of application, the silicon film can be very thin at a sub-micron scale (< 50 nm for fully depleted transistors), or it can be from a few microns to several hundred microns (for MEMS applications) [152]. Similarly, the buried oxide (BOX) thickness ranges from tens of nanometres to several micrometres; this depends largely on their intended application, operating voltage, frequency, and device scale requirements, among other factors. Choices of insulator - typically silicon dioxide (SiO_2) or other materials such as sapphire (Silicon-On-Sapphire, SOS) and quartz (Silicon-On-Quartz, SOQ), have been found to offer further advantages in microwave circuits, optical mobile and micro-display (liquid-crystal display) applications.

SOI substrates are fabricated using various technologies based on two basic approaches. First, the SIMOX (Separation by Implementation of Oxygen) process employs high-dose oxygen ion implantation and high-temperature annealing to form the buried oxide (BOX) layer into a bulk silicon wafer. The formation of the BOX layer resulting from oxygen implantation strongly depends on the dose and the implant ion energy. In oxygen implantation, an oxygen dose of ~ 0.3 - 2.0×10^{18} cm^{-2} and energy of $\sim$ 120-200 keV, yields a typical Si film thickness varying from $\sim$ 10-200 nm and BOX layer thickness of 100 - 400 nm. The use of the SIMOX wafer is very limited because of the maximum buried oxide thickness of around 400 nm, which is obviously thin for other applications (refer Table 5.1).

Alternatively, SOI wafers can be formed by bonding a device silicon wafer (active regions) to another silicon wafer normally called a handle wafer. The buried oxide is normally grown on one wafer and then two wafers are bonded together using silicon direct bonding, also referred to as silicon fusion bonding. The bonded wafer pair is then split apart. At this step,

there are various techniques employing thinning or splitting of the structure that eventually form the SOI film (a device Si layer) at its target thickness. Thick-film SOI wafers (typically device layer thickness > 1 μm) can be produced by the Bonded and Etch-Back Silicon-On-Insulator (BESOI) method or, in the higher thickness range, by the precision back-grinding and polishing method which is often adequate. In the BESOI process, two wafers are bonded with an oxide layer in between them. One of the wafers is thinned by grinding, polishing and etching. A well-defined and highly-uniform thickness control of a thin SOI film can be obtained by introducing the etch stop layers. BESOI wafers are typically made of growing epitaxial layers on a device wafer, oxidising the epi layer, and then thermally bonding a second oxidised wafer (the handle wafer) onto the oxidised epi layer. After bonding is accomplished, the device wafer is thinned by grinding and polishing; a selective etch which is impurity-sensitive is used to remove the etch-stop layer and, finally, only the epi layer is left to form the SOI film [153].

For very-thin SOI films, defining thin thickness by the implantation process leads to a much better thickness uniformity control than those of chemical-mechanical thinning processes. To achieve precise control over silicon thickness and crystal quality, a new way of making SOI wafers emerged from the 1990s. The layer transfer technique has led to the recent development of at least three production methods for fabrication of SOI wafers: SmartCut™ (by CEA-LETI), NanoCleave™ (by Silicon Genesis Corporation), and ELTRAN™ (by Canon). The SmartCut and NanoCleave processes both employ high-dose ion implantation (using hydrogen and helium). The difference between these processes lies in the splitting mechanism. In Smart Cut™, the splitting is subjected to hydrogen implantation and thermal treatment inducing the growth of microcavities which lead to the formation of micro-cracks or microsplitting [154]. An atomic-layer cleaving process, also called "*Nanocleave*", is based on forming a cleave plane on an active wafer. The cleaving is done at room temperature using the force of a nitrogen jet at the implant depth in NanoCleave process [155], [156] or a high-pressure water jet at the porous Si layer in ELTRAN process [157].

Table 5.1 – SOI wafer applications. (Table from ref. [158].)

Application	Device layer thickness	Buried oxide thickness	SOI technology
CMOS	10-100 nm	200-400 nm	Smart-cut, SIMOX
Bipolar	1-10 μm	0.1–1.0 μm	Various
MEMS	50-500 μm	0.5–4 μm	Bonded SOI
Power IC	1-100 μm	1-4 μm	Bonded SOI

5.2 Surface-electrode ion traps with SOI substrates

The most common microfabrication processes and techniques (e.g. standard printed circuit board (PCB) technology, MEMS fabrication and semiconductor fabrication) used in the development of surface-electrode ion traps (SEITs) for large-scale quantum systems with trapped ions were reviewed in the literature review (Chapter 2). Each fabrication technique has some inherent advantages and disadvantages with respect to the trap structure and performance. Structural electrode geometry being amenable to microfabrication as a monolithic structure eliminating the need for manual assembly and alignment is necessary for truly large-scale ion-trap quantum devices. The selection of fabrication is also based on both the electrical and structural characteristics (e.g. desired electrode feature size, geometry and surface integrity, voltage-breakdown, capacitance, resistance, and power dissipation). Besides all technical requirements mentioned above, in practice, the availability of facilities and equipment tools in cleanrooms and laboratories dictates practical solutions in terms of process difficulty, cost effectiveness and turnaround time.

The use of SOI technology for ion-trap devices was first demonstrated in Britton et al. [87]. In Britton's thesis, the use of the SOI process consumed less process time by a factor of 2/3 than that consumed by in-house anodic bonding of silicon to glass technique. Furthermore, recent works utilised a combination of SOI and multi-metal layers to build a more complex SEIT with multi-zone traps in Stick et al. [71], a 2D trap array that incorporates a Y-junction in Moehring et al. [86], and an X-junction in Wright et al. [49]. Considering all factors

mentioned above, the most suitable microfabrication for the proposed microtraps (a Y-junction trap and a 2D lattice trap) is a SOI-based MEMS fabrication technique due to three main reasons. First, the SOI structure is a monolithic heterostructure (Si-oxide-Si) which requires no manual assembly. Second, the construction of trap electrode geometry is straightforward, using etch processes to form electrically isolated electrodes. The electrodes are formed on the front-side SOI substrate called Si device layer. In addition, the back-side Si layer, a handle layer, can be optionally patterned and etched through. This allows for the through-hole structures where optical access and integration is required. The oxide layer extending across the entire wafer is used as an etch-stop. It also provides isolation of the trap electrodes at the front Si layer from the back Si layer acting as a ground plane. The selective undercut of the buried oxide can be beneficial for more complete shielded dielectrics avoiding unwanted charge build-up on the exposed dielectrics close to the trap region and the affecting of trap performance. Third, a SOI substrate in its commercialised form is available from various wafer suppliers. SOI substrates can be obtained from inventory stock (standard SOI specifications) and be customised in varieties of SOI film thicknesses corresponding doping levels and oxide thickness to fit to customers' needs. SOI technology provides certain added benefits such as very tight tolerances in the film thickness and uniformity.

For ion-trap devices, the successful substrate has to exhibit the common characteristics needed for the ion trapping scheme such as ultra-high vacuum (UHV) compatibility, dielectric breakdown to withstand high voltage, dielectric loss (in particular, the operation in the radio-frequency range requires low RF loss tangent). To construct the proposed traps using a SOI substrate as a starting material, the basic electrical characteristics and requirements in determining SOI substrate specification are described below.

i) The thickness of the buried oxide layer should be maximised to increase bulk breakdown voltage as an applied RF voltage of more than 200 V is normally used in ion-trapping operations.

ii) It is very important to achieve an effective coupling between the ion-trap chip and the RF source via a helical resonator (RF generator). Impedance matching between a RF voltage source and load (an ion trap) is required to ensure that

the maximum power is delivered to the trap, and that any reflections are avoided, which can damage the equipment. The ability of a helical resonator represented by the quality factor or Q-factor where $Q = 1/2\pi f_0 RC$ (a resonant frequency f_0, the resistance R and capacitance C of the ion trap). Since a large Q-factor is preferred for the resonator, it is important to minimise the resistance and capacitance of the trap. A heavily doped silicon substrate producing highly conductive, very low resistivity characteristics and a thick dielectric layer can be exploited for decreasing the electrode resistance and the capacitance between the RF electrodes and the recessed ground electrode (Si-handle layer).

In buying the SOI wafers, several structure parameters can be customised such as the thickness of the oxide and top/bottom Si layers, the dopant type, resistivity and orientation of Si, and the wafer diameter to match with customer requirements from a large number of suppliers. The 150 mm (6-inch) SOI substrates used in this present work were purchased from Ultrasil Corporation with two different specifications as listed in Table 5.2. For Ultrasil SOI wafer manufacturing process, the buried oxide is normally grown on one wafer and then two wafers are bonded together. The bonded wafer is then nanoground, and the Si device and handle layers are polished down to the desired target thickness. In wafer lot number 5445 obtained from the Ultrasil's on-line inventory, the 5 μm of wet thermal oxide was grown on the device wafer. Then the device and handle wafers were bonded together using a fusion bonding at room temperature followed by a high-temperature annealing of the bonded wafer pair at 980 °C. For a thicker buried oxide layer of 10 μm in wafer lot number 5440 obtained from a custom-built order, the buried oxide can be formed by oxide film-oxide film (SiO_2+SiO_2) bonding but this strength is expected to be lower than that of silicon-oxide film(Si+SiO_2) bonding. As a result, the 5 μm of wet thermal oxide was grown on both the device and the handle wafer. The wafer bonding and polishing steps are similar to those of the standard process.

Table 5.2 – Ultrasil® SOI substrate specifications

Specification	Batch#1 (custom-built)	Batch#2 (standard)
Wafer Lot ID#	5440	5445
Diameter (mm)	150 ± 0.2 mm	150 ± 0.2 mm
Si Device layer		
Type/Dopant	N/Arsenic	N/Arsenic
Crystal orientation	<100> ± 0.5 degree	<100> ± 0.5 degree
Resistivity	0.001 - 0.005 Ω.cm	< 0.005 Ω.cm
Thickness	30 ± 0.5 μm	25 ± 1.0 μm
Si Handle layer		
Type/Dopant	N/Arsenic	N/Phosphorus
Crystal orientation	<100> ± 0.5 degree	<100> ± 0.5 degree
Resistivity	0.001 - 0.005 Ω.cm	1-20 Ω.cm
Thickness	600 ± 10 μm	485 ± 10
Buried oxide (BOX)		
Thickness	10 ± 5% μm	5 ± 5% μm
Process	WET thermal oxidation	WET thermal oxidation
Overall thickness	640 ± 10 μm	515 ± 10 μm
Polish	Double-side	Double-side
Price per slice	$332.50	$250

5.3 Fabrication process flows

This section describes the developed fabrication process for the proposed SEIT prototypes. The devices were fabricated on the Silicon-On-Insulator (SOI) substrates. The SOI-based fabrication process flows developed was on the basis of ease of fabrication that only one photolithographic mask was needed. In addition, the number of processing steps was also minimised. The processes involved only five main fabrication processes including wafer cleaning, metallization, photolithography, and both wet and dry etching.

The first process flow (Flow A) was initially developed and aimed to pattern arbitrary-shaped structures, e.g. Y-junction, hexagonal lattices using wet etching process which was considered to be a straightforward implementation. As shown in Figure 5.1, this process flow

started with a substrate clean prior to the metal deposition step. A bare SOI wafer was immersed in a bath of fuming nitric acid (FNA) solution for 10-15 minutes to remove any organic contaminants. This was followed by rinsing in deionised (DI) water and blow drying with a nitrogen gun. Next, the wafer was dipped in a buffered HF (or BOE), BHF 20:1 bath for 10 seconds to remove the native oxide on the Si surface. 50 nm-chromium (Cr) and 500 nm-gold (Au) layers were then deposited on the SOI substrate by the electron-beam (e-beam) evaporation (LEYBOLD Optics, BAK 600 model).

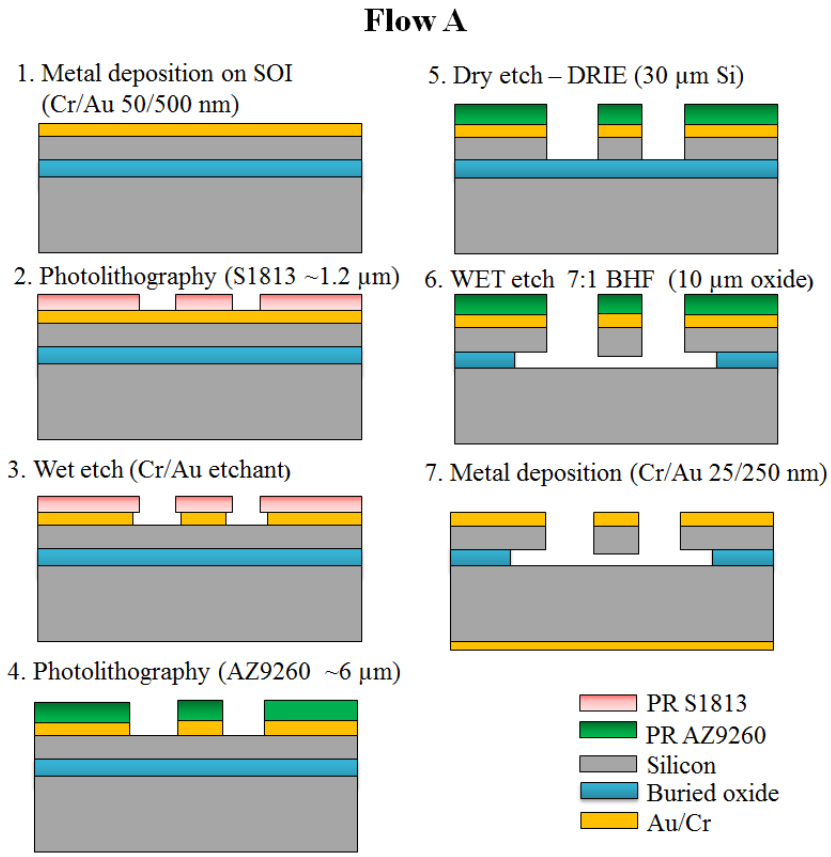


Figure 5.1 – The initial fabrication process flow (Flow A) of the proposed ion-trap chips fabricated on Silicon-On-Insulator (SOI) wafers.

The electrode geometry was patterned using photolithography by spin-coating the positive photoresist (Shipley S1813) on a clean wafer at a speed of 5000 rpm for

30 seconds, which formed a resist layer of 1.2-1.3 μm. To transfer the electrode patterns onto the underlying layers, the patterning of the photoresist by UV lithography was done using the mask aligner EVG 620T with an exposure duration of two seconds. The exposed photoresist was then developed using Microposit™ MF™ 319 metal-ion-free developer (Rohm and Hass Electronics materials LLC) for 20 seconds. Using such a thin resist yields a well-optimised photolithographic pattern transferred to the substrate compared to use of a thick resist. When wet etching was used, an isotropic etch with undercut was produced causing the formulated electrode dimensions to deviate from the mask design with ~ 7% offset at the junction area of critical dimension (CD) of about 5 μm. This is an inherent trade-off between the mask feature resolution and process simplicity obtained from wet chemical processes. To form the desired Au-Si-electrodes, the patterned photoresist was used as a mask for etching through the thin metal films of 500 nm Au and 50 nm Cr acting as an adhesion promoter, and the 30-μm top Si layer, respectively. The exposed Au layer was removed by a mixture of Au etchant (KI < 25% + I_2 1-10% + H_2O remaining, OM Group Ultra Pure Chemicals) and DI water in the ratio of 1:2 by volume. The Cr layer was then removed using a Cr etchant (Acetic acid 1-10% + Ceric ammonium nitrate 10-30% + H_2O remaining, OM Group Ultra Pure Chemicals).

With the wet chemical etching processes described above, the metallised electrodes were formed on top of a silicon device layer. To etch the top-Si layer, a deep reactive ion etching (DRIE) process developed on the STS Pegasus system was developed for anisotropic etch. From standard DRIE recipes, the selectivity of Si to resist mask has a ratio of approximately 20:1, which suggests that the resist thickness should be more than 2 μm to etch a 30 μm Si device layer. Thus, the remaining 1.2 μm photoresist S1813 was stripped off by immersing it in acetone followed by IPA. Then, a second photolithographic process was undertaken to produce a thick AZ9260 resist (target photoresist thickness ≈ 6 μm) on top of the completely etched Cr/Au structures using the same mask. However, the second photolithography was prone to the alignment issue since the overlay alignment error was observed. A 30 μm-thick Si device layer was etched down to the etch-stop (buried oxide) layer.

After the electrodes were transferred to the top Si (device) layer, the oxide layer was exposed and removed using a buffered hydrofluoric (BHF) acid etch. A 7:1 BHF solution was used instead of a 20:1 solution because the higher concentration yields a faster etch rate but a more pronounced undercut which is tolerable in this case. Unless a precise control of oxide removal is required, more dilute HF could be used. Finally, the photoresist mask was stripped off using the AZ 100 positive resist remover, and rinsed with DI water, followed by solvent cleaning using acetone/IPA and blow drying with the N_2 gun.

The optimised process flows were then developed for process improvements after encountering several process issues and limitations. The main problematic process observed was the buffered HF (BHF) etching process of a 10 μm-thick oxide layer. To completely etch through the 10 μm oxide layer with a 7:1 BHF solution, the optimal etch time was in a range of 140 ± 10 minutes (based on the etch rate of a 7:1 BHF solution ≈ 70-80 nm/min at room temperature). However, etching in a buffer HF solution for a long period of time continuously produces several process problems such as pinholes in the Au/Cr layer, completely undercutting (and lifting off) in very narrow geometries, stiction, and contamination. Furthermore, the occurrence of massive undercut area in the Au/Cr layers resulted in the pattern transfer error in the second photoresist patterning step. The resulting misalignment up to 3 μm has a significant impact on the smallest features (also called the critical dimension) of 5 μm at the Y-junction area. However this was an acceptable error for the larger structures in a 2D hexagonal lattice trap with the size of critical dimension ≈ 20 μm.

The optimized process flow named Flow B as shown in Figure 5.2 was developed to solve the issues found in Flow A. This process flow consists of four steps including photolithography, deep Si etching by DRIE, thick oxide etching by buffered HF, and metallization. The optimised process flow reduces the number of steps in Flow A by half and only requires a single photolithography step. However, thick oxide etching with a buffered HF solution was only suitable for a 2D hexagonal lattice trap but not for a Y-junction trap which has narrow and long electrode configurations. To alleviate this issue, another process flow named Flow C was developed to replace the buffered HF process with an anisotropic dry plasma etch using

an inductively coupled plasma (ICP). Additionally, the selective wet etch removing the exposed oxide in the gaps between electrodes (avoiding the charge accumulation on the dielectrics) was performed using a buffered HF with low concentration (e.g. 10:1 or 20:1) allowing for achieving a better control on the degree of undercut. Even though Flow C has one additional step compared to Flow B, it could be used to fabricate various microstructural geometries, particularly when several microtrap designs are simultaneously fabricated at a wafer level. The following sections provide the microfabrication processes, results and discussion in depth.

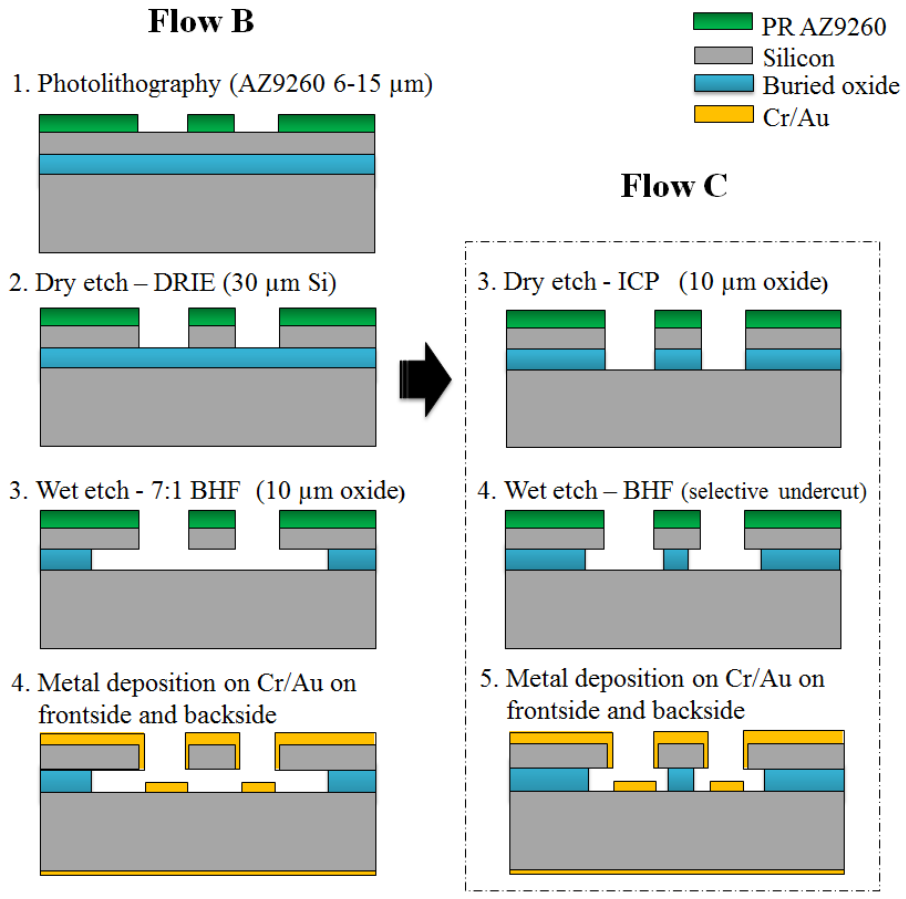


Figure 5.2 – The optimized fabrication process flows (Flow B and C). Flow B is restricted to the 2D hexagonal lattice trap (feature sizes $>$ 200 µm) due to the massive undercut in a buffered HF oxide etching. Flow C is more suitable for smaller electrodes of the Y-junction trap using an anisotropic ICP etching through a 10 µm-thick oxide layer, followed by a selective undercut process using a buffered HF. The metallisation step was performed at the end of the process.

5.4 Fabrication processes, results and discussions

This section describes in greater detail the individual processes involved in the developed fabrication process flows described in previous section. Several fabrication techniques used to make the metal-on-SOI microscopic traps include

(i) wafer cleaning procedure,

(ii) metallisation,

(iii) metal etching using a wet chemical process (i.e. chrome etchant, gold etchant),

(iv) photolithography using different photoresists to achieve the desired resist film thickness,

(v) silicon (Si) etching by deep reactive ion etching (DRIE),

(vi) oxide (SiO_2) etching by a buffered oxide etch (BOE), also known as buffered HF, and

(vii) oxide (SiO_2) etching by inductively coupled plasma (ICP) etching.

5.4.1 Wafer cleaning procedure

There are several common wafer cleaning processes developed within the SNC cleanroom. Standard RCA is one of the more effective processes and is commonly used in semiconductor processing. The processing step needs to be performed before any high-temperature processing steps (oxidation, diffusion, PECVD). RCA-1 cleanser (a hot mixture of ammonium hydroxide, hydrogen peroxide and deionised (DI) water in a ratio of 1:1:5) is commonly used to remove any organic residues from silicon wafer. In the process, it produces a thin layer of oxide on the Si substrate which is subsequently removed by quickly dipping the wafer in a hydrofluoric (HF) solution. RCA-2 cleanser (a hot mixture of hydrofluoric, hydrogen peroxide and DI water) is effective for removal of any ionic contaminations, particularly metals. A final HF dip is optional. For an extreme cleaning process, fuming nitric acid (HNO_3) gives a very good result. In this work, FNA cleaning was applied prior to any depositions to clean the substrate surface of any contaminants. The wafers were immersed in a clean fuming nitric acid (FNA) tank for five minutes for non-processed wafers and 10-15

minutes for the processed wafers. Photoresist (PR) can also be stripped off using a strip FNA followed by a clean FNA. Wafers were then rinsed in a quick dump rinser for at least three complete cycles. For any reused wafers, an extra cleaning step such as FNA+RCA1/2+HF was applied.

For the next step, the native oxide on Si surface grown over a long exposure time to atmosphere or due to the delay time between the substrate preparation and subsequent process was removed by a buffered hydrofluoric acid (BHF) solution. The growth rate of a native oxide depends both on the concentrations of oxygen and moisture and on wafer storage time. The surface oxidation usually forms rapidly up to 2-3 angstroms to reach saturation point within two hours in the ambient air at room temperature [159]. Also, the study of the initial surface oxidation stage immediately after HF cleaning process on silicon <100> surfaces [160] suggests that the forming of native oxide is likely to be stable at 2 angstroms within the first few hours and continuously increases to 8 angstroms within 16 hours. To strip the native oxide from the surface Si of SOI wafer, the wafers were quickly dipped in a 20:1 BHF tank (available for both non-metal and metal contamination) for about 10-15 seconds based on an etch rate of 125 angstroms per minute at room temperature. This was sufficient to remove the thin native oxide thickness. The wafers were first rinsed in a quick dump rinser for at least three complete cycles. The wafer was then hydrophobic (i.e. water should not adhere to the surface); if any droplets remain, this indicates that the oxide film was not completely removed and a repeat stripping process would be required. Finally the wafers were spun dry using the automated rinser/dryer (suitable for multiple wafers) or dried with the N_2 gun.

5.4.2 Metallisation

Several choices of conductive materials such as gold (Au), aluminium (Al), tungsten (W), platinum (Pt), silver (Ag) and copper (Au) have been utilised in the construction of the ion-trap electrodes. One typically selects an electrode material that has very low resistivity and does not oxidise. This makes gold being the most common choice. Since the gold film tends to exhibit poor adhesion to the Si substrate, chrome (Cr) or titanium (Ti) is commonly used as an adhesion promoter. In this work, chrome was used instead of titanium because

the latter can be affected by the HF acid etch in subsequent fabrication processes. The trap electrodes were made of a chrome-gold film (Cr - 50 nm and Au - 500 nm) using a Leybold BAK600 electron-beam evaporator. A 50-nm chrome film was first deposited on the Si substrate at a deposition rate of 0.06 nm/second (corresponding to a beam current of 21 mA at 5 kV) followed by a 500-nm gold film at a deposition rate of 0.23 nm/second (corresponding to a beam current of 113 mA at 5 kV). For the gold deposition, the system normally requires a higher vacuum condition of 5×10^{-6} mbar compared to other materials that only need a process pressure of 10^{-5} mbar. The thickness of a chrome-gold film obtained from the e-beam evaporation varied within 10% from the centre to the outer edges of the wafer. To achieve a 500 nm-thick gold film, the developed recipe was utilised two crucibles instead of a single crucible normally used in the standard gold deposition recipes (for gold thickness < 300 nm). The use of each crucible to evaporate a gold film thickness of ~ 250 nm is to avoid damaging crucible when the gold ingot became insufficient after a long deposition processing time. Alternatively, the aluminium deposition was used on the subsequent batches after the BAK600 evaporator broke down for several months due to crucible rotation was malfunction. Aluminium is a straightforward, cost-effective choice of evaporation metal materials and also beneficial for investigating the effect of surface material on trap performance.

5.4.3 Photolithography

In this work, different photoresists were used depending on the process requirements, such as desired resist film thickness, resolution, high selectivity for dry etching, and substrate adhesion. The photolithography recipes developed for each resist type and its target thickness are presented in detail in Appendix B-2, including a resist coating, soft baking, exposure and development of photoresist, respectively. Substrate preparation is very important before spin-coating the resist. The substrates were cleaned to remove contamination followed by a dehydration bake at a raised temperature of 210 °C for 30-60 minutes. The substrates were then cooled to room temperature and coated as soon as possible to reduce any reabsorption of water attributed to an uncontrolled humid environment. To avoid adhesion issues, a promoter can be added. Furthermore, the resist should be left at room temperature for at least one hour

to eliminate bubbles and adjust resist viscosity and stability before spin-coating. A brief description of two resist types used in this work is provided below.

S1813 is a positive resist and is widely used in processes involving both wet and dry etching. In this work, the aim is to attain good control of the arbitrary electrode geometries, as well as minimise undercut during wet chemical etching of thin metal layers (500/50 nm of Au/Cr). The substrate was loaded into a Brewer spinner and the resist was then dispensed at the centre of the wafer and spun at 5000 rpm to give a target thickness of 1.2 μm. This was followed by a soft bake for 90 seconds at 95 °C on a hot plate. The exposure of photoresist was carried out using an EVG 620T mask aligner. A pressure of one bar was applied to create the vacuum and hard contact during photolithography. Exposure duration of two seconds (without i-line (365 nm) filter, UV light intensity 18 mW/cm^2) was used. The exposed photoresist was then developed using Microposit™ MF-319 metal-ion-free developer (Rohm and Hass Electronics materials LLC) for 20 seconds and rinsed with DI water to completely remove the developer solution, and then blow dried with a nitrogen (N_2) gun.

AZ®9200 photoresist is suitable for higher resolution and thicker resist requirements. This photoresist series can produce film thicknesses from 2 to 24 μm. Since the adhesion on noble metals or a Si substrate is often quite poor, it is often recommended to use TI-Prime as an adhesion promoter to mitigate adhesion failures between the resist and underlying surface material. First, the aim was to achieve a thick resist mask for the subsequent DRIE process where the selectivity of Si to a resist mask was about 20:1. This implied that the resist thickness should be more than 2 μm for successful DRIE etching of a 30 μm-thick Si device layer in the Flow B. For processing through Flow C involving multiple dry etching steps, a thicker resist mask was needed. Therefore, the required thickness for the photoresist mask was at least 12 μm based on the computed selectivity values (20:1 for DRIE Si etch and 1:1 for ICP SiO_2 etch). To optimise the recipes for the photoresist layer with a target thickness up to 14 ± 2 μm, several trials were carried out with bare Si substrates. When the developed recipes were implemented with the processing SOI wafers, problems of photoresist burn were encountered during the DRIE process.

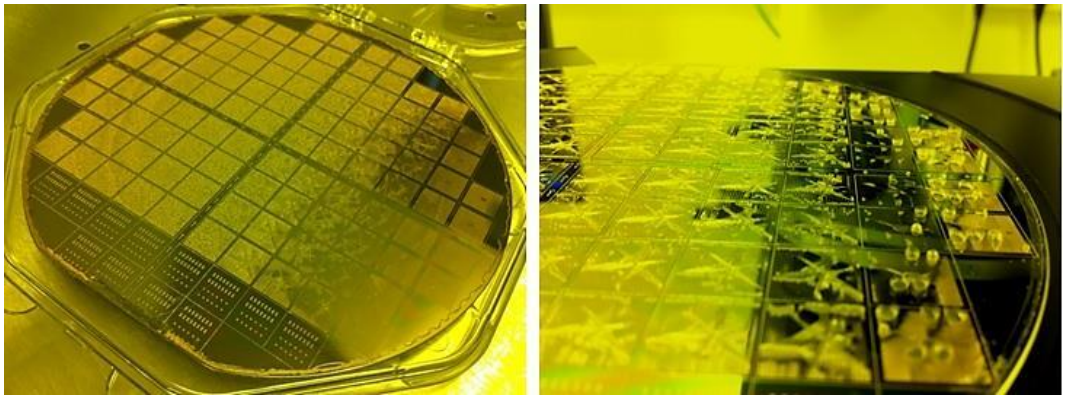


Figure 5.3 – Photographs of the burnt photoresist film after DRIE process on a six-inch SOI substrate patterned with a 15 μm-thick PR mask.

To investigate the issue of the burnt resist, three different wafers including a test Si wafer, a SOI with a 2 μm-thick oxide layer and a SOI with a 10 μm-thick oxide layer underwent the DRIE process at the same time. In fact, these wafers were handled from substrate preparation to photolithography at the same period of time and in the same working environment. First, a dummy Si wafer was loaded to the DRIE machine and processed with the DRIE Si etch processing recipe (SNC Recipe#2) followed by another two test wafers: i) SOI with 25 μm Si, 2 μm SiO_2 and ii) SOI with 30 μm Si, 10 μm SiO_2 (actual ion trap devices). The etch time was also varied between six and seven minutes for the desired 30 μm Si thickness based on the etch rate of 5 μm/min. The substrates were then inspected under an optical microscope. The Si layer of the dummy Si and SOI (with a 2 μm-thick buried oxide layer) substrates was etched away without any grassing issue or damage to the photoresist mask. However, for the SOI with a 10 μm-thick buried oxide, burnt photoresist was observed as seen in Figure 5.4.

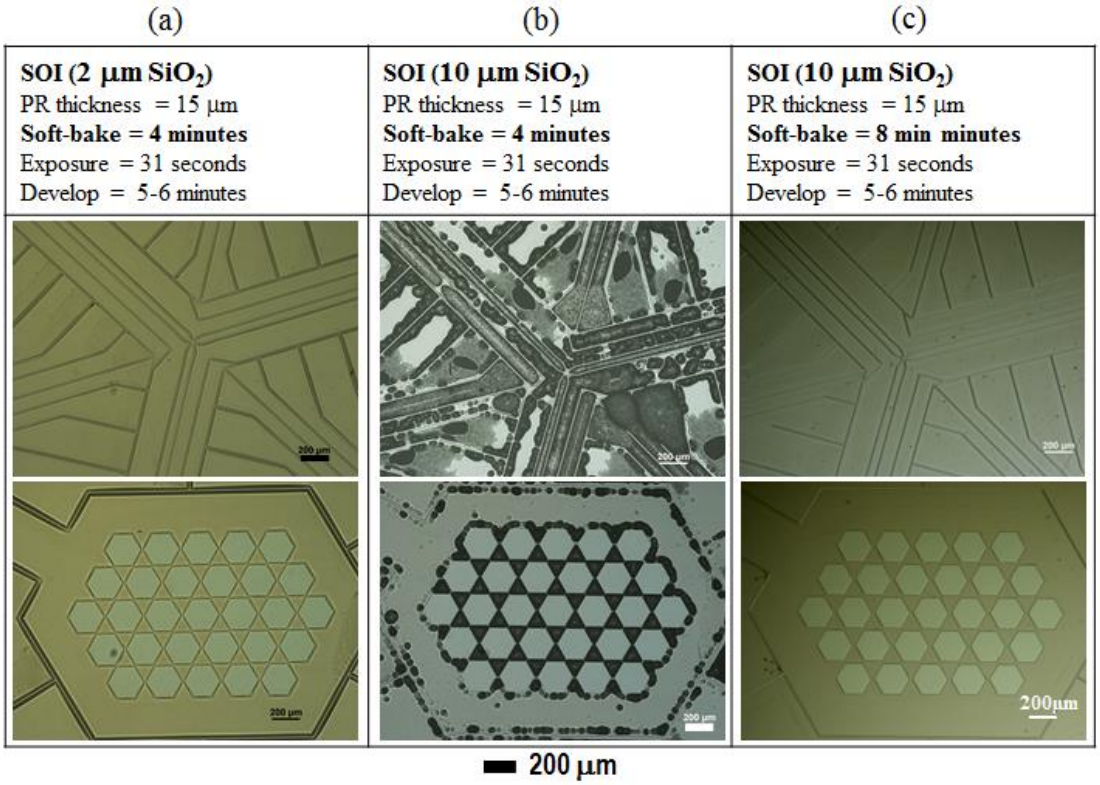


Figure 5.4 – Effect of buried oxide (BOX) thickness to soft-bake time used for a 15-μm thick photoresist. (a) A SOI test wafer with a 2 μm-thick oxide with a soft-bake time of four minutes. SOI test wafers with a 10 μm-thick oxide with (b) a soft-bake time of four minutes observed burnt resist and (c) a soft-bake time of eight minutes with no burnt resist.

Photoresist burning was attributed to the soft-bake time being insufficient for SOI substrates with a thick oxide layer. The soft-bake process reduces the remaining solvent in the photoresist. Thicker resists require longer time for this process than those of thinner resists. The reason for reducing the solvent content is to stabilize the resist film. Short soft-bake times leave a softer resist film which is more prone to photoresist deforming/burning during subsequent plasma-etching steps. Therefore SOI substrates having thick buried oxide layer would require longer soft-bake time to allow heat to dissipate from the bottom of substrate through the resist surface when using a hot plate.

The optimum soft-bake time needs to be optimised for a particular resist thickness (15 μm) and substrate type (SOI substrate with a 10 μm-thick oxide layer). The study was carried out by varying the soft-bake time from the initial value four minutes to 10 minutes.

Also, a comparison between hot plate and oven bake was investigated. After several trial runs, the best practice allowing a more appropriate soft-bake time required for a thick resist-coated SOI substrate to be identified was to spin the resist with different soft-bake times without performing any exposure or development steps prior to the Si DRIE step. In this method, the test wafer were investigated through the DRIE process without any physical etch on the Si device layer of the SOI wafer, and the same SOI wafer could then be reused for the evaluation of soft-baking times to photoresist burning. The optimised recipe with increasing a soft-bake time to eight minutes was found to be suitable for a thick resist film with a target thickness 15 ± 1 μm spin-coated on a SOI substrate with a thick buried oxide. There were no observations of burn photoresist in the subsequent dry etch processes using this optimised recipe.

Generally, the recommended soft-bake condition is 100 °C on a hotplate for 1 minute per 1 μm-thick resist film. However, the optimized soft-bake parameter for 15 μm of AZ9260 PR thickness was performed on a hot plate at 110 °C for eight minutes and followed by one hour relaxation time at the cleanroom temperature (~ 21 °C). The optimised recipe had one major weakness, which was that the resist on the sidewalls was underdeveloped. Using the profiler tool, the excessive photoresist was approximately 50 nm. This problem was resolved using a descum RIE process.

5.4.4 WET etching: Gold/ Chrome etch

The wet chemical etching process involved the removal of the gold (Au) layer using Potassium Iodide (KI) solution, a mixture of gold etchant (KI < 25% + I_2 1-10% + H_2O remaining, OM Group Ultra Pure Chemicals) and DI water at the ratio of 1:2 by volume. The removal of the chrome (Cr) layer was by using chrome etchant (Acetic acid 1-10% + Ceric ammonium nitrate 10-30% + H_2O remaining, OM Group Ultra Pure Chemicals). The process discussed in this section was determined after several trials by varying the concentration of the Au etchant (KI < 25% + I_2 1-10% + H_2O remaining) by mixing additional DI water. Figure 5.5 shows the outcome of one of the trials achieved by etching a wafer patterned with a 1.2 μm-thick positive photoresist (S1813). Without the etch rate

given by the supplier, a non-diluted Au etchant was used to evaluate the etch rate. The dummy wafer was etched for 60 seconds. It is clearly evident from Figure 5.5 that there was a severe undercut through the electrode structures due to the combination of fast etch rate, long etch time and etch lag associated with the sizes of the mask features. The latter issue was attributed to the availability of more ions to etch the larger exposed area on the Au layer compared to that of the smaller exposed areas. Consequently, deep undercuts were formed by the time the Au layer at the small openings was etched completely, thereby causing a significant deviation in the geometry of the critical Y-shaped electrodes.

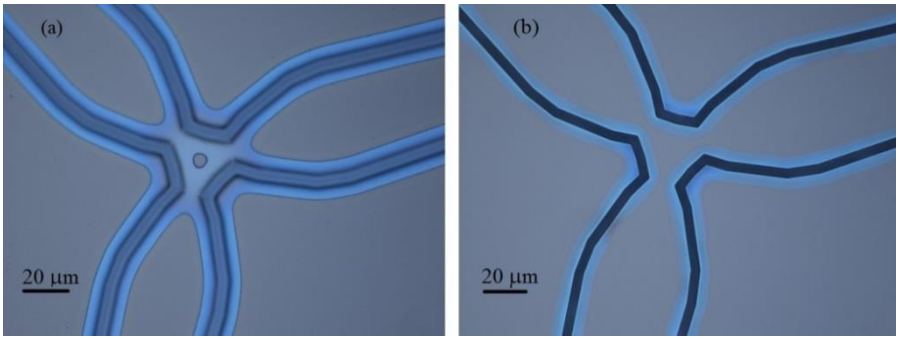


Figure 5.5 – Comparison of severe undercutting (from wet-chemical etching of gold) at the crucial trap region between two different feature sizes. (a) The electrode feature sizes and gap widths of 9.5 µm and 7.5 µm. (b) The electrode feature sizes and gap widths of 15.0 µm and 5.5 µm. (A strong undercut can be seen in an optical microscope as a bright outline of the edges of the trenches in a dark-sharp outline.)

To achieve a well-controlled etch rate on the different feature sizes with a relatively uniform etch across the wafer the lower concentration of the etchant was required. Au etchant mixed with DI water at the ratio of 1:2 by volume was employed to etch the Au layer for 15 seconds (etch rate ≈ 2 µm/min). This was followed by a Cr etch using standard Cr etchant (Acetic acid 1-10% + Ceric ammonium nitrate 10-30% + H_2O remaining) for another 15 seconds (etch rate ≈ 200 nm/min). Figure 5.6 shows the etch results obtained using the optimised process discussed. It is clearly evident that a relatively uniform etch was achieved by minimising the undercut effects. Optical microscope examination revealed that

the central Y-shaped junction region etched slower with relatively minor undercut compared to the previous etch result using the non-diluted Au etchant. By changing the etch concentration, it is possible to achieve arbitrary shaped metallised electrode structures with in-plane complexities using the wet chemical etching process.

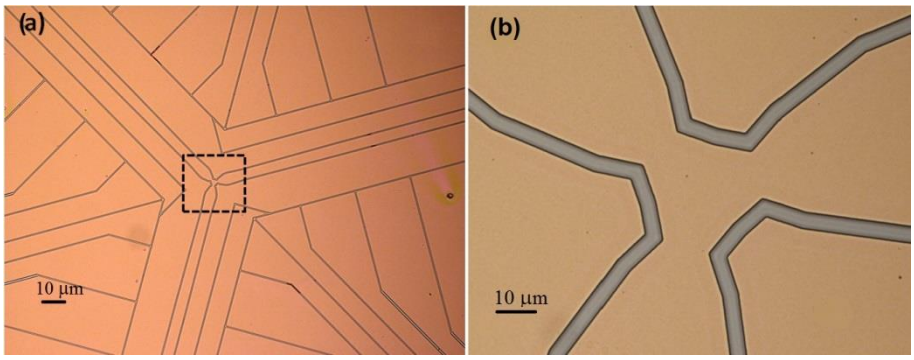


Figure 5.6 – Optical microscope images of the Y-junction trap device after Cr/Au etching with the optimised recipes. (a) The central trap region. (b) A close-up image of the Y-shaped junction. The exposed Si surface appears in a dull grey region after Cr/Au etching. The electrode gap is ≈ 5 µm.

The reliability of the fabrication process to create microstructures close to the design is critical for ion-trap applications. Hence, the comparison was made between the etched features and the corresponding mask by taking in-plane optical microscopic measurements. The microscopic measurements were taken at two regions; namely a) the critical dimensions of Y-shaped electrodes at the centre where RF potentials would be applied, and b) the proximity of the DC control electrodes from the centre to the outer edge. Table 5.3 shows the comparison between the in-plane dimensions of the etched features to the corresponding features on the mask obtained by microscopic measurements. Perhaps the most important contribution is the ability to realise the complex Y-shaped electrode structures with in-plane dimensional variation $< 5.3\%$ which is potentially promising for ion trap applications. Table 5.4 shows similar measurements on the proximity of the DC control electrode structures. The maximum deviation in the proximity of the DC control electrodes was found to be 6.6%.

Table 5.3 - Comparison of the Y-shaped electrode dimensions between the etched feature and the photomask.

Etch zone	Top device			Bottom device (μm)			Schematic Y-junction trap
	Etched (μm)	Mask (μm)	Offset (%)	Etched (μm)	Mask (μm)	Offset (%)	
A	14.82	15.00	1.2	9.63	9.50	1.4	
B	14.93	15.00	0.5	10.00	9.50	5.3	
C	15.44	15.00	2.9	9.91	9.50	4.3	
D (Gap)	5.08	5.00	1.6	7.71	7.50	2.8	

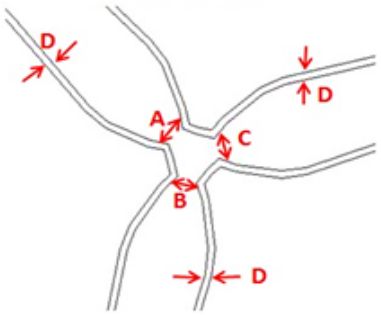
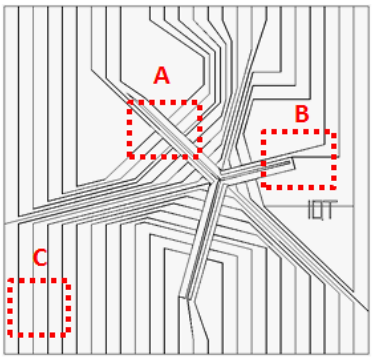


Table 5.4 - Comparison of the DC electrode dimensions (top and bottom devices) between the etched feature and the photomask.

Type	Area	Device	Electrode dimension (μm)				Gap dimension (μm)	Offset to Mask (%)	Schematic of Y-junction trap
			Electrode #1	Electrode #2	Electrode #3	Electrode #4			
Etched features	A	Top	115.7	101.1	61.1	204.5	5.3	6.6	
		Bottom	113.2	101.5	55.7	202.0	7.8	3.8	
	B	Top	114.5	101.8	60.2	202.5	4.8	4.9	
		Bottom	112.2	101.7	55.9	202.4	7.2	3.6	
	C	Top	409.8				10.2	2.4	
		Bottom	409.2				10.2	2.4	
Mask	A/B	Top	112	100	60	200	5.0	-	
		Bottom	110	100	55	200	7.5		
	C	Top	410				10		
		Bottom	410				10		



5.4.5 Deep reactive ion etching (DRIE)

To completely construct the metal-on-SOI microstructures, the electrodes were transferred on to the Si device layer by a deep reactive ion etching (DRIE) process performed in a STS Pegasus system with the Bosch process license. The DRIE technique can achieve a smooth sidewall with roughness < 50 nm and small 2-3 μm trenches having an etch rate of 1-3 μm/min. This system enables microfabrication of high-aspect ratio structures (HARS). Bosch etching mechanism [161] uses directional etching via radicals dissociated from only SF_6 in the high density plasmas called the etching cycle, and then switches to the passivating cycle (or protective polymer deposition) using only C_4F_8 to achieve high aspect ratios. During the subsequent etching cycle, the passivating film allows for complete removal of the bottom of the trenches by ion bombardment while preventing etching of the sidewalls. In some cases, the addition of O_2 gas during the etch step will drive the process toward an ion-assisted chemical mechanism. The alternating cycle of etching and passivating is simply named as a time multiplexed deep etching (TMDE) scheme. The TMDE process tends to inherently develop a scallop-shaped profile. The Bosch etching process commonly used to micro-machine MEM structures is shown in Figure 5.7.

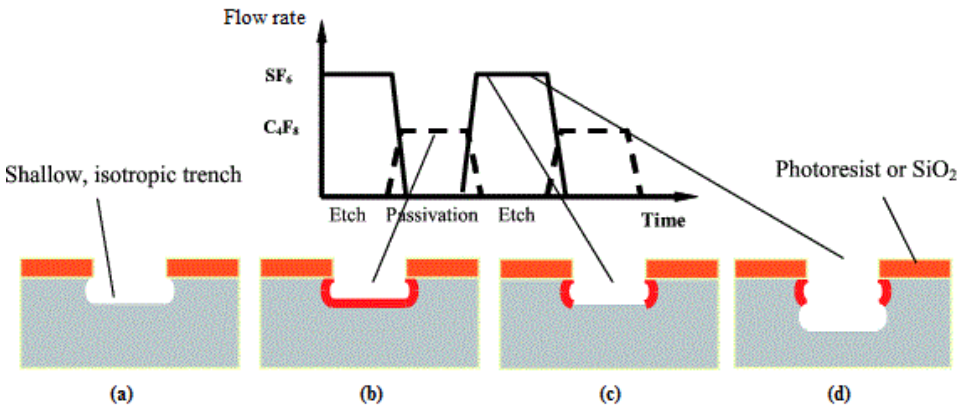


Figure 5.7 – Illustration of the BOSCH DRIE process with an alternating cycle of isotropic etching (by plasma of SF_6) followed by protection film deposition (by plasma of C_4F_8). (a) First isotropic etching. (b) Passivation layer deposition. (c) Start of second etching. (d) Second isotropic etching continues with fluoropolymer sidewall residue. (Figure from ref. [162].)

In the study of the HAR silicon etch [161], [163], several key challenges to achieving HAR, including the inherent disadvantages, were discussed. For instance, the dependence of etch rate on feature size is observed where wide trenches etch quicker than narrow ones. Aspect ratio dependent etching (ARDE) or RIE lag is a transport phenomenon that occurs when a wide variation in feature sizes has to be etched simultaneously. The root cause of ARDE is the depletion of the fluorine content at the trench bottom based on the SF_6 flow rate and its dissociation. ARDE causes the large features to be etched faster since the higher the aspect ratio (trench depth/width), the more difficult it is for the reactants to reach the trench bottom and for the by-products to escape. Also the etch uniformity is varied from the centre to the outer edges of the entire wafer. Aside from the scalloped sidewall obtained from the TDME process, the notching (or footing) effect is also a common phenomenon of the TMDE process. The root cause of notching is charge accumulation resulting in the excessive lateral etch in regions where silicon has an underlying dielectric layer, which is a buried oxide layer in the case of SOI substrates. One solution to prevent notching is to increase the thickness of the polymer during the period of over-etch by increasing the duration of the passivating cycle. In achieving the desired shaped profiles (opening/closing or straight), the optimisation of critical DRIE process parameters such as O_2 flow rate, SF_6 flow rate, ratio of etching/passivation cycle, RF power, pressure and temperature is required.

Based on the standard recipe developed at the Southampton Nanofabrication Centre (SNC) with Surface Technology Systems (STS) ICP DRIE (Bosch process), users are given the standard recipes to further develop a particular recipe corresponding to device structures and applications. The selectivity of DRIE on Si material by using a photoresist (PR) mask is suggested at $\approx$ 20:1. Thus, the resist thickness should be more than 2 μm for etching a 30 μm-thick Si device layer. The optimisation of the DRIE process was first performed on Si test wafers instead of SOI wafers. A 6 μm-thick photoresist AZ9620 was spun on a virgin Si test wafer (Wafer Prime Si type N<100> phosphorus doped) with 640-675 μm of Si thickness. The DRIE result from the first batch (see Table 5.6, Recipe: SNC#1) shows a micrograss formation or 'black silicon' at the bottom of the etched trenches. This is shown in optical microscope images presenting as dark spots across the etched regions; (a, b). The photoresist

was removed using the PVA Tepla 300 Plasma system (O_2 600 mL/minute, 800 W for 10 minutes) before taking the cross-section scanning electron microscopy (SEM) images. The wafer was then diced into individual chips, which were cleaved to get a cross-section of the electrode gaps. From the cross-section SEM images of the electrode gaps and periphery (dicing line) shown in (c, d), the anisotropic etching profile was obtained. It also suggested that the etch lag was inherently exhibited in the developed DRIE Si etch process when various interelectrode gaps with different dimensions were etched simultaneously. A narrow trench of the interelectrode gap < 10 μm was etched slower than a wider trench at the periphery with depths of approximately 31 μm and 38 μm, respectively.

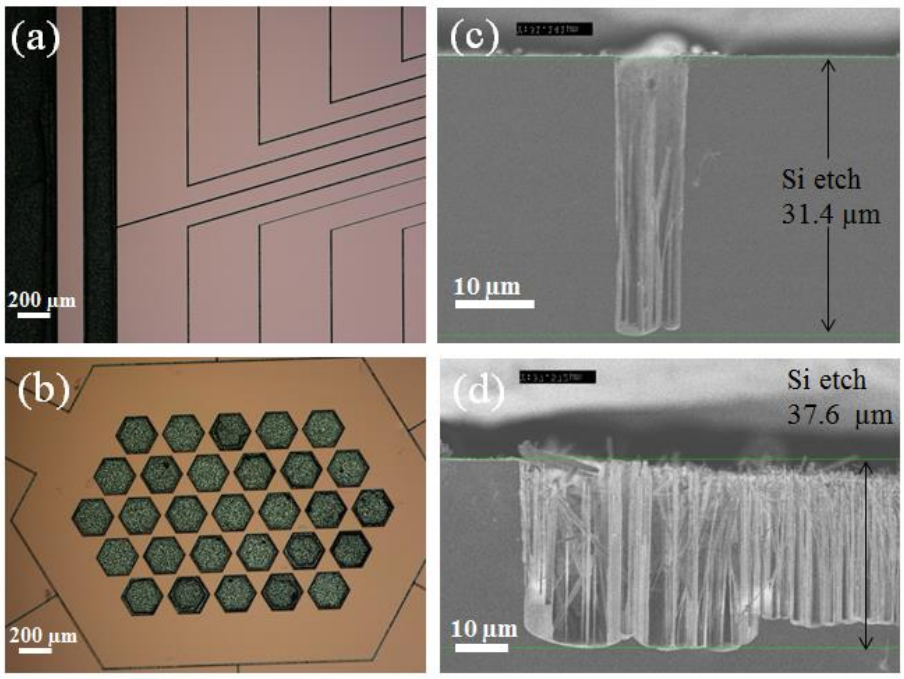


Figure 5.8 – Micrograss formation after DRIE from the initial run (Recipe name: SNC#1). (a-b) An optical microscope image of the trap shows dark spots in the etched trenches. (c-d) Cross-section SEM images of a small trench (10 μm) and large trench (>200 μm) showing a needle like so-called micrograss.

The micrograss formation is possibly caused by a combination of high automatic pressure control (APC) and high deposition-to-etch cycle time ratio, and also the effect of etch gas flow, SF_6 based on the study by Wu et al. [163]. There are several solutions to solve the grass formation such as increasing the etch gas flow rate, etch-to-deposition cycle time ratio, pressure, etch coil power or platen power. The initial DRIE recipe was optimized by adjusting the two main processing parameters. The adjustments were made by increasing etch-to-deposition cycle time ratio, and the platen power (see Table 5.6, Recipe SNC#2). The optimised DRIE recipe showed a good result by eliminating the micrograss issue. ARDE ratio was still less than 2:1. However, it promoted a negative profile compared to the initial the DRIE optimisation process, several silicon test wafers including SOI processing wafers were patterned with various PR AZ9260® thickness of 6-16 μm using this tuned recipe (SNC#2). The resist thickness of ~ 6-7 μm was suitable for the subsequent oxide etching process by a buffered HF (Flow B). However, a thicker resist of 12 μm or more (estimated by a 30 μm-Si etch by DRIE with a selectivity of 14:1 ratio and a 10 μm-thick oxide etch by ICP with a selectivity of 1:1 ratio) was required for a series of dry etching processes (Flow C).

Table 5.5 - STS DRIE Si etching result using Recipe SNC#2.

Feature size (μm)	Etch zone	Etch Depth (μm)		Trench width (μm)		Etch rate (μm/min)		Selectivity		Profile angle θ (°)
		(d_1)	(d_2)	(w_1)	(w_2)	(d_1)	(d_2)	(d_1)	(d_2)	
Small < 20	Centre	35.81	37.43	12.29	15.49	5.64	5.99	13.72	15.75	91.5
	Middle	36.21	38.71	11.60	15.74	5.83	5.16	15.27	15.25	95.0
	Edge	36.71	39.17	11.84	15.35	5.82	5.22	15.25	15.44	93.6
Large > 200	Centre	42.80	47.27	232.50	237.75	5.71	6.30	16.87	18.63	92.0
	Middle	43.34	49.84	300.00	315.00	5.78	6.65	17.08	19.64	95.0
	Edge	43.60	50.68	206.93	212.70	5.81	6.76	17.18	19.97	95.2

Table 5.5 provides the summary of DRIE Si etch results using Recipe SNC#2. The data were taken from the center to the outer edges of the six-inch wafer. This process achieved an etch rate of 5-7 μm/min across the wafer with a selectivity Si to photoresist (PR)

from 15:1 to 20:1 and a sidewall angle of up to 95 degree. The etch rate variation of the small trench was from 5 μm/min at the centre to 5.22 μm/min at the outer edges of wafer. As expected, the larger diameter trench was etched faster with an etch rate of 6.3-6.8 μm/min. The measured uniformity was ± 2.3% and ± 4% for the small trench and large trenches, respectively. Figure 5.9 shows cross-section SEM images illustrating Si etching results using Recipe SNC#2.

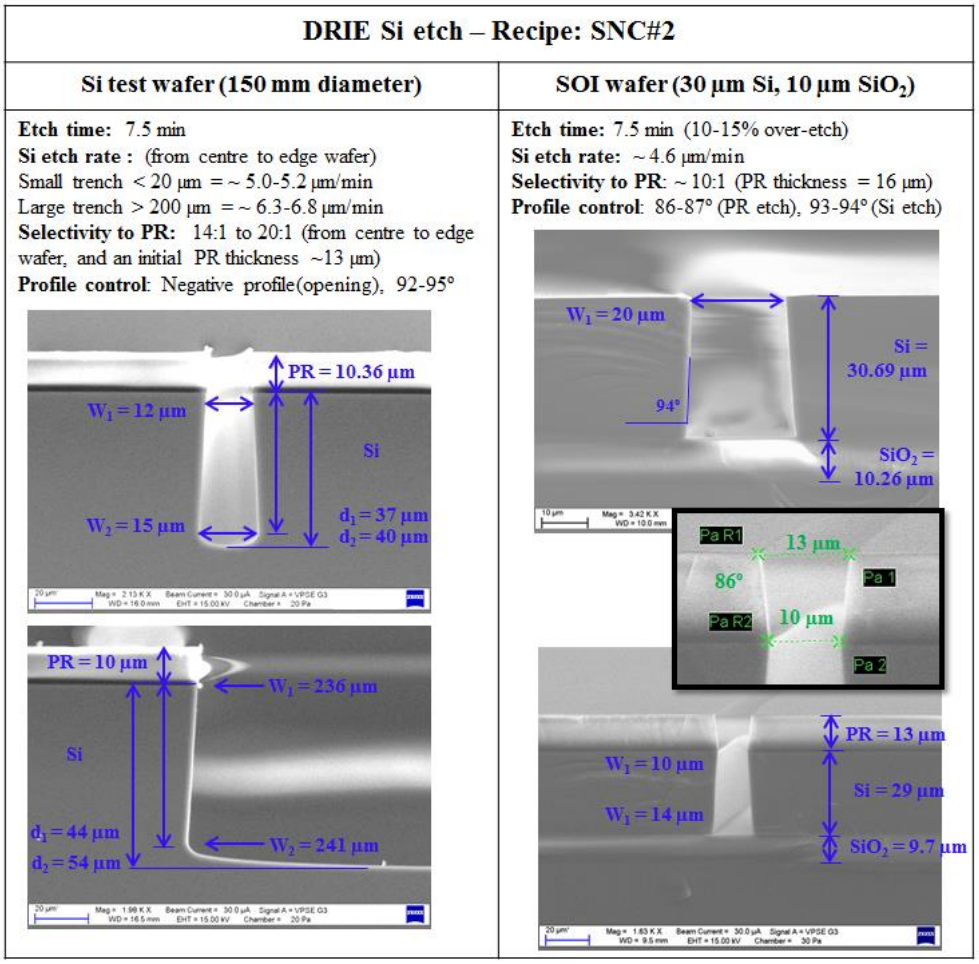


Figure 5.9 – STS DRIE Si etching result using the optimised recipe (Recipe name: SNC#2).

During the process development, the STS DRIE equipment at the Southampton Nanofabrication cleanroom (SNC) broke down for several months and was eventually replaced with a new model. To avoid fabrication delays which could take up to three to four months based on the replacement schedule, the pending tasks were continued using the cleanroom facilities and the STS DRIE machines at University College London (UCL). The DRIE Si etching process developed in the UCL cleanroom (Recipe: UCL#1)[5] achieved a high selectivity (to PR) ranging 47:1 to 66:1 (small to large trench) but slower etch rate 1.5-2.3 μm compared to the previous recipes. This recipe exhibited a straight sidewall profile control 90 ± 1 degree. However, the notching (or footing) effect was observed at a smaller trench diameter (less than 20 μm) but not found at any larger trenches greater than 40 μm (see Figure 5.10). This is due to the fact that our SOI-based structures consist of a buried oxide layer which acts as etch-stop layer.

For SOI substrates, the conventional DRIE process contains many aspects that lead to notching. Charging accumulation at the oxide layer is the main reason for the notching problem which widely exists in SOI structures. Notching occurs due to the surface charge accumulated on the oxide interface. The notching formation involves three mechanisms of electric field effect – i) charging transient, ii) Si etching reactions, and iii) the forward scattering effects of ions from the exposed insulator – causing sidewall passivation breakdown an thus the unwanted lateral etching into the sidewalls [164]. The notching effect on SOI substrates containing non-uniform trenches (depending on the ARDE, microloading or RIE lag) can be reduced using a multi-step process recipe [165]. In addition, one useful technique available for use on the STS ICP-RIE system is the low frequency puled etch which allows the ions to escape the surface of the oxide, resulting in decreasing of the charge build-up and reducing of the notching [166], [167]. However, the further optimisation of notch reduction on the processing SOI wafers was not proceeded due to the limited access and working hours at UCL cleanroom. Table 5.6 provides the details of the DRIE Si etch processing recipes developed at the SNC and UCL cleanrooms.

[5] The DRIE Si etch (Recipe: UCL#1) was developed by Graham S. Wood, a PhD student at the Nano Research group, University of Southampton

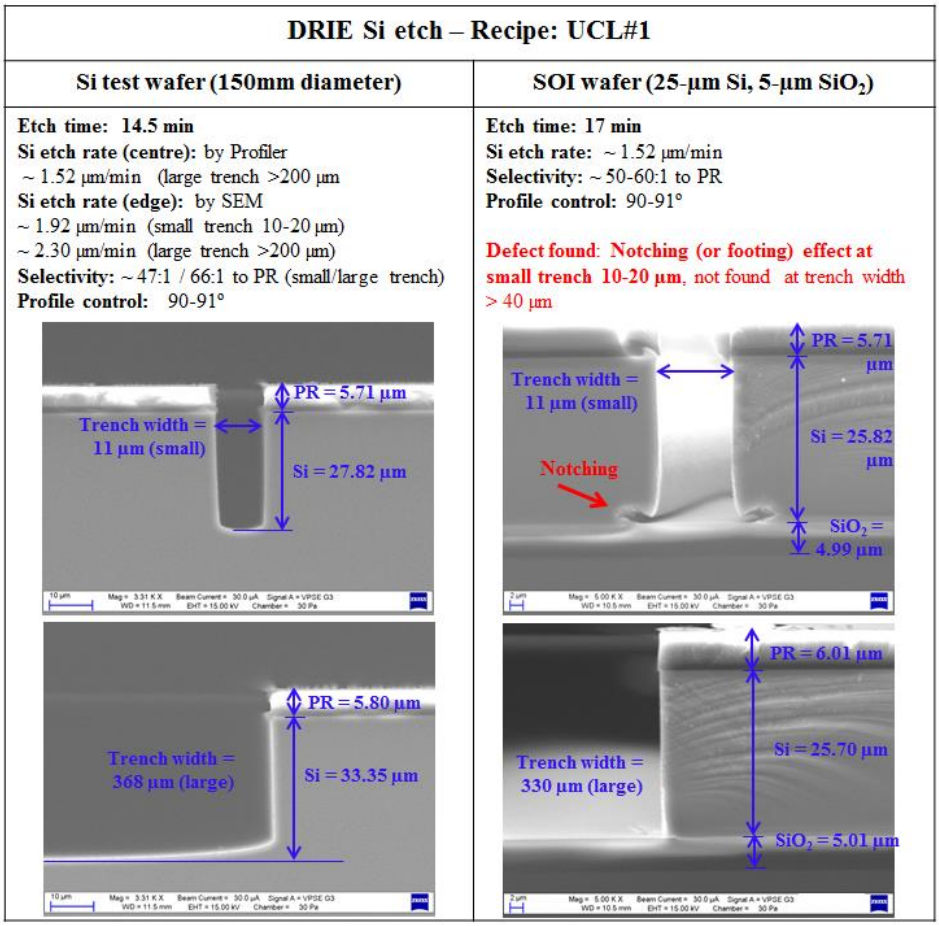


Figure 5.10 – STS DRIE Si etching result using the recipe developed at UCL (Recipe name: UCL#1).

Table 5.6 - STS DRIE Si etching process recipes developed in the SNC and UCL cleanrooms. Etch results are based on small feature size < 20 µm located at the centre of a wafer (the lowest etch rate).

Recipe	Cycle time (Etch/Pass)	SF_6+O_2 flow rate	C_4F_8 flow rate	Platen Power	Coil Power (Etch/Pass)	Pressure (Etch/Pass)	Temperature	Etch rate	Selectivity to PR	Side-wall angle θ
	sec.	sccm	sccm	W	W	mTorr	°C	µm/min	-	(°)
SNC#1	1.7/2.0	36.21	38.71	11.60	15.74	5.83	5.16	5.00	14:1	95.0
SNC#2	2.6/2.6	36.71	39.17	11.84	15.35	5.82	5.22	5.64	14:1	93.6
UCL#1	9.0/5.5	42.80	47.27	232.50	237.75	5.71	6.30	1.92	47:1	92.0

5.4.6 Buffered oxide etch (BOE or BHF)

The exposed buried oxide (BOX) layer between electrodes need to be etched away to avoid a build-up of static charges on the dielectric surfaces. Oxide etching is primarily based on the hydrofluoric (HF) acid. The HF will etch the amorphous SiO_2 without attacking the Si surface. Since wet etching of SiO_2 using concentrated hydrofluoric (HF) acid induces a lateral undercut as it does in a vertical etch, buffered oxide etch (BOE) solutions with different concentrations of NH_4F, also known as buffered HF or BHF are more favourable for etching small structures. Buffered oxide etch results in a relatively slower etch rate compared to the concentrated HF (49%) or HF/H_2O mixture. In this work, a commercially-available solution of a 7:1 buffered HF (NH_4F (40%) + HF (50%) in a 7:1 ratio) was used. Based on the study undertaken by Williams et al. [168], the etch rate of thermal oxide in a 5:1 and 10:1 BHF solution at 20 °C given in Table 5.7 suggests that the etch rate in a 7:1 BHF solution can vary between 50 nm and 100 nm per minute.

Table 5.7 - Thermal oxide etch rate collected from different HF concentration. (Table modified from ref. [168].)

Etchant	Thermal oxide etch rate (nm/min)
Concentrate HF (49%)	2300
10:1 HF	23
25:1 HF	9.7
100:1 HF	2.3
5:1 BHF	100
10:1 BHF	50
20:1 BHF	30

At room temperature, a 7:1 BHF solution etches the thermal oxide at ≈ 60-70 nm per minute. To successfully etch a 10 μm-thick oxide layer, the total etch time may vary between 150 ± 10 minutes. From the initial trial runs, 150 ± 10 minutes were required to completely etch away a 10 μm-thick oxide layer. The success of the oxide etch was observed by

the change of its colour (a rainbow of colourations as the thickness altered and eventually disappear completely with the exposing of the Si layer (a grey colour) underneath). However, long etching in a buffered HF solution for 150 minutes actually resulted in several process problems such as pinholes in the Au/Cr layer, completely undercutting (and lifting off) in very narrow geometries, stiction, and contamination as shown in Figure 5.11. It was suspected that the pinhole issue was a result of the long immersion time in the buffed HF etchant solution. In theory, the common hard masks for glass or oxide etching such as metals (e.g. Al, Ni, Cr and Au) are resistant to HF [168], [169]. However, these can cause failure in practice because any cracks in tensile-stressed film tend to enlarge and let the etchant penetrate through them as explained by Franssila [170]. A similar defect was observed as shown in Figure 5.12.

To investigate the effect of the long etch time on the pinhole issue, the total etch time was split into 20-minute and 10-minute sections. The chips were immersed in the 7:1 buffered HF solution for 20 minutes, rinsed with DI water, and then placed back into the buffered HF solution for another 20 minutes. This process was repeated until the total etched time reached 150 minutes, or when a completed oxide etching was observed. The first batch showed a positive result with less number of pinholes. Next, the shorter interval etch time of 10 minutes was repeated. The result showed no incident of pinholes or damages to the Au/Cr layer. Nevertheless, this problem was still observed on some chips but to a very minimal degree compared to the initial 150-minute and 20-minute interval times.

Because of the large surface tension of HF solution and the hydrophobic nature of the silicon, the formations of air bubbles mostly located between small interelectrode gaps was also observed during the etching process. This incident is shown Figure 5.11(e) which can be clearly seen under the optical microscope (dark field mode) where air bubbles left some marks over the isolation trenches between electrodes. These air bubbles partly prevented the BHF etchant from dissolving the buried oxide layer at the bottom of the trenches resulting in the partially un-etched area of the oxide layer as shown in Figure 5.11(f) after a 150-min total etching time. To reduce the risk of air bubble formation, the samples were immersed in DI water to wet the wafer surface before BOE etching.

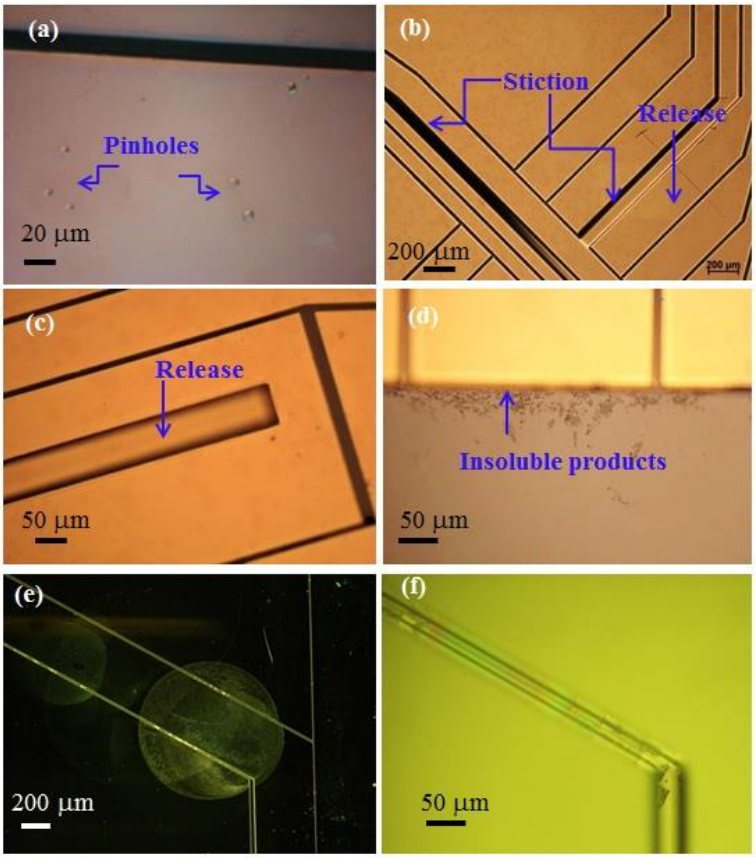


Figure 5.11 – Process problems after long duration etching of 150 minutes in a 7:1 BHF solution. (a) Pin holes on gold electrodes. (b-c) Stiction and completely undercutting (and lifting off) in narrow electrodes. (d) Contaminants. (e-f) Formation of air bubbles in the etched trench, resulting in non-uniform etch.

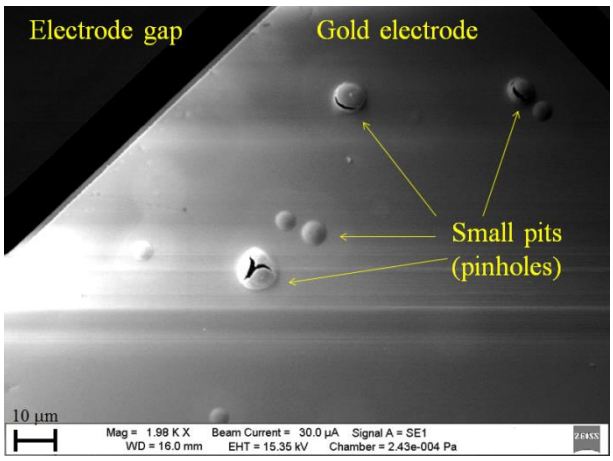


Figure 5.12 – A SEM image of the Y-junction trap fabricated by the process flow A. With long duration etching of 150 minutes in a 7:1 BHF solution (for a 10 µm oxide etch), the BHF process leaves small pits (or pinholes) on the Cr/Au surface.

Figure 5.13 shows cross-section SEM images after a completed oxide etch showing the deep V-shaped undercuts of the oxide layer underneath the Si device layer. The extended study of this particular undercut profile was carried out by observing the etch profile using the cross-section under SEM at different etch cycle times until the over-etching period occurred. A typical isotropic wet etch profile from the start to a half-way etch of 5 μm within 70-80 minutes (see Figure 5.13 - etch time from zero to 60 minutes) was observed. Since the 10-μm thick SOI wafer is a fused bond SOI substrate with a double oxide layer (5 μm + 5 μm) formed by oxide film-oxide film (SiO_2+SiO_2) bonding, it is likely that the wet etch mechanism behaves differently compared to typically isotropic profiles of wet chemical etching. Since the etch rate has a relation with the bond strength, the presence of a weak bond strength leads to a faster etch rate [152], [171]. In this case, the buffed HF solution etched the buried oxide much faster at the area of a weak bonding interface of two oxide layers (5 μm - 5 μm SiO_2 bonding), leading to the locally enhanced lateral etching (see Figure 5.13 etch time from 90 minutes to 200 minutes).

With this unique etch behaviour, additional HF etch experimental runs were conducted with two different oxide thickness of 2 μm and 5 μm fabricated by a single buried oxide layer. Figure 5.14(a, c) indicates that a typical wet isotropic etch profile is exhibited in a single oxide SOI structure. However, a deeper undercut and a much faster etch rate at a weak strength bond between the buried oxide and the handle wafer which were bonded together were observed in this single oxide SOI structure as shown in Figure 5.14(b). A comparison of undercut profiles between a single oxide layer and double-oxide layer of SOI structures based on this study is illustrated in Figure 5.15.

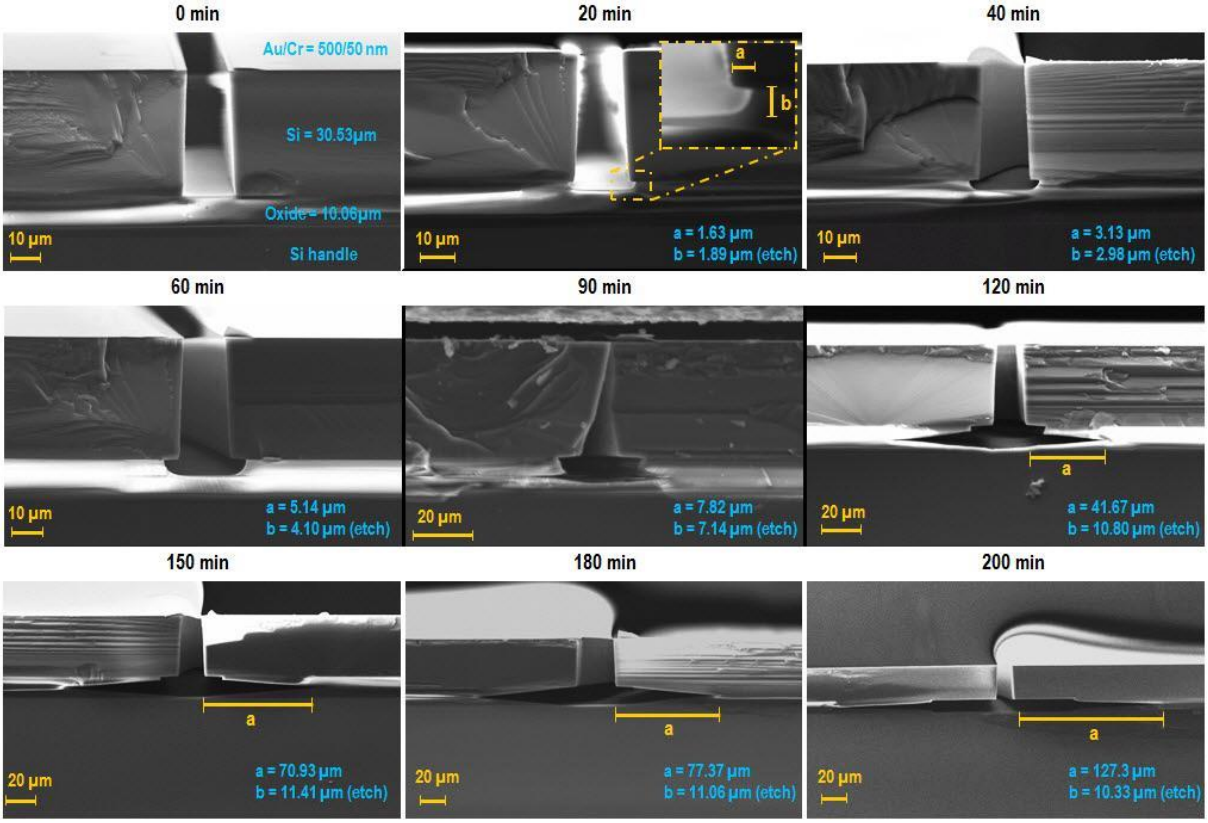


Figure 5.13 – Cross-section SEM images of a deep V-shaped undercut in a 10 µm-thick buried oxide (5 µm SiO_2 - 5 µm SiO_2 bonding) using a 7:1 BHF etching solution.

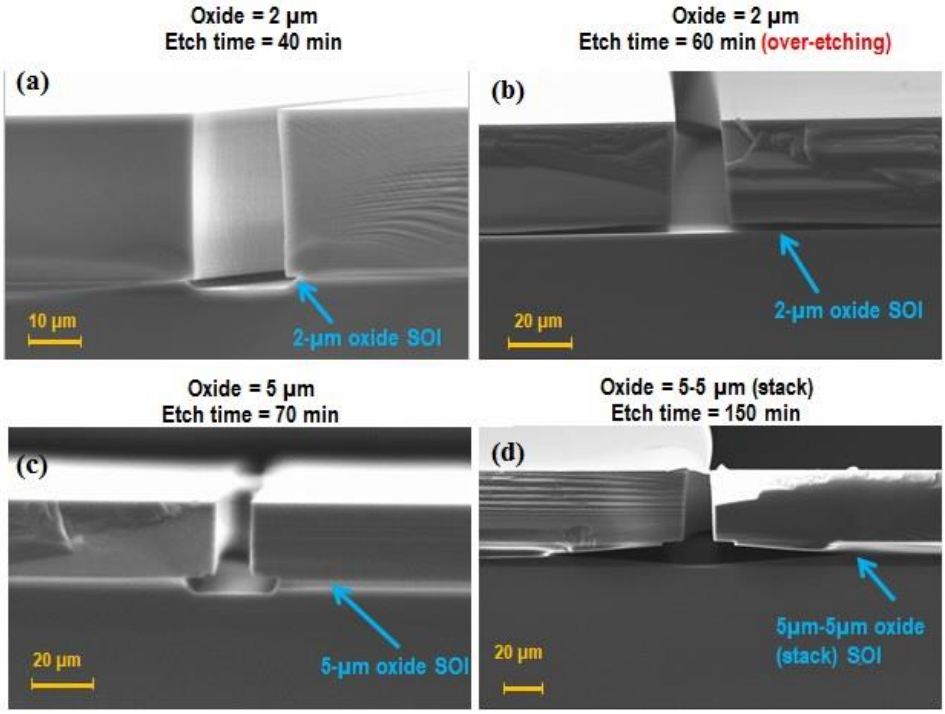


Figure 5.14 – Cross-section SEM images of undercut profiles from a 7:1 buffed HF etching in SOI wafers with different buried oxide thicknesses. (a) and (b) A 2 µm-thick oxide layer. (c) A 5 µm-thick oxide layer. (d) A 10 µm-thick oxide layer (5 µm SiO_2 - 5 µm SiO_2 bonding).

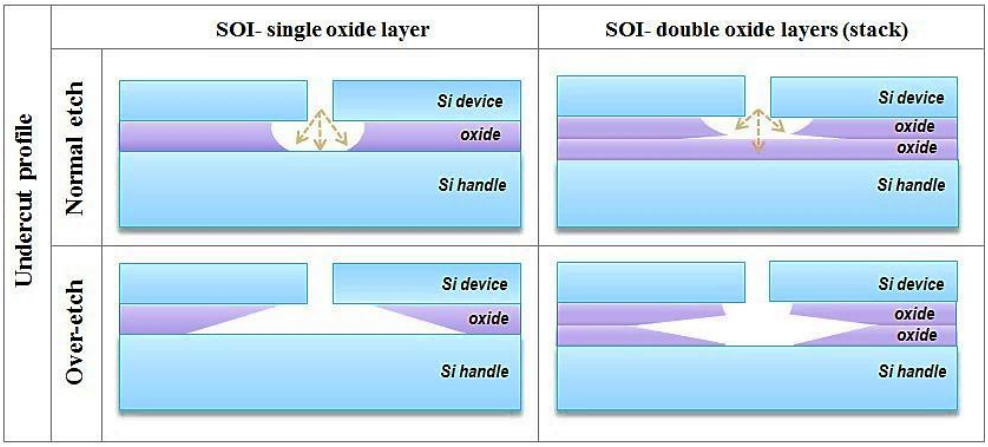


Figure 5.15 – Schematic of the undercut profiles of the etched buried oxide in a buffed HF. (Left) A single buried oxide (standard process). (Right) An oxide-oxide bonding (customised process).

Even though this process produces such a massive undercut (≈ 60-70 μm), it becomes very beneficial for the improvement of electrical breakdown up to 1 kV at the drive frequency $\Omega_{RF}/2\pi = 28 \pm 0.5$ MHz in vacuum as reported in the study of surface breakdown voltage on the SOI samples conducted by Sterling [135], [172] at the collaborators' laboratory[6]. On the other hand, this deep undercut severely affects narrow electrodes with diameter less than 100 μm, and results in a completed completely undercutting of the oxide layer. Without having a supportive oxide layer underneath the active regions, the long and narrow electrodes tend to lift off as shown in Figure 5.11(b, c). For gold surface damage, one possible solution is to deposit multiple layers of gold to improve the metal mask quality. Unfortunately, the smoothness of the gold surface is also critical in the ion-trap operations. To avoid the pinhole issue, the silicon layer may be used as the etch mask since HF does not attack Si. Another problem is stiction caused by the drying of released or over-hanging structures. Unfortunately, this problem is inevitable since the proposed process using the short-interval of etch time will lead to a more frequent drying step. Although stiction can be overcome by using HF vapour phase etching, the massive lateral etches or undercuts could not be resolved. In summary, a 10 μm-thick oxide layer was fully etched using a 7:1 BHF solution at etch rate of ≈ 60-70 nm per minute.

Despite the fabrication issues discussed above, fabricating good devices of a 2D lattice ion trap was achieved; these traps have electrode dimensions in the order of hundreds of microns. However, a zero yield was obtained for a Y-shaped junction trap having the electrode widths < 100 μm. An inductively coupled plasma (ICP) dry etching is therefore a choice of oxide etching process for smaller ion-trap geometries as described in the section below.

5.4.7 Inductive Coupled Plasma Etch (ICP)

One of the most widely used plasma sources for dielectric material etching is the inductively coupled plasma (ICP) etching process. The etching of oxide using ICP plasma with various fluorocarbon gas combinations such as CF_4, CHF_3 and C_4F_8 has been carried out

[6] Ion Quantum Technology (IQT) group at the University of Sussex, UK

experimentally in several studies [173]–[180]. Fluorocarbons are ionised to generate a mixture of fluorine and carbon ions. These ions are then accelerated down to the oxide film where fluorine combines with silicon and carbon combines with oxygen. The volatile etch products, SiF_4 and CO_2 are then pumped away leaving an etched structure. The contribution from ion bombardment is essentially required to break the Si-O bonds and to atomise Si [173]. Thus, increasing the RIE bias power will increase the oxide etch rate, but will lower the oxide-to-resist selectivity ratio. Since every SiO_2 molecule needs one intact carbon atom and four intact fluorine atoms, there will be excessive carbons in the chamber which will possibly deposit back on to the substrate. For this reason, a small amount of O_2 additive is generally used to remove re-deposited carbon atoms.

The system used in this work was an OIPT SYS380-based inductively coupled plasma (ICP) reactor. This ICP features include a 1.8-2.2 MHz 3 kW remote plasma RF generator, and a 13.56 MHz 300 W RF platen generator for DC bias. This system allows for independent control over both the plasma density at the top coil and the sheath bias at the platen, thus yielding significant improvements in the achievable structures. The tool is compatible with both four-inch and six-inch wafers, which is mechanically clamped to the substrate holder against the platen for helium backside cooling. The helium applied to the backside of the wafer maintains a constant wafer temperature during processing. In particular, this work used two etching tools - a metal contaminated ICP reactor and a non-metal contaminated ICP reactor - to develop the recipes for etching a 10 μm-thick buried oxide of the SOI wafers. Experiments were initially carried out using small samples, followed by the actual run on the processing SOI wafers (six-inch wafers) using the optimised recipes. For oxide etching, the gases available in these two systems include C_4F_8, SF_6, Ar and O_2 for a metal contamination chamber and C_4F_8, CHF_3, CF_4, SF_6, Ar and O_2 for a non-metal contamination chamber.

Gas mixtures of C_4F_8-based plasma are promising for the development of high-performance plasma etching processes. The most frequently used gases added to C_4F_8 for oxide etching are Ar and O_2 gases. In fluorocarbon gas mixtures, fluorocarbon deposition on the surface occurs along with fluorocarbon etching. To provide a better insight of the relative process changes of the fluorocarbon deposition and etching rates, Li et al. [180] investigated

the effect of Ar and O_2 additives on SiO_2 etching in C_4F_8-based plasma using the ICP etch process. The data show that the addition of Ar and O_2 is useful for controlling the degree of surface polymerisation and etching selectivity compared to pure C_4F_8. However, the etch rate of oxide is significantly dependent on the thickness of the fluorocarbon film. The etching rate of oxide can be improved when applying a sufficient self-bias voltage resulting in only a thin fluorocarbon film developed with the direct ion-induced chemical etching dominating the oxide etch.

In this work, C_4F_8/O_2 gas mixture was selected for oxide etching with the metal film mask (500 nm Au, 50 nm Cr). The initial process parameters were C_4F_8/O_2 = 40/100 sccm, 10 mTorr at 20 °C, 150-watt RF power and 1400-watt ICP power. After several trials with varying RF powers from 70 W to 250 W, a set-up of 200 W was adequate to achieve the etch rate of 180 μm/min and the oxide-to-resist selectivity ratio of 0.8:1.0. However, the selectivity of the metal mask to the oxide at this condition was very low. The metal film mask was completely etched away after the first etch cycle of 10 minutes, with an oxide etch depth of 1.8-2.0 μm and an etch rate of 170-190 nm/minute. During the second to fifth etch cycles, the Si layer became the etch mask for the oxide etch with the selectivity of SiO_2 to Si at a 1:1 ratio. The oxide etch rate was approximately 180-200 nm/minute.

Figure 5.16(top) shows the cross-section SEM images of a 10 μm trench etched by the optimised recipe named Recipe#1. The vertical etch depth of 1.8 μm was obtained after the first cycle (10 minutes) with a very thin metal mask remaining. The fully etch of a 10 μm-thick oxide is demonstrated in Figure 5.16(bottom). This process was achieved using 10-minute etch intervals to a total etch time of 50 minutes (five cycles) with the vertical etch rate of 187-200 nm/minute and the etch depth of 9.5-10 μm. The metal mask was completely etched away after the first cycle for 10 minutes giving the etch depth of 1.8 μm. The etch profile with a positively sloped angle in the range of 75-80° was presented. Under the identical process condition, Recipe#1 with the mixture of C_4F_8/O_2 process still led to the development of residual fluorocarbon polymers on the wafer surface after multiple-etch cycles (see Figure 5.17).

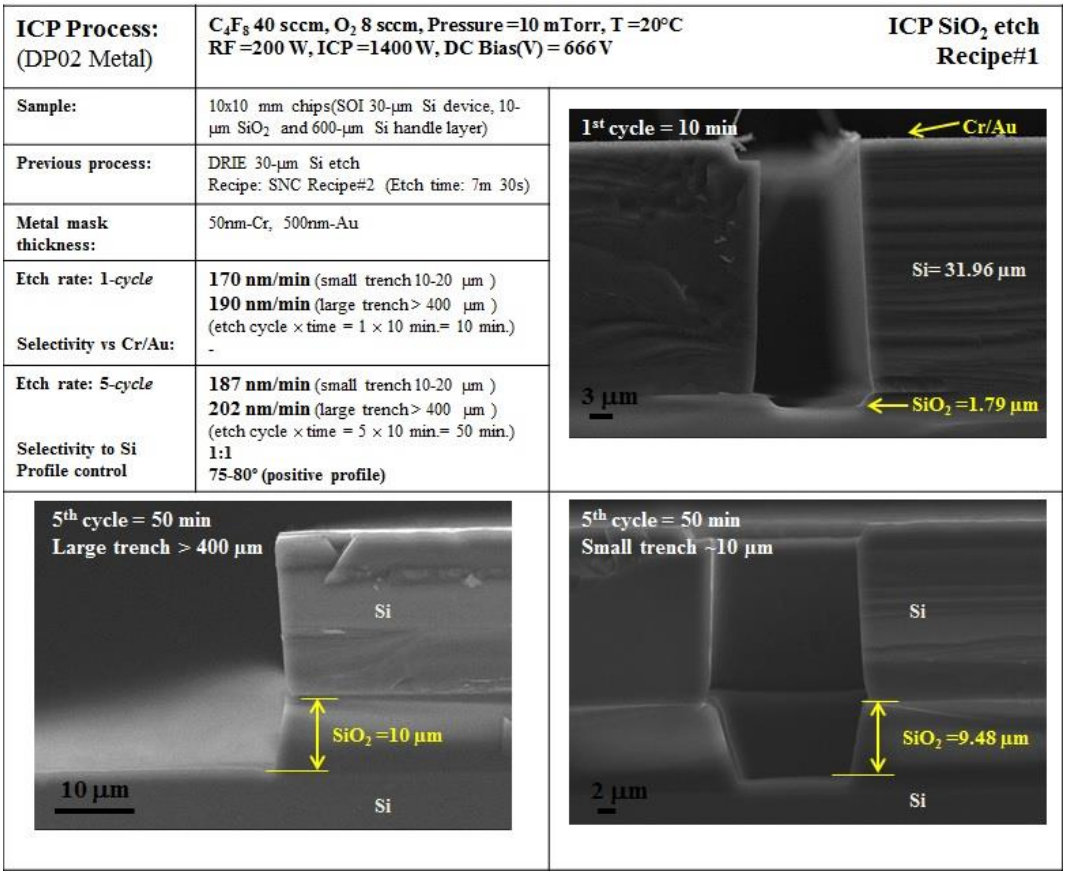


Figure 5.16 – Cross-section SEM images of a 10 µm-thick buried oxide etched using ICP process - Recipe #1 with a mixture of gases C_4F_8/O_2 = 40/8 sccm flow rate, RF/ICP power = 200/1400 W, pressure at 10 mTorr, and temperature at 20 °C.

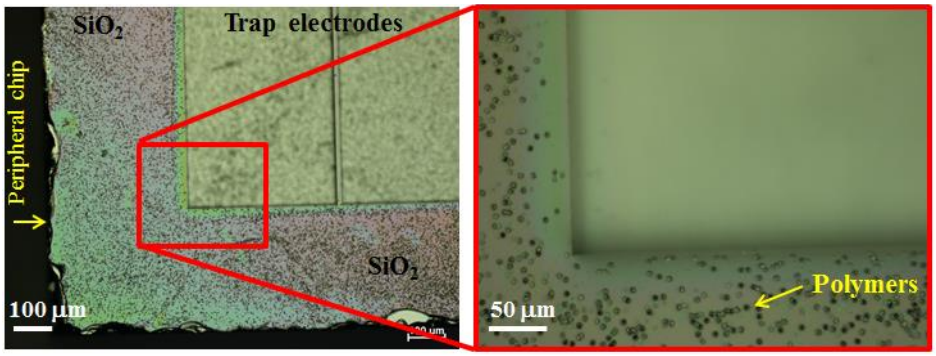


Figure 5.17 – Optical microscope images of the etched oxide using ICP process (Recipe#1) with gas mixtures of C_4F_8/O_2 showing C-F polymers on the etched areas appearing from the third etch cycle.

The ICP process optimisation was continued in the ICP dielectric etcher. In this work, standard silicon wafers were initially subjected to a wet oxidation process to grow a 1 μm-thick oxide layer. The electrode structures were then patterned using photolithography with a 6 μm-thick AZ9260 photoresist on this oxide film. These wafers were used as dummies for the process optimization instead of SOI wafers. Several trials were carried out using standard oxide etch recipes (for microstructures and nanostructures) developed in the Nanofabrication centre environment. One of the most promising standard recipes was the gas mixtures of $CHF_3/C_4F_8/O_2$ = 44/40/10 sccm at a chuck temperature of 15 °C, ICP/RF platen power of 1500/100 W and a process pressure of 7 mTorr. This process was achieved in etching a thin oxide thickness < 1 μm with the etch rate of 300 nm/minute, sidewall angle of 80 degrees, an etch depth of 1.5 μm/5 minutes, and the oxide-to-resist selectivity ratio of 1:1. The same recipe was repeated on a SOI wafer patterned with a 15 μm-thick AZ9260 photoresist as the etch mask with a target etch depth of 10 μm. To fully etch a 10 μm-thick oxide, the process would require ~ 35 minutes of the etch duration based on the etch rate obtained from a five minute etch cycle. To avoid the thermal dissipation problem in SOI wafers, which could damage the photoresist mask during a long etching process, the etch duration needed to be less than 5 minutes. Therefore, the total etch time of 35 minutes was split into shorter five-minute intervals for seven cycles and a cooling interval time was added to the recipe to ensure that the inherent heat build-up during the etching process would be minimized.

Figure 5.18 illustrates the etch profile obtained under ICP process condition Recipe#2 shown in Table 5.8. The shape of the etched trench presented is a V-shaped profile. Due to negatively sloped sidewalls of the Si top layer etched by the DRIE process from the previous step, the negatively sloped sidewalls also unintentionally act as an oxide etch mask. The effective ion flux along these angled sidewalls is reduced compared to those of vertical sidewalls (88-90 degree) allowing the ion flux goes straight to the bottom of the trench (flat region). A higher etch rate at the bottom of the trench and a lower etch rate close to the sidewalls are expected, resulting in a gradual formation of a V-shaped etch profile. The etch rate was decreased by more than half of that obtained from the first cycle etch. The etch depth of small trenches varied from 2.41 μm to 5.06 μm with poor oxide-to-resist

selectivity ratio of 0.56 observed. Another issue found was that the excessive polymer re-deposition can be seen at the bottom of trenches and the sidewalls as shown in Figure 5.20(a, b). This signature is one of the common defects associated with oxide etching in CHF_3/C_4F_8-based plasmas reported in some previous studies [177], [181]. The balance between fluorocarbon deposition and etch reaction results in a net polymer accumulation which becomes more significant for long etching processes [178]–[180].

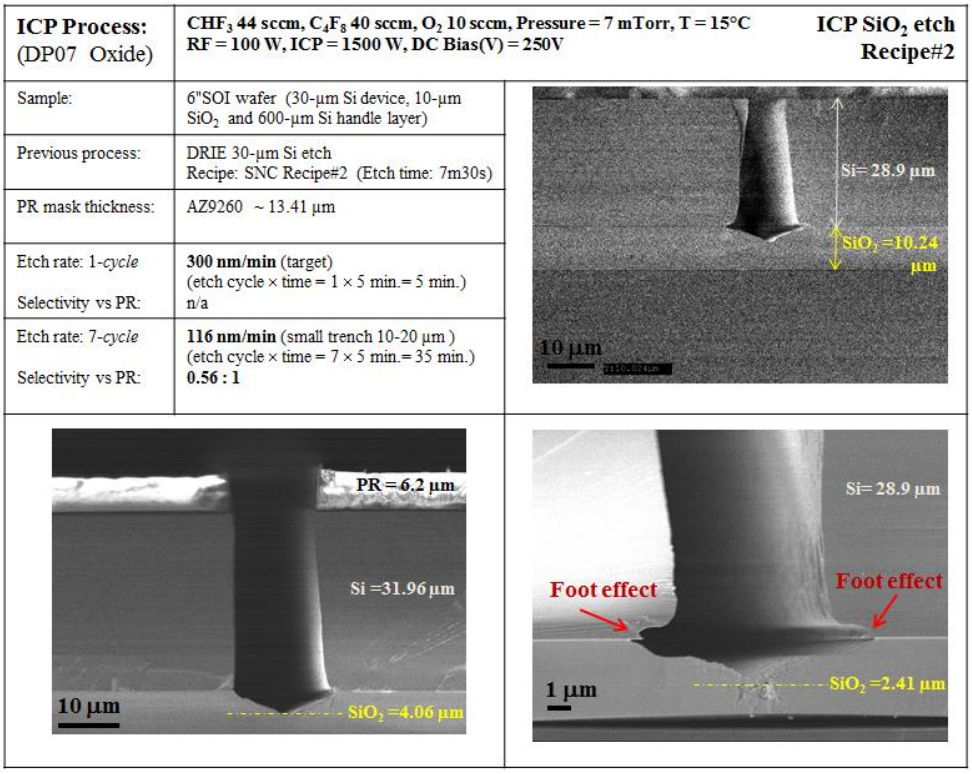


Figure 5.18 – Cross-section SEM images of the 10 µm-thick buried oxide etched using ICP process - Recipe #2 with a mixture of gases $CHF_3/C_4F_8/O_2$ = 44/40/10 sccm, RF/ICP power = 150/1400 W, pressure = 7 mTorr, and temperature = 15 °C. The vertical etch depth is 2.5-5.0 µm. Total etch time is 35 minutes. Forming of C-F polymers at the sidewalls and the bottom of trenches inhibits etching.

To obtain vertical sidewalls and homogeneous oxide etch, the DRIE process optimization was revisited. The angle of the sidewalls was improved as shown in the DRIE Si etch Recipe: UCL#1 obtaining a better control of a 90-degree sidewall (see Figure 5.10). The experiment was carried out at chip level. The small sample was glued with vacuum oil to a silicon carrier. The use of vacuum oil provides an effective heat transfer from the sample to the cooling electrode platen using a helium gas flow to prevent resist from burning. Several trial runs were undertaken by varying three main parameters - O_2, RF, and ICP power. This optimised recipe was used to improve the etch rate, profile and minimal polymer re-deposition. The increase of the etch rate was significant; about twice compared to the previous recipe. The selectivity was improved from 0.6:1 to 1:1 ratio. In Figure 5.19, the shape of the etched trench was clear and completely removed the 5 μm-thick oxide layer for both small features ($<$ 20 μm) and large features ($>$ 200 μm). However, this process induced a small amount of photoresist mask erosion including the Si layer at the small trench, resulting in a positively-sloped sidewall (opening). The sidewall angles of etched feature size of more than 200 μm were observed to be near 90 degrees. A significant reduction in polymer re-deposition at the etched regions as seen in Figure 5.20(c, d) was achieved using this optimised process (Recipe#3).

Table 5.8 provides the process parameters and etch results of ICP oxide etch recipes developed on SOI substrates. The optimised ICP oxide etching process of $CHF_3/C_4F_8/O_2$ gas mixtures (Recipe#3) offers the most suitable etching conditions for a thick buried oxide layer up to 10 μm. The etch rate varies between 250 nm/min to 280 nm/min from the smallest trench of 5 μm (the electrode gaps at the Y-shaped junction) and the largest trench of 400 μm (the large opening trench at the peripheral trap). The issue of heavy polymer formation found in previous processes (Recipes #1 and #2) is significantly reduced by a 5% increase in oxygen flow while the selectivity of oxide to photoresist (oxide:PR) is retained at 1:1. The vertical sidewall profile is improved to 87 ± 2 degrees

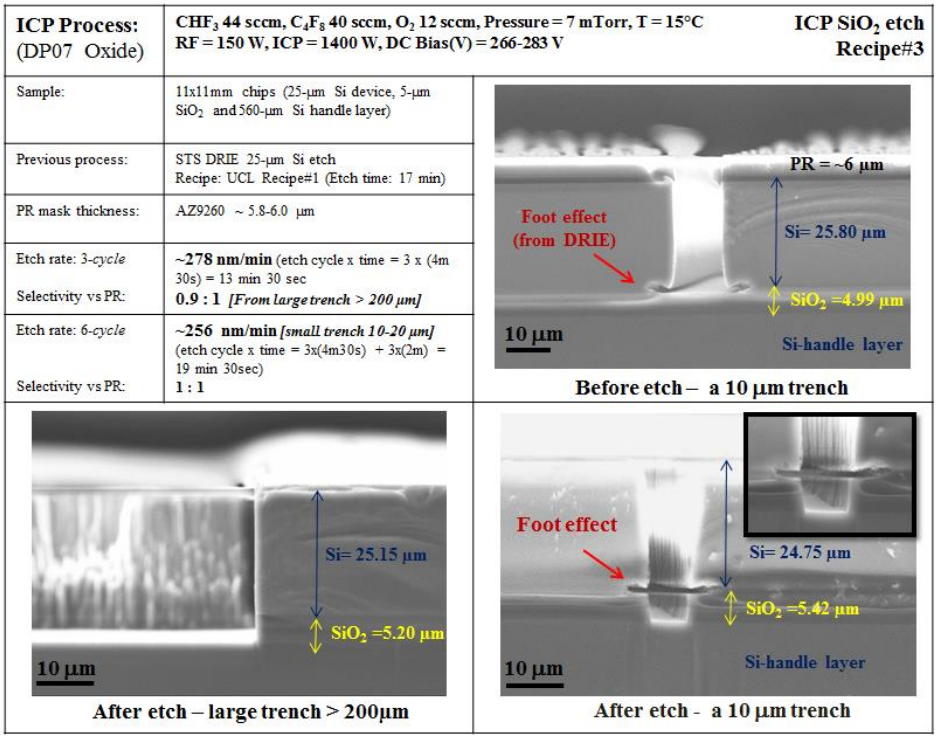


Figure 5.19 – Cross-section SEM images of a 5 µm-thick buried oxide etched away using ICP process - Recipe #3 with a mixture of gases $CHF_3/C_4F_8/O_2$ = 44/40/12 sccm flow rate, RF/ICP power = 150/1400 W, pressure = 7 mTorr, 15 °C. Total etch time is 19 minutes 30 seconds.

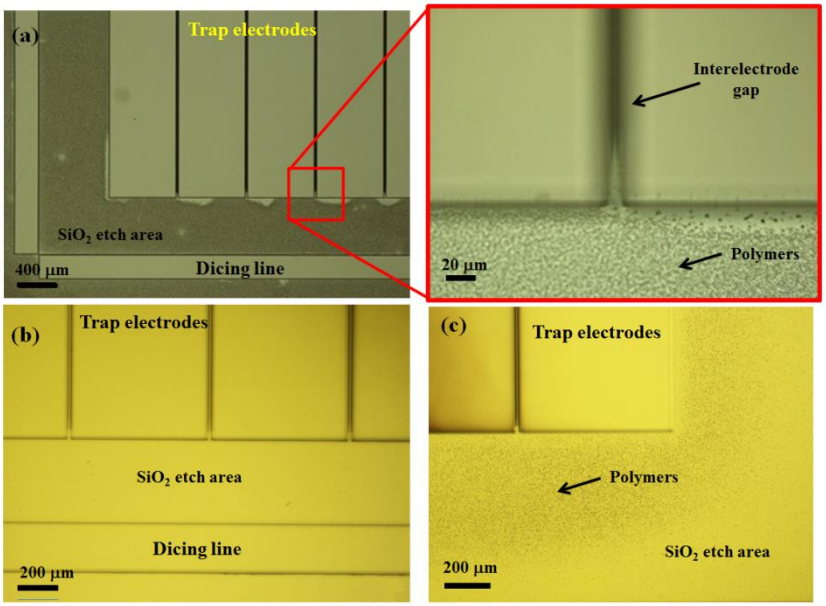


Figure 5.20 – Optical microscope images of ICP oxide etch result with polymers build-up. (a and inset) Recipe#2 with a large amount of polymer. (b-c) Recipe#3 with a reduction of polymer..

Table 5.8 - ICP oxide etching recipes suitable for a thick buried oxide layer (up to 10 μm) of SOI substrates.

ICP Process	Etcher[7]	CHF_3 Flow rate	C_4F_8 Flow rate	O_2 Flow rate	RF Power	ICP Power	Pressure	Temperature	Etch rate	Selectivity to PR	Side-wall angle θ
Recipe	#	sccm	sccm	sccm	W	W	mTorr	°C	nm/min	-	(°)
#1	1	-	40	8	200	1400	10	20	187	-	77±2
#2	2	44	40	10	100	1500	7	15	116	0.6:1	-
#3	2	44	40	12	150	1500	7	15	256	1:1	87±2

5.5 Conclusion

The fabrication of two prototype SEIT devices - (i) a Y-junction trap and (ii) a two-dimensional (2D) hexagon lattice trap - was developed at the Southampton Nanofabrication centre (SNC). The optimised fabrication process flows utilised a single-photomask-level process together with electrode pattering, etching and metallisation to form the trap structures. The devices were fabricated on SOI substrates with choices of the buried oxide layer of 5 μm-thick (Si-SiO_2 bonding) and 10 μm-thick (SiO_2-SiO_2 bonding). Also, the trap electrodes were metallised with two different metals (e.g. gold and aluminium) to investigate the effects of surface material on microtrap performance.

First, the SOI substrate was coated with AZ9260 positive photoresist and patterned using photolithography. The exposed silicon areas were etched away using the deep reactive ion etching (DRIE) process, followed by etching of the buried oxide layer; this could be either

[7] Etcher#1 is for a metal contamination process and CHF_3 gas is not supplied. Etcher#2 is for a non-metal contamination process.

a wet or dry process. At this step, the trap electrodes were completely transferred on to the SOI substrate. The patterned electrodes on the SOI substrate were then coated with two choices of metals – i) Cr/Au (50/500 nm), and ii) Al (500 nm) – using the e-beam evaporation. To complete the fabrication, the back-side of the trap (a Si handle layer) was also evaporated with thin layers of Cr/Au (25/250 nm) or Al (300 nm). Metal coating on the top and bottom Si surfaces is to make good electrical contacts and to reduce trap resistance. It also benefit for protecting any subsequent oxidation on bare Si known to be developed quickly in air after a few hours. The importance of the metal surface lies in the fact that surface-electrode ion traps can be particularly prone to charge build-up on exposed dielectric surfaces that perturbs trapped ions and degrades trap fidelity.

The key factors in determining a suitable oxide etching process for the proposed designs are the minimum feature size and the thickness of the buried oxide layer. In this work, the use of the SOI substrate with a 10-μm thick buried oxide limited the achievable fabrication process of a Y-junction trap to the ICP process. Otherwise, for SOI substrates with a 5 μm-thick buried oxide, both trap structures can be fabricated using the optimised process flows either wet or dry oxide etching. However, thick oxide etching with the 7:1 buffered HF solution was only suitable for a 2D hexagonal lattice trap but not for a Y-junction trap due to a completed undercutting (and lifting off) of small electrode geometries. To alleviate this issue, an alternative process flow was developed to replace a chemical wet etch process with an anisotropic dry plasma etch using an inductively coupled plasma (ICP). Additionally, a selective undercut (for a dielectric shield) was produced using a buffered HF oxide etch with low concentration (e.g. 20:1 BHF) allowing for a better control etch profile and undercut after the thick oxide layer was etched away using ICP process. A list of the fabrication process flows and recipes used to fabricate both surface-electrode trap geometries made of different electrode materials and oxide thicknesses is provided in the following table.

Trap designs	Trap CD (μm)	Trench width		Oxide thickness (μm)	Process Flow	Metal	Si etch DRIE	Oxide etch process	
		Min (μm)	Max. (μm)					BHF	ICP
Y-junction trap	9.5	5.0	400	5	C	Al	UCL#1	-	Recipe#3
				10	C	Au	SNC#2	-	Recipe#3
2D lattice trap	20	10	270	5	B/C	Au, Al	UCL#1	7:1 BHF	Recipe#3
				10	B	Au	SNC#2	7:1 BHF	-

The fabrication challenges encountered in removing a thick buried oxide layer of a SOI substrate were highlighted and solutions for improvement were also outlined. In particular, a deep V-shaped undercut (~ 60-70 μm wide) obtained from a buffered HF oxide etch, thought to be a result of fast etching rate at a weak bonding interface of two buried oxide layers. The impact of this particular undercut profile on flashover characteristics of the SOI-built trap devices is investigated in the subsequent experiments. However, the complete removal of the exposed oxide areas at the trench bottom between trap electrodes and the resulting undercut offer the added benefit for a more effective shield of exposed dielectric surfaces near the trapping regions, resulting in the minimization of decoherence for ion trapping.

Chapter 6

Ion-trap experiments with ytterbium ions

This chapter presents the first demonstration of ytterbium ($^{174}Yb^{+}$) ion trapping in the fabricated two-dimensional (2D) hexagonal lattice trap chips or the "*microtrap chips*" from the work described in Chapter 5. The design and construction of the ion-trap experimental apparatus including the vacuum system, the optical system, trap electronics and control system were all contributed to several members from the Ion Quantum Technology (IQT) group at the University of Sussex. The experiments discussed in this chapter were mainly conducted by former PhD students – primarily Robin Sterling, with assistance from Seb Weidt, Kimberley Lake and Simon Webster. The main components used for ytterbium ion trapping in an ultra-high vacuum system are described. More specific details of the experiment setup including ion sources, the vacuum system, optical layout, trap packaging and wiring, shielding, atomic ovens, pumps, radio frequency (RF) and DC sources are described in the doctoral works of Nizamani [182], Sterling [135], Hughes [183] and Lekitsch [184]. The experiment results based on the published work in Sterling et al. [172] demonstrate the fundamental operations of ytterbium ion trapping and rudimentary shuttling in the 2D hexagonal lattice trap. In addition, the electrical characterisation of surface flashover in a vacuum is described. The deterministic introduction of defects in to the 2D ion lattice is also presented.

6.1 Ytterbium ion trapping

Trapped ions in radio frequency (RF) Paul traps have long been recognised as a promising physical implementation of quantum bits (qubits) for quantum computing (QC) and quantum information processing (QIP). This is due to long ion lifetimes (single ions can remain trapped for several hours or days) and long coherence times (ranging from milliseconds to seconds), compared to the time taken in quantum operations (e.g. logical gate operation times typically in the order of microseconds). Furthermore, strong Coulomb interaction between neighbouring ions can be used to realize quantum logic gates, entanglements, spin-spin coupling between qubits in a 1D ion chain, a 2D or 3D ion lattice. In ion-trap quantum experiments, there are two methods to create a qubit using electronics states of an ion: 1) two ground state hyperfine levels with non-zero nuclear spin ("*hyperfine qubits*"), and 2) the optical transitions of a ground state to a metastable excited state ("*optical qubits*").

Hyperfine qubits can be derived from two hyperfine sub-levels of the electronic ground state, separated by a microwave frequency. To manipulate individual hyperfine qubits coherently, both microwaves and two-photon Raman transitions can be used to resonantly couple the hyperfine splitting of the relevant energy levels [185]. Choices of atomic species employing an odd number of isotopes and an odd spin such as $^{9}Be^{+}$, $^{25}Mg^{+}$, $^{43}Ca^{+}$, $^{87}Sr^{+}$, $^{137}Ba^{+}$, $^{111}Cd^{+}$, $^{171}Yb^{+}$ and $^{199}Hg^{+}$ possess a hyperfine structure which can be used to form hyperfine qubits [97], [123], [186]–[194]. Isotopes with hyperfine structure offer two significant advantages of the magnetic field insensitivity to first-order, and large hyperfine splitting (typically in radio-to-microwave frequency ranges) allowing for efficient detection between the two qubit states. Although hyperfine structures make the use of laser cooling more complicated, they are desirable and advantageous for efficient quantum gate operations due to their robust and long-lived internal states. For example, very long coherence times exceeding 10 minutes have been observed for superposition states of qubits based on laser-cooled $^{171}Yb^{+}$ ions in a linear Paul trap [195] and $^{9}Be^{+}$ ions in a Penning ion trap [196].

Alternatively, optical qubits can be derived from a ground electronics state and a metastable excited state separated by an optical frequency. Several ion candidates with an even isotope (which have zero nuclear spin) such as $^{24}Mg^{+}$, $^{40}Ca^{+}$, $^{88}Sr^{+}$, $^{138}Ba^{+}$, $^{172}Yb^{+}$,

$^{174}Yb^{+}$ and $^{198}Hg^{+}$ have been used for manipulating optical qubits [96], [197]–[203]. Coherence times of optical qubits are limited by the natural decay time from the excited state to the ground state, which is normally in the order of one second, which far exceeds the experimentally achieved gate times [204]. Lack of a hyperfine structure makes its level structure relatively simplified and potentially less complex in optical transitions used for the laser cooling process. Nevertheless, the optical qubits are more sensitive to magnetic field noise and laser phase fluctuations which are the dominant sources of decoherence.

The qubits stored in internal atomic energy levels of the ions have been widely investigated in various different atomic species [97], [123], [186]–[194], [96], [197]–[203]. Of various candidates of atomic species for ion-trap qubits, ytterbium (Yb) offers several attractive features. It has the ground state transitions in both its neutral atom and singly ionised forms. All optical transitions are accessible by commercially available diode lasers. This is beneficial as it does not require custom optics which is normally a more expensive solution. Additionally, selective loading of ytterbium isotopes can be achieved by using photoionisation lasers [205], [206]. Naturally occurring ytterbium is composed of seven stable isotopes, ^{168}Yb, ^{170}Yb, ^{171}Yb, ^{172}Yb, ^{173}Yb, ^{174}Yb, and ^{176}Yb. $^{171}Yb^{+}$ is a stable isotope of ytterbium with ~ 14% natural abundance and a spin half nucleus that allows for potentially less complex and more efficient preparation and detection of the hyperfine ground state levels which can be used for qubit operations (see Table 6.1). Alternatively, the abundant ^{174}Yb isotope being the most abundant (~ 32% natural abundance) possesses a simple level structure (a hydrogen-like atom, with no nuclear spin) allowing for precise control over the ions' state. Due to its simple ionisation, Doppler cooling and the fact that it is the most naturally abundant, $^{174}Yb^{+}$ is an ideal isotope of choice for the first experimental evaluation of a microfabricated 2D lattice trap described in this chapter.

Table 6.1 - Relative abundance of ytterbium isotopes. (Table from refs. [182], [207].)

Isotope	Mass (a.m.u)	Isotope abundance (%)	Nuclear spin	Hyperfine Splitting (GHz)
^{168}Yb	167.933894	0.13	0	
^{170}Yb	169.934759	3.04	0	
^{171}Yb	170.936323	14.28	1/2	12.64
^{172}Yb	171.936378	21.83	0	
^{173}Yb	172.938208	16.13	5/2	10.49
^{174}Yb	173.938859	31.83	0	
^{176}Yb	175.942564	12.76	0	

6.2 Experimental setup

6.2.1 Ion source (atomic oven)

Prior to performing ion-trapping experiments, ion source and loading steps are required. Ion traps are commonly loaded by photoionising a flux of neutral atoms typically sourced by an "*atomic oven*". An atomic oven used in this work consists of a resistively heated metallic tube (20 mm long and 1.5 mm in diameter) which was crimped on one end and welded shut with a constantan foil. The tube was filled with natural ytterbium wire (Part number: GO019 from Goodfellow Cambridge). Applying an electric current of 5-7 A for several minutes through the constantan foil and copper wire, the oven was sufficiently heated up to ~ 400 °C and started outgassing natural Yb atoms. At this point, the evaporated atoms left the oven and travelled to the trapping region where the atoms can be ionised.

For ion trapping in asymmetric traps of which all electrodes lie in a single plane, a flux of natural atoms can be efficiently loaded via backside loading [71], [73], [87], [88] to avoid natural atom flux contaminating the trap surface or coating of notches between electrodes leading to risk of short circuiting electrodes. In the absence of a backside loading hole in

the 2D lattice trap design, the atomic flux with sufficient atoms was able to be injected parallel to the surface (front-side loading) due to the low atomic flux required for the photoionisation process.

6.2.2 Photoionisation

There are two primary methods that can be used to produce ion source for loading ion traps; these are electron-impact ionisation [208] and photoionisation [209]. The electron-impact ionisation using an electron gun, the most common method used in mass spectrometry, is carried out by bombarding a gaseous sample with a stream of high-energy electrons. Normally, an electron gun (a heated tungsten wire), which generates the primary electron beam, can produce vast quantities of electrons resulting in an excess build-up of stray ionisation and charges nearby trap electrodes, surrounding structures and chamber walls. These make the process of electron impact ionisation less efficient for precise ion trapping experiments. To avoid uncontrolled charge build-up, the photoionisation (PI) technique is more efficient and causes less of a disturbance compared to electron bombardment. In recent times, it has been widely used in ion trap experiments [77], [81], [86]–[88], [92], [121], [209], [210]. The generation of ions by photoionisation employs a physical process in which an ion is formed from the interaction of a photon with an atom or molecules. This technique provides a significant advantage of the isotope-selective ion-trap loading of neutral atoms based on resonance of the incident light [211]–[213].

Ytterbium ions can be loaded into the trap using a two-photon ionisation method first demonstrated by Kjaergaard et al. [211]. The two-photon ionisation scheme for neutral Yb atoms which is similar for all isotopes is illustrated in Figure 6.1. The neutral Yb atoms is excited from its ground state S to its P state by a light of wavelength near 398.91 nm and then ionised by any light with wavelength less than 394 nm to reach the continuum. For the first stage of photoionisation process carried out in this experiment, the 399 nm light was used to excite a neutral Yb atom from the $^1S_0 \rightarrow ^1P_1$ transition. Then the second photon of the light wavelength near 369 nm was used to ionise it directly from $^1P_1$ state into the continuum and to cool the trapped Yb^+ ion immediately after the ionisation through excitation from

$^2S_{1/2} \rightarrow ^2P_{1/2}$ transition (see more detail in Section 6.2.3). In particular, ^{174}Yb ions were loaded into the trap using the detuning of the ionisation laser frequency given in Table 6.2 showing the accurate value of the transition wavelengths required for isotope-selective photoionisation corresponding to the experimental setup at the optics laboratory at the University of Sussex [135], [182].

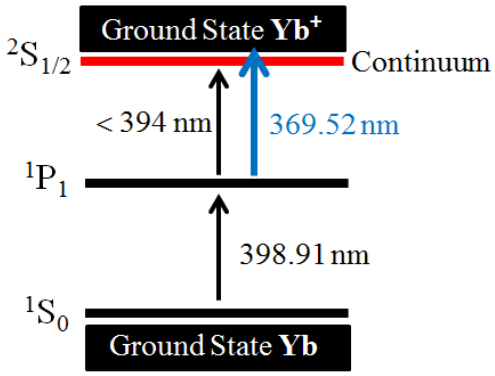


Figure 6.1 – The relevant energy level scheme of neutral ytterbium identifying the state transitions involved in the two-photon (also called the two-colour) photoionisation process. A 399-nm light is used to excite the atom from the ground state to the excited state followed by any light with wavelength less than 394 nm to excite an electron to pass the continuum (Figure modified from ref. [214]).

Table 6.2 - The transition wavelengths required for isotope-selective photoionisation of neutral Yb atoms and Doppler cooling of ytterbium ions the experimental setup at the optics laboratory at the University of Sussex. (Table from refs. [135], [182].)

Isotope	$^1S_0 \leftrightarrow {}^1P_1$ transition wavelength (nm)	$^2S_{1/2} \leftrightarrow {}^2P_{1/2}$ transition wavelength (nm)	$2D_{3/2} \leftrightarrow {}^3D[3/2]_{1/2}$ transition wavelength (nm)
$^{170}Yb^+$	398.91051(6)	369.52364(6)	935.19751(19)
$^{171}Yb^+$	398.91070(6)	369.52604(6)	935.18768(19)
$^{172}Yb^+$	398.91083(6)	369.52435(6)	935.18736(19)
$^{174}Yb^+$	398.91114(6)	369.52494(6)	935.17976(19)
$^{176}Yb^+$	398.91144(6)	369.52550(6)	935.172252(19)

6.2.3 Doppler cooling

Once neutral Yb atoms have been successfully ionised, it is necessary to cool the Yb^+ ions to the ground motional state using Doppler cooling. To efficiently Doppler-cool $^{174}Yb^+$ ions, three different lasers at 369 nm, 935 nm and 638 nm were used to drive the cooling cycle. All of the transition wavelengths between 369 nm and 935 nm can be achieved with commercially available laser diodes. The Doppler-cooling steps of $^{174}Yb^+$ described in Olmschenk [214] are outlined below. The relevant energy level diagram of $^{174}Yb^+$ ion Doppler cooling is also shown in Figure 6.2.

1) The main Doppler cooling proceeds with the $^2S_{1/2} \rightarrow {}^2P_{1/2}$ electric dipole transition driven by a 369.5 nm laser. The $^2P_{1/2}$ excited state spontaneously decays with a lifetime of 8.12 ns and returns to $^2S_{1/2}$ ground state.

2) With a spontaneous emission-branching ratio of 0.5% probability, however, the ion can decay from the $^2P_{1/2}$ into the metastable $^2D_{3/2}$ state which is relatively long-lived with a lifetime of ~ 53 ms. Once a trapped ion falls into the $^2D_{3/2}$ state, it will no longer scatter photons and be cooled by the 369 nm laser. An additional laser is required at 935.2 nm to excite the ion $^2D_{3/2} \rightarrow {}^3D[3/2]_{1/2}$ state where it rapidly decays back to $^2S_{1/2}$ ground state (with 98% probability).

3) Occasionally, the ions can be transferred from $^2D_{3/2}$ into the extremely long-lived $^2F_{7/2}$ state (with an estimated lifetime of ~ 6 years) where it would go dark and remain trapped until eventually lost. This is usually caused by collisions with background gases. To avoid the ion loss by the decay to the metastable state $^2F_{7/2}$, an additional laser at 638 nm is used to depopulate the $^2F_{7/2}$ state via the $^2F_{7/2} \rightarrow {}^1D[5/2]_{5/2}$ transition from which the ion decays back to the $^2D_{3/2}$ state.

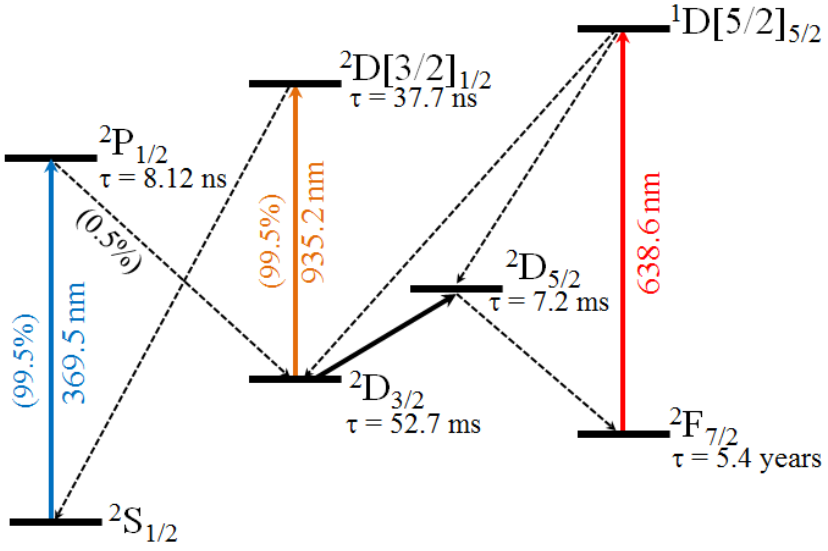


Figure 6.2 – The relevant energy level scheme of $^{174}Yb^+$ ions associated with Doppler cooling with the lifetime and the transition probability of the relevant states. The driven transitions are shown in solid lines with corresponding transition wavelengths. The decays by collisions with background gases during the cooling process are shown in dashed lines. (Figure modified from ref. [214])

6.2.4 Laser system

For the photoionisation and Doppler cooling process of $^{174}Yb^+$ ions, 399-nm, 935-nm and 638-mm coherent light sources were generated using a home built external cavity diode laser (ECDL) setup. Adopting a different approach, the main Doppler cooling laser with 369 nm was generated by a frequency doubling system purchased from Toptica. Mode detailed descriptions of the laser setup procedures can be found from Nizamani's thesis [182] and Hughes's thesis [183].

6.2.5 Vacuum system

In an attempt to perform precise quantum operations within minimal decoherence, ion trap devices require to be operated in a system which is well-isolated from environmental perturbations. To limit the collisions between trapped ions and the background gas destroying the quantum state of the qubit or causing ion loss, an ultra-high vacuum (UHV) system at a pressure in the order of ~ 10^{-12} Torr is required for ion-trap experiments. At UHV range,

the mean free path of particles increase up to > 10^5 km resulting in a significant reduction of collision rate inside the vacuum chamber. Therefore the ions can remain trapped for longer period of time, from a few hours to several days.

The construction of an UHV chamber for ion-trap experiments is primarily based on two key requirements to achieve a pressure of 10^{-12} Torr and to provide laser access along different axes for trapped ions in different types of trap geometries. The vacuum chamber used in the Sussex lab consists of the Magdebug hemisphere and the spherical octagon (P/N: MCF450-MH10204/8-A and MCF450-S020008-C from Kimball Physics). The design allows optical access for both symmetric and asymmetric (or surface-electrode trap) ion traps. Atomic ovens producing a natural Yb beam are mounted within the hemisphere. When operating a surface-electrode trap, the atomic ovens were mounted onto the chip rail to produce a natural Yb beam ejected parallel to the trap surface (see Figure 6.9). The picture of a complete vacuum system is shown in Figure 6.3. A complete assembly shows a hemisphere and octagon arrangement, a residual gas analyser (RGA) for leak testing of the vacuum, an ion pump, a titanium sublimation pump (TSP) and electrical connectors (atomic oven, RF and 100-pin feedthroughs). A complete design and construction of a vacuum system is described in more detail by Nizamani [182] and Sterling [135] for the first- and second-generation vacuum systems respectively.

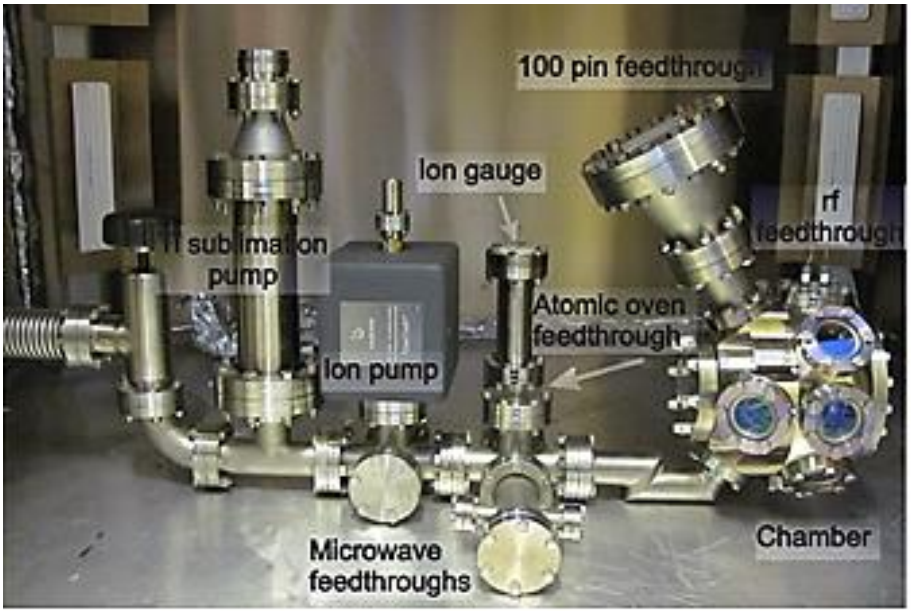


Figure 6.3 – Photograph of the complete vacuum system for ion trapping experiments conducted in the Sussex optics laboratory. (Figure from ref. [183].)

6.2.6 Trap electronics

- **Micro-trap chip packaging**

The fabricated 2D lattice traps were mounted on a commercial 101-pin ceramic pin grid array (CPGA) chip carrier (P/N PGA10047002, Global Chip Materials) using UHV conductive glue. The backside of the trap, which is a handle Si layer coated with a Au/Cr layer, was glued onto a stainless steel block connected to a ground pad of the chip carrier. Raising the surface of the trap above the CPGA allows better optical access for lasers. Wire bonding with 30 μm diameter gold wires was used to interconnect all six compensation electrodes and a RF electrode to the CPGA pads. Each electrode was bonded with multiple gold wires to allow large current-carrying levels in the order of 1 ampere.

- **RF power source**

A high RF power supply, typically > 100 V, with appropriately low noise levels is needed for ion-trapping experiments. The use of a RF resonator is to impedance match between a RF

source and its load (impedance of an ion trap), and so avoiding any dangerous reflections. Another advantage of using a resonator is the ability to provide a frequency source with a narrow bandpass, defined by the quality factor (Q) of the resonator connected to an ion trap. A helical resonator was constructed with an adjustable coupling antenna and a copper coil inside a grounded copper tube. The RF voltage was generated by a commercial function generator (P/N: HP 8640B, Hewlett Packard) and amplified using a high power RF amplifier (P/N: NP-541, MiniCircuits, max output 30W). This RF source (output) impedance of 50 **Ω** was matched to the impedance of the ion trap by adjusting the mutual inductance between an antenna and the copper coil. The quality factor (Q) of the resonator and resonant frequency f_0 is derived as,

$$Q = \frac{1}{2\pi f_0 RC}, \qquad f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{6.1}$$

where R, L and C are the resistance, inductance and capacitance of the ion-trap resonator circuit as shown in the equivalent circuit diagram in Figure 6.4. The design and construction of the helical resonator were undertaken by James Siverns. The operation of resonators with ion traps was also explained in more detail in Siverns et al. [215].

As seen in Equation 6-1, the Q-factor is inversely proportional to the load capacitance and resistance. The additional capacitance and resistance will reduce the Q factor. It is important to minimize the capacitances and resistances of the ion trap (described in more detail in the design and fabrication chapter), wiring and feedthrough to obtain high Q values. With a measured capacitance of a 2D lattice trap (~ 19 pF), the helical resonator used in the basic ion-trapping experiments possessed the Q-factor of 160 with a resonant frequency of 32 MHz In the surface flashover measurement on the SOI test chips, a loaded Q-factor of the helical resonator and the resonant frequency were calculated to be approximately Q = 210 and f_0 = 28 MHz, respectively.

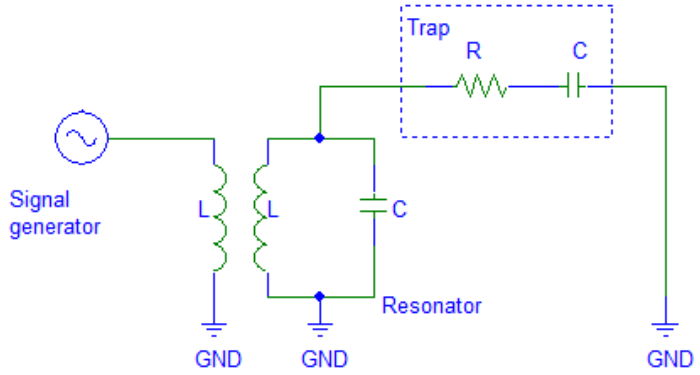


Figure 6.4 – Equivalent circuit diagram of a helical resonator connected to the RF source and its load (an ion trap).

- **DC voltage supply**

The DC voltages applied to the compensation electrodes were obtained directly from an analog card providing 8-output voltage channels with a nominal range of ±10 V. The control of electrode voltages employed a LabView™ programming. During ion-trapping operations, the voltage fluctuations mostly due to RF pick up on neighbouring DC electrodes may lead to changes in the radial secular frequencies ($\omega_{x,y}$) and the displacement of the ion positions. To locally suppress RF noise on DC electrodes, each compensation electrode was connected to the RF ground through 820 pF capacitors soldered directly on to the CPGA.

6.3 Experimental results

6.3.1 Trap electrical breakdown in vacuum

Electrical breakdown in vacuum via a connecting surface (over the surface of the dielectric material between two electrodes) known as “surface flashover” is expected to be a dominant breakdown in microfabricated ion traps as discussed in Sterling et al. [216]. In general the withstand voltage of a solid insulator in vacuum is less than that of a vacuum gap of similar dimensions and bulk breakdown. The surface flashover characteristics of

an insulator are in relation to the electric field concentrations and surface charging. Surface flashover of insulators, primarily in vacuum, is generally initiated by the emission of electrons from "*triple point*", defined as the junction of metal, insulator and vacuum. The electron emission from cathode triple-junction occurs and accumulates on the insulator surface as shown in Figure 6.5. The triple point has been considered as the source where the first electrons are produced. These first generation electrons, once produced, may lead to rapid multiplication, either through impact ionization of neutrals or through secondary electrode emission (SEE) if these electrons strike the insulator surface with a sufficiently high energy. There are several models proposed to explain surface flashover in vacuum [217]–[219]. One is the secondary electrode emission avalanche (SEEA) model which is believed to trigger off the surface flashover. However, the fundamental processes of SEEA have not yet to be fully understood because they are influenced by various factors of insulators, such as the surface condition, size, shape, material properties and surface charge distribution.

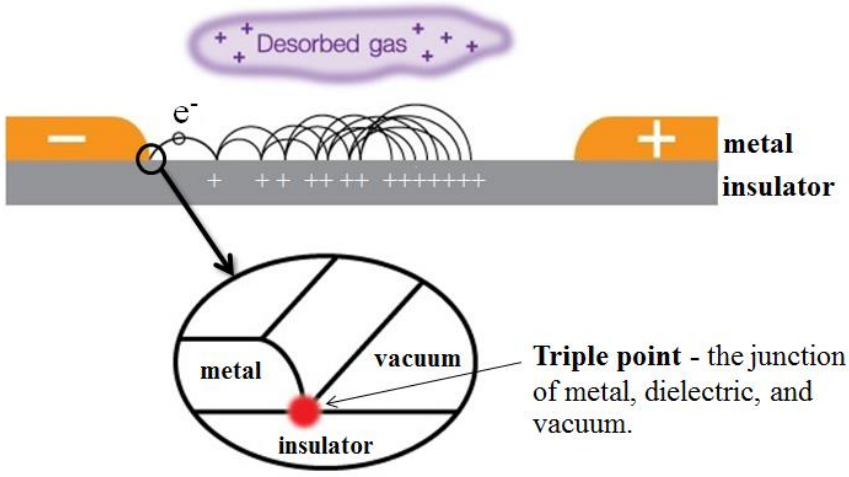


Figure 6.5 – Schematic illustrating secondary electron emission avalanche with the triple points, often initiation points for insulator flashover.

The mechanisms governing surface flashover of insulator in vacuum upon insulator geometries have been well documented by Miller [220], [221]. It was found that certain

insulator angles are more favourable to the initiation of flashover over others. The poorest insulator performance seems to come from an insulator with slightly negative angles. Some of the insulator geometries in Miller's study are shown in Figure 6.6. This result also correlated to the previous study by Lee et al. [222] with PMMA cones in vacuum which discovered that the cylinder shape of insulator has the lowest flashover voltage, with the +30° angle representing a 23% increase, and the 45° and 60° angle representing an increase of at least 67% in the flashover voltages. Later, Mazurek and Tyman [217] reported a relative increase in a flashover voltage in more complex shapes such as a ~ 25% increase for the corrugated cylinder. Various works with similar results as reviewed in Miller's work also show that the flashover voltage of an insulator geometry (cylinder) with a positive 45-degree angle is better than those of a negative 45-degree angle, and one with a slightly negative angle give generally the worst results [220], [221].

Taking into consideration the effect of insulator angle on surface flashover discussed above, types of etch profiles of insulators depending on the etching mechanisms could play an important role in flashover performance of the microfabricated structures. For instance, a typical isotropic etch profile similar to the concave cylinder shown in Figure 6.6 establishing a relatively small negative angle (< -20°) at both sides of the conductor-insulator interface may result in the reduction of the flashover voltage

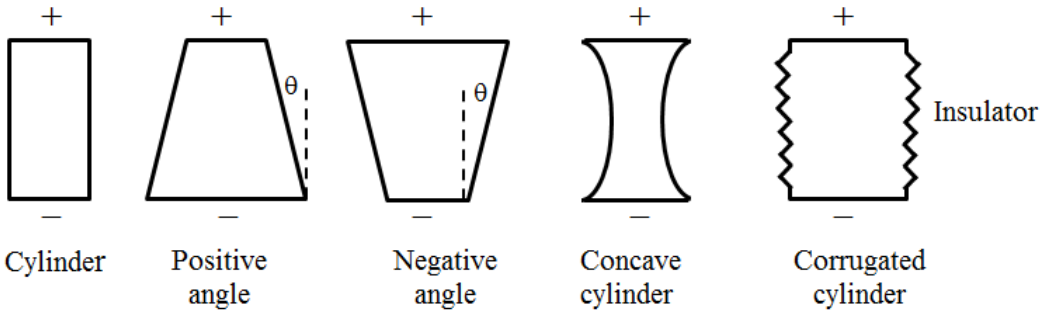


Figure 6.6 – Insulator surface geometries. (Figure modified from refs. [220], [221].)

The measurement of breakdown voltage was performed on the test samples consisting of a single square electrode (500×500 μm^2) fabricated on a SOI substrate with 10-μm thick buried oxide. The chip was glued to the CPGA chip carrier using UHV compatible conductive glue (P/N: A-H21D from LewVac) as shown in Figure 6.7(a). The sample was then placed in a vacuum chamber at a pressure of 6×10^{-4} Pa. A gold-coated silicon island was supplied by the RF voltage from the helical resonator allowing coupling between the amplifier and the chip with ≈ 90% of the power at a resonant frequency of 28 ± 0.5 MHz and a Q-factor of 210 ± 15 [172]. The exposed Si handle layer (the surrounding black region) was grounded as shown in Figure 6.7(b). The buried oxide is undercut beneath the gold-coated island and not visible in this picture. The RF voltage was slowly increased until breakdown occurred. The breakdown voltages were collected from four samples giving the average flashover voltage of 1061 ± 5 V by RF at frequency ~ 28 MHz and 1298 ± 32 V by DC [135]. The RF flashover voltage approximately 20% lower than those of the static DC flashover was observed. The mechanism of this reduction is not known but is likely to be a result of local heating in the substrate and outgassing of the surface when the RF voltage was applied. Likewise, the poorest flashover performance of an insulator caused by AC test voltages compared to other sources (e.g. negative impulse, DC, bipolar waveforms) has previously been reported [220], [221].

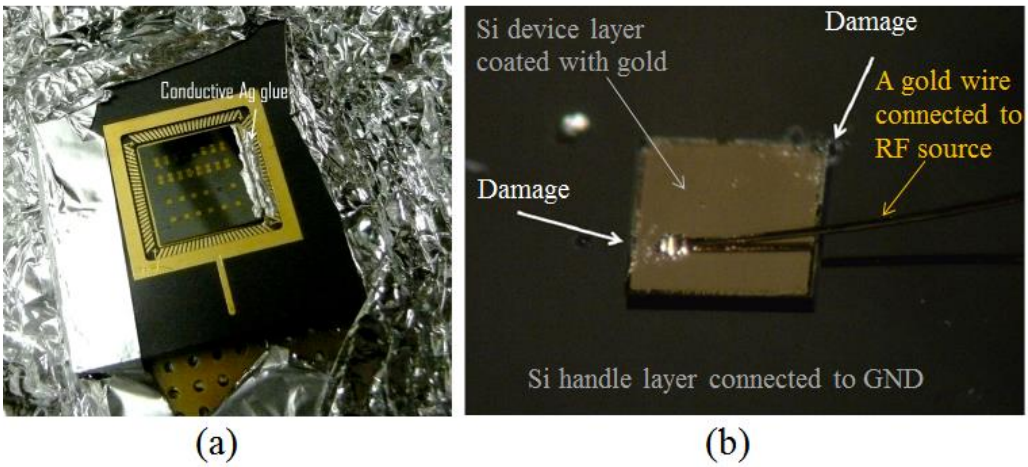


Figure 6.7 – A SOI-built test sample for breakdown measurement. (a) The test chip mounted with conductive silver glue on a CPGA chip carrier. (b) A single square structure after breakdown shows the damages on the gold around the top right corner and wire-bond area. (Figure from ref. [135].)

The breakdown mechanisms in the SOI-built ion-trap device are illustrated in Figure 6.8(a). From surface flashover breakdown test, an extremely high-breakdown voltage up to 1 kV was observed. Effect of insulator profiles is shown to greatly influence on the flashover performance. The fabricated devices exhibit the deep V-shaped undercut profile obtained from the buffered HF etching process (see Section 5.4.6 for graphical illustration and explanation). This undercut profile results in a significant increase of the surface flashover path length from ~ 10 μm to ~ 140 μm as shown in Figure 6.8(b), and so mitigating surface breakdown effects. This finding has a significant impact on the improvement of surface flashover performance to more than double the breakdown voltages that can be applied to other microscopic ion traps and microstructure devices.

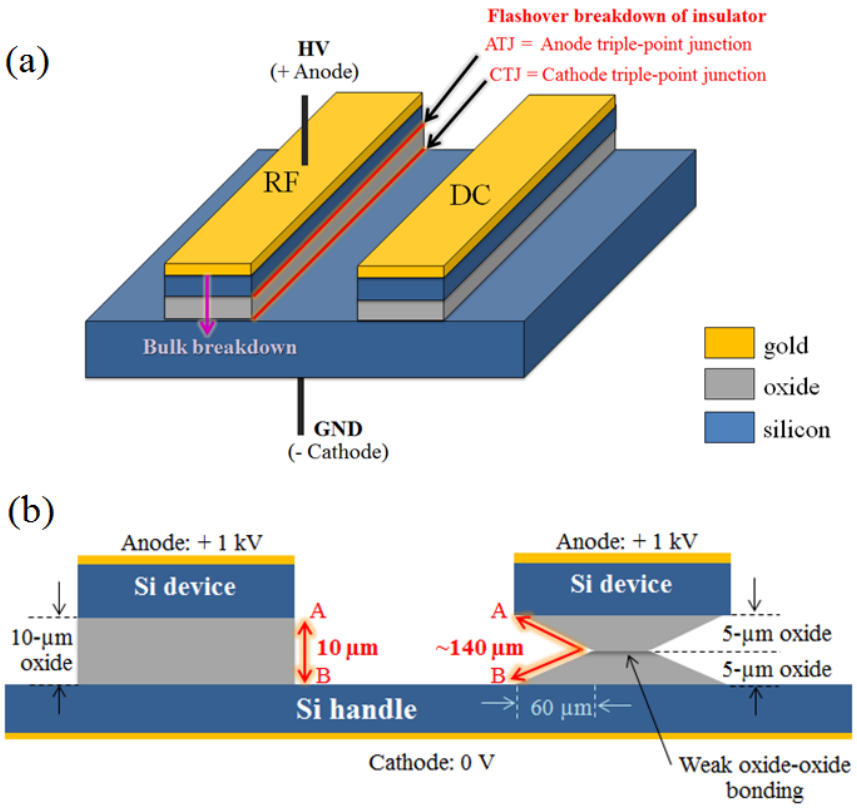


Figure 6.8 – Diagrams of breakdown mechanisms in the SOI-built ion-trap device. (a) The bulk and surface flashover breakdown. (b) Surface breakdown path (A-B) of insulators with different surface profiles.

6.3.2 Trap operations (trapping, shuttling, quantum experiments)

The microfabricated 2D hexagonal lattice trap on a chip was packaged and placed in the UHV chamber at a pressure of 8×10^{-8} Pa to perform several experiments. The photoionisation and Doppler cooling lasers were aligned for trapping conditions and light collection. Firstly, to demonstrate $^{174}Yb^{+}$ ion trapping in 2D lattices, ions were loaded to the trap region using ohmically-heated atomic ovens (see Section 6.2.1) to produce a neutral flux of ytterbium atoms travelling parallel to the trap surface shown in Figure 6.9. Atoms were then resonantly ionised using a two-photon photoionisation process with light at 399 and 369 nm (see Section 6.2.2).

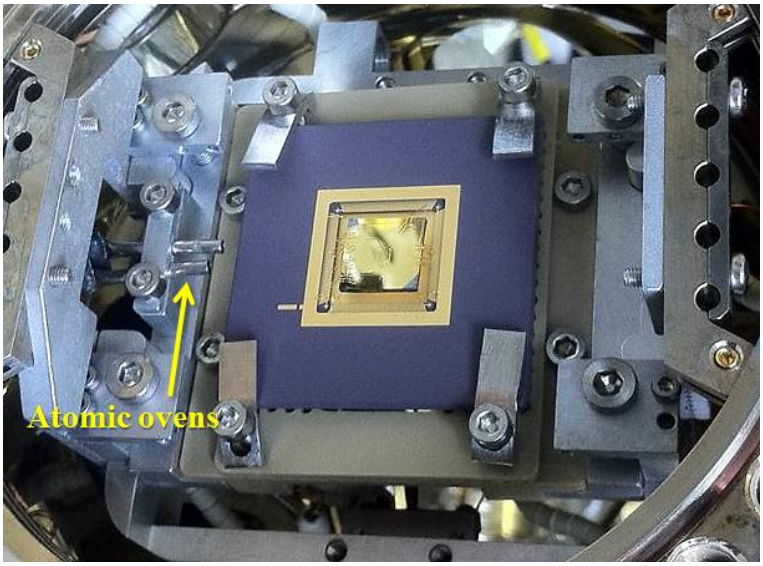


Figure 6.9 – A front-view image of the vacuum chamber shows the chip rail with mounted chip bracket hosting a mounted 2D hexagon trap on a CPGA chip carrier. Two atomic ovens serving as the front-loading ovens are attached on the chip rail. (Figure internally provided by Robin Sterling.)

A RF voltage of 455(3) V at frequency $\Omega/2\pi = 32.2$ MHz via a helical resonator with Q = 160 was applied to the RF electrode. All compensation electrodes were initially held at RF ground. Trapped ions were Doppler-cooled by the 369 nm light followed by the 935 nm light used to repump the ions from a long-lived D-state (see Section 6.2.3). The lifetime of

a laser-cooled ion was ~ 90 minutes which was likely limited due to collisions with background gas atoms and molecules. An ion lifetime of 5 minutes or greater was obtained without laser cooling. The electron multiplying charged coupled device (EMCCD) camera was used to detect trapped ions. With the viewable area limited by the imaging setup, a CCD image of six ions trapped simultaneously in a 2D ion lattice is shown in Figure 6.10(a). The secular frequencies along the three principal axes of the trap (radial and axial) can be measured using a technique often referred to as "*tickling*", by applying resonance excitations to the trapped ion using a small RF signal applied to nearby DC electrodes. In this experiment, one of the compensation electrodes near the ion was applied with a small RF voltage to excite the radial trap modes. The resonant frequency was swept until the ion secular frequencies were reached. At this stage, the secular motion was excited, and a decreasing of ion fluorescence was observed due to the Doppler shift of the ion. With the applied RF voltage and the DC electrodes held at ground, the ion secular frequencies along the three principal axes of the trap were measured as $\omega_x, \omega_y/2\pi = (1.58, 1.47) \pm 0.01$ MHz for the radial frequencies and $\omega_z/2\pi = 3.30 \pm 0.01$ MHz for the axial frequency. For known trap dimensions, the applied RF voltage and frequency, the trapping depth of the resulting secular frequencies was computed to be 0.42 eV using the electric field solver (bemsolver) and Mathematica analysis (refer Chapter 4).

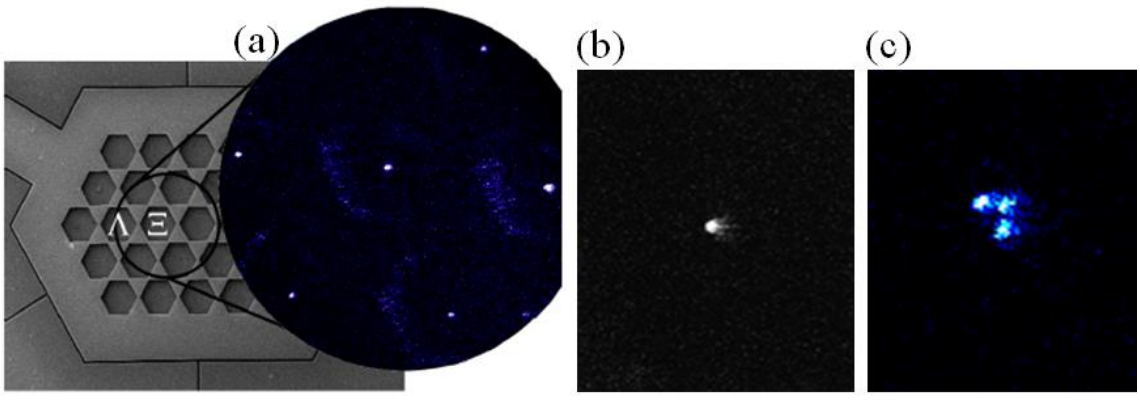


Figure 6.10 – CCD images of trapped $^{174}Yb^{+}$ ions in a 2D lattice trap. (a) An image of six ions trapped simultaneously in a 2D lattice with reduced background noise overlaying on a SEM image of the centre trap surface. (b) An image of a singly trapped ion. (c) An image of a three-ion Coulomb crystal in a single lattice site demonstrating its ability to deterministically introducing lattice defects into the ion lattice. (Figures internally provided by Robin Sterling.)

The ability to address individual ions was achieved by steering the 399-nm ionisation laser to address individual trapping sites, so that individual ions can be controllably trapped in each lattice site. Furthermore the ability to deterministically introduce defects into a uniform ion lattice - either a missing ion or the inclusion of an additional ion in each lattice site - was carried through in the same manner. Figure 6.10(b) shows an example of a single lattice site with such a defect, a three-ion Coulomb crystal. In addition, it was possible to perform individual ion shuttling within the 2D lattice sites by controlling the static and radio frequency (RF) voltages. For example, an ion was initially trapped at site Ξ as labelled in Figure 6.11(a). By lowering the RF voltage to minimise the potential barrier and supplying DC voltages to the DC electrodes to control the shuttling direction, the ion was shuttled to the adjacent lattice site Λ. The voltage sequence on the RF electrode and six compensation electrodes in Figure 6.11(b) was for a single ion shuttling from lattice site Ξ → Λ. To shuttle the ion back to site Ξ, the polarity of DC voltage on the Comp 3 and Comp 6 electrodes was reversed.

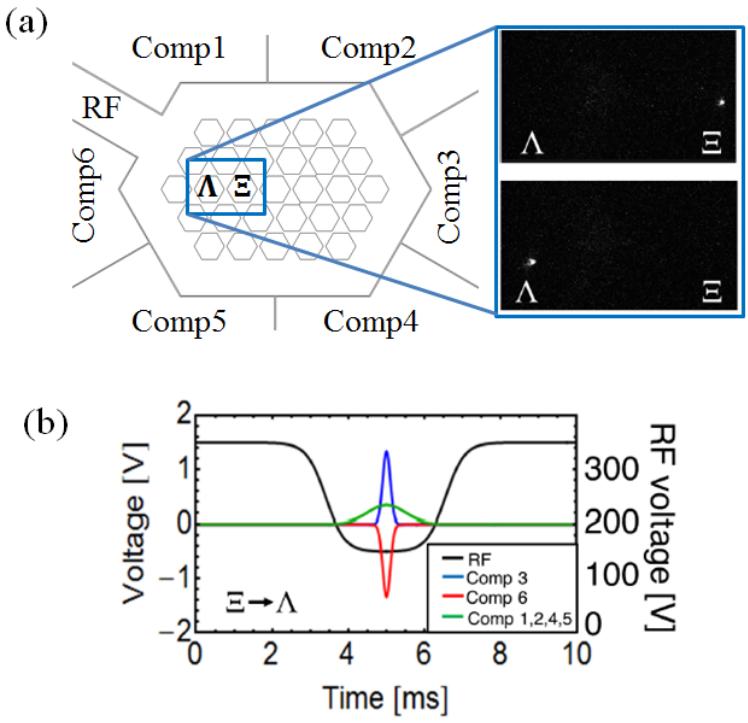


Figure 6.11 – Rudimentary ion shuttling in 2D lattice sites. (a) Trap electrode schematic and CCD images showing a single ion shuttling between two adjacent lattice sites, from Ξ to Λ. (b) The voltage sequence for ion shuttling from lattice site Ξ to Λ. (Figures internally provided by Robin Sterling.)

6.4 Conclusion

The first experimental demonstration of ytterbium ion ($^{174}Yb^{+}$) trapping in the microfabricated 2D hexagonal lattice trap was achieved. In this work, the 2D lattice trap was loaded with $^{174}Yb^{+}$ ions produced by ohmically heating a natural abundance ytterbium oven. The ytterbium atoms were ionised by a two-photon ionisation process, wherein the first laser (399 nm) excited the neutral atoms and the second laser (369 nm) completed the ionisation. Trapped ions were then Doppler cooled by the 369 nm light, followed by the 935 nm light to repump the ion from a long-lived D-state.

Ion trapping with a relatively long lifetime of a laser-cooled ion up to 90 minutes and ≤ 5 minutes without cooling in ultra-high vacuum system at a pressure of 8×10^{-8} Pa was demonstrated. Under the operating condition with RF voltage of 455(3) V at a frequency $\Omega/2\pi$ = 32.2 MHz, the measurements of the secular frequencies employing the control electrode tickle technique (resonance excitation) were reported with the radial frequencies of $\omega_x, \omega_y/2\pi$ = (1.58, 1.47) ± 0.01 MHz and the axial frequency of $\omega_z/2\pi = 3.30 \pm 0.01$ MHz. The ability to individually address trapped ions in the 2D ion lattice was attained. The deterministic introduction of defects into the ion lattice (e.g. the missing ions in the lattice or the inclusion of additional ions in an individual lattice site) which may be of interest in studies of Bose-Hubbard physics was performed. The rudimentary shuttling between neighbouring lattice sites was carried out through lowering the RF voltage amplitude to reduce the potential barrier and supplying the DC voltages to the compensation electrodes to control the shuttling direction.

In addition, the electrical characterisation of surface flashover in vacuum was conducted and demonstrated a significantly higher flashover voltage. Owing to the deep V-shape undercut of the buried oxide layer achievable with the developed fabrication process, such a deep lateral undercut substantially increases in the breakdown path of the insulator surface, thereby increasing the flashover voltage. The breakdown voltage of above 1k V in the SOI-built ion-trap devices could be very beneficial for ion trapping at much higher trap depths and applications where it is necessary to have a very high voltage. This finding has a significant impact on the improvement of the flashover performance to more than double the breakdown voltages that can also be applied to other microscopic ion-trap and microstructure devices.

Chapter 7

Microparticle trap experimental apparatus

This chapter describes the development of experimental apparatus for trap performance assessment of the microfabricated ion traps. In this work, the microparticle trapping and transporting mechanism was evaluated in an ambient environment instead of in a vacuum system due to lack of appropriate ion-trap laboratory facilities at the Nano Research Group. The experimental facility for performing experiments with trapped ions normally requires a special ultra-high vacuum (UHV or cryogenic UHV) construction including a vacuum chamber equipped with pumping, background gassing and bakeout systems, and other UHV-compatible interfaces for electrical signals and lasers needed during the experiment and for ion detection. Microparticle trapping in ambient air exhibits its own advantages as it is relatively less demand in construction equipment and set-up time compared to a vacuum system. This can reduce a turnaround time through the trap design optimisation. Furthermore, trapping microparticles only requires a drive frequency in a low-audio frequency range which is normally available in electronics laboratory equipment. For ion trapping, the radio frequency (RF) high voltage commonly supplied via a helical resonator and an amplifier filter is required to drive the trap. The design and construction of a helical resonator for a desired frequency and voltage needs to take several requirements into account such as maximising the quality factor (Q-factor), and impedance-matching between the RF source and the trap to minimise the background noise and the signal reflection from the load back to the source. This makes

the circuitry and interface design for ion trapping in a vacuum system more complex than those of microparticle trapping in air.

The following sections discuss the experimental apparatus (inexpensive, off-the-shelf laboratory instruments) capable of being easily configured to run all of the required experiments including microparticle trapping, 2D shuttling and levitation in a two-dimensional (2D) hexagonal lattice trap. The experimental apparatus is divided into two main parts: (i) trap drive electronics and experiment controls, and (ii) imaging system. The complete setup was built and used for the first time for realising microparticle trapping in the microfabricated 2D hexagonal lattice trap chips under ambient air environment.

7.1 Trap drive electronics and experiment controls

7.1.1 Trap electrical interconnect: die-to-package

In order to make interconnections between the trap electrodes to the chip carrier, the ultrasonic wire-bonding technique was used. To begin the wire-bonding process, the fabricated SEIT chips were attached on to a custom chip carrier (Myro PCB, 200-DIL24, Layer: 2, 32×23 mm, FR-4, pad finishes with immersion gold) using a silver colloid electro-conductive paint, Dotite D-550. The wire-bonding machine is a user-programmable wedge-wedge bonder, F&K Delvotec 5430 model. According to the standard setup in this wire bonder, the installed capillary was particularly fit for an aluminium ribbon of 25 μm in diameter which was also used in this work. The maximum current flow (DC) was tested on a 25 μm diameter, 10 mm-long aluminium wire capable of carrying a current flow up to 500 mA. The bonding recipe for a trap chip mounted on a chip carrier was created from the standard wire-bonding recipe. The bonding parameters were optimised based on the first bond, second bond, foot width and tail length associated with desired loops and bond positions. The high-quality of a wire bond requires a proper wedge shape and size design. The foot size of the wedge is commonly set to 1.5 to 2 times that of the wire size. The bond

foot size of ≈ 50 μm plus a tail length of > 150 μm at the first bond is shown in Figure 7.1(d). There are two basic types of bonding: forward and reverse. A forward wire bonding process placed the first bond on the die, followed by the second on the package bond pad. With this method, the RF electrode (~ 400 μm wide) was apparently narrow for the use of multiple wire bonded on a single pad which was needed to increase the current-carrying capacity, but which was not easy to accomplish in that limited bond pad area. Figure 7.1(d) shows a misaligned-bonded wire occasionally causing a short electrode. Also, reworking of missed bonds was a difficult process because stray wires could be trapped in the interelectrode gaps (isolation trenches) and cause short circuits. The solution was to use a reverse wire bonding process. With this process, the first bond was made on the package bond pad which has large pad size where extra tail can be accommodated and the second was made to the die (RF electrode) where no tail was left after the bond.

The microtrap chip mounted on a chip carrier socket during the wire-bonding process is shown in Figure 7.1(a). Next, a 12-way PCB header was then soldered to a chip carrier each side to make 24-pin connections. Problems were observed when soldering the headers to the chip carrier without a proper socket holder. Some damage to the bonding wires was noticed because of handling damage. The solution was to solder the headers to the chip carrier first; the chip was then mounted on the chip carrier and finally wire-bonded. Figure 7.1(b, c) shows the bonding diagram of a 2D hexagon lattice trap on a chip using the modified method. To ensure good conductivity from the backside of the chip, the recessed handle Si wafer around the periphery of the chip was directly wire-bonded to Pin 1. This allows the continuity checks to be made.

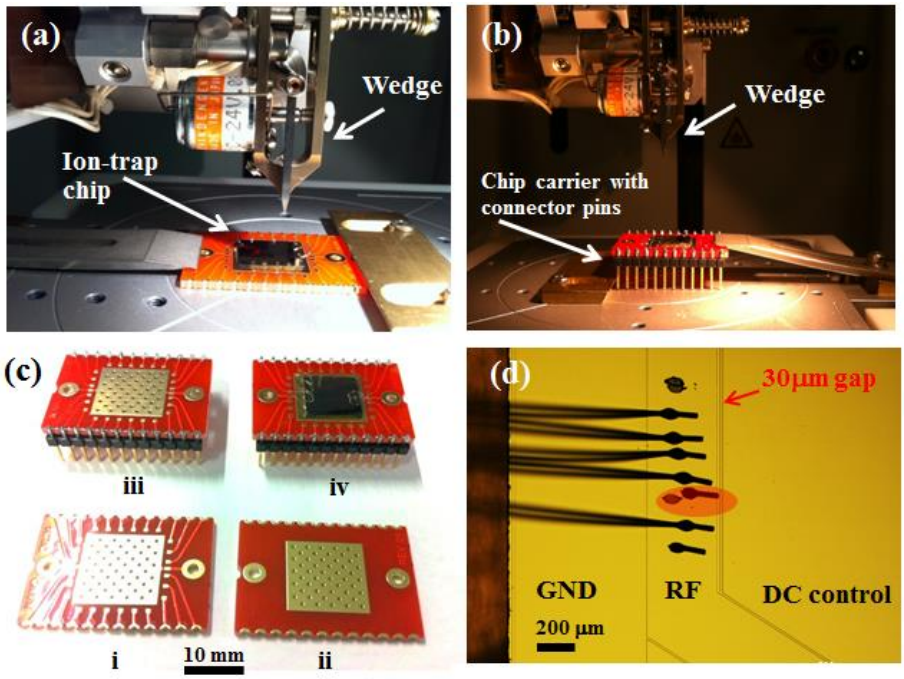


Figure 7.1 – Photographs of wire-bonding process (die-to-package). (a) Wire-bonding before soldering connector pins. (b) Wire-bonding after soldering connector pins. (c) A customized chip carrier (DIL24): (i) front-side, (ii) backside, (iii) soldering connector pins, and (iv) a mounted ion-trap chip with wire-bonding. (d) Multiple-wires bonded to a narrow RF electrode pad to increase the current flow. The highlight (in red) shows a misaligned-bonded wire occasionally causing a short electrode.

7.1.2 Trap electrical interconnect: chip-to-external power source

The electric current drawn by the microtraps is estimated to be less than the order of milliamps. A typical operating AC voltage for a 2D hexagon lattice trap is in a range of 200-500 V. All electronic components used in this setup are compatible with the high-voltage system. Since a 24-pin DIL chip carrier is customised and has a dimension of 3.2×2.3 cm, its row width of 2.3 cm (0.9 inch) is not compatible with DIL sockets available in the market. Therefore, the customised chip socket was required for a non-standard chip carrier. Hence a set of two in-line ZIP strip sockets (24-way ZIP strip SIL socket, Brand 3M, current rating 1 A, voltage 1000 V_{RMS}, glass fibre reinforced PSU, pitch 2.54 mm) was used to create a socket having the pitch equal to the chip carrier dimension as shown in Figure 7.2. These two ZIP strip socket were mounted on a high quality stripboard (VERO 10-2449K, euroboard 100×160 mm, Pitch 2.54 mm) by soldering. Next, the copper strips were cut to break the electrical

connection of two ZIP strip sockets. In the process of breaking the tracks, pieces of copper debris were created and might fall through the holes of the stripboard causing an unwanted connection. The board was cleaned and inspected to make sure that all holes were free of debris.

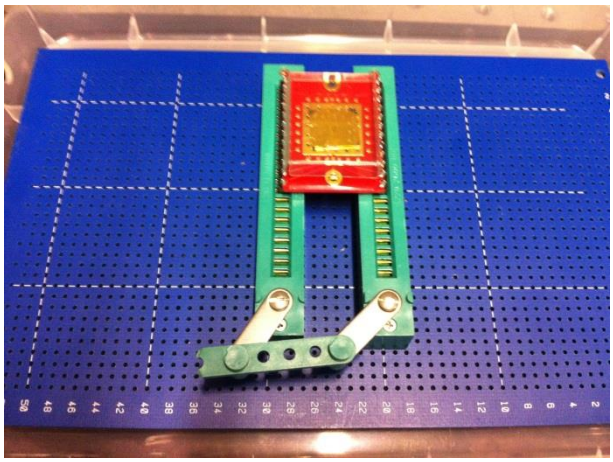


Figure 7.2 – Electrical connection from the chip package to the external power source with a set of two in-line ZIP strip sockets with ganging bar inserted for loading/unloading the device.

7.1.3 Choices of high-voltage AC power supplies

The development of the hardware platform depends on the complexity of testing schemes and number of electrodes. During the initial stage of particle trapping, only a high voltage AC signal applied to RF electrode is required, with the rest of electrodes grounded. A secondary AC high voltage is required for the levitation (out-of-plane). This signal is supplied to a recessed electrode (handle layer of SOI, backside of the chip) which is initially grounded during the initial trapping. For secular frequency measurement, two independent AC signals are essentially required. One is for the initial trapping by a high RF voltage V_{RF} at a frequency $\Omega_T/2\pi$ of a few megahertz applied to the RF electrode. Another is for sweeping the resonant effect by a very small AC voltage (~ 1-2 V) at a frequency $\Omega_{osc}/2\pi$ of a few hertz applied to a compensation DC electrode. A summary of voltage sources needed by each operation is provided in Table 7.1.

One of the crucial components for microparticle trapping experiment is a high-voltage power supply to drive the RF electrode. Considering typical operating ranges of the microtraps reported in Pearson et al. [83] and Britton et al. [87], a high-voltage power supply capable of producing a high-voltage range of 200-500 V at drive frequency up to several kilohertz is required. The following discusses several types of electrical power supplies that can be suitable or restricted to the desired experiments.

Table 7.1 – Summary of power sources for various ion-trapping experiments.

Operation	RF electrode (Primary AC)	Recessed electrode (Secondary AC)	Compensation electrodes
Trapping	AC 200-500 V, 0-2 kHz	GND	GND
Shuttling		GND	DC ±15 V
Levitating		AC 0-200 V, 0-2 kHz	GND
Secular frequency		GND or small AC 0-2 V	small AC 0-2 V

- **Commercial high-voltage power supplies**

This is an ideal choice with several advantages: compact, efficient, precise control of output voltages, reliable and long life-time, well-suited for different applications. For example, Trek Model 2210 offers controllable output voltage in a range of 0 V to ± 1 kV DC or peak AC, output currents in a range of 0 V to ± 40 mA peak AC, and large signal bandwidth DC to 40 kHz (-3 dB). Also Model 2220 offers a higher voltage range of 0 to ± 2 kV DC or peak AC but a lower output current range up to ± 20 mA and signal bandwidth of 7.5 kHz. However, these power supplies can cost thousands of pounds (Model 2210/2220, 1400 GBP).

- **Integrated circuits (ICs) high-voltage operational amplifier (op-amp)**

A high-voltage op-amp such as APEXPA95 was used by Pearson [113]. This op-amp offers a high output voltage swing up to 900 V (± 450 V), high output current up to 100 mA, and pulse current up to 200 mA into capacitive loads. To achieve a 900 $V_{pk\text{-}pk}$ output voltage, it requires a wide DC supply voltage range up to 450 V. There is also an option to have

output voltage up to 1000 $V_{pk\text{-}pk}$ from PA89. However, the cost becomes an issue since the price is higher for the model PA89, 493.61 GBP (per unit) compared to PA95, 137.44 GBP (per unit: refer to Digikey website).

- **Variable autotransformer (Variac)**

A variable autotransformer commonly also known as Variac provides continuously adjustable AC voltage from a fixed AC voltage supply. However, Variacs are usually designed for a nominal input voltage and frequency usually connected to an AC main supply 120/230 V, 50/60 Hz but only the amplitude of the output voltage is variable by rotating a knob-controlled output. Unlike a true transformer which has two electrically isolated windings called the primary and secondary, an autotransformer has a single voltage winding and does not provide isolation from the wall outlet as an input. This makes an autotransformer not suitable and unsafe for directly powering low-voltage devices or small loads. Variacs are generally used in many school or college laboratories including research labs because they are easy to find in the markets with different specifications to suit buyer needs at cost-effective prices compared to double-wound transformers of the same voltage/current rating. Variac costs start from less than a hundred pounds, but some may cost hundreds of pounds. Even though Variac offers several advantages such as adjustable voltage and low cost, a variable frequency is one of key requirements for microparticle trapping experiments. Thus a variable autotransformer does not fully fit all the test requirements.

- **Transformer circuits**

A core-trapping mechanism requires no DC offset for the main AC drive signal. Building a transformer circuit for microparticle trapping experiments is considered by far the best option when it comes down to cost. A transformer circuit can be built for less than one hundred pounds, but one single high-voltage op-amp chip costs many hundreds of pounds each. In electronics circuits, it is very common to use a voltage transformer to step-up or step-down a voltage. In this work, this was accomplished by building the high-voltage amplifier with a step-up-voltage transformer circuitry. The drawback is that transformers do not work

for DC. Hence a DC offset in the high AC voltage supplied to the RF electrode for the study of Mathieu's stability diagram under damped microparticle trapping in air cannot be achieved using a transformer circuit accordingly.

7.1.4 Primary high-voltage AC power supply

After reviewing all possible options, the use of transformer circuits for supplying high-voltage AC signals up to 1 $kV_{pk\text{-}pk}$ at frequency range below 10 kHz is considered to best suit all needs. The first and main reason is that the cost of building a transformer circuit for a high-voltage amplifier is lowest. The second reason is that the operating frequency for microparticle trapping is relatively low in the frequency range of 500 Hz to 2 kHz which attains a decent output and frequency response based on the transformer's specification. Furthermore the study of the trap stability region is not included in this framework; the absence of a DC offset voltage to AC voltage in the transformer circuits does not affect the trap operations listed in Table 7.1. A self-built transformer box[8] shown in Figure 7.3 contains six audio frequency transformers with all the secondary windings are connected in series. Two sets of three primary windings connected in series are connected in parallel giving an impedance of 6 ohms (see Appendix C). The transformer ratio is 1:200. The box is fitted with an overvoltage indicator which illuminates when the high-voltage output exceeds 1 kV_{RMS} (2.8 $kV_{pk\text{-}pk}$). Due to the fact that the frequency response of the transformer is not uniform and tends to attenuate more when the frequency is more than 10 kHz, the over-voltage indicator provides the limiting voltage to keep the output at a safe voltage level while operating in a wide frequency range. As a precaution during the experiment, the audio power amplifier and the oil-filled transformer box (a high-voltage amplifier) is not to run continuously over a long period of time (limited to one hour maximum) for safety purposes. A junction box on the top of the transformer allows for alternative series/parallel combinations of the primary and the secondary windings to be selected if required. It also has a 1000:1 potential divided output

[8] An oil-filled transformer box and audio power amplifier was built by Trevor Austin, ORC technical staff.

for output monitoring using 1 Mohms input of an oscilloscope. The transformer box is oil-filled so as to prevent corona discharge and other high-voltage breakdown.

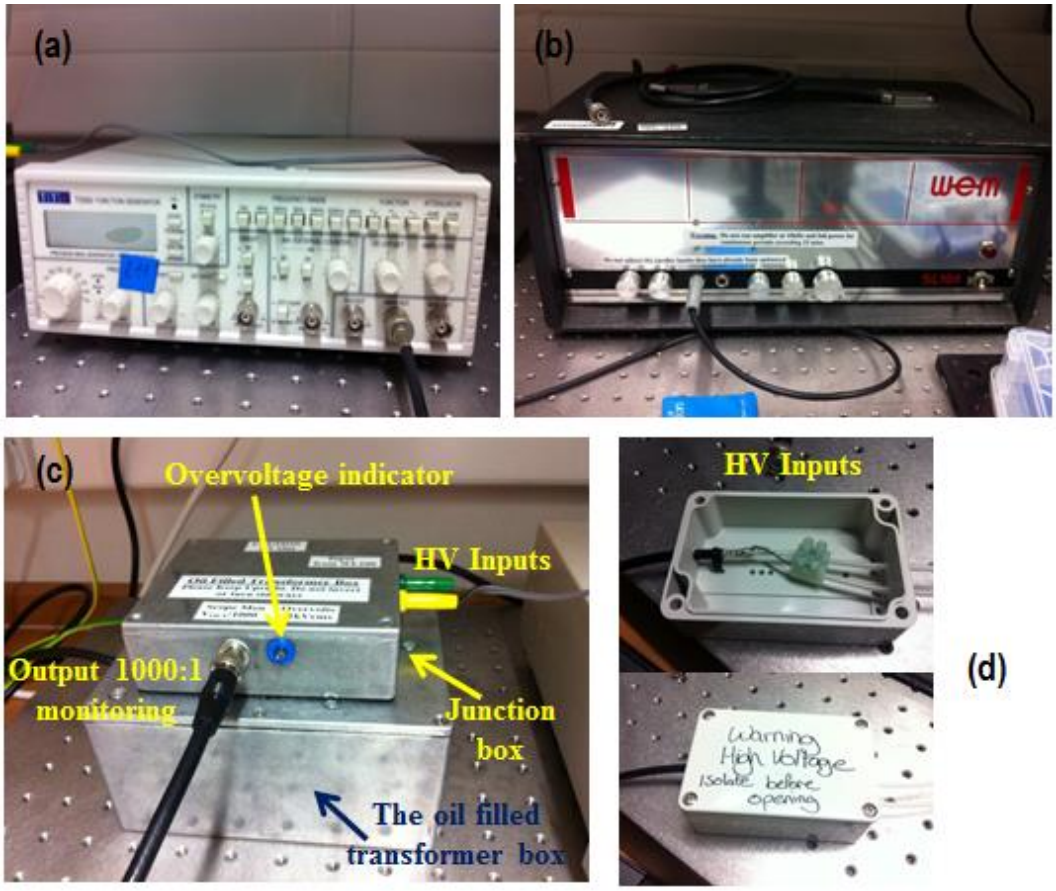


Figure 7.3 – A high-voltage AC supply to drive the RF electrode consists of (a) the function generator, (b) the power amplifier, (c) the oil filled transformer box, and (d) the BNC high-voltage output cable in a seal box.

7.1.5 Secondary high-voltage AC power supply (for levitating)

The level of AC voltage required to perform levitating scheme is based on the ε ratio (a ratio of the secondary to primary AC voltage) exhibiting the displacement of RF nil point (ion height) as discussed in Section 4.5.4. However the maximum RF nil shifting is limited to $\varepsilon < 0.4$ for the in-phase mode ($\theta = 0°$), resulting in decreasing ion height. Considering typical trapping conditions with a primary AC voltage range of 200-500 V, the secondary AC voltage

up to 200 V is required to be capable of observing the change in the ion position. Therefore, a commercial high-voltage amplifier, a New Focus 3211 model with the maximum output of ± 200 V[9] can be used to produce the secondary AC voltage.

7.1.6 The complete trap-drive electronic setup

For the high-voltage AC system, both primary and secondary AC voltages (V_{AC1}, V_{AC2}) require the same frequency, zero degrees or 180 degrees phase shift (for the levitation operation) and need to avoid the other relative phase shifts, leading to excessive micromotion. Thus a single output voltage from the function generator was used to supply both high-voltage amplifiers as depicted in Figure 7.4. The voltage level from the function generator was preferably fixed to approximately 3.6 $V_{pk\text{-}pk}$ to drive the audio power amplifier. Therefore inverting operational amplifier (Op-amp) circuits was needed to produce a small AC output less than 5 V (maximum input level of high voltage amplifier 3211) and with a 180-degree phase shift (see Appendix C). A rotary switch (one pole, 12 positions, withstanding an AC voltage up to 500 V) was used for selecting choices of the input voltage to the 3211 high-voltage amplifier. This small AC input was amplified with a gain of 40 to produce a desired output level for the secondary AC voltage supplied to the recess electrode. All high-voltage AC signals supplied to the trap electrodes were monitored using a simple form of a voltage divider resistor circuit. The output of the divider circuit was connected to the oscilloscope. With a known voltage divider ratio, the actual high-voltage level can be calculated.

Six DC voltage input channels for the shuttling operation were powered by a typical DC power supply capable of providing a DC signal in a range of ± 15 V. Six toggle switches (DPDT, On-Off-On) were needed for controlling the polarity of the input DC signals corresponding to a transport direction and a polarity of charge carried by the particles. A diagram of the complete electronic control used for different trap operations is illustrated in Figure 7.5.

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[9] A New Focus 3211 high-voltage amplifier (max output voltage: ± 200 V, max output current: 110 mA, gain: +40V/V, DC offset: -200 to +200 V, max slew rate: 650 V/us and input impedance: 5.75 k)

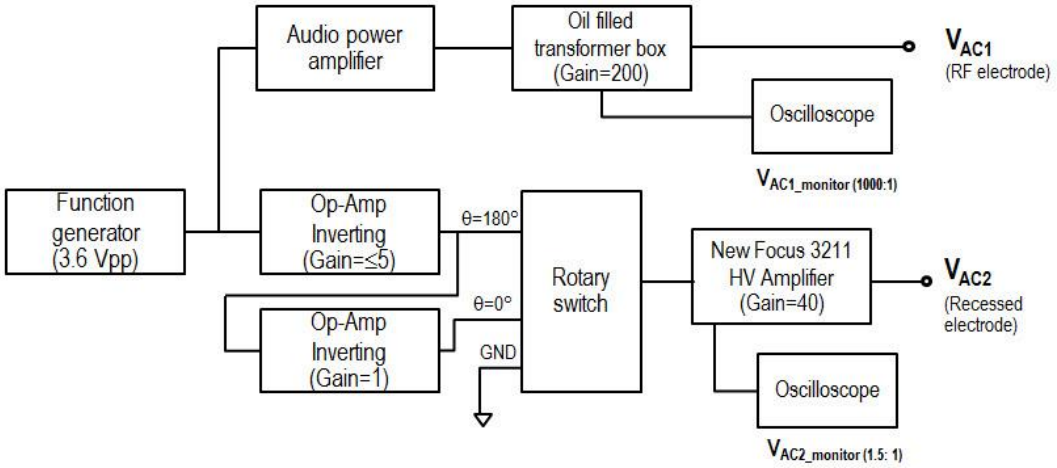


Figure 7.4 – Block diagram of high-voltage AC power supplies to trap electrodes (a RF electrode and a recessed ground electrode).

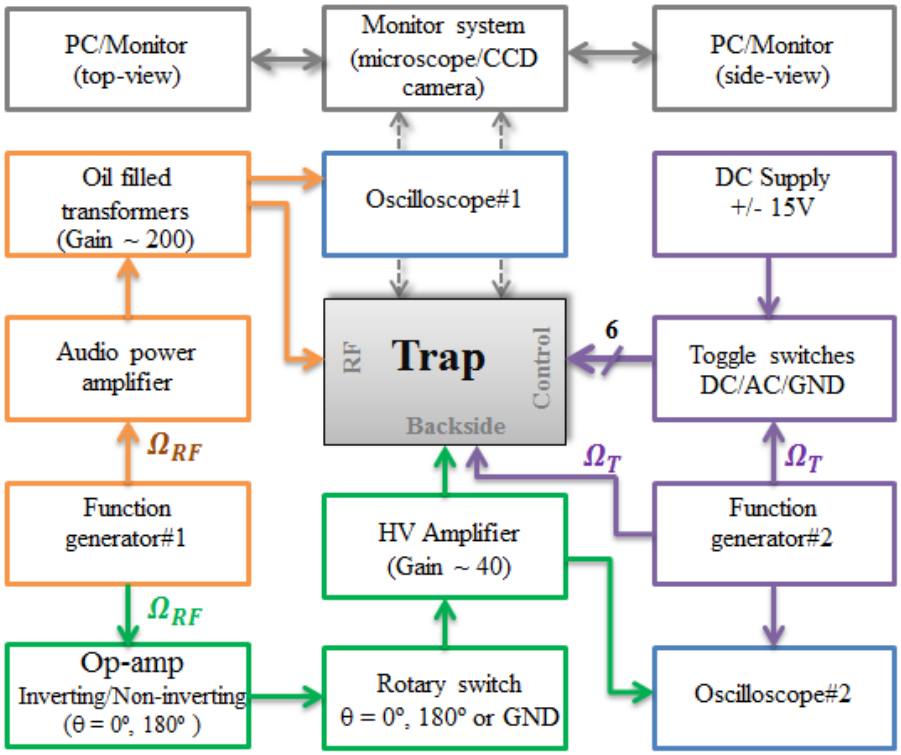


Figure 7.5 – Block diagram of the complete trap drive electronic setup.

7.2 Imaging system

All motional observations and measurements of microparticles in the experiments were carried out using charge-coupled device (CCD) cameras borrowed from the optical laboratory[10]. In each experiment, the angles of imaging were adjusted by means of trap axis of interest. For instance, the top- and side-view cameras with medium magnification were required for a normal trapping and shuttling operation. The levitation operation required higher magnification for observing particle levitation heights using a side-view camera. The secular frequency measurement for particle motion oscillating in all three directions also required both side-view and top-view cameras. Two computers were used for monitoring and recording the positions and motions of trapped particles during the experiments. For initial trapping, the objective lenses mounted on a Motic Digital Camera[11] for top-view imaging and a Dino-Lite USB digital microscope was used for side-view imaging, respectively. A Watec digital colour camera (Model: WAT-202D Auto IRIS) was used to monitor variation in particle height during the levitation experiment. This camera setup consists of the ordinary camera lens mounted onto a charge-coupled device (CCD) camera attached to an USB video capture device[12] and a computer. A crude measurement of the particle height above the surface electrode was obtained from the photographs captured by frame during the operation and calculated with known objects such as optical fibres (a 125-μm diameter cladding and a 0.25-mm outer coating diameter) or glass microspheres (e.g. 30 μm, 100 μm in diameter).

[10] The Optoelectronics Research Centre (ORC) at the University of Southampton, UK

[11] Moticam 2300 3.0M Pixel USB2.0 which includes Motic's Images application software for image capture, video capture, magnification calibration for dimension measurement

[12] EZCAP.TV 116 EzCAPTURE USB 2.0 video capture device, PAL: 720×576 @ 25 fps

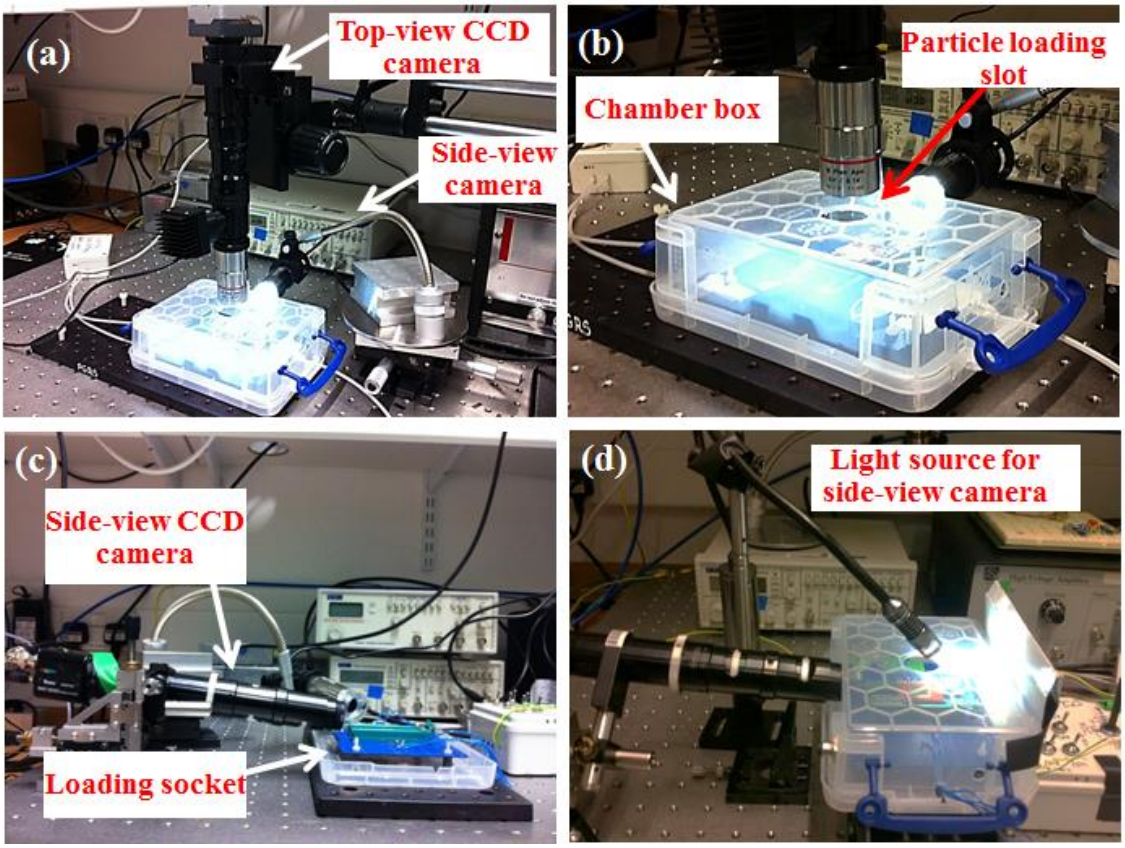


Figure 7.6 – Imaging system setup. (a-b) A top-view camera (Moticam Digital Microscope 2300 3.0M Pixel USB2.0) and side-view camera (Dino-Lite USB digital microscope) used for initial trapping and shuttling. (c-d) A side-view camera (Watec WAT-202D Digital colour camera Auto IRIS) used for measuring trap height shifting during levitating operation.

7.3 Conclusion

The development of experimental apparatus for experimental realisation of a 2D hexagonal lattice trap including microparticle trapping, shuttling between different lattice traps and levitation in air was presented. This experimental apparatus, designed for accommodating non-complex testing schemes and a small number of electrodes, is a cost-efficient hardware setup made from standard off-the-shelf components and in-house developed tools. The microfabricated ion-trap chip was first mounted on a chip carrier socket of which a 12-way PCB header was soldered to each side to make 24-pin connections. The trap electrodes were then wire-bonded to the bond pads of the chip carrier. Since the chip carrier was customised and not compatible with commercial DIL sockets, two in-line ZIP strip sockets were adapted to create a socket compatible with the chip carrier size. A primary high-voltage AC source used for all key operations includes a self-built transformer box, a power amplifier and a function generator giving the output up to 1 $kV_{pk\text{-}pk}$ at a frequency range below 10 kHz. For levitation operation, a commercial high-voltage amplifier was used as a secondary AC source with a voltage level of ± 200 V. The experimental control was based on manual control switches for selecting input phase (i.e. zero degrees or 180 degrees phase shift) of a secondary high-voltage AC signal (for levitation) and inputs of six DC voltages (for shuttling).

All motional observations and measurements of trapped particles in the experiments were carried out by charge-coupled device (CCD) cameras. There were two computers for monitoring and recording the position and motion of trapped particles during the experiments. Since this experimental setup was assembled and used for the first time for the microparticle trap, the efficiency and limitation of this apparatus is evaluated during the course of experiments in Chapter 8.

Chapter 8

Microparticle trap experimental results

In this chapter, the experimental realisation of microparticle trapping in the fabricated two-dimensional (2D) hexagonal lattice trap is presented. First, particle charging and loading methods are discussed. The experiments are conducted in air at atmospheric pressure. The PCB macro-scale trap prototypes containing a single, large trapping zone and a deep trapping depth is used in early stages of experimental setup in which trapping of various particle materials and dimensions with unknown charges can be examined conveniently. Next, the measurement of electrical properties (i.e. capacitance and breakdown voltage) of the SOI-built test devices is reported. The key operations of the microparticle trap (i.e. stationary trapping, 2D shuttling, and levitation to different trap heights) are demonstrated. In addition, the secular frequency measurement using a technique called "*tickle*" and the charge-to-mass (Q/m) approximation using "*the boundary ejection*" method are investigated experimentally in this work. Besides the successful demonstration of microparticle trapping in the 2D hexagonal lattice trap, a fault in the design of the Y-junction trap discovered later in the development is addressed at the end of the chapter.

8.1 Particle charging and loading technique

The charging mechanism commonly used in the experimental demonstration of charged particle trapping and manipulation using ion-trap devices [90], [111] is the triboelectric charging method. The triboelectric charging technique is based on rubbing and separating particles of interest against a suitable material; for example, a Teflon sheet using a brush, or pushing them through a Teflon tube. Charging the micron-size particles conducted in this work is also based on a triboelectric process. The optical fibre covered by a coating material made of acrylates (a type of vinyl polymer) with a diameter of 250 μm, was charged by rubbing it against nylon, wool or a paper sheet. The fibre was then negatively charged according to the triboelectric series (see Appendix D). When neutral particles were touched by a negatively charged fibre, the transfer of charge by contact occurred. Hence, the particle surface was negatively charged. In Figure 8.1(a, b), the charged fibre was used to pick up some particles and load them through the opening window at the top of box surrounding the trap setup. To load particles, a plastic pipette was exploited to guide the fibre through the centre of the lattice traps. With some modification as shown in Figure 8.1(c), the tip of the guiding pipette mounted on a translation stage was attached with a micro-fine-tip plastic pipette (~ 200 μm in diameter) to prevent the fibre falling on to the microtrap chip. The fibre was gently tapped to drop particles into the trapping zone. By chance, a few particles were trapped simultaneously at different trap sites. A dummy trap with some particles loaded was used for aligning the particle loading tool and setting up cameras for optimal imaging. The most suitable loading distance was found to be ≈ 15-20 mm above the surface trap and the transfer pipette must be tilted to avoid blocking the top-view camera.

Several of the trials on charging and loading various particles listed in Table 8.1 were carried out. The use of 30-μm soda lime glass spheres was found to give the best result because they are less likely to stick to one another or to solid surfaces compared to other materials such as Al_2O_3 and Lactose monohydrate particles. From optical microscope inspection, soda lime glass particles showed a spherical particle shape that makes charge transfer by contact more efficient than non-spherical particles. Most of the particles fell on to the trap surface could be removed. However, some of them can become stuck within the small isolation

trenches between electrodes and also the trap sites which have opened trenches > 270 μm wide. This ruled out the use of copper spheres or any conductive materials because of the risk of short circuit. Therefore non-conductive particles are the ideal choice for conducting microparticle trapping experiments in the surface-electrode trap geometries.

Table 8.1 - List of micron-size particles available in the laboratory.

Material	Dimension (in diameter ∅, μm)	Density (g/cm^3)
Soda lime glass	30, 100	2.4-2.6
Al_2O_3 (Ceramic, aluminium oxide)	< 53	3.9-4.0
Lactose monohydrate	< 32	0.35-0.78
Copper	20-50	5.0

After many trials during the initial loading and trapping stage, it also became clear that the trap will become contaminated by sticking particles on the electrode surface and inside the isolation trenches between electrodes. Importantly, controlling the integrity of electrode surface and trench isolation is a benefit for the long-term use and reliability. In order to minimise the numbers of particles sticking in individual lattice sites and in between isolation trenches, and to keep the gold electrode surfaces as clean as possible, untrapped particles needed to be efficiently removed after loading by blowing them off the trap as often as possible. After several trials for the most convenient and efficient way of cleaning the trap surface, the best practice was established as purging of the trap surface with N_2 gas. The N_2 gas was introduced into the chamber via a small plastic tube located in close proximity to the central trap region. There is a need to be careful not to damage the delicate bonded wires around the microtrap with the small plastic tube. This procedure allows operating the trap for long periods of time and does not require the operation of the trap to be interrupted. This method also saves times in re-aligning the optical imaging system and particle loading tool, which needs to be done every time the trap chip is removed from the chamber.

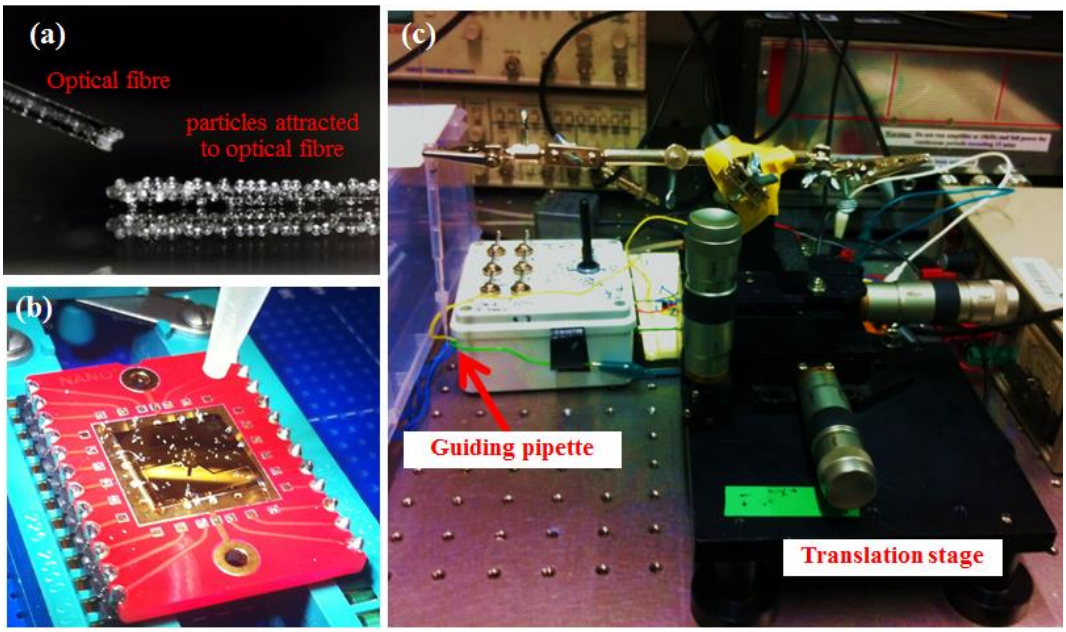


Figure 8.1 – Charging and loading of microparticles to the experimental trap. (a) The charged fibre was used to pick up some particles and (b) to load them to the microtrap chip through the opening window at the top of the box surrounding the trap setup. (c) The guiding pipette mounted on a translation stage was loaded with the fibre shown in (a).

8.2 Microparticle trapping in a PCB-planar ring electrode trap

There are several factors that affect the motion of microparticle trapping in air. These include the value of charge-to-mass ratio of trapped particles, air flow conditions and drag force, trap properties (i.e. trap depth and the stability parameters corresponding to the trap-drive voltage and frequency). Thus initial trapping of a particle of unknown charge-to-mass ratio can be quite difficult in practice. At the beginning of the experiments, soda lime glass dry spheres of 100 μm in diameter were used because these particles can be clearly seen using a typical CCD camera within a mid-high range of magnification. The initial driving AC voltage was 300 V at frequency $\Omega/2\pi = 1000$ Hz based on the simulation results provided in Appendix A (Table A.1). After trying unsuccessfully to trap for a long time in the fabricated 2D hexagonal lattice traps with various particles and combinational values of drive voltages and frequencies, the dummy trap, a ring electrode trap similar to a surface-electrode point Paul trap presented in [112] was exploited for the experimental start-up instead. This trap was

fabricated on the PCB without the need for cleanroom facilities and completed within a few days by Lekitsch[13]. The ring-electrode trap consisting of a single trap zone was also found to be useful for evaluating charged particles and trap properties due to its higher trap depth, larger trap size and higher breakdown voltage in air (for large interelectrode gap ~ 120 μm). This made it much easier to achieve microparticle trapping compared to the 2D hexagonal lattice trap.

The ring electrode geometry consists of an inner circular ground electrode with radius a = 0.68 mm, and an outer RF ring electrode with radius b = 1.240 mm, respectively. The interelectrode gap is approximately 0.15-0.20 mm. The trap height is calculated to be approximately z_0 = 642.87 μm above the electrode plane. The material used is FR4 and composite pre-sensitised PCB laminates, 1.6 mm board thickness with 35 μm of copper on both sides[14]. The ring electrode was designed using a program called "*DipTrace*" and printed on a transparent foil followed by an in-house PCB exposure step (two-minute exposure), a PCB development (one-minute development) and chemical wet etch (etch time varies from 5 to 30 minutes due to variations in the saturation of the etching solution from one wafer batch to the next). The 0.30 mm diameter holes were drilled into the centre and side pads of the patterned PCB-trap chip. A thin copper wire (0.25 mm in diameter) was then soldered into the holes to make contacts between top pads and bottom ground plate. At the final step, the trap was slightly polished to flatten the solder bumps with sandpaper (P800 sandpaper). The finished trap is shown in Figure 8.2(b).

[13] The PCB-ring electrode trap was constructed by Bjoern Lekitsch, a PhD student at Ion Quantum Technology (IQT) group at the University of Sussex, UK.

[14] MEGA PCB, FR4, 100×160 mm, DS, PHOTORESIST, and Manufacturer Part No: 3204959.

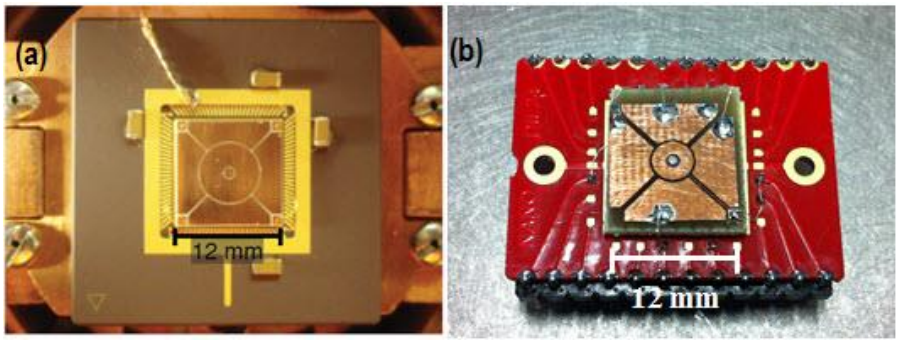


Figure 8.2 – A dummy trap used during the experimental start-up and the initial particle charging and loading trails. (a) The original design of a surface-electrode point Paul trap by Kim et al. [112]. (b) Self-constructed ring electrode trap (similar to Kim's design) mounted on the chip carrier.

Single glass particles were loaded through the access window from the top of the chamber immediately after charging. With this setup, it was possible to temporarily suspend one particle or multiple particles above the trap. Most of the untrapped particles would fall onto the electrode surface. The experiments were repeated many times at the same condition because charge on a particle was varied from one to another. The experiments were performed within the operating ranges of AC voltage V_{RF} = 300-350 V at drive frequency $\Omega/2\pi$ = 600-1100 Hz corresponding to the trap depth $D \geq 0.15$ eV and the stability parameter $q \leq 0.70$ suggested by the numerical calculation. The driving voltage and frequency were continuously tuned for stable trapping due to the fact that the exact charges on these particles were unknown. Experimentally, trapping 100 μm glass spheres was not possible. It became clear that both millimetre-size and micrometre-size traps are not capable of trapping a 100 μm glass sphere. This is suspected to be a result of a small value of charge-to-mass (Q/m) ratio (very small charge Q, large mass m), the influence of gravity. Hence, smaller particles (soda lime glass dry spheres with 30 μm in diameter) were used for trapping. Using similar test conditions, 30 μm glass spheres were successfully trapped in the ring electrode trap at ~ 650 μm above the trap surface as shown in Figure 8.3. At the AC voltage V_{RF} = 350 V at drive frequency $\Omega/2\pi$ = 700 Hz, the first attainable trapping with a long lifetime of 60 minutes was observed. However, the particle can potentially be trapped for longer periods of time but the high-voltage AC source (the oil-filled transformer box) was always turned off after one

hour to avoid damaging the transformers from continuous operation (for safety purposes).

Table 8.2 shows the normal operating conditions of this trap. During the experiment, the trapped particle oscillated widely in the trapping axis (perpendicular to the electrode surface) and moved in a circular motion as shown in Figure 8.4(a). This incident happened while using one of the light sources which created high noise level coupling into the main AC power/ground system connected to the ground electrode of the trap. The affecting noise induced by the external source resulted in excess micromotion causing the alteration of trap position from the RF nil point and instability trap. After the problematic light source was removed, the strong oscillation disappeared, as seen in Figure 8.4(b).

Table 8.2 - Operating parameters of a millimetre-size ring electrode trap, operated in ambient air, using 30 μm diameter glass microspheres.

Trap dimension	Operating parameters		Experimental results		
	Voltage (V)	Frequency (Hz)	No. of trapped particle(s)	Ion height h (μm)	Particle lifetime
A PCB-planar trap (a single ring electrode) radii = 0.55 to 1.80 mm electrode-gap = 0.12 mm	300	600	1	-	15 sec
	350	600	1	700	4 min
	350	700	1	656	60 min[1]
	300	800	2	-	5 sec

[1] Terminated high-voltage power supply

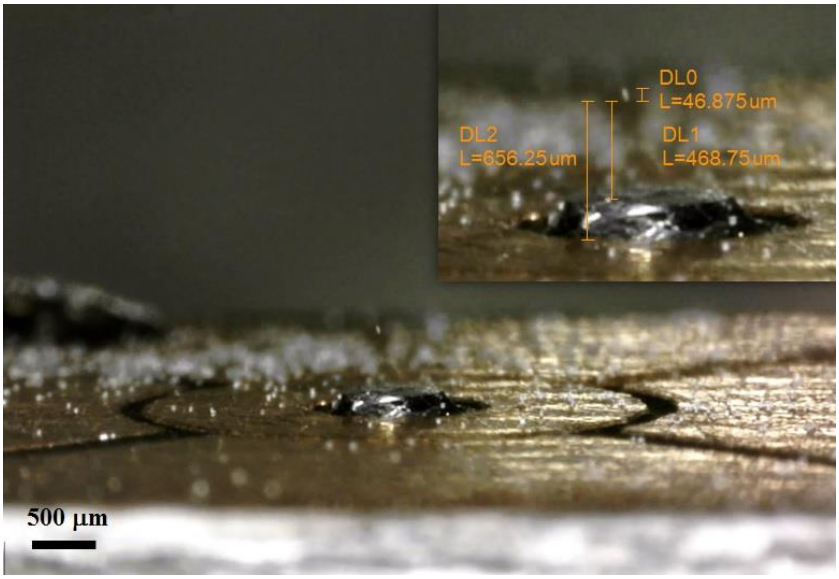


Figure 8.3 – A photograph of a single 30 µm glass microsphere trapped at ~ 650 µm above the trap surface (refer DL2). Inset shows a protrusion of the centre ground electrode (~ 200 µm) from the surface plane. In this image, the measured particle height is based on the tilt of the camera.

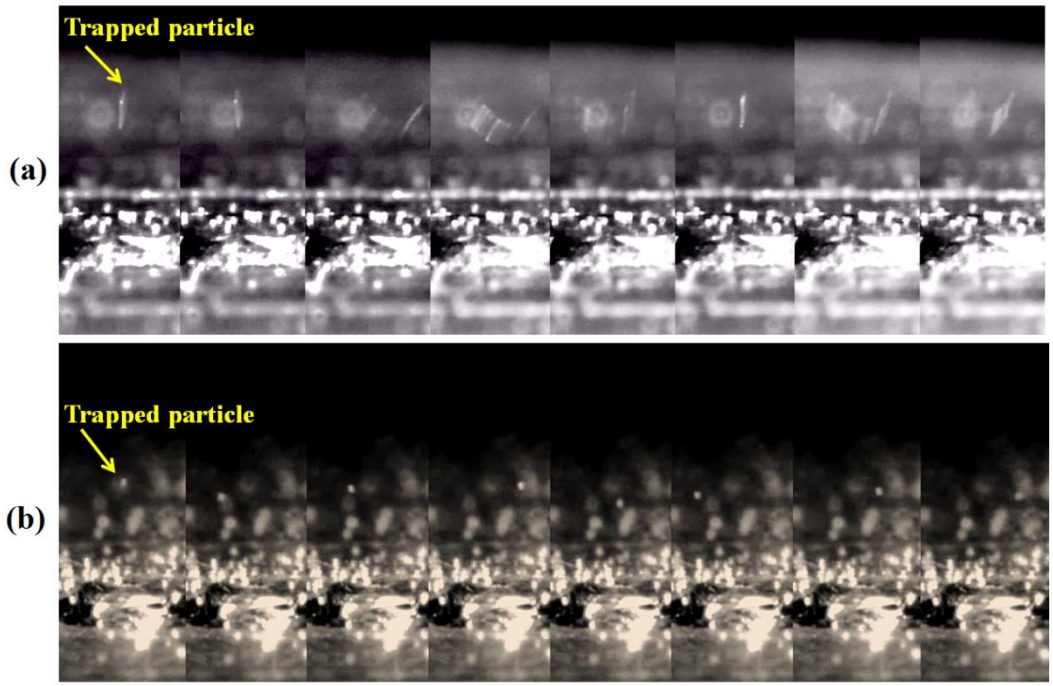


Figure 8.4 – The motion of a particle trapped in the PCB-ring electrode trap. (a) In the presence of excess micromotion due to additional ground noise from the problematic light source, the particle exhibited oscillatory motions on the trap axis. (b) The excess micromotion was eliminated after the problematic light source was removed. (The still images were captured in intervals of five seconds from the video files).

8.3 Microparticle trapping in a 2D hexagonal lattice trap

After successfully trapping 30-μm glass microspheres in the PCB-ring electrode trap, the experiments with a 2D hexagonal lattice trap were carried out using similar experimental procedures. Each experiment began with charging and loading particles close to the centre of the trap. After one or multiple particles were trapped, the experiments towards 3D particle manipulation illustrated in Figure 8.5 started. The operations include a 2D shuttling to different lattice traps (in the xy-plane), and levitation (changing in the trap height by means of RF nil shifting in the z-direction). Furthermore, the measurement of the secular frequencies in association with the determination of Q/m ratio of trapped particles is also demonstrated.

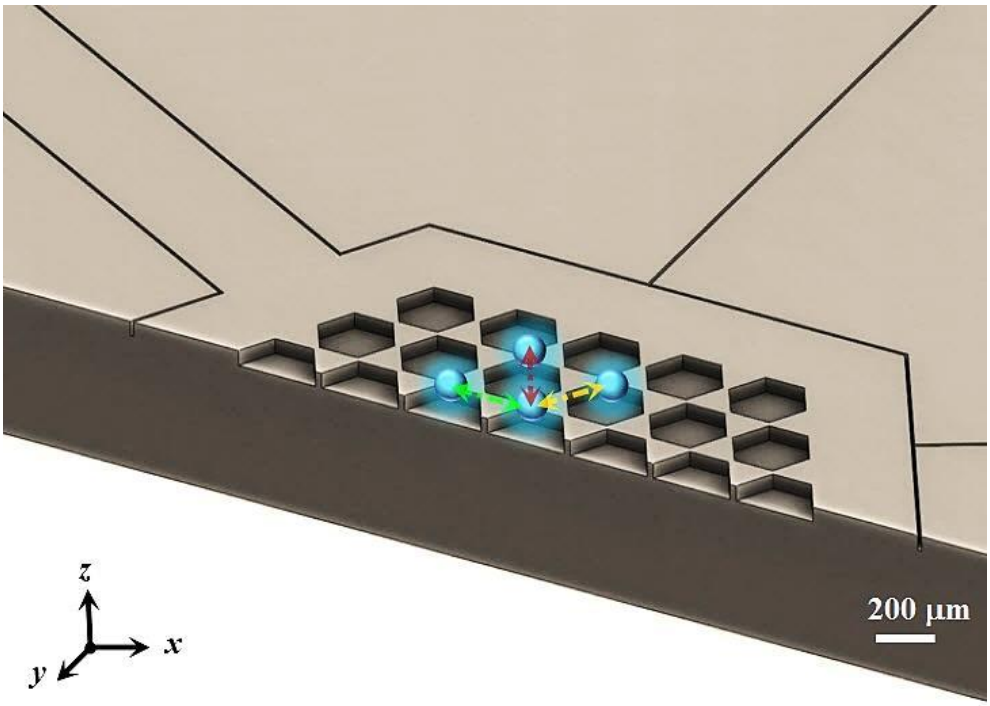


Figure 8.5 – Illustration of a 2D hexagonal lattice trap (in a cross-sectional view) with particle transporting in 3D (shuttling in the xy-plane and levitation in the z-axis).

8.3.1 Electrical breakdown in air

In an attempt to evaluate the electrical breakdown voltage of the microstructures, the electrical breakdown can occur through an insulating material (bulk breakdown), micrometre-scale gaps between electrodes or surface breakdown (i.e. voltage breakdown along the surface of insulators, primarily in vacuum). Commonly, surface breakdown (flashover) of insulators is known to occur at electric field strengths which are lower than those of the bulk breakdown through the material. With the increase of a voltage applied to the insulator in uniform fields in directions parallel with the insulator surfaces, the field strength at the triple junction (the region where the electrode, insulator and vacuum or gas meet) increases. The mechanism of surface flashover is generally initiated by the emission of electrons at the triple junction. The model of surface flashover based on the assumption that discharge develops in a layer of gas desorbed from the insulator surface was presented in Miller [220], [221] and Belyaev [219]. The dependence of the flashover voltage was experimentally investigated under both vacuum and atmospheric air conditions using various solid insulators introduced by Sivathanu and Hackam [218]. The experiment results described in their research suggest that the surface flashover field of the insulator at a fixed dimension (in millimetre scale) is relatively lower (by a factor of 4 to 6) in atmospheric air (10^5 Pa) than in high vacuum (10^{-6} Pa). However the electrical breakdown for microstructures with micrometre-size air gaps between electrodes can be the dominant effect limiting the maximum voltage that can be applied to the devices.

For ion traps, a relatively lower breakdown threshold at RF frequency range is an issue of great concern when designing micrometre-scale ion traps, as reported in Stick et al. [77]. In particular, surface-electrode ion traps (SEITs) have much shallower trap depth compared to conventional linear Paul traps. Deeper well depth and greater trapping efficiency are both essential. Therefore, the design of microtrap structures which offer a greater limit of applied voltages is a favourable condition. There were two different test structures - (i) a single square electrode, and (ii) two electrodes with a micrometre gap - used in this study. Both devices were fabricated on SOI substrates with similar processes used for the actual devices (a 2D hexagonal lattice trap). The test structures have simple electrode geometries designed for

the study of electrical breakdown behaviours. A single square electrode was primarily used to investigate the surface breakdown (flashover) of the insulator (a buried oxide layer with different thicknesses of 5 µm and 10 µm) in ambient air. A two-electrode structure with a small isolation trench was used to study the electrical breakdown in air of interelectrode gaps ranging from 3 µm to 9 µm. .

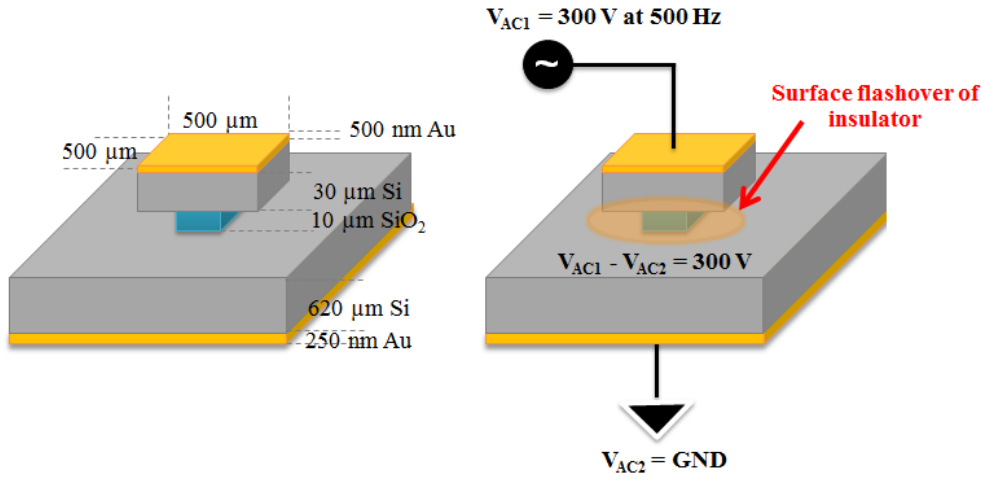


Figure 8.6 – Schematic of a SOI-built test device (a single square structure) used for measurement of surface breakdown voltage.

The electrical breakdown characterisation presented in this study was performed in a small chamber in an ambient air environment at room temperature. In the first experiment, the surface (flashover) breakdown test of the SOI-built test device containing a single square structure is illustrated in Figure 8.6. This device was mounted on the chip carrier using the conductive glue providing the electrical contact between the ground system (GND) to the Si handle layer (gold coating at the back side to improve the conductivity). The square gold electrode was connected to the AC voltage source (V_{AC1}) and the Si handle layer was grounded from the back side of the chip. To perform the breakdown measurement, the AC voltage was applied to the electrode and slowly increased by controlling the gain of the audio amplifier fed through the step-up transformer circuit, with a gain of 200. This method of

measurement relies on the speed of reaction from the operator as the breakdown events can happen rapidly and it is impossible to stop and measure precisely at the actual breakdown threshold. Thus, the breakdown voltage (V_{bd}) reported is the applied AC voltage level allowed before the breakdown takes place, which can be observed on the voltage drop to zero (short circuit at the breakdown point) through the oscilloscope. In addition, the observation of breakdown events was performed by monitoring a visible breakdown due to arcing, showing a rapid spark or glow using a real-time record by CCD cameras. Since the step of voltage control is coarse (≈ 20 V/step as a smallest step from turning the gain knob manually), a weak glow (or a localised spark) resulting in minimal destruction on the device was rarely observed due to the limitation of high-voltage power supply resolution and imaging system capability.

The breakdown was measured across four different samples and the surface breakdown voltage (V_{bd}) observed is approximately 360-380 V from the SOI-built test devices with the oxide thickness of 10 μm. The lower values of the breakdown voltage of 320-322 V were found from a thinner oxide layer of 5 μm. Figure 8.7 shows that arcing during the breakdown event last for 5-10 seconds recorded from two different CCD cameras. The images from the side-camera show the spark glowing underneath the gold-Si electrode interfacing with the buried oxide layer which is undercut and not visible in this figure, see Figure 8.7 (b1-b4). The vacuum flashover measurement using similar SOI-built test samples (see more details in Section 6.3.1) reports an average RF breakdown voltage of 1061 ± 5V and the static DC breakdown voltage of 1298 ± 32 V [135]. It can be clearly seen that the mechanisms that govern the breakdown in air and vacuum are different.

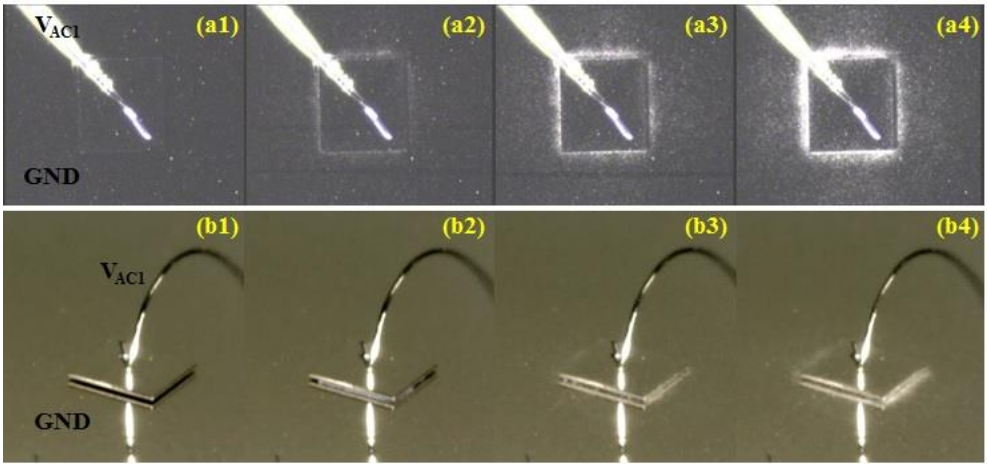


Figure 8.7 – Surface breakdown (flashover) in air of a SOI-built test device consisting of a single square electrode with a 10 μm-thick buried oxide. The still images (a1-4 from a top-view camera, b1-b4 from a side-view camera) were captured from the video file. (a1 and b1) Before breakdown. (a2-a4 and b2-b4) During breakdown observed a glowing spark at the oxide layer sandwiched between two electrodes at the breakdown voltage $V_{bd} \approx$ 360 - 380 V.

The second experiment of the electrical breakdown behaviour in a micrometre scale gap between two planar electrodes illustrated in Figure 8.8 was carried out with the same procedure used in the first experiment. In this experiment, the breakdown voltage in air gap for electrode separations between 3 μm and 9 μm was investigated. The result shows that the breakdown voltage for smallest air gap of 3 μm is found to be 305 V, and this increase slightly to 320 V with increased gap spacing up to 9 μm. During the breakdown ($V_{bd} \approx$ 315 V), the localised sparks along a 7 μm gap and underneath metal-Si electrode were observed (see Figure 8.9). From this breakdown, burnt residues at the microgap region and the Si handle layer underneath the buried oxide layer can be seen in Figure 8.10. Similar electrical breakdown tests were repeated on the SOI-test structures with the oxide thickness of 5 μm. Table 8.3 is a summary of AC breakdown voltages in air for two different types of test structures.

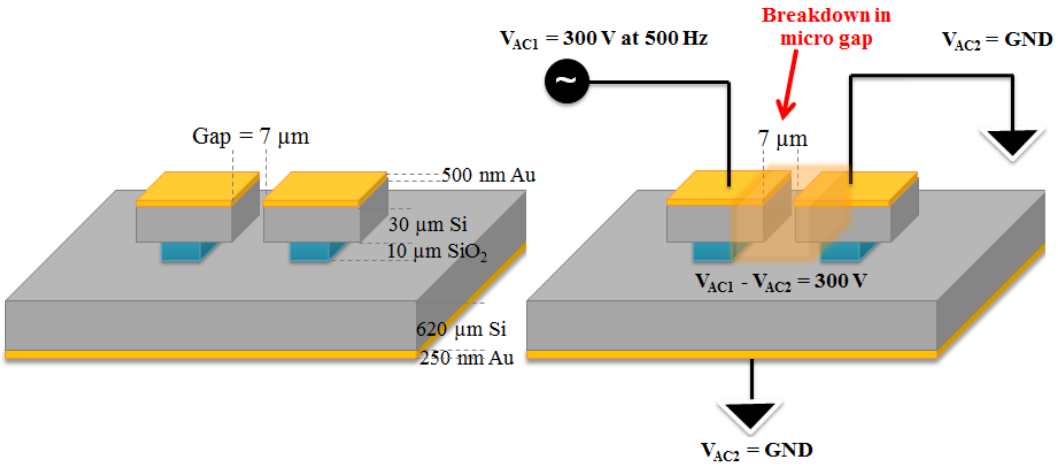


Figure 8.8 – Schematic of a SOI-built device (two square electrodes with a 7 µm electrode gap) used for measurement of electrical breakdown in air across micron scale gaps.

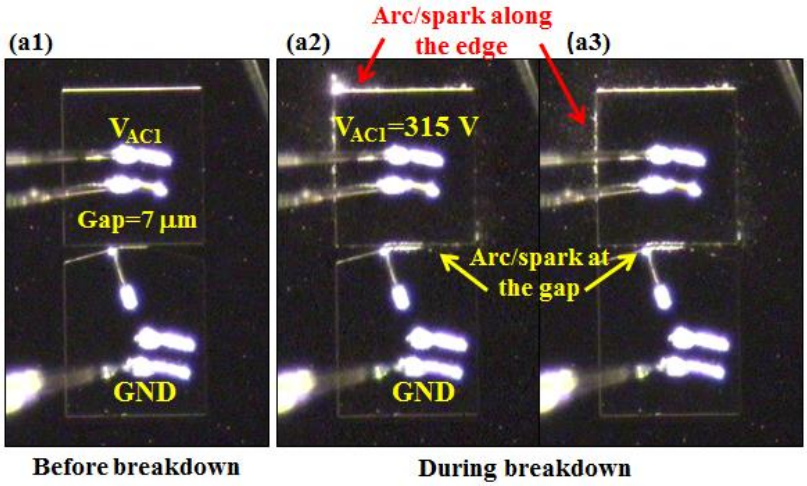


Figure 8.9 – Electrical breakdown in air of a SOI-built test device consisting of two square electrodes with a 7 µm electrode gap fabricated on a SOI substrate with a 10 µm-thick buried oxide. (a1) Before breakdown. (a2-a3) The localized spark was initiated along the electrode gap region and continued to the oxide layer underneath the gold-Si electrode at the breakdown voltage $V_{bd} \approx 315$ V.

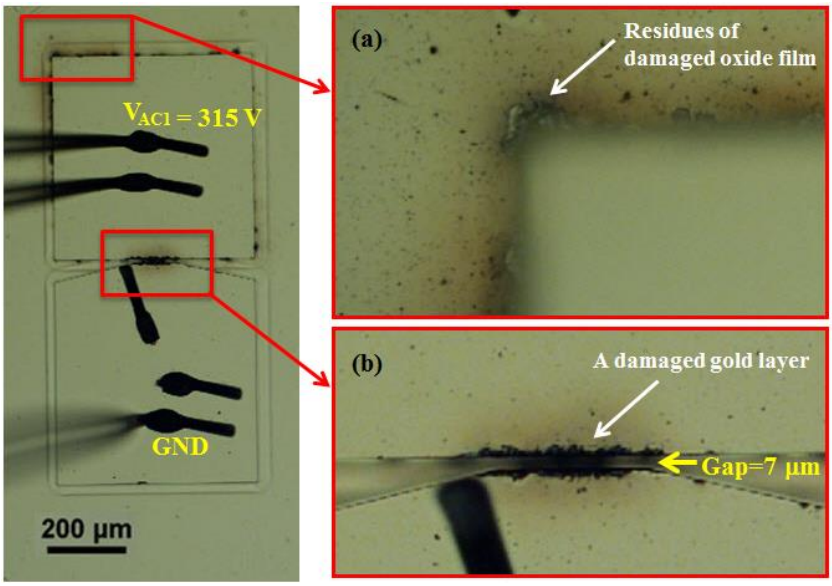


Figure 8.10 – Optical microscope images of a two-electrode test device with a 7 µm electrode gap after the air breakdown at $V_{bd} \approx 315$ V. Insets: (a) Burnt residue of the buried oxide layer. (b) Burnt residue and the damage occurred on gold electrode surfaces at the micro-gap region.

The resulting electrical breakdown across micron-scale gaps observed in this study is slightly lower than those published results between 380 V and 410 V for the same air gap distances [223], [224]. This is suspected due to the environmental variations from one to another. In addition, moist surface under relatively high humidity in air or accumulation of contaminants on the electrode surface and inside isolation trenches after using the traps for some time can cause the surface breakdown to be much worse. Attempts to clean the trap surface during operations or removing moisture pickup using baking treatment may improve the breakdown potentials. The surface breakdown (flashover) that occurred is associated with the thickness and undercut profile of the insulator sandwiched between the top metal electrode and the ground plane. In particular a deep V-shaped undercut (~ 60-70 µm wide) obtained from a buffered HF oxide etch, thought to be a result of a poor bonding of two buried oxide layers. This etched profile with a deep lateral undercut results in a substantial increase of the path length along the surface of the insulator (a buried oxide), thereby increasing the surface flashover voltage due to the extra path length as illustrated in Figure 8.11. Thus, a higher surface breakdown voltage was observed in a SOI microstructure with a 10 µm-thick

buried oxide layer compared to one with a 5 μm-thick buried oxide layer. For the experiments conducted in air, the dominant breakdown in a 2D hexagonal lattice trap is the electrical breakdown across micrometre-scale electrode gaps. Therefore, the maximum AC voltage which can be applied to the microtrap is limited to ≈ 320 ± 10 V for the smallest interelectrode gap of 10 μm.

Table 8.3 – Electrical breakdown voltage V_{bd} on the SOI-built test devices.

Electrode geometries	AC breakdown voltage in air (Volt)	
	5 μm-thick buried oxide	10 μm-thick buried oxide
A single square	320-322	360-380
A 3 μm gap	305	305
A 5 μm gap	312	310
A 7 μm gap	316	315
A 9 μm gap	322	320

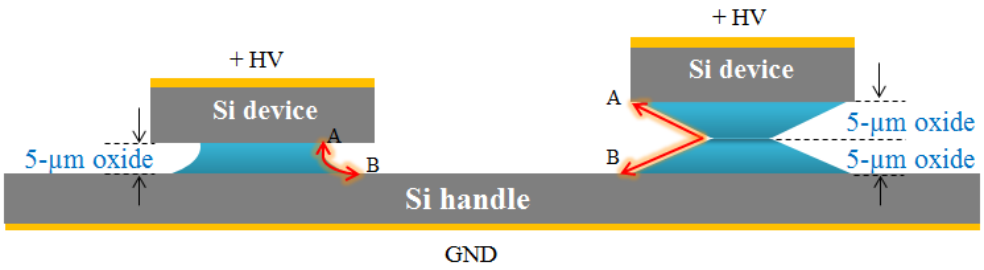


Figure 8.11 – Diagram of a SOI-built test device with a single square electrode used for the surface breakdown investigation in relation to the effect of thickness and surface profile of insulators, resulting in different triple junction geometries and surface breakdown path length (A-B).

For initial trapping, only the RF electrode was connected to the high-voltage AC signal while other electrodes were grounded. With an applied AC voltage below the breakdown thresholds of 320 V, the localized sparks or damages along the gaps where any untrapped particles stuck between two electrodes are shown in Figure 8.12. Moreover, the sparks at sharp corners causing the partial gold layer removal in Figure 8.13 were observed. With this damage

level, the trap chips were not completely destroyed. However, a severe case of catastrophic breakdown to the electrodes when the applied voltage was beyond the breakdown voltage in air of ≈ 320 V is shown in Figure 8.14.

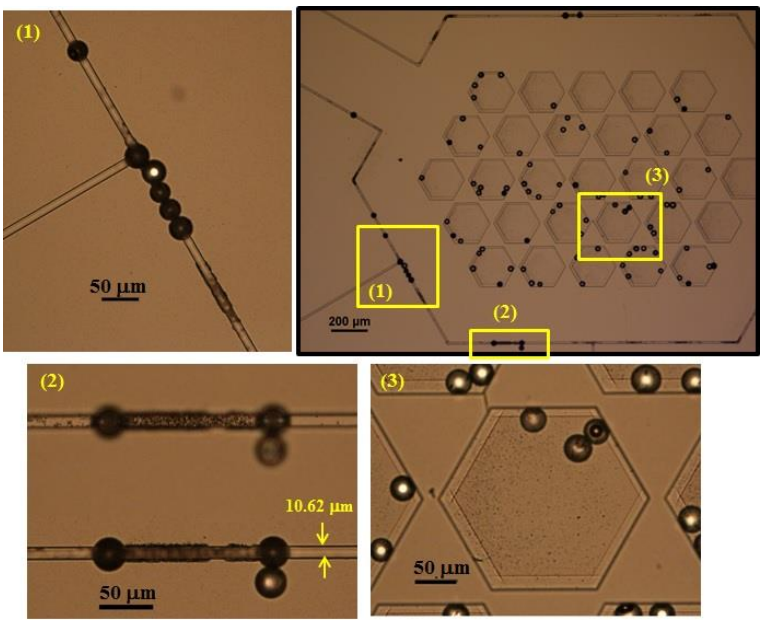


Figure 8.12 – Low level breakdown in a 2D lattice trap under test at an applied AC voltage of 250 V. The localized spark/arc along the microgap where any untrapped particles stuck between two electrodes (inset 1 and 2) and inside the recessed hexagonal lattices (inset 3).

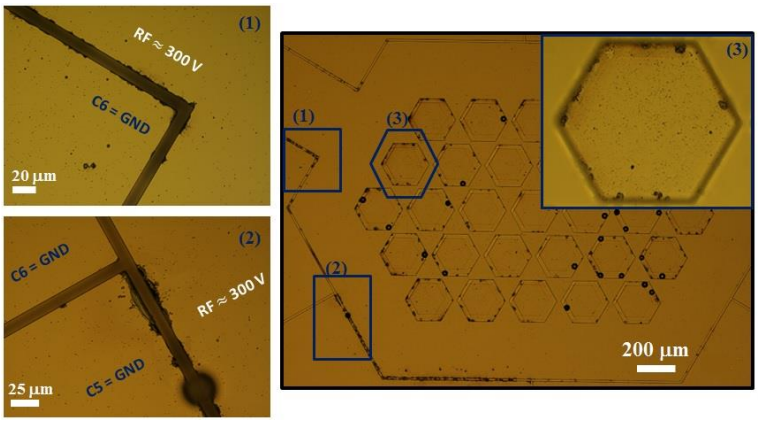


Figure 8.13 – Breakdown in a 2D lattice trap under test at an applied AC voltage of 300 V. Insets: (1) The localized spark/arc at sharp corners. (2) The partial gold layer removal along the gap. (3) The burnt residue of insulator at the hexagonal lattice site.

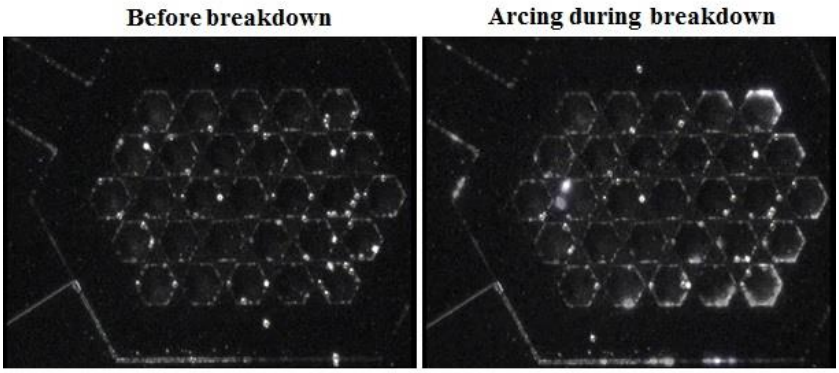


Figure 8.14 – A severe case of catastrophic breakdown occurred when the voltage applied to the RF electrode exceeded the breakdown voltage in air over microgaps at ~ 320 V. A white glow or sparking/arcing around the outer hexagonal lattice sites and along microgaps was observed.

8.3.2 Trap electrode capacitance

The capacitance of a single RF electrode as shown in Figure 8.15 consists of two dominant capacitances: the capacitance C_1 between the RF and the surrounding DC electrodes, and the capacitance C_2 between the RF electrode and the handle Si layer serving the ground plane. A simple parallel-plate capacitor model is given by the expression below.

$$C = k\varepsilon A/d \ . \tag{8.1}$$

where A is the overlapping surface area of two plates, d is the distance between the plates, k is the dielectric constant of the material and ε is the permittivity in the gap.

Assuming a simple model of parallel-plate devices in Equation (8.1) is used to estimate the capacitance between two parallel-conductive electrodes separated by an air gap (C_1) or an insulator (C_2) of the microtrap structure as shown in Figure 8.15. For C_1, a capacitance of two microstrips separated by an air gap is computed with the overlapping surface area (A) equivalent to the sidewall surface area in the trench width ($d = 10$ μm) between these two electrodes and k equal to 1. The capacitance C_2 is calculated from the two parallel plates (RF electrode and ground plane) separated by a buried oxide layer ($d = 10$ μm, $k = 3.9$). Using this model, the total capacitance of the RF electrode is estimated to $C_{Total} = C_1 + C_2 \approx$ 19 pF, as reported by Sterling [135].

The C-V measurements were performed with a LCR meter[15] across different frequency ranges and test samples. The average value of the measured capacitance across micron-scale air gaps C_1 is found to be ≈ 27 pF which is uncorrelated to the modelling value expected to be ~ 0.26 pF. In Table 8.4, the experimental results are compared with the calculations from the two-parallel plate capacitor model. In this calculation, the overlapping surface area of two electrodes (A) is roughly estimated using a single microstrip model with the RF electrode length $l \times d_2 \approx 10 \times 0.40$ mm^2 illustrated in Figure 8.16, due to the fact that the actual RF electrode is formed in hexagonal lattices. The average values of the capacitance C_2 are approximately 12.43 pF and 34.71 pF for the buried oxide thickness of 10 μm and 5 μm, respectively. This result suggests that a simple parallel-plate capacitor model is not suitable for predicting the capacitances of microtrap structures. However, based on the study of influence of insulator thickness on electrical characteristics of the microtrap, the capacitance reduction in the microstructure with a thicker oxide layer is proven to be more favourable for the RF helical resonator to maximise the quality factor (Q-factor) which is inversely proportional to the trap capacitance. Also a microtrap with a thicker oxide layer exhibits higher breakdown voltage reported in Section 8.3.1.

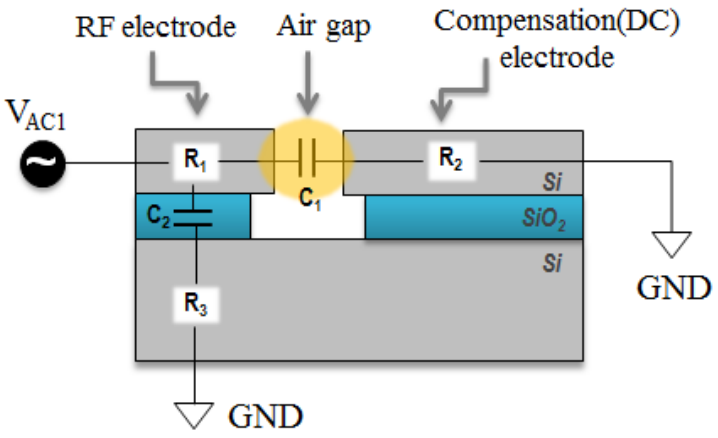


Figure 8.15 – Schematic of the resistance and capacitance model of a SOI-built ion trap.

[15] Stanford Research Systems Model SR720 LCR meter (Measurement range in C+R mode for C 0.0001 pF – 99999 μF, R 0.00001 – 99999 kΩ)

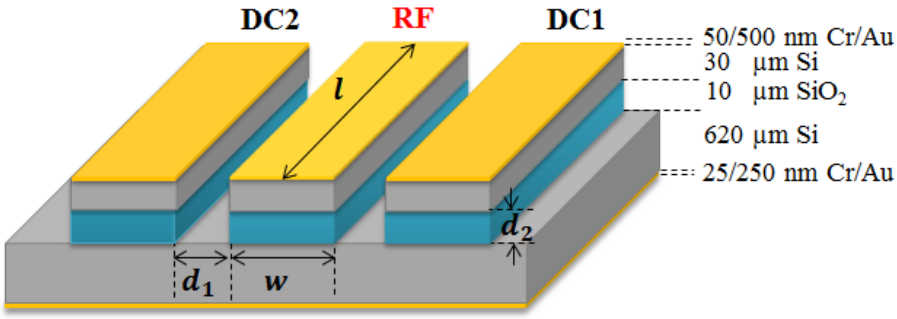


Figure 8.16 – Schematic of a simple SOI-built structure used to calculate a RF electrode capacitance C_2 between a metal-Si strip and ground layer separated by an insulator (SiO_2): $w = 0.4$ mm, $l = 10$ mm, $d_1 = d_2 = 10$ µm.

Table 8.4 – Measurement of capacitance on the SOI-built devices with different oxide thicknesses (5 µm and 10 µm).

Device	Dimension	Oxide thickness (µm)	Average capacitance C_2 (pF)	
			Calculation	Measurement
2D hexagonal lattice traps	Hexagonal lattice 1.8×2.5 mm	5	27.62	34.71
		10	13.81	12.43
SOI-built test samples	A single square 0.5×0.5 mm	5	1.73	2.50
		10	0.86	1.72

8.3.3 Initial trapping

The experimental results of the electrical breakdown measurement suggest that the maximum AC voltage which can be applied to the trap electrodes is limited to ≈ 320 ± 10 V by the electrical breakdown of air as a function of electrode separation (10 to 30 µm). Hence, the operating voltages of these micro-trap devices were limited to 300 V to avoid the breakdown damage which may result in the dielectric degradation, or even destroy the trap. Under the initial experimental trials, electrostatic charge (also known as triboelectric charge) on trapped microspheres was unknown. To facilitate trapping of unknown charge particles, the highest voltage (resulting in deeper trapping potentials occurs) before

the breakdown of 300 V at a drive frequency of 1600 Hz suggested by the numerical simulation (refer to Test#25 in Table A.1) was used as the starting point. After several unsuccessful attempts to trap a single 30 μm glass microsphere with this initial operating condition, lowering the drive frequency to 1100 Hz (Test#26) at a fixed RF voltage of 300 V resulted in increasing the trap depth with sacrificing fidelity. Trapping 30 μm glass microspheres was achieved within a short lifetime. The experiments were repeated under the same operating condition several times. However, the particle lifetime was still limited to 15-60 seconds. It was suspected that the stability parameter of the trap approached the boundary of the stability region at $q_{max} = 0.908$. Other parameters such as insufficient trap depth and large deviation of the Q/m ratio between the experiment and the simulation may lead to the particle loss.

To improve the particle-trapping lifetime, the trap depth and stability parameter need to be improved. To achieve this, there is a trade-off between increasing the trap depth and shifting the stability parameter q from the boundary of the stability region $q_{max} = 0.908$ (where a = 0) towards the combination of the drive (AC) voltage and frequency. This relation is described by the stability parameter q in Equation (3.18) and the pseudopotential in Equation (3.32). To obtain an optimal stability q parameter, the drive frequency needs to be lower while maintaining the drive voltage as high as possible for sufficient trap depth. Since the electrical air breakdown voltage of microgaps is 320 ± 10 V, increases in voltage is not an option. Therefore, lowering the drive frequency is only applicable in this case. The drive frequency was slowly decreased from 1100 Hz to 1000 Hz where the trapping life time was improved by up to five minutes. As the drive frequency was continuously decreased to 700 Hz, a longer particle lifetime of up to 60 minutes was achieved until the high-voltage source (the oil-filled transformer and the amplifier) had to be turned off for safety purposes. This result indicates that the actual values of Q/m ratio of trapped particles are lower than the initial values that are used in the simulations (Test#25-26). The traps were characterised under various operating conditions listed in Table 8.5. The minimum voltage that still retains a stable trajectory with lifetime of several minutes and low particle loss rate is limited to 150 V at a drive frequency range of 450-500 Hz. A single glass particle of 30 μm in diameter was stably trapped in a 2D hexagonal lattice trap as shown in Figure 8.18 and Figure 8.19

taken from different angles. Other parameters such as the secular frequencies and the Q/m ratio are discussed in detail in the following sections. In addition to the excess micromotion issues that occurred in the PCB-ring electrode trap (refer Section 8.2), this incident was also observed when trapping microparticles in a 2D lattice trap as shown in Figure 8.17. The excess micromotion from the noise coupling on the ground trace caused the particle to oscillate strongly and move radially off from the trap centre (it is supposed to lie at a RF nil or pseudopotential minimum).

The particle's motion in a 2D lattice trap was monitored using both a standard USB microscope camera (up to 100x magnification) as shown in Figure 8.18 and a standard CCD camera attached to high-magnification objective lenses and interfaced with a video capture device as shown in Figure 8.19. Both cameras are capable of capturing the particle's position by frame (still images) and video recording. In this experiment, the particle's position in each captured frame from the video recording associated with the use of an object with known size for calibration was used to estimate the trap height. The measured trap height is ~ 82-95 μm above the electrode surface which deviates from the simulation data of 117 μm. Comparing the simulation to the measurement, the trap height is not in good agreement. Referring to the simulated trap height of 117 μm (see Section 4.5.2), the measured trap height is ~ 22-35 μm less. It is suspected that this relates to the absence of the gravitational force compensation, and the limitations of the imaging system and the measurement method described above. In addition, the CCD camera setup in Figure 7.6 was slightly tilted (a slight down angle) by ~ 10-20 degrees due to the trapping plane lying some distance below the camera focal plane. With this small degree of tapering angle, the measurement error in trap height may be affected in some degree.

Table 8.5 – Operating parameters of a 2D hexagonal lattice trap, operated in air, using 30 μm diameter glass microspheres.

Trap dimension	Operating parameters		Experimental results		
	Voltage (V)	Frequency (Hz)	No. of trapped particle(s)	Ion height h (μm)	Particle life time
2D hexagonal lattice traps with the ion-ion separation of 270.5 μm	300	1600	Not able to trap	-	-
	300	1100	1	-	15-60 seconds
	300	1000	1	-	Up to 5 minutes
	300	700-800	1	92	60 minutes[1]
	250	600-700	1,2	90	60 minutes[1]
	200	500-600	1,2	88	60 minutes[1]
	150	450-500	1	-	Up to 10 minutes
	<150	400	Not able to trap	-	-

[1] Terminated high-voltage power supply

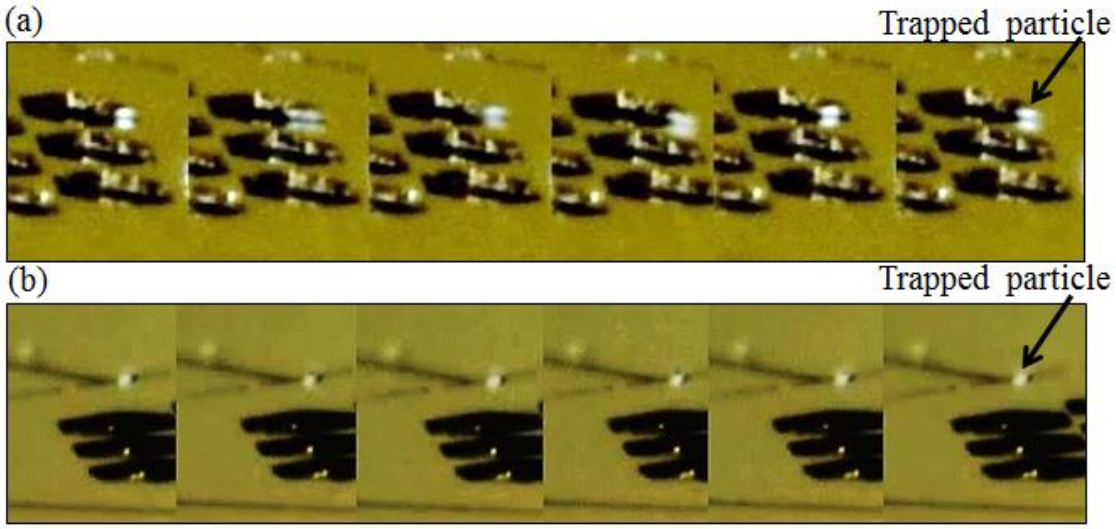


Figure 8.17 – Images captured by frame mode of a single 30 μm microsphere trapped above a 2D hexagonal lattice trap. (a) The particle oscillated widely due to electrical noise coupling on the ground system from the high-noise light source. (b) After the problematic light source was removed, strong oscillation disappeared that leads to stable particle trapping.

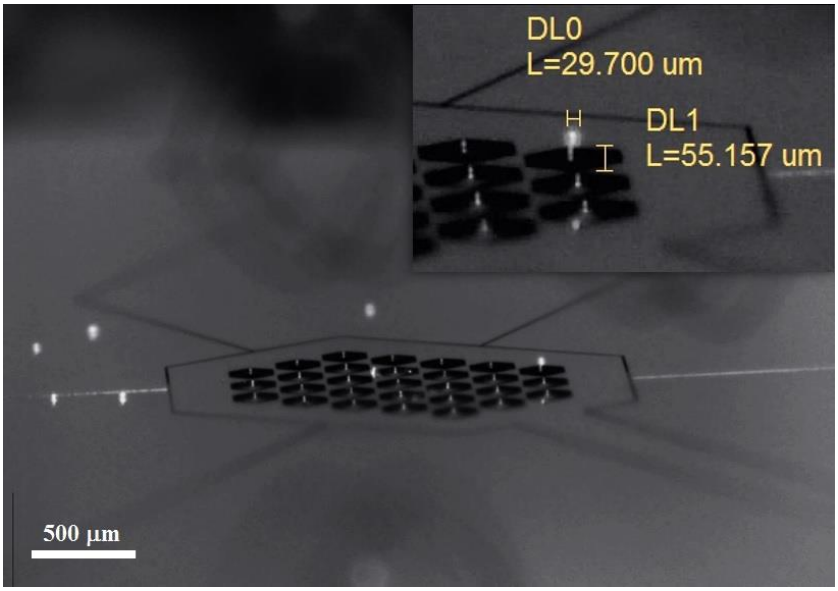


Figure 8.18 – Photograph of a single 30 µm glass microsphere trapped in a 2D hexagonal lattice trap. (In this image, the measured particle height is based on the tilt of the camera.)

Figure 8.19 – Photograph of a single 30 µm glass microsphere trapped in a 2D hexagonal lattice trap at 93 µm above the electrode surface. The measured trap height is less than the simulated value of 117 µm due to a small tilt angle of the CCD side camera.

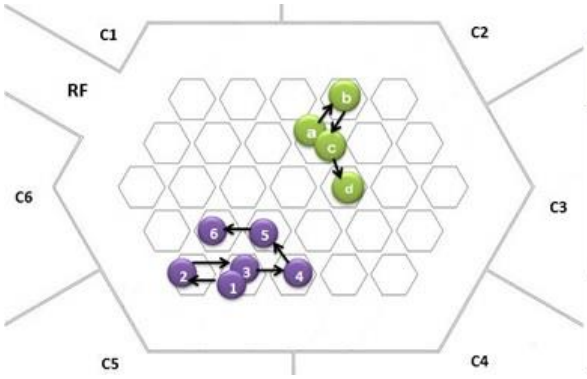
8.3.4 Shuttling operation

In this experiment, shuttling of microparticles utilises a similar approach to the rudimentary shuttling of ions presented in Section 6.3.2. To perform shuttling operation between distinct trap sites in a 2D lattice trap, the initial AC voltage applied to the RF electrode was reduced to minimise the potential barrier between the lattice sites. Once this potential barrier became sufficiently low, a particle was then able to shuttle towards the desired regions. Shuttling directions were controlled by the polarity of DC voltages supplied to the surrounding compensation (DC) electrodes associated with type of charge on a particle. Once a shuttled particle entered a new trap site, the applied AC voltage was increased to its initial value to ensure that the RF pseudopotential resumed to the stable trapping condition with maximum trap depth. Doing this slowly moved a particle to the centre of the trap (or RF nil point).

Figure 8.20 shows the arbitrary shuttling diagram including a typical set of voltages and the voltage control sequence used for two different shuttle routes: (1)→(6) and (a)→(d). From the experimental results, it was found that ± 10 V_{DC} was sufficient to move particles through the entire array. When the particle was shuttled to lattice traps at close proximity to the compensation (DC) electrodes, an applied DC voltage must be lowered to ± 8 V to prevent hoping of the particle to unwanted trapping sites and to make the shuttling more controllable and precise. On the other hand, a larger DC voltage up to ± 13 V was required when the shuttles took place at the centre of the array. The critical point of successful shuttling is to have a sufficiently low potential barrier but still retain sufficient trap depth to prevent the particle loss. Figure 8.21 and Figure 8.22 demonstrate multiple shuttles in two different routes the experimental results of multiple shuttles followed the route (1)→(6) and (a)→(d).

It was realized that a 2D shuttling between neighbouring lattice traps was much simpler in ambient air with microparticles than in vacuum with ytterbium ions. The main issue that limits a series of shuttling was a wrongly set voltage. In actual practice, a high-voltage AC signal supplied to the RF electrode was adjusted by turning up/down the power amplifier gain knob with coarse resolution of ~ ± 20 V. With this manual adjustment, a slightly excessive voltage exceeding the breakdown voltage at 320 ± 20 V by chance can

result in damage or dielectric degradation. At low applied voltage below 200 V, Particle losses due to insufficient trap depth may occur. To further improve shuttling performance, the use of a computer-based system in controlling the voltage control electronics more accurately and precisely is necessary. This flexibility also accommodates more complex shuttling, requiring the voltages applied to each electrode to be altered simultaneously or in a time sequence.



AC Voltage RF Start	Shuttle sequence	DC Volatge C1	C2	C3	C4	C5	C6	AC Voltage RF End
300 → 200	1 → 2			-10			+10	200 → 300
	2 → 3			+10			-10	
	3 → 4			+10			-10	
	4 → 5	+10	+10		-10	-10		
	5 → 6			-10			+10	
300 → 200	a → b		+10		-10			200 → 300
	b → c		-10		+10			
	c → d		-10		+10			

Figure 8.20 – Schematic of shuttling operation for two different shuttling routes by applying the AC/DC voltages to the RF and compensation electrodes in sequence.

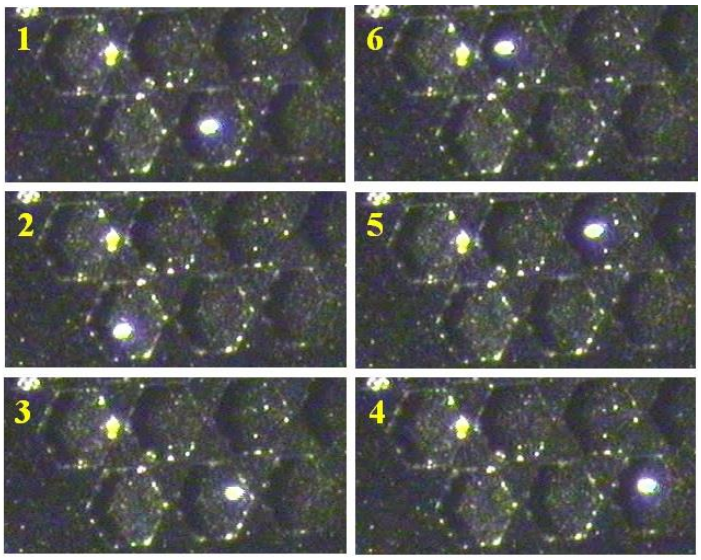


Figure 8.21 – Photographs of 2D shuttling of a single microparticle in air. Six shuttles follow the route (1)→(6) in Figure 8.20.

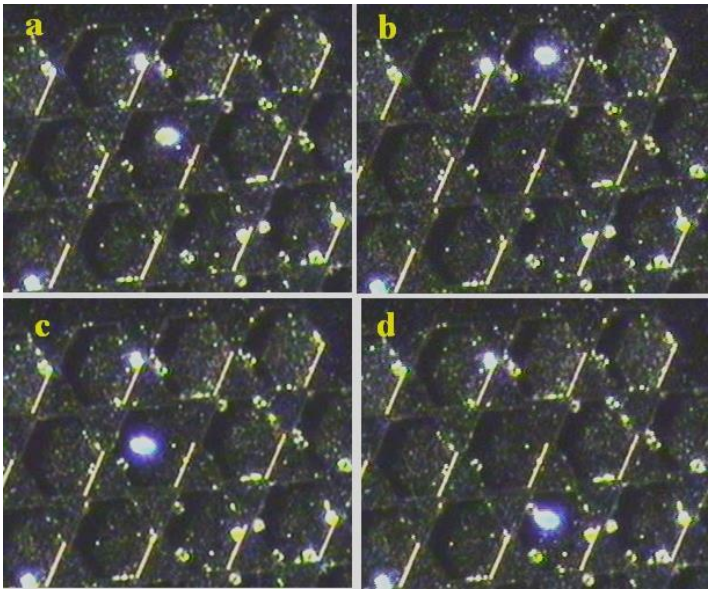


Figure 8.22 – Photographs of 2D shuttling of a single microparticle in air. Four shuttles follow the route (a)→(d) in Figure 8.20.

8.3.5 Levitation operation

A similar levitation technique to Kim et al. [112] in a planar ring electrode trap was applied to the 2D lattice trap as demonstrated below. For initial trapping, the 2D lattice trap was operated with a fixed RF potential (also called a primary AC voltage, V_{AC2}) while other electrodes were grounded. To perform the levitation, a secondary AC voltage (V_{AC2}) was supplied to the recess electrode. To shift the particle levitation height (or RF nil point) without leading to excess micromotion, it is important to strictly apply phase difference between the two AC sources by $\theta = 0°$ or 180° only. The RF nil point shifts towards the electrode surface with a zero-degree in-phase, and for a reverse direction with a 180-degree out-of-phase. The levitation height depends on the magnitude of the "ε" ratio which is the ratio of the secondary AC voltage (V_{AC2}) to the primary AC voltage (V_{AC1}).

For particles with the estimated Q/m value in the order of 10^{-4} C/kg ($Q \approx 9 \times 10^{-15}$ C, $m \approx 3.39 \times 10^{-11}$ kg, see the detailed analysis in Section 8.3.7), four combinations of the optimal primary and secondary AC voltages and drive frequencies listed in Table 8.6 were derived from the numerical simulation presented in Section 4.5.4. As previously discussed, the breakdown

voltage in air of the microtraps was found to be ≈ 320 V. This breakdown level became a critical constraint when performing the out-of-phase levitation. This is due to the fact that the voltage between the RF electrode and the recess electrode (V_{AC1} - V_{AC2}) is now the sum of two AC voltages. To achieve the levitation with stable trapping, the trap depth ≥ 50 meV and stability parameter q of ≤ 0.60 are required to avoid particle loss.

With all requirements and constraints considered, four operating conditions in Table 8.6 were determined within three categories. First, the initial trapping condition in the absence of a secondary AC voltage is in a dark blue highlight. Second, the applicable test conditions allowing the levitation both in-phase and out-phase are in a light blue highlight. Third, the inapplicable test conditions leading to a breakdown in air (V_{AC1} - V_{AC2} > 300 V) are highlighted in orange. This determination suggests that the applied AC voltage at 200 V at $\Omega/2\pi$ = 550 Hz (Test#2) is the best trade-off between the trap depth and the stability parameter q while retaining a large operating range allowing for both in-phase (levitating downward) and out-of-phase (levitating upward) experiments to be investigated at the same time. Even though the combination of voltage and frequency shown in Test#1 offers a larger operating range without the issue of breakdown in air (V_{AC1} - V_{AC2} < 320 V), the trap depth is relatively inadequate to trap (< 0.50 eV). This was observed in the previous experimental runs during the initial trapping experiments. Test#3 and Test#4 also suffer from the breakdown in air that restricts the out-of-phase experiment. Also, unstable trapping conditions indicating "*Error*" in the trap depth and the axial secular frequency (not shown in Table 8.6) occur when the ε ratio is greater than 0.4, which applies to all test cases.

Table 8.6 – Calculation of the trapping parameters of charged microparticle levitation in air based on the estimated Q/m value in the order of 10^{-4} C/kg.

Test#1				Test#2				Test#3				Test#4						
V_{AC1} = 150 V Frequency = 500 Hz				V_{AC1} = 200 V Frequency = 550 Hz				V_{AC1} = 250 V Frequency = 600 Hz				V_{AC1} = 300 V Frequency = 700 Hz						
V_{AC2} (V)	V_{AC1}-V_{AC2} (V)	Stability q	Trap Depth (eV)	V_{AC2} (V)	V_{AC1}-V_{AC2} (V)	Stability q	Trap Depth (eV)	V_{AC2} (V)	V_{AC1}-V_{AC2} (V)	Stability q	Trap Depth (eV)	V_{AC2} (V)	V_{AC1}-V_{AC2} (V)	Stability q	Trap Depth (eV)	ε ratio = V_{AC2}/V_{AC1}	Trap height (um)	Trap height offset (um)
-150	300	0.31	0.02	-200	400	0.34	0.03	-250	500	0.36	0.04	-300	600	0.32	0.04	-1.0	161.02	44.03
-135	285	0.33	0.02	-180	380	0.36	0.03	-225	475	0.38	0.04	-270	570	0.33	0.04	-0.9	156.94	39.95
-120	270	0.35	0.02	-160	360	0.38	0.04	-200	450	0.40	0.05	-240	540	0.35	0.05	-0.8	152.83	35.83
-105	255	0.37	0.03	-140	340	0.40	0.04	-175	425	0.42	0.05	-210	510	0.37	0.05	-0.7	148.69	31.69
-90	240	0.39	0.03	-120	320	0.43	0.04	-150	400	0.45	0.06	-180	480	0.39	0.06	-0.6	144.54	27.55
-75	225	0.41	0.03	-100	300	0.45	0.05	-125	375	0.47	0.06	-150	450	0.42	0.07	-0.5	140.29	23.29
-60	210	0.44	0.04	-80	280	0.48	0.05	-100	350	0.51	0.07	-120	420	0.45	0.07	-0.4	135.94	18.95
-45	195	0.47	0.04	-60	260	0.51	0.06	-75	325	0.54	0.08	-90	390	0.48	0.08	-0.3	131.52	14.52
-30	180	0.50	0.04	-40	240	0.55	0.06	-50	300	0.58	0.08	-60	360	0.51	0.09	-0.2	126.89	9.89
-15	165	0.54	0.05	-20	220	0.60	0.07	-25	275	0.63	0.09	-30	330	0.55	0.10	-0.1	122.05	5.06
0	150	0.59	0.05	0	200	0.65	0.07	0	250	0.68	0.10	0	300	0.60	0.10	0.0	117.00	0.00
15	135	0.65	0.06	20	180	0.71	0.08	25	225	0.75	0.11	30	270	0.66	0.11	0.1	111.58	-5.42
30	120	0.72	0.06	40	160	0.79	0.09	50	200	0.83	0.11	60	240	0.74	0.12	0.2	105.80	-11.20
45	105	0.82	0.06	60	140	0.90	0.09	75	175	0.95	0.12	90	210	0.83	0.13	0.3	99.34	-17.66
60	90	0.95	0.07	80	120	1.05	0.10	100	150	1.10	0.13	120	180	0.97	0.14	0.4	92.23	-24.76
75	75	0.12	Error	100	100	0.13	Error	125	125	0.13	Error	150	150	0.12	Error	0.5	Error	Error
90	60	0.15	Error	120	80	0.16	Error	150	100	0.17	Error	180	120	0.15	Error	0.6	Error	Error
105	45	0.17	Error	140	60	0.18	Error	175	75	0.19	Error	210	90	0.17	Error	0.7	Error	Error
120	30	0.19	Error	160	40	0.21	Error	200	50	0.22	Error	240	60	0.20	Error	0.8	Error	Error
135	15	0.23	Error	180	20	0.25	Error	225	25	0.27	Error	270	30	0.23	Error	0.9	Error	Error
150	0	0.40	Error	200	0	0.44	Error	250	0	0.46	Error	300	0	0.41	Error	1.0	Error	Error

Breakdown in air | Normal operating conditions | Initial trap condition with V_{AC2} = 0 V (ε = 0)

Error Unstable trapping conditions with "Error" in the trap depth and the axial secular frequency when the ε ratio > 0.4

Several experiment runs were performed using the operating parameters outlined in Test#2 predicting the change of particle levitation height within ± 25 μm (positive for motion upward and negative for motion downward). Since every newly trapped particle has its own charge Q and mass m, the simulation with the estimated Q and m values merely serves as a guideline for initial loading and trapping. It was often found that particles were trapped unstably either further away from the centre trap (RF nil point), or to significantly oscillate in all directions. To improve trap stability for a newly trapped particle with a certain charge prior to starting the levitation experiment, the drive frequency was slightly adjusted for optimum trapping (a particle was displaced to the trap centre) which in turn alters both the trap depth and stability q parameters. However, the primary AC voltage was fixed at 200 V throughout to obtain the maximum levitation height of 25 μm.

With the initial trap parameters of a primary AC voltage V_{AC1} = 200 V at drive frequency $\Omega/2\pi$ = 550 Hz, a single 30-μm diameter microsphere was trapped at ~ 93 μm above the electrode plane as shown in Figure 8.23. Next, the frequency was slightly decreased to 500 Hz where the particle was further focused towards the trap centre. The amplitude of a secondary AC voltage V_{AC2} with 180-degree phase shift was increased from 0 V to +100 V carefully to avoid the overvoltage by chance and a risk of the electrical breakdown. The particle was slowly moved in upward direction from the surface plane (see $t_0 \rightarrow t_3$) as a result of an increase in the ε ratio. To move the particle towards the electrode plane, two AC voltages (V_{AC1} and V_{AC2}) were in the same phase (zero-degree phase shift). The particle's position from varying the amplitude of V_{AC2} is shown in $t_3 \rightarrow t_8$. It was found that when V_{AC2} was further increased until $\varepsilon > +0.4$, the trap became unstable. This result is consistent with the simulation suggesting that the unstable regime of in-phase levitation starts from $\varepsilon >+ 0.3$ (refer Figure 4.16). While V_{AC2} was increased to 100-120 V resulting in $\varepsilon \approx 0.5$-0.6, the particle started to oscillate widely around the trap centre and eventually flew off from the trap.

Operating parameters

Time (t_i) = t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
ε = 0	-0.32	-0.4	0	0.2	0.3	+0.4	+0.3	0
V_{AC2} = 0 V	-64	-80	0	+40	+60	+80	+60	0
Trap height shifting (μm) from initial trap height at 93 μm								
Simulation	+14.52	+18.95	0	-11.20	-17.66	-24.76	-17.66	0
Experiment	+11.25	+15.00	0	-7.50	-11.25	-15.00	-13.50	0

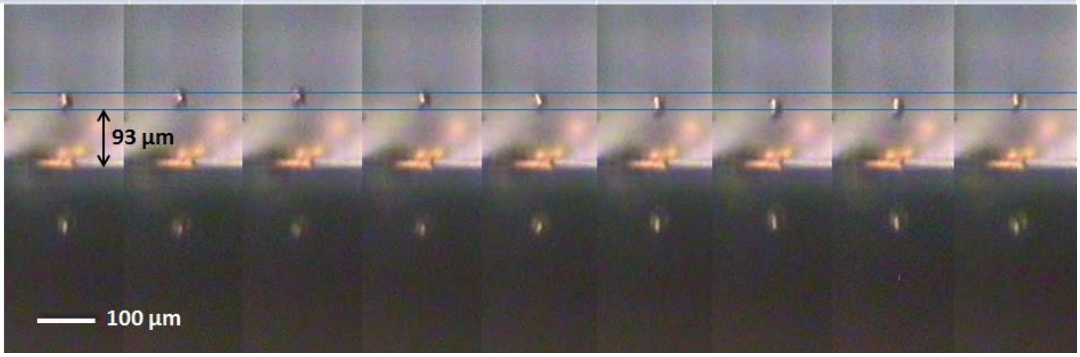


Figure 8.23 – Photographs of microparticle levitation (RF nil point shifting) in air. At V_{AC1} = 200 V at $\Omega/2\pi$ = 550 Hz and a varying voltage V_{AC2} = ± 80 V (Test#2), the levitation height ranges ± 15 μm from the initial trap height at ~ 90-93 μm.

8.3.6 Secular frequency measurement

In this experiment, the radial secular frequencies ($\omega_{x/y}/2\pi$) were measured using a technique called "*tickling*" [83]. This technique is to apply an auxiliary AC waveform of a small potential (typically 0.5-2.0 V) to the control (DC) electrodes in order to induce the resonance excitation. The resonance condition is achieved by matching the frequency of an auxiliary potential to the secular frequency of the particle. Experimentally, this small AC signal (a "*tickle*") is swept through a range of frequencies to observe the resonant effect. Once the scan frequency (f_{osc}) matches the secular frequencies of the trap, the resonant excitation takes place and the particle's motion gets excited and oscillates widely.

From the initial trapping condition of 300 V at $\Omega/2\pi$ = 700 Hz, an auxiliary potential of 0.5 V was applied to one of the compensation electrodes which was in close proximity to the trapped particle. A weakly oscillating particle was observed at a very low frequency range of 3-5 Hz. Then the particle started to oscillate strongly at the scan frequency f_{osc} range of 7 to 16 Hz. After that, the scan frequency was continuously swept through the frequency range up to 100 Hz. The resonant effect on the particle's motion disappeared when the scan frequency f_{osc} was greater than 30 Hz. The resonant effect was monitored through the CCD camera mounted at the top window to observe the radially oscillating particles under the resonant effect.

To improve the accuracy in this measurement, the experimental runs were repeated several times on the same trapped particle and also different batches by searching the scan frequency f_{osc} in both descending order ($f_{osc} > \omega_{x/y}/2\pi$) and ascending order ($f_{osc} < \omega_{x/y}/2\pi$) several times. The resonant effect was monitored through the real-time recording CCD camera and the secular frequencies were determined by the scan frequency at the strongest oscillating effect.

To improve the ability in observing the resonant effect on micrometre-scale particles, several techniques were explored. Firstly, increasing amplitude of a small AC sinusoidal (sine wave) potential from 0.5 V to 2.0 V resulted in a stronger excitement in the particle's motion, but any applied voltage greater than 2.5 V caused particle losses. Secondly, the effect of the signal waveform (e.g. a sine wave, square wave) on the resonance effect was investigated.

The initial assumption was that the sharp edges in the square-wave signal produce a sharp resonance effect. However, no significant result between two different signal waveforms was observed. Since the secular frequencies of the particle were determined by the observation of the strongest oscillating condition, the improvement in the particle motion imaging and tracking systems is necessary to obtain a more accurate and precise result. Based on the measured radial secular frequencies $\omega_{x/y}/2\pi$ = 7-16 Hz corresponding to the operating voltage V_{RF} = 300 V at $\Omega/2\pi$ = 700 Hz, it is however possible to roughly estimate the amount of charges on the particles, which is described in detail in the following section.

8.3.7 Charge-to-mass ratio approximation

The stability of charged-particle motion in a quadrupole ion trap is determined by the dimensionless Mathieu stability parameters (a, q) depending on its charge-to-mass (Q/m) ratio, the trap geometrical size, and the operating as derived in Equation (3.18). From this relation, a particle with a specific value of the charge-to-mass ratio can be stably trapped in the appropriate combination of the operating voltage and frequency. To retain its stability, the stability parameters (a, q) need to fall inside of the stable regimes of the Mathieu stability diagram as shown in Figure 3.4 and Figure 3.5.

For charged particle trapping, the values of charge Q and mass m of individual trapped particles are not identical. Following the derivation in Equation (3.22) with a given trap operating condition and trap size, it gives the particle charge-to-mass (Q/m) limitation where the stability parameter q is at the stability boundary (i.e. a = 0, q = 0.908 for the first boundary region). The upper limit of the charge-to-mass ratio is inversely proportional to the driving voltage (V_{AC}) and is inversely proportional to the square of the driving frequency ($\Omega/2\pi$). Therefore knowing of charge to mass ratios provides insights into the relationship between the trap operating parameters and trap stability.

First, the knowledge of the particle's properties such as density, shape and size can be used to calculate the mass of the particle. Particle mass density ρ is defined as the mass m per unit volume v (kg/m^3). The mass of a spherical object can be found by diving its mass density by its volume, $v = (4/3)\pi r^3$, where r is the radius of the sphere. A glass microsphere used in

the experiments has a diameter of 30 μm and a mass density of 2400-2600 kg/m^3. So the mass m of a glass microsphere is calculated to be ≈ 3.39-3.68 × 10^{-11} kg. Next, the charge on a single particle needs to be determined. Besides measuring the charge using a Faraday cup, the combination of numerical calculation and experimental methods can be used to estimate the charge-to-mass (Q/m) ratio of the particles. The experiment was conducted to calculate the Q/m value of trapped particles using the "*boundary ejection*" method (or a "*mass-selective instability scan*") [83]. Under normal operating conditions, the AC voltage is fixed and the frequency ($\Omega/2\pi$) was slowly decreased until the ejection frequency ($\Omega_{eject}/2\pi$) was found, where the particles trapped with stable trajectory up to q_z of 0.908 (where $a = 0$) were ejected from the trap. With the observation of the ejection frequency ($\Omega_{eject}/2\pi$), the Q/m ratio can be obtained from

$$\frac{Q}{m} = \frac{q_{eject} r_0^2 \Omega_{eject}^2}{2V}, \tag{8.2}$$

where $q_{eject} = q_{z\_max} = 0.908$ (for an ideal quadrupole trap).

Since the theoretical analysis of ion's motion may not exactly apply to microscopic particle trapping particularly in air, the addition of the air damping effect may enlarges and shifts the stability regions in the parameter space as reported in Spann et al. [141]. According to the damping analysis discussed in Section 4.6, the computed drag coefficient b of the experimental condition particularly used in this study (a particle size of 30 μm, a given frequency range of $\Omega/2\pi$ = 500-1000 Hz) was found to be relatively small, b = 0.05-0.10. This value exhibits only a small effect (weak damping where $b \ll 1$) and has no significant effect on the shift of the stability boundary. Therefore, the original stability boundary q_z = 0.908 is also valid for microparticle trapping in air and can be used to estimate the Q/m value. Table 8.7 presents the experimental results by observing the ejection frequencies of several trapped particles together with the numerical calculation of the charge-to-mass ratio using Equation (8.2). This study suggests that the charge-to-mass (Q/m) ratio of the trapped particles (glass microspheres of 30 μm in diameter) is in the range of 2.2 - 3.1 × 10^{-14} C/kg. The charge Q on the particle confined in the 2D lattice trap is varied between 7.44 × 10^{-15} C to 1.14 × 10^{-14} C .

Table 8.7 - Charge-to-mass (Q/m) ratio approximation of 30 μm diameter glass microspheres using the boundary ejection method.

Batch#	Experiment			Calculation		
	Voltage V_{AC} (V)	Frequency f_{AC} (Hz)	$\Omega_{eject}/2\pi$ (Hz)	$\frac{Q}{m} = \frac{q_{eject} r_0^2 \Omega_{eject}^2}{2V_{AC}}$ × 10^{-4} (C/kg)	Charge Q_1 of m_1 × 10^{-15} (C)	Charge Q_2 of m_2 × 10^{-15} (C)
1	150	500	396	2.56	8.86	9.42
2	150	500	415	2.81	9.53	10.30
3	200	600	468	2.68	9.09	9.86
4	200	600	503	3.10	10.5	11.40
5	250	700	499	2.44	8.27	9.98
6	250	700	473	2.20	7.44	8.08
7	300	800	527	2.27	7.70	8.36
8	300	800	537	2.36	7.99	8.68
			Average	2.55	8.65	9.39

Soda lime glass dry spheres:
Diameter = $2R$ = 30 μm
Density, ρ = 2.4-2.6 g/cm^3 = 2400-2600 kg/m^3
Volume, $v = 4/3\ \pi\ R^3$
Mass, $m = \rho \times v$
Mass, m_1 = 3.39 × 10^{-11} kg with ρ_1 = 2400 kg/m^3
Mass, m_2 = 3.68 × 10^{-11} kg with ρ_2 = 2600 kg/m^3

Trap operating conditions:
Trap size (or trap height), r_0 = 117 μm
The stability boundary, q_{eject} = 0.908
The ejection frequency = $\Omega_{eject}/2\pi$

8.4 Problems of the Y-junction trap design

It should be mentioned that due to a fault in the design of the Y-junction trap, the fabricated devices were not tested. That is the problematic of two RF rails in the bottom linear section (labelled B and C) remaining separate in order to allow electrical connection to the central DC electrode, as shown in Figure 8.24. This results in two different path lengths for the RF electrode. A more detailed study of the design fault of the Y-junction trap was conducted by Sterling [135]. The phase difference between the two arms (from points A→B and A→C) of the Y-shaped junction trap is a result of the different path lengths and the different impedances. In this study, a total RF phase difference, also called phase angle (ϕ)

in degrees, was numerically calculated to be $\emptyset_{total} \approx 1.7$ degrees. The induced micromotion from a phase angle of one degree contributing to an increase in the minimum ion temperature from mK to the order of 1 K is also reported in Berkeland et al. [225]. In addition, it is impossible for this excess micromotion to be compensated using DC compensation voltages applied to the neighbouring DC electrodes. Therefore the presence of micromotion has potential to affect the trap performance, particularly successful adiabatic shuttling operations. A similar derivation of problematic Y-junction trap was also discussed in the thesis of Britton [226].

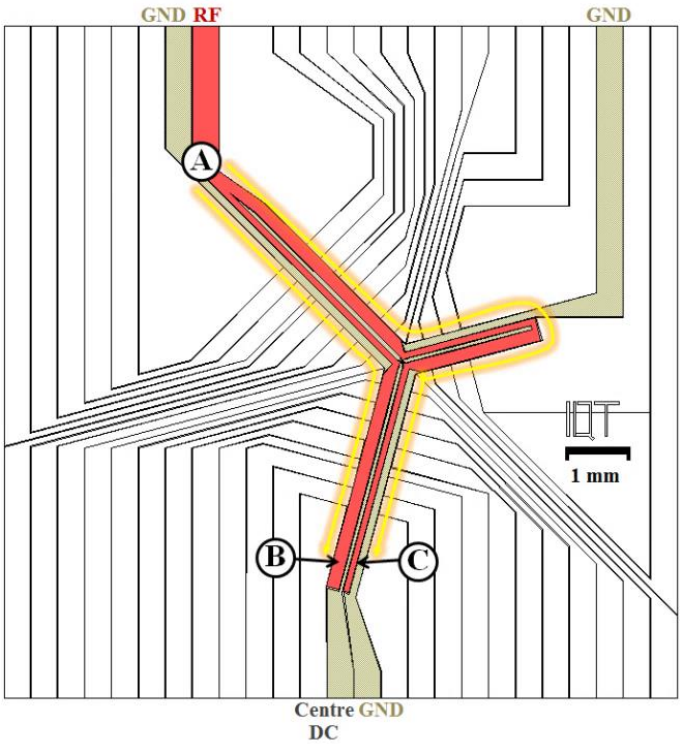


Figure 8.24 – The different RF path lengths (from point A→ B and A→ C) in a Y-shaped junction trap result in the phase mismatch between the two arms of the RF electrode.

For the problematic Y-junction trap, one workaround is to connect points B and C together using either a wire bonding to resolve the issue of splitting the RF electrode path at the lower leg of the Y-junction geometry. However, the resultant phase mismatch at

the junction, approximately $\emptyset_{junc} \approx 0.35°$ using a similar calculation, can be pronounced. Hence the most efficient solution to mitigate this issue and not to create some other problems is to apply a different method of fabrication. The buried wire and vertical interconnect access (via) techniques discussed in Section 2.4.5 allowing all electrical contacts to isolated electrodes can be applied in the future fabrication.

8.5 Conclusion

This work represents the experimental effort to achieve microparticle trapping and manipulation in the 2D hexagonal lattice trap fabricated on a SOI substrate. The experiments were performed in a closed-air environment under atmospheric pressure. The study on the breakdown characteristics of the SOI-built test devices suggests that the electrical breakdown across a micron-sized electrode gap is the dominant breakdown mechanism for the microtrap chips operated in air. For the 2D lattice trap with the smallest electrode spacing of 10 μm, the measured breakdown voltage is approximately 320 ± 10V. Hence, the maximum AC voltage of 300 V employed during the course of this work is within safe limit to avoid damaging the microtrap chips due to the breakdown.

Experimental realisation including a reliable trapping and three-dimensional (3D) control over microparticle's motion (i.e. shuttling between distinct lattice sites in the x-y plane and levitation in the z-plane) of the 2D lattice trap was successfully demonstrated. Under typical operating conditions of an applied AC voltage range from 150-300 V and the frequency range from 500-800 Hz, the 2D lattice trap demonstrated stable confinement of glass microspheres of 30 μm diameter. The longest trapping lifetime up to 60 minutes was achieved until the high-power AC source (the oil-filled transformer and the power amplifier) had to be turned off for safety reasons. Microspheres were trapped at about 90 μm above the electrode surface. This measured particle height is about 22-35 μm less compared to the simulation result, predicting a particle height of 117 μm. Deviation of the experimental result from the simulation

is suspected to be related to the absence of the gravitational force compensation, and the height measurement based on the tilt of the camera.

A 2D shuttling of microparticles between neighbouring lattice traps utilising a similar approach to the rudimentary shuttling of ions was demonstrated. This was achieved by controlling the potential barrier on the RF electrode and the shuttling path depending on the polarity of DC voltages supplied to the surrounding compensation (DC) electrodes associated with the charge type (positive or negative) on the particles. After a series of experimental runs, this shuttling operation was found to be much simpler in ambient air with microparticles than in vacuum with ytterbium ions. The multiple shuttles throughout the entire the trap were demonstrated.

A similar technique for microparticle levitation in a planar ring electrode trap [112] was experimentally investigated in the 2D lattice trap. For initial trapping, the trap was operated with a primary AC voltage (V_{AC1}) applied to the RF electrode while other electrodes were grounded. The *in situ* levitation technique is of RF nil point shifting at varying heights perpendicular to the surface plane with the addition of a secondary AC voltage (V_{AC2}). To shift the particle height (or RF nil point) without leading to excess micromotion, it is important to strictly apply phase difference between the two AC sources by a phase shift of zero-degrees or 180 degrees only. The levitation height depends on the magnitude of the ε ratio of the secondary and the primary AC voltages. For V_{AC1} = 200 V at frequency $\Omega/2\pi$ = 550 Hz, the microparticles were successfully levitated either towards (in-phase, $\theta = 0°$) or away (out-of-phase, $\theta = 180°$) from the electrode surface with the maximum levitation height of 15 μm, which corresponds to the maximum ε ratio of 0.4 (varying V_{AC2} between 0-80 V). A further increase in the ε ratio leads to the development of instability (in-phase mode) and the breakdown in air over micro-gaps (out-of-phase mode).

The secular frequencies were measured using a technique called "*tickling*" employing the observation of resonance condition by matching the frequency of an auxiliary small oscillating voltage (a "*tickle*") to the secular frequency of the particle. In this experiment, an auxiliary small oscillating voltage of 0.5 V was applied to one of the compensation (DC) electrodes to induce the resonance excitation. This small AC signal was swept through a range

of frequencies to observe the resonant condition. If the particle is in resonance with the tickle frequency, the particle's motion gets excited and oscillates widely. This response was monitored through CCD camera. For V_{AC} = 300 V at $\Omega/2\pi$ = 700 Hz, the observed secular motional frequencies of the trapped particles is approximately 7-16 Hz.

A technique called a "*boundary ejection*" method (or a "*mass-selective instability scan*") was used to estimate the charge-to-mass ratio of trapped particles. In this experiment, for a given AC voltage, the drive frequency ($\Omega/2\pi$) was slowly decreased until it approached the ejection frequency ($\Omega_{eject}/2\pi$) where a particle was ejected from the trap due to the fact that its stability parameters fall outside of the stability boundaries (i.e. $a = 0$, $q_z = 0.908$). The charge-to-mass (Q/m) ratio can be calculated with knowledge of the observed ejection frequencies. This study suggests that the charge-to-mass (Q/m) ratio of the trapped particles (30 μm diameter glass microspheres with density of 2400 - 2600 kg/m^3) is ~ 2.2 – 3.1 × 10^{-4} C/kg. Hence, the charge Q on the particle varies between 7.44 × 10^{-15} C to 1.14 × 10^{-14} C. In addition, it was also found that the buried oxide thickness (i.e. 5 μm and 10 μm) and the metal electrodes material (i.e. gold and aluminium) do not affect the overall microparticle trap performance. However, a lower surface breakdown (flashover) was observed on the trap devices fabricated on the SOI substrate with a 5 μm-thick buried oxide.

The overall experimental setup is proven to be capable of performing basic operations including trapping, shuttling and levitation of charged microspheres in air. However, accurately performing and high-precision measuring in more comprehensive studies (i.e. the secular frequency, particle levitation height, series of shuttling, and stability analysis under damped condition) is limited in the present experimental setup. Improving experimental apparatus and measurement techniques, in turn, allows achieving better performance and measurement accuracy. In addition, a fault in the design of the Y-junction trap associated with the existence of RF phase difference between the RF electrodes in each junction leg, leading to excess micromotion is reported. As a result, this would require modifying the existing design and the fabrication process. These are discussed in more detail in the Chapter 9.

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Chapter 9

Conclusion and future work

9.1 Conclusion

This thesis presents the development of microscopic surface-electrode ion traps (SEITs) towards scaling ion-trap architectures for quantum computation and information processing. Scaling of surface-electrode ion traps was addressed by the implementation of microfabrication techniques. Design, analytical and numerical analyses, fabrication, experimental apparatus, key operations and electrical characteristics of the proposed ion-trap chips have been conducted across collaborative research groups as detailed in the acknowledged contributions. In this work, this performance of the traps has been assessed in two regimes - ion trapping in ultra-high vacuum (UHV), and charged microparticle trapping in ambient air.

The first part of this thesis describes design of the proposed surface-electrode ion traps including a Y-junction trap and a two-dimensional (2D) hexagonal lattice trap, based on the work of Robin Sterling. Numerical field simulations of the trap electrodes based on the boundary element method (BEM) solver are used in optimisation design. With pseudopotential approximation, the simulated electric potential of the trap electrodes are numerically analysed the key trapping parameters (i.e. operating voltage and frequency, pseudopotential well depth, secular frequency and trap height). Based on these, the computed datasets of the trapping parameters are beneficial for gaining detailed insight of the trapping

mechanisms of ions and charged particles in the fabricated traps prior to the experimental measurements.

The processing steps involved in the fabrication of the devices include photolithography, etching, and metal evaporation. The devices were fabricated on SOI substrates with different buried oxide thicknesses (i.e. 5 μm-thick and 10 μm-thick) and different metals for the finished electrodes (i.e. gold and aluminium). First, the electrode pattern was transferred onto the SOI substrate using standard photolithography. The exposed Si device layer was then etched away using DRIE process followed by the oxide etching (i.e. wet or dry process). At this step, the trap electrodes and isolation trenches were completely formed on the SOI substrate. The patterned Si/SiO_2 electrodes were then coated with Cr/Au layer. To complete the fabrication, the backside of Si handle wafer was coated with a thin layer of Cr/Au. The metallisation on both the front side and backside of the microtrap chips is used for making good electrical contacts and reducing trap resistance. This also helps preventing any subsequent oxidation on bare Si which is known to be developed quickly in air after a few hours. Charging of exposed dielectrics near trapping regions can accumulate stray charge that perturbs the trapping potentials and leads to uncontrolled micromotion or ion heating. As trap sizes are reduced, surface-electrode traps can be particularly prone to this issue. To minimise charging effects in the proposed traps, the buried oxide areas at the locations of isolation trenches between electrodes were completely removed. The occurrence of undercut from chemical wet etching can be an added benefit for a more effective shield of exposed dielectric surfaces.

The main issue that has to be addressed to ensure successful fabrication is to identify the most suitable oxide etching process for two different trap configurations and the thickness of the buried oxide being chosen. The maximum available oxide thickness on a commercial SOI substrate of 10 μm is chosen to achieve higher breakdown voltage and lower trap capacitance, hence increasing the quality factor of the resonant circuit formed by the trap and helical resonator. While the removal of thick oxide using buffered HF oxide etch is suitable for fairly large-scale features of the 2D lattice trap allowing for overhanging structures, the resulting massive undercutting causes small features with dimension less than 200 μm of the Y-junction

trap to be lifted off. Therefore, the achievable fabrication process of the Y-junction trap with a 10-μm thick oxide is restricted to the ICP etching process. Removal of thinner oxide (i.e. a 5-μm thick oxide) is achieved either with buffered HF acid or ICP etching process. The fabrication challenges encountered in removing a thick buried oxide layer are highlighted and solutions for improvement are provided. In particular, the deep V-shaped undercut (~ 60-70 μm wide) obtained from a buffered HF oxide etching is thought to be a result of the fastest etch rate along a weak bonding interface between two buried oxide layers. This is due to the fact that the etch rate has a relation with the bond strength, faster etch rate means weaker bond. However, it was discovered that such an undercutting profile has the added benefit of improving in the surface flashover characteristics. To be noted, the design of unequal RF path lengths in the Y-junction trap was realised to be particularly problematic for adiabatic shuttling operations due to the induced excess micromotion from the RF phase difference [135]. Eliminating this design flaw will involve modifications of both design and fabrication. Hence, the fabricated Y-junction trap could not be used for ion trapping attempts described in the following part.

The second part of this thesis presents the experimental realisations of the microfabricated 2D lattice trap chips conducted in two different regimes – ion trapping in vacuum and charged particle trapping in ambient air. In the first experiment, the demonstration of ytterbium ($^{174}Yb^{+}$) ion trapping in the 2D lattice trap is achieved with a relatively long lifetime of a laser-cooled ion up to 90 minutes and ≤ 5 minutes without cooling in ultra-high vacuum system. The rudimentary shuttling between neighbouring lattice sites was carried out by lowering the RF voltage amplitude to reduce the potential barrier and supplying DC voltages to certain compensation electrodes to control the shuttling direction. The deterministic introduction of defects into the ion lattice (e.g. the missing ions in the lattice or the inclusion of additional ions in individual lattice sites) was successfully demonstrated. The surface flashover measurement of the SOI-built test devices was conducted in high vacuum. An extremely high-breakdown voltage up to 1 kV was observed on the devices fabricated on a 10 μm-thick buried oxide. This is attributed to the deep V-shaped

undercut profile of the oxide layer which results in a large breakdown path length, and so mitigating surface breakdown effects.

In another set of experiments, charged microparticle trapping, shuttling and levitation in the fabricated 2D hexagon trap were conducted in ambient air. The 2D lattice trap demonstrated stable trapping of 30-μm glass microspheres. The longest trapping lifetime up to 60 minutes is achieved but not limited by the trap performance due to the fact that the oil-filled transformer and the power amplifier had to be turned off for safety reasons. Although not measured precisely in this work, a particle was trapped at ~ 90 μm above the electrode surface. The measured trap height is about 22-35 μm less compared to the simulation predicting trap height of 117 μm. It is suspected that this is caused by the absence of the gravitational force compensation (pulling a particle down from the equilibrium trap position), the measurement errors due to camera tilt and the use of a manual calibration technique. A series of shuttling between neighbouring lattice traps through the entire trap array is achieved and found to be much simpler in ambient air with microparticles than in vacuum with ions. The levitation technique used in this experiment is of RF nil point shifting perpendicular to the electrode plane using the addition of a secondary AC potential field. The maximum levitation height of 30 μm is achieved. The particle can be trapped over the trapping height range of 90 ± 15 μm. In an attempt to estimate an unknown charge and Q/m ratio of individually trapped particles using a "*boundary ejection*" method, the average Q/m ratio taken from six particles is 2.55×10^{-4} C/kg. In this case, a particle's charge Q can be varied between 7.44×10^{-15} to 1.14×10^{-14} C.

The electrical breakdown characterisation was performed in a small chamber in an ambient air environment at room temperature. Owing to the V-shaped undercut profile, the surface breakdown voltage (~380 V) is improved by 15% for the devices fabricated on SOI substrates with a 10 μm-thick buried oxide compared to one with a 5 μm-thick buried oxide. The lower breakdown voltage of 320 ± 10 V over small micron-sized gaps is the dominant breakdown mechanism when operating the microfabricated ion traps in air. With this restriction, the device is thereby incapable of operating over a wide range of voltage, frequency and charge-to-mass ratio (Q/m). For instance, the levitation height as a function of

the amplitude ratio of two AC signals is restricted to the voltage difference of two AC signals applied to trap electrodes required to be lower than the air-breakdown level of ~ 320 V. As a result, the levitation of glass microspheres in this experiment can only achieve a limited height of 15 μm. For a similar experiment conduced in vacuum, the levitation height can be increased up to 40 μm for the higher breakdown level of > 500 V based on the simulation. For microparticle trapping in air, both gold and aluminium electrodes led to comparable trapping performances. However, the aluminium trap has not yet been used in ion-trap experiments. Further investigation is required to determine if light-induced charging of aluminium electrodes will have an impact on the performance of the proposed trap since aluminium exhibits more charging compare to copper or gold [227]–[229]. This is due to the fact that aluminium reacts immediately with atmospheric oxygen and quickly forms a native aluminium oxide layer, Al_2O_3. This air-formed oxide film on aluminium electrodes may induce unwanted charge build-up upon lasers illuminating the trap, leading to excess micromotion which can affect the stability of the trap.

In summary, the fabricated 2D hexagonal lattice trap demonstrates a large voltage and frequency operating ranges over 150-455 V and 500 Hz to 32 MHz respectively, for trapping ions and microparticles. This 2D lattice trap design also allows for reliable trapping of 2D ion lattices, rudimentary shuttling between lattice sites and deterministic introducing of defects into the ion lattice. Based on all these abilities, such a 2D lattice trap with the predicted reduction of lattice spacing down to 32 μm can be configured as a versatile architecture for 2D quantum simulations with trapped ions [172]. Furthermore, the *in situ* levitation of microparticles is successfully demonstrated. This ability provides additional control on the trapping height which increases the overall functionality of the 2D lattice trap. The surface flashover voltage up to 1 kV observed in this work is much higher than that reported in any other trap fabricated on a silicon substrate [79], SOI substrate [71], or other material components [77]. This is the added benefit of being able to trap ions in much higher trap depths and to be utilised in applications that the use of very high voltages is very desirable. For example, the study of ion trajectories in higher stability regions at a much higher stability parameter q requires higher RF voltage than those of normal operation in the first stability

region [133], and the levitation experiment as discussed above. Owing to the V-shaped undercut profile of the etched oxide, the fabrication technique of achieving high breakdown voltage in the microfabricated ion-trap chips gives a way to improve the surface breakdown voltage in microscopic ion traps and other microstructure devices.

9.2 Future work

9.2.1 Quantum information science with trapped ions

Efforts to develop an array of 2D lattice ion traps for quantum simulations have been made based on Porras and Cirac's proposal [230], [231]. To date, the implementation of a 2D lattice trap was experimentally limited to the confining of dust particles and ion clouds in either a millimetre-scale PCB trap [107], [108], [113] or a millimetre-scale wire-mesh trap [116] with lattice spacing (ion-ion separation, s) in the order of a millimetre. To make trapped ions an ideal quantum simulator, strong spin-spin interactions between ion-qubits can be achieved by decreasing ion spacing with optimum trap geometry is required.

In this work, the microfabricated 2D hexagonal lattice trap with lattice spacing of ~ 270 μm is achieved in demonstrating a reliable trapping of 2D ion lattices with long ion lifetimes. Shuttling of single ions between lattice sites adds more flexibility and control, increasing the overall functionality of the 2D ion-trap array. The ability to control ion lattice distribution and to deterministically introduce defects into the ion lattice (e.g. the missing ions in the lattice or the inclusion of additional ions in individual lattice sites) is also achieved. Structural defects in the ion lattice may be of interest in studies of Bose-Hubbard physics (i.e. the quantum phase transition from the Mott insulator state to the superfluid and simulations of spin models with spin greater than 1/2 [230]–[232]). To the best of the author's knowledge, this trap design is the first realisation of a 2D lattice trap with the lattice spacing scaled down to the micrometre scale, achieved by utilising the microfabrication techniques. The design of the 2D lattice trap presented in this work is the first prototype. At the time of designing this trap, the initial optimisation model developed by Siverns and his colleagues [109] was utilised.

However, the trap geometry was not yet completely optimised in all lattice parameters and constraints for achieving a strong coupling strength, a sufficiently deep trapping potential, a low heating rate, and being appropriate for quantum simulation schemes (e.g. Porras and Cirac's proposal [105], [230], [231]). The lattice design experimentally investigated in this work has an ion-ion separation s = 270.5 μm, lattice radius r of 125 μm and ion height h of 117 μm. For the secular motional frequency $\omega/2\pi$ = 1 MHz, the Coulomb coupling strength (J) of ions with a nearest-neighbour separation s = 270.5 μm is expected to be at 2 Hz which is relatively small compared to the coupling strengths already experimentally demonstrated using linear surface traps [233], [234]. This means that the current lattice trap is impractical for performing quantum simulations with ions. Hence, optimisation of the future lattice traps for quantum simulations will require a further reduction of lattice site radius (r) and lattice spacing (s).

Choosing to focus on the Porras-Cirac spin simulation scheme, the optimum geometry with lattice spacing of 32 μm and the lattice radius of 13 μm is proposed in a recent published work [172]. With the reduction of lattice spacing from 270.5 μm to 32 μm, the coupling strength is increased to ~ 1.3 kHz, which is in the order of 10^3 compared to those of the original design. With the modified trap configuration, ions are trapped at 15 μm above the electrode surface and the diagonal ion-electrode distance (d) determined by the edge of the hexagonal lattice is calculated to be ~ 19 μm. The modified trap can be constructed on the optimised SOI thickness of a 2.5 μm Si device layer and a 2.5 μm buried oxide layer (with the oxide-oxide bonding process to improve surface flashover voltage) using a similar fabrication method developed in this thesis. As the trap is miniaturised, the ion height (h) is also reduced. Determination of the heating rate ($\dot{n}$) and its applicability for quantum spin simulation in a miniaturised 2D ion-trap array with a significant reduction in the ion-height (also refer the ion-electrode distance) is importantly required. The heating rate strongly depends on the minimal distance d between the nearest electrode surface and the ion's position, approximately proportional to 10^{-2} for Johnson noise [131] and to 10^{-4} for anomalous heating [114]. At the diagonal ion-surface distance of 19 μm, the heating rate, which corresponds to an electric-field noise density $S_E(\omega)$ = 5.3 × 10^{-12} V^2m^{-2} Hz^{-1} for $\omega/2\pi$ =

1 MHz, is estimated to be at $\dot{n} = 180$ s^{-1} for $^{171}Yb^{+}$ ion trapping in the cryogenic condition (7 K). It is important that the resulting heating rate is significantly less than the effective spin-spin coupling rate $J = 2\pi \times 1.2$ kHz, suggesting that this particular quantum spin simulation scheme (algorithm) should be feasible with the combination of the optimised design and an appropriate driving laser.

In the present design of a 2D lattice trap, the distribution of trapped ions over the lattice sites can be controlled during ion loading by the intersection of the laser beams. In the next generation trap, the addition of individually controllable DC electrodes of each lattice would allow the distribution of ions over the lattice sites to be changed after the ions are loaded. This would enable the controlled filling of vacant lattices in case of ion loss by collisions with the background gas and the specific ejection of unwanted ions. Such local control also provides more precise control of the micromotion at each trapping site. Modifying lattice trap design to allow for lowering the trap secular frequency leading to the suppression of motional heating rate discussed in [114], [116] should be explored.

The fundamental explanation of heating effects in quantum regime is still an open question. Motional heating of ions in microfabricated traps is one of the major technical hurdles to progress in realizing a practical, large-scale quantum computation device. In this work, the *in situ* variation of the ion height in a 2D lattice trap using charged microparticles was experimentally demonstrated. This technique is particularly applicable for searching a true scaling of heating rate to a variation of ion height in an identical trap which only few experiments have thus far been able to conduct a systematic study on this issue [85], [235]. A deeper knowledge of heating effects in arrays of miniature ion traps with small ion height (well below 100 μm) is a crucial step to the development of high-fidelity quantum computation and simulation systems.

In order to make a Y-junction trap applicable to future work in quantum computing and information processing, the design requirement is the elimination of existing RF phase difference between the RF electrodes in each junction leg. The resulting phase shift of the RF signal leads to excess micromotion which is a fundamental source of heating in ion traps. This heating cannot be compensated and affects crucially to the quantum decoherence,

resulting in a degradation of the gate fidelity. Therefore, a modified trap will require a design of equal RF path lengths between junction legs together with the use of buried wires to allow the electrical connection to the isolated static electrode without breaking the RF electrode. Furthermore, the fabrication of a surface-electrode ion-trap array incorporating buried wires has significant benefits in allowing more complex ion-trap structures to be implemented using standard microfabrication techniques. For example, new electrode designs of multiple-isolated static and RF electrodes [117], and multi-dimensional arrays incorporating multiple junctions [96] have been proposed. This will also increase the scalability and trapping zone density to accommodate a large number of trapped ions (qubits) necessary for theoretical and experimental research in advanced quantum computing and information processing. Alternatively, the use of vertical interconnect access (via) has been presented with trade-off between the greatest flexibility in trap designing and the complicated fabrication commonly performed using VLSI facilities [71], [88].

9.2.2 Microparticle trapping in ion traps

Attempts at constructing the experiment with a cost-efficient hardware setup made from standard off-the-shelf components and in-house developed tools have both advantages and drawbacks. Experimentally, the existing experimental setup is proven to be capable of performing basic operations including trapping, shuttling and levitation of charged microspheres in air. In practice, however, accurately performing and measuring a more comprehensive experimental study is limited. For instance, the study of particle dynamics in damped surface-electrode trap geometries as a function of the nonlinear electric fields deviating from a perfect quadrupole trapping field of an ideal ion trap, remains an open question. In the study of the damping effect on the boundaries of the stability diagram, careful design of trap electronics together with multi-channel, high-speed voltage control systems to accommodate a wide range of both AC and DC voltages and frequencies in driving the trap RF electrode is necessary. Also, the secular frequency of the resonating particles can be analysed directly using a fast Fourier transform (FFT) routine with the data taken from the photon detector (e.g. photomultiplier tube and spectrum analyser). Subsequently,

the resulting secular frequencies are then used to determine the charge-to-mass (Q/m) ratio at a given trap geometry (ion-electrode distance) and operating parameters (voltage, frequency) more accurately. Alternatively, a static (DC) electric field can be used to compensate the gravitational force, for instance a wire mesh placed above the trap [107] or a conductive plate under the trap [116] providing a repulsive force that acts on trapped particles. The particle's charge-to-mass ratio can be precisely calculated using the given DC electric field that exactly balances the gravity and moves particles under micromotion to rest at the equilibrium position (RF nil).

In this embodiment, the improvement of trap electronics, imaging and tracking capability of the ion's position and the computer date acquisition (DAQ) hardware and control system is needed. A computer-controlled xyz-translation stage allowing for alignment of the position of the laser beam at the exact trapping height and for fine adjustment of CCD cameras during an ongoing experiment offers a higher degree of experimental control, flexibility, and measurement accuracy. Advancing such an experiment offers a valuable opportunity to explore many more interesting theoretical aspects and experimental findings.

One considerable disadvantage of microparticle trapping experiments in the surface-electrode trap structure is the surface contaminants. This issue is caused by particles adhering to the electrode surfaces and inside the isolation trenches after the performing of several experimental runs. Some charged particles sticking over the isolation trenches can induce a localised pre-breakdown at a low level of damage to the trap while the operating voltage supplied to the trap is still below the measured breakdown voltage in air. Controlling surface and trench contamination is a benefit for the long-term use and reliability of microstructure devices. To minimise the numbers of particles adhering to the trapping regions, a new method of loading and clearing out particles is needed. For instance, a more accurate particle-dispensing technique allowing for precisely-controlled doses and selective areas such as dry powder micro-feeding systems based on the ultrasonic vibration of a piezoelectric transducer [236]–[238] can be useful. By integrating this technique, micro- and nanoparticles can be loaded to trapping regions in precisely-controlled doses to reduce contaminant level and particles sticking to the electrode surface and inside the micro-gap electrodes. In addition, ability in

efficient loading of particles to selective areas will allow for demonstrating arbitrary 2D patterns of micro- and nano-particles and controlling the number of trapped particles simultaneously which are not applicable in the current experiment setup.

With the directions for overcoming the major challenging issues described above, these improvements would provide valuable capabilities for further investigation of single and parallel manipulation of micro- and nanoparticles in microscopic surface-electrode ion traps. For instance, examining *in situ* charging and discharging and methods for obtaining higher charges on particles, and measuring of the physical properties of particles with various sizes, shapes and materials under background gas pressure, could also be quite fruitful and highly beneficial for future research in particle science and technology.

Appendix A

SEIT numerical models in Mathematica

This is a demo Mathematica notebook with the basic functions used to evaluate performance of SEITs. After extracting electrode basis functions simulated using bemsolver, the raw data files of individual electrode potential are then processed using Mathematica. Pseudopotential and trap parameters including RF nil point (trap location), escape point, secular frequencies, trap depth, stability parameter q can be computed using the analytical expressions described in Section 4.2.2. The results of both ion and microparticle trapping in two types of surface-electrode ion traps are summarized in Table A.1. In addition, the resultant pseudopotential can be visualized using Mathematica Plot functions. The summary of trap characteristics obtained from the numerical study of Yb^+ ion trapping and microparticle trapping with given charge and mass values is provided in Table A.1.

2D hexagonal lattice traps - Charged Particle Trapping

Constants for 174Yb ion trapping

```
e   = 1.6 10^-19;
my  = 174 1.66 10^-27;
Ω   = 2 Pi 45 10^6;
ψ   = (e^2) / (4 my Ω^2);
Vrf = 500;
VrfBase = 0;
```

Constants for microparticle trapping

```
e   = 9 10^-15;
my  = 3.39 10^-11;
Ω   = 2 Pi 900;
ψ   = (e^2) / (4 my Ω^2);
Vrf = 500;
VrfBase = 0;
```

Input data (extracted from bemsolver)

```
dataRF = Import["C:\\Users\\hr1e09\\Southampton\\hexagon\\data\\RF1.dat","Table"];
dataHexBase = Import["C:\\Users\\hr1e09\\Southampton\\hexagon\\data\\hex_base1.dat","Table"];
dataComp1 = Import["C:\\Users\\hr1e09\\Southampton\\hexagon\\data\\comp1.dat","Table"];
dataComp2 = Import["C:\\Users\\hr1e09\\Southampton\\hexagon\\data\\comp2.dat","Table"];
dataComp3 = Import["C:\\Users\\hr1e09\\Southampton\\hexagon\\data\\comp3.dat","Table"];
dataComp4 = Import["C:\\Users\\hr1e09\\Southampton\\hexagon\\data\\comp4.dat","Table"];
dataComp5 = Import["C:\\Users\\hr1e09\\Southampton\\hexagon\\data\\comp5.dat","Table"];
dataComp6 = Import["C:\\Users\\hr1e09\\Southampton\\hexagon\\data\\comp6.dat","Table"];
```

Unit conversion from mm to μm

```
For[i=1,i<Length[dataRF]+1,
        For[j=1,j<4,
  {dataRF[[i,j]]=dataRF[[i,j]]/1000}
   {dataHexBase[[i,j]]=dataHexBase[[i,j]]/1000}
   j++];
 i++]

For[i=1,i<Length[dataComp1]+1,
        For[j=1,j<4,
  {dataComp1[[i,j]]=dataComp1[[i,j]]/1000}
   {dataComp2[[i,j]]=dataComp2[[i,j]]/1000}
   {dataComp3[[i,j]]=dataComp3[[i,j]]/1000}
   {dataComp4[[i,j]]=dataComp4[[i,j]]/1000}
   {dataComp5[[i,j]]=dataComp5[[i,j]]/1000}
   {dataComp6[[i,j]]=dataComp6[[i,j]]/1000}
   j++];
 i++]
```

Data interpolation

```
RF = Interpolation[dataRF]
Hexbase = Interpolation[dataHexBase]
Comp1 = Interpolation[dataComp1]
Comp2 = Interpolation[dataComp2]
Comp3 = Interpolation[dataComp3]
Comp4 = Interpolation[dataComp4]
Comp5 = Interpolation[dataComp5]
Comp6 = Interpolation[dataComp6]

InterpolatingFunction[{{-0.0015,0.0015},{-0.0012,0.0012},{0.,0.0003}},<>]
InterpolatingFunction[{{-0.0015,0.0015},{-0.0012,0.0012},{0.,0.0003}},<>]
InterpolatingFunction[{{-0.0015,0.0015},{-0.0012,0.0012},{0.,0.0003}},<>]
InterpolatingFunction[{{-0.0015,0.0015},{-0.0012,0.0012},{0.,0.0003}},<>]
InterpolatingFunction[{{-0.0015,0.0015},{-0.0012,0.0012},{0.,0.0003}},<>]
InterpolatingFunction[{{-0.0015,0.0015},{-0.0012,0.0012},{0.,0.0003}},<>]
InterpolatingFunction[{{-0.0015,0.0015},{-0.0012,0.0012},{0.,0.0003}},<>]
InterpolatingFunction[{{-0.0015,0.0015},{-0.0012,0.0012},{0.,0.0003}},<>]
```

Calculation of pseudopotential and trap parameters

```
RFbase[x_,y_,z_] = VrfBase Hexbase[x,y,z] + Vrf(1.0 RF[x,y,z]+ 0.00(Comp1[x,y,z] +
Comp2[x,y,z] + Comp3[x,y,z] + Comp4[x,y,z] + Comp5[x,y,z] + Comp6[x,y,z]));

pondpotential[x_,y_,z_] = ((D[RFbase[x,y,z],x])^2 + (D[RFbase[x,y,z],y])^2+
(D[RFbase[x,y,z],z])^2);

Totalpotential[x_,y_,z_] =  (e^2) / (4 my (Ω)^2) pondpotential[x,y,z] ;

Dervx[x_,y_,z_] = D[Totalpotential[x,y,z],x];
Dervy[x_,y_,z_] = D[Totalpotential[x,y,z],y];
Dervz[x_,y_,z_] = D[Totalpotential[x,y,z],z];

ax = x/.
FindRoot[{Dervx[x,y,z]==0,Dervy[x,y,z]==0,Dervz[x,y,z]==0},{{x,0.000},{y,0.000},{z,0.000120}}];
ay = y/.
FindRoot[{Dervx[x,y,z]==0,Dervy[x,y,z]==0,Dervz[x,y,z]==0},{{x,0.000},{y,0.000},{z,0.000120}}];
az = z/.
FindRoot[{Dervx[x,y,z]==0,Dervy[x,y,z]==0,Dervz[x,y,z]==0}, {{x,0.000},{y,0.000},{z,0.000120}}];

Print["Trap location (x, y, z) (um)"]
ax 10^6
ay 10^6
az 10^6

atx= x/.
FindRoot[{Dervx[x,y,z]==0,Dervy[x,y,z]==0,Dervz[x,y,z]==0},{{x,ax},{y,ay},{z,0.000250}}];
aty = y/.
FindRoot[{Dervx[x,y,z]==0,Dervy[x,y,z]==0,Dervz[x,y,z]==0},{{x,ax},{y,ay},{z,0.000250}}];
```

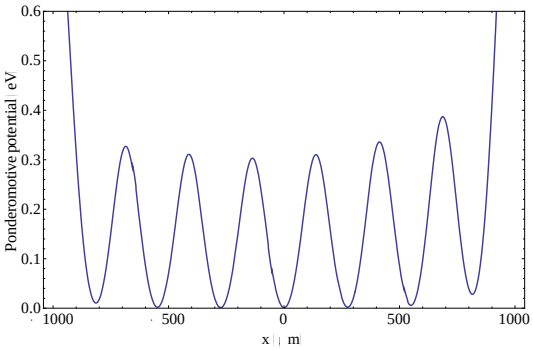
```
atz = z/.
FindRoot[{Dervx[x,y,z]==0,Dervy[x,y,z]==0,Dervz[x,y,z]==0},{{x,ax},{y,ay},{z,0.000250}}];

Print["Escape location (x, y, z) (um)"]
atx 10^6
aty 10^6
atz 10^6

xyzhex[x_,y_,z_] =(1/my)*(D[Totalpotential[x,y,z],{x,2}]);
Print["x secular frequency (Hz)"]
(xyzhex[ax,ay,az]^0.5)/(2 Pi)

xyzhey[x_,y_,z_] =(1/my)*(D[Totalpotential[x,y,z],{y,2}]);
Print["y secular frequency (Hz)"]
(xyzhey[ax,ay,az]^0.5)/(2 Pi)
xyzhez[x_,y_,z_] =(1/my)*(D[Totalpotential[x,y,z],{z,2}]);
Print["z secular frequency (Hz)"]
(xyzhez[ax,ay,az]^0.5)/(2 Pi)

Print["RF nil position micro-meters"]
{ax,ay,az}

Print["RF turning point (micro-meters)"]
{atx,aty,atz}

Print["Pseudopotential at RF nil (eV)eV"]
Totalpotential[ax,ay,az] /e

Print["Pseudopotential at escape point (eV)"]
Totalpotential[atx,aty,atz] /e

Print["Trap depth eV"]
(Totalpotential[atx,aty,atz]-Totalpotential[ax,ay,az])/e

Print["Stability qz"]
(2 e Vrf)/(my az^2 Ω ^2)
```

Output

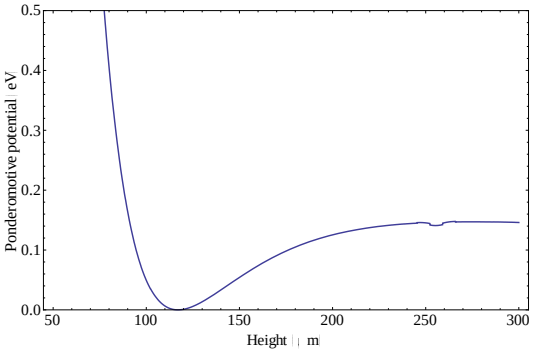
```
Trap location (x, y, z) (um)
0.600482
-0.209139
116.998

Escape location (x, y, z) (um)
1.79933
0.60025
247.035

X secular frequency (Hz)
20.894

y secular frequency (Hz)
19.4073

z secular frequency (Hz)
42.0011

RF nil position (um)
{6.00482×10^-7,-2.09139×10^-7,0.000116998}

RF nil position (um)
{1.79933×10^-6,6.0025×10^-7,0.000247035}

Pseudopotential at RF nil (eV)
1.36642×10^-16

Pseudopotential at escape point (eV)
0.172897

Trap depth (ev)
0.172897

Stability qz
0.600024
```

Plots

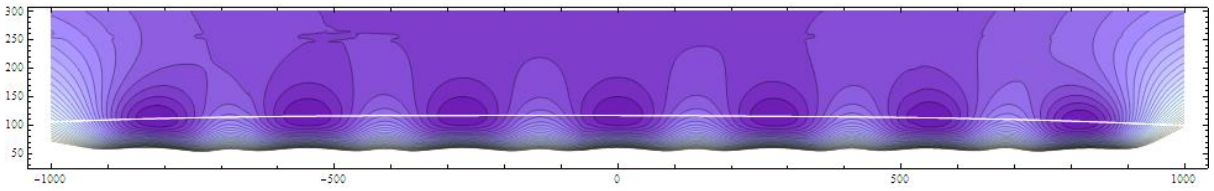
```
Plot[Totalpotential[x/10^6,0,120 /10^6]/e,{x,-0.001 10^6,0.0010 10^6}, PlotRange →{0,0.6},
PlotStyle→Thickness[0.003],Axes→False,Frame→True,FrameStyle→Large,FrameLabel→{"x
(μm)","Ponderomotive potential (eV)"},PlotPoints→Automatic]
```




```
Plot[ Totalpotential[0,0,z /10^6]/e,{z,0.00005 10^6,0.000310^6}, PlotStyle→Thickness[0.003],
PlotRange →{0,0.50},Axes→False,Frame→True,FrameStyle→Large,FrameLabel→{"Height
(μm)","Ponderomotive potential (eV)"},PlotPoints→Automatic]
```



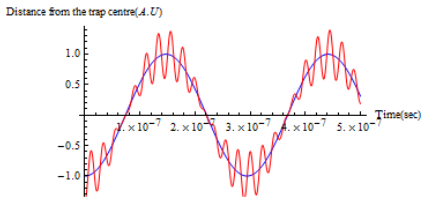

```
cross =ContourPlot[Totalpotential[x  10^-6,0,z 10^-6]/e,{x,-1000,1000},{z,30,300},AspectRatio-
>Automatic,Contours->30,PlotPoints->100]

FindRoot[{Dervz[x, 0, z] == 0, Dervx[x, 0, z] == 0}, {{x, 800 10^-6}, {z, 0.00011}}]
{x->0.000816063,z->0.000106697}

nils = {{-0.0008138484185222732`,0.00011163591108254672`},\
{-0.0005480997188552023`,0.00011580728848745761`},\
{-0.00027446943812605015`,0.00011693856477431965`},\
{0.000000600991415975 4617`,0.00011699801032225242`},\
{0.00027588176958010365`,0.00011560587430700113`},\
{0.0005493991805825225`,0.00011292006596789717`},\
{0.0008160628514850511`,0.00010669722541665485`}};

nilsline = Interpolation[nils];

nil = Plot[nilsline[x/ 10^6] 10^6, {x, -1000 , 1000 }, PlotStyle -> White];

Show[cross, nil]
```



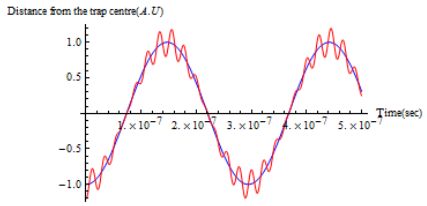
Stability parameter plots

```
ui = 1;
w1 = 2 Pi 3.4*10^6;
phi = Pi;
omega = 2 Pi 45*10^6;
qi = 0.78;

q1 = 1.00;
q2 = 0.80;
q3 = 0.60;
q4 = 0.40;
q5 = 0.20;
q6 = 0.10;

Print["Satbility paramter q = "];
N[q1]
Plot [  {ui Cos[w1 t + phi], ui Cos[w1 t + phi]* (1 + (q1/2) Cos[omega t])}, {t, 0, 0.5*10^-6},
 AxesLabel -> {Time [sec], Distance from the trap centre [A.U]}, PlotStyle -> {Blue, Red}]
N[q2]
Plot [  {ui Cos[w1 t + phi], ui Cos[w1 t + phi]* (1 + (q2/2) Cos[omega t])}, {t, 0, 0.5*10^-6},
 AxesLabel -> {Time [sec], Distance from the trap centre [A.U]}, PlotStyle -> {Blue, Red}]
N[q3]
Plot [  {ui Cos[w1 t + phi], ui Cos[w1 t + phi]* (1 + (q3/2) Cos[omega t])}, {t, 0, 0.5*10^-6},
 AxesLabel -> {Time [sec], Distance from the trap centre [A.U]}, PlotStyle -> {Blue, Red}]
N[q4]
Plot [  {ui Cos[w1 t + phi], ui Cos[w1 t + phi]* (1 + (q4/2) Cos[omega t])}, {t, 0, 0.5*10^-6},
 AxesLabel -> {Time [sec], Distance from the trap centre [A.U]}, PlotStyle -> {Blue, Red}]
N[q5]
Plot [  {ui Cos[w1 t + phi], ui Cos[w1 t + phi]* (1 + (q5/2) Cos[omega t])}, {t, 0, 0.5*10^-6},
 AxesLabel -> {Time [sec], Distance from the trap centre [A.U]}, PlotStyle -> {Blue, Red}]
N[q6]
Plot [  {ui Cos[w1 t + phi], ui Cos[w1 t + phi]* (1 + (q6/2) Cos[omega t])}, {t, 0, 0.5*10^-6},
 AxesLabel -> {Time [sec], Distance from the trap centre [A.U]}, PlotStyle -> {Blue, Red}]
```

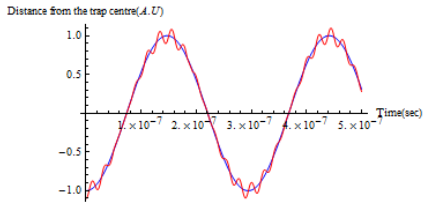
```
Satbility paramter q =
0.8
```




```
0.4
```




```
0.2
```




```
0.1
```

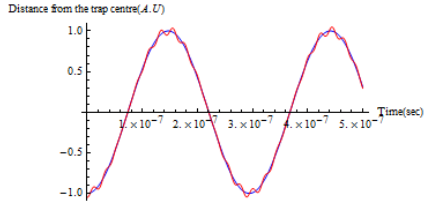


Table A.1 - Summary of trapping parameters for both ion and microparticle trapping in two types of surface-electrode ion traps.

Trap design	Type		Charge Q (C)	Mass m (kg)	Q/m ratio (C/kg)	Test # -	V_{RF} (V)	$\Omega_{RF}/2\pi$ (Hz)	$\omega_x/2\pi$ (Hz)	$\omega_y/2\pi$ (Hz)	$\omega_z/2\pi$ (Hz)	Trap height (μm)	Escape point (μm)	Trap depth eV	Stability q -
Y-junction trap	Ion	$^{171}Yb^+$	1.6×10^{-19}	$171\times1.66\times10^{-27}$	0.56×10^{6}	1	300	71.24M	2.24M	0.03M	2.33M	74.81	148.89	0.09	0.3
						2	300	50.38M	3.14M	0.04M	3.26M	74.81	148.89	0.18	0.6
						3	400	82.27M	2.55M	0.03M	2.65M	74.81	148.89	0.12	0.3
						4	400	58.17M	3.61M	0.04M	3.75M	74.81	148.89	0.24	0.6
						5	500	91.98M	2.90M	0.03M	3.02M	74.81	148.89	0.15	0.3
						6	500	65.04M	4.02M	0.05M	4.18M	74.81	148.89	0.30	0.6
	Microparticle	CuO/RbCl crystal 20 μm in diameter	1.6×10^{-14}	20×0^{-12} (20 ng)	8.0×10^{-4}	7	300	2684.22	83.02	0.99	86.37	74.81	148.89	0.09	0.3
						8	300	1898.03	117.32	1.40	122.06	74.81	148.89	0.18	0.6
						9	400	3099.48	95.88	1.14	99.75	74.81	148.89	0.12	0.3
						10	400	2191.66	135.59	1.61	141.06	74.81	148.89	0.24	0.6
						11	500	3465.32	107.22	1.28	111.55	74.81	148.89	0.15	0.3
						12	500	2450.35	151.64	1.81	157.76	74.81	148.89	0.30	0.6
2D hexagonal lattice trap	Ion	$^{171}Yb^+$	1.6×10^{-19}	$171\times1.66\times10^{-27}$	0.56×10^{6}	13	300	44.53M	0.54M	0.50M	1.08M	117.00	247.04	0.05	0.3
						14	300	31.48M	0.75M	0.70M	1.51M	117.00	247.04	0.11	0.6
						15	500	57.48M	0.69M	0.64M	1.39M	117.00	247.04	0.09	0.3
						16	500	40.65M	1.00M	0.93M	2.02M	117.00	247.04	0.19	0.7
						17	600	62.97M	0.76M	0.71M	1.54M	117.00	247.04	0.11	0.3
						18	600	44.53M	1.07M	0.99M	2.15M	117.00	247.04	0.21	0.6
	Microparticle	CuO/RbCl crystal 20 μm diameter	1.6×10^{-14}	20×0^{-12} (20 ng)	8.0×10^{-4}	25	300	1677.64	20.37	18.92	40.95	117.00	247.04	0.05	0.3
						26	300	1186.27	28.82	26.77	57.94	117.00	247.04	0.11	0.6
						27	500	2165.82	26.31	24.44	52.90	117.00	247.04	0.09	0.3
						28	500	1531.47	37.24	34.59	74.85	117.00	247.04	0.18	0.6
						29	600	2372.54	28.81	26.76	57.91	117.00	247.04	0.11	0.3
						30	600	1677.64	40.74	37.84	81.90	117.00	247.04	0.22	0.6
		Glass microspheres 30 μm in diameter	9.0×10^{-15}	3.39×10^{-11}	2.65×10^{-4}	31	200	809.33	9.34	8.68	18.78	117.00	247.04	0.03	0.3
						32	200	572.28	13.21	12.27	26.56	117.00	247.04	0.07	0.6
						33	300	991.22	11.44	10.63	23.01	117.00	247.04	0.05	0.3
						34	300	700.90	16.18	15.03	32.53	117.00	247.04	0.10	0.6
						35	400	1144.56	13.21	12.27	26.56	117.00	247.04	0.07	0.3
						36	400	809.33	18.69	17.36	37.57	117.00	247.04	0.14	0.6
						37	500	1279.66	14.77	13.72	29.70	117.00	247.04	0.09	0.3
						38	500	904.86	20.89	19.41	42.00	117.00	247.04	0.17	0.6

Appendix B

B-1 Layout of fabrication photolithography mask

The fabrication photolithography mask was designed by Dr. Prasana Srinivasan (University of Southampton) using Tanner EDA L-edit commonly used in designing MEMS devices and drawing layouts. Three different ion-trap designs were placed in a single 6-inch diameter bright field mask as shown in Figure B-1. In the future photomask design, the ion-trap devices located at the peripheral region of the photomask will be placed in separated masks to improve the fabrication yield and to facilitate optimisation the fabrication processes with diverse trap geometries.

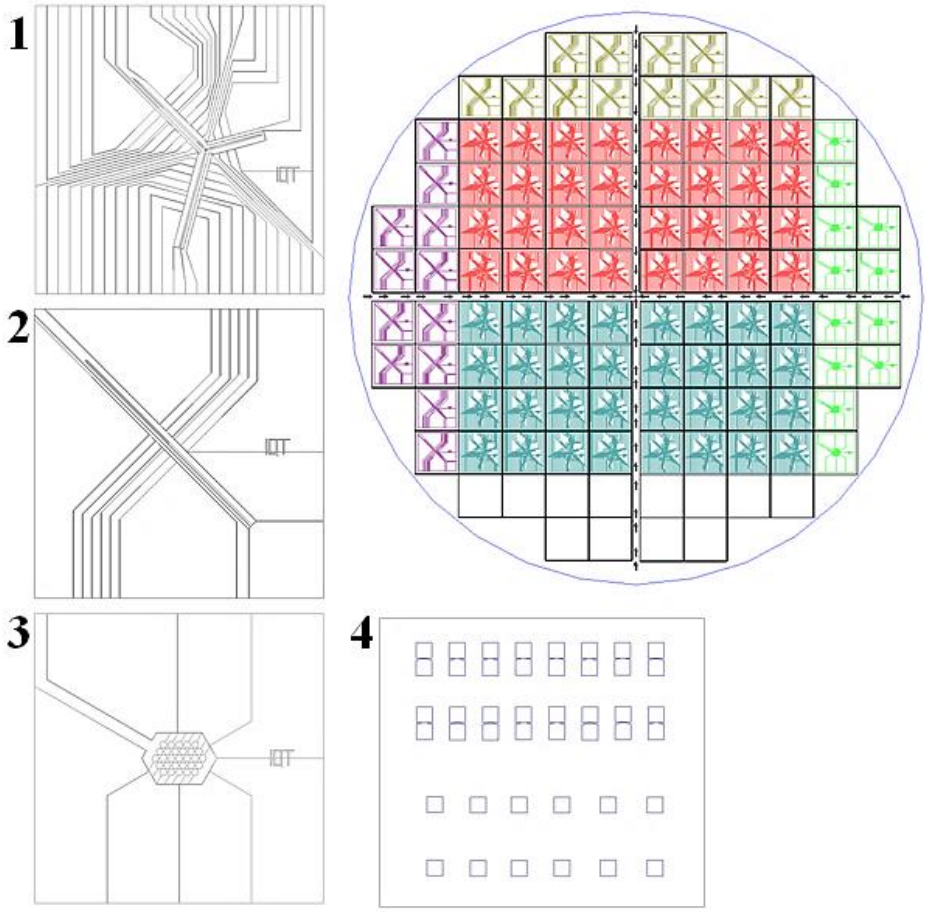


Figure B.1 – A 6-inch diameter wafer layout containing four different surface-electrode trap geometries with variation of electrode gap widths.

Table B.1 - List of surface-electrode ion trap (SEIT) designs.

Surface-electrode ion trap (SEIT) designs	Electrode gap dimension (μm)	No# of trap chips
1. Y-junction trap (multiple trap zones)	5.0 7.5	32 32
2. Linear section of Y-junction trap (single trap zone)	7.5	12 × 2
3. 2D hexagonal lattice traps (29 trapping sites)	10.0	12
4. Electrical breakdown test structures i) A single square electrode ii) Two-electrodes with microgaps	 - 3/5/7/9	 12 4 × 4

SEIT design 1

Trap description: Y-shaped junction trap

Approximate trap height: 75 μm (at linear regions)

Number of DC electrodes: 44

Design: At the linear regions (five-wire design), two RF electrodes are asymmetrically designed with widths of 100 μm and 200 μm, along with the central ground and extra ground electrode with a width of 60 and 100 m respectively. This asymmetrical RF electrode geometry allows a rotation of the principal axis required for effective laser cooling of an ion. The trap has four main operating regions: Y-junction (shuttling through the junction), top and bottom linear sections (combination and separation required for quantum gate operations) and right linear section (ion storage).

SEIT design 2

Trap description: Linear section of Y-shaped junction trap

Approximate trap height: 75 μm (at linear regions)

Number of DC electrodes: 10

Design: This trap has similar electrode dimensions to those of SEIT design 1 and can be used to demonstrate the ion separation and combination process.

SEIT design 3

Trap description: 2D hexagonal lattice traps

Approximate trap height: 117 μm

Number of DC electrodes: 6

Design: This trap consists of 29-trapping sites arranged in a triangular shape. Each trapping site is surrounded by up to six nearest neighbours with the ion-ion separation of 270.5 μm measured from the centre of each lattice site. This trap is capable of trapping an array of ions and useful for observing ion-ion coulomb interactions. One important future application for a 2D ion lattice array is in the field of quantum simulations.

SEIT design 4

Trap description: Electrical breakdown testing structures

Approximate trap height: -

Number of DC electrodes: -

Design: A single square electrode device can be used to evaluate the surface (flashover) breakdown of insulator in SOI structural traps. The breakdown voltage for small air gaps is verified using a two-electrode testing device.

B-2 Photolithography processing recipes

In this work, different kinds of photoresists were used depending on requirements such as desired resist film thickness and resolution, subsequent etching processes (i.e. high selectivity for dry etching). The following tables provide further detail of photolithography process parameters used in three different process flows.

Table B.2 - S1813® process parameter for photoresist (PR) thickness of 1.2 μm used for metal wet etching process (Process flow A).

S1813® Process Parameters				
Substrate:	Gold film			
Photoresist: Positive	Shipley® S1813 photoresist			
Spin coating:	Speed (rpm) 5000 5000 100	Acc. (rpm) 2500 0 1000	Time (sec) 2.0 30.0 2.0	Resist thickness 1.2 ± 0.1 μm
Softbake:	95 °C/60 seconds, Hotplate			
Exposure:	EVG620T, 18.34 mW/cm² (no I-Line) Vacuum+Hard Contact Exposure time: 2 seconds			
Develop:	Microposit® MF®319 developer Develop time: 25 ± 10 seconds @ 21 °C			

Table B.3 - AZ9260® process parameters for photoresist (PR) thickness of 6 μm (Process flow B with a buffed HF SiO_2 etch).

AZ9260® Process Parameters				
Substrate:	Gold film			
Adhesion promoter:	MicroChemicals TI-Prime			
Spin coating:	Speed (rpm)	Acc. (rpm)	Time (sec)	Resist thickness -
	500	250	2.0	
	500	0	3.0	
	3000	1000	2.5	
	3000	0	20.0	
	500	1000	2.5	
	500	0	2.0	
	0	250	2.0	
Pre-Bake:	120 °C/120 seconds, Hotplate			
Photoresist: Positive	AZ9260® thick film photoresist			
Spin Coating:	Speed (rpm)	Acc. (rpm)	Time (sec)	Resist thickness 6.0 ± 1 μm
	500	250	2.0	
	500	0	7.0	
	4000	1750	2.0	
	4000	0	60.0	
	500	1750	2.0	
Soft-bake:	110 °C/150 seconds, Hotplate			
Interval:	30 minutes at @ 21 °C			
Exposure:	EVG620T, 24.38 mW/cm² (no I-Line) V+H contact EVG620TB, 14.97 mW/cm² (no I-Line) V contact Exposure time: 10-11 sec. (620T), 8.5-9.0 sec. (620TB)			
Develop:	AZ 400K developer diluted with DI water 1:4 Develop time: 120 ± 10 seconds @ 21°C			

Table B.4 - AZ9260® process parameters for photoresist (PR) thickness of 15 μm (Process flow C with ICP SiO_2 etch).

AZ9260® Process Parameters				
Substrate:	Gold film			
Adhesion promoter:	MicroChemicals TI-Prime			
Spin coating:	Speed (rpm)	Acc. (rpm)	Time (sec)	Resist thickness -
	500	250	2.0	
	500	0	3.0	
	3000	1000	2.5	
	3000	0	20.0	
	500	1000	2.5	
	500	0	2.0	
	0	250	2.0	
Pre-Bake:	120 °C/120 seconds, Hotplate			
Photoresist: Positive	AZ9260® thick film photoresist			
Spin Coating:	Speed (rpm)	Acc. (rpm)	Time (sec)	Resist thickness 15 ± 1 μm
	500	5000	0.1	
	500	0	3.0	
	2000	5000	0.3	
	2000	0	7.0	
	500	5000	0.3	
	500	0	2.0	
	0	5000	0.1	
Soft-bake:	110 °C/8 minutes, Hotplate			
Interval:	45-60 minutes at @ 21 °C			
Exposure:	EVG620TB, 20.00 mW/cm^2 (no I-Line) V contact Exposure time: 31 seconds			
Develop:	AZ 400K developer diluted with DI water 1 : 3 ratio Develop time: 5-6 minutes @ 21 °C			
Result:	1. Edge bead reduction 2. Longer soft-bake time 8 min. required for any subsequent dry etching process on SOI wafer with 10 μm thick oxide layer to avoid photoresist burning.			

Appendix C

Trap electronic components

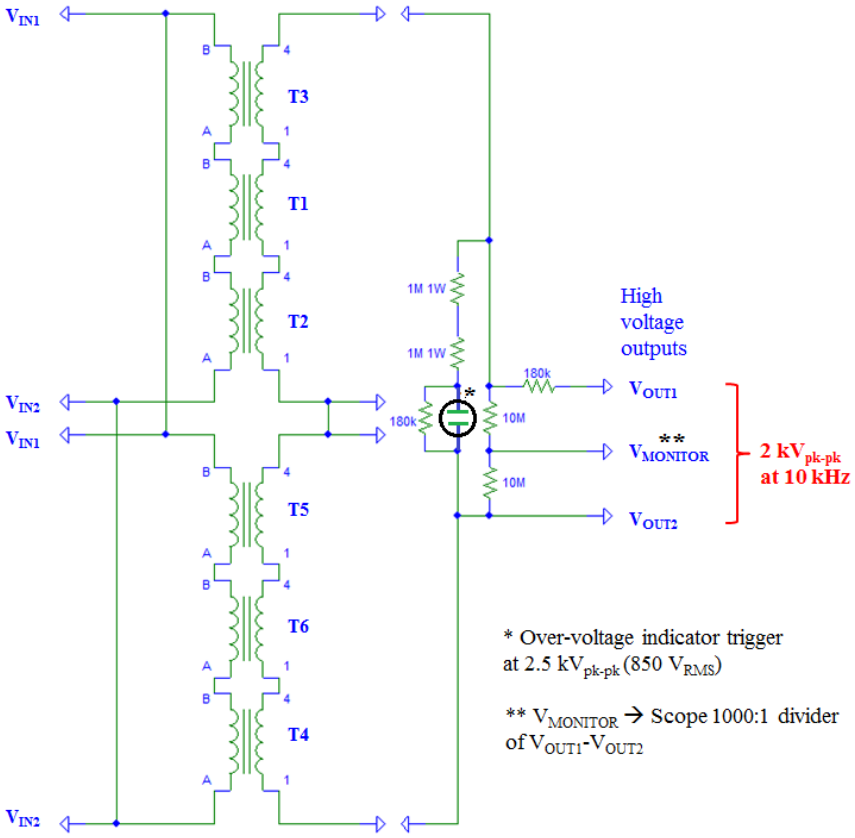


Figure C.1 – An oil filled transformer circuit diagram

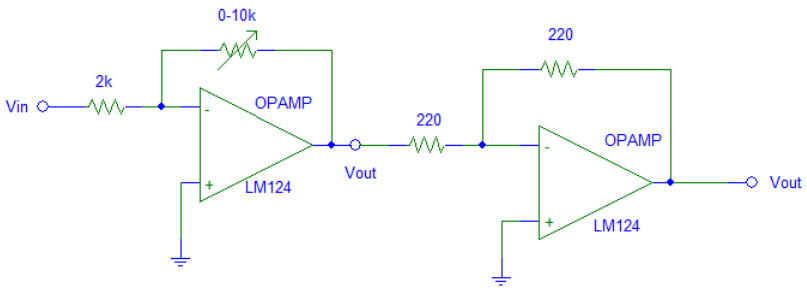


Figure C.2 – An inverting op-am circuit used for generating a 180° out-of-phase signal and a 0° in-phase input signal (a secondary AC voltage).

Appendix D

Triboelectric series

Table D.1 – The triboelectric series.

Most Positive (+)		
Air	+++	
Human hands, skin		Spores are in this range
Leather		
Asbestos		
Rabbit fur		
Glass		
Human hair		
Mica		
Nylon		
Wool		
Lead		
Cat fur		
Silk		
Aluminium		
Paper	+	
Cotton		neutral
Steel	-	
Wood		
Lucite		
Amber		
Rubber balloon		
Hard rubber		
Nickel		
Copper		
Silver		
Brass		
Synthetic rubber		
Gold, Plattinum		
Sulfur		
Acetate, Rayon		
Polyester		
Celluloid		
Polystyrene		
Polyurethene		
Polypropylene		
Vinyl (PVC)		
Silicon		
Teflon		Silica is in this range
Silicone rubber	---	
Most Negative (-)		

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