Reliable Power Gating with NBTI Aging Benefits

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***Abstract*—In this paper, we show that Negative Bias Temperature Instability (NBTI) aging of sleep transistors (STs), together with its detrimental effect for circuit performance and lifetime, presents considerable benefits for power gated circuits. Indeed, it reduces static power due to leakage current, and increases ST switch efficiency, making power gating more efficient and effective over time. The magnitude of these aging benefits depends on operating and environmental conditions. By means of HSPICE simulations, considering a 32nm CMOS technology, we demonstrate that static power may reduce by more than 80% in 10 years of operation. Static power decrease over time due to NBTI aging is also proven experimentally, using a test-chip manufactured with a TSMC 65nm technology. We propose an ST design strategy for reliable power gating, in order to harvest the benefits offered by NBTI aging. It relies on the design of STs with a proper lower V_{th} compared to the standard power switching fabric. This can be achieved by either re-designing the STs with the identified V_{th} value, or applying a proper forward body bias to the available power switching fabrics. Through HSPICE simulations, we show lifetime extension up to 21.4X and average static power reduction up to 16.3% compared to standard ST design approach, without additional area overhead. Finally, we show lifetime extension and several performance-cost trade-offs when a target maximum lifetime is considered.**

***Index Terms*—power gating, NBTI aging, power switches, leakage current, static power**

I. Introduction

Power gating has emerged as an effective approach to tackle static power [1]. It utilizes transistors as power switches (also referred to as *sleep transistors*, and denoted by STs) to disconnect logic blocks from supply voltage during periods of inactivity. Particularly, a header switch uses a high-V_{th} pMOS transistor to control V_{dd}, while a footer switch uses a high-V_{th} nMOS transistor to control V_{ss}. Since header STs are more commonly used in commercial power-gated circuits [1], they will be considered in this paper.

Along with power issues, electronic systems at nano-scale are increasingly suffering from reliability reduction [2]. Particularly, they are prone to aging effects, which negatively impact circuit performance and long-term reliability. Among several aging effects, Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) are the two most important ones [3]. They cause an increase in transistor threshold voltage (V_{th}) over time, which leads to a performance degradation and reduce their lifetime [3]–[6]. Positive BTI (PBTI) and HCI degrade the behavior of nMOS transistors, while negative BTI (NBTI) affect pMOS transistors [3]. NBTI is predominant over the PBTI and HCI, and is recognized as one of the primary parametric failure mechanisms for modern ICs [3], [5], [7]. Header STs employed in power gating designs degrade because of NBTI like any other pMOS transistor. Moreover, since they are always ON (under stress) when a power-gated circuit is operating, STs may suffer from an even higher degradation compared to functional transistors [8], [9]. As a result, since STs are always on the critical path, their degradation undermines both circuit performance and lifetime, thus causing long-term reliability issues [9]. NBTI aging is exacerbated by high operating temperature and supply voltage. In the IC manufacturing flow, these conditions are experienced during burn-in test, which aims at stressing circuits under test in order to identify those likely to fail early in their life cycle [10]. Therefore, standard burn-in test can cause a significant NBTI degradation even for short burn-in duration [11].

Standard power gating approaches, as those presented in [1], [12]–[14], have so far ignored the detrimental effects of NBTI on header STs. They rely on the identification of IR drop, static power and ST switch efficiency (defined as the ratio between on and off currents [1]) constraints at *time zero* ($t0$), neglecting their variation over time due to NBTI aging. In [8], [9], countermeasures have been proposed to tackle NBTI effect on power-gated circuits. They are mainly based on ST network oversizing, or on the increase of their number accompanied by a selective activation procedure, in order to reduce the stress applied to each ST. In [8], the combination of these techniques with adaptive body bias [15] has been also assessed. The techniques in [8], [9] allow designers to extend circuit lifetime and increase its long-term reliability by considering the detrimental effects of NBTI aging, at the cost of more area and increased design complexity. However, they ignore the beneficial effects of NBTI aging on static power reduction [16], [17] and ST switch efficiency. Moreover, they do not account for the effect of different operating conditions on degradation of STs.

In this paper, we show that ST NBTI aging, together with the detrimental effects on performance and lifetime, comes with considerable benefits for static power reduction and ST switch efficiency. Moreover, we show that both detrimental and beneficial effects are a critical function of the operating conditions (stress time and aging temperature). By HSPICE simulations performed considering two case studies (10 FO4 cascaded inverters and the *b02* benchmark from the *itc99* benchmark suite), implemented with a 32nm CMOS technology [18], we show that static power (ST switch efficiency) may reduce (increase) by more than 50% ($2.5\times$) after 1 month, and by more than 80% ($6.2\times$) in 10 years of operation. Static power decrease over time due to NBTI aging has been also

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proven experimentally, using a test-chip manufactured with a TSMC 65nm technology. Leakage current reduction up to 8.9% after 526 hours of operation has been measured.

Based on these results, we propose an ST design strategy for reliable power gating, which harvests the leverage for ST design offered by NBTI aging benefits. It relies on the identification of an ST threshold voltage suitably lower than that of standard high-V_{th} STs, accounting for the NBTI degradation induced during burn-in test. The proposed ST design allows designers to trade-off part of NBTI aging benefits for static power and ST switch efficiency in order to counteract NBTI detrimental effects on circuit propagation delay and lifetime. It is worth noting that the proposed ST design strategy, which has been validated for a CMOS 32nm technology, can be applied also to more scaled technologies using finfets. As known, FINFETs exhibit lower leakage current than standard CMOS devices. Nonetheless, according to the literature [19], [20], they are still prone to high BTI aging. Therefore, the relative impact (both detrimental and beneficial) of BTI aging on sleep transistors is expected to be similar. Consequently, the proposed ST design approach will also be beneficial to FINFETs.

Through HSPICE simulations of ISCAS85 and IWLS benchmarks, we show that we can achieve a circuit lifetime extension up to $21.4\times$ and an average static power reduction (per year of lifetime) up to 16.3% compared to standard power gating designs. These improvements are achieved without any area overhead, thus reducing considerably the cost over alternative techniques [8], [9]. Finally, we show lifetime extension and performance-cost trade-offs when a maximum lifetime target LT_{max} is considered. As an example, for LT_{max} equal to 5 years (10 years), the proposed ST design strategy achieves a lifetime extension up to 5.8X (11.6X) compared to a standard ST design, and offers the possibilities to either improve circuit operating frequency up to 9.9% (6%), or reduce ST area overhead up to 19.8% (7.1%). A list of abbreviations and acronyms used frequently throughout the paper is reported in Table I.

The rest of the paper is organized as follows. In Sec. II, we present some basics on NBTI and power gating. In Sec. III, we assess the ST NBTI aging impact on the behavior of power-gated circuits considering a standard high-V_{th} ST design and different operating conditions. We then provide experimental evidence of the NBTI aging benefits on static power consumption. In Sec. IV, we discuss the proposed ST design strategy and, in Sec. V, we present HSPICE simulation results to validate it. Finally, in Sec. VI, we draw some conclusions.

TABLE I
LLIST OF ABBREVIATIONS AND ACRONYMS

(N)BTI	(Negative) Bias Temperature Instability
ST	Sleep transistor
HCI	Hot Carrier Injection
VDSM	Very Deep Sub-micron
LT	Lifetime
VV_{dd}	Virtual V_{dd}
SwE	ST Switch Efficiency
S_{ST}	ST shape factor
τ_{wc0}	Worst case propagation delay at t_0
$SPDC_0$	Static Power Design Constraint at t_0
$SwEDC_0$	ST Switch Efficiency Design Constraint at t_0
MP	Medium Performance
HP	High Performance
t_{BI}	Burn-in test duration
t_{BE}	Time at break-even

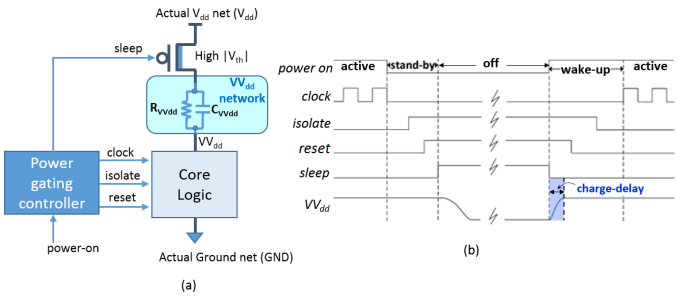


Fig. 1. (a) Power gating approach; (b) power gating protocol.

II. BACKGROUND ON POWER GATING AND NBTI AGING

Power gating is one of the most effective static power reduction techniques for VDSM technologies. It relies on selectively powering down certain blocks in the chip that are not being used by inserting header STs in series with the pull-up logics, or footer STs in series pull-down logic. This way, an intermediate virtual V_{dd} or virtual ground (GND) is created. Header STs use high-V_{th} (in absolute value) pMOS transistors to connect actual and virtual V_{dd}, while footer STs use high-V_{th} nMOS transistors to connect actual and virtual GND. Footer nMOS STs are typically used in voltage scaling approaches [1]. However, they are costly to design, since they require a triple well CMOS process [1]. Header pMOS STs exhibit better leakage characteristic than nMOS transistors, and they are preferred in designs where leakage constraints are stringent. Moreover, their design is cheaper compared to nMOS STs, since the n-well is readily available for bias tapping in the standard CMOS process [1]. Therefore, the use of pMOS STs is preferred in commercial power-gated circuits, and will be considered in this paper. The general scheme using header STs is shown in Fig. 1(a), together with the stand-by and wake-up protocols, which are depicted in Fig. 1(b) in the typical case where the power-gated core is equipped with clock-gating and isolation features [1].

NBTI causes significant degradation of pMOS transistors [21], [22]. Particularly, it induces a threshold voltage increase, when pMOS transistors are ON (stress phase) [23]. NBTI-induced degradation is partially recovered, when they are OFF (recovery phase). The reaction-diffusion model in [23] allows designer to estimate threshold voltage increase as a function of technology parameters, operating conditions and time. However, it is not suitable to model long-term NBTI degradation. In [7], an analytical model has been proposed that allows designers to estimate the long-term, worst-case threshold voltage shift ΔV_{th} as a function of applied voltage, stress/recovery time and temperature. It is:

$$\Delta V_{th} = K_{lt}\sqrt{C_{ox}(V_{dd}-V_{th})}e^{\frac{-E_a}{kT}}\alpha^{\frac{1}{6}}t^{\frac{1}{6}} \quad (1)$$

The parameter C_{ox} is the oxide capacitance, t is the operating

time, α is the fraction of the operating time during which a MOS transistor is under a stress condition, k is the Boltzmann constant, T the device temperature and E_a is a fitting parameter ($E_a \simeq 0.08$ [24]). By means of the parameter α ($0 \leq \alpha \leq 1$), we are able to account for the effective amount of time during which a device is under stress. It is $\alpha = 0$ if the MOS transistor is always OFF (recovery phase), while $\alpha = 1$ if it is always ON (stress phase). The parameter K_{lt} lumps technology specific and environmental parameters, and has been estimated to be $K_{lt} \simeq 2.7V^{1/2}F^{-1/2}s^{-1/6}$ by fitting the model with the experimental results reported in [25].

III. Impact of NBTI Aging of Sleep Transistors on Power-Gated Circuits Characteristics

In this section, we analyze the beneficial effects of ST NBTI aging on static power (during off mode) and ST switch efficiency, denoted by SwE and defined as: $SwE = I_{on}/I_{off}$ [1]. We also observe static power reduction over time with an experiment conducted with an actual chip. Finally, the detrimental effects of ST NBTI aging on propagation delay and lifetime (during active mode) of the power-gated logic, and on the charge delay of VV_{dd} network (during wake-up protocol) are also analyzed.

A. Simulation Set-up

We consider the power gating approach in Fig. 1(a) applied to two logic blocks: the *b02* benchmark from the *itc99* benchmark suite, and a circuit composed by 10 FO4 cascaded inverters. They are implemented with a 32nm Metal Gate, High-K Strained-Si CMOS technology [18], with a supply voltage $V_{dd} = 1V$. Header pMOS STs are implemented by adopting a high-V_{th} model, while logic gates are designed using the low-V_{th} model. Logic gates are sized in order to be symmetric for the worst case delay. The VV_{dd} network is modeled with a lumped RC circuit, whose parameters have been derived from [26]: $R_{VVdd} = 1\Omega$, $C_{VVdd} = 5fF$ for the *b02* benchmark, $C_{VVdd} = 7fF$ for the NOT chain. Note that the NOT chain (composed by 10 FO4 inverters) is larger than the b02 benchmark and this area difference is reflected by the different values of the parasitic capacitance associated to the VV_{dd} power network in the two case studies.

In actual designs, power network is distributed [27] and switching logic is realized by means of many STs deployed throughout the system [28]. For the purpose of our analysis, since the VV_{dd} network is modeled as a lumped RC circuit, we design the STs as a single, equivalent high-V_{th} pMOS transistor. If we considered multiple STs, they would be all in parallel with the same gate, drain and source voltage values, and would be exposed to the same BTI degradation. Consequently, they would behave as a single, larger transistor. Since the main goal of our analysis is to evaluate the relative impact of NBTI aging with respect to the characteristics exhibited by the power gated circuit at $t0$, this simplification does not affect the validity of the obtained results.

For each considered circuit, we determine the aspect ratio of the STs in order to introduce an IR drop equal to $0.1V_{dd}$ at $t0$. This is a constraint usually adopted by

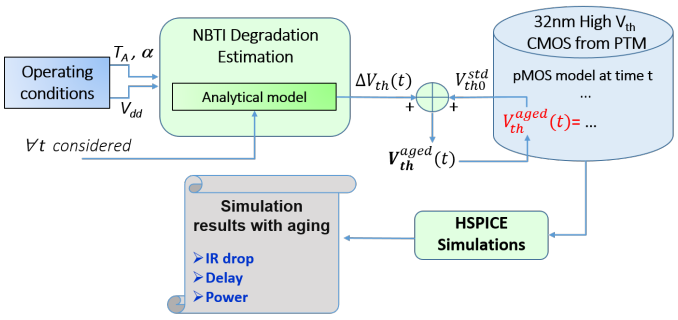


Fig. 2. Simulation flow with embedded aging effects.

standard power gating approaches neglecting the effect of NBTI [1], [8], [12]–[14]. The obtained values of the ST equivalent aspect ratios $S_{STeq} = (W/L)_{eq}$ are $S_{STeq}(b02) = 110 and S_{STeq}(NOT) = 38$, which represent approximately 23.1% and 12.7% of the area of the respective power gated circuit. In this regard, it is worth reminding that the STs are sized in order to fulfill $0.1V_{dd}$ IR drop requirement for the worst case current, which depends on the considered circuit. If we considered a lower IR drop value as a requirement, the ST area ratio would be bigger. For these ST sizes, we obtain the following values of the ST switch efficiency: $SwE(b02) \simeq SwE(NOT) = 1.02 \times 10^7$.

In order to highlight the effect of ST NBTI aging on circuit IR drop and propagation delay (in active mode) and static power (in off mode), we do not include the aging of logic transistors in our simulations. For the same reason, we do not consider the effect of PVT variations on circuit characteristics. As for NBTI, it is worth noticing that STs, exhibiting a higher V_{th} compared to logic transistors, undergo a lower electric stress. According to (1), this might lead to a lower degradation. Nevertheless, differently from logic transistors, STs are under stress for 100% of time during which a power-gated circuit is operating. As a result, the degradation of STs dominates over that of standard logic [8]. The obtained simulation results are normalized over the values exhibited at $t0$. This allows us to highlight the effect of the NBTI-induced degradation on circuit characteristics.

We assess trend over time of the threshold voltage increase ΔV_{th}, as well as of the other power gated circuit characteristics, for different aging temperatures and stress ratios. Particularly, we consider two operating condition set-ups: a) different aging temperatures $T_A = 25^oC, 50^oC$ and 75^oC, and constant stress ratio $\alpha = 0.5$; b) different $\alpha = 0.25, 0.5$ and 0.75, and constant $T_A = 75^oC$. In Fig. 2, we show the approach followed to embed aging effects in our simulation flow. Following the procedure in [25], [29], [30], given power supply V_{dd} and operating conditions (aging temperature T_A and stress ratio α), the ΔV_{th} degradation is estimated. The ΔV_{th} value obtained for each considered operating time interval is then utilized to customize the HSPICE device model and simulate STs with the proper NBTI degradation.

B. Power Switch NBTI Aging Beneficial Effects

In this subsection, we assess the beneficial effects of ST NBTI aging on both static power consumption and ST switch

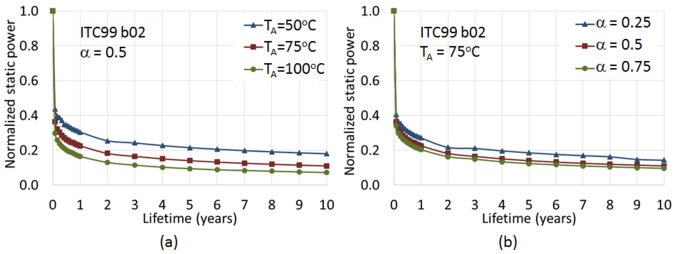


Fig. 3. Profile of the normalized static power over time for *b02* benchmark (normalization factor: $SPDC_0$(b02)=64.5pW) with: (a) different aging temperatures; (b) different stress ratios.

TABLE II
MEASURED LEAKAGE CURRENT

Meas. i	1	2	3	4	5
Lifetime (h)	0	68	96	162	526
Temperature (^oC)	59.3	60.0	60.5	60.5	61.3
I_{leak} (μA)	30.4	31.1	30.9	30	30.9

efficiency, and we show that power gating techniques becomes more efficient and effective over time.

1) Static Power: When a standard power gating approach using high-V_{th} ST is applied, static power drops to $64.5pW$ (*b02* benchmark) and $35.1pW$ (NOT chain), with a reduction exceeding 95% compared to a design without power gating. These two values are the amount of static power that designers expect to consume if a standard power gating design flow (not accounting for NBTI) is considered. Therefore, they represent the actual design constraints for static power consumption. We refer to these values as *static power design constraint at t0*, and we denote them as $SPDC_0(b02)$ and $SPDC_0(NOT)$.

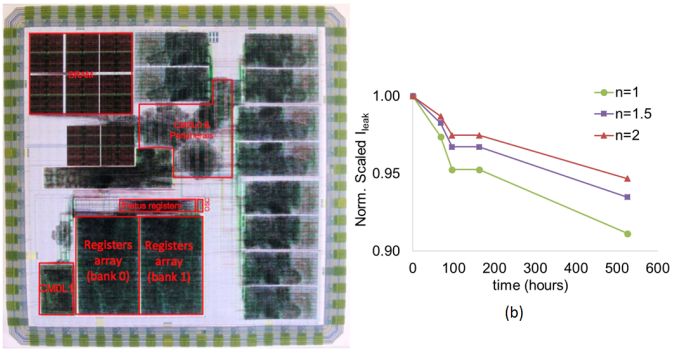
It should be considered that leakage current has two main contributors [1]: subthreshold current and gate current. Subthreshold current contribution dominates, since gate current can be well controlled by the use of high-k dielectrics. Therefore, when a ST is OFF, its leakage current I_{leak} is [1]:

$$I_{leak} \simeq \mu C_{ox} \frac{W}{L} \left(\frac{kT}{q}\right)^2 e^{\frac{-qV_{th}}{nkT}}, \qquad (2)$$

where W and L are the ST channel width and length, respectively, q is the electron charge, k the Boltzmann constant, T the temperature, and n a parameter that depends on device fabrication.

Since the main NBTI effect is to increase V_{th}, as shown in (1) **in Sec. II**, we expect that actual static power $P_{st} = V_{dd} \cdot I_{leak}$ decreases as STs age. This is confirmed by the obtained HSPICE simulation results shown in Fig. 3, which depicts the trend over time of P_{st} for the *b02* benchmark and considered operating conditions. Similar trend has been obtained for the NOT chain. The P_{st} profile has been normalized over the $SPDC_0$. As we can see, the relative P_{st} reduction over time is noticeable. After only 1 month of operation, P_{st} drops well below 50% of $SPDC_0$. It further reduces to less than 30% after 1 year and, after 10 years of operation, static power falls below 20% of $SPDC_0$ for all operating conditions.

The obtained HSPICE simulation results confirm that static power is considerably benefited by ST NBTI aging. To further support this beneficial effect, we have measured actual I_{leak} using a test-chip manufactured with TSMC 65nm technology.



(a)

Fig. 4. (a) Test-chip floorplan; (b) experiment set-up; (c) normalized measurement results.

Its design floorplan is depicted in Fig. 4(a). The experimental set-up is shown in Fig. 4(b). The V_{dd} of the test-chip is connected to 1.2V power supply through a Digital Multimeter (DMM), whose range and resolution are set to 200uA and 0.1uA, respectively. The oscilloscope measures the voltage of the supply rail and the virtual rail. The leakage current of the test-chip is measured by the DMM in the power gated domain containing processor (CM0L1) and two banks of registers, when the STs are all turned off. The voltage drop across the STs is calculated by the difference in measurements between two oscilloscope channels. The effective age of the test-chip is approximately equal to 1 day. Consider that the resolution of the multimeter employed in our experiment does not allow us to measure the leakage current with the desired accuracy. Table II reports the obtained measurement results.

It should be noted that the different chip temperatures during measurements have a big impact in the determination of the actual I_{leak} values. In order to highlight the I_{leak} relative reduction over time as a function of NBTI aging, and suppress the effect of different measurement temperatures, we have normalized the obtained data by a factor derived from (2). Denoting by I_{leak-i} and T_i (with $i = 1 \ldots 5$) leakage current and chip temperature at the $i-th$ measurement, respectively, the normalization and scale factor NSF_i is:

$$NSF_i = I_{leak-1} e^{\frac{qV_{th}(T_i - T_1)}{nkT_1T_i}} \left(\frac{T_i}{T_1}\right)^2, \text{with } i = 1 \ldots 5.$$

The normalized data are plotted in Fig. 4(c) for different values of the parameter n [1]. A clear I_{leak} decrease over time is exhibited, which is in the range 5.4%-8.9% after 526 hours of operation, depending on the value of parameter n. This decrease, however, is smaller than that found by simulation using a 32nm CMOS technology. In this regard, it should be considered that circuits implemented with smaller technology nodes usually exhibit a larger NBTI aging degradation [3] and, as a consequence, a more evident leakage current reduction over time.

2) ST Switch Efficiency: Leakage current reduction due to NBTI aging previously highlighted leads to an improvement in ST switch efficiency $SwE = I_{on}/I_{off}$, where $I_{off} = I_{leak}$. In fact, both I_{on} and I_{off} decrease over time due to NBTI aging: I_{on} decreases almost linearly with the increase of ST

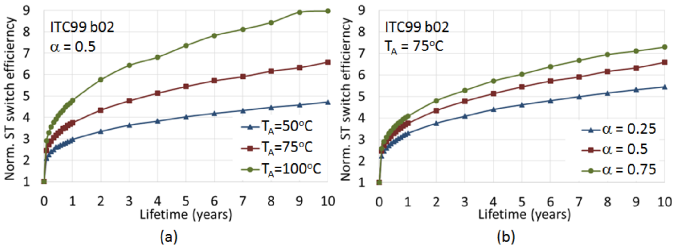


Fig. 5. Profile of the normalized ST switch efficiency over time for *b02* benchmark (normalization factor: $SwEDC_0(b02) = 1.02 \times 10^7$) with: (a) different aging temperatures; (b) different stress ratios.

threshold voltage, while I_{off} decreases exponentially. As a result, SwE increases over time with respect to the value identified at design stage. We will refer to this value as *switch efficiency design constraint at t0*, and denote it by $SwEDC_0$. Fig. 5 depicts the trend over time of SwE for the *b02* benchmark and the considered operating conditions. A similar trend has been obtained for the NOT chain. The ST efficiency profiles have been normalized over $SwEDC_0$. The NBTI aging benefits for ST switch efficiency are noticeable: SwE increases up to $2\times$ after 1 month of operation, and up to $4.9\times$ after 1 year. Over 10 years of operation, the SwE improvement ranges between $4.8\times$ and $9\times$, depending on the operating conditions.

C. Power Switch NBTI Aging Detrimental Effects

As highlighted in the previous subsection, NBTI aging causes a decrease in ST I_{on}. This can be modeled also as an increase in ST equivalent resistance. When a power-gated circuit is active, STs are ON and operate in triode region. The equivalent resistance of an active ST can be expressed as:

$$R_{ST} \propto [(W/L)\,\mu_p C_{ox}\,(V_{dd} - V_{th})]^{-1}. \quad (3)$$

R_{ST} increases as ST degrades, and so does the IR drop between its source (V_{dd} in Fig. 1(a)) and drain (VV_{dd} in Fig. 1(a)), when the current drained by the power-gated circuit flows through it. As a consequence, the following NBTI aging detrimental effects are experienced: increase in propagation delay of power gated circuits and possible consequent decrease of their lifetimes (during active mode); increase in charging delay of VV_{dd} network (during wake-up protocol).

1) Propagation Delay and Lifetime: In order to assess the ST NBTI aging impact on propagation delay, IR drop has been evaluated by considering the worst case active current drained by the circuit at $t0$. Relative increase of worst case propagation delay τ_{wc} over the value exhibited at $t0$ ($\tau_{wc0}(b02) = 52.8ps$ and $\tau_{wc0}(NOT) = 113.2ps$) is reported in Table III for 1 month, 1 year, 5 years and 10 years lifetime (LT). The same operating conditions as described in Sec. III-A have been considered. For the *b02* benchmark, propagation delay increase may exceed 12% after the first month of operation, while for the NOT chain this degradation is in the range 8%-10.5%. Depending on the operating conditions, delay degradation may reach 15% (14%) after 1 year for the *b*02 benchmark (NOT chain), and approximates 20% (18%) after 10 years.

If this performance degradation exceeds the circuit time margin, it may eventually lead to a delay fault, thus circuit

TABLE III
WORST CASE PROPAGATION DELAY INCREASE AS A FUNCTION OF LIFETIME LT, AGING TEMPERATURE T_A AND STRESS RATIO α FOR *b02* BENCHMARK AND NOT CHAIN ($\Delta = [\tau_{wc}(LT) - \tau_{wc}(t0)]/\tau_{wc}(t0)$).

LT	$\Delta\tau_{wc}$ (%)											
	T_A ($\alpha = 0.5$)						α ($T_A = 75^oC$)					
	50^oC		75^oC		100^oC		0.25		0.5		0.75	
	b02	NOT	b02	NOT	b02	NOT	b02	NOT	b02	NOT	b02	NOT
1m	11.5	8.5	12.3	10.1	12.5	10.5	12.1	8.2	12.3	10.1	12.6	10.3
1y	12.5	10.3	14.5	12.8	15.3	14.3	13.6	10.4	14.5	12.8	14.9	13.5
5y	13.9	11.2	15.5	14.3	17.6	16.2	14.6	11.6	15.5	14.3	16.4	14.9
10y	14.8	12.0	17.1	15.2	19.4	17.8	15.2	12.2	17.1	15.2	17.5	16.3

lifetime shortening. Let us define circuit maximum lifetime (LT_{max}) as the time required by a circuit to degrade its performance by 15% with respect to its worst case propagation delay at $t0$, τ_{wc0}. In fact, we can consider that a 15% time margin is added to τ_{wc0} in order to determine the clock period T_{CK}, accounting for a degradation induced by PVT variations [8]. It is: $\tau_{wc}(LT_{max}) = T_{CK} = 1.15 \cdot \tau_{wc0}$. Maximum lifetime varies noticeably for the considered case studies and operating conditions. It ranges from 0.94 years ($T_A = 100^oC$ and $\alpha = 0.5$) to 11.3 years ($T_A = 50^oC$ and $\alpha = 0.5$) for the *b02* benchmark. For the NOT chain, it is limited to 3 years for $T_A = 100^oC$ and $\alpha = 0.5$, while it does not present any actual limitation for $T_A = 50^oC$. Therefore, we can conclude that lifetime limitation due to NBTI aging strongly depends on circuit and operating conditions. If also NBTI aging of power-gated logic had been taken into account, its effect would have augmented the detrimental/beneficial effects discussed so far. Moreover, if the impact of process variations on propagation delay was considered, time margins might have been violated even for shorter lifetimes.

It is worth pointing out that NBTI may induce some skew in the clock signals due to aging affecting clock drivers within clock distribution network [31], [32], both at global and local level. However, the clock frequency will remain unaltered. At local level, if we reasonably assume that clock signals coming from the same branch of the clock tree are used to trigger input and output flops, the timing margin of the circuit will not be appreciably affected by NBTI aging, and the probability of having a delay fault induced by ST aging will not be impacted.

2) VV_{dd} Charge Delay: The first step of the *wake-up* protocol (Fig. 1) consists on the restoration of the proper VV_{dd} value. In actual designs, where multiple STs are employed, this protocol is more elaborated and usually embeds a procedure based on a daisy-chain mechanism to prevent excess current (*rush current*) during wake-up. The detailed analysis of rush current on wake-up sequence it out of the scope of this paper, which focuses on NBTI-induced degradation over the circuit characteristics exhibited at $t0$. More details on wake-up protocol and rush current effect can be found in [1]. It is of utmost importance to estimate the relative increase of VV_{dd} *charge delay* τ_{VVdd} due to NBTI aging affecting STs, in order to prevent the timing constraints of the wake-up protocol from being violated. Table IV reports relative increase over the value exhibited at $t0$ ($\tau_{VVdd0} \simeq 32.4ps$) for the *b02* benchmark. LT values and operating conditions are the same as considered previously. Analogous trend has been found for the NOT chain. The degradation exhibited by the VV_{dd} charge

TABLE IV
VV_{dd} CHARGE DELAY INCREASE AS A FUNCTION OF LIFETIME LT, AGING TEMPERATURE T_A AND STRESS RATIO α FOR *b02* BENCHMARK ($\Delta = [\tau_{VVdd}(LT) - \tau_{VVdd}(t0)]/\tau_{VVdd}(t0)$).

LT	$\Delta\tau_{VVdd}$ (%)					
	T_A ($\alpha = 0.5$)			α ($T_A = 75^oC$)		
	50^oC	75^oC	100^oC	0.25	0.5	0.75
1m	11.2	13.9	18.5	12.5	13.9	15.2
1y	21.8	27.2	32.6	24.1	27.2	28.8
5y	28.9	35.5	43.6	31.0	35.5	38.2
10y	31.7	40.2	50.1	34.7	40.2	43.5

delay is noticeable, and varies considerably with the operating conditions. It shows a greater sensitivity to aging temperature T_A than to stress ratio α. The increase of τ_{VVdd} ranges from 10% to 20% after only 1 month of operation and, in the worst case, it reaches 50% after 10 years.

IV. PROPOSED STRATEGY FOR ST DESIGN

The ST NBTI aging beneficial effects on static power (ST switch efficiency), which reduces (increases) over time well below (above) the identified design constraint $SPDC_0$ ($SwEDC_0$) have been so far ignored by power gating techniques. We propose to trade-off part of these benefits in order to counteract NBTI aging detrimental effects. This can be achieved by designing STs with a lower V_{th}, either by re-designing the power switching fabric (device level approach, suitable for the development of future power switching fabrics), or by applying a proper forward body bias to available power switching fabrics (circuit level approach). An ST with lower V_{th} will exhibit a lower resistivity, thus a lower IR drop. This allows designers either to extend circuit lifetime and increase long-term reliability, or to increase performance, or even to reduce power network cost by downsizing the STs.

The ST threshold voltage and static power profiles of the proposed approach are qualitatively depicted in Figs. 6(a)(b), respectively (blue solid lines). Due to the lower initial V_{th}, a higher P_{st} at the very early stage of lifetime is exhibited. Nevertheless, as V_{th} increases due to NBTI aging, the P_{st} rapidly drops and reaches the break-even with the design constraint $SPDC_0$ (red dashed line) at t_{BE}. For $t \geq t_{BE}$, the P_{st} of the proposed ST design becomes even lower than the expected $SPDC_0$.

The proper ST V_{th} value can be determined accounting for burn-in test. The stress conditions usually applied during burn-in (high temperature and voltage) induce a significant NBTI degradation (V_{th} increase) [10], [11]. The method to determine the ST V_{th} for the proposed design approach can be qualitatively explained through Fig. 6. Let t_{BI} be the burn-in duration (the initial time instant is set to 0), $V_{th}^{prop}(t0)$ the initial threshold voltage value of the proposed ST design, and V_{th0}^{std} the initial threshold voltage of a standard high-V_{th} ST. The threshold voltage $V_{th}^{prop}(t0)$ is selected so that, as a consequence of NBTI degradation, V_{th}^{prop} reaches V_{th0}^{std} (break-even point) at the end of the burn-in test (at $t_{BI} = t_{BE}$ in Fig. 6(a)). In fact, if size and bias conditions of the proposed ST design are the same as in the standard case, it is:

$$P_{st}^{prop}(t_{BI}) = SPDC_0 \iff \iff V_{th}^{prop}(t_{BI}) = V_{th0}^{std}. \quad (4)$$

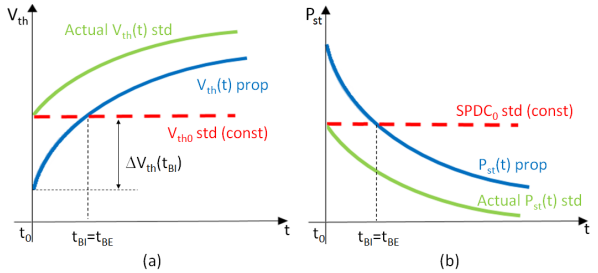


Fig. 6. Schematic representation of the proposed method to determine ST V_{th} optimal value: (a) qualitative V_{th} trend over time for the proposed (prop) and standard (std) ST design, and (b) correspondent static power trend.

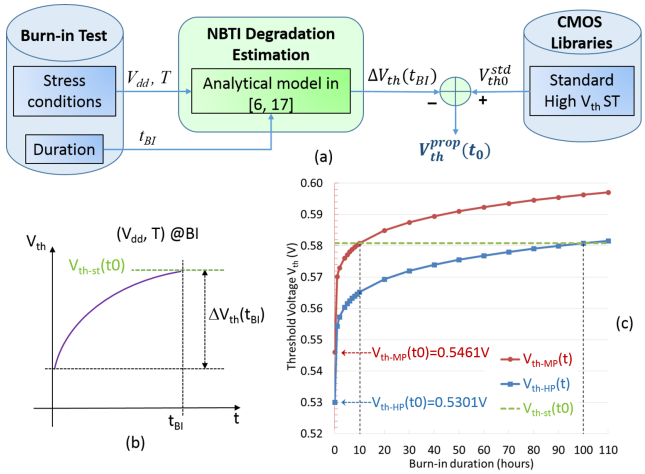


Fig. 7. (a) Flow of the proposed ST V_{th} determination approach; (b) threshold voltage degradation during burn-in; (c) V_{th} drift over time for the two considered burn-in conditions.

TABLE V
IDENTIFICATION OF THRESHOLD VOLTAGE FOR MP AND HP ST DESIGNS ACCOUNTING FOR BURN-IN STRESS ($V_{th0}^{std} = 0.5808V$ [18]).

Burn-in test stress condition			NBTI-induced V_{th} degradation	V_{th} for proposed ST design
T_{BI}	V_{dd}	t_{BI}	ΔV_{th}	V_{th}^{prop}
105^oC	$1.3V$	10h	$47mV$	MP: 0.5461V
		100h	$70mV$	HP: 0.5301V

This way, the static power exhibited by a power-gated circuit during its effective lifetime ($t > t_{BE}$ in Fig. 6(b)) turns out to be considerably lower than the expected $SPDC_0$.

The flow of the proposed method is represented in Fig. 7(a). The threshold voltage degradation during burn-in test, denoted by $\Delta V_{th}(t_{BI})$ (Fig. 7(b)), can be properly estimated given burn-in stress conditions (temperature and voltage) and duration by means of the model in (1). The threshold voltage V_{th0}^{std} is extracted from the used CMOS library. The (initial) threshold voltage of the ST for the proposed design strategy is then computed as: $V_{th}^{prop}(t0) = V_{th0}^{std} - \Delta V_{th}(t_{BI})$.

Different stress conditions (V_{dd} and temperature T_{BI}) and duration (t_{BI}) may characterize burn-in test. The considered stress conditions, as reported in [33], together with the derived degradation ΔV_{th} and identified threshold voltage V_{th}^{prop} are summarized in Table V. The two derived V_{th}^{prop} values for the two considered burn-in durations are $V_{th1}^{prop}(t0) = 0.5461V$, hereafter referred to as MP (medium performance) ST design; $V_{th2}^{prop}(t0) = 0.5301V$, hereafter referred to as HP (high

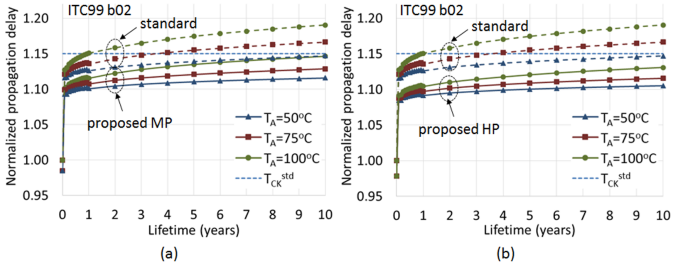


Fig. 8. Profile over time of the normalized propagation delay for the *b02* benchmark (normalization factor: $\tau_{wc0}(b02) = 52.8ps$) with: (a) MP ST design; (b) HP ST design.

performance) ST design. Fig. 7(c) depicts the threshold voltage drift over time for the two considered burn-in conditions and the two identified initial threshold voltages for both MP and HP ST designs.

V. Validation and Comparison

The proposed ST design strategy has been validated by means of HSPICE simulations. To this end, the same simulation set-up as described in Sec. III has been considered. For the sake of simplicity, we report only the results obtained for different aging temperature T_A. Nevertheless, in the previous section we have seen that T_A dominates over α in determining the circuit characteristics. All simulation results are normalized considering the same normalization factors as in Sec. III.

A. Lifetime and VV_{dd} Charge Delay

Fig. 8 depicts the normalized worst case propagation delay τ_{wc} trend over time. For the sake of space limitation, only the results for the *b02* benchmark are shown, both for the MP and HP design (solid lines). The results for the standard ST design (dashed lines) are also shown for direct comparison. We can see that the τ_{wc} is considerably lower than in the standard case, and varies noticeably with aging temperature. It is in the range 1.09-1.15 for the MP design for all aging temperatures, while it is between 1.07 and 1.13 for the HP design. For all shown operating time interval, τ_{wc} is lower than the T_{CK}^{std} utilized to estimate circuit lifetime (1.15), as defined in Sec. III.

We have evaluated more in detail the lifetime extension enabled by the proposed ST deigns for different operating conditions. Particularly, we have identified the following three meaningful conditions:

- *Worst case* condition (WC), characterized by aging temperature and stress ratio (among those considered in our analysis) inducing the highest degradation: $T_A = 100^oC$, $\alpha = 0.75$;
- *Nominal* condition (*Nom*), characterized by aging temperature and stress ratio that can be considered typical for many applications: $T_A = 75^oC$, $\alpha = 0.5$
- *Best case* condition (BC), characterized by aging temperature and stress ratio inducing the lowest degradation: $T_A = 50^oC$, $\alpha = 0.25$.

In Table VI, we report the lifetime increase ('LT ext.') compared to a standard (Std) approach based on high-V_{th} STs. For the *b02* benchmark, it ranges from $9.1\times$ for MP design in the *nominal* condition, to $25.2\times$ for HP design in the *worst case* condition. If the NOT chain is considered, the lifetime increase is in the range $8.3\times$-$25.2\times$ for MP design in the *nominal* condition and HP design in *worst case* condition, respectively. In the *best case* condition, there is no need to increase circuit lifetime, which is already much longer than what could be reasonably expected from an electronic system. However, as we will show in Sec. V-C, the proposed ST design strategy allows us to achieve better lifetime-performance-cost trade-offs compared to the standard design also in this case.

TABLE VI
Lifetime (LT) increase over a standard design.

Operating conditions	Std design LT		MP design LT ext.		HP design LT ext.	
	b02	NOT	b02	NOT	b02	NOT
WC	0.86y	1.88	$10.2\times$	$9.4\times$	$25.2\times$	$21.8\times$
Nom	3.49y	8.45y	$9.1\times$	$8.3\times$	$21.6\times$	$20.6\times$
BC	24.5y	60.9y	$9.9\times$	$10.2\times$	$22.3\times$	$20.8\times$

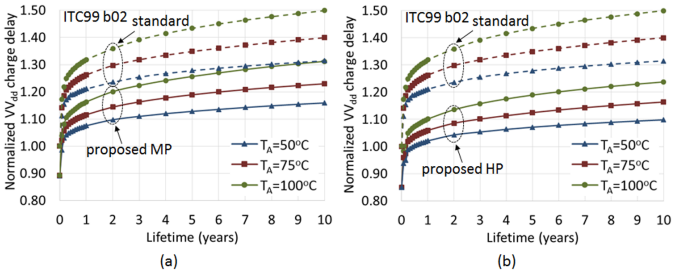


Fig. 9. Profile over time of the normalized VV_{dd} charge delay during the wake-up protocol for the *b02* benchmark (normalization factor: $\tau_{VVdd0}(b02) = 32.4ps$) with: (a) MP ST design; (b) HP ST design.

In Fig. 9, we report the results for the normalized VV_{dd} charge delay exhibited during wake-up protocol by the *b02* benchmark (solid lines). The results for the standard ST design are also shown (dashed lines). The equivalent aspect ratio of the STs is that determined in Sec. III ($S_{ST}(b02) = 110$). Analogous results have been found for the NOT chain. The normalized τ_{VVdd} is in the range 1.08-1.17 (1.01-1.10) for the MP (HP) design after 1 year of operation, and reaches 1.16-1.32 (1.10 - 1.24) after 10 years. Compared to the standard ST design, the τ_{VVdd} reduction enabled by the proposed design strategy reaches 12% for the MP design and 18% for the HP design. This allows designers to reduce the timing margins during *wake-up* protocol (Fig. 1(b)), thus reducing the impact of power gating implementation on circuit performance.

B. Static Power and ST Switch Efficiency

In this subsection, we assess the impact of the proposed ST design strategy on static power/energy (P_{st}, E_{st}) and ST switch efficiency, and we compare it with the respective design constraints. Fig. 10 shows the static power trend over time for the *b02* benchmark and the considered operating conditions, for both MP and HP design. For comparison purposes, we have evaluated the excess static power (compared to what is expected) exhibited by the proposed ST designs at very early lifetime as it was consumed during effective lifetime (and not during burn-in). In the MP case, the P_{st} is well below the $SPDC_0$ identified without considering NBTI effect after only 1 year of operation. It is in the range $40\% - 70\%$ of

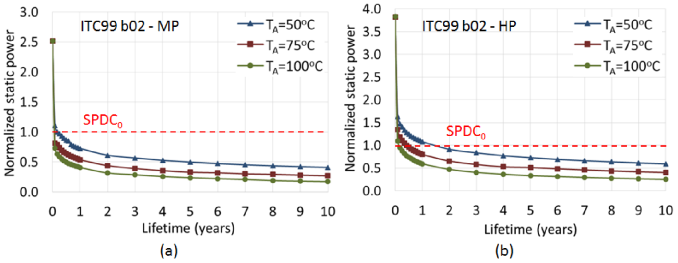


Fig. 10. Profile over time of the normalized static power for the *b02* benchmark (normalization factor: $SPDC_0(b02) = 64.5pW$) with: (a) MP ST design; (b) HP ST design.

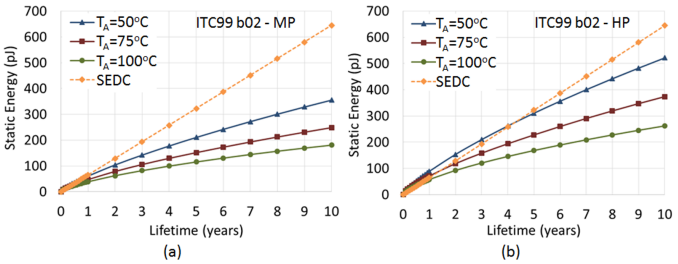


Fig. 11. Profile over time of static energy for the *b02* benchmark with: (a) MP ST design; (b) HP ST design.

$SPDC_0$, depending on the operating conditions, and drops below 50% of $SPDC_0$ after 10 years of operation. For the HP design, the P_{st} is slightly higher: it is approximately equal to, or below, $SPDC_0$ after 1 year, and around 50% of $SPDC_0$ after 10 years. As expected, the more NBTI degradation ($T_A = 100^oC$), the more P_{st} reduction over time.

The energy efficiency of the proposed ST design strategy has been assessed also by evaluating the static energy E_{st} consumption for a circuit operating up to 10 years. The E_{st} consumed for $t < t_{BE}$ (Fig. 6) has been also accounted for. The obtained results are depicted in Fig. 11 for the *b02* benchmark with MP and HP ST design. Very similar results have been obtained also for the NOT chain. We also report the E_{st} expected to be consumed if a standard design NBTI-unaware ST design is adopted. It is referred to as *static energy design constraint*, and denoted by $SEDC$. For the MP design (Fig. 11(a)), E_{st} is clearly lower than $SEDC$ even after only 1 year lifetime for all considered operating conditions. The E_{st} reduction varies considerably with the aging temperature. It is in the range 5.5%-39.6% after 1 year, 34.7%-64.2% after 5 years, and 44.9%-72% after 10 years of operation. For the HP design (Fig. 11(b)), the $SEDC$ is reached after an operating time ranging between 0.75 years ($T_A = 100^oC$) and 4 years ($T_A = 50^oC$). After 10 years, the E_{st} reduction over the $SEDC$ is in the interval 19.1%-59.3% for the different operating conditions.

In Fig. 12, we show the trend over time of the normalized ST switch efficiency (SwE) for the *b02* benchmark and the considered operating conditions, for both MP design and HP design. In the MP case (Fig. 12(a)), SwE is above $SwEDC_0$ after less than 1 month for $T_A = 75^oC$ and $T_A = 100^oC$, and less than 2 months for $T_A = 50^oC$. It is in the range of 2.23×-4.77× after 10 years of lifetime. For the HP design (Fig. 12(b)), the break-even point is reached for a lifetime in the range 2 months - 1 year. At 10 years, the SwE improvement

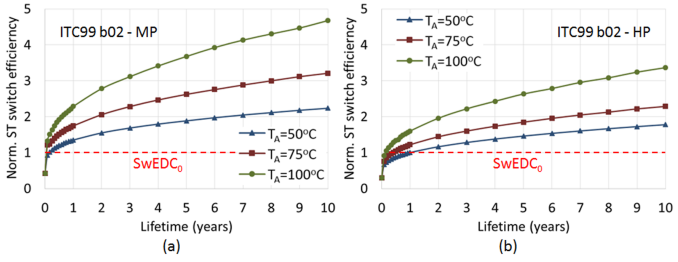


Fig. 12. Profile over time of normalized ST switch efficiency for the *b02* benchmark (normalization factor: $SwEDC_0 = 1.02 \times 10^7$) with: (a) MP ST design; (b) HP ST design.

TABLE VII
OPERATING FREQUENCY INCREASE FOR 5 AND 10 YEAR LT
($\Delta = [f_{CK}^{max}(HP, MP) - f_{CK}^{std}]/f_{CK}^{std}$)

Circuit (WC)	Std design T_{CK}	Δf_{CK}@5y MP	Δf_{CK}@5y HP	LT ext @5y	Δf_{CK}@10y MP	Δf_{CK}@10y HP	LT ext @10y
b02	52.8ps	4.4%	8.3%	5.8×	0.9%	2.5%	11.6×
NOT	113.2ps	5.8%	9.9%	2.7×	4.9%	6.0%	5.4×

over the expected $SwEDC_0$ may reach 3.36×.

C. Lifetime-Performance-Cost Trade-offs

Lifetime improvements reported in Table VI would lead to a circuit lifetime excessively long for many applications, even in the worst case conditions, as defined in Sec. V-A. Therefore, let us consider a reasonable, maximum lifetime target (LT_{max}) for the considered case studies of either 5 years or 10 years, to be guaranteed in the worst case conditions. These values represent a noticeable increase in circuit lifetime over standard power-gating approach, as evaluated in Sec. III: from 2.7× for the NOT chain for the MP design and $LT_{max} = 5$ years, to 11.6× for the *b02* benchmark and $LT_{max} = 10$ years.

The identification of a maximum lifetime target enables to increase the operating frequencies, thus improving performance, while keeping the size of the ST at the values identified in Sec. III. In fact, as represented in Fig. 8, there are margins to operate the considered circuits at higher frequencies, yet satisfying the lifetime target. Therefore, we can identify the maximum operating frequency f_{CK}^{max} such that:

$$1/f_{CK}^{max} = \tau_{wc}(LT_{max}), \text{ with } LT_{max} = 5y, 10y. \quad (5)$$

Table VII reports the obtained results. As can be seen, the operating frequency for the HP design can be increased up 8.3% (9.9%) for a lifetime target of 5 years, for the *b02* benchmark (NOT chain) with respect to a standard ST design. With an MP design, 4.4% (5.8%) frequency increase for the *b02* benchmark (NOT chain) can be achieved.

Alternatively, a reduction of the ST area with respect to a standard power gating approach can be pursued. In this case, the frequency is fixed at the value identified in Sec. III. By reducing the ST size, its resistance increases, so does the IR drop. As a result, the propagation delay of the power-gated circuit increases as well. Therefore, the ST size can be reduced down to a minimum value S_{STeq}^{min}, yet fulfilling the LT_{max} targets, so that:

$$\tau_{wc}(LT_{max}) = 1/f_{CK}^{std}, \text{ with } LT_{max} = 5y, 10y. \quad (6)$$

The obtained results are reported in Table VIII. The HP design

TABLE VIII
ST AREA REDUCTION FOR 5 AND 10 YEAR LT
($\Delta = [A_{ST}^{std} - A_{ST}(HP, MP)]/A_{ST}^{std}$)

Circuit (WC)	Std design S_{STeq}	ΔA_{ST}@5y MP	ΔA_{ST}@5y HP	LT ext @5y	ΔA_{ST}@10y MP	ΔA_{ST}@10y HP	LT ext @10y
b02	110	10.0%	18.8%	5.8×	3.3%	5.7%	11.6×
NOT	38	10.4%	19.8%	2.7×	3.9%	7.1%	5.4×

TABLE IX
LT EXTENSION AND AVERAGE P_{st} VARIATION OVER A STANDARD ST DESIGN, IN THE NOMINAL CASE OPERATING SCENARIO.

Circuit	Standard		MP design		HP design	
	LT (years)	P_{st}^{av}	LT ext	ΔP_{st}^{av}	LT ext	ΔP_{st}^{av}
c432	7.1	230pW	7.8×	-8.8%	16.5×	-19.7%
c499	5.3	245pW	9.1×	-12.4%	18.9×	-22.3%
c1355	6.8	734pW	8.2×	-9.1%	17.0×	-21.1%
c6288	6.3	5.51nW	7.7×	-9.0%	16.7×	-20.2%
c7552	5.6	6.10nW	7.9×	-8.5%	17.1×	-19.4%
s38417	6.9	35.2nW	7.5×	-8.8%	16.2×	-19.8%
b18	6.5	197.1nW	7.1×	-8.6%	16.0×	-19.2%
avg	-	-	7.9×	-9.3%	16.9×	-20.2%

enables up to 18.8% (19.8%) ST area reduction for the *b02* benchmark (NOT chain) for a target of 5 years of operation. These values represent approximately 2.2% of the area of the overall circuit for both cases. Area saving offered by the MP reaches 10.0% (10.5%) for the *b02* benchmark (NOT chain), which is approximately 1.2% of the area of overall circuit for both case studies.

D. Validation of the Proposed ST Design for Larger Circuits

We further validated the proposed ST design considering benchmarks from ISCAS85 and IWLS05 benchmark suites. The obtained HSPICE simulation results, reported in Table IX, confirm those for *b02* benchmark and NOT chain. As can be seen, an average $16.9\times$ ($7.9\times$) LT extension for the HP (MP) design can be achieved, with a 20.2% (9.3%) average (per year of lifetime) static power reduction over the respective static power design constraint $SPDC_0$. These results, obtained with no additional ST area overhead, represent an improvement with respect to those reported in [8], [9] (obtained for different technologies and different power gating strategies), which also imply an increase in ST area overhead with respect to a standard power gating technique. Similarly to the *b02* benchmark and NOT chain, different lifetime-performance-cost trade-offs can be achieved if we identify a lifetime target to be guaranteed in the worst-case condition, as defined in Sec. V-A. The obtained results are reported in Table X. If a LT target of 5 years is considered, the proposed HP (MP) ST design offers either an average 8.2% (4.0%) increase in operating frequency, or a 17.0% (10.3%) ST area reduction with respect to a standard power gating approach. For 10 years LT target, the proposed HP (MP) ST design enables either to increase the operating frequency by an average 5.3% (1.7%) on average, or to reduce ST area overhead by 7.6% (6.6%).

VI. CONCLUSIONS

In this paper, we showed that sleep transistor (ST) aging presents noticeable beneficial effects on static power and ST switch efficiency, whose magnitudes depend on operating conditions. The beneficial effect on static power has been proven also by means of experimental measurements. Based on this feature, we proposed a new ST design strategy for reliable power gating, which offers better cost-reliability trade-offs compared to alternative approaches based on either ST oversize, or adaptive body bias. Through HSPICE simulations, we showed a lifetime (thus long-term reliability) improvement up to $21.4\times$ and average static power reduction up to 16.3% compared to a standard ST design approach, with no additional area overhead. Moreover, if a maximum target lifetime of either 5 or 10 years is considered, our proposed ST design strategy enables either to improve circuit operating frequency up to 9.9%, or to reduce ST area overhead up to 19.8%.

TABLE X
ST AREA REDUCTION FOR 5 AND 10 YEAR LT, IN THE WORST CASE OPERATING SCENARIO.

Circuit	MP				HP			
	Δf_{CK}		ΔA_{ST}		Δf_{CK}		ΔA_{ST}	
	@5y	@10y	@5y	@10y	@5y	@10y	@5y	@10y
c432	3.2%	0.5%	9.4%	6.1%	7.7%	4.9%	16.8%	7.1%
c499	4.1%	1.9%	11.2%	7.5%	9.2%	6.3%	18.8%	8.4%
c1355	4.5%	3.1%	10.9%	7.0%	8.7%	5.7%	17.2%	8.0%
c6288	4.0%	1.6%	10.5%	6.7%	8.1%	5.3%	16.8%	7.8%
c7552	3.8%	1.1%	10.1%	6.2%	7.7%	4.8%	16.1%	6.9%
s38417	4.2%	1.7%	10.4%	6.8%	8.0%	4.9%	16.5%	7.2%
b18	4.0%	1.9%	9.9%	6.0%	7.9%	5.0%	17.1%	7.6%
avg	4.0%	1.7%	10.3%	6.6%	8.2%	5.3%	17.0%	7.6%

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REFERENCES

[1] D. Flynn, R. Aitken, A. Gibbons, and K. Shi, *Low Power Methodology Manual: For System-on-Chip Design*. NY, USA: Springer-Verlag, 2007.
[2] "The International Technology Roadmap for Semicopnductors - Edition 2013," http://www.itrs.net/LINKS/2013ITRS/Home2013.htm.
[3] H. Yi, T. Yoneda, M. Inoue, Y. Sato, S. Kajihara, and H. Fujiwara, "A failure prediction strategy for transistor aging," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 11, pp. 1951–1959, 2012.
[4] S. Borkar, "Electronics beyond nano-scale cmos," in *Proc. of IEEE/ACM Design Automation Conference (DAC)*, 2006, pp. 807–808.
[5] M. Agarwal, V. Balakrishnan, A. Bhuyan, K. Kim, B. C. Paul, W. Wang, B. Yang, Y. Cao, and S. Mitra, "Optimized circuit failure prediction for aging: Practicality and promise," in *Proc. of IEEE International Test Conf. (ITC)*, 2008, pp. 1–10.
[6] M. Omaña, D. Rossi, N. Bosio, and C. Metra, "Low cost nbti degradation detection and masking approaches," *IEEE Trans. on Computers*, vol. 62, no. 3, pp. 496–509, 2013.
[7] W. Wang, Z. Wei, S. Yang, and Y. Cao, "An efficient method to identify critical gates under circuit aging," in *Proc. of IEEE/ACM International Conf. on Computer-Aided Design (ICCAD)*, 2007, pp. 735–740.
[8] A. Calimera, E. Macii, and M. Poncino, "Design techniques for nbti-tolerant power-gating architectures," *IEEE Trans. on Circuits and Systems II: Express Brief*, vol. 59, no. 4, pp. 249–253, 2012.
[9] K. Wu, I. Lin, Y. Wang, and S. Yang, "Bti-aware sleep transistor sizing algorithm for reliable power gating designs," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 10, pp. 1591–1595, 2014.
[10] N. Sumikawa, L.-C. Wang, and M. S. Abadir, "An experiment of burn-in time reduction based on parametric test analysis," in *Proc. of IEEE International Test Conf. (ITC)*, 2012, pp. 1–10.
[11] A. Chakraborty and D. Z. Pan, "Controlling nbti degradation during static burn-in testing," in *Proc. of the IEEE 16th Asia and South Pacific Design Automation Conf.*, 2011, pp. 597–602.

[12] H. S. Deogun, D. Sylvester, R. Rao, and K. Nowka, "Adaptive mtcmos for dynamic leakage and frequency control using variable footer strength," in *Proc. of IEEE International SOC Conf.*, 2005, pp. 147–150.
[13] H.-O. Kim and Y. Shin, "Semicustom design methodology of power gated circuits for low leakage applications," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 54, no. 6, pp. 512–516, 2007.
[14] A. Sinkar and N. S. Kim, "Analyzing and minimizing effects of temperature variation and nbti on active leakage power of power-gated circuits," in *Proc. of 11th International Symp. on Quality Electronic Design (ISQED)*, 2010, pp. 791–796.
[15] S. Narendra, D. Antoniadis, and V. De, "Impact of using adaptive body bias to compensate die-to-die vt variation on within-die vt variation," in *Proc. of the International Symp. on Low Power Electronics and Design*. ACM, 1999, pp. 229–232.
[16] D. Rossi, V. Tenentes, S. Khursheed, and B. M. Al-Hashimi, "Nbti and leakage aware sleep transistor design for reliable and energy efficient power gating," in *Proc. of IEEE European Test Symposium (ETS)*, 2015, pp. 1–6.
[17] D. Rossi, V. Tenentes, S. Khursheed, and B. Al-Hashimi, "Bti and leakage aware dynamic voltage scaling for reliable low power cache memories," in *Proc. of IEEE 21st InternationalOn-Line Testing Symposium (IOLTS)*, 2015, pp. 194–199.
[18] "Predictive Technology Model (PTM)," http://www.ptm.asu.edu.
[19] C. Prasad, "Advanced cmos reliability challenges," in *Proc. of IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, 2014, pp. 1–2.
[20] B. Choelhwyi and *et al.*, "Sram stability design comprehending 14nm finfet reliability," in *Proc. of IEEE International Reliability Physics Symposium (IRPS)*, 2015, pp. MY.13.1–MY.13.5.
[21] S. K. Krishnappa and H. Mahmoodi, "Comparative bti reliability analysis of sram cell designs in nano-scale cmos technology," in *Proc. of IEEE International Symposium on Quality Electronic Design (ISQED)*, 2011, pp. 384–389.
[22] S. Khan, S. Hamidioui, H. Kukner, P. Raghavan, and F. Catthoor, "Bti impact on logical gates in nano-scale cmos technology," in *Proc. of IEEE International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)*, 2012, pp. 348–353.
[23] M. A. Alam, H. Kufluoglu, D. Varghese, and S. Mahapatra, "A comprehensive model for pmos nbti degradation: Recent progress," *Microelectronics Reliability*, vol. 47, no. 6, pp. 853–862, 2007.
[24] K. Joshi, S. Mukhopadhyay, N. Goel, and S. Mahapatra, "A consistent physical framework for n and p bti in hkmg mosfets," in *Proc. of IEEE International Reliability Physics Symposium (IRPS)*, 2012, pp. 5A.3.1–5A.3.10.
[25] H.-I. Yang, W. Hwang, and C.-T. Chuang, "Impacts of nbti/pbti and contact resistance on power-gated sram with high-metal-gate devices," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 7, pp. 1192–1204, 2011.
[26] V. Tenentes, D. Rossi, , S. Khursheed, S. Yang, and B. M. Al-Hashimi, "Dft architecture with power-distribution-network consideration for delay-based power gating test," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, early access*, vol. 34, no. 12, pp. 2013–2024, 2015.
[27] V. Tenentes, S. Khursheed, B. Al-Hashimi, S. Zhong, and S. Yang, "High quality testing of grid style power gating," in *Proc. of 2014 IEEE 23rd Asian Test Symposium (ATS)*, 2014, pp. 186–191.
[28] V. Tenentes, D. Rossi, S. Khursheed, and B. Al-Hashimi, "Diagnosis of power switches with power-distribution-network consideration," in *Proc. of 20th IEEE European Test Symposium (ETS)*, 2015, pp. 1–6.
[29] D. Rossi, M. Omaña, C. Metra, and A. Paccagnella, "Impact of aging phenomena on soft error susceptibility," in *Proc. of IEEE International Symp. on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, 2011, pp. 18–24.
[30] ——, "Impact of bias temperature instability on soft error susceptibility," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 4, pp. 743–751, 2015.
[31] S. Tam, S. Rusu, U. Nagarji Desai, R. Kim, J. Zhang, and I. Young, "Clock generation and distribution for the first ia-64 microprocessor," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 11, pp. 1545–1552, Nov 2000.
[32] C. Metra, D. Rossi, and T. Mak, "Won't on-chip clock calibration guarantee performance boost and product quality?" *IEEE Transactions on Computers*, vol. 56, no. 3, pp. 415–428, March 2007.
[33] (March 2012) Production Release Qualification Report. [Online]. Available: https://qdms.intel.com/prq/prq.aspx/B756408D-E58E-4656-92A9-47AA9A7D8AC3/PRQ_9038b.pdf

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