UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Optoelectronics Research Centre

Electrode Design for High Speed Silicon Optical Modulator

by

Arifa Nazir Ahmed

Thesis for the degree of Doctor of Philosophy

August 2015

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Optoelectronics Research Centre

Thesis for the degree of Doctor of Philosophy

ELECTRODE DESIGN FOR HIGH SPEED SILICON OPTICAL MODULATOR

Arifa Nazir Ahmed

Due to their limited speed and high power dissipation copper wires can no longer meet the demands of future high speed computing devices. While many different approaches are being tried to overcome the challenge, the one based on a high-speed optical link looks promising. By using photons to transfer information one is able to eliminate the bottlenecks associated with electronic based interconnects. Where optical alternatives usually suffer from high costs and a cost effective approach that is also capable of high volume production is required. In this regard, silicon photonics offers a solution due to its CMOS compatibility.

Over the last decade remarkable progress has been made in the field of silicon photonics where photodetectors, optical sources (lasers) and modulators have been the focus of the study. The electro-optic modulator, which converts electrical signal into optical signal, is a fundamental building block of silicon photonics. Designers have previously concentrated more on optimizing the optical design of the modulator but the modulator's bandwidth can significantly improve if its electrode design is optimized. The aim of the project was to optimize the modulator electrode to maximize the bandwidth performance of the electrode.

Each element of the electrode has been studied separately. These include bends, tapers and two different dimensions of the coplanar line. Simulation results of square bend, mitred bend, round bend, exponential taper, Klopfenstein taper, triangular taper and two different dimensions of the coplanar line losses are presented. The fabrication process, analysis of aluminium surface morphology and etching techniques are discussed. As a result, characterization of different types of bends, tapers and electrodes are shown where discontinuities like bends and tapers reveal insignificant added loss between 0GHz and 67GHz. The final characterized electrode for a 0.5mm long modulator has a 3dB point above 67GHz whereas previous designs were limited to 42.8GHz.

Since velocity mismatch between optical and electrical signals also limits the modulator's performance, an effective technique to slow the electrical signal to match its velocity to that of the optical signal for slow wave modulators has successfully been demonstrated with the potential to achieve very high slowing down factors. The slow wave structure for electrode consisted of silicon dioxide and floating metal strips. The characterised slow wave modulator with slow wave electrode confirms a slowing down factor of 2. Not only will the slow wave structure slow down the electrical signal to reduce the mismatch with optical signal velocity, it will also reduce the substrate loss. This shows the potential of slow wave modulator bandwidth to double if optimized further.

Table of Contents

List of Tables

List of Figures

DECLARATION OF AUTHORSHIP

I, Arifa Nazir Ahmed, declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

ELECTRODE DESIGN FOR HIGH SPEED SILICON OPTICAL MODULATOR

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
7. Parts of this work have been published as:

    - G. T. Reed, Y. Hu, G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, J. Soler-Penades, M. Nedeljkovic, A. Khokar, P. Thomas, C. Littlejohns, **A. Ahmad**, S. Reynolds, R. Topley, C. Mitchell, S. Stankovic, D. J. Richardson, P. Petropoulos, P. Thomas, P. R. Wilson, L. Ke, T. M. Ben Masaud, A. Tarazona, and H. Chong, "Near infrared and the mid infrared silicon photonic devices," Nano Korea 2014 Symposium, Seoul, South Korea, 2-4 July 2014. (invited)

    - G. T. Reed, G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, Y. Hu, J. Soler-Penades, M. Nedeljkovic, A. Khokar, P. Thomas, C. Littlejohns, **A. Ahmad**, S. Reynolds, R. Topley, C. Mitchell, S. Stankovic, X. Chen, P. R. Wilson, L. Ke, T. M. Ben Masaud, A. Tarazona, and H. Chong, "Silicon Photonics," 7th International Silicon-Germanium Technology and Device Meeting, Singapore, 2-4 June 2014. (plenary)

- G. T. Reed, G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, Y. Hu, J. Soler-Penades, M. Nedeljkovic, A. Z. Khokhar, P. Thomas, C. Littlejohns, **A. Ahmed**, S. Reynolds, R. Topley, C. Mitchell, S. Stankovic, P. R. Wilson, L. Ke, T. M. Ben Masaud, A. Tarazona, H. M. H. Chong, "Silicon photonic devices for the near - and mid-infrared wavelength ranges," Mediterranean Photonics Conference 2014, Trani, Italy, 7-9 May 2014. (invited)

- G. T. Reed, G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, Y. Hu, J. Soler-Penades , M. Nedeljkovic, A. Khokhar, P. Thomas, C. Littlejohns, **A. Ahmad**, S. Reynolds, R. Topley, C. Mitchell, S. Stankovic, N. Owens , X. Chen, P. R. Wilson, L. Ke, T. Ben Masaud, A. Tarazona, H. M. H. Chong, "Recent results in Silicon Photonics at the University of Southampton," Photonics West 2014, San Francisco, USA, 1-6 February 2014. (invited)

- G.Z.Mashanovich, F.Y.Gardes, D.J.Thomson, Y.Hu, R.Loiacono, N.Owens, M.M.Milošević, M.Nedeljković, **A.N.Ahmed,** P.Thomas, R.Topley, G.T.Reed Silicon optical modulators for supercomputing and optical communications *Telekomunikacije* 2011 Vol.(7) (Invited)

Signed: .....

Date: .....

Acknowledgements

I would like to express my upmost gratitude to my supervisor Professor Graham T Reed, who provided invaluable guidance, encouragement, supervision, and support throughout this journey. I also would like thank my second supervisor, Goran Mashanovich.

I wish to express my gratitude to Dr David Thomson, who has abundantly provided me with the necessary assistance, support and guidance. I would like to also mention, Dr Frederic Gardes, who provided me with expert knowledge on silicon modulators as well as Dr Charles Free and Dr Tim Brown whom provided key guidance towards Microwave engineering techniques at University of Surrey. I would like to thank Dr Nathan Owens for providing me with key suggestions on fabrication techniques at University of Surrey.

I would like to also show my thanks to Antulio Tarazona for the fabrication of doped silicon using Hot-Wire CVD. I would also like show appreciation for Dr Stuart Pearce and my friend, Chirenjeevi, for their assistance during fabrication. I would like extend my graduate towards all the cleanroom technicians for all the training and support they provided.

I would like to thank my whole group, Stevan Stankovic, Ali Khokhar, Xia Chen, Colin Mitchell, Milos Nedeljkovic, Li Ke, Rob Topley, Callum Littlejohns, Milan Milosevic, Paul Thomas, Scott Reynolds, Jordi Soler Penades, Thalia Bucio Dominguez, Nathan Soper, Zhibo (Will) Qu and Lorenzo Mastronardi, who have helped me directly or indirectly.

I would like to thank all my family and friends who have always provided me with encouragement and support. A special thank you to my sister (Ayesha Nazir) and parents (Ch. Nazir Ahmed and Abida Nazir) for believing in me, love, encouragement, understanding and endless support. Hence why, I dedicate this thesis to my first and foremost beloved parents, without them all this would not have been possible.

Acronyms

ADS	Advance Design System
K Taper	Klopfenstein Taper
HF	Hydrofluoric Acid
PECVD	Plasma Enhanced Chemical Vapour Deposition
HW-CVD	Hot Wire Chemical Vapour Deposition
r.m.s	root mean square
RF	Radio frequency
IPA	Isopropyl Alcohol
DI water	De-Ionized water
IBE	Ion Beam Etching
SEM	Scanning Electron Microscope
RIE	Reactive Ion Etching
DRIE	Deep Reactive Ion Etching
IC	Integrated Circuit
CMOS	Complementary Metal-Oxide Semiconductor
SOI	Silicon On Insulator
LED	Light Emitted Diode
PDE	Plasma Dispersion Effect
MZI	Mach-Zehnder Interferometer
CPW	Coplanar Waveguide
MMIC	Monolithic Microwave Integrated Circuits
GSG	Ground-Signal-Ground
TRL	Thru-Reflect-Line

SOLT	Short-Open-Load-Thru
S-CPW	Shielded-Coplanar Waveguide
MS	Microstrip
CPWG	Coplanar waveguide Grounded
SPP	Series Push-Pull
RTA	Rapid Thermal Annealing

Symbols

α	attenuation
$\check{N}$	complex refractive index
n	normal refractive index
c	speed of light
κ	extinction coefficient
$\acute{\epsilon}_r$	complex dielectric constant
λ_0	free space wavelength
λ_g	guided wavelength
$\Delta\emptyset$	phase shift
Δ	change
G	conductance
L	inductance
R	resistance
C	capacitance
α_d	dielectric attenuation
$tan\delta_c$	loss tangent

ε_r	relative permittivity
δ	skin depth
μ	permeability
σ	conductivity
Z_o	characteristic impedance
γ	propagation constant
β	phase constant
Γ	reflection coefficient
f	frequency
v_p	phase velocity
Q	quality factor
ω	angular frequency
Z_L	load impedence
ρ	resistivity
α_c	attenuation constant
C_s	correction factor

Abbreviation

TPR	taper
STR	straight-line equivalent
MRD	mitred bend
SQR	square bend
RND	round bend
BND	bend

Note: where number in front of it represent the number of bends or tapers cascaded.

Chapter 1: INTRODUCTION

For data networks, the bandwidth demands have been increasing significantly in recent years. However, the conventional solution of copper wires merely meets the current needs of the market. Optical solutions are capable of delivering terabyte per second, whereas the copper is limited to few gigabyte per second. The next question, which arises, is “How to transfer electrical data in an optical format?” High-speed optical modulators are the solution. Conventional high-speed modulators exist in expensive III-V semiconductors [2] such as Gallium Arsenide (GaAs) or Indium Phosphide (InP) and ferroelectric materials such as Lithium Niobate (LiNbO3). LiNbO3 is interesting due to its electro-optic properties [1]. It exhibits a large refractive index change due to the linear electro-optic effect, which enables optical modulation via the Pockels effect. Later, silicon photonic devices were conceived in the late 1980’s [1][4]. The first all-silicon integrated optical components were demonstrated at the time [1] and their use has been rapidly increasing in recent years. Silicon benefits from low cost and performs optoelectronic functions. The majority of optical devices can be designed to be complementary metal-oxide-semiconductor (CMOS) technology compatible with high volume production potential. This potentially allows the monolithic integration of electronic and photonic devices, although in the short term it is likely that photonic and electronic chips will continue to be fabricated separately. Silicon optical modulators are one of the fundamental building blocks of future networks and for monolithic integration on a single chip. The motivation is their “potential” to enhance future microelectronics and communications networks.

1.1 Silicon Photonics

The microelectronics industry continues to grow with Moore’s Law, according to which the data transfer speed of a microprocessor doubles every 18 months [13]. The law is based on the observation that rapid miniaturization of device sizes doubles the number of transistors on a chip every 18 months [13]. While making the transistor smaller is a challenge, the requirement of a good interconnection between transistors now poses a bigger challenge to Moore’s Law. In recent times, there has been a decline in Moore’s law and doubts have already been raised if silicon based electronic integrated devices could deliver the functionality demanded by future devices [13].

The interconnection on a chip is simply electrical wiring made out of copper that provides ground, power, clock and signal to different circuits/systems on a chip. Reducing the transistor’s size increases the processing speed; however the same is not true for the interconnection. Smaller

interconnection lengths increase cross talk, the RC time constant and the power dissipation in interconnects [14]. Cross talk in ICs arise due to increased interconnect densities leading to higher coupling capacitances between neighbouring interconnects. On the other hand the resistance of interconnects (and therefore the RC time constant) increases with reducing the interconnect width since shorter gate lengths require the interconnect width to be small. Further, the increased switching frequencies and higher device densities on a chip result in large switching currents that lead to excessive power dissipation in the interconnects[14]. As a result the ratio of heat dissipated within interconnects to that in the transistors has risen considerably with the shrinkage of device dimensions.

Using light or photons removes most of the problems associated with metal interconnects that use electrons [14]. Optical signals are not affected by the RC time constant and in transparent media photons are able to propagate with less heat dissipation. Optics has therefore generated great interest and the vision of an optical superchip capable of carrying out light manipulation dates back to early 1990s [5]. Traditionally, photonic circuits have employed expensive materials like the ferroelectric Lithium Niobate (LiNbO3) and the III-V semiconductors Gallium Arsenide (GaAs) & Indium Phosphide (InP)[1]. They have therefore been primarily used for high-end applications, i.e. for long haul communications which make up the backbone of the communication infrastructure. Because copper wires have been providing the necessary bandwidth so far, there has been no immediate mass scale application for very short-range optical links. But as Moore's law approaches its end and the cost of optical interconnects goes down, it is predicted that optical links will gradually replace their electrical counterparts.

Over the last decade silicon photonics has emerged as the leading optical interconnect technology capable of providing the benefits of optics at low costs. The advantages of using silicon as the primary photonic material are noteworthy. It is a low cost, highly abundant and the most widely studied material. Silicon is transparent at telecommunication wavelengths (1.3-1.5 μm) and has a very high refractive index contrast with conventional dielectrics (silica/air) allowing it to transmit light with negligible losses [15]. Above all, it has a large established manufacturing infrastructure which means that photonic devices made of silicon can be produced in the same facilities used for fabricating CMOS (complementary metal oxide semiconductor) devices. However, silicon has not been famous for its optical properties as much as for its electronic properties. But this is now proving to be more of an engineering problem and it appears that silicon is a viable electronic & photonic material.

The fundamental building blocks of an integrated silicon photonic chip are: a laser source to generate light, an optical waveguide to confine and thus guide light on a chip, an optical

modulator to convert electrical data into an optical signal, a photodetector to convert light back into electrical data and electronic components for driving the modulator and for amplifying incoming signals from the photo-detector. From a technological point of view, there are challenges to the development of an integrated silicon photonics chip, two examples being the silicon based modulator and laser. This is because silicon is a poor light emitting material owing to its indirect band gap and because traditional modulation methods used in semiconductor materials are weak in silicon at telecommunication wavelengths. Nevertheless, in recent times significant progress has been made in the development of these components.

1.2 A brief history of silicon photonics

Work on silicon photonics began in the late 1980's, when researchers started to apply design principles of the microelectronics industry to photonic circuits. Of significance was the work of Reed from the University of Surrey [6] and of R. Soref at Rome Air Development Center [7]. Soref's group found numerical expressions for the change in the refractive index and absorption coefficient of Si with change in carrier concentration at telecommunication wavelengths. This enabled modelling of devices for light modulation in silicon. The work of Graham Reed on the other hand was of great commercial significance to silicon photonics. Reed demonstrated light confinement with very low absorption losses in CMOS compatible silicon-on-insulator (SOI) rib waveguides that could manipulate light. This led to the development of large waveguides (greater than 10 μm^2 in cross section) that could be used in fibre optic networks. The primary application of silicon photonics was therefore telecommunications. However, interest in silicon photonics grew and it was realized that silicon photonics could well have a role beyond telecommunications.

In the 1990's Bookham Technology became the first company to manufacture photonic devices from low cost processing techniques used in the microelectronics industry founded by Dr Rickman which adapted the research activities of Reed's group. But the modulation speeds of these circuits were very low and despite continuous research silicon photonic devices could not demonstrate modulation speeds greater than 20 MHz. In 2004, Intel Corp. reported a silicon based CMOS compatible optical modulator with modulation speeds in excess of 1GHz [8]. This breakthrough demonstrated the potential of a silicon based optoelectronic integrated circuit that would combine electronic intelligence and photonic functionality. In recent times, the field has expanded: laser technology has been integrated with a silicon based optical chip [9], modulation speeds as high as 70 Gb/s have been reported [10] and waveguide dimensions have reduced to the nanometre range. A vibrant community of companies and academics is emerging with a vision to enable silicon photonics to provide the functionality for future integrated circuits.

1.3 Aims and objectives

The literature on silicon modulators suggests that not much attention has been given to the electrode design, which could potentially provide significant improvement in modulator performance [11]. Recently, for enhanced performance of a silicon modulator, the slow wave structure has been exploited [12]. Unfortunately, the performance of the slow wave modulator was also held back due to a mismatch between the velocities of the electrical and optical signals. This problem can be resolved by improving the electrode design and by reducing the mismatch between electrical and optical signals. Hence, the aim of this research is to improve the overall performance of the optical modulator by improving the design of the electrode carrying the electrical signal. To do so, different components, which form the electrode, will be analysed, designed and measured separately. A complete electrode design will then be presented to give a better response in comparison to [12]. The research will also extend to improving the velocity mismatch between electrical and optical signals to improve slow wave modulator performance. This will be achieved by slowing down the electrical signal which will in turn reduce the mismatch.

1.4 Outline of thesis

This prelude has introduced the field of silicon photonics, it has given a brief historical view and discussed the importance of silicon photonics and finally the aim and objectives of this research has been outlined.

Chapter 2 provides the setting for silicon modulators. It introduces the design and operation of the silicon modulator, leading to a discussion on current silicon modulators and the operation of slow wave modulators. This provides the motivation for this research work.

Chapter 3 will introduce the microwave engineering concepts which are applicable to the electrode design. The design consideration for electrode designs for silicon modulators will also be considered, and any relevant work related to electrode design will be discussed.

Chapter 4 describes the design of the electrodes. This chapter will go through the design work and will present the simulation results on the tapers, bends, and different dimensions of electrode. The design and simulation results for the slow wave electrode will also be presented.

Chapter 5 is a chapter on fabrication. Firstly, the fabrication process used will be discussed. It will also explore fabrication methods used and any constraints in the fabrication from deposition to characterisation will be analysed.

Chapter 6 is concerned with measurement, and comparison of the experimental results with simulation results. This chapter will go through the electrical measurements conducted and also optical measurements.

Chapter 7 concludes the thesis, and will summarise and draw conclusions from the work. It will provide the overall contributions. This chapter will also suggest the future work.

References

[1]Luennemann et al. 'Electrooptic properties of lithium niobate crystals for extremely high external electric fields', Appl. Phys. B 76, 2003, pp. 403–406

[2]Tarucha et al. 'Waveguide-Type Optical Modulator of GaAs Quantum Well Double Heterostructures Using Electric Field Effect on Exciton Absorption', J. Appl. Phys., 1985, pp. 442-444

[3]R.A. Soref and J. P. Lorenzo, 'Single-crystal silicon – a new material for 1.3 and 1.6 μm integrated-optical components' , Electronic letters, 21,1985, pp. 853-954

[4]R.A. Soref and J.P. Lorenzo, 'All-silicon active and passive guided-wave components for λ= 1.3 and 1.6 μm' , IEEE J. Quantantum Electron., vol.QE-22,1986, pp. 873-879

[5] R. A. Soref, "Silicon-based optoelectronics," Proc. IEEE, vol. 81, 1993, pp. 1687-706

[6] Tang, C.K., Kewell, A.K., Reed, G.T., Rickman, A.G., and Namavar, F.,"Development of a library of low-los silicon-on-insulator optoelectronic devices", IEE Proc. Optoelectron.,1996, pp.312–315

[7] Soref, R.A., and Bennett, B.R., "Electrooptical effects in silicon," IEEE J. Quant. Electron., QE-23, 1987, pp.123–129

[8] Liu, A., Jones, R., Liao, L., Samara-Rubio, D., Rubin, D., Cohen, O., Nicolaescu, R., and Paniccia, M., "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," Nature, 2004, pp.615–618

[9] Fang, A.W., Park, H., Cohen, O., Jones, R., Paniccia, M.J., and Bowers, J.E., "Electrically pumped hybrid AlGaInAs-silicon evanescent laser," Optical Express, 2006, pp. 9203–9210

[10] Hao Xu, Xianyao Li, Xi Xiao, Peiji Zhou, Zhiyong Li, Jinzhong Yu, and Yude Yu, "High-speed silicon modulator with band equalization", Optics Letters, Vol. 39, No. 16, August 15, 2014, pp.4839-4842

[11]H Yu and W Bogaerts, 'An Equivalent Circuit Model of the Traveling Wave Electrode for Carrier-Depletion-Based Silicon Optical Modulators', Journal of Lightwave technology, vol. 30, no. 11, June 1, 2012 pp. 1602-1609

[12] A. Brimont, D. J. Thomson, P. Sanchis, J. Herrera, F. Y.Gardes, J. M. Fedeli, G. T. Reed, and J. Martí, 'High speed silicon electro-optical modulators enhanced via slow light propagation', Optics Express, Vol. 19, Issue 21, 2011, pp. 20876-20885

[13] L.G. Roberts, "Beyond Moore's law: Internet growth trends", IEEE Computer, Vol 33. Jan 2000, pp.117-119

[14] J A Davis and J D. Meindl, 'Interconnect technology and design for gigascale integration', Springer, 1st edition, Kluwer Academic Publisher, 2003, pp.384

[15] F Grades, G Mashanovich and G Reed, 'Evolution of optical modulation in silicon-on-insulator devices', SPIE Newsroom, Dec 2007

Chapter 2: FUNDAMENTALS OF SILICON MODULATOR

Electro-optic modulators require the application of an electrical signal to the modulating device that results in either direct modulation or material modulation. In direct modulation, the electrical signal is superimposed on to the injected current of the optical signal such as in a laser diode or a light emitting diode (LED) [1]. This modulation is straightforward but it results in frequency chirping due to a carrier induced wavelength variation and this leads pulse broadening and as a result performance degradation [2]. Using material modulation, also known as external modulation, can reduce such effects significantly. There are two types of external modulation: absorptive and refractive modulation. Absorptive modulation also known as electro-absorption modulation is realised by changing the absorption coefficient of the material. On the other hand, refractive modulation also known as electro-refraction modulation can be achieved by changing the refractive index of the material. The electric field effects that lead to electro-absorption or electro-refraction are the linear electro-optic (Pockels) effect and the Franz-Keldysh effect. However, the Pockels effect is not found in silicon and Franz-Keldysh effect is found to be weak [3] [4], making these effects ineffective for silicon [5]. The main two effects used in silicon are the thermo-optic effect and plasma dispersion effect (PDE). When temperature of the material is varied, its refractive index can vary. If it varies with temperature then the material is said to exhibit the thermo-optic effect. This effect is found in silicon but is slow [6] whereas, the plasma dispersion effect has proven to be the one of the best option for modulation in silicon [7]. Recently new approaches are emerging where different materials are added to the silicon and have proved to be successful, for example: SiGe alloy[8], graphene[9], organic polymer[10] and III-V on Si[11].

2.1 Concepts for Silicon Modulator

This section will firstly discuss the important parameters for modulation in silicon such as refractive index and how it is varied to achieve the modulation. The free carrier absorption from silicon modulator's perspective will also be discussed.

2.1.1 Refractive Index

The complex refractive index (ň) is defined as ň=n+ ĵκ. The real part of the refractive index (ň) is the normal refractive index (n). The normal refractive index of a material is defined as a ratio of the speed of light (c) to the velocity (v) of light propagating in the medium. Whereas the imaginary part (κ) is known as the extinction coefficient and it is determined by the absorption

coefficient (α) of the material. The relation between the absorption coefficient and extinction coefficient is $\alpha=4\kappa\pi/\lambda_0$, where λ_0 represents the free space wavelength of light. This relation also shows that the absorption coefficient and the extinction coefficient are directly proportional [12].

Using Maxwell's equations [12], the relationship between the refractive index and the dielectric constant can be deduced to be $n= (\varepsilon_r)^{1/2}$. If the refractive index is a complex quantity then the dielectric constant will also be complex. Hence, the complex dielectric constant ($\acute{\varepsilon}_r$) is equal to $\varepsilon_1+\hat{\jmath}\varepsilon_2$. It also means $\check{n}^2$ and $\acute{\varepsilon}_r$ are equal. Now, if the complex refractive index is squared and then compared with the complex dielectric constant the relation becomes: $\varepsilon_1= n^2 - \kappa^2$ and $\varepsilon_2= -2\pi\kappa$. The relationship between refractive index and dielectric constant shows that they are not independent quantities.

2.1.2 Refractive Index Change and Attenuation Change for Silicon

The mathematical relations established from the Drude-Lorentz model were first refined experimentally for silicon by Soref and Bennet [13]. In particular, they focused on the communication wavelengths of 1.3 µm and 1.55 µm. In the case of electrons their results were in good agreement with the classical Drude-Lorentz model while for holes the dependence was $\Delta N^{0.8}$, rather than a linear relationship. Their expressions have been reproduced here and have been widely used to evaluate changes due to concentration changes of carriers in silicon.

At λ_0 = 1.55 µm,

$$\Delta n = \Delta n_e + \Delta n_h = -[8.8x10^{-22}\Delta N_e + 8.5x10^{-18}(\Delta N_h)^{0.8}] \quad \text{Equation 2.1}$$

$$\Delta \alpha = \Delta \alpha_e + \Delta \alpha_h = 8.5x10^{-18}\Delta N_e + 6.0x10^{-18}\Delta N_h \quad \text{Equation 2.2}$$

Where Δn_e =change in refractive index due to free electrons, Δn_h = change in refractive index due to free holes, $\Delta\alpha_e$ = change in absorption due to free electrons, $\Delta\alpha_h$ = change in absorption due to free holes, ΔN_e = free electron concentrations, and ΔN_h = free hole concentrations.

From the modulator's perspective, it is important to achieve a high phase shift while keeping the absorption losses to a minimum. The phase shift can be achieved by changing the refractive index. In silicon, this is achieved via the plasma dispersion effect where free carriers modulate the refractive index but it introduces absorption loss. Equations 2.1 and 2.2 are used to design the silicon modulator. It is clear that a change in concentration of holes would result in a higher

change in the refractive index. Also, the loss due to the holes is lower, hence making the waveguide predominantly P type is preferred over N type.

2.2 Design of Silicon Modulator

This section will discuss how electrical manipulation of the free carrier concentration is carried out to change the refractive index and to achieve a phase shift. It also describes how this phase shift is then translated into intensity modulation. The important figures of merit will be discussed. The enhancement of silicon modulator performance via slow wave structures will also be explored and some results from the previous work will be analysed leading to the importance of this work being shown.

2.2.1 Electrical manipulation and phase modulation

Electrical manipulation of free carriers can be done in three ways in plasma dispersion silicon modulators; carrier accumulation, injection and depletion [16]. Carrier accumulation is realized in the form of a capacitance structure where a thin insulating layer, typically SiO_2 separates the waveguide into two regions. When the device is a forward biased, electron and holes accumulate at the interface, on either side of the insulating layer resulting in a change in carrier concentration and therefore a change in refractive index and ultimately a change in phase shift. However the oxide complicates device fabrication [16]. This limitation can be subdued with an injection design where the thin insulating layer is not present and forward biasing the device results in carrier injection and therefore change in carrier concentration within the waveguide region. The injection mode device performance has high modulation efficiency [17] but is limited by minority carrier lifetime [18]. Carriers injected under forward bias recombine with minority carriers during their flow. This limits the switching speed of the modulator, as some excess carriers are lost.

Carrier lifetime effects can be avoided if the modulator is operated in depletion mode. The depletion mode modulator has high-speed performance [19] and is the subject of this thesis. In this case, doped p and n regions are used to form a pn diode in or in close proximity to the waveguide. The device is reverse biased and that allows the depletion width of the PN junction to increase. As the depletion region is devoid of free carriers an increase in the depletion width leads to a change in carrier concentration and thus a change in refractive index. The change in refractive index is greater for a change in hole density as opposed to electron density according to Soref and Bennet [13] and therefore provides better phase modulation efficiency [20]. For such reasons, the depletion region in these devices is usually extended in the p-type region. This is achieved by doping the p and n regions asymmetrically [21].

The phase shift can be approximated from the change in refractive index by [17],

$$\Delta\emptyset \approx \frac{2\pi\Delta nL}{\lambda}$$

Equation 2.3

The equation can be rearranged to predict the active length (L) required to give the phase shift of π, where Δn is the change in refractive index [19].

$$L_\pi = \frac{\lambda}{2\Delta n}$$

Equation 2.4

In the case of depletion mode modulators, with increasing reverse bias the depletion width increases and the resulting phase shift would increase. However, the phase shift cannot increase indefinitely. As the DC voltage increases, the depletion region can increase significantly but the depletion width does not increase linearly with voltage. In other words, the change in depletion width is smaller from -1 to -2V than it is from 0 to -1V. Also, an increased depletion width will in turn reduce the interaction of the optical wave with free carriers. This means that the refractive index cannot be varied any more and more phase shift will not be possible (i.e. it saturates). Thus, it is critical to optimize the doping profile to maximize the interaction of the optical wave with free carrier density change, otherwise the optimal phase shift will not be achieved [22].

2.2.2 Intensity modulation

To convert phase shift into intensity modulation either an interferometric or resonant structure can be used. The most commonly used are Mach-Zehnder Interferometer (MZI) and the ring resonator.

In a ring resonator, a change in the refractive index will induce a change in the resonance condition at the operating wavelength. The device has the advantage of being small but is limited in optical bandwidth as it operates on a specific resonant wavelength [16]. Furthermore, it is also sensitive to fabrication conditions and temperature, therefore affecting the device performance. This temperature sensitivity is due to the thermo-optic effect in silicon, which will change the refractive index of the medium in the opposite sense to the change induced by free carriers [19].

The Mach-Zehnder Interferometer (MZI) converts phase shift into intensity modulation. In figure 2.1, a MZI has been shown where light is split into two arms of the waveguide using a Y-junction [23]. Light on both arms can be modulated with respect to each other by changing the refractive index on one arm. Another option is to modulate both arms by using a push-pull configuration [24]. The light is then combined again using a Y-junction at the output end. The resulting electric field of the light wave is the sum of the amplitude of the two electric fields of the two optical waves passing through the arms of the MZI (i.e. interference). The MZI thus translates phase modulation into intensity modulation, with the output being maximised for two in-phase waves, and minimised for waves in anti-phase. The device is broadband unlike the ring resonator [25] however, it is much longer since a significant interaction of the optical wave and the active region of the device is required. For ring resonator modulator, the resonant spectral width is small so requires less phase shift to drive the modulator out of phase and in phase.

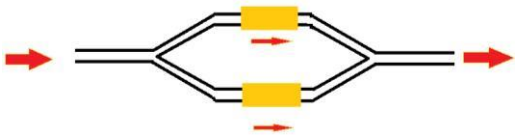


Figure 2-1– Diagram of an MZI structure with modulators on both arms

In this work, a MZI that uses the depletion mode modulator configuration is employed. An electrical signal/microwave signal travelling on a coplanar line is applied to only one arm of the MZI. The electrical signal is offset to below zero via a negative DC bias (figure 2.2) to ensure that the voltage remains negative (reverse biased device) in order to allow only carrier depletion to take place. The negative bias just offsets the electrical signal sufficiently to ensure that the maximum voltage (digital 1) has a zero volt level.

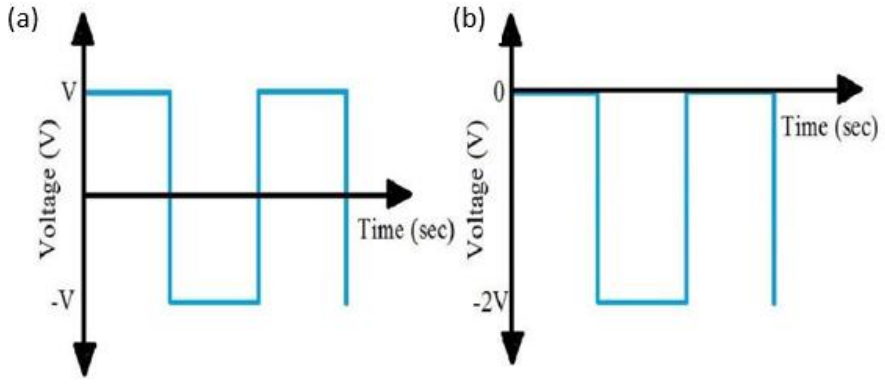


Figure 2-2– (a) electrical signal without DC bias (b) electrical signal with negative DC bias

As noted earlier, the phase of the optical signal changes in proportion to the bias. When the electrical signal is a digital 0, the bias is greater (more negative). This results in an increase in the depletion width and consequently a larger phase shift. In the case when this phase shift is π the phase of the optical signal in one arm of the MZI is shifted by π with respect to the signal in other arm. Consequently, the two signals would add destructively and the output optical intensity would be a minimum. When the electrical signal is a digital 1 the bias is lower (less negative / zero) and both arms of the MZI would not experience any phase shift since the bias applied on both the arms is zero. The two signals thus add constructively and the optical intensity is a maximum. It is important that both the optical and electrical signals co-propagate [25] with the same speed or this introduces bandwidth limitations. The ratio of maximum to minimum intensity is expressed in the form of an extinction ratio which should ideally be kept high [16].

$$Extinction\,ratio = 10log\left(\frac{I_{max}}{I_{min}}\right)$$

Equation 2.5

The above situation however requires a phase shift of π in the modulating arm of the MZI to achieve ON and OFF states of the intensity modulator with a maximum extinction ratio. Such a large phase shift would require a sufficiently long device length [7], which in turn would result in significant attenuation of the electrical signal. A reasonable device length would allow a phase shift of π/2. However, this small phase shift would not result in destructive interference of the optical signals in the two arms of the MZI. This then compromises the extinction ratio and a clear distinction between maximum and minimum intensities may become difficult at the receiving end. However, this demonstrates the flexibility available to the device designer, as he can trade-off device length (hence, the loss) with extinction ratio and drive power.

With the high speed modulator providing π/2 phase shift a significant improvement on extinction ratio without compromising the device length can be achieved by adding a low speed modulator in the modulating arm of the MZI to allow tuning of the bias point. The low speed modulator provides an additional phase shift of, for example, π/4 (biasing at the quadrature [26]). When the high-speed modulator is also operated the total phase difference between the two arms would be 3π/4. This would provide with a minimum output power but the two waves in the different arms of the MZI would still not add completely for perfect destructive interference even in this case. Further, when the electrical signal is a digital 1 (0V bias), the low speed modulator would result in a π/4 phase shift. In this case, the output power would be a maximum since there is smaller shift in one arm with respect to the other. In this case a small degree of loss would be caused since the two waves would not completely constructively interfere. The extinction ratio in this case is however, high mainly due to the property of the sinusoidal wave. In figure 2.3, the output

intensity is plotted versus phase shift. At a phase shift of π/4 the output power is lower as compared to 0, however the intensity does not drop significantly due to the nature of the sinusoidal wave [26]. Going from a phase shift of π/4 to 3π/4 (shown as red points in figure 2.3) one observes a rather large change in output power. That is to say, the major change in output intensity happens in the region π/4 to 3π/4. We therefore choose this region as the operating region to provide with a larger extinction ratio while keeping the device length reasonably short. If π was to be used as operating point imagine going from π/2 to 3π/2 (illustrated as yellow point in figure 2.3) then this end up at same power state therefore quadrature operating point is used for a π phase shift.

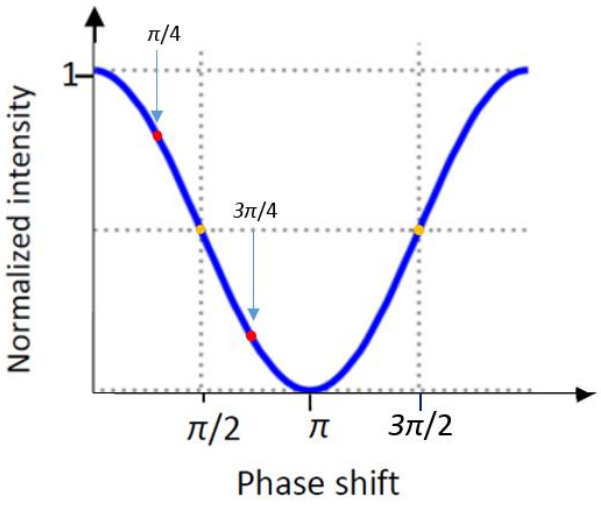


Figure 2-3– Normalized intensity versus phase shift [26]

2.2.3 Slow wave modulation

The use of a slow wave structure is a method used to enhance the performance of silicon modulators based on the plasma dispersion effect (figure 2.4(a)). The slow wave structure principally increases the interaction between the matter and the field which results in shorter devices and/or lower power consumption [27]. Slow wave structures are formed of periodic nano-structures. The periodic structure used in this case is the 1D laterally corrugated periodic structure (LCWG) as shown in figure 2.4(b)[27]. The PN junction is incorporated in the slow light structure, the light is slowed using the one dimensional periodic structure and phase is modulated via PN carrier depletion method [27]. The design of the corrugated waveguide is shown in figure 2.4(b), where width We is equal to 650nm and W is 300nm where the period a= 310nm with the heights H=220nm and h=100nm [27]. The periodic structure is designed to operate at certain wavelength and allows the propagation of the light. When coherent light reaches the grating in

the periodic structure, backscattering will takes place and interference will occur between the incident light and backscattered light. When the incident light and the backscattered light is in phase then a standing wave is generated and has zero group velocity of slow mode [30]. In the case of the incident light and the backscattered light being out of phase then internal reflection occurs and behaves like normal waveguide with regular group velocity [28] but when they are slightly out of phase then slow light will be generated therefore only in certain region where slow light will occur [30]. The slow light is greatly impacted by the roughness of the sidewalls of the waveguide due to the increase interaction between the sidewalls and slow light. Therefore high accuracy in fabrication is required [28].

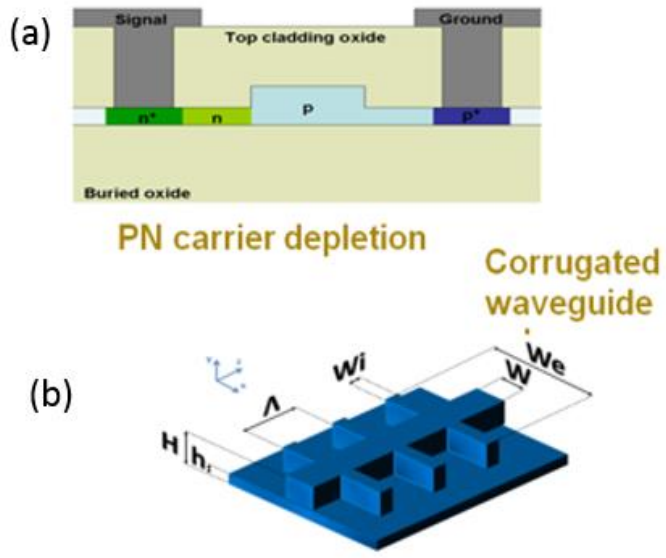


Figure 2-4–(a) shows the PN junction used in slow wave structure (b) shows the 1D laterally corrugated periodic structure (LCWG) used as slow wave structure (reproduced from [27])

An asymmetric MZI (Mach-Zehnder Interferometer) is used to convert the phase shift into intensity modulation in which an MMI (Multi-Mode Interference) structure is used to spilt and combine the light at input and output respectively [27] (refer to figure 2.5). Figure 2.5(b) shows the 3D image of slow wave structure integrated with conventional modulator to get the enhanced performance.

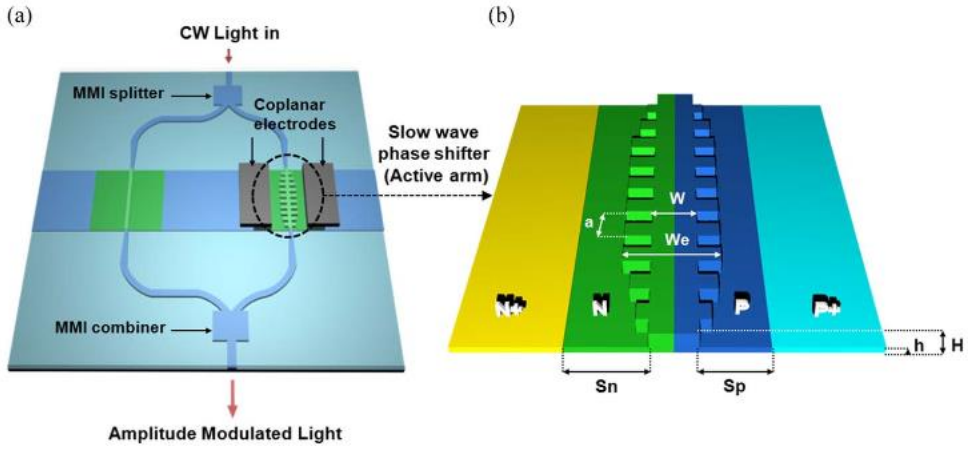


Figure 2-5–(a) shows the schematic of the modulator and (b) shows the closer look of the slow wave modulator with PN junction (reproduced from [29]).

The graph in figure 2.6 shows phase shift vs the reverse bias voltage for different effective index. It can be observed that as the effective index (n) increases, the wave is slowed down and the required drive bias (reverse voltage) required to achieve the same phase shift is lowered. This denotes the merit of figure will be improved significantly by using the slow wave structure.

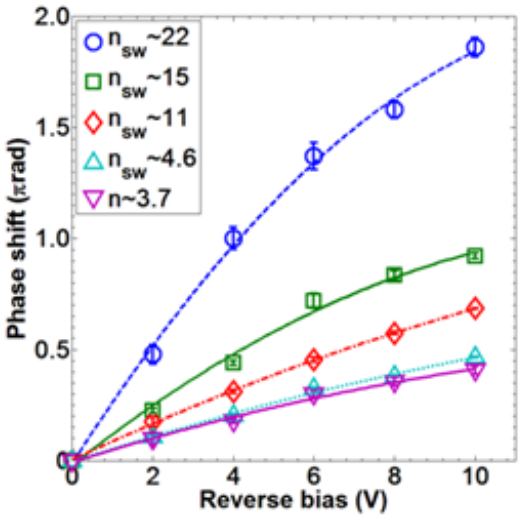


Figure 2-6– Graph shows phase shift vs reverse bias voltage for different effective refractive index (reproduced from [27)

The enhancement in modulation efficiency can be achieved either by lowering of the drive voltage while keeping the same length or decreasing device length while keeping the same drive voltage. In this case, the drive voltage was kept the same while the length of the device was decreased.

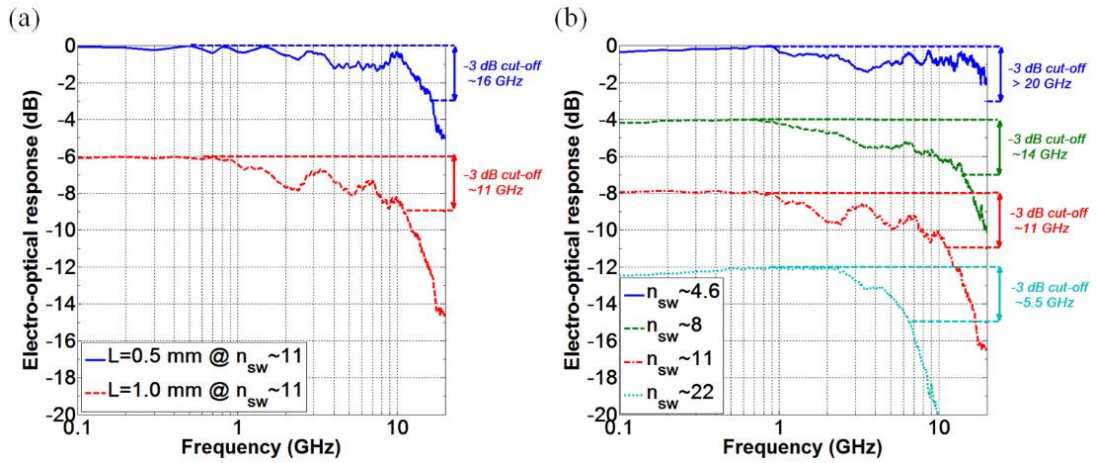


Figure 2-7–(a) shows the electro-optical response versus frequency for 2 different lengths when group index is ~11 (b) electro-optical response versus frequency for different group indices (reproduced from [27]).

Figure 2.7(a) shows the electro-optic response of slow wave modulator with two different modulator lengths (0.5mm and 1mm) where the group index is equal to ~11 and the drive voltage are equal for both cases. The 3dB roll-off the short length (0.5mm) is at 16GHz whereas for the longer length (1mm), the 3dB roll-off is at 11GHz. This shows that a longer modulator will see more limitation on the bandwidth due to the same velocity mismatch.

However, as the effective index is increased, the electro-optic performance degrades as evident from figure 2.7b. As the refractive index is increased, the optical signal is slowed down further, whereas, the electrical signal propagates with unaltered velocity causing the mismatch. Thus the degree of improved performance of the slow wave is mainly limited by the mismatch between the optical and electrical signals. Part of this project will concentrate on reducing the mismatch and improving the overall performance of slow wave modulators. The overall performance can be improved further if the attenuation loss is lowered while maintaining the characteristic impedance of electrodes to keep reflection loss minimal. To achieve this, each component of electrode will be analysed separately. This leads to the next chapter which discusses the electrode and the applicable literature.

References

[1]G Ghione, 'Semiconductor devices for high-speed optoelectronics', Cambridge University Press, 2009, pp.255

[2]R Ramaswami, K N. Sivarajan, G H Sasaki, 'Optical Networks: A Practical Perspective, Morgan Kaufmann, 2009, pp. 192 -193

[3]R.A. Soref and J.P. Lorenzo, 'All-silicon active and passive guided-wave components for λ= 1.3 and 1.6 μm', IEEE J. Quantantum Electron., vol.QE-22, 1986, pp. 873-879

[4]A. Soref and B. R. Bennett, "Electro-optical effects in Silicon," IEEE J.Quantum Electron, QE-23,1987, pp.123-129

[5]G T Reed, 'Silicon photonics: The state of the art', John Wiley & Sons Ltd 2008, pp.98-100

[6] G. Cocorullo, and I. Rendina, 'Thermo-optical modulation at 1.5 μm in silicon etalon' Electron. Lett. 28, 1992, pp.83–85

[7] F. Y. Gardes, G. T. Reed, N. G. Emerson, & C. E. Png, "A sub-micron depletion-type photonic modulator in silicon on insulator" Optics Express 13, 2005, pp.8845–8854

[8]D. Feng, S. Liao, H. Liang, J. Fong, B. Bijlani, R. Shafiiha, B. J. Luff, Y. Luo, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "High speed GeSi electro-absorption modulator at 1550 nm wavelength on SOI waveguide," Optics Express, vol. 20, no. 20,2012, pp. 22224

[9]L. Yang, T. Hu, R. Hao, C. Qiu, C. Xu, H. Yu, and Y. Xu, "Low-chirp high-extinction-ratio modulator based on graphene – silicon waveguide," vol. 38, no. 14, 2013, pp. 2512–2515

[10]M. Lauermann, S. Wolf, P. C. Schindler, R. Palmer, S. Koeber, D. Korn, L. Alloatti, T. Wahlbrink, J. Bolten, M. Waldow, M. Koenigsmann, M. Kohler, D. Malsam, D. L. Elder, P. V Johnston, N. Phillips-sylvain, P. A. Sullivan, L. R. Dalton, S. Member, and J. Leuthold, "40 GBd 16QAM Signaling at 160Gb/s in a Silicon-Organic Hybrid Modulator," vol. 33, no. 6, 2015, pp. 1210–1216

[11]Y. Tang, J. D. Peters, and J. E. Bowers, "Over 67 GHz bandwidth hybrid silicon electroabsorption modulator with asymmetric segmented electrode for 13 μm transmission," Optics Express, vol. 20, no. 10, 2012, pp. 11529

[12]M Fox, 'Optical Properties of Solids', Oxford University Press, 2001, pp.3 -7

[13]R.A. Soref and B.R. Bennett, "Kramers-Kronig analysis of E-O switching in silicon," SPIE Integr. Opt. Circuit Eng., vol. 704, 1987, pp. 32–37

[15]R G. Hunsperger, 'Integrated Optics: Theory & Technology', Springer, Sixth edition 2009, pp. 113

[16]G. T. Reed, G. Mashanovich, F. Y. Gardes and D. J. Thomson, 'Silicon optical modulators', Nature Photonics vol.4, August 2010, pp. 518-526

[17]Xu, Q. et al. 'Micrometre-scale silicon electro-optic modulator,' Nature, 2005, pp. 325-327

[18]Gan, F. et al. , ' High-speed silicon electro-optic modulator design' , IEEE Photon Techn lett 17, 2005, pp. 1007-1009

[19]Liao, L. et al. 40 Gbit/s silicon optical modulator for high-speed applications. Electron. Lett. 43, 2007, pp.1196–1197

[20]Liu, A. et al. High-speed optical modulation based on carrier depletion in a silicon waveguide. Optics Express 15,2007, pp. 660–668

[21]D Thomson, 'Design of his modulator', University of Surrey, 2010

[22]A Liu et al., 'Recent development in a high-speed silicon optical modulator based on reverse-biased pn diode in a silicon waveguide', Semicond. Sci. Technol. 23 2008, pp. 1-7

[23]G T Reed, 'Silicon photonics: The state of the art', John Wiley & Sons Ltd 2008, pp.245

[24]C. K. Tang, G. T. Reed, 'Highly efficient optical phase modulator in SOI waveguides', Electron Lett. 31, 1995, pp.451-452

[25]Xu, Q. et al. 'Micrometre-scale silicon electro-optic modulator,' Nature 435, 2005, pp. 325-327

[26]G T Reed, A P Knights, 'Silicon Photonics: An Introduction' Chichester John Wiley & Sons, Ltd., 2004, pp.167

[27]Brimont, A, Thomson, DJ, Sanchis, P, Herrera, J, Gardes, FY, Fedeli, JM, Reed, GT and Martí, J High speed silicon electro-optical modulators enhanced via slow light propagation Optics Express,2011, pp.20876 – 20885

[28]A. María, G. Campo, S. Pablo, and S. Kilders, "Development of Integrated Silicon Photonics Modulation Devices for Digital and Analog Applications," Universitat politecnica Valencia,Thesis, 2013, pp.49-50

[29]Brimont et al. 'Slow-light-enhanced silicon optical modulators under low-drive-voltage operation', IEEE photonics, vol 4, no. 5, 0ct 2012, pp. 1306-1315

[30] T F Krauss, “Slow light in photonic crystal waveguides”, J. Phys. D: Appl. Phys. 40, 2007 pp.2666–2670

Chapter 3: ELECTRODES FOR MODULATORS

This chapter will discuss the coplanar waveguide which is used as an electrode for the modulator and its advantages over the microstrip line. It will also discuss the losses associated with the coplanar line followed by the characterization method adapted at higher frequencies. A review of the literature on dominant losses in coplanar lines, discontinuities and slow wave electrodes will also be presented.

3.1 Introduction

To decrease the RC limitation on the optical modulator's bandwidth, due to the added capacitance of the electrode [1], the travelling wave electrode in the form of transmission line is used where the electrode capacitance is distributed [1]. The transmission line for the electrical signal is also one of the most fundamental passive components at high frequencies [2]. For better performance of a silicon modulator operating at millimetre wavelengths, the electrical design can no longer be sidelined [1]. The electrical signal should co-propagate with the optical signal. The two signals should have minimal velocity mismatch while keeping the transmission loss of the electrical line to a minimum.

The transmission line chosen for the design is a coplanar waveguide with a finite ground plane due to its advantages over the microstrip line. A microstrip line is formed when a ground plane is applied on one side of the substrate and the signal conductors on the other side. Thus the majority of electrical field lines travel in the substrate. The coplanar line was first introduced by C.P. Wen [3] in 1969. At that time, it did not gain much popularity despite of its attractive properties, because the microstrip was the preferred transmission line since it was well established. However as time progressed and the demands for high frequency increased, the focus shifted to the coplanar line. This was mainly due to very high losses in the substrate associated with the microstrip line at microwave frequencies. Since the ground plane lies on the opposite side of the substrate to the signal electrode, most of the field penetrates completely into substrate giving a much higher loss compared with the coplanar waveguide. In a coplanar waveguide both the ground plane and signal electrode are fabricated on the same side of the substrate and are separated by a gap. Thus the fields are concentrated in the gap (between signal and ground plane) and therefore the field does not completely penetrate into the substrate making the substrate type (and hence substrate loss) less important [4]. Also, Stegens *et al*. [5] suggested that the characteristic impedance and phase velocity are more dependent on dimensions of CPW (Coplanar Waveguide) rather than thickness of the substrate. The other

advantage of using a CPW is that it is CMOS compatible and it simplifies the fabrication process as the ground and signal electrodes lie in the same plane which makes it easier to mount components. This in turn also reduces the fabrication cost and allows the possibility of on-wafer measurements [6]. The CPW also gives greater flexibility to achieve a given characteristic impedance by using different combinations of gap and signal dimensions due to reduced dependency on the substrate.

To better understand the losses associated with the transmission line at high frequencies, it is shown as a lumped-element circuit model, presented in figure 3.1. By understanding the equivalent circuit of a transmission line, this will also lead to an understanding of the impedance of the transmission line (in most cases characteristic impedance) and propagation constant of the line as will be discussed later in this section.

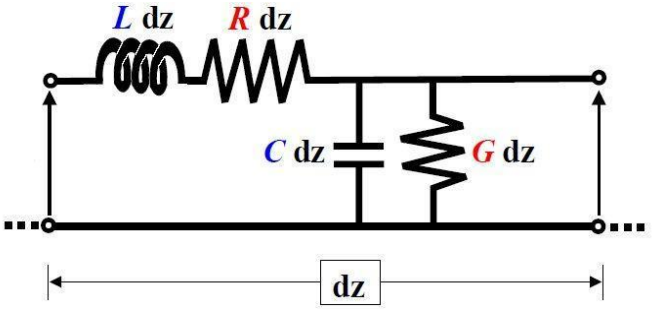


Figure 3-1– Equivalent circuit of high frequency transmission line

The series resistance (R) per unit length (Ω/m) will take into account conductor losses, radiation losses and geometry of the conductor (length and width). The wider the width of the conductor, the lower the resistance and as the length increases, the loss increases. As frequency increases, more current will travel on the outer most surface of the conductor, an effect known as the skin effect [42]. It also means that the current density will increase thus converting more energy into heat, which translates into more loss at higher frequencies.

The series inductance (L) per unit length (H/m) will be affected by the geometry and the inductance increases with the length of the conductor. A decrease in the inductance is achieved with a larger cross section. Current travelling at different depths in the conductor will also have slightly different phase delays where the net effect will be inductive. The shunt capacitance (C) per unit length (F/m) is mainly dependent on the permittivity of the substrate and the geometry of the conductor. As the width of the signal line increases, it will also increase the capacitance (C) per unit length since the area between the signal line and the substrate increases. The shunt conductance (G) per unit length (S/m) will be affected mainly by the conductance of the dielectric and loss tangent. The loss tangent reflects the absorption of electromagnetic energy in the dielectric material [41] hence the higher the loss tangent, the higher the dielectric loss. The

dielectric properties are usually defined in terms of real permittivity and loss tangent at certain frequency [37] where the loss tangent defines how lossy the dielectric is. The loss tangent is the ratio of imaginary and real parts of permittivity of the dielectric [38] and this permittivity is equal to:

$$\varepsilon = \varepsilon' - j\varepsilon'' = \varepsilon_r\varepsilon_o(1 - jtan\delta) \qquad \text{Equation 3.1}$$

Where $\varepsilon' = \varepsilon_r\varepsilon_o$ Equation 3.2

And the dielectric loss (α_d) is the total loss contribution from the substrate and is given by [7][8]:

$$\alpha_d = 8.867\pi \frac{tan\delta_c}{\lambda_0} \frac{\varepsilon_r}{\sqrt{\varepsilon_{re}}} \frac{\varepsilon_{re}-1}{\varepsilon_r-1} \qquad \text{Equation 3.3}$$

where the attenuation α_d is given in dB/metre, $tan\delta_c$ is the loss tangent, λ_0 is the free space wavelength. ε_r is the relative permittivity and ε_{re} is given by ε_{re}= (ε_r−1)/2 where 8.867 (1 Np= 20/ln10 dB) is to convert nepers to dB. It can be noted from the equation that the dielectric loss is directly proportional to loss tangent which means the higher the loss tangent, the higher the dielectric loss will be. The dielectric loss is the loss due to the conductivity of the substrate as well as dipole relaxation phenomena which gives rise to loss.

The conductor loss is the total loss associated with the conductor. Since this will have its resistance and inductance. These are series inductance and series resistance in the lumped element view (figure 3.1). As the frequency varies, the line inductance and resistance will change with changes in skin depth. Skin depth is a function of frequency, resistivity and permeability and is defined as:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \qquad \text{Equation 3.4}$$

Where δ= skin depth (m), μ=permeability (4π* 10^{-7} H/m) note: H = Henries = Ω*s,

σ= conductivity (mho/m) note: mho [℧] = Siemen [S]

The resistance of the conductor will be affected by the skin depth as well as the surface roughness. In addition to the conductor and dielectric loss, radiation loss can also occur in coplanar lines. Any discontinuities can give rise to unwanted modes (such as the odd mode)

resulting in radiation loss [11]. At high frequencies, a lot of attention is given to avoiding a highly conductive substrate [13] as this gives rise to majority of the loss and can be significantly be higher than the conductor loss.

For a propagating wave to be completely transmitted through a finite length of transmission line, the line should be terminated by a characteristic impedance (Z_o). This ensures that no signal is reflected. Not only should the termination take the value of the characteristic impedance but also the transmission line should have the same impedance otherwise, as a wave propagates through the transmission line, some of the signal will be reflected back resulting in a transmission loss. Applying the Kirchhoff's laws of voltage and current to the lumped element equivalent circuit shown in figure 3.1 and solving the equations, leads to the equation for characteristic impedance Z_o and the propagation constant. The mathematics behind it can be found in most books dealing with high frequency transmission lines (e.g. in [9]).The characteristic impedance is defined [10] as:

$$Z_o = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \qquad \text{Equation 3.5}$$

And the propagation constant is described as [10]:

$$\gamma = \alpha + j\beta = \sqrt{(R+j\omega L)(G+j\omega C)} \qquad \text{Equation 3.6}$$

where α is the attenuation and β is the phase constant. The propagation constant is a complex parameter like a characteristic impedance and it describes the behaviour of the transmission line.

3.2 Characterization of transmission lines

The transmission lines required are drastically smaller in size at microwave frequencies. At these frequencies, the two port is completely characterized using scattering parameters (S parameters) [14]. By definition, a two port network is defined when the device has two terminals, one for excitation (input) and other to measure the response (output) [34]. S parameters provide the complete characterization of the transmission line giving an accurate measurement of the performance of transmitted and reflected signals of the line. S parameters in simple terms are the ratio of voltages (voltage out versus voltage in) or the ratio of incident wave to the reflected wave [14]. The usual units are decibels. Since S parameter is a voltage ratio then S_{ij}(dB) is given by 20*log(S_{ij}(mag)). S parameters are written in matrix form, so for a two port device, it can be

explained by looking at the block diagram as shown in figure 3.2[33]. Where a_1 and b_1 are the incident wave and reflected wave at port 1 and a_2 and b_2 are the incident wave and reflected wave at port 2 respectively[33].

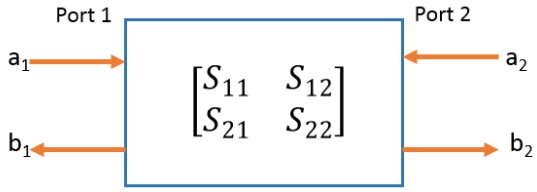


Figure 3-2– Block diagram to define S parameter [33]

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad Forward\ Reflection\ Coefficient \qquad \text{Equation 3.7}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad Reverse\ Transmission\ Coefficient \qquad \text{Equation 3.8}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad Forward\ Transmission\ Cofficient \qquad \text{Equation 3.9}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad Reverse\ Reflection\ Cofficient \qquad \text{Equation 3.10}$$

The first subscript represents the output port whereas second subscript represents input port (port which is excited). So S_{11} means that port 1 is excited and its response is measured at port 1. It represents the input reflection coefficient at port 1 when output port is terminated by a matched load [14]. S_{21} means that port 1 is excited and its response is measured at port 2 and represents the forward transmission coefficient. S_{12} represents the reverse transmission coefficient when the input is terminated by the matched load [14]. S_{22} represents the output reflection coefficient when the input port is terminated with matched load [14]. Since the transmission line is a passive component and is symmetrical $S_{11}=S_{22}$ and $S_{21}=S_{12}$. Hence the S parameters of two ports is defined as:

$$S = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \qquad \text{Equation 3.11}$$

To achieve the condition of maximum power transfer, the characteristic impedance of the line should be equal to the source impedance (typically 50Ω). This also means that nothing will be reflected back and the entire signal will be transmitted. The insertion loss is the loss when a device is inserted into the network. If P_i is the input signal power, P_o is the output signal power received at output with the device inserted [15]. The insertion loss (S_{21}) consists of attenuation loss in the line and reflection loss due to mismatch.

$$Insertion\ loss = reflection\ loss + attenuation\ loss \quad \text{Equation 3.12}$$

$$Insertion\ loss = \frac{P_o}{P_i} = \frac{P_i - P_r}{P_i} * \frac{P_o}{P_i - P_r} \quad \text{Equation 3.13}$$

$$10log\left(\frac{P_o}{P_i}\right) = 10log\left(\frac{P_i - P_r}{P_i}\right) + 10log\left(\frac{P_o}{P_i - P_r}\right) \quad \text{Equation 3.14}$$

Below are the formulas to find the reflection coefficient and the reflection loss. The return loss is equal to - 20log|Γ| [15]. The reflection coefficient is the ratio of the reflected power to the incident power [4]. If no signal is reflected back then the reflection coefficient is equal to 0 and if all the signal is reflected back then the reflection coefficient will be equal to 1 [4].

$$Reflection\ coefficient\ \Gamma = \frac{Z_L - Z_o}{Z_L + Z_o} \quad \text{Equation 3.15}$$

$$Reflection\ loss = 10log(1 - |\Gamma|^2) \quad \text{Equation 3.16}$$

Where Z_L is the impedance of the load and Z_0 is the impedance of the source. The reflection coefficient represents the reflections due to mismatch in impedance between the load and the source. The attenuation loss and reflection loss can be extracted from return loss (s_{11}) and insertion loss (s_{21}) data.

3.3 Discontinuities of coplanar line

Coplanar lines have many applications e.g. monolithic microwave integrated circuits (MMIC), on chip transmission lines. Their performance is however limited by discontinuities such as bends, tapers and T junctions. However, these discontinuities have not been studied extensively in the

past and are believed to degrade the performance[19]. As for the bends, the technique mostly used to improve performance was the use of air-bridges to suppress the unwanted modes which generate radiation. However, the use of air-bridges complicates fabrication and alters the impedance to the line [35]. The un-wanted (odd) modes are generated due to a difference in path length between two slots on the bend causing the signal to distort and generate radiation[20]. Dielectric overlay has also been suggested to reduce this effect [36].

In 1992, Alexandrou et al. [21] studied the transient behaviour of coplanar waveguide bends on GaAs substrates to understand propagation characteristics, where 2 bends correspond to 1mm of length, 4 bends correspond to 2mm and with total length equal to 10mm corresponding to 20 bends. The substrate used was undoped GaAs with a thickness of 500µm, while the signal line and gap were 50µm each and were fabricated using Au. The three different types of bends (square bend, chamfered bend and the round bend) were studied along with a straight coplanar line. A sampling beam was used for measurement at different points (measured after 2, 4, 10 and 20 bends). The measured results are presented in figure 3.3.

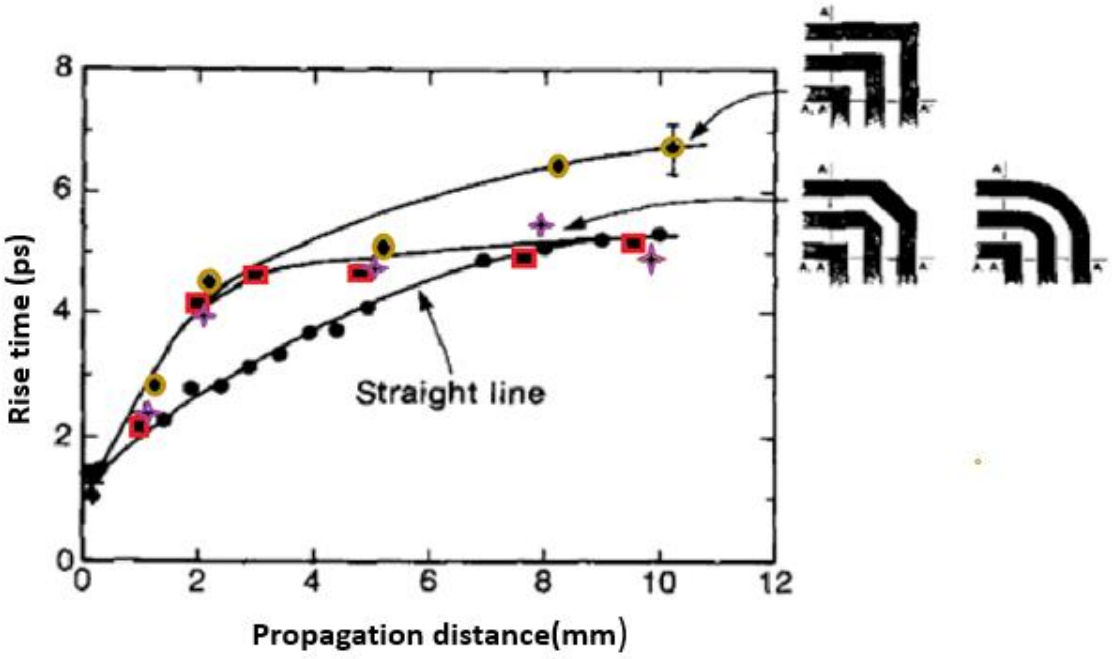


Figure 3-3– shows the rise time vs propagation distance for different type of bends as well for the straight line(reproduced from [21]).

The author did not differentiate between chamfered bends and round bends but referred to it as a “smooth” bend line. The colour has been added to the graph (figure 3.3) for easier illustration where the black points presents the results for the straight line, brown circles represent the results for the square bend and the red and purple represent the points for the “smooth” bend.

For 2 bends at 1mm and 20 bends at 10mm, the smooth bend and straight coplanar line showed a similar response. At 1mm, the square bend required higher rise time by 1ps when compared with the straight line. The rise time for the smooth bend was found to level off after 4mm of propagation length. Hence the bandwidth of the bends was found to be in the region of 100GHz with limited signal distortion. Where to achieve 100GHz performance, the rise time ($rise\ time = \frac{0.35}{f}$) should be equal to 3.5ps at the 3dB point. They also studied the behaviour when the two grounds were wire-bonded and found that unwanted modes were suppressed and propagating waves exhibited less distortion.

In 1993, Omar et al [22] studied the effect of air-bridges added to coplanar waveguide 90° bends, which should supress the parasitic slot-line mode and in return reduce radiation loss. The comparison was made between non-mitred and mitred coplanar bends with theoretical air-bridges, and it was concluded that the result is slightly improved with the mitred bend. The authors only presented the measured mitred coplanar bend results along with theoretical predictions, as shown in figure 3.5. The dimensions are presented in figure 3.4 where the units are µm and the dielectric constant of the substrate was equal to 12.9.

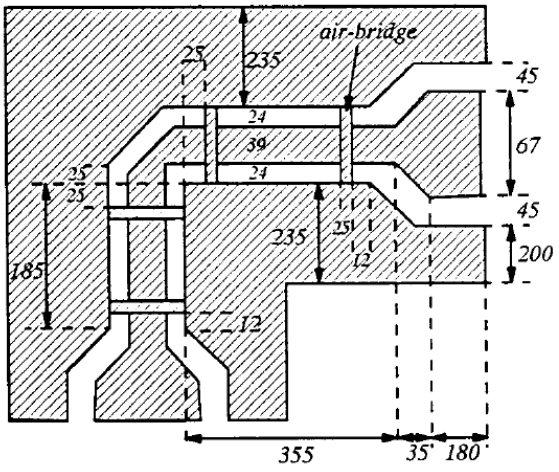


Figure 3-4–Measured mitred coplanar bend with air-bridges [22]

The measured results are shown up to 25GHz in figure 3.5, where the transmission loss was found to be higher than the theoretical value, whereas the reflection loss was the same for experimental results and theoretical predictions. Also, with the aid of the theoretical method and simulation, the effect of air-bridge width, length, and height on the performance were studied and it was concluded that if the air-bridge dimensions and location are chosen properly, it can minimize the losses. However, the results were not presented for bend without air-bridge hence it is difficult to draw a comparison on how much improvement was achieved by adding air-bridges.

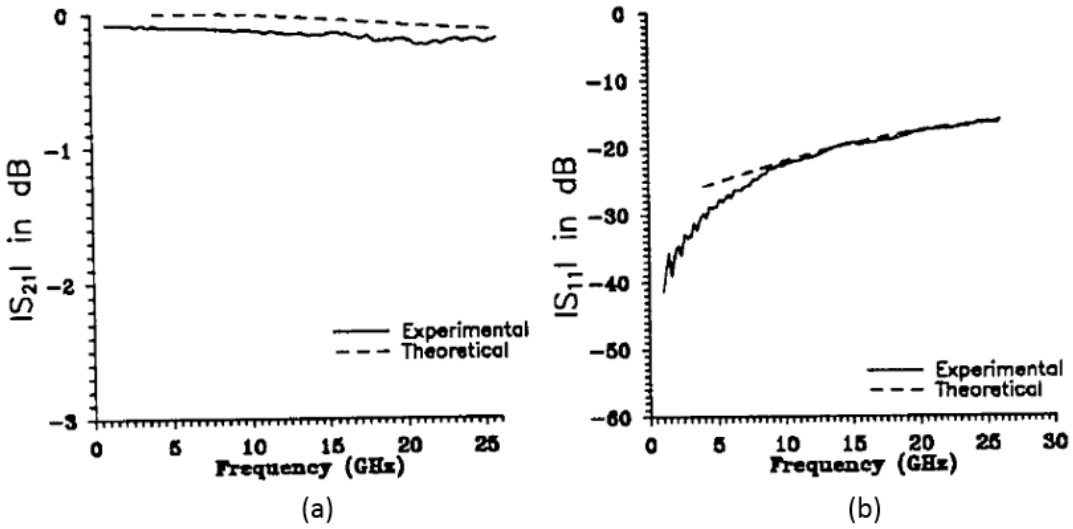


Figure 3-5–comparison between measured and theoretical results [22].

In 2000, Beilenhoff [23] studied the effect of adding air bridges to a coplanar line in monolithic microwave integrated circuits (MICC), where the signal line width was equal to 15µm, the gaps were equal to 10µm and the height of the air bridge was varied between 2µm and 3µm. It was found that not only is capacitance added due to the air-bridges, but that the inductance of the line is significantly reduced which affects the impedance of the line. Thus the air bridge effects cannot be simply modelled by adding capacitances and the equivalent circuit for an airbridge is shown in figure 3.6.

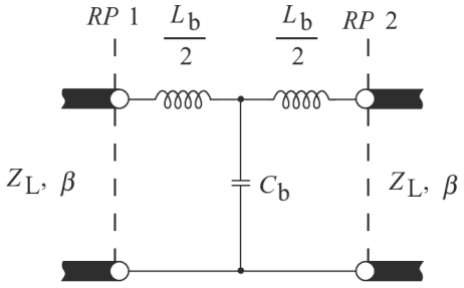


Figure 3-6– Equivalent circuit for an airbridge [39].

Since the air-bridges, increase the fabrication cost and the impedance of the line is also affected, an alternative solution needs to be explored. As a result, in 2009, Kim and Drayton [20] presented a wire-bond free technique which consisted of slowing down the wave on the shorter slot (a similar effect to using a dielectric overlay) to compensate the path length difference between the gaps (shown as path1 and path2 in figure 3.7). The corrugated structure increases the electrical length as shown in figure 3.7.

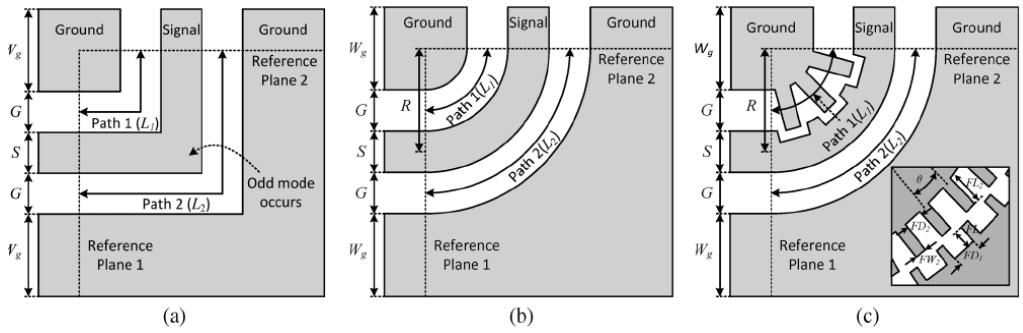


Figure 3-7–(a) square bend (b) rounded bend (c) rounded bend with slow wave compensation. Where L_1 and L_2 represents physical lengths for inner and outer slots (reproduced from [20])

The signal width, gap, and ground plane were equal to 225µm, 130µm and 1350µm respectively where the radius for the round bend was equal to 1500µm. Due to the dimensions being significantly bigger as compared to the bends needs for the electrode, it is possible to incorporate a slow wave structure on one slot with significantly larger dimensions. Six different structures were fabricated on a highly resistive silicon wafer with thickness of ~400µm and resistivity >2000Ω.cm. Straight coplanar lines, square bends for reference and the round bends with a slow-wave structure of two different lengths were fabricated. Measurements were then carried out up to 50GHz using Cascade Microtech ACP250 GSG probes and the setup was calibrated using a TRL calibration technique.

Figure 3.8 (a) shows the insertion loss for a straight coplanar line, a square bend and a round bend with a slow wave compensation on a shorter slot where the total length for all the structures are equal to 4.7mm. The corresponding return loss is shown in (c). The insertion loss for the three structures but with a longer length (8.7mm) is presented (b) and the return loss in (d).

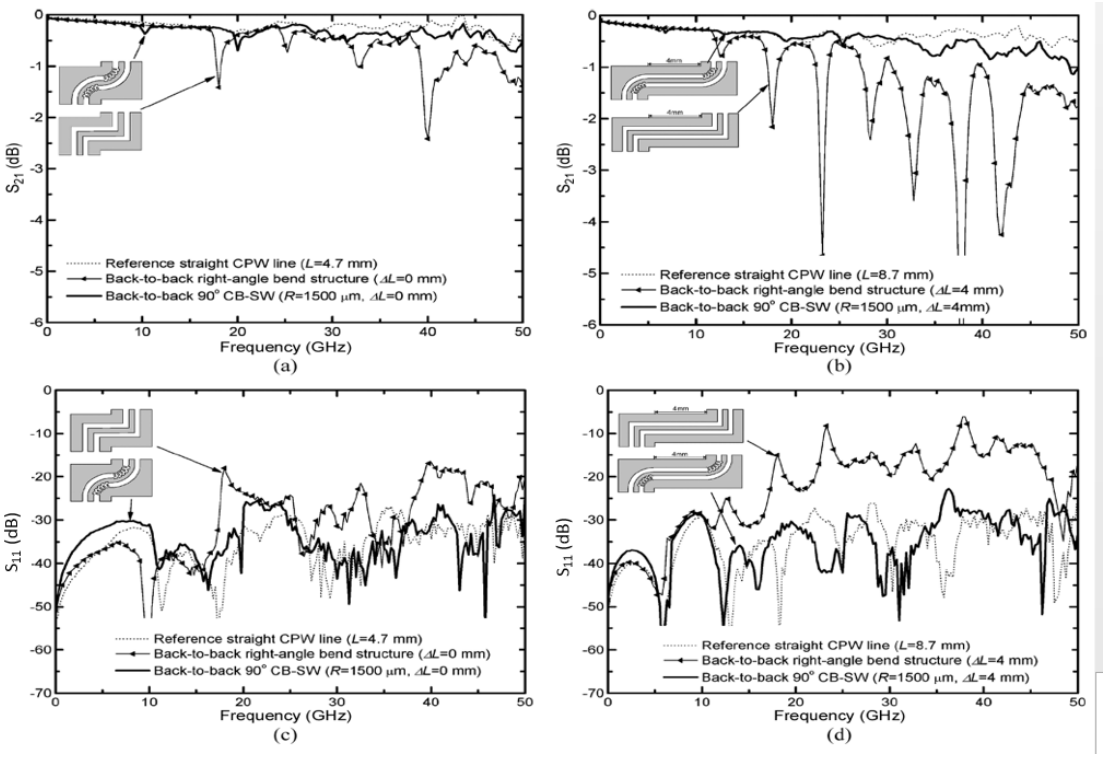


Figure 3-8–(a) transmission loss for reference straight CPW, right bend and rounded bend with slow wave compensation where L=4.7mm (b) transmission loss for reference straight CPW, right bend and rounded bend where L=8.7mm (c) return loss for reference straight CPW, right bend and rounded bend when L=4.7mm (d) return loss for reference straight CPW, right bend and rounded bend where L=8.7mm (reproduced from [20])

The transmission loss (shown in (a)) due to the square bend with respect to rounded bend with show wave compensation and the straight coplanar waveguide (CPW) is much higher and the resonance peaks at certain frequencies was also observed whereas for the rounded bend with the slow wave compensation, the resonances were not observed and the behaviour was found to be more aligned with straight line coplanar line. This indicates that odd modes were not generated in the rounded bend with slow wave compensation. The return loss shown in (c) is also higher for the square bend. When the length of the coplanar line as illustrated in (b), was increased by 4mm with respect to (a), the resonance peaks became more pronounced. The transmission loss for rounded bends with respect to straight lines increases after 25GHz, with an increase of 0.5dB at 50GHz. The return loss for rounded bend with slow structure was also found to behave in a similar fashion to the straight coplanar line.

In 2010, Zou *et al* [19] presented bends on a conductive (conventional) silicon substrate of about 10Ω.cm with silicon dioxide layer and limited thickness of aluminium layer. They referred to them as ‘on-chip’ transmission line bends and differentiated from previous work which was referred to

as 'off-chip' in this paper. The lack of work on 'on-chip' transmission line bends was acknowledged. The signal width, gap and ground plane were equal to 20µm, 9µm and 20µm respectively. The silicon substrate, oxide and metal thicknesses were 500µm, 1µm and 0.5µm respectively. The mitred angle is defined as a percentage and is equal to $Mitred = \left(\frac{x}{d}\right) x100\%$ [32] where *x* and *d* are shown in schematic for the bend presented in figure 3.9.

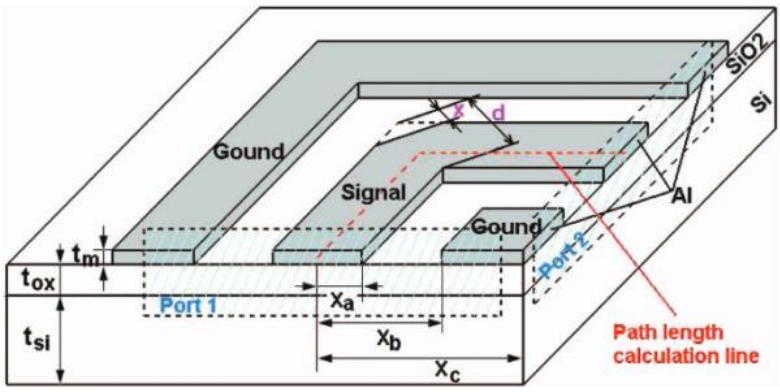


Figure 3-9–schematic of signal coplanar bend (reproduced from [19])

A cascaded structure consisting of 12 bends was fabricated along with the same length of straight coplanar line for comparison. The number of bends was chosen to boost the losses allowing for easier analysis and also to see if an even number of bends compensates for asymmetrical path length. Figure 3.10 shows the measured S parameters for a straight coplanar line and the structure with mitred bends, measured up to 20GHz. No noticeable insertion loss due to the mitred bend was observed. The reflection loss was also found to be aligned with the straight coplanar line. This indicates that, if the 50% mitred bends are used of the dimensions used in this paper, then the losses due to bends are negligible up to 20GHz, although larger bandwidths may be required.

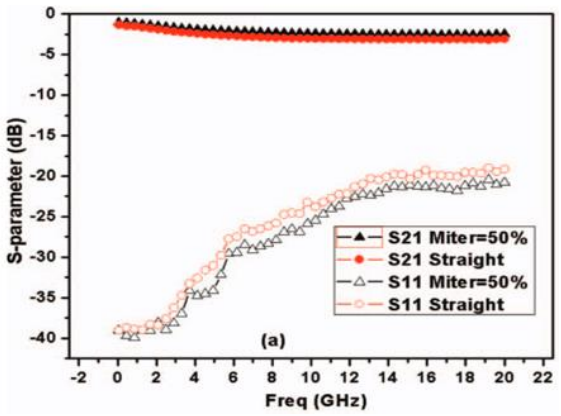


Figure 3-10–(a)S_{21} for straight coplanar line and mitred (reproduced from [19])

HFSS simulations up to 20GHz were then conducted for other types of bend as shown in figure 3.11(a) and the simulated results are presented in figure 3.11 (b) and (c). The simulation results suggest that at these dimensions of the coplanar line, the air-bridges would give the highest loss. This is probably because, as the dimensions of the coplanar line becomes smaller, it becomes more susceptible to the added capacitance of the air-bridges. Also, the simulation results suggest that the mitred bend performs better than all of the other bends that were considered. The simulation results showed good agreement qualitatively but the loss in the measured results was typically found to be higher. The losses due to metal roughness was neglected in the simulation hence the reason that a higher loss was observed in the measured results. Since 2010, no further results on coplanar bends have been reported.

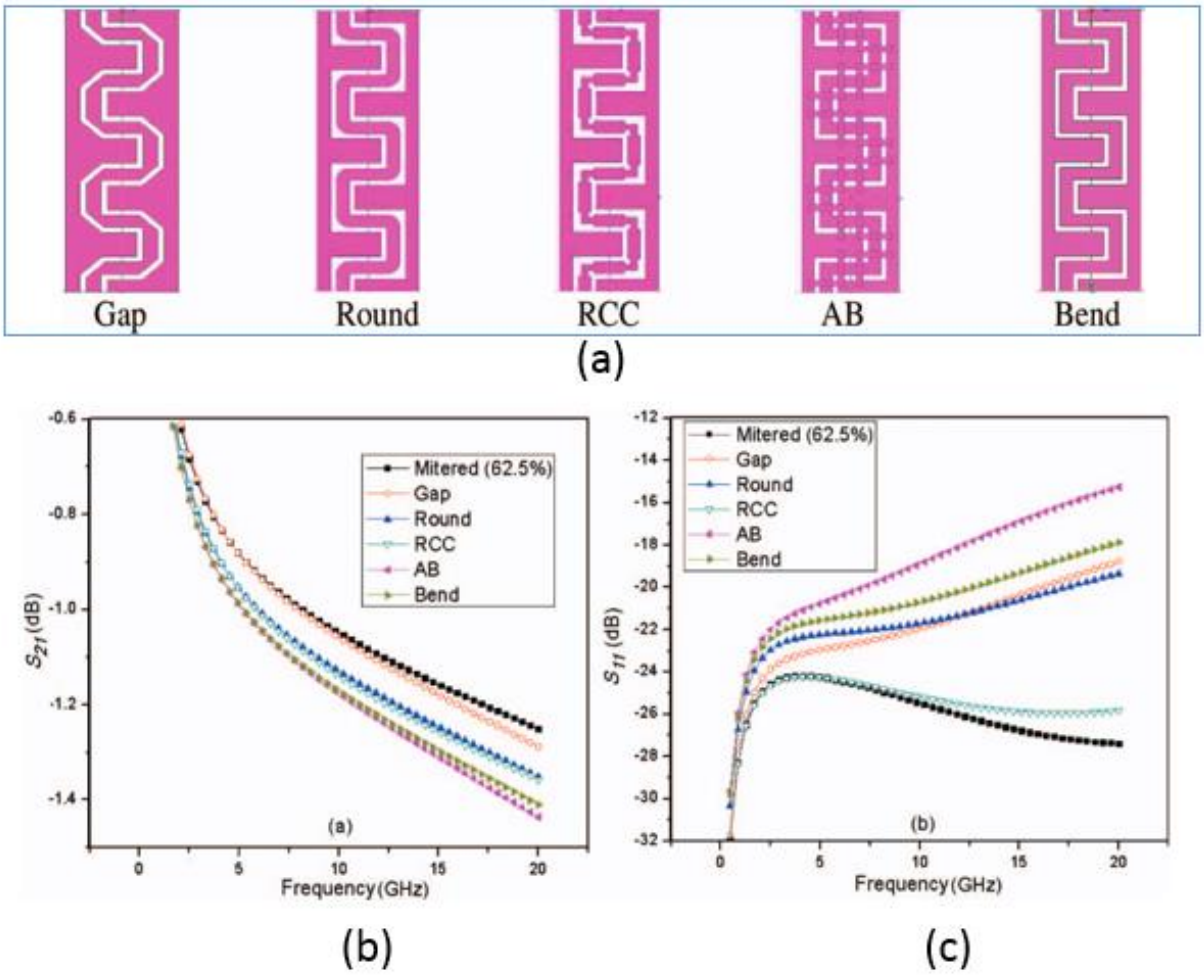


Figure 3-11–(a) Gap: mitred bend with constant gap, Round: round corner at the bend, RCC: reduced signal conductor width at the corners, AB: air-bridges added and bend:

Square bend (b) Simulated S_{21} for the bends shown in (a). (c) Simulated S_{11} for bends shown in (a) (reproduced from [19])

From the literature, it can be concluded that the dimensions as well as the substrate plays a major role in the performance of the bends and the closest dimensions to the electrode to be used for the modulator was presented in [19] where the gap was equal to 9µm but the results were presented up to 20GHz whereas the required frequency range is up to 40GHz or beyond. The optimized gap of the electrode for modulator is in the region of 4µm. If the gap is too big then the resistance of the PN junction will be higher and if the gap is too small then it will increase the optical loss since the metal will be too close to the waveguide as some of the optical signal will be lost to the electrode. To author's best knowledge the bend loss for 4µm for required frequencies (0-40GHz) has not been studied till date. This makes it essential to explore the behaviour of bends for the modulator electrode's dimension needs.

3.4 Substrate loss

Ru-Yuan Yang *et al.*[16] studied the losses due to the different resistivities of silicon substrate for frequencies up to 10GHz. Figure 3.12 shows the measured attenuation per unit length for conventional p type silicon with low resistivity (10Ω-cm) and the float zone with high resistivity (7000 Ω-cm). It can be seen that the loss/mm is much higher in the case of the conventional substrate and loss increases as the frequency increases whereas the loss for float zone silicon is low, and the attenuation loss per length is not affected significantly as the frequency increases.

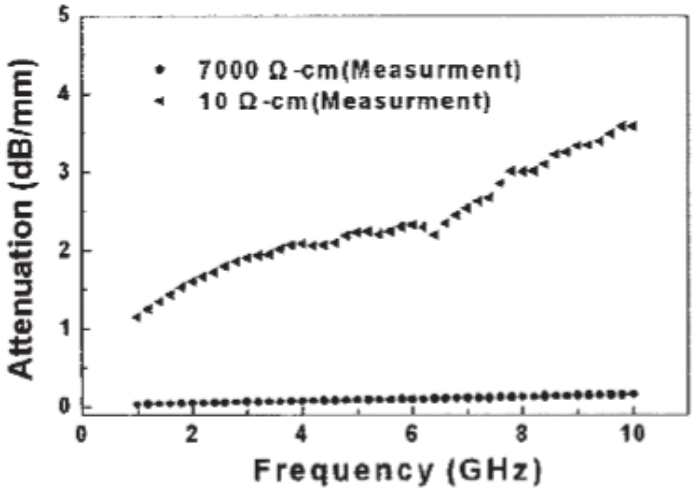


Figure 3-12– the measured attenuation loss per unit length for high resistive float zone and conventional silicon [16]

As discussed earlier, an increase in the width of the signal line will increase the distributed capacitance per unit length. Zaage and Groteluschen [17] studied the effect of the transmission line width on conductive silicon substrates up to 20GHz. Figure 3.13 shows the distributed capacitance C versus frequency for two different resistivities of silicon for a series of different transmission line widths. Figure 3.13 (a) shows the graph for distributed capacitance of silicon with resistivity of 6Ω-cm. It can be observed that at low frequencies the capacitance is high for wide signal lines but as the frequency increases the capacitance decreases and converges to the same value. This is because when the period of the signal is larger (at low frequencies) compared to the relaxation time of the charge beneath the signal line of the substrate then the charge does not penetrate deeply into the substrate which leads to a high capacitance [17]. As the frequency increases the charge cannot follow the process as the electric field changes rapidly. This leads to an increase in charge penetration depth which gives a lower capacitance.

The relaxation time decreases with the substrate's conductivity [17]. Consider (b) in figure 3.13 which shows the capacitance for a doped (conductive) silicon substrate. The relaxation time for the doped wafer has decreased, thus charge will be able to be orientated along the electric field until the relaxation time of the charge is greater than period of the frequency. Thus the decrease in capacitance is very minimal[17].

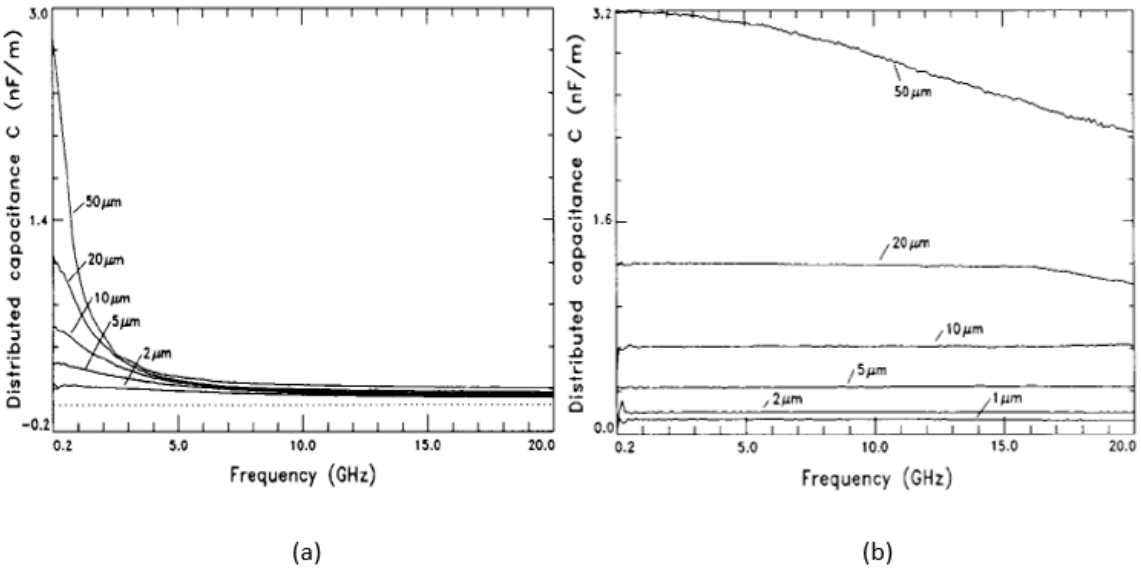


Figure 3-13–(a) Distributed capacitance versus frequency for silicon with resistivity= 6Ω-cm. (b) Distributed capacitance versus frequency for silicon with resistivity= 0.01Ω-cm[17]

A highly conductive substrate will not only impact the capacitance but also the shunt conductance (G) which arises due to the substrate. Figure 3.14 shows the attenuation per unit length for a low resistive (doped) silicon substrate for different widths of the signal line. At lower frequencies, the wider the signal line the lower the attenuation is but at higher frequencies the

opposite can be observed. As the line is made wider the line becomes less resistive thus series resistance(R) per unit length decreases with increasing width of the signal line. This series resistance is affected by frequency and it will increase with increasing frequency due to skin effect phenomena. However, when the substrate is conductive and the line is made wide then the interaction between the line and substrate is higher causing the shunt conductance (G) to increase significantly. This is why the total attenuation of the line is much greater for the wider line at higher frequencies when fabricated on a conductive substrate[17].

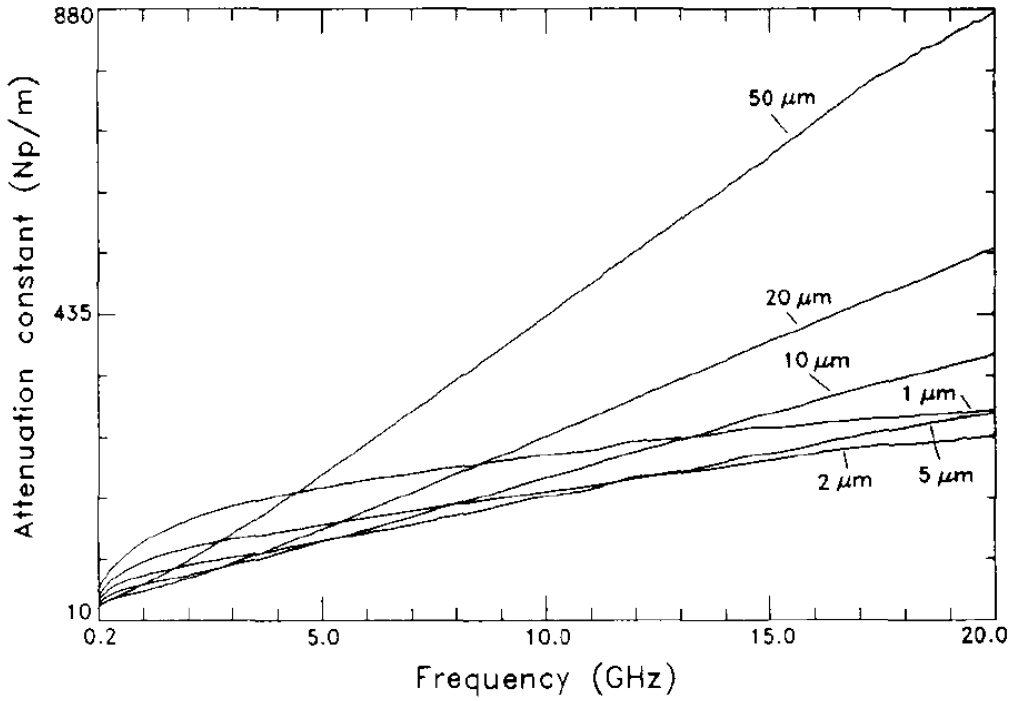


Figure 3-14– Attenuation per unit length presented in nepers/metre versus frequency up to 20GHz for substrate with resistivity 0.01Ω-cm[17]

In 2013, Shu *et al*. [18] characterized coplanar lines on top of a silicon dioxide layer on a silicon substrate (8000Ω-cm, 15Ω-cm, and 0.015Ω-cm). The silicon dioxide was thermally grown on top of the silicon and the metal used was gold with thickness of 1μm (measured up to 110GHz). The insertion loss and reflection loss of the coplanar line was presented for three different resistive substrates. Figure 3.15 shows the graph of attenuation loss per unit length for three different resistive substrates. As evident from the graph, the loss due to highly doped silicon is significantly higher as compared with conventional silicon and a high resistivity substrate (HRS). At 40GHz, 8000Ω-cm silicon gave a loss of 0.6dB, 15Ω-cm silicon gave a loss of 3.2dB and 0.015Ω-cm silicon gave a loss of 45dB.

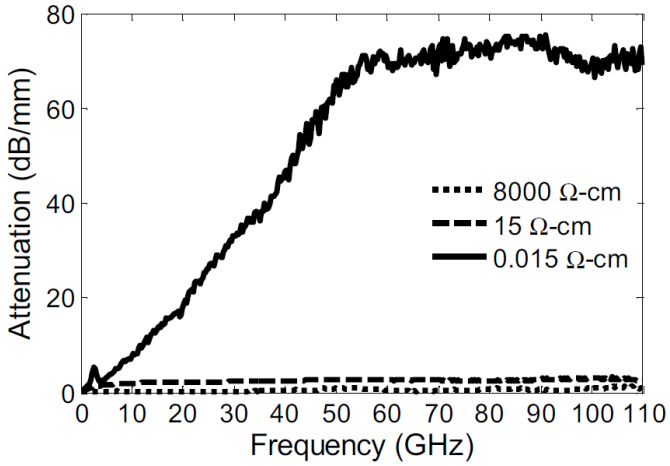


Figure 3-15–Attenuation loss per unit length for 0.015Ω-cm, 15Ω-cm, and 8000Ω-cm [18]

The comparison between simulated (conductor loss and substrate loss) and measured total attenuation was also presented for 8000Ω-cm and 15Ω-cm, as shown in Figure 3.16. Figure 3.16(a) is for the high resistive substrate (8000Ω-cm) and it can be seen from the graph that the dominating loss in this case is the conductor loss which comes from metal roughness. This gives rise to the resistivity of the metal and increases with frequency due to the skin depth effect. The simulated loss due to the substrate is very minimal. However, in figure 3.16 (b) the reverse can be observed. The simulated loss due to the conductor still stays the same as in the high resistivity case of but loss due to the substrate has shown an enormous increase, hence the total loss follows the trend of the substrate loss which is the dominating loss in this case.

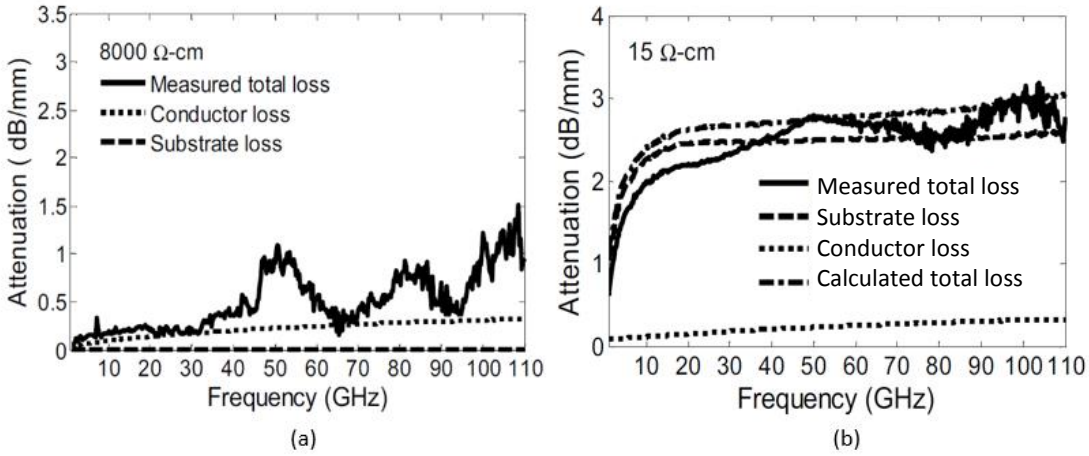


Figure 3-16–(a) shows the total attenuation per unit length and loss for the conductor and substrate in the case of 8000Ω-cm silicon. (b) the total attenuation per unit length and loss for conductor and substrate in the case of 15Ω-cm silicon[18]

As a result of the literature review on the substrate losses, a few conclusions can be drawn.

Firstly, the most apparent observation is that the attenuation loss increases as the substrate resistivity decreases. When the resistivity of the substrate is lowered, the dominating loss comes from the substrate which increases with frequency until the charge in the substrate can no longer respond to the electric field resulting in a saturation of the attenuation loss. The saturation level depends on the resistivity value of the substrate. For a conventional silicon substrate, the saturation is found to occur at around 55GHz [18]. Lower resistivity substrates also give rise to a higher capacitance. When designing the coplanar waveguide, the substrate loss has to be considered to find the trade off point between the resistance (R) and conductance (G). For highly resistivity substrates, the signal line should be chosen to be wider to keep the resistance (R) lower. On the other hand for low resistivity substrates the width of the signal line needs to be small to keep conductance (G) low.

3.5 Slow wave electrodes

Due to substrate loss in conventional silicon, different ways have been explored to minimize the substrate losses. For instance, micromachining [25] but it is not CMOS compatible. Slow wave propagation on coplanar lines was also first proposed in 1981 [26] to minimize the substrate loss, but due to the technological constrains at the time, flexibility to optimize the slow wave coplanar structure was not possible. With the advances in CMOS processing in the last decade, it has been possible to optimize slow wave transmission lines[27]. With the help of slow wave structures the substrate loss can be reduced to less than 1% [28] and since then it has been explored due to the CMOS compatibility for MMIC applications[29]. Slow wave structures not only eliminate the substrate loss but also the required lengths of the devices are reduced. Slow wave propagation can be achieved by using corrugated metal strips (also referred as strip shields) which are placed below the coplanar line separated by a silicon dioxide layer as an isolation layer (figure 3.17). The corrugated metal strips are either floating strip shields or are grounded.

When the corrugated structures are added, the phase velocity, v_p (equation 3.17) will decrease and so will the guided wavelength. This also affects the effective relative permittivity which will increase and can be interpreted from equation 3.17.

$$v_p = f\lambda_g = \frac{c_o}{\sqrt{\varepsilon_r \mu_r}} \qquad \text{Equation 3.17}$$

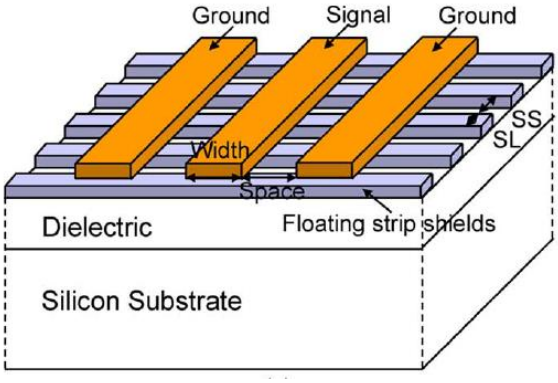


Figure 3-17– Slow wave coplanar line with floating corrugated metal strips (reproduced from [29])

In 2006, Cheung et al. [30] studied the behaviour of the floating and grounded metal strips. They were fabricated using IBM's SiGe-7HP BiCMOS technology interconnect on a 10Ω.cm silicon substrate. The coplanar waveguide had the thickness of 4µm and corrugated metal strips (known as shields) had a thickness of 1.25µm. The oxide layer in between was 4µm thick. Figure 3.18 shows the microscopic view of shielded CPW (S-CPW) line which is 500µm in length.

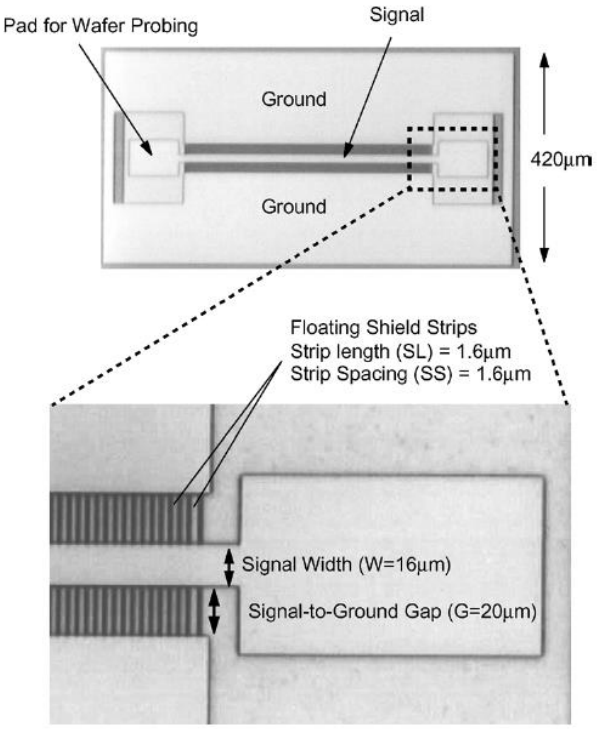


Figure 3-18– microscopic view of S-CPW (reproduced from [30])

Different types of transmission line such as coplanar waveguide (CPW), microstrip (MS) and shielded coplanar waveguide (S-CPW), with different dimensions were studied. Table 3.1 shows the different type of transmission line which were measured from 1GHz to 40GHz.

Table 3.1–Shows the transmission line measured from 1GHz to 40GHz (reproduced from [30])

Transmission Line	Signal Width (W)	Signal-to-Ground Gap (G)	Shield Strip Length (SL)	Shield Strip Spacing (SS)
CPW1	15µm	5 µm	No shield strips	
CPW2	50µm	20µm		
MS1	6µm	4µm (between M4 signal on M3 ground plane)		
MS2	15µm	9.25µm (between M4 signal on M2 and M1 ground plane)		
CPW_REF (on alumina)	55µm	20µm		
S-CPW1	16µm	20µm	1.6µm	1.6µm
S-CPW2	34µm	120µm	1.6µm	1.6µm
S-CPW3	16µm	20µm	10µm	2µm
S-CPW4	34µm	120µm	4µm	5µm
S-CPWG1 (grounded shield)	26µm	120µm	1.6µm	1.6µm

Cheung et al. increased the gap between signal and ground plane of a CPW to achieve high inductance and the shield strips were added to achieve the added capacitance. A simultaneous increase in inductance and capacitance was therefore achieved and hence a higher reduction in the phase velocity. Another way to quantify phase velocity, is to look at the relative dielectric constant. When the relative dielectric constant is higher, then the phase velocity is lower (equation 3.17). Figure 3.19 (a) shows relative dielectric constants for the transmission lines in Table 3.1. We are mainly interested in the coplanar line hence only the CPW results are considered. From looking at figure 3.19 (a), if CPW1 and CPW2 are compared, it can be seen that CPW2 (with larger gap) has a higher effective dielectric constant. When the gap (g=130µm) was increased and shielded strips (in S-CPW2) added, the relative dielectric constant increases significantly. This shows the phase velocity can be decreased by a factor of 10, if required.

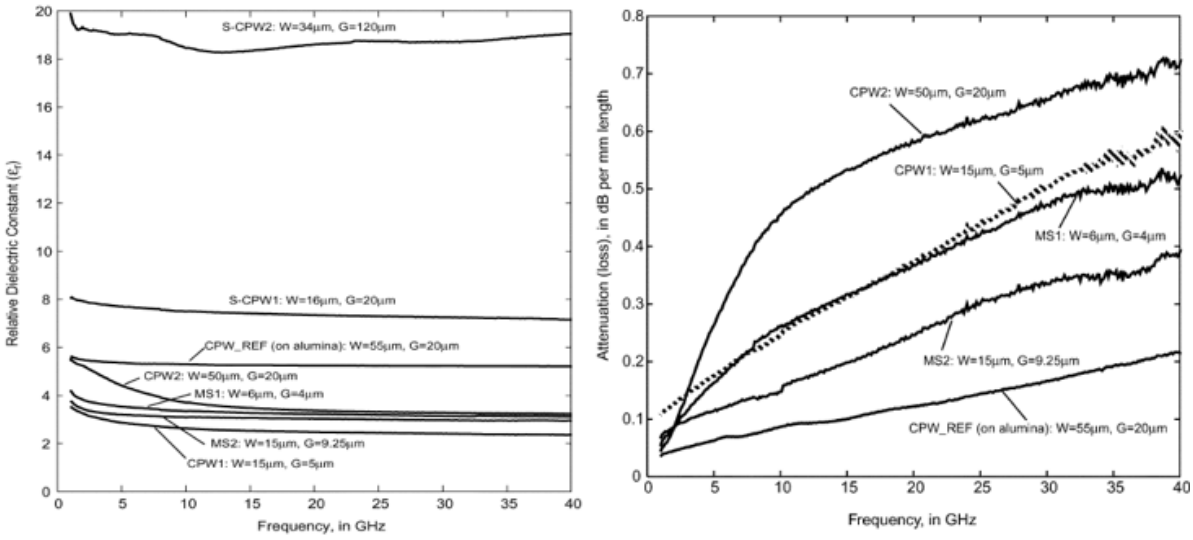
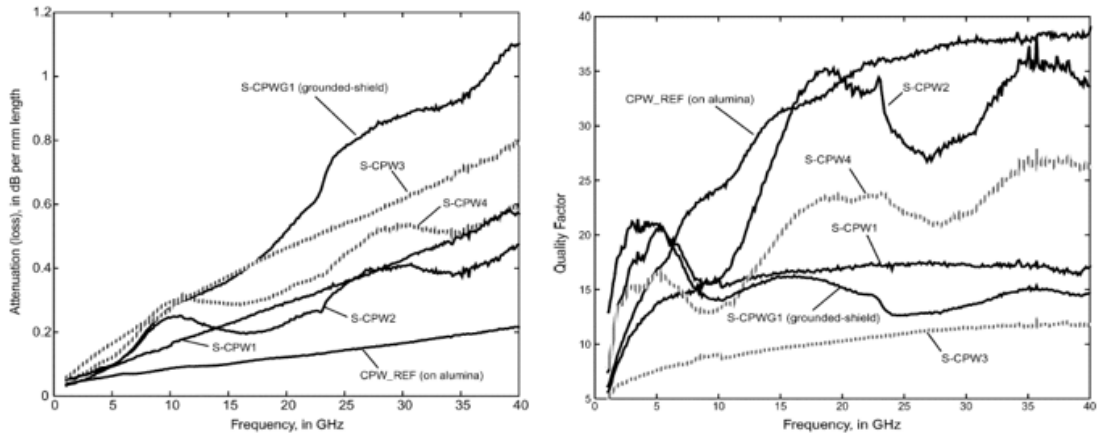


Figure 3-19– (a) measured relative dielectric constant (b) attenuation loss per unit length(reproduced from [30)

Now consider figure 3.19(b) which shows the attenuation loss per unit length. It can be seen that the attenuation loss for CPW2 is higher than CPW1. When the gap was increased, the attenuation loss per unit length also increased. The authors state that the reason for this is because more of the electromagnetic field will be permitted to leak to the substrate. The quality factor is one of the metrics used to determine the overall performance of the device as it takes into account the phase velocity as well as the attenuation. The quality factor(Q) is given by $\frac{\beta}{2\alpha}$ where β is phase delay (in radians/m) and α is attenuation per unit length (in nepers/m). When the quality factor for CPW1 and CPW2 was considered then CPW1 showed a better performance by the factor of ~2 (figure3.20(b)).



(a) (b)

Figure 3-20– (a) Attenuation loss per unit length (b) Quality factor versus frequency (reproduced from [30])

Figure 3.20 (a) shows the attenuation loss per unit length for the shielded coplanar line from [30]. When comparing S-CPW1 (gap=20µm) and S-CPW2 (gap=120µm), the attenuation loss for S-CPW1 and S-CPW2 is similar. Since S-CPW2 has higher inductance, the quality factor of S-CPW2 was found to be better. The quality factor is shown in Figure3.20 (b). When the shield strips were grounded (S-CPWG1) with otherwise the same dimensions as S-CPW2, then the attenuation loss was found to be substantially higher (figure 3.19(a)). The reflection loss was not presented hence it is difficult to the completely interpret where the losses are coming from.

In 2009, Cho et al. [29] presented measured results of slow mode transmission lines (CPW) which utilized the floating corrugated metal strips as well as grounded metal strips. Measurements were performed up to 50GHz. They were fabricated using a 45nm CMOS process. The advantage of using the floating corrugated structure over the grounded structure was to lower the electric field leakage to the substrate and this also gives rise to lower eddy currents. Figure 3.17 shows the schematic of the structure where SL is the strip length and SS is the strip spacing. The density of the corrugated structure is usually defined as the ratio R$\left(=\frac{SL}{SL+SS}\right)$ of the strip dimensions. The signal line width and the gap were equal to 30µm and the ground plane width was equal to 10µm. The dielectric which was used between coplanar line and the metal shield was silicon dioxide with dielectric constant of around 5.4. The dielectric thickness between M8 and M10 is equal to 3.2µm whereas the dielectric thickness is equal to 0.74µm between M9 and M10. The coplanar waveguide was placed on metal layer 10 (M10) and the metal shields were either placed on M8 or M9. The study mainly concentrated on altering the corrugated metal strip dimensions to see the

effects on the attenuation loss as well as on effective relative permittivity. Where effective relative permittivity is calculated using the formula $\left(\varepsilon_r = \frac{c^2\beta^2}{\omega^2}\right)$.

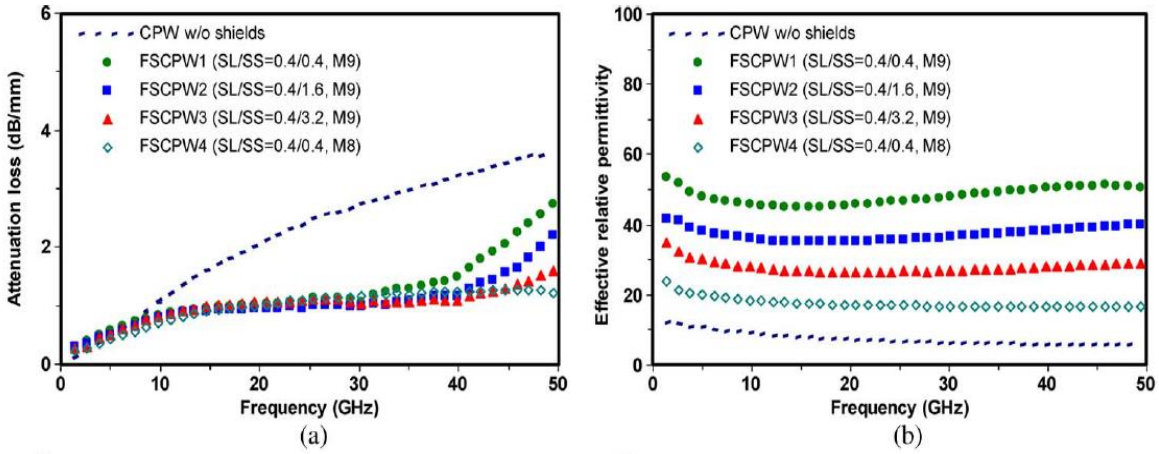


Figure 3-21– (a) shows the attenuation loss with varied dimension of metal strips (b) effective relative permittivity (reproduced from [29])

Figure 3.21 (a) shows the attenuation loss for a slow wave coplanar line with varied dimensions of the floating shield metal strips. SL stands for the shield length and SS is for the shield spacing. It can be seen that the coplanar line with no metal strips gave the highest attenuation loss. The dimensions of the metal strips showed almost no impact up to 30GHz but as the frequency is increased after 30GHz, the dimensions of the metal strips have an impact on the attenuation loss. When the shield width was equal to 0.4µm and spacing was equal to 0.4µm (placed on Metal layer 8) then the attenuation loss was found to be lowest in comparison (light blue curve, figure 3.21(a)) which means the further the shield was placed from the coplanar line, the lower the attenuation loss was found to be. The shield length (SL) was not varied during this experiment. Figure 3.22 shows the effective relative permittivity and attenuation loss versus metal shield ratio (R). It can be seen when R is in the region of 0.5 (meaning that the spacing and the shield width is kept approximately equal) then high effective relative permittivity (~30) and low attenuation loss per unit length (~1dB/mm at 40GHz) can be achieved.

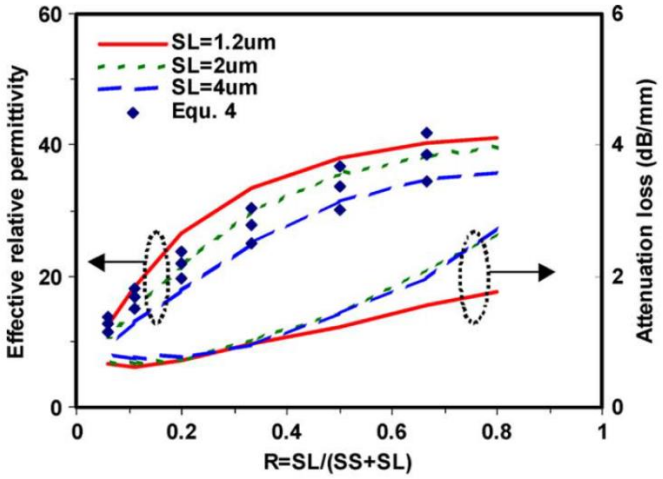


Figure 3-22– effective relative permittivity and attenuation loss versus the metal shield ratio(reproduced from [29])

As a conclusive result, Cho et al.[29] then went on with fabricating and measuring the response of the structure with a shielded strip ratio of 0.5, an oxide separating layer of 3.2µm and with the metal strips on layer M8 and the coplanar line on M10. This time the comparison was drawn between the conventional coplanar waveguide, coplanar waveguide with floating shield and coplanar line with grounded shield (figure 3.23).

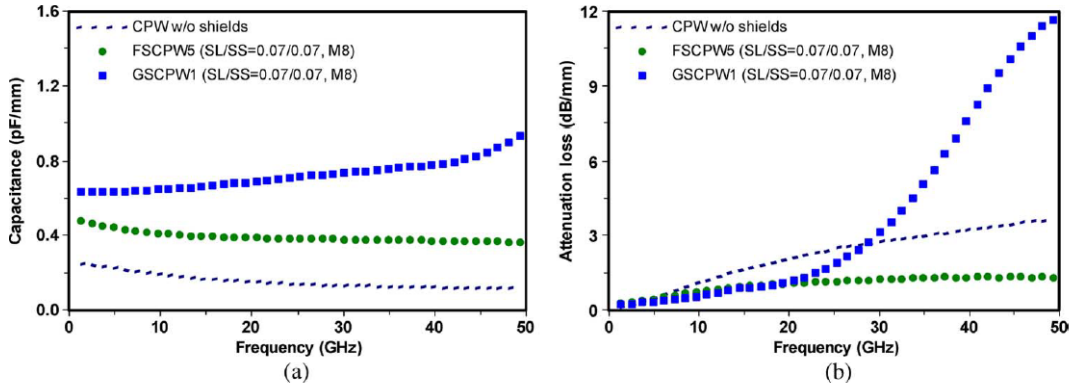


Figure 3-23–(a) shows the capacitance for grounded and floating shield (b) attenuation loss for grounded and floating shields (reproduced from [29])

It can be seen that the grounded shield version will give rise to higher capacitance as compared with the floating shield structure. When the attenuation loss for both is compared (figure 3.23(b)), it can be noted that up to 20GHz, the attenuation loss is equal for both the grounded and floating shield and is lower than the coplanar line. As the frequency increases beyond 20GHz, the attenuation loss increases substantially for the grounded shields. This is because the eddy current is higher in the grounded shields which is proportional to square root of frequency [29]. Therefore if the frequency range is below 20GHz then the grounded shield is a better option as this will give

a higher capacitance and low attenuation. If the frequency range extends beyond 20GHz, then the floating shielded coplanar line should be opted for.

In 2013, Franc et al. [27] mainly presented simulation results up to 110GHz for the corrugated metal strip structure. From the simulation results, it was interpreted that the electrical and magnetic field occurrence is mainly restricted in between the coplanar waveguide and floating shield which is why the loss contribution from the substrate is almost negligible. The magnetic field strength weakens while moving away from the coplanar waveguide and this magnetic field generates eddy currents in the floating metal shields. The coplanar line gaps considered in this paper were 20µm and 50µm and the line widths were 7µm, 5µm and 30µm. Figure 3.24 shows the simulated results for loss in the floating shield structure when the ratio of the metal shield is varied. The R ratio is denoted as d in this paper and is given as a percentage. It can be seen that when d=80% which means that the strip width is greater than the gap, the metal loss is at its lowest (figure 3.24a) but this gives rise to the highest eddy current loss (figure 3.24b). Hence a trade-off needs to be found between two losses. As a result of this work, it was concluded that the floating shield loss (eddy current and conductor loss) depends on the characteristic impedance and the capacitance of the line[27].

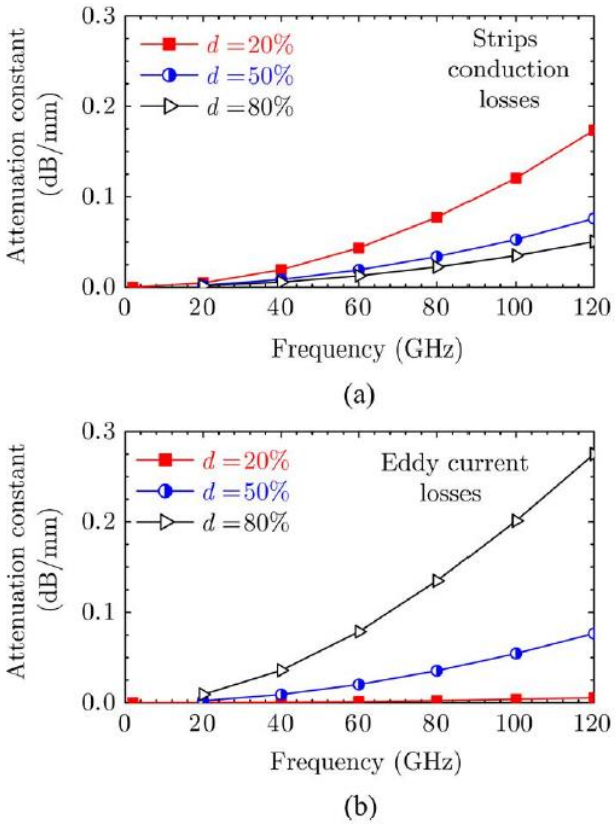


Figure 3-24–(a) simulated attenuation conductor loss for floating metal shields (b) simulated eddy current loss for floating metal shields(reproduced from [27]).

In 2014, Xu et al. [40] demonstrated silicon optical modulator based on MZI up to 70Gbit/s. This is the fastest silicon optical modulator to date. Figure 3.25(a) shows the microscopic view of the modulator and (b) shows the equivalent circuit for it. Z_L was formed by depositing titanium nitride (TiN) film and was designed to be 23Ω and Z_o was designed to be 25Ω. The electrode was 1µm thick where the signal like was equal to 20µm and the gap was equal to 5µm. Gold wire bonds were used at three different locations to maintain the coplanar mode which will also change the impedance of the line.

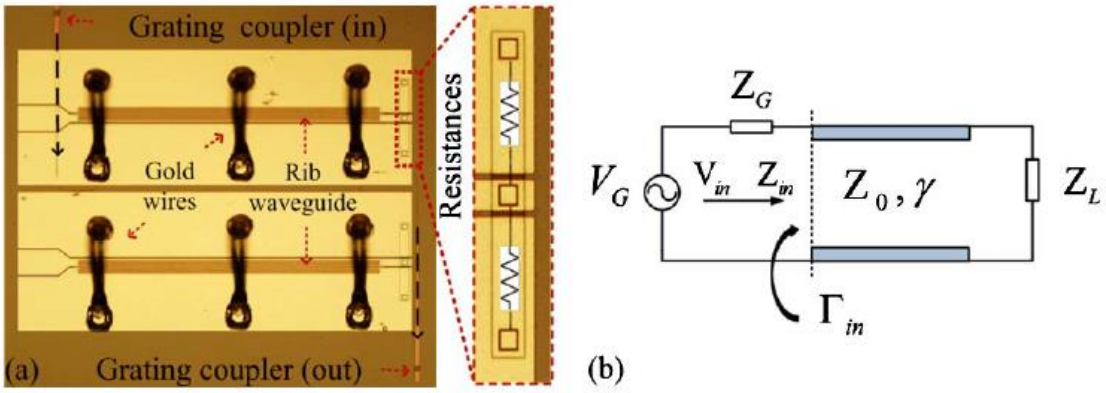


Figure 3-25–(a) microscopic view of the modulator (b) equivalent circuit (reproduced from [40])

As it can be seen from the figure 3.25(a), the total length of the electrode was reduced by eliminating the bend from electrode instead bend was added to optical waveguide. The taper length was not given but the author used straight taper for probing purposes. From microwave engineering perspective, the only results which were presented in [40] were reflection coefficient and the input impedance and they are shown in figure 3.36. The measurement which was carried was 1 port measurement while the other end was terminated with Z_L.

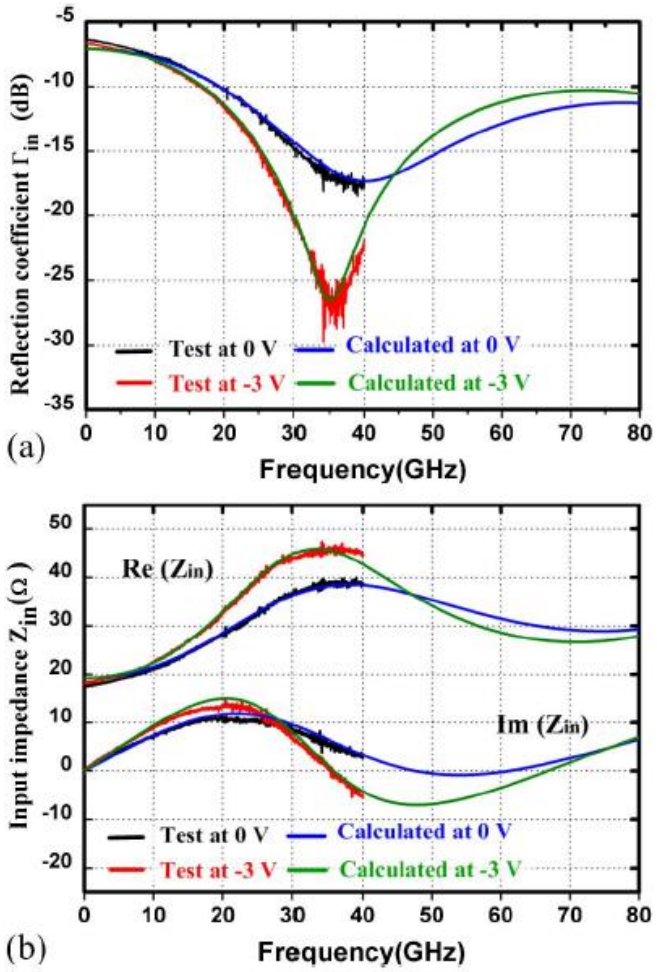


Figure 3-26–(a) Reflection coefficient measured response up to 40GHz and calculated response (b) Input impedance measured response up to 40GHz and calculated response up to 80GHz.

It can be seen the input impedance is around 20Ω at 100MHz (figure 3.26(a)) which causes the mismatch and reflection loss (-7dB) to be high (figure 3.26(b)) at this frequency. Insertion loss results were not presented. The performance of the electrical signal was degraded due to the reflection loss caused by the impedance mismatch. The design change of electrode which gave much higher bandwidth is due to reduced length of the electrode by eliminating the electrode bend but Z_o was designed to be 25Ω which gives impedance mismatch. By adding the gold wire bond the mismatch was further increased as the impedance changed from 25Ω to 20Ω. If the reflection loss is reduced, the results could be further improved.

In 2015, Patel et al. [31] published a paper on a series push-pull (SSP) configured modulator (figure 3.27) with the motivation to improve the microwave losses. Using this configuration a reduction in the capacitance is achieved which causes a velocity mismatch for their design.

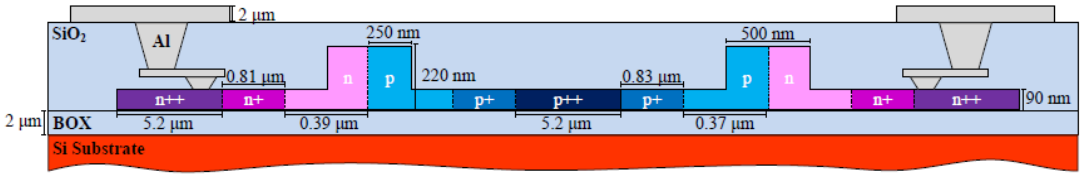


Figure 3-27– Shows the series push-pull (SPP) modulator's cross-section schematic [31]

Hence, Patel et al. theoretically studied the effects of a different electrode design to achieve velocity matching. Figure 3.28 shows three cases which were studied. The authors used a coplanar stripline (CPS) which has got two metal strips where one is at high potential and the other is grounded.

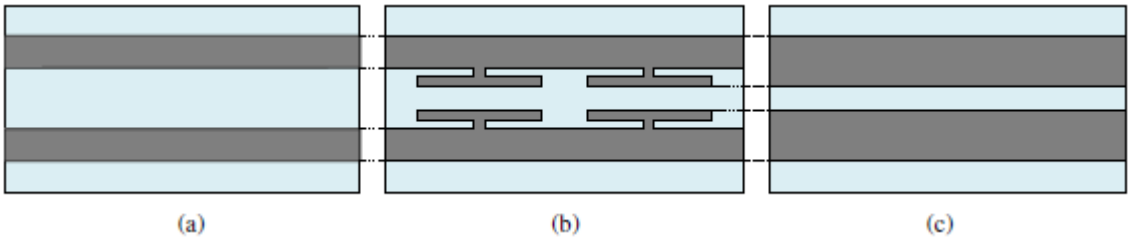


Figure 3-28– (a) coplanar stripline (CPS) where W=120µm and S=51µm (b) T shaped structured added to CPS (c) CPS where W=139.2µm and S=12.6µm [31].

Figure 3.28(a) shows the CPS with large spacing and without the T shaped structures. Case (b) is when the slow wave structures were added to case a (figure 3.28(a)). Figure3.28(c) shows the coplanar strip with smaller gap equivalent to the gap of T shaped structure in figure 3.28(b). Simulation of the structures was carried out using Ansys's HFSS. Figure 3.29 (a) shows the attenuation loss and it can be seen the loss due to (a) is lowest whereas the attenuation loss for cases (b) and (c) are similar. The reasons were evident with further simulation discussed later in the paper. Figure 3.29 (b) shows the effective index of the electric signal. When the refractive index increases the velocity decreases ($v = \frac{c}{n}$) where n is the refractive index. Due to increased spacing between coplanar strip (case b in figure 3.29(b)), the inductance of the line is increased which slows down the electrical signal compared with case (a). When the T shaped structure was added (case b) then the slowing down factor was increased.

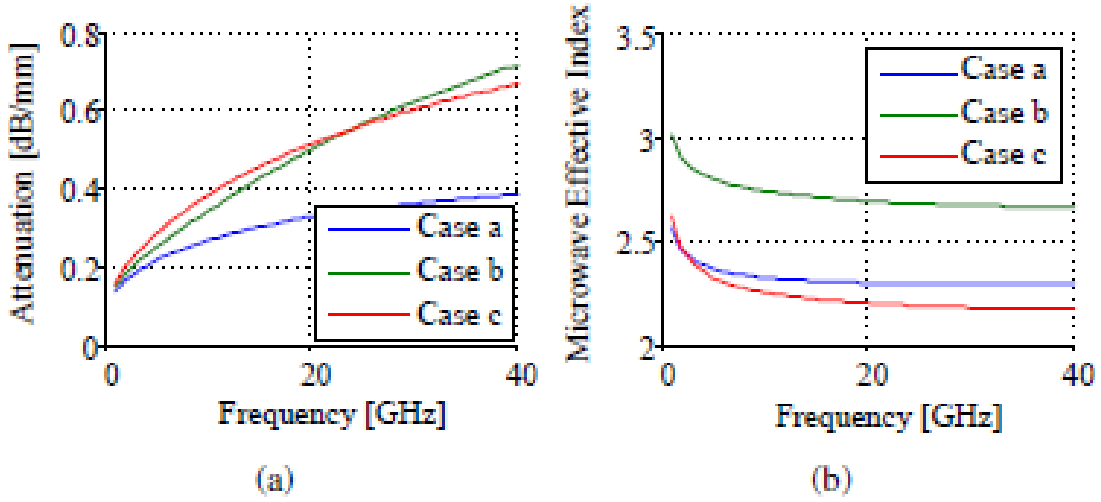


Figure 3-29–(a) shows the simulated attenuation loss for the three cases (b) shows the effective index versus frequency for all three cases [31].

Further simulation suggests that the reason for the lower attenuation loss in case a (figure 3.39 (a)) is due to the resistance and conductance per unit length being lower as compared with the other two cases. Case b (figure 3.29 (a)) has the highest conductance per unit length as well as the highest resistance per unit length hence the highest loss. Case b also has the highest inductance per unit length, which together with the high capacitance per unit length give the highest effective index. Case c gives a higher capacitance compared with case a, and has comparable capacitance to case b due to smaller spacing. Whereas, the inductance is higher for bigger space (case a), and comparable to case b, case c gives the lowest inductance per unit length. The ratio between the inductance per unit length and capacitance per unit length should be maintained or else the characteristic impendence ($Z_o = \sqrt{\frac{L}{C}}$) will be disturbed causing more reflection loss. Although, the T shaped structure (case b) gives a higher effective index which means a slower the electrical signal, the slowing down factor is found to be insufficient even for their case. At 40GHz, case b has the effective index equal to 2.7, case c has effective index equal to 2.2 and case a has the effective index equal to 2.3. If case a and case b are compared then the slowing down factor of 1.17 is achieved. Hence, this approach to reduce the velocity of the electrical wave is of limited value.

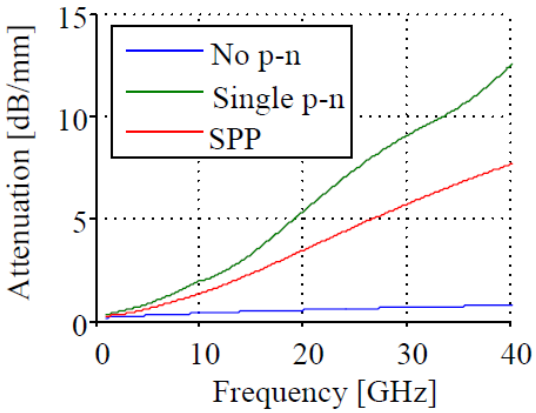


Figure 3.30– Simulated attenuation loss for no p-n junction, with single p-n junction and two p-n junction configured as SPP[31].

Another important simulation result presented by Patel et al. [31] was based on how the positioning of the PN junction has an impact of microwave attenuation loss, where, the electrode structure was kept the same while the p-n junction was varied. The details for the electrode design used were not given, making it difficult to fully appreciate the work in this study. However, the results (figure 3.30) shows that an SPP (series push-pull) configured modulator should give lower attenuation loss and the loss due to p-n junction is the dominant loss. However, the drawback for using the SPP structure over the single p-n junction cited is that it requires higher drive voltage hence the higher power consumption. Patel et al. [31] found the lower microwave loss can be achieved at the expense of higher optical loss.

In this section, we have seen that the substrate losses can be eliminated by using the corrugated metal strips of the slow wave structure which were placed beneath a coplanar line separated by an oxide layer but the slow wave effect will give rise to eddy currents. However, eddy current losses are much lower than substrate loss in conventional silicon, so this is a significant result. Also the slow down factor is in the region of 10 which means the size of the device can be reduced significantly. This will also reduce the overall attenuation loss due to reduced size of the device. It can also be concluded that the floating shield is well suited for devices whose frequency range extends beyond 40GHz and the optimal shield width and shield spacing ratio is 0.5. By optimizing the shield dimensions, dielectric between coplanar line and the shields as well as the coplanar line dimensions, the attenuation loss can be minimized while achieving very high slowing down factor. The positioning of the PN junction in the modulator also has a significant impact on electrical transmission loss and therefore required careful design consideration. However, since the electrode (coplanar line) needs to provide the bias to the PN junction which means the corrugated strips cannot be placed below the coplanar line. However, the same principle can be applied by moving the corrugated strip on top of the modulator's electrode. This requires the

study to see if moving the corrugated metal strips will provide required slowing down factor and if it will reduce the substrate loss.

Literature review on bends shows the bend performance is highly dependent on the dimensions and there hasn't been an invigilation on electrode's dimensions in the required frequency range. Therefore the investigation on coplanar bends with the optimized gap- in the region of 3µm- between 100MHz up to 67GHz is required.

To the author's best knowledge, there has been little work done on coplanar tapers for silicon optical modulators, where the effect of the discontinuity can result in additional loss. However, there has been investigation on microstrip tapers which are used to match two different impedances and are also known as impedance transformer. To understand the complete behaviour of the coplanar taper, the invigilation is required. Hence the author will look into coplanar taper which is requirement for electrode of the modulator over a wide frequency range.

The literature clearly shows how the conductivity of the substrate contribute most to the total transmission loss of the electrode however the dimensions can be altered to minimize this loss. If the substrate is doped -PN junction region- and the resistivity is low, it is better to use dimensions in the region of ~5µm -10µm and where the substrate is not doped – probing pads- the larger dimensions in the region of ~50µm is preferred. This method is utilized for the design of the electrode.

Microwave engineers adapted the slowing down method by adding corrugated metal strips below coplanar waveguide to minimize the required length of the transmission line as well as the substrate loss in MMIC. Other slowing down methods has shown limited slowing down factor whereas the bottom corrugated metal strips showed much higher slowing down factor. Corrugated metal strips will be exploited to see if this can be applied to slow the electrical signal for the modulator but the corrugated metal strips cannot be added at the bottom of the electrode as it provides the bias to the optical signal. Therefore investigation to add the corrugated structure on top of electrode will be carried out. By slowing the electrical signal in the case of slow wave modulator, the mismatch between the optical and electrical signal will be reduced henceforth increase the operating bandwidth. This will reduce the footprint of the device as well as minimize the loss/length due to shorter length.

References

[1] J P Dakin, R G W Brown, 'Handbook of optoelectronics', Vol 1 , CRC Taylor & Francis , 2006 , pp.498

[2] D. M. Pozar,' Microwave Engineering', New York, MA : John Wiley and Sons Ltd, 2nd edition, 1998. pp. 56

[3] C. P. Wen, "Coplanar Waveguide: A surface strip transmission line suitable for nonreciprocal gyromanetic device applications", IEEE Trans. On Microwave Theory and Techniques, vol. 17, Dec 1969, pp. 1087-1090

[4] E. da Silva, 'High frequency and microwave engineering' 1st edition, Newnes, 2001, pp.65

[5] R. E. Stegens and D. N. Alliss, 'Coplanar Microwave Integrated Circuit for Integrated Subsystems', Microwave Sys. News Comm. Tech., vol. 17, no. 11, Oct 1987, pp. 84-96

[6] J. Browne, 'Broadband Amp Drops through Noise Floor', Microwaves RF, vol. 31, no. 2, Feb 1992, pp. 141-144

[7]Anh-Vu H. Pham, Morgan J. Chen, Kunia Aihara, 'LCP for Microwave Packages and Modules' Cambridge University Press, 2012, pp.11

[8] K. C. Gupta, R. Garg, and I. J. Bahl, "Microstrip lines and slotlines," Norwood, MA, Artech House, 1979, pp.417

[9] D. M. Pozar, *Microwave Engineering*, New York, MA : John Wiley and Sons Ltd, 4nd edition, 2012, pp. 48-51

[10]B C. Wadell, 'Transmission line Design Handbook', *Artech house, Canton Street*, 1991, pp. 9-14

[11] K. C. Gupta, R. Garg, and I. J. Bahl, "Microstrip lines and slotlines," Norwood, MA, Artech House, 1979, pp.422

[12] M. Tsuji, H. Shigesawa, and A. A. Oliner, "New coplanar leakage behaviour on coplanar waveguides of finite and infinite widths," IEEE MR., vol. 39, No. 12, December 1991, pp. 2130-2237

[13]S Alexandrou, "The bent coplanar waveguide at sub-terahertz frequencies", PhD thesis, University of Rochester, 1994, pp.39

[14] M. Radmanesh, 'RF &Microwave Design Essentials: Engineering Design and analysis from DC to microwaves', Author House, 2007, pp.361-363

[15]Annapurna Das, Sisir K. Das, 'Microwave engineering' 2nd edition, Tata McGraw-Hill, 2009, pp. 507

[16]Y.-K. S. Ru-Yuan Yang, Cheng-Yuan Hung and and H.-W. W. Min-Hang Weng, ' Loss characteristics of silicon substrate with different resistivities' Microw. Opt. Technol. Lett., vol. 48, no. 9, 2006, pp. 1773–1776,

[17]S. Zaage and E. Groteluschen, "Characterization of the broadband transmission behavior of interconnections on silicon substrates," IEEE Trans. components, hybrids, Manuf. Technol., vol. 16, no. 7, 1993, pp. 686–691

[18]W. Shu, S. Shichijo, and R. M. Henderson, "Loss mechanism and high-low doping profile effects of silicon substrate with different resistivities at high frequency," in IEEE MTT-S International Microwave Symposium Digest, 2013, pp. 13–16

[19]H. Zou, H. Zhang, C. Song, H. Wang, and P. Wang, "Characterisation and modelling of mitered coplanar waveguide bends on silicon substrate," Int. J. Electron., vol. 97, no. 6, 2010, pp. 715–727

[20]H. Kim and R. Franklin-Drayton, "Wire-bond free technique for right-angle coplanar waveguide bend structures," IEEE Trans. Microw. Theory Tech., vol. 57, no. 2, 2009, pp. 442–448

[21]S. Alexandrou, R. Sobolewski, and T. Y. Hsiang, "Time-domain characterization of bent coplanar waveguides," IEEE J. Quantum Electron., vol. 28, no. 10, 1992, pp. 2325–2332

[22]A. A. Omar, Y. L. Chow, L. Roy, and M. G. Stubbs, "Effects of air-bridges and mitering on coplanar waveguide 90° bends: theory and experiment," IEEE MTT-S Int. Microw. Symp. Dig., vol. 2, 1993, pp. 823–826

[23]K. Beilenhoff, "The scattering effects of air bridges as used in coplanar MMI Cs," 2000 30th Eur. Microw. Conf. EuMC 2000, vol. 33, 2000, pp. 1–4

[24]C. C. Chen, S. Y. Chen, and Y. T. Cheng, "A patterned dielectric support process for high performance passive fabrication," IEEE Microw. Wirel. Components Lett, vol. 18, no. 2, 2008, pp. 82–84

[25]H-T Kim, S Jung, J-H Park, C-W Baek, Y-K Kim and Y Kwon, "A New Micromachined Overlap Cpw Structure With Low Attenuation Over Wide Impedance Ranges," Microw. Symp. Dig. 2000 IEEE MTT-S Int., vol. 1, 2000, pp. 299 – 302

[26]S. Seki and H. Hasegawa, “Cross-tie slow-wave coplanar waveguide on semi-insulating GaAs substrates,” Electron. Lett., vol. 17, no. 25, 1981, pp. 940–941

[27]A. L. Franc, E. Pistono, G. Meunier, D. Gloria, and P. Ferrari, “A lossy circuit model based on physical interpretation for integrated shielded slow-wave CMOS coplanar waveguide structures,” IEEE Trans. Microw. Theory Tech., vol. 61, no. 2, 2013, pp. 754–763

[28]X. L. Tang, A. L. Franc, E. Pistono, A. Siligaris, P. Vincent, P. Ferrari, and J. M. Fournier, “Performance improvement versus CPW and loss distribution analysis of slow-wave CPW in 65 nm HR-SOI CMOS technology,” IEEE Trans. Electron Devices, vol. 59, no. 5, 2012, pp. 1279–1285

[29]H. Y. Cho, T. J. Yeh, S. Liu, and C. Y. Wu, “High-performance slow-wave transmission lines with optimized slot-type floating shields,” IEEE Trans. Electron Devices, vol. 56, no. 8, 2009, pp. 1705–1711

[30]T. S. D. Cheung, “Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits,” IEEE J. Solid-State Circuits, vol. 41, no. 5, 2006, pp. 1183–1200

[31] David Patel, Samir Ghosh, Mathieu Chagnon, Alireza Samani, Venkat Veerasubramanian, Mohamed Osman, and David V. Plant, “Design, analysis, and transmission system performance of a 41 GHz silicon photonic modulator” , Optics Express, vol. 23, No. 11, 1 Jun 2015, pp. 14263-14287

[32] Wadell, Brian C. "Transmission Line Design Handbook" Artech House, 1991, pp. 294-296

[33] Janusz A. Dobrowolski, “Microwave network design using the scattering matrix”, Artech house, 2010, pp.96-99

[34] Matthew M. Radmanesh, “RF & Microwave Design Essentials: Engineering Design and Analysis from DC to Microwaves” Author House, 2007, pp.355

[35] Rainee N Simons, “Coplanar Waveguide Circuits, Components and Systems”, John Wiley & Sons, 7 Apr 2004, pp.254

[36] Rainee N Simons et al. “Channelized coplanar waveguide: discontinuities, junctions, and propagation characteristics,” IEEE MTT-S symposium digest, 1989, pp.915-918

[37] D. M. Pozar, *Microwave Engineering*, New York, MA : John Wiley and Sons Ltd, 4nd edition, 2012, pp. 10

[38] Thomas H. Lee, “Planar Microwave Engineering” Cambridge University Press, 2004, pp.137

[39] Ingo Wolff, “Coplanar Microwave Integrated Circuits”, John Wiley & Sons, Inc., 2006, pp.190

[40] Hao Xu, Xianyao Li, Xi Xiao, Peiji Zhou, Zhiyong Li, Jinzhong Yu, and Yude Yu, “High-speed silicon modulator with band equalization”, Optical letters, Vol. 39, No. 16, August 15 2014, pp. 4839- 4842

[41] M Hein, “High-temperature superconductor thin films at microwave frequencies”, Springer Tracts in modern physics, 1999, pp.269

[42] Thomas H. Lee, “Planar Microwave Engineering” Cambridge University Press, 2004, pp.123

Chapter 4: ELECTRODE DESIGN

A simulator provides an aid to understand and optimize the electrode design. The 2.5D simulator called Agilent's ADS (Advanced Design System) 2008 Momentum, which can accurately model the electrical behaviour of the transmission line at high frequencies, was used for this purpose. Each segment of the electrode is simulated and analysed separately. Firstly, this chapter goes through the simulation settings used which includes the port settings, meshing and sampling points. The second section covers the simulation results of the loss associated with varying dimensions and type of bends. The bends considered are straight, mitred, and rounded. The simulation results of Straight, Exponental, and Klopfenstein tapers will also be presented. The loss per millimetre of thin (w=8.4µm and g=3µm) and thick (w=60µm and g=35µm) coplanar waveguide lines will be shown. The metal stack used to form the electrodes will be discussed to find the effective electrode conductivity. Subsequently, the simulation results of the slow wave electrode structure will be shown.

4.1 Simulation Settings

Agilent's ADS simulator which uses a numerical method called the method of moments (MoM) with green's functions as the computational domain [12]. This electromagnetic (EM) solver gives solutions to Maxwell's equations. In MoM, the Maxwell equations are transformed into integral equations which are used to determine the surface current distribution of conductors and then the propagation and radiation of EM waves. Momentum simulations can be run under two settings i.e. RF mode or full mode. RF mode is a quasi-static mode employing a simplification made to Maxwell equations. Thus the frequency's impact on a transmission loss cannot be seen if RF mode is selected. Whereas, full mode (also known as microwave mode) solves full electromagnetic equations and provides more accurate results and considers radiation effects [11]. As the frequency increases, the radiation effect becomes more dominant. This effect is ignored in RF mode providing a fast simulation run time. RF mode can be used when the structure is complex and a quick simulation is required to see the response before a more detailed simulation is carried out. The structure in this work is not considerably complex therefore, the full mode setting was found to be appropriate. Due to the 2.5D nature, the current will be confined in 2 planes but fields are calculated in three dimensions. The substrate definition option on Momentum enables the designer to define the permittivity and loss tangent of the substrate. More than one layer of the substrate can be added. The bottom most layer is treated as infinite in

the lateral direction. Conductor (transmission line) characteristics can be defined as a perfect conductor with infinite conductivity or with finite conductivity by defining its impedance or sigma, however, other variables that vary with the method of fabrication, such as conductor roughness, cannot be incorporated into the simulations.

The simulations reflect effects such as radiation and coupling but they do not include fringing effects [12]. The simulation results are presented in terms of S parameters. The Momentum simulator also gives an option to visualize animations of the structure's surface current at different phases and frequencies whereas other 3D software usually allow the user to view electrical and magnetic fields. Momentum does 2D cell meshing whereas 3D simulators provide volume meshing.

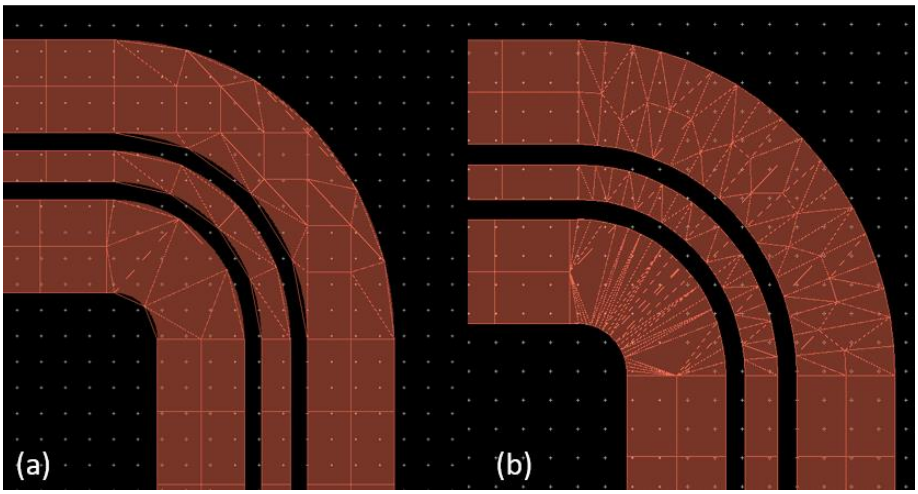


Figure 4-1– (a) arch facet angle of 45 degrees (b) arch facet angle of 5 degrees

The meshing can separately be defined at angular surfaces. This is refered in momentum as arch facet angle. Figure 4.1 (a) shows an arch facet angle of 45 degrees while in (b) it is set to 5 degrees. The resolution is improved when the angle is decreased. The arch facet angle was set to 5 degrees for the simulation and was found to be suitable due to the curvatures in the designs.

Since much of the current travels at the edges, edge meshing refines the mesh without the need to increase cells/wavelength. If the option of edge mesh has been activated then the software will automatically create a denser mesh at the edges. This feature enables to give more accurate results with reduced simulation time. The mesh is based on cells/wavelength thus a single frequency needs to be specified for the mesh settings. The mesh frequency was chosen to be 40GHz.

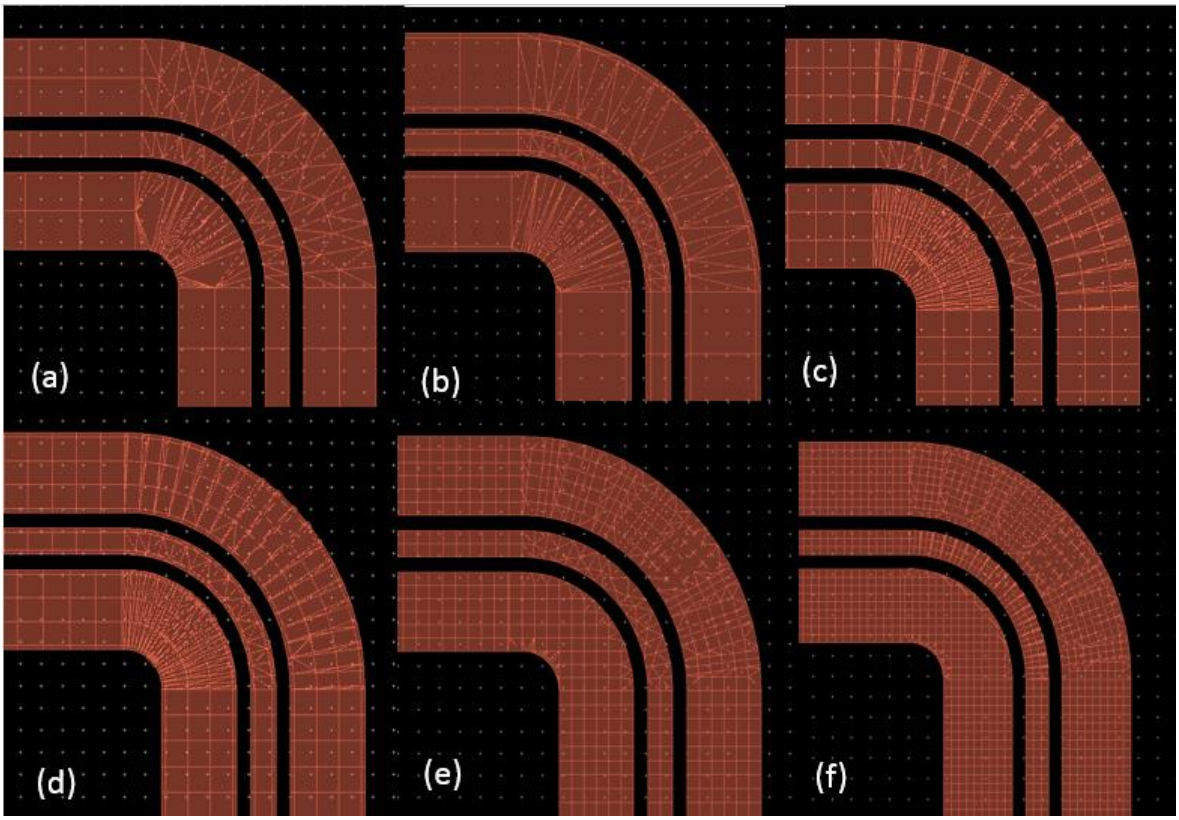


Figure 4-2–different mesh settings: (a) 20cells/wavelength (b) 20cells/wavelength with etch mesh (c) 50cells/wavelength (d) 50cells/wavelength with edge mesh (e) 100cells/wavelength (f) 150cells/wavelength

Figure 4.2 shows different mesh settings where (a) represents 20cells/wavelength, (b) 20cells/wavelength with edge mesh, (c) 50cells/wavelength, (d) 50 cells/wavelength with edge mesh, (e) 100cells/wavelength, and (f) 150cells/wavelength. As the number of cells per wavelength is increased the mesh gets denser, this increases the accuracy of simulation but the simulation time also increases. Therefore the mesh is increased until the results converge to the same value and does not show any change. This helps in maintaining the accuracy while reducing the simulation time.

There are two ways of defining the coplanar line(s) using Momentum in which either the drawn structure is treated as the metallization layer or the drawn layers are treated as gaps between signal line and the ground plane. Therefore, the metal layer is either defined as a strip or a slot. In strip the drawn objects are conductive/metal layers (Figure 4.3 (a)) whereas in slot everything from port to port is conductive except the drawn objects (Figure 4.3 (b)). Single mode is applied to strip and ground references are defined and associated with single modes on the same plane (Figure 4.3(a)). In the case of slot, ports are defined as coplanar with the same potential but reverse polarity. Under the slot settings, the ground plane will be treated as infinite and the

conductor is treated as a perfect conductor, whereas the strip setting gives an option to define metal conductivity as well as to define the finite width of the ground plane.

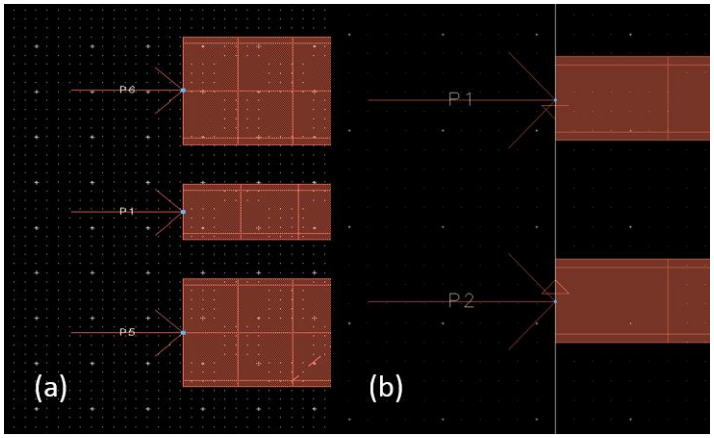


Figure 4-3– (a) single mode port (b) coplanar port

In order to draw a comparison the same coplanar line was simulated under both configurations and the simulated results are shown in figure 4.4. The coplanar port under the slot metal setting shows much lower loss due to treating the ground plane to be infinite and the perfect conductivity of the coplanar line and single mode port (figure4.3(a)) shows higher loss as this takes finite conductivity and ground plane into account which is close to real case. The strip metal setting is therefore found to be more accurate since ground plane's dimension is defined and finite. Hence, single mode port is used throughout the work to increase the accuracy of the simulation.

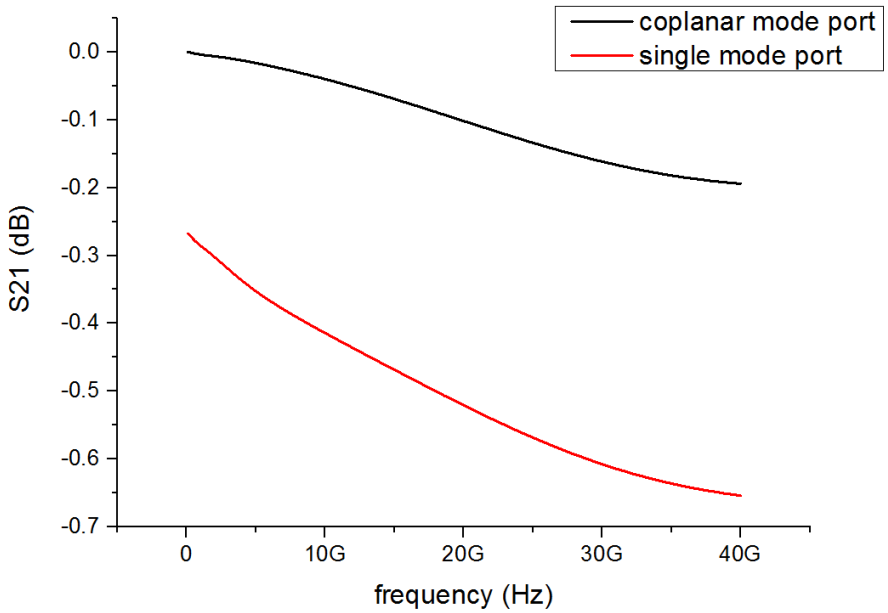


Figure 4-4–Simulation result of coplanar line using two different port settings

Once the density of the mesh and port type is selected then the number of frequency points for the simulation is required. The solution of the structure can be found at a single frequency or at multiple frequencies. The frequency range is defined as well and the number of frequency points for sampling. Momentum also gives an option of sweep types which are adaptive, logarithmic, linear or single point. The adaptive sweep is usually the preferred type over a wide frequency range as it is a fast and accurate. This is because sampled points are compared with a rational fit and when convergence is achieved the simulation is completed. In the adaptive sweep, the limit of the number of sample point is specified. This will dictate the maximum number of sampling points. Hence, for most simulations in this work, the adaptive sweep was used while the number of points was restricted to 200 points for the frequency range 100MHz- 40GHz in order to get sufficient accuracy whilst maintaining an acceptable simulation time. 200 points for the frequency range 100MHz- 40GHz means each sample point will be taken with the interval of 200MHz (5 sampling points for every GHz).

4.2 Bends

A limitation of the testing setup is that the optical fibre carrying light must not be in the vicinity of the probes for the electrical signal. Consequently the light waveguide cannot always be parallel to the coplanar waveguide. Further to this when optical modulators are typically packaged, the RF ports are required to be at the sides of the die (orthogonal to the optical input/output) and therefore a bend in the coplanar waveguide is required. When the travelling wave comes across the bend, the existing mode can be distorted and other modes can be generated due to the path difference between two grounds on either side of the signal track. Since a bend is a discontinuity of the transmission line it can cause loss in the transmitted signal. Watson et al. [13] have looked at using an air bridge to connect the two grounds together before and after the bend so that it does not see any path difference. But the design modification of Watson et al. [13] requires additional fabrication processing and adds unwanted capacitance. In this work other means to reduce the loss, such as the use of mitred bends, rounded bends and conventional square bends are considered. The slot line mode is generated due the to the path length difference of the gaps [5]. To reduce the capacitance and hence the current accumulation at the bend, the signal line can be chamfered at the corner which is known as a mitred bend (refer to figure 4.5). Rounded bends will create a smooth transition at the bend, which will insure current accumulation at the bend is minimized. RF loss due to the bend is seen as unavoidable but the aim is to make the bend loss

insignificant. A test structure comprising different numbers of bends can be compared with a straight coplanar line of equal lengths to determine loss per bend.

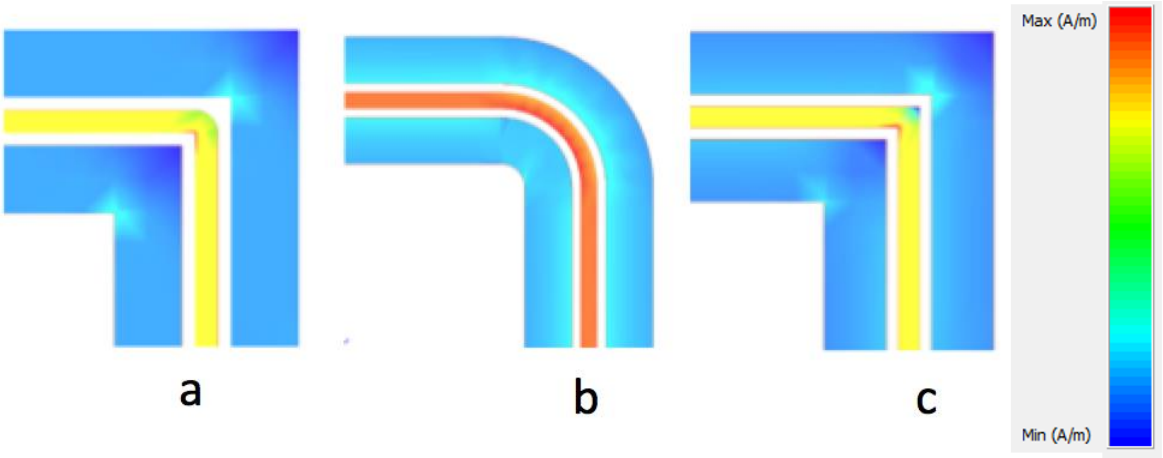


Figure 4-5– Simulated current visualization of different bends (a: mitred bend, b: round bend, c: square bend)

Simulations were carried out on two types of coplanar lines with bends; one that could directly be probed by 100µm pitch microwave probes (referred in the text as the thick bend) and the other to match electrode dimensions of the modulator (referred in the text as the thin bend). The bends were compared with one another and with the straight line of equivalent length. The mask design for the thick bend is shown in figure 4.6.

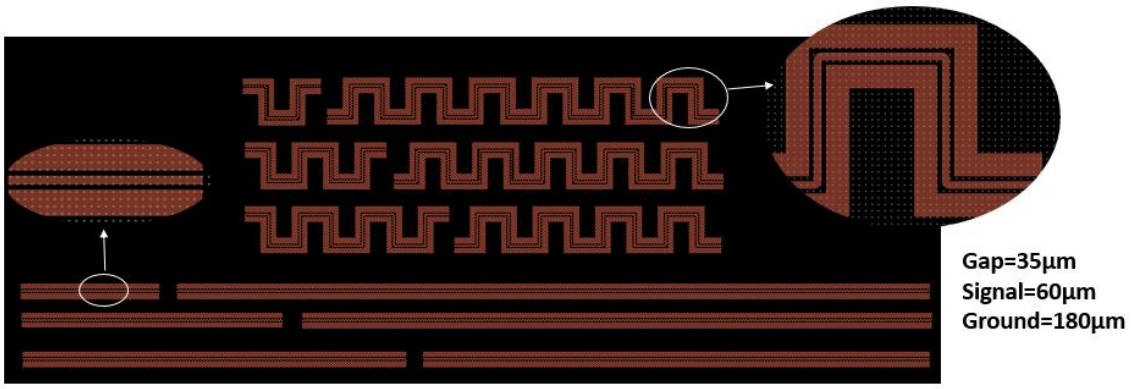


Figure 4-6– Mask for thick bend comparison

The simulation results for the thick bends are shown in figure 4.7 for the three different types of bends. Figure 4.7 shows 8 mitred bends, 12 round bends and 20 square bends with equivalent straight coplanar lines labelled as 8 mitred bends straight, 12 round bends straight and 20 square

bend straight respectivily. Different number of bends was used so all the simulated results could be illustrated in the same graph. It can be seen, there is virtually no loss due to thick bends when compared with the equivalent straight coplanar line, regardless of the type of bend used.

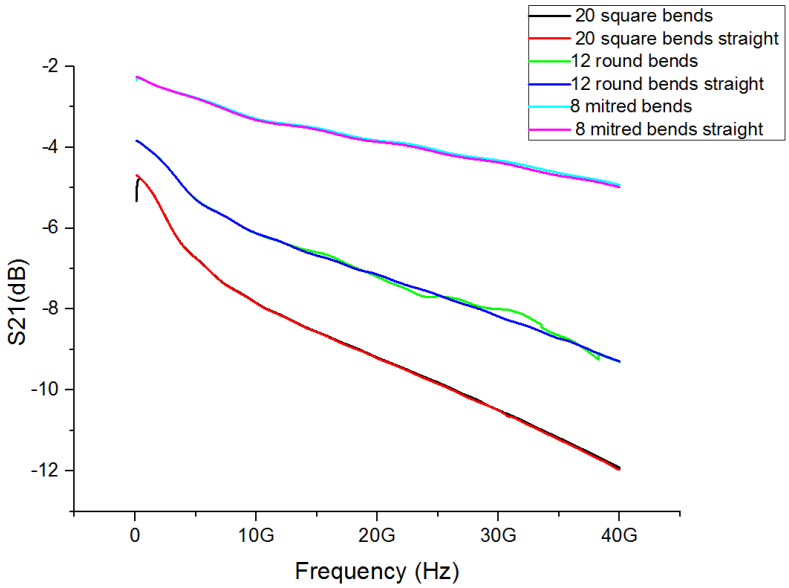


Figure 4-7– Simulation bend results for thick bends

The thin bends were also considered but the taper was required which facilitates the measurement using GSG100 probes. Figure 4.8 shows the mask design for the thin bends and comparable straight lines with tapers and probing pads added to both. 6 different numbers of bends were added for each bend type along with the equivalent length of straight line.

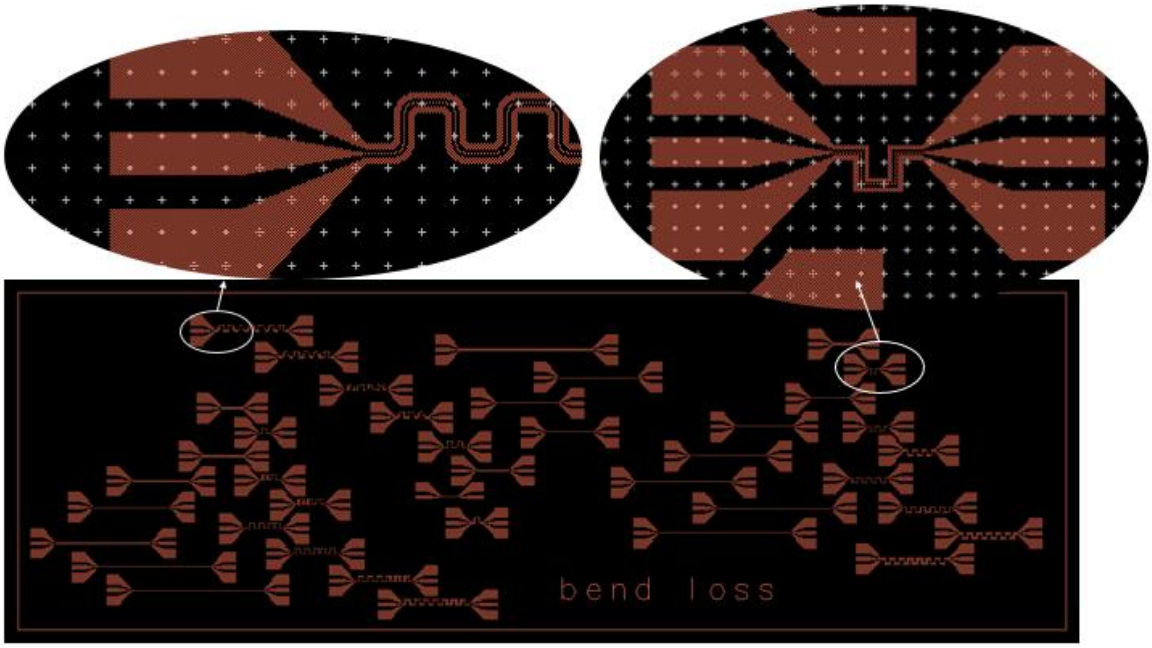


Figure 4-8– Mask for thin bend

Table 4.1 summarises the simulation results of thin bends at 40GHz compared to straight coplanar lines. The transmission loss for the rounded thin line is equal to -15.7dB which is the highest among all three bend types and significantly higher when compared to straight thin lines. The mitred thin bend simulation results show the least loss compared to other bends and the loss is close to negliable when compared with the straight lines. Simulated current visualization shown in figure 4.5b indicates high surface current density in the rounded bend of coplanar line which means higher energy will be lost as radiation.

Table 4.1– Simulation results for 3 thin bends and straight thin line

Type	**S21 (dB)**	**S11 (dB)**
Straight thin line	-8.3	-8
Mitred thin bend	-8.5	-7.8
Rounded thin bend	-15.7	-6
Square thin bend	-10.2	-6.8

From the simulation results, it can be concluded that there is virtually no loss added due to the thick bend. The lowest loss for the thin line was observed for the mitred bend (0.2dB at 40GHz). Therefore, if the design permits, the simulations suggest that it is better to form the bend in the thick CPW however the footprint will be larger. Larger footprint will increase the total insertation

loss per unit length whereas the thin line will give significantly less loss per unit length. Four thick bend requires the length of 4370µm whereas four thin bend requires the length of only 330µm. Considering these two factors in mind, it may be better to use mitred thin bend. Nevertheless, to fully understand the behaviour of the bends of different dimensions, it is necessary to carry experimental work on both.

4.3 Taper

The conventional tapers used at microwave frequencies are designed for matching two microstrip transmission lines with two different impedances to give minimal reflection loss for the specified frequency range. This is known as an impedance transformer [6]. When designing the traditional mircostrip taper the length of the taper plays an important role and the length of the taper is usually taken to be between a quarter and a half of the wavelength [8]. For this project, a coplanar taper is needed as a transition between the thick coplanar waveguide dimensions used to probe the device, down to the smaller thin coplanar waveguide dimensions required in the modulator section for biasing the PN junction. The aim is for the impedance to be kept the same throughout the taper length and to therefore minimise reflections. The modulator footprint is on the order of a millimetre and therefore it is important that the taper length does not exceed few hundred (100-250) micrometres. The taper types considered for this project were straight, exponential and Klopfenstein tapers. Test structures consisted of transmission lines with different numbers of tapers and these were compared with a straight coplanar line of equivalent length. The current densities, transmission losses and reflection losses were analysed at 40GHz.

Design of Straight Taper

A straight taper with length of 195µm was chosen to provide a smooth transition to the thin line. As the taper becomes narrower towards the thin line the current flow becomes concentrated and can cause reflection. The current distribution for the straight taper is shown in figure 4.9. As the current becomes concentrated, some of the energy will be dissipated and some of the signal will be reflected back. This is evident from the simulation results (S21 and S11) of 30 staight tapers in a row and equivalent coplanar line shown in figures 4.10(a) and (b) .

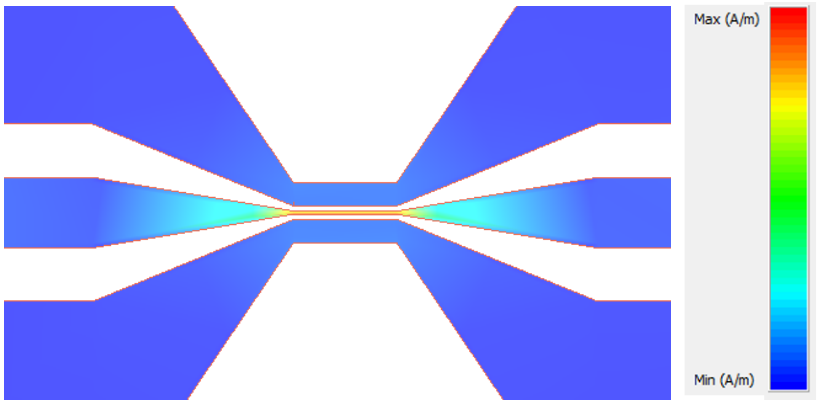


Figure 4-9– Simulated current density of the straight bend

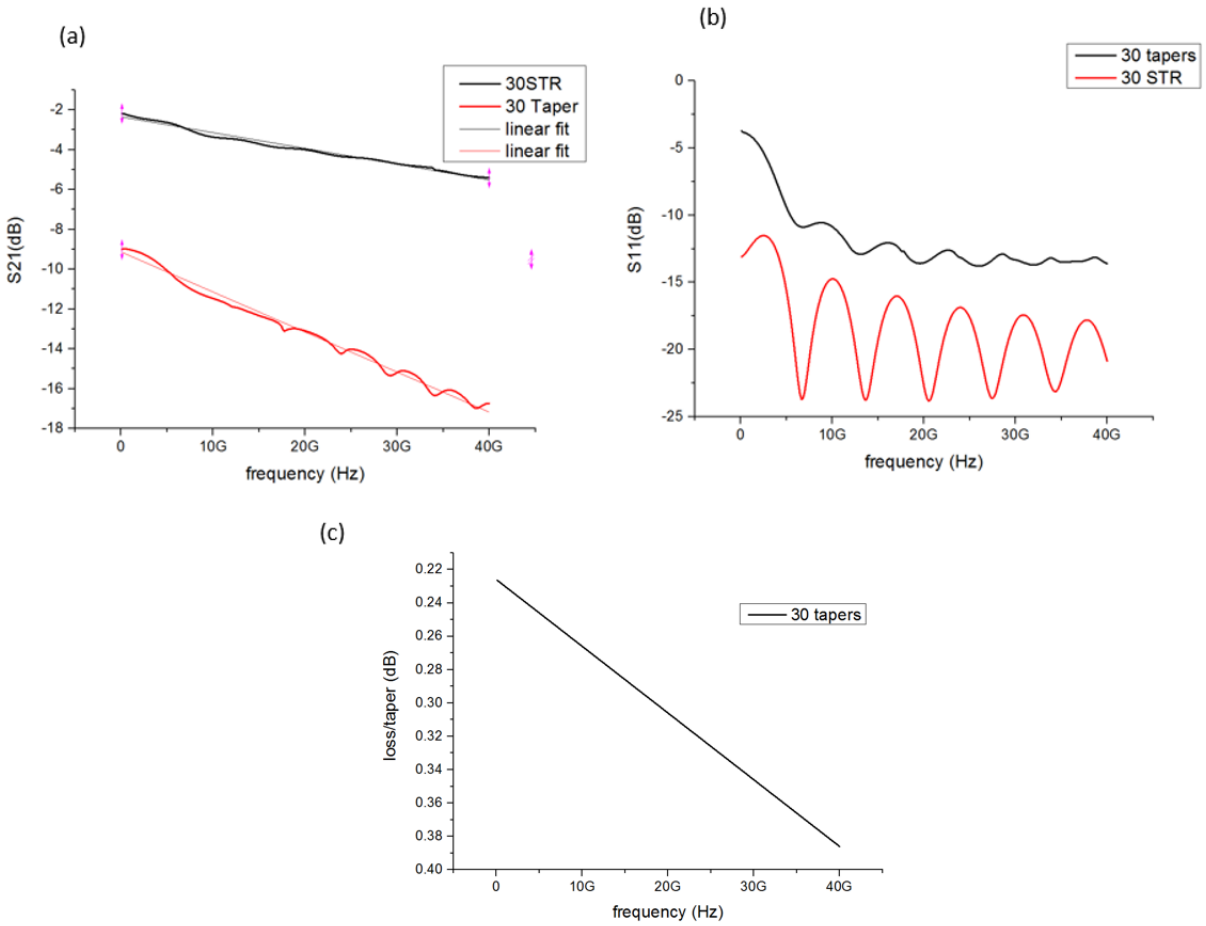


Figure 4-10– (a) S21 for 30 straight taper and 30 straight coplanar line (b) S11 for 30 straight taper and 30 straight coplanar line (c) loss per taper for straight taper

The best fit for the insertation loss (S21) was found and from this the loss per taper over the frequency range was calculated and is presented in figure 4.10(c). The graph shows a linear

increase of loss with frequency. This loss is due to the increase in dissipated energy with frequency increase.

Design of Exponential Taper

The design of the coplanar exponential taper is carried out in a similar way as is it for a microstrip exponential taper. In a microstrip, the exponential taper is used to transform from one impedence (Z_o) to another impedence (Z_L) in order to give minimum reflections [8]. The taper lengths in most cases are designed to be greater than half of the wavelength. Mathematically this is equivalent to having the product of phase shift and length equal to π (Lxβ=π). In this case, the design is limited to a 200μm length in order to keep the desired foot print of the device. Exponential taper function take the form of equation 4.1, where z is the distance away from first impedance Z_o, L represents the total length of the taper and Z is the impedence at a point [7].

$$Z(z) = Z_0 e^{\left(\frac{z}{L}.ln\left(\frac{Z_l}{Z_o}\right).z\right)} \qquad \text{Equation 4.1}$$

Exponential functions can be simplied into the equation as:

$$\ln\left(\frac{Z}{Z_o}\right) = \left(\frac{z}{L}\right)\left(ln\left(\frac{Z_L}{Z_o}\right)\right) \qquad \text{Equation 4.2}$$

When numbers are substituted into equation 4.2, then Z(z=0) =Z_o and Z(z=L) =Z_L is obtained.

Figure 4.11(a) shows a 100 μm long exponential taper where the required signal width has been calculated from equation 4.2. In figure 4.11(b), the coplanar expontential taper achieved is shown by finding the required gap to maintain characteristic impedence throughout the taper.

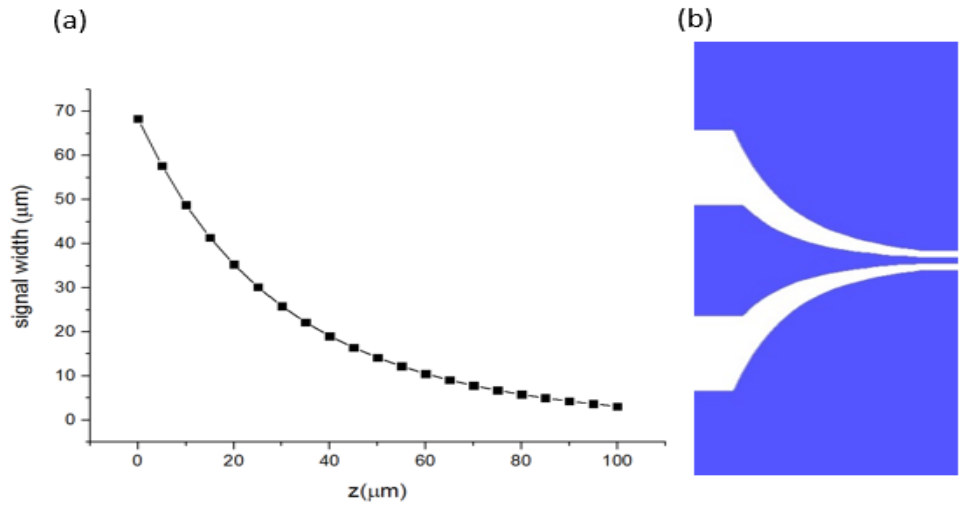


Figure 4-11– (a) shows the 20 points calculated for exponential taper with 100µm length versus signal width (b) shows final exponential taper design for coplanar line

The S parameters for a test structure with 6 exponential tapers with length equal to 200 µm and a straight coplanr line of equivalent length (2160µm) is shown in figure 4.12. These graphs show that the reflection loss (figure4.12(b)) increases the transmision loss (figure4.12(a)) due to the taper. Current density for the exponential taper was found to be similar to straight tapers (figures 4.9 and 4.15) suggesting that some signal is lost due to energy disspiation in both cases.

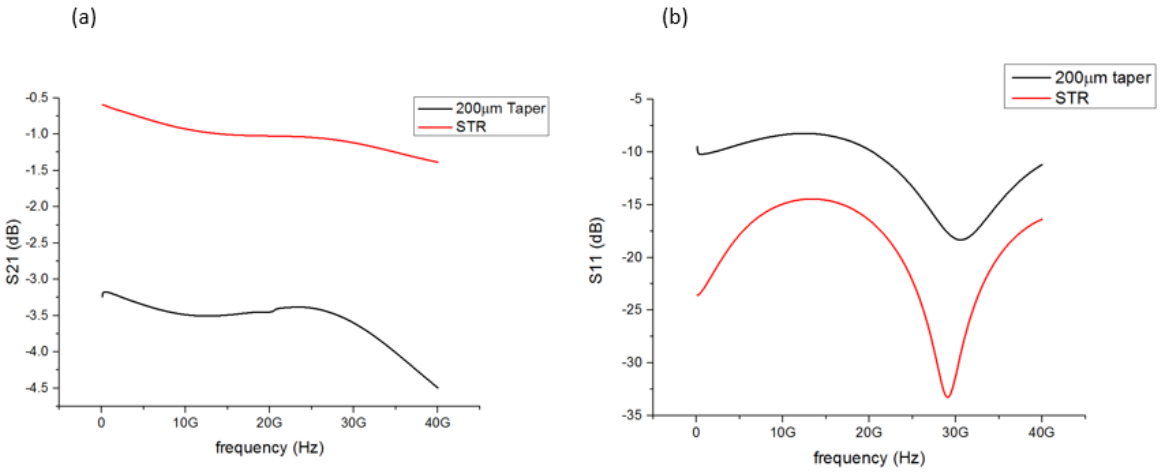


Figure 4-12– (a) S21 for 200µm taper and straight line (b) S11 for 200µm taper and straight line

A three degree polynomial fit was found for S21 (figure 4.12(a)) and the equation from polynomial has been used to determine the loss per taper which is presented in figure 4.13 along with the loss per taper for a 100µm long taper. It can be seen that 100µm long taper gives a lower loss over the required frequency band (100MHz-40GHz). The loss for the longer taper is higher as the signal

needs to propagate through longer length and the loss per length dominates over reflection loss. At higher frequencies, the loss due to reflection dominates over loss per millimetre. Thus a tradeoff needs to found between reflection loss of taper versus the attenuation of the line.

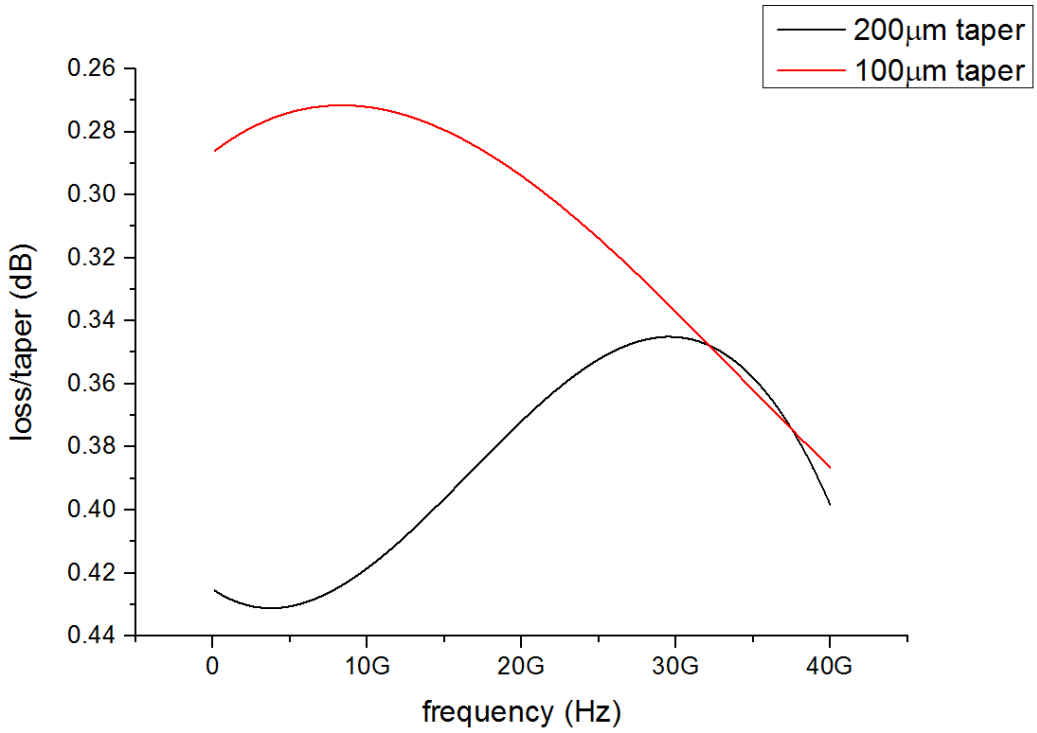


Figure 4-13– Loss per taper for 100μm and 200μm exponential taper

Design of Klopfenstein Taper

The design and simulation of the Klopfenstein taper is presented in this subsection. In 1956, Klopfenstein presented a taper, which is now widely referred to as Klopfenstein taper (K taper) [1]. The derivation of the taper is based on the Dolph-Tchebycheff transformer. It is known for giving the minimum reflection with the shortest length when compared with the other taper types [1]. The Klopfenstein taper impedance is given by equation 4.3. The derivation of this equation can be found in [1].

$$lnZ(z) = \frac{1}{2}lnZ_0Z_L + \frac{\Gamma_0}{coshA}A^2\phi\left(\frac{2z}{L} - 1, A\right) \quad for\ 0 \leq z \leq L \qquad \text{Equation 4.3}$$

Where

$$\Gamma_0 = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad \text{Equation 4.4}$$

$$A = cosh^{-1}\left(\frac{\Gamma_0}{\Gamma_m}\right) \qquad \text{Equation 4.5}$$

$$\phi(z,A) = -\phi(-z,A) = \int_0^x \frac{I_1(A\sqrt{1-y^2})}{A\sqrt{1-y^2}}\,dy \quad for\ |z| \leq 1 \qquad \text{Equation 4.6}$$

Γ_m is the maximum ripple allowed in the passband, L is the taper length, Z_0 is input impedance and Z_L is output impedance. *z* is the distance away from the taper and $\phi(z,A)$ is defined as the integral of a modified Bessel function $I_1(z)$ and the closed-form relationships are defined as:

$$\emptyset(0,A) = 0 \qquad \text{Equation 4.7}$$

$$\emptyset(z,0) = z/2 \qquad \text{Equation 4.8}$$

$$\emptyset(1,A) = \frac{\cosh(A) - 1}{A^2} \qquad \text{Equation 4.9}$$

Klopfenstein evaluated $\phi(z,A)$ numerically and presented the accurate tabulated results in a tabular form. Using the Klopfenstein tabulated results [1], the design of the taper was acheived as shown in figure 4.14 where the taper is 100µm long.

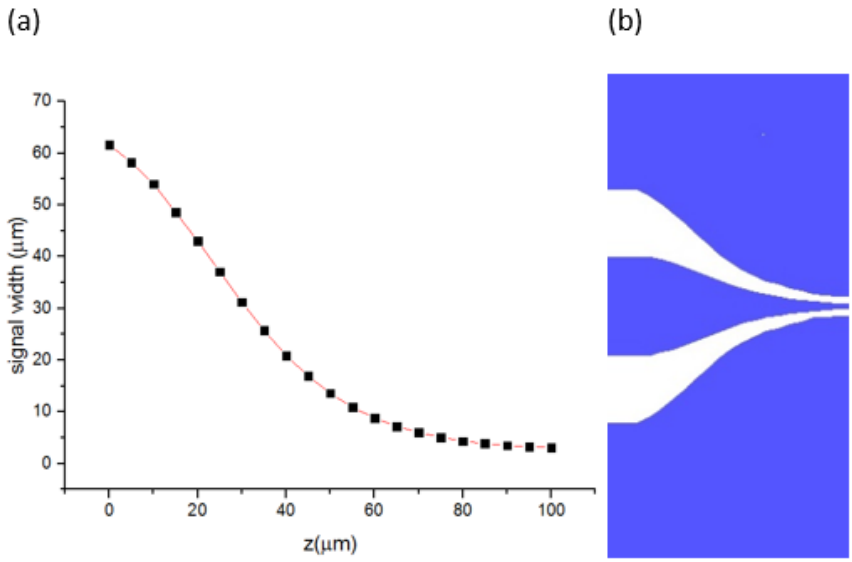


Figure 4-14– (a) shows the 20 points calculated for Klopfenstein taper with 100µm length versus signal width (b) shows final Klopfenstein taper design for coplanar line

Current densities found for 100µm length of K tapers is shown in figure 4.15. It can be noted as the taper is tapered down to the thin coplanar line, the current density increases.

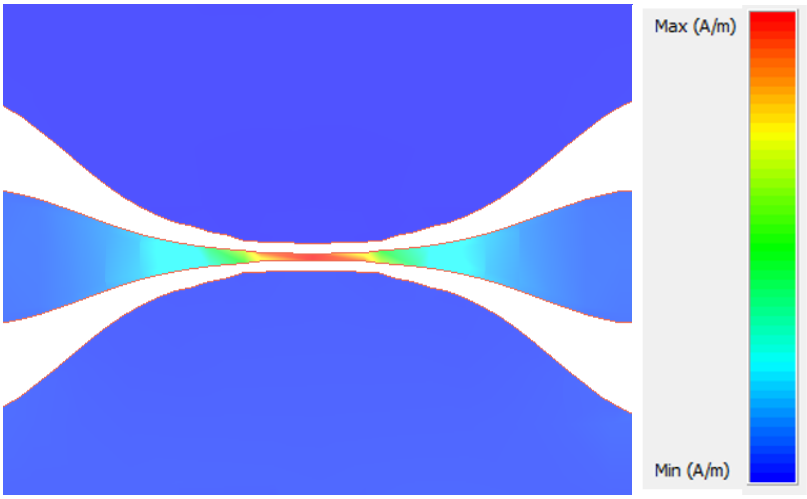


Figure 4-15– Simulated current densities for 100µm long k taper

The simulated S parameters for a test structure with fourteen 100µm long K tapers and the equivalent coplanar line length (1730µm) is shown in figure 4.16. Again, a third degree polynominal equation for S21 (figure4.16(a)) was determined and was used to calculate the loss per taper.

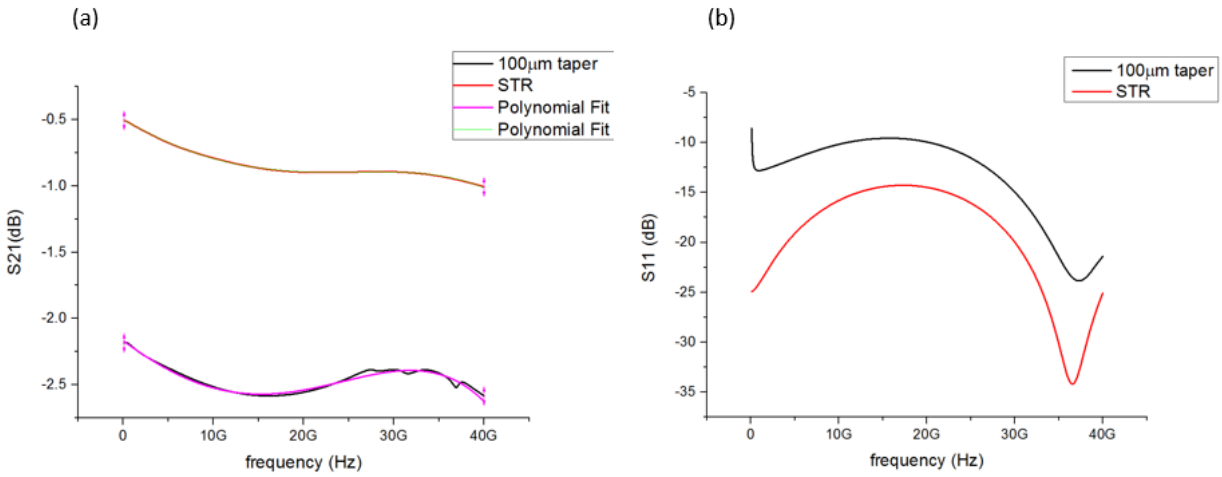


Figure 4-16– (a) simulated S21 for 100µm long K taper and coplanar line referred as STR with polynomial fit (b) simulated S11 for 100µm long K taper and coplanar line referred as STR with polynomial fit

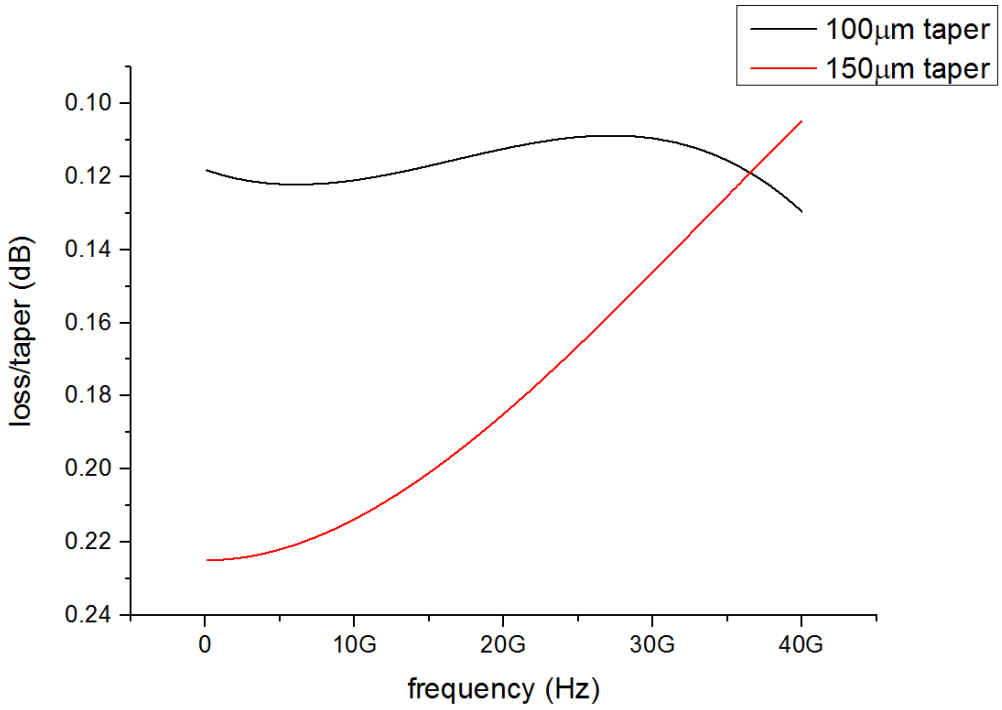


Figure 4-17—loss per taper for two different lengths of K taper

Figure 4.17 shows the loss per taper for 100µm and 150µm. The loss of the 100µm taper over the frequency range does not vary as much as the 150µm taper and is in the range of -0.12dB to -0.13dB. For the 150µm taper the loss is higher at lower frequencies and it decreases as the frequency increases.

If the direct comparison is made for simulated results was made of the same length of the taper, the K taper gave significantly lower loss per taper as opposed to the straight and exponential tapers as shown in figure 4.18. When the comparison of reflection coefficient versus frequency was made between straight (figure 4.9(b)), exponential (figure 4.11(b)) and Klopfenstein tapers (figure 4.15(b)), the best reflection coefficient was once again obtained for the K taper.

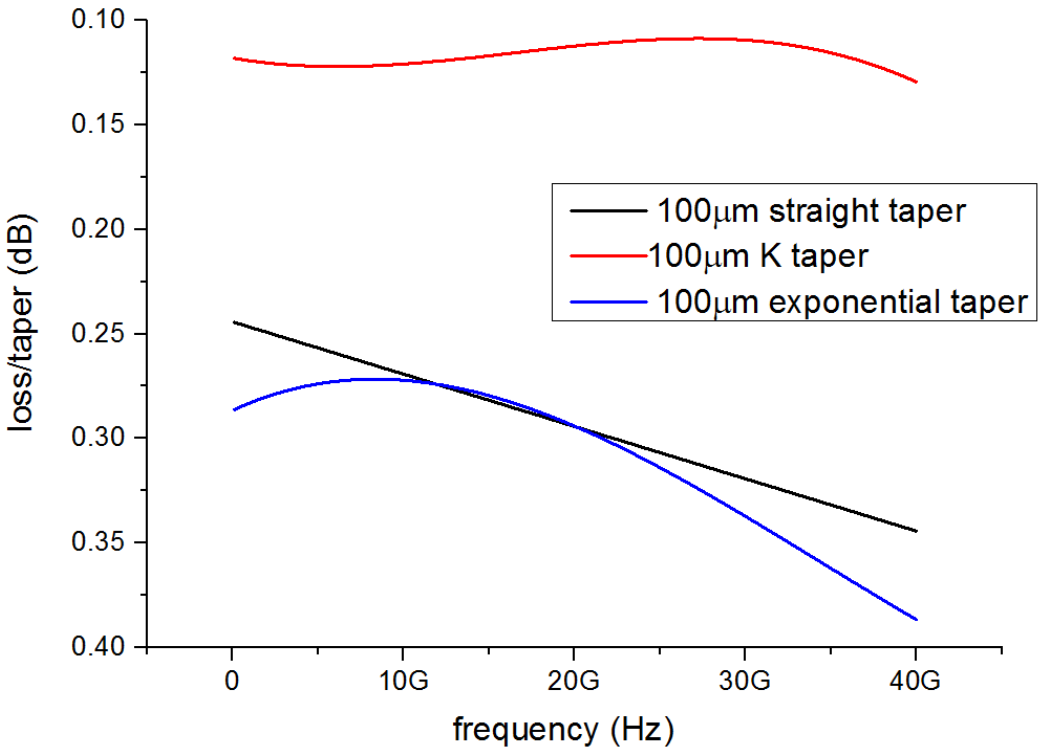


Figure 4-18– Loss per taper for the three types of the tapers

As a result of simulation for three different types of tapers. The mask designed for comparing the losses associated with different tapers was designed and is shown in figure 4.19. Where different number of tapers and its equivalent coplanar line were added.

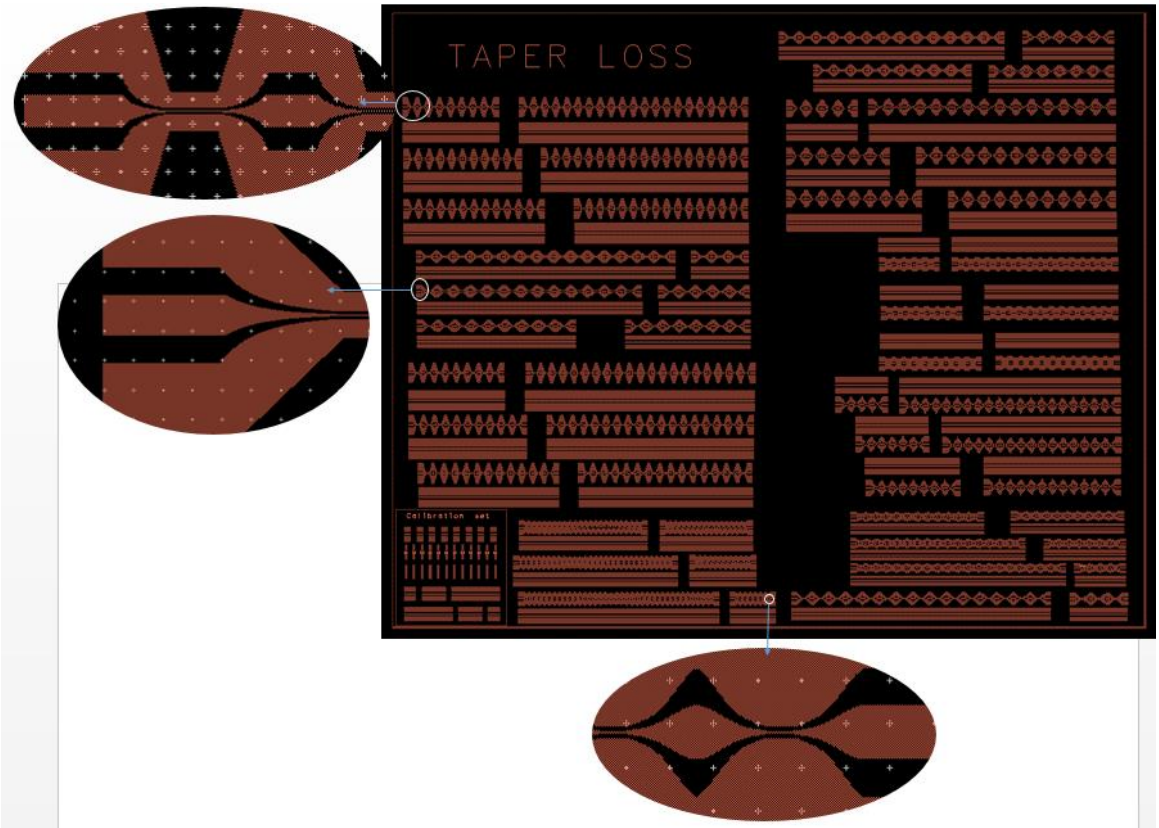


Figure 4-19– Mask design for the taper loss

4.4 Transmission line

This section will show the simulation results for thin line and the thick line as applicable to the modulator designs. The simulated results will present the loss per unit length. The thick line is used as the probing pad and the thin line is connected to the active region of the modulator (shown in figure 4.20). The signal and gap for the thin line is equal to 8.4µm and 3µm and for the thick line is equal to 60µm and 35µm respectively. These dimensions were selected to give an impedance of 50Ω and to fit the dimensions of the active region and probes respectively.

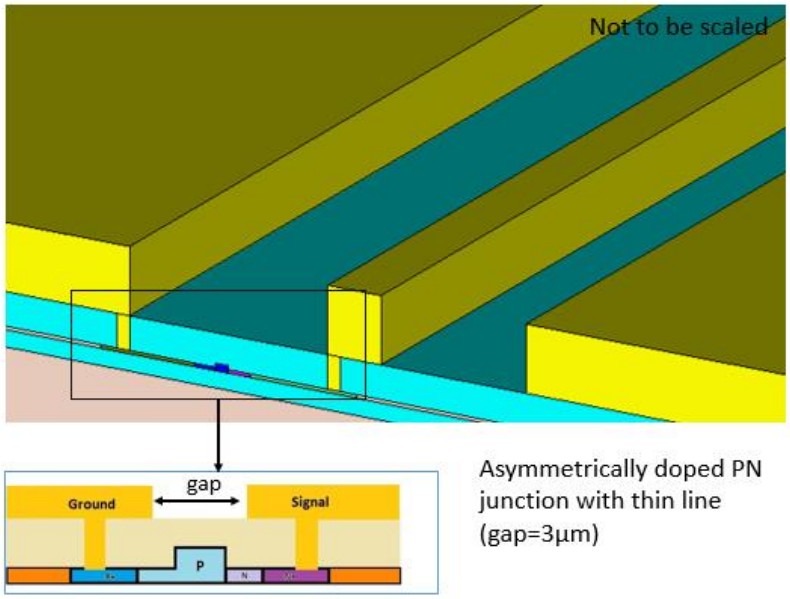


Figure 4-20–Thin line of coplanar line connected to the PN junction of the modulator [10]

In the simulations the length of the thin line and the thick line were set as 1mm. The simulation results are presented in figure 4.21. The thin line was simulated without the probing pad and the taper. The simulation results suggest that the loss due to the thin line is much higher than for the thick line. When the transmission line is thin, the loss per unit length is higher due the increase in the resistance of the line and the reflection loss also increases. The loss at 40GHz for the thick line is equal to 0.35dB whereas for the thin line, it is equal to 3.51dB. Since the length taken was equal of 1mm thus it can be concluded the loss for thick line is equal to 0.35dB/mm whereas thin line is equal to 3.51dB/mm.

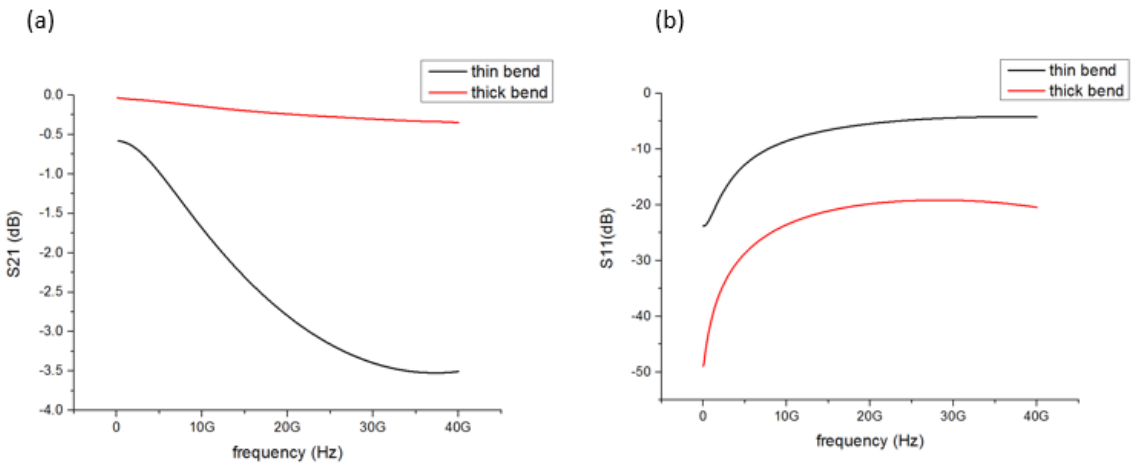


Figure 4-21– (a) transmission loss and (b) reflection loss for thin and thick line of length equal to 1mm

However, it is not possible to measure the thin line without probing pads, and tapers. Thus the simulation of the thin line with probing pads and a straight line was also simulated where the total length of the thin line is equal to 1122µm and where length of thin line itself is equal to 332µm. The thick line with total length equal to 4370µm was also simulated. The S21 results are presented in figure 4.22. Again, the thin line gives significantly higher loss compared with the thick line where the thick line is significantly longer than the thin line with probing pads.

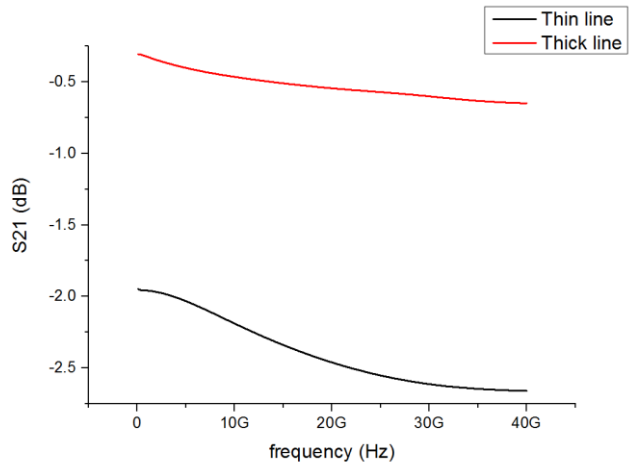


Figure 4-22–Transmission loss for thin and thick line

4.5 Electrode Design

This section will present the modulator electrode designs which are made up of bends, tapers, and sections of thin line and probe pads (thick line). All these elements were as analysed separately in earlier sections. Figure 4.23 shows the electrode design with alignment marks so the electrode could be incorporated into the modulator without any need for changing the design work of the optical side of the modulator.

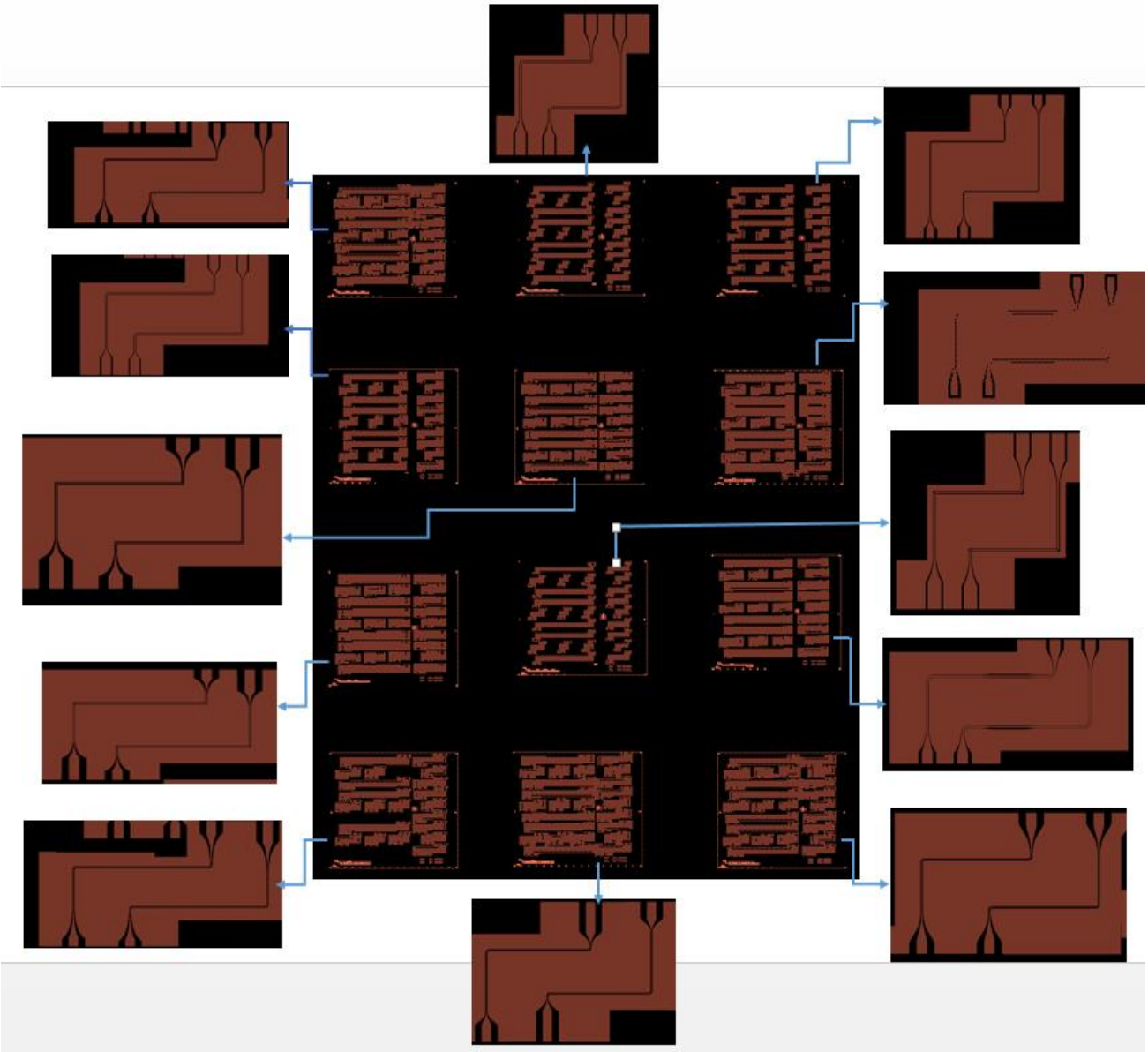


Figure 4-23– Mask design of electrodes for modulators

Figure 4.24 shows an illustration of a few complete electrode designs alongside the design of Thomson et al.[19] labelled as Ref.

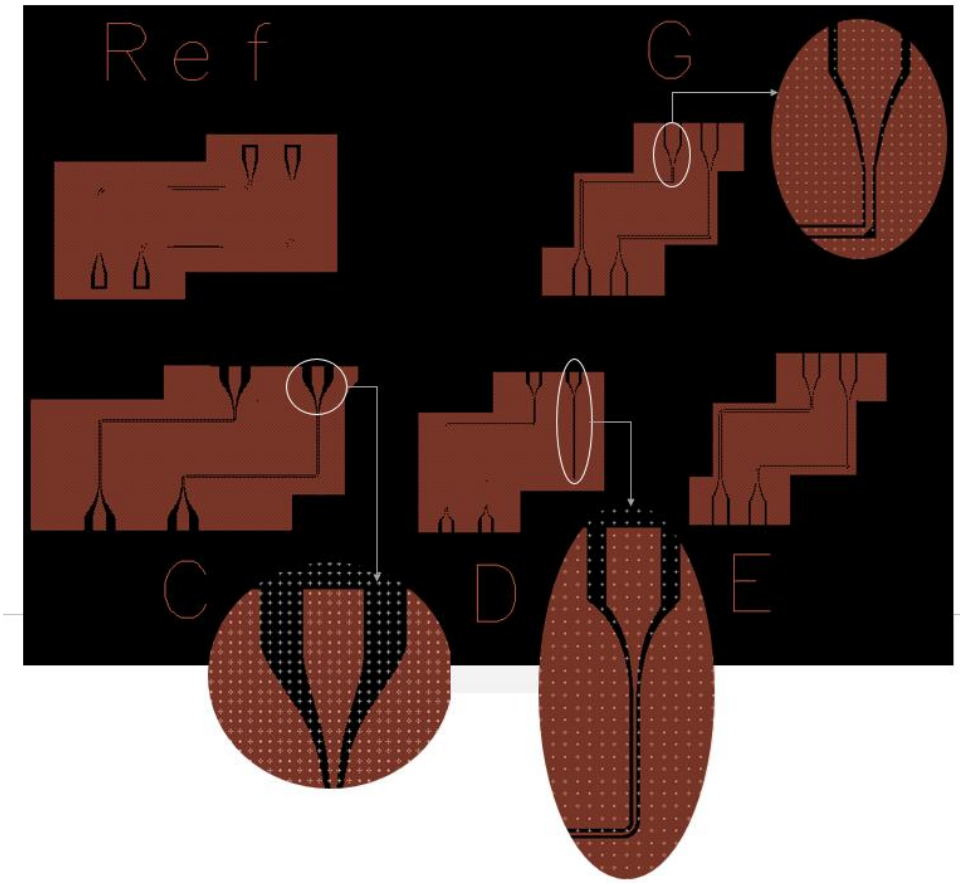


Figure 4-24–Top to bottom electrode design: Thomson et al. [19], Design G, Design C, Design D, and Design E

4.6 Transmission line

The dominating losses in a coplanar line are the dielectric and conductor losses. Both losses occur continuously along the transmission line. Therefore it is usually quoted in terms of attenuation per unit length or similar notation. Dielectric loss of the substrate also known as substrate loss becomes the dominating loss when the dielectric conductivity increases [9]. It is defined by the effective permittivity, and loss tangent (chapter 3) of a substrate.

The most dominating factors for the attenuation in this case would be dielectric/substrate loss (discussed in chapter 3) [14]. For the 'lossy' silicon substrate taking a single loss tangent is not sufficient to define the whole frequency range (for example: from 0 GHz to 40 GHz). The loss tangent increases with increasing frequency. Instead the loss tangent at different frequencies needs to be taken into consideration. Simulations were carried out using ADS 2008 (Momentum) for 1mm long electrode length. The substrate is defined as silicon (permittivity=11.7, loss

tangent=0.015) [10] with silicon dioxide on top (0.8µm thick, permittivity=3.8, loss tangent=0.001). ADS 2008 accepts one fixed loss tangent for the substrate for simulation. The loss tangent should however increase with increasing frequency. This adds one kind of uncertainty to the simulation results. The other dominating loss in CPW is the conductor loss. Conductor loss takes into account the conductor's resistivity, skin effect and surface roughness [15]. Surface roughness somewhat depends on the fabrication technique and cannot directly be accounted for in the simulations. Surface roughness, however, becomes more important as the frequency increases due to the skin effect. As the frequency increases, the current has the tendency to travel at the surface (skin) of the conductor and this phenomena is called skin effect [16]. In this case, a further complication is that the electrode is formed of a complex stack of different metals as shown in figure 4.25. This means there is a need to find the effective conductivity of the entire stack. The metal stack of the electrode was fabricated (by foundry called CEA-LETI) on silicon substrate without the device and measurements were carried out by the author to find the effective conductivity of the metal stack of total thickness 1.44µm (figure 4.25). Electrodes were fabricated on top of a 0.8µm silicon dioxide layer grown on the silicon substrate.

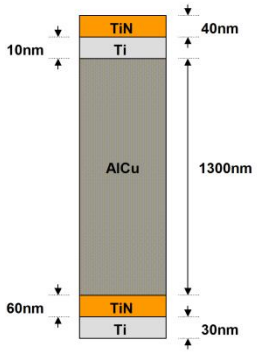


Figure 4-25– Metal stack for the electrode

The effective conductivity at DC was therefore found by applying the voltage and measuring current of two different lengths of electrodes. The calculation of effective conductivity of the metal stack changes is shown below.

For length =3.5mm, V=0.1V, I= 8 x10^{-3}A so R=12.5Ω

So for length= 3.5mm-1mm= 2.5mm Resistance= 12.5 Ω - 4Ω = 8.5 Ω

Electrode metal thickness (t) =1.3µm, width of the signal track width (W) =9.1µm

Cross-sectional Area= 1.3µm×9.1µm =1.183x10^{-11}m^2

$$R = \frac{\rho l}{A}$$ Equation 4.10

Where R= resistance, ρ = resistivity, l =length, A= Cross-sectional area=Wt

R=8.5 Ω, l=2.5mm, A= 1.183x10^{-11}m^2 so ρ= 4.0222x10^{-8} Ω·m

So conductivity (σ) = reciprocal of resistivity (1/ρ), Hence DC Conductivity = 2.5x10^7 S/m

Due to the skin effect, more current will travel on the outer most surface of the conductor especially at higher frequencies [16]. Hence, the effective conductivity will be frequency dependant, as the current overlap with the different metals in the stack will vary with frequency. It also means that the current density will increase thus converting more energy into heat, which translates into more loss at higher frequencies. The skin depth is a measure of the penetration depth of the current in the conductor. Where δ= skin depth (m) is given by:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$ Equation 4.11

μ=permeability (4π*10^{-7} H/m) note: H = Henries = Ω*s, σ= conductivity (mho/m) and mho [℧] = Siemen [S]

Using the effective conductivity found through experimental work, the skin depths at different frequencies were calculated. Figure 4.26 shows skin depth versus frequency curve as the result of the calculated values. It can be seen that as the frequency increases the current concentrates on the skin of the conductor, this validates the skin effect.

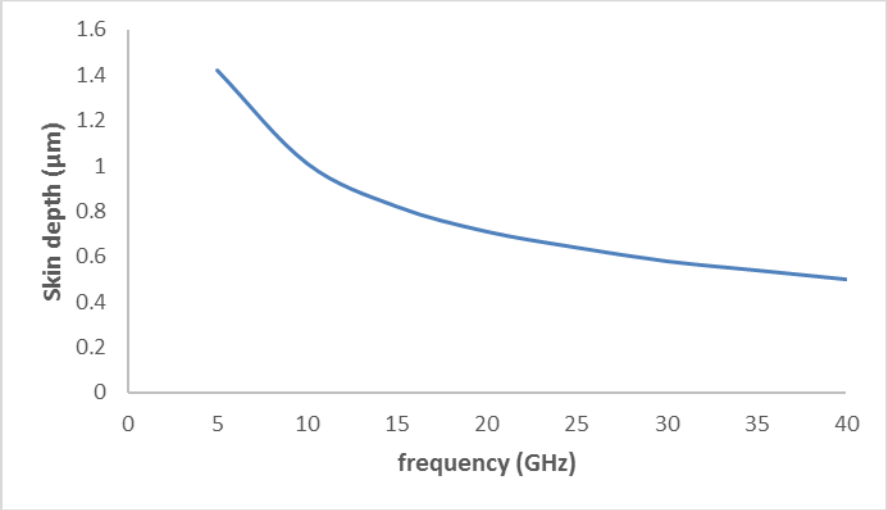


Figure 4-26– Skin Depth of effective conductivity

The electrode was then modelled using the effective conductivity at DC found experimentally. Simulation results using effective conductivity as the metal conductance and measured results are shown in figure 4.27. It can be seen that the loss is much higher than the simulated results. Hence the model needed to be further optimized.

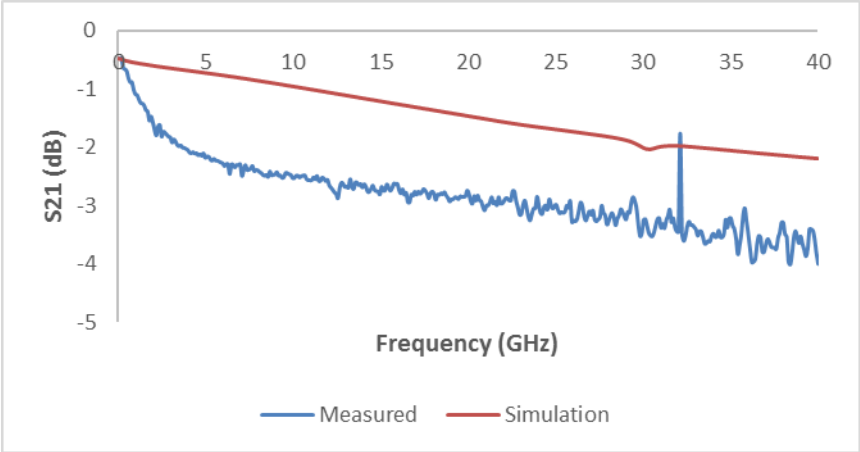


Figure 4-27– Electrode's simulation and measured using effectivity conductivity

This result (figure 4.27) shows that measured and simulated results diverge rapidly with increasing frequency. There are various reasons for this most of which have been previously mentioned. The top layer of the metal stack is formed of titanium nitride (TiN) which has a conductivity of 1.3×10^6 S/m [3]. The simulation was then carried out using the conductivity of the TiN. Figure 4.28 shows the comparison of transmission loss versus frequency between TiN conductivity, effective conductivity (measured at DC) and the measured response. The measured response gives an

exponential attenuation. This is because as the frequency increases, the current density will be more concentrated (skin effect) in TiN (has lower metal conductivity) giving higher loss.

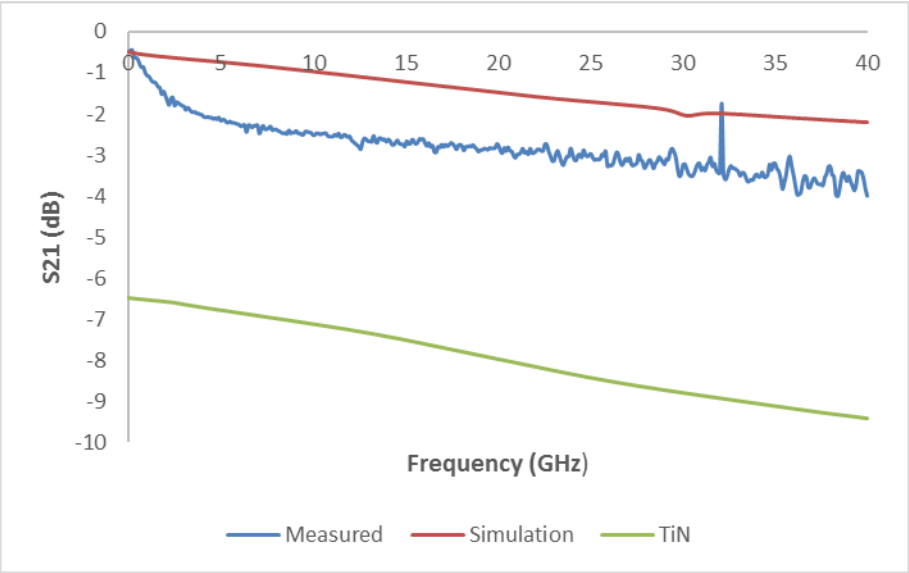


Figure 4-28– Simulated and measured response of electrode

Due to the skin effect, surface roughness affects conductivity at high frequencies and the loss tangent of the substrate changes. It is then necessary to find the effective conductivity at different frequencies. Effective conductivity can be found using ADS 2008 simulation results (refer to figure 4.29). The effective conductivity is then used in simulation of the slow wave electrode designs in order to improve the simulation accuracy. This conductivity will take the conductor losses (i.e. fabrication tolerance, skin effect, surface roughness of the conductor, conductor resistivity) into account. The effective conductivity of $5x10^{6}$S/m can be used in the simulations.

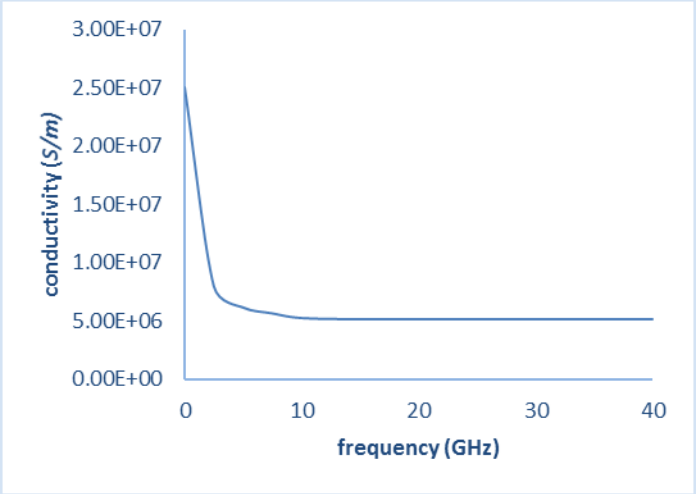


Figure 4-29–Effective conductivity variation over the frequency

4.7 Slow wave electrode

This section will present the simulation results for the slow wave electrode structure for a high speed silicon electro-optical modulator where the performance is enhanced using slow light propagation as found in [4]. The characterization of the modulator in [4] shows the bandwidth can be clearly be improved by matching the speed of electrical signal with the slow wave optical signal (section 2.2.3). Thus the velocity matching method will be presented here. The velocity of the electrical signal should be decreased which means the wavelength of wave is made smaller ($\lambda=v/f$). The velocity of the line can be varied by changing the inductance or/and capacitance of the line ($v=1/\sqrt{LC}$), from the formula, it can be appreciated, as the inductance or/and capacitance of the line is increased, the velocity of the line will be decreased. However, changing the capacitance and/or inductance of the line will also alter the impedance (Z_0) of the line. The impedance (Z_0) of the line is equal to $\sqrt{\frac{R+jwL}{G+jwC}}$ but if the inductance and capacitance ratio is kept the same while increasing the inductance and capacitance then a slow wave structure is achievable whilst keeping the impedance the same. A method involving the use of corrugated metal strips was found to be most effective way to slow down the electrical signal. This is achieved by adding a silicon dioxide layer on top of the original electrode and then adding corrugated metal strips perpendicular to the direction of the propagation on the coplanar waveguide top.

As there is a limitation of defining 3D circuits in Agilent's ADS, the PN junction (diode) has to be approximated in the model by defining the substrate conductivity. However, the effective conductivity of the diode changes with applied signal. Thus the substrate was not completely replicated during the modelling, whereas, the effective conductivity of the electrode's metal stack was analysed separately in section 4.6 and is used in these simulation to improve the accuracy. Also, as an initial simulation to design a slow wave electrode, the electrode was modelled without the discontinuities (such as bends and tapers) and the active region of the modulator was simulated to reduce the simulation complexity and time.

The electrode with additional slow wave structure was modelled and was compared to the original electrode (gap1= 4µm, gap2=7.8µm and signal=9.1µm) to see the effects on the velocity of electrical signal. The simulated slow wave structure is shown in figure 4.30. The slow wave structure consists of the original modulator electrodes (shown in grey) with a silicon dioxide layer on top (sky blue) and corrugated metal strips on top of that (shown in yellow). The idea is that the corrugated metal strips will add additional capacitance to the line and the velocity will be decreased.

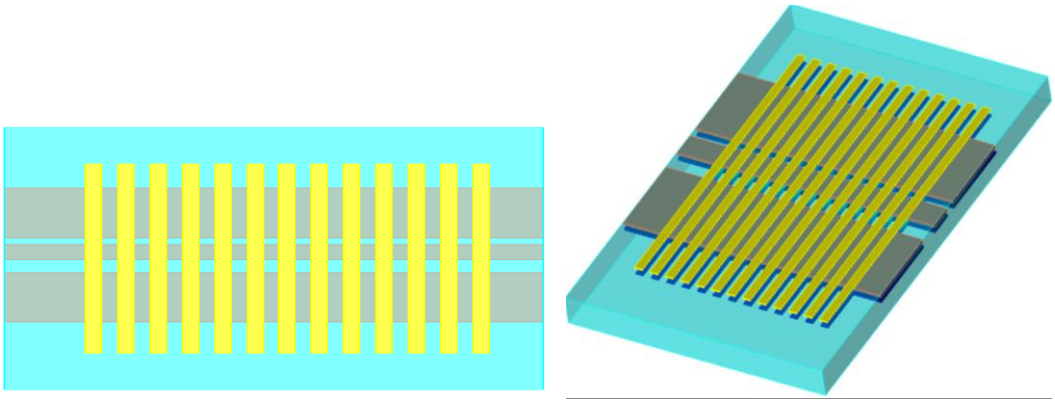


Figure 4-30– Simplified structured of electrode modelled with slow wave structure

Figure 4.31 shows the simulated current density, which indicates that an insignificant amount of the signal is coupled to the corrugated metal strips and therefore the loss contribution due to this will be insignificant.

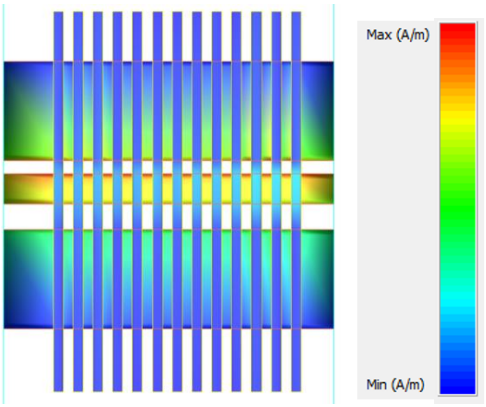


Figure 4-31– Simulated current density

Variation of period of the corrugations showed little impact on the phase shift. Figure 4.32 shows the simulation results of keeping the width of corrugated metal constant at 3µm while the gap was varied from 1µm to 5µm and the silicon dioxide layer was also kept constant at 1000nm. The simulation results confirm that the design of the corrugated metal layer gap has little impact on the results thus it is better to choose the gap, which will be easy to fabricate. Therefore the gap of 3µm was chosen.

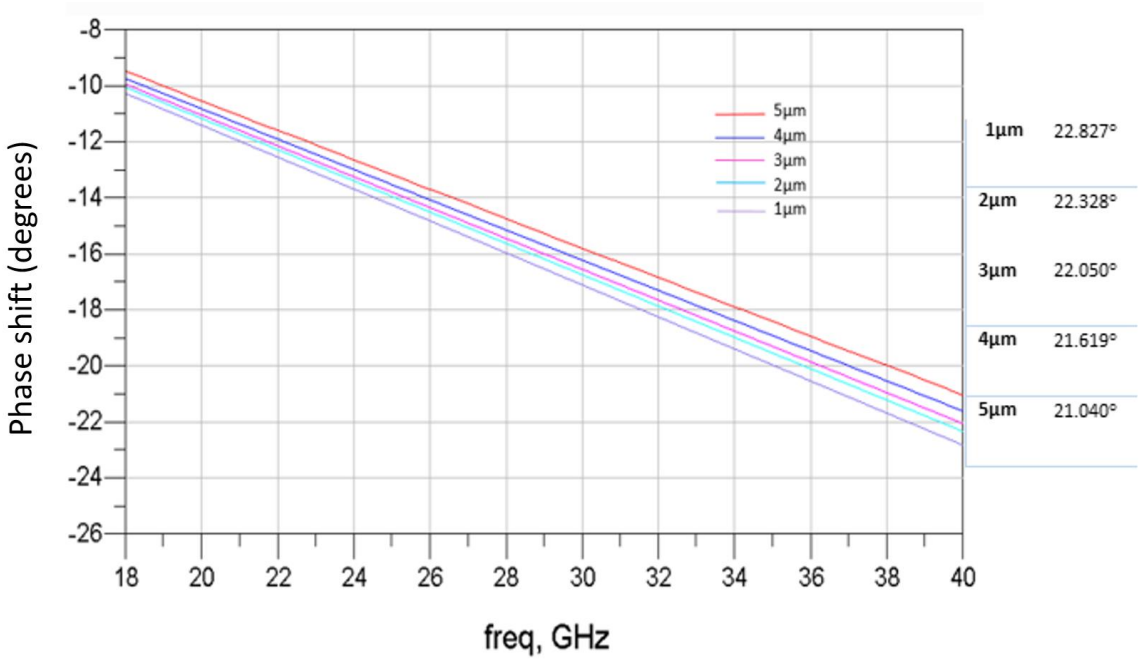


Figure 4-32– The graph shows the phase shift for different gaps of corrugated metal structure for frequency range of 18GHz- 40GHz. The table on the right shows phase shift values at 40GHz extracted from the graph

Table 4.2 summarises the simulation results obtained at 40GHz for a 200µm long line with different silicon dioxide layer thicknesses whilst keeping the corrugated metal layer constant. The corrugated metal has width of 3µm and the gap of 3µm. Varying the thickness of the silicon dioxide layer between electrode and the corrugated metal strips changes the inductance and capacitance of the electrode.

Table 4.2–Summary of simulation results for slow wave structure

	S21(dB)	**S11 (dB)**	**Phase shift (Degrees)**	**Velocity (m/s)**	**Slowing down factor**
Conventional CPW	-0.091	-16.899	17.504	1.69×10^8	-
SiO_2=0.25µm	-0.825	-7.644	49.535	0.58×10^8	2.91
SiO_2=0.3µm	-0.662	-8.525	47.035	0.6×10^8	2.82
SiO_2=0.35µm	-0.481	-9.831	43.774	0.66×10^8	2.56
SiO_2=0.4µm	-0.36	-11.042	41.21	0.7×10^8	2.41
SiO_2=0.45µm	-0.275	-12.174	39.148	0.73×10^8	2.32
SiO_2=0.5µm	-0.176	-14.093	36.231	0.79×10^8	2.14
SiO_2=0.75µm	-0.057	-19.100	31.227	0.97×10^8	1.74
SiO_2=1µm	-0.019	-23.909	21.826	1.32×10^8	1.28
SiO_2=1.25µm	-0.021	-23.422	68.38	1.33×10^8	1.27

When metal strips are added on top of the electrodes it will not only change the capacitance but also the impedance of the electrodes. If metal strips were closer to the electrode there would be more interaction between electrodes and the metal strips resulting in a larger change in impedance and capacitance. As evident from table 4.2, if the silicon dioxide layer is 0.25µm thick then the loss increases from 0.455dB/mm to 4.125dB/mm, compared to conventional CPW. The corresponding slowing down factor achieved is 2.91. With such a large electrode loss the (slow wave) modulator's bandwidth is no longer limited by the mismatch of the phase between optical and electrical waves but by the electrode transmission loss.

The impact of connecting the ground plane of the electrode to the corrugated metal strips using vias was also analysed. The simulation results obtained with vias are listed in table 4.33. via is the vertical metal which forms the contact between two metals on different metal layers. By adding a via, the corrugated metal will no longer be floating but will be connected to ground plane of the electrode.

Table 4.3— Simulation results for slow wave structure with the via

	S21(dB)	**S11 (dB)**	**Phase shift (Degrees)**	**Velocity (m/s)**	**Slowing down factor**
Conventional CPW	-0.091	-16.899	17.504	$1.69x10^8$	-
SiO_2=0.25µm	-1.167	-6.301	53.614	$0.54 x10^8$	3.13
SiO_2=0.3µm	-0.839	-7.584	49.256	$0.59 x10^8$	2.86
SiO_2=0.35µm	-0.625	-8.769	45.89	$0.63 x10^8$	2.68
SiO_2=0.4µm	-0.479	-9.864	43.225	$0.67x10^8$	2.52
SiO_2=0.45µm	-0.375	-10.882	41.07	$0.7 x10^8$	2.41
SiO_2=0.5µm	-0.299	-11.835	39.294	$0.73x10^8$	2.32
SiO_2=0.75µm	-0.117	-15.918	33.68	$0.86x10^8$	1.97
SiO_2=1µm	-0.004	-35.959	25.601	$1.12x10^8$	1.51
SiO_2=1.25µm	-0.003	-42.711	25.149	$1.15x10^8$	1.47

The summary of the simulation results with and without vias is presented as a graph in figure 4.33. The graph shows the slowing down factor versus the thickness of the silicon dioxide layer. The results suggest that the addition of the vias will not give a massive improvement in the slowing down factor but it will complicate the fabrication process. For this reason, it was decided that vias would not be used.

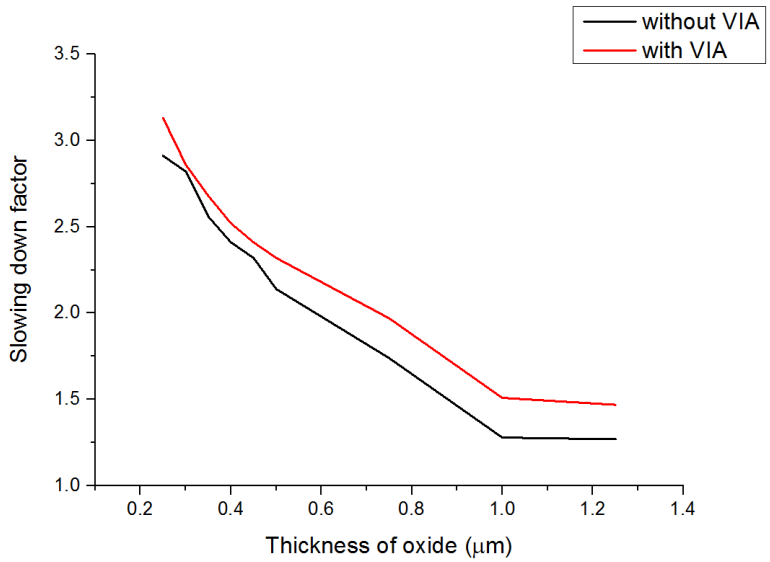


Figure 4-33– Summary of simulation results for slow wave structure

Different thicknesses of corrugated metal strip layer (for slowing down) were simulated and it was found that the thickness of the metal has most impact on phase shift of the transmission line. However, the reflection loss seems to get worse as the metal thickness is reduced. The conductivity of the metal strips was modelled as if it was to a perfect conductor. For the corrugated metal strips, 1μm thickness was found to be suitable. After 1μm thickness of the metal, the impact on reflection loss was found to be negligible.

Other dielectrics instead of silicon dioxide were also considered which have a larger permittivity (and would naturally slow the electrical wave). Table 4.4 shows simulation results obtained for BST (Barium Strontium Titanate), which has a permittivity of 500 and loss tangent of 0.03[18]. Again, the original coplanar line with total length of 200μm was simulated. The results show that the phase shift can be increased by increasing the permittivity of the dielectric material but it will also have an effect on the impedance of the line and hence an increase in loss will be seen.

Table 4.4— Table for simulation results for BST

Thickness	S21(dB)	S11(dB)	Phase (degree)	Z_0 real	Z_0 imagery
0.1	-0.048	-31.398	27.428	61.218	0.552
0.2	-0.0228	-14.917	36.558	48.431	0.659
0.3	-0.563	-10.116	44.708	41.451	0.708
0.4	-0.995	-7.519	51.722	36.891	0.737
0.5	-1.484	-5.847	57.785	33.562	0.757
0.6	-1.995	-4.710	62.961	31.046	0.771

Another design for slowing down, the electrical wave, which involves having a slotted ground plane, was also considered. Figure 4.34 shows the slotted ground plane, which gave the maximum slow down factor (1.34) for slotted ground electrodes, which is not a significant decrease in the velocity.

Figure 4-34– Slotted grounded for varying the velocity

The corrugated metal strips were found to be the most effective slow down structure shown through simulation results (table 4.2). The results also shows that the increase in impedance mismatch causes higher reflections. Further simulations were carried to see if the reflection loss can be reduced by varying the electrode design. Simulated electrode design results at 40GHz with the length of electrode equal to 100µm is presented in table 4.5. From the table, it can be noted that electrode 3 gave the slow down factor of 2.077 while the reflection loss is much lower (-33.7dB) than conventional CPW (without slow wave structure) which gave the reflection loss of -22.795dB. However, the dimensions of coplanar line are not compatible with the modulator configuration. Electrode 9 is found to be compatible with the modulator design, the transmission loss and reflection was found to be similar to the conventional CPW while a slowdown factor of 2.118 was achieved.

Table 4.5— Simulation results at 40GHz while the electrode design is varied

	Gap1 (µm)	**Signal (µm)**	**Gap2 (µm)**	**S21 (dB)**	**S11 (dB)**	**Phase shift**	**Slow down factor**
Conventional CPW	4	9.1	7.8	-0.023	-22.795	8.788	
Conventional CPW with slow wave structure (0.25µm)	4	9.1	7.8	-0.361	-10.98	28.6	3.25
Conventional CPW with slow wave structure	4	9.1	7.8	-0.077	-17.534	19.917	2.266

(0.5µm)							
Electrode 1	4	4	7.8	-0.031	-21.4	19.544	2.224
Electrode 3	6	3	9	-0.002	-33.7	18.257	2.077
Electrode 4	3	3	9	-0.007	-28.288	17.462	1.987
Electrode 5	3	5	9	-0.078	-17.488	21.293	2.423
Electrode 6	3	6	9	-0.136	-15.138	23.178	2.637
Electrode 8	3	4	9	-0.035	-21.024	19.359	2.203
Electrode 9	3	3.6	9	-0.021	-23.179	18.613	2.118

The simulation results shown in table 4.5 suggest that if the electrodes design is changed as well as adding the slowing down structure then the reflection loss can be decreases due to improved impedance matching, whilst obtaining the slowing down factor needed.

References

[1] R.W. Klopfenstein, 'A transmission line taper of improved design', proceedings of the IRE', vol 44, 1956, pp.31

[2] M.A. Grossber, "Extremely Rapid Computation of the Klopfenstein Impedence Taper, Proceeding of IEEE, vol 56, 1968, pp. 1629-1630

[3] J. F . Shackelford and W Alexander, CRC Materials Science and Engineering Handbook, Third Edition, CRC Press 2000, pp. 565

[4] Brimont et al., 'High speed silicon electro-optical modulators enhanced via slow light propagation', Optics Express, vol. 19, issue 21, 2011, pp. 20876-20885

[5] Paul M Watson and Kuldip C. Gupta, ' Design and optimization of CPW Circuits using EM-ANN Models for CPW components', IEEE Transactions on microwave theory and techniques, vol. 45 ,no.12, December 1997,pp.2515-2523

[6] R. E. Collin, 'The Optimum Tapered Transmission Line Matching Section', proceedings of the IRE, 1956, pp.539-548

[7] Masanori Kobayashi and Narutoshi Sawada,' Anlysis and synthesis of tapered microstrip transmission lines', IEEE Transactions on microwave theory and techniques, vol.40, no 8, aug 1992, pp.1642-1646

[8] T C Edwards and MB Steer, 'Foundations of interconnects and microstrip design', third edition, John Wiley & Sons Ltd, 2000, pp.435

[9] R.S. Rao, 'Microwave engineering', PHI learning private limited, 2012, pp.225

[10] Lioubtchenko D, Tretyakov S, Dudorov S., 'Millimeter-Wave Waveguides' , Kluwer Academic Publishers,2004, pp.110

[11] http://cp.literature.agilent.com/litweb/pdf/ads2008/mom/ads2008/Momentum_Basics.html accessed on 01/07/2015

[12]http://cp.literature.agilent.com/litweb/pdf/ads2008/mom/ads2008/Theory_of_Operation_for_Momentum.html accessed on 01/07/2015

[13] Watson et al. "EM-ANN modelling and optimal chamfering of 90/spl deg/ CPW bends with air-bridges", Microwave Symposium Digest, IEEE MTT-S International, vol 3, 1997, pp.1603-1606

[14]Y.-K. S. Ru-Yuan Yang, Cheng-Yuan Hung and H.-W. W. Min-Hang Weng, 'Loss characteristics of silicon substrate with different resistivities', Microw. Opt. Technol. Lett., vol. 48, no. 9, 2006, pp. 1773–1776

[15]W. Shu, S. Shichijo, and R. M. Henderson, "Loss mechanism and high-low doping profile effects of silicon substrate with different resistivities at high frequency," in IEEE MTT-S International Microwave Symposium Digest, 2013, pp. 13–16

[16] Thomas H Lee, "Planar Microwave Engineering", Cambridge university press 2004, pp.123

[17] Chong, K. B.; Kong, L. B.; Chen, L. F.; Yan, L.; Tan, C. Y.; Yang, T.; Ong, C. K. and Opsipowicz,T. "Improvement of dielectric loss tangent of Al2O3 doped Ba0.5Sr0.5TiO3 thin films for tunable microwave devices", Journal of Applied Physics, vol.95, no.3, 2004 , pp. 1416–1419

[18] A. Brimont, D. J. Thomson, P. Sanchis, J. Herrera, F. Y.Gardes, J. M. Fedeli, G. T. Reed, and J. Martí, 'High speed silicon electro-optical modulators enhanced via slow light propagation', Optics Express, vol. 19, issue 21, 2011, pp. 20876-20885

Chapter 5: FABRICATION

In this chapter the fabrication process of the final devices will be discussed. There are three different process flows, two of which started off with a bare silicon (Si) wafer. The third process which required the fabrication of a slow wave structure on to the slow light modulator. The slow light modulator were processed at CEA LETI and slow wave structure will be discussed separately. All fabrication steps were carried out in the University of Southampton unless otherwise indicated.

5.1 Fabrication Process

Fabrication steps were chosen from the viewpoint of CMOS compatibility. A schematic of the fabrication process used to produce test electrodes and test structures for assessing the losses of the different elements of the full electrode structure is shown in figure 5.1. A 2µm thick silicon dioxide, SiO_2, layer was deposited on top of a prime Si wafer to isolate RF loss associated with the silicon. Prime Si wafer is the highest grade wafer and is referred as “device-quality” wafer in some text. Next, Aluminium was sputter deposited on to the wafer with a thickness of 1.2 to 2µm to minimize losses due to skin depth. Resist was then spun on the wafer with final thickness of ~ 2.45µm ±0.05µm. The wafer was patterned using photolithography followed by dry etching and resist striping. Dry etching was chosen due to its superior aspect ratio over wet etching.

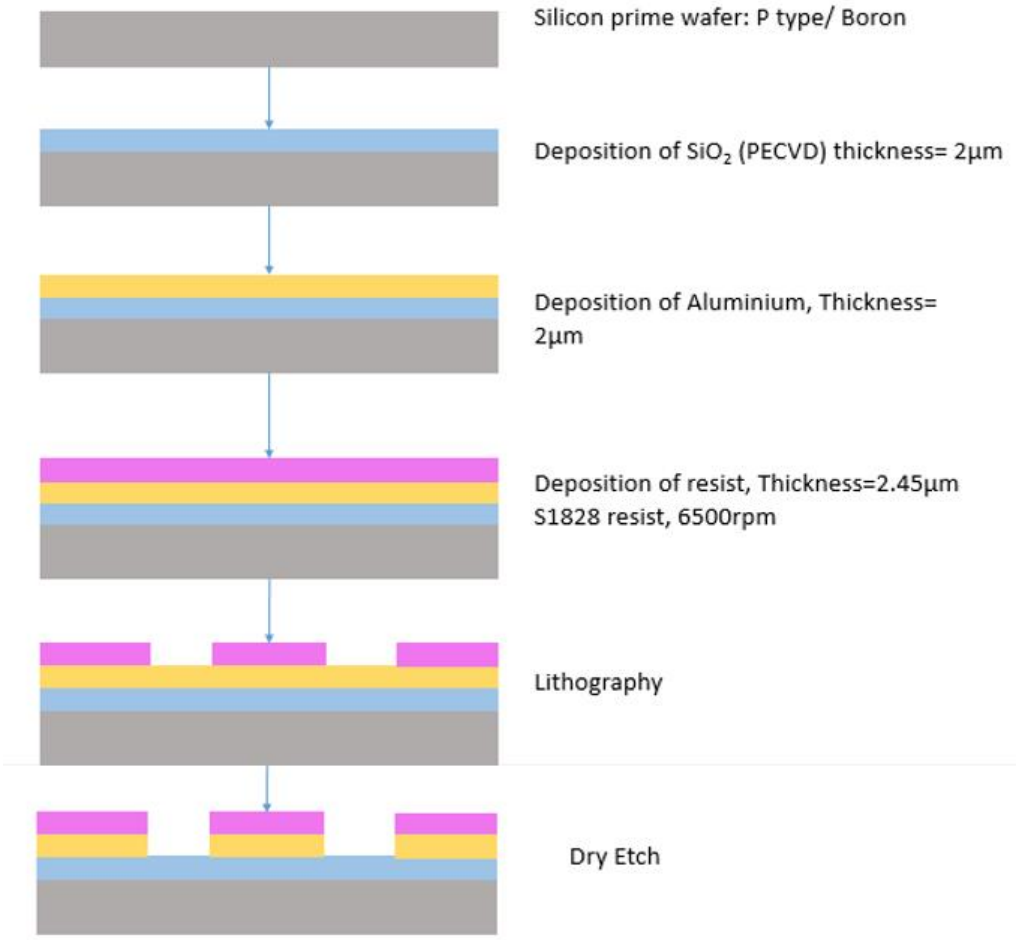


Figure 5-1– Fabrication process flowchart for Oxide wafer

The process flowchart in figure 5.2 shows the fabrication process for fabricated test electrodes on a doped Si wafer. The reason for doing this is to try to replicate the dielectric constant of the actual modulator (wherein light travels in the doped region) as closely as possible and to examine the losses due to doping even when it has been isolated by an oxide layer. An oxide layer of 2µm was thus deposited on the doped wafer using PECVD to replicate the buried oxide layer in the SOI wafers upon which the optical modulators are fabricated. Next a ~209nm thick p-type (boron doped) poly silicon layer is deposited. This is because the optical signal waveguide under study is a 200nm thick p-type region with doping level of $1x10^{17}$ cm^{-3} (0.194 Ω.m resistivity). The poly silicon in this work is deposited using Hot-wire CVD (HWCVD). The dopant in the poly silicon layer is activated using an 850 ^{o}C annealing step for 15 min[32] in the presence of an oxide cap which is then stripped off using HF. Oxide cap is needed during the anneal to ensure the dopants do not defuse into chamber and contaminate the chamber. Another layer of oxide of 1µm thickness was then deposited using PECVD to replicate the top cladding layer of the optical modulators followed by sputtering of a 2µm thick aluminium layer. The patterning process comprised photolithography steps, dry etching and resist stripping.

Figure 5-2– Fabrication process flowchart for doped wafer

5.2 Deposition

This section will discuss all of the materials and deposition methods used in the fabrication processes. The depth of discussion varies according to the importance of the deposited layer on the measurement results. The aluminium deposition and the quality of the deposition has a very high impact on the results thus the problems and remedies involved will be discussed. Silicon dioxide is used as an isolation layer from the silicon or/and doped polysilicon. Doped polysilicon deposition and the variation in thickness and doping levels will also be looked at.

5.2.1 Aluminium deposition

Certain considerations need to be made when choosing the deposition method for metals. Primary considerations include: the contact resistance between the semiconductor and the metal layer to form an ohmic contact, the adhesion between the metal and the semiconductor and whether or not an isolation barrier is required and the stress induced by differences between the two materials. Two types of aluminium deposition were considered due to the availability of the tools; sputtering and evaporation.

The Bak700 evaporator by Leybold was used for the evaporation of Aluminium. It is an electron beam evaporator unit where free electrons are produced by the cathode and the beam is directed onto the target material to be deposited via the anode. The electron beam heats up the material held in the crucible (in this case Aluminium) to its evaporation temperature. It then evaporates and is directed towards the wafer. The deposition rate for aluminium using this method is around 2.7Å/sec. The disadvantage of evaporation is that it does not give good step coverage which is essential for modulators as the surface is not planar. The step coverage term is used when the deposition is not conformal over the features. To keep consistency for result purposes, sputtering was adopted for most of the fabrication cases.

In sputtering, the target (Aluminium) is bombarded with argon ions (Ar+) which knocks atoms off the target (negatively biased) by breaking bonds. During this process, some energy will also be transferred to the target atoms (Al) which are sputtered on to the wafer. Sputtering also allows the formation of alloys with controlled composition. Sputtering is also the preferred method used for metal stack formation discussed in section 4.2. This is because it requires the step coverage and alloys are used in the metal stack. The Leybold Helios sputtering tool at the nanofabrication cleanroom, University of Southampton was used for sputtering Aluminium. The Helios tool is a plasma assisted reactive magnetron sputtering (PARMS) tool. The deposition rate found for Aluminium in this work is 15nm/min. The deposition rate was found by depositing different

thicknesses on 5 samples, using 5 different deposition times and measuring the deposited thickness using a profilometer (contact measurement using a stylus).

5.2.2 Surface roughness

In 1949, Morgan [1] studied the behaviour of regular grooves on the surface of a conductor at microwave frequencies using numerical modelling to show the power dissipated due to surface roughness of the conductor. And concluded conductor loss increases significantly as the skin depth becomes comparable to the surface roughness. In 1980, Hammerstand and Jensen [2], presented correcting factors to account for the surface roughness in attenuation of the conductor.

$$\alpha_c' = \alpha_c \left\{ 1 + \frac{2}{\pi} arctan\left(1.4 \left[\frac{R_{rms}}{\delta} \right]^2 \right) \right\}$$

Equation 5.1

Where R_{rms} = r.m.s value of surface roughness, δ = Skin depth, α_c = attenuation constant for a smooth conductor.

At low frequencies the skin depth will be large and the correction factor will be equal to 1. This means that the attenuation at low frequencies will be that of a smooth conductor. But as the skin depth decreases and the frequency increases, the loss due to the roughness will double as the correction factor will increase up to its saturation value of 2.

Later in 1996, Groisee et al. [3] presented a similar correction factor

$$C_s = 1 + exp\left\{ -\left(\frac{\delta}{2R_{rms}} \right)^{1.6} \right\}$$

Equation 5.2

Again, this formula suggests that the loss due to the surface roughness can only be doubled at most.

Historically the equations mentioned above have shown good agreement with measured data [4]. Tsang et al. [5] suggested via simulations that saturation to the value of 2 does not occur and the value of the correction factor increases beyond 2. This was confirmed by the experimental results of Horn et al. [4] in 2010 which were carried out up to 50GHz frequencies as shown in figure 5.3. In figure 5.3 H&J stands for Hammerstad and Jenson's model curve whereas ED (electrodepoisited) and RT (reverse-treated) abbreviate the deposition method. The graph shows the measured results for surface roughness r.m.s values of 0.5µm, 0.7µm, 1.5µm and 3µm. The

measured insertion loss when R_{rms} = 3µm was increased by a factor of three when compared with a smooth conductor as predicted by H&J. This means that the surface roughness can increase the insertion loss very significantly hence it is an important aspect to consider. The literature also suggests that the effect of surface roughness can be taken into account in simulation via changing the conductor resistivity to match the measured loss [4].

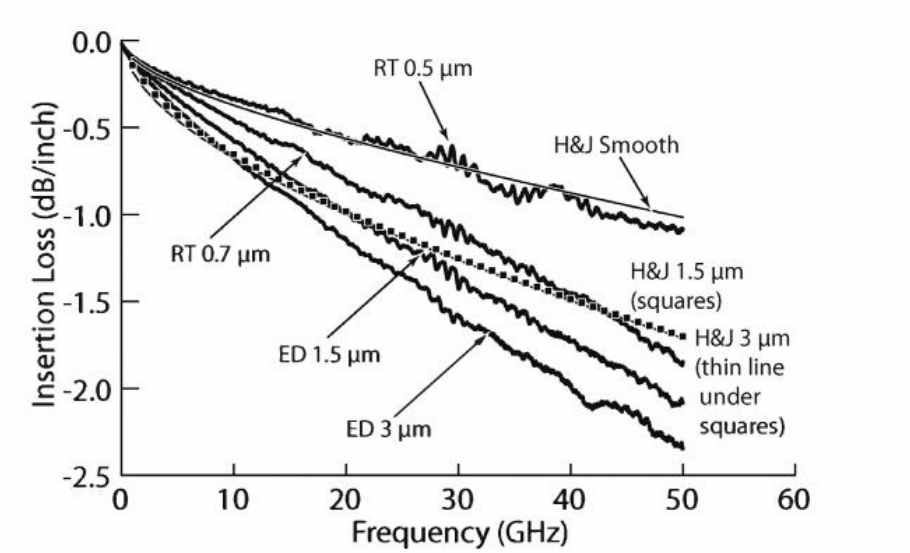


Figure 5-3– Insertion loss per inch of different r.m.s surface roughness and Hammerstad and Jensen model, taken from [4].

There are several factors that need to be taken into account for surface roughness in the deposition process, such as the formation of hillocks, grain size, hillock density, and hillock size. For hillock analysis using a scanning electron microscope (SEM), an area of 37µmx60µm was considered with the same magnification (1780X), working distance (4.4mm) and tilt angel (54°). The formation of hillocks for aluminium has been previously reported and studied [5][6]. The formations of hillocks, especially with large size, can be problematic as they can cause short circuits. When metals (like Al) with high thermal expansion coefficients are sputtered onto materials with low coefficients of thermal expansion (CTE) (such as Si or SiO_2) the stress between the materials cause hillocks to appear [7]. Where the CTE of the Al is 10 times higher than the CTE of the Si [5]. The mismatch in the thermal expansion coefficients of Al and SiO_2 will result in stress which will increase with increasing temperature. Formation of the hillocks is found to be the stress relaxation mechanism [5]. Stress relaxation/relieve could take place either by bulking up the material (hillocks) or cracking [28].

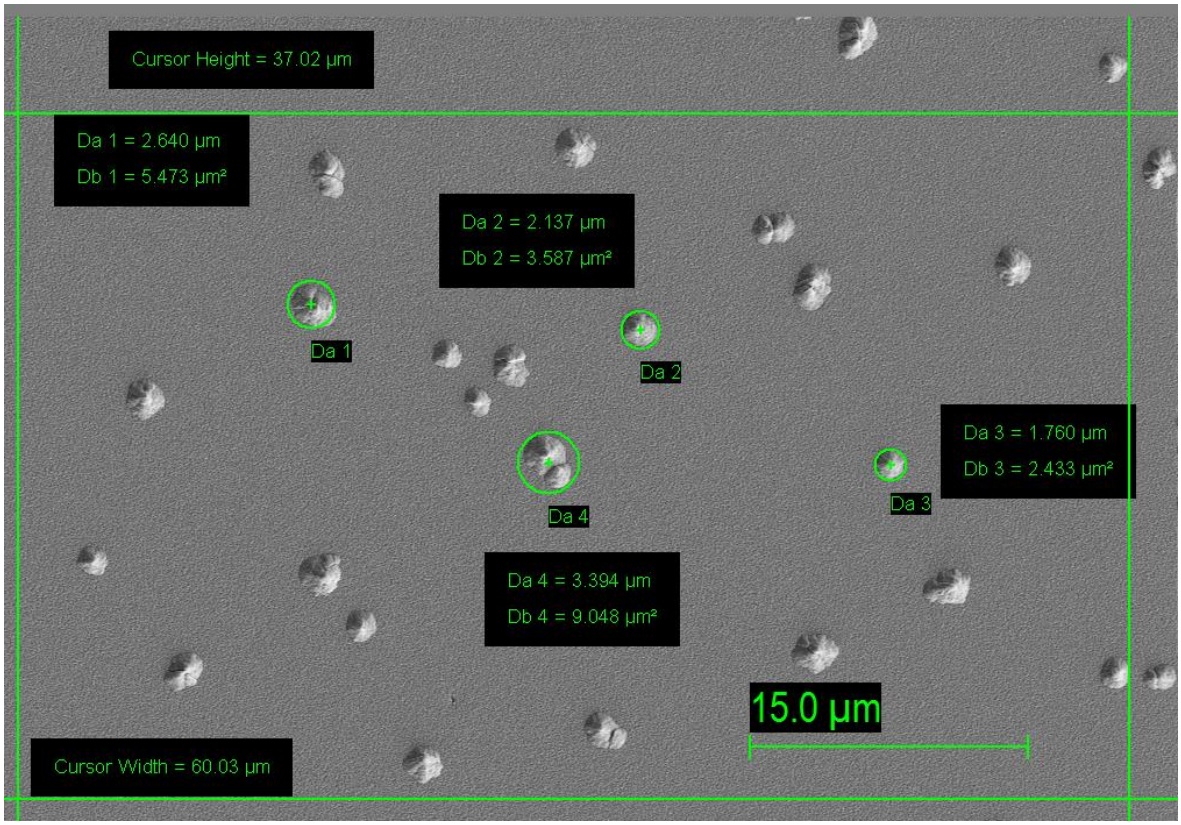


Figure 5-4– SEM image of Al (location A) with a thickness of 1.5µm used to calculate the average number of hillocks.

Figure 5.4 shows an SEM image of Al with 1.5µm thickness. Three different locations on the wafer were studied (A, B and C). The size of the hillocks was found to be of similar range in each of 3 areas on the wafer. Graph in figure 5.5 shows the average hillock diameter measured using figure 5.4 where the uncertainty of measurement is ±0.05µm. Where the green diamond shape represents the average value of the hillock diameter and the average of sample A, B and C are equal to 2.48µm, 2.92µm and 2.32µm respectively.

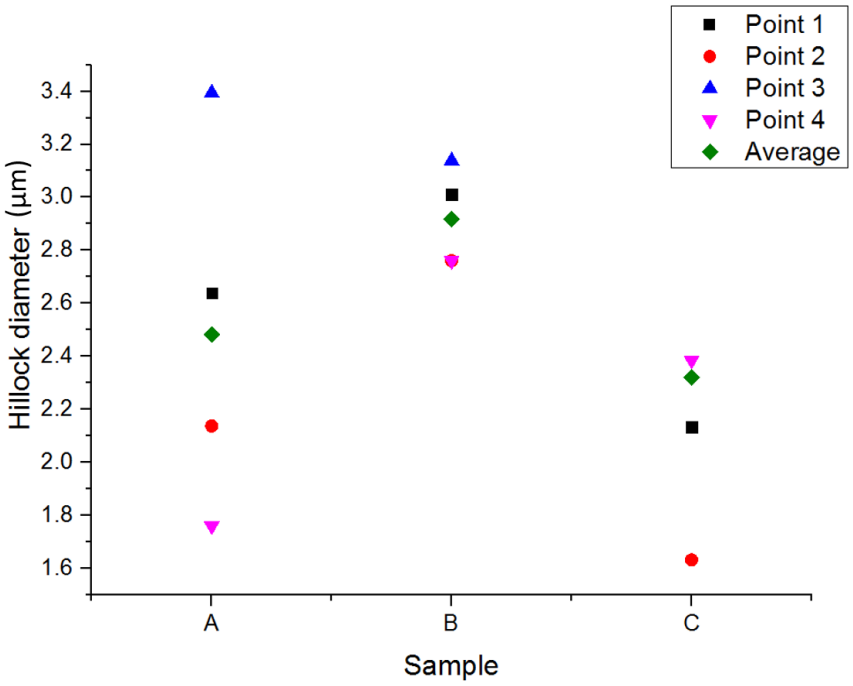


Figure 5-5–Hillock diameter (µm) for three samples for 1.5µm Al thickness

The number of hillocks found on sample A was 22 while sample B and C have 27 hillocks each, which gives an average of 25 hillocks in an area of 2220µm^2 (i.e. a hillock density of 11260 Hillocks/mm^2).

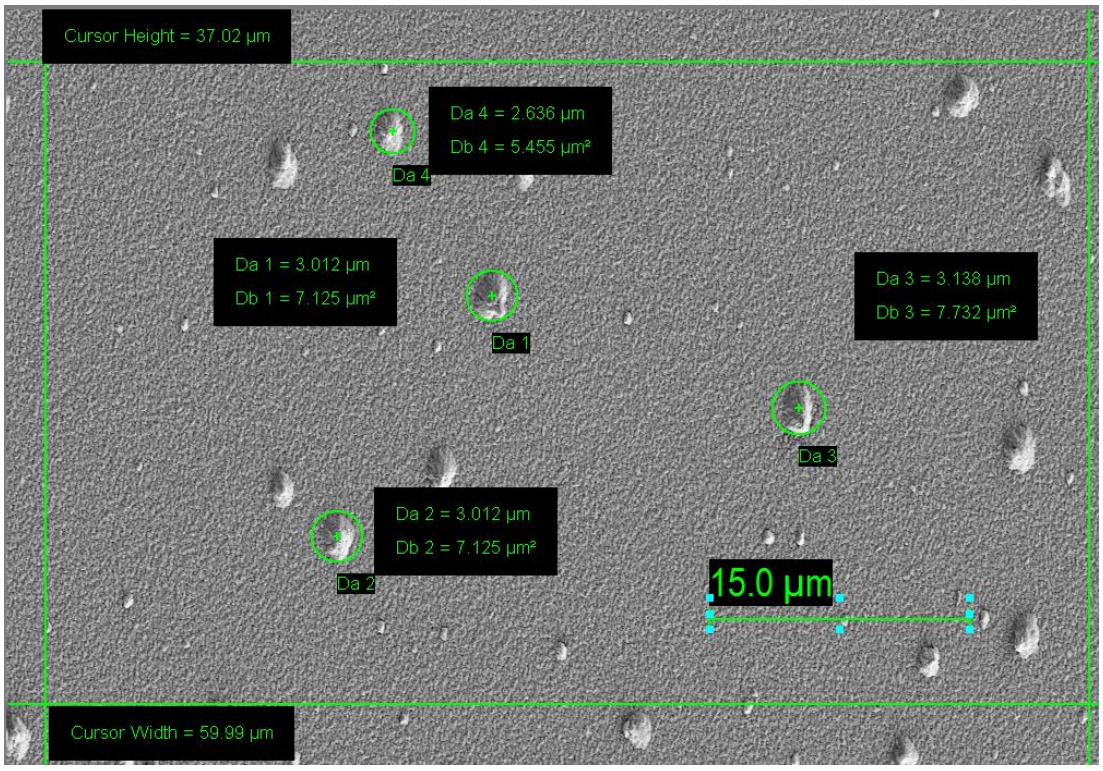


Figure 5-6– SEM image of Al (location A)with thickness of 2µm to calculate the average number of hillocks.

Figure 5.6 shows an image of sputtered Al with thickness of 2µm at location A. Graph in figure 5.7 shows the calculated size of average hillocks from figure 5.6 at three different locations on the wafer where the average is shown in green diamond shape and the average for sample A, B and C are equal to 2.95µm, 1.98µm and 1.75µm respectively.

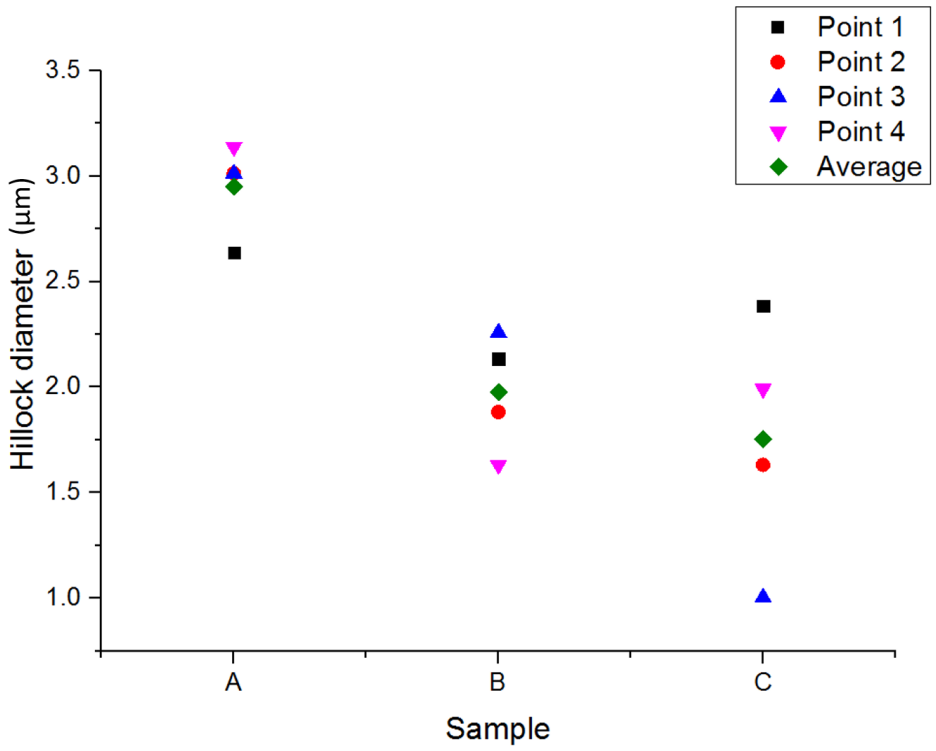


Figure 5-7– Hillock diameter (µm) for three samples for 2µm thickness of Al

For 2µm thick Al, the number of hillocks increased with varying size. The total number of hillocks in sample A was 36 where 13 of the hillocks were of larger (and similar) size compared to the remaining 23 hillocks which were found to be of smaller sizes. Sample B had a total of 38 hillocks with 13 big hillocks and 25 smaller sized hillocks. Sample C had a total of 46 hillocks where 18 were big hillocks and 28 small hillocks. This gives an average of 40 hillocks in the area of 2220 μm^2 (i.e. a hillock density of 18018 hillock/mm^2). The number of hillocks found for 2µm thick sputtered Aluminium was higher but the average size of the hillocks were found to be smaller in comparison to 1.5µm thick aluminium layer. This shows that when the thickness of the film increases the hillock density increases, while diameter of hillocks decreases.

In [6], they studied the effects of varying the thickness of Al on hillocks on glass substrate (700 µm) and Mo (Molyddenum) as a barrier (50nm). Their analysis concluded that hillock density decreases while hillock diameter increases with increasing thickness of Al but the system used for sputtering and conditions at which sputtering was done was not given in the paper. The thickness

which they studied were from 250nm up to 1000nm whereas the thickness studied here are 1500nm and 2000nm. The hillock formation and behaviour is highly dependent on the substrate and its coefficient of thermal expansion. Since substrates used in [6] and in this work are different hence the direct comparison is not possible. The paper [6] also studied the behaviour of sputtered Al with different thickness (250nm, 400nm, 600nm and 1000nm) under various annealing temperatures (180°C, 220°C, 250°C and 280°C) for 400 minutes. They also found that hillock density in the area is directly proportional to annealing temperature.

In this work the effect of annealing on surface morphology was also studied, via SEM. Annealing was carried out using rapid thermal annealing (RTA) on 3 samples cut from the same wafer, and annealed at different temperatures (180°C, 380°C and 420°C) for 15 minutes to see the effects on hillock density, hillock diameter and the aluminium grain size. The grain size appeared to be independent of the annealing temperature and was found to be ~ 220 nm. Stress relaxation mechanism is usually by formation of hillocks or cracking [28] hence, no difference in the grain size was observed. However, when evaporated Al films on glass, silicon and mica was studied in [29] and it was found that the grain size of Al was largest on silicon in comparison to glass and mica.

Hillock diameters on three different locations of the sample that was annealed at 180°C were determined to be 2.1335µm, 2.306µm and 2.4687µm. The total number of hillocks for these three samples, which consisted of both small and large hillocks, were 50 (large=29, small=21), 53(large=30, small=23), and 40 (large=18, small=22). Hillock diameters for three different locations on the 380°C sample were also measured to be 2.54µm, 2.35µm and 2.57µm. This shows an increase in hillock size by about 200nm as compared to the 180°C sample. The total number of hillocks for each of these three samples were 47 (large=43, small=5), 48(large=44, small=4), and 53(large=47, small=6). At 420°C the Hillock diameters of three different locations were 2.89µm, 2.70µm and 2.76µm, i.e. an increase in hillock diameter by ~ 500nm as compared to the 180°C sample. The total number of hillocks for the three locations were 32 (large=21 small=13), 56(large= 36, small 20), 50 (lager=31, small=19). It can be seen that the total number of hillocks (totalled over the 3 locations) for the 3 cases (180°C, 380°C and 420°C) is approximately the same i.e. the number of hillocks does not change significantly with annealing temperature. Hence it can be concluded from this work that aluminium annealing only increases the size of hillocks, contrary to [6] where the hillock density was also found to increase with temperature. This is because the time for annealing for both experiments were different. In this work, the anneal time was only 15 minutes whereas in the case of [6] the anneal time was 400 minutes due to prolonged annealing time, this may have caused hillock density to increase.

Cracks had appeared on specimens that were annealed at 380°C and at 420°C the number of cracks had increased with increasing temperature. Figure 5.8 shows an SEM image of a crack on the 420°C sample. For this reason 5 more samples were cut from the same wafer and annealed for temperatures between 180°C and 380°C (220°C, 250°C, 280°C, 320°C, 350°C) to see if the appearance of cracks takes place at a temperature below 380 °C. None of these samples showed crack formation.

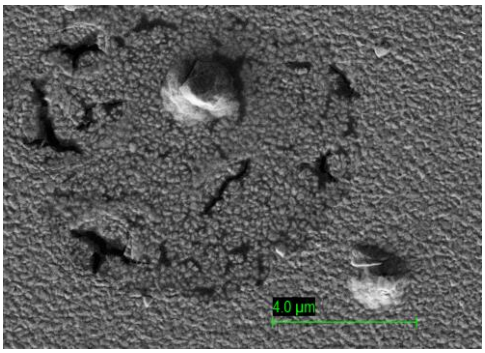


Figure 5-8– The formation of crack when the Al was annealed at 420°C

The grain size of the aluminium film was studied. Figure 5.9 shows the grain size of 2µm thick aluminium with an average grain size of 271µm (figure5.9 (a)) and average height of 121µm (figure5.9 (b)).

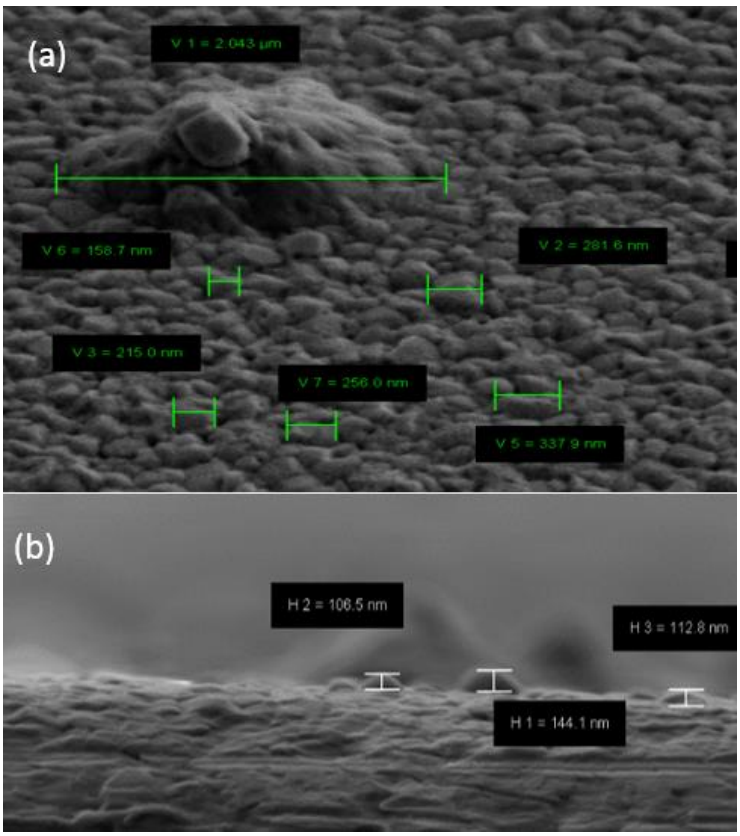


Figure 5-9– (a) Grain diameter for 2µm thick Al (b) grain height for 2µm thick Al

In 2008, Jang et al. studied the behaviour of capping an aluminium layer with different materials (Ti, Mo and SiO2) to see the effects on aluminium hillock formation. Different thicknesses (20nm, 30nm, 50nm and 100nm) of capping layer were deposited on top of the aluminium where SiO2 was deposited by PECVD and titanium (Ti) and Molyddenum(Mo) were sputtered. All samples were then annealed for 400mins at 280°C. The hillock density was found to have been reduced significantly in the case of titanium and Mo Capping. The hillock density decreased as the cap thickness increased. The metal stack of the electrodes discussed in section 4.2 and fabricated by CEA LETI consisted of Ti, TiN and AlCu. Where TiN is used as a barrier to prevent any diffusion of the electrode metal into the silicon and to prevent any reaction up to temperatures of 750°C [9]. If Cu diffuses into Si then it can damage the device. In other words, Cu contamination to Si was found to degrade the carrier lifetime of n type as well as p type silicon [30]. Al and Cu have high conductivities compared to other metals which results in a reduced RC delay. Cu gives better electromigration resistance, which is why a small percentage of Cu is added to Al in the part of the metal stack [9].

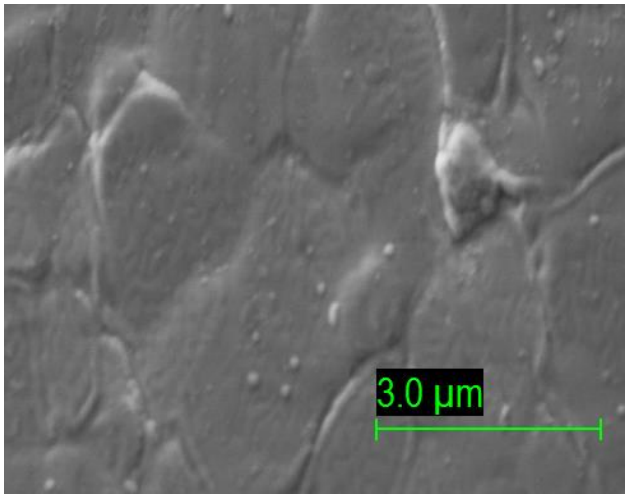


Figure 5-10– Metal surface of electrode fabricated by CEA LETI

Figure 5.10 shows the metal surface of metal stack fabricated by CEA LETI (fabrication foundry). It can be seen it is much smoother than Al alone would be as Ti has been used which will smooth the metal surface.

5.2.3 Silicon dioxide deposition

For silicon dioxide deposition, an Oxford Instruments PLasmaLab PECVD (Plasma- enhanced Chemical Vapor Deposition) system was used. PECVD is the deposition of material using gaseous sources consisting of atoms/molecules of material to be deposited. The chemical reactions take place in the gas phase during the deposition of the layer onto the substrate. SiO_2 layers were deposited using SiH_4 and N_2O to give SiO_2 ($+H_2$ $+N_2$). The SiH_4 (silane) was diluted using the 'inert'

gas (Nitrogen N_2). A standard recipe for silicon dioxide was used for the PECVD and this was characterised using a J.A. Woollam spectroscopic ellipsometry system which takes measurements between wavelengths of 192nm and 1700nm and is a non-contact method. The ellipsometer measures amplitude and phase of the reflected polarized light. The raw data is presented as "psi" and "delta" where psi is the ratio of the amplitudes and delta is the phase difference due to the reflection. A model based on the interaction between light and the material is then used to fit with the raw data to give meaningful results such as layer thickness, reflective index, surface roughness, composition, uniformity and other parameters.

For the slow wave electrode (discussed later in this chapter) silicon dioxide was sputtered since the samples already had metal on them which would contaminate the PECVD chamber. Figure 5.11 shows the deposition rate using Leybold Helios sputtering tool. The deposition rate for sputtering was found to be 0.52nm/sec.

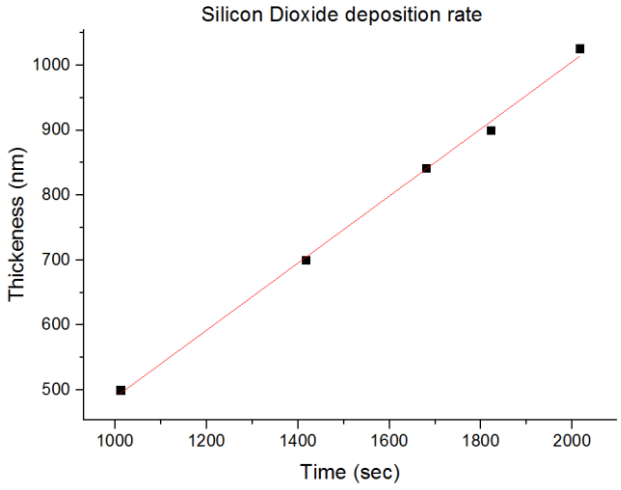


Figure 5-11– Silicon dioxide deposition rate using sputtering

5.2.4 Poly silicon P doped deposition

Doped polycrystalline silicon was deposited using Echerkon's HW-CVD (Hot-Wire Chemical Vapour Deposition) tool. In HW-CVD, the deposition is achieved at low substrate temperatures without the need of a plasma. Instead a hot filament is used to decompose the source gases into the required deposition material, where the hot filament temperature reaches up to 2100°C. The system also has two chamber heaters at the top and bottom which were set at a temperature of 500°C and the wafer is heated by radiation with no direct contacts. This ensures the temperature of the wafer is kept low (≤300°C) [10]. A 200nm p-type layer with hole/doping concentration of $1x10^{17}$ cm^{-3} was required. This is the concentration used in the waveguide region of the modulator. To achieve this, the gases used for the process were SiH_4, B_2N_6 and H_2. Figure 5.12

shows the thickness of the doped silicon across the wafer. It can be seen that the layer is quite uniform with about 10nm variation.

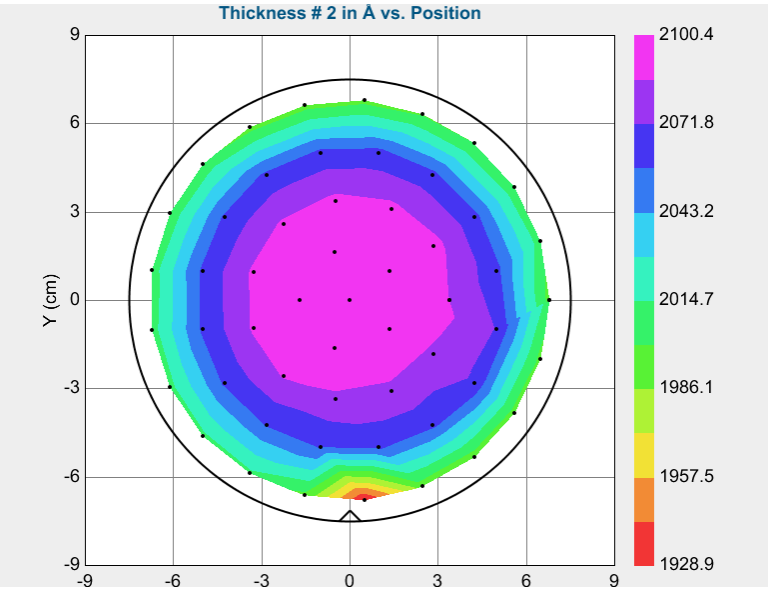


Figure 5-12– Thickness variation across the wafer before annealing the sample

The sheet resistance of the wafer was measured at different locations using a 4 point probe (Jandel, RM3-AR). Prior to annealing the sheet resistance was found to be 800kΩ/□, 1MΩ/□, 773kΩ/□ and 905kΩ/□. The wafer was then capped with a silicon dioxide layer and annealed using an RTA (rapid thermal annealer) to activate the dopants. Annealing was done in a non-metal contaminated RTA. The anneal temperature was 850°C and annealing time was 15 minutes [32]. After anneal, the sheet resistance of the wafer was found to be 397.9kΩ/□, 391.14kΩ/□, 381.64kΩ/□ and 413.3kΩ/□. The thickness of poly silicon also dropped by 10Å angstrom. Optimization of the doping level was not carried out as this was not used as an active region but rather to see the effects on the dielectric constant. The doped layer was separated from the metallization layer by a silicon dioxide layer as discussed above.

5.3 Patterning

After the metal layer is deposited on to the substrate, patterning of the metallization is done using photolithography and etching. This section will discuss the process of photolithography and etching methods used for this project.

5.3.1 Lithography

Lithography is a process in which a pattern is transferred to the wafer, typically from a mask. However, not all lithography processes require a mask. There are many techniques available for

lithography such as photolithography, electron beam, ion beam, x-ray and soft lithography. Photolithography uses light, electron beam uses electrons, ion beam uses energetic ions and soft lithography uses mechanical contact indentation [11]. Photolithography is the most common technique used when a resolution of 100nm or more is needed [11]. It is much cheaper with higher throughput compared to electron beam and x-ray lithography. Electron beam lithography has a high resolution (down to 10nm) [11] and the wafer is directly patterned, but the method is slow and thus expensive and is thus more suitable for smaller areas. X-ray lithography is a faster method when compared to electron-beam lithography, but masks are expensive to produce and cannot be focused through a lens. Thus photolithography was found to be most suitable for fabricating the electrodes as the smallest feature needed is not smaller than 2µm.

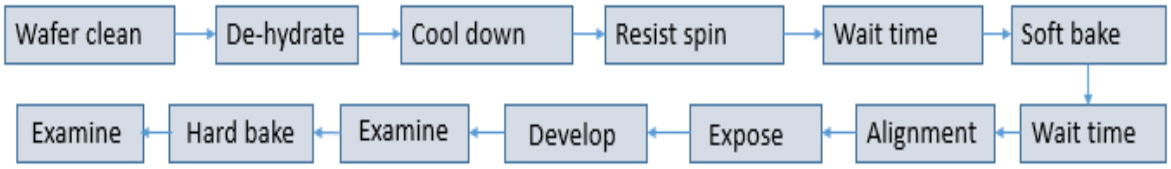


Figure 5-13– Flow chart for photolithography

Figure 5.13 shows the procedure followed in photolithography. The substrate is first cleaned to remove contamination, followed by a dehydration bake step which removes any absorbed water and promotes adhesion. Wafer contamination can either be organic or inorganic. Organic contamination can be oils or polymers that might have made their way onto the wafer during previous processing. Sodium/Potassium salts or the native oxide are usually classed as inorganic contamination. The cleaning process comprised a solvent clean which is an acetone dip. The acetone leaves a residue and this is removed by using IPA (Isopropyl Alcohol) and DI (Deionized) water. The sample is then dried using a nitrogen gun. This process will remove any oils or organic residues. The sample is then de-hydrated at 120 degrees for 30 minutes in the oven following which it is left out for 5 minutes to cool to room temperature.

Patterning can take place once the wafer is cleaned and dehydrated. The pattern is transferred on to the substrate (wafer). This is done by transferring the pattern from the photomask on to the photo sensitive resist using UV light. The resist is dispensed on to the centre of the wafer which is mounted onto the wafer chuck in a spinner. The resist spreads under centrifugal forces during spinning, performed at a pre-determined speed which coats the material and the excess resist is drained away. The thickness of the resist mainly depends on the rotation speed and viscosity of the resist. For most of the fabrication, positive resist Shipley S1800 series was used. Positive resist is the resist when exposed to UV light, it becomes more soluble hence removed and unexposed to

UV is the pattern left behind. For example: S1813 would usually give a 1.3µm thick resist at a spin speed of 5000rpm. The thickness of the resist can be varied by a few hundred nano-metres if the spin speed is changed. The slower the spin rate the thicker the resist would be. Shipley has published calibration graphs for their resists which shows resist thickness versus the spin rate. Conventionally, spin coating of resist is believed to give a poor step coverage while the spray coating should give better step coverage [12]. However, the step coverage is also dependant on how quickly the resist dries when it has been sprayed and the viscosity of the resist. Spray coating can give a more conformal coating but the resist viscosity should be less than 20cSt to be suitable for spraying [13]. The less viscous the resist is, the more easily it would flow. Spray coating is typically more suitable when a thin layer of resist is required. It is also inferior to spin coating in terms of uniformity [13]. However, due to the aspect ratio, the thick layer of resist was required, hence spin coating was adapted for this project and step coverage was not found to be issue for the smallest feature size (2µm) used in this project.

Soft baking also has an effect on step coverage. The viscosity of the resist is lowered which accelerates the resist flow before the solvents are removed and the resist is dried [13]. It is therefore best to wait for 5 to 10 minutes after applying the resist to allow enough time for the resist to dry. The drying process is important to ensure no bubbles, cracks or stress are formed between processing steps. Figure 5.14 shows the effect on the fabrication when bubbles are formed, after which the soft bake on the hot plate is carried out.

Soft baking was done at 115 ^{o}C degrees for 60 seconds. The temperature of the bake decides the sensitivity of the resist to exposure. If the soft bake temperature is too high the resist will require higher exposure [14]. After the soft bake the sample is again allowed to cool to room temperature for 5 minutes which allows the resist to settle.

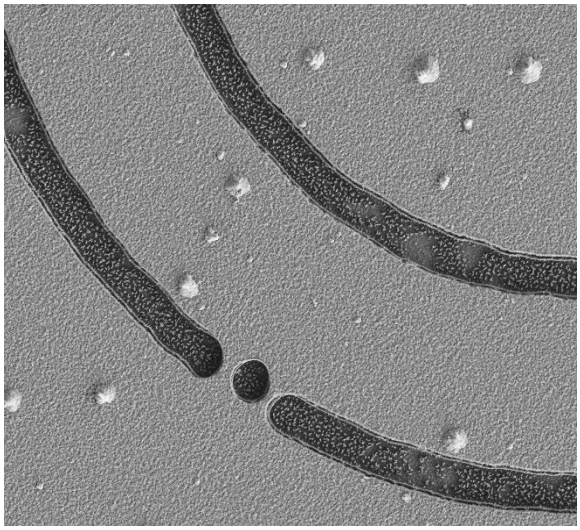


Figure 5-14—formation of bubble by the resist

This process is followed by exposure to UV light with help of a mask aligner. The mask aligner has four different contact options which are proximity, soft contact, hard contact and vacuum contact. Vacuum contact gives best resolution among all the contact types as it minimizes diffraction effects at the edge of the chrome features on the photomask. However, because of the physical contact between the mask and the wafer, this can result in damaging the mask due to resist contamination. The resolution achieved also depends on wafer flatness. Other than resist thickness and feature size [13] the exposure dose will also depend on the material on which the resist is spun. For reflective surfaces the dose needs to be lower, e.g., for aluminium the exposure dose is reduced when compared with a silicon substrate which is relatively non-reflective. It also depends on the thickness of the resist and feature sizes required [13]. For S1828 resist spun at 6500rpm, a dose of 216mJ is required for a coated Aluminium layer. In this work, hard contact was used for the exposure to minimize the damage caused to the mask while keeping the diffraction effects to a minimum.

Once the resist is exposed it is developed for 90 seconds in the developer solution with development rates vary with sample size. Therefore it is best practice to observe the sample under the microscope in order to ensure that it has been fully developed. The next step is to hard bake at 115 ^{o}C for 5 minutes on a hot plate. It can then be further examined under the microscope and the thickness of the resist can be measured using a contact profiler. Figure 5.15 shows the microscope image of the resist on top of the Aluminium. Figure 5.15 (a) shows the coplanar waveguide taper and figure 5.15 (b) shows the feature of 3µm.

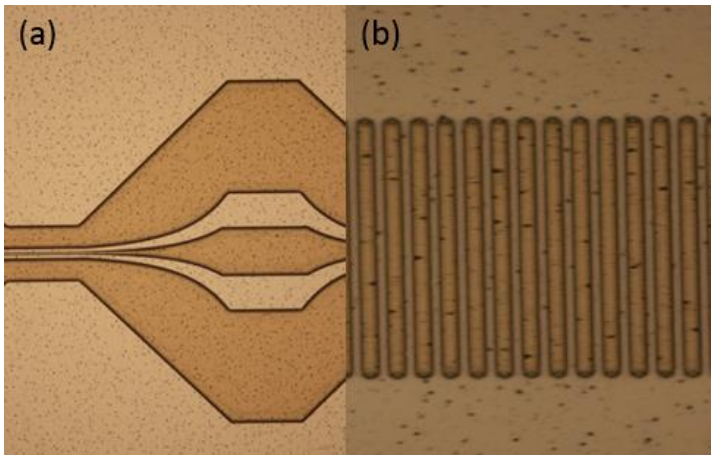


Figure 5-15–(a) Developed resist (S1818 with 2.1 µm thickness) for cpw taper (b) Developed S1818 resist for corrugated metal structure.

5.4 Etching

Depending on the feature size required, either dry or wet etching can be employed to transfer the pattern from the photo resist on to the substrate. In this project, both etching methods were adopted at different instances. Etching is a process of removing material which is unmasked (not covered in resist) by the means of a wet etch or dry etch. Important considerations for etching are: selectivity to other exposed materials, etch rate, degree of isotropy (side wall profile), uniformity and damage [13]. Selectivity means how quickly the material etches compared to the resist (or other exposed material) and the rate with which the material etches is known as the etch rate. This rate is also dependant on feature size (aspect ratio dependant etch) and sample size (loading effect), where the dependency on the area to be etched is referred to as the loading effect [13]. Aspect ratio dependant etching is when the small features on the same sample etches slower than bigger features. The angle of sidewalls (degree of isotropy) is crucial for fabricating the electrodes, as they will have a high impact of electrical measurement as this will vary the impedance of the line. For wafer scale fabrication, the uniformity issue can also be noticed. During the etch, damage might also be caused to the substrate and this could be crucial for certain cases. The etch rates affects the cost of production as well as the throughput thus fast etch rates are preferred.

Wet etching is a process of immersing the sample into an etchant solution and the material is removed by chemical reaction or dissolution. An isotropic etch has the same etch rate in all directions whereas anisotropic etching refers to a non-uniform etch. The aspect ratio, which is an important design consideration, is the ratio of width to depth of the feature to be etched.

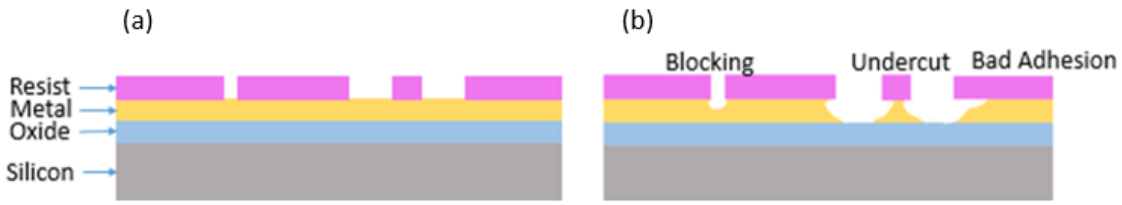


Figure 5-16– (a) before wet etch (b) after wet etch

Wet etching generally gives a higher throughput and high selectivity but it leads to isotropic undercutting and can also suffer from photoresist adhesion problems (see figure 5.16) [13]. It can also be seen that blocking can occur if the gap is too small and etch rate would vary with the feature size. Due to undercutting, wet etching is not suitable when the width starts to become comparable to the thickness of the material to be etched. Wet etching was adopted in this project when the feature size was large for example in the case of etching a window in the oxide layer

between the original electrode and slow electrode structure. The oxide layer etching area, more than 1.25x105µm^2, is etched away to expose the electrode's probing pad on the original underlying device electrodes. Hence issues associated with wet etch will have no impact on measurement results. The SEM image of the etched silicon dioxide layer on top of electrodes is shown in figure 5.17. It will be discussed further in section 5.5. Silicon dioxide was etched using HF (hydrofluoric acid). HF can be buffered using ammonium fluoride (NH_4F). The ratios which can be used are 7:1(NH_4F: HF) and 20:1 (NH_4F: HF). Silicon dioxide was sputtered for the slow wave electrode and the wet etch rate found for 7:1 HF ratio is shown in figure 5.18.

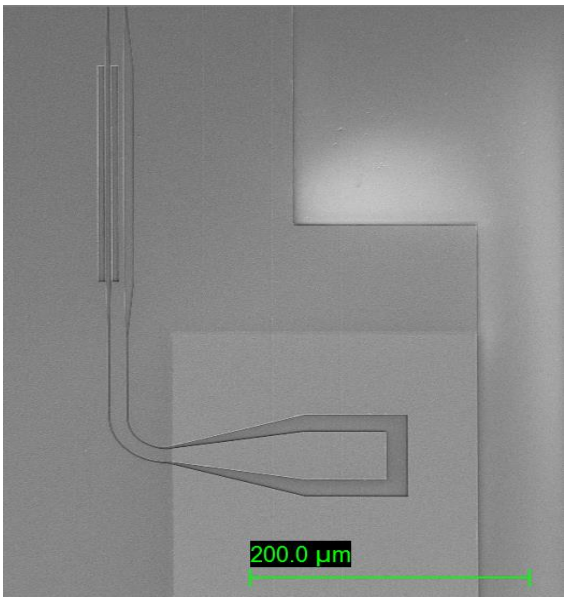


Figure 5-17– shows SEM image of slow wave electrode wet etched for exposing the probing pads

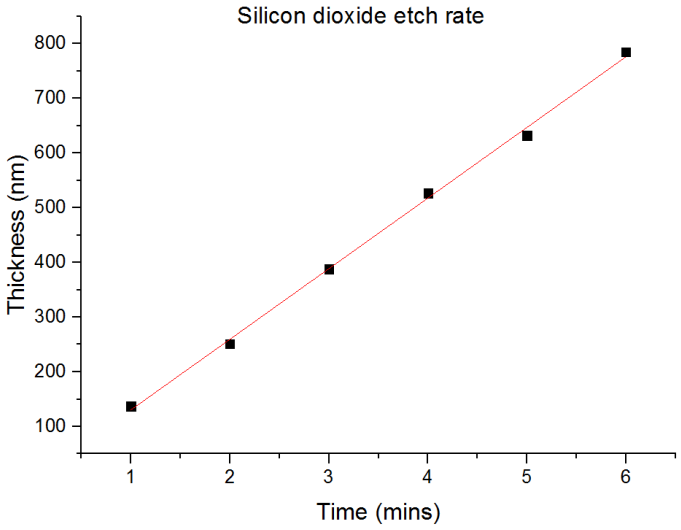


Figure 5-18– Graph showing silicon dioxide etch rate for sputtered silicon dioxide

Dry etching is an alternative to wet etching and uses a plasma to remove material from the surface. The hardware involves gas delivery to a vacuum chamber with exhaust and RF generator [13]. Due to the aspect ratio of the metal layer, the dry etch was required for electrode etching.

Dry etching does not suffer from photoresist adhesion issues and anisotropic etch profiling is possible due to the way it is etched whereas in wet etch the chemical can enter beneath the photoresist. The recipe can be optimized to give the desired vertical sidewalls. Dry etching is either plasma etching, RIE (reactive ion etching), DRIE (deep etching ion etching, aka bosch process), or IBE (ion beam etching). The silicon dioxide dry etching process uses fluorine based gases such as CF_4, SF_6, NF_3 and CHF_3[13]. Inert gases like oxygen, argon and helium can be used for the plasma stabilization, for ionization and for heat transfer [13].

5.4.1 IBE etching

IBE (Ion beam etching aka ion milling) performed by the Ionfab300Plus system from Oxford instruments was used to carry out the physical dry etch. It is a physical process in which the sample is etched away using energetic argon ions which are bombarded onto the substrate at low pressure to remove material. This will not only remove exposed material to be etched away but also the resist and the etch rates vary with sample size. Therefore the resist and the material to be etched need to be of similar thickness. The substrate is rotated during the process to give uniform etching throughout the process. Also the tilt of the sample can be varied. Heat is generated when energetic ions bombard the sample. Thus the back side of the sample is cooled using helium.

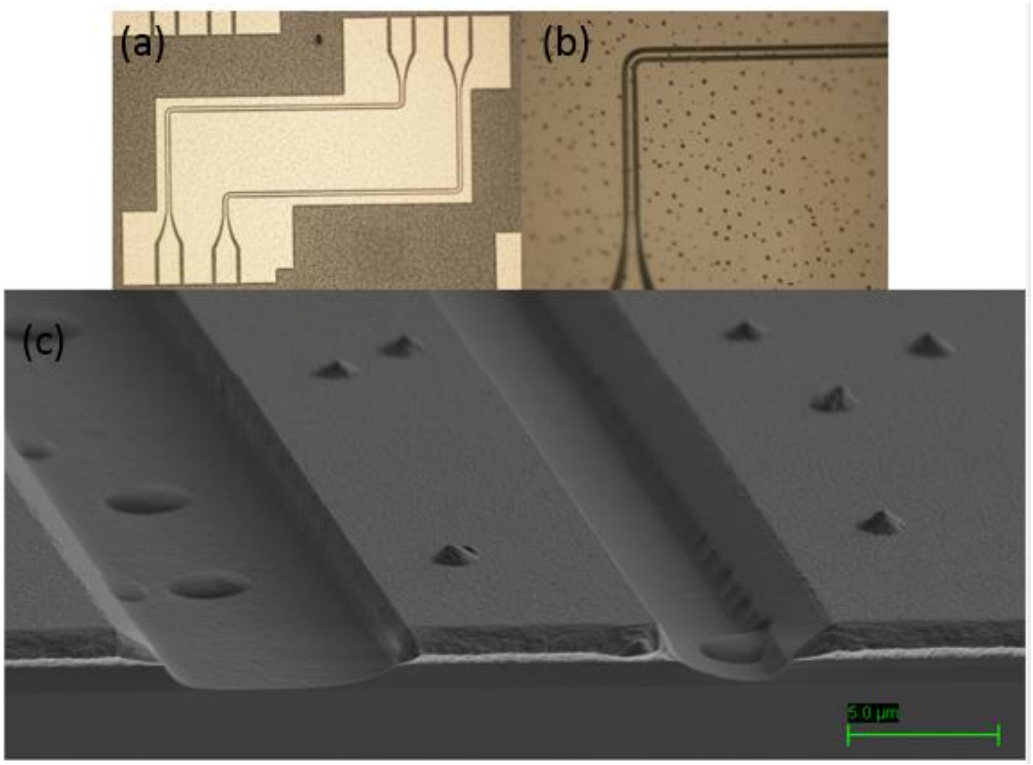


Figure 5-19– (a) and (b) shows the microscopic view and (c) shows the cross section of the electrode fabricated using IonFab300

Figure 5.19(a) and (b) shows the microscopic view and (c) SEM cross section of the electrodes fabricated using the Ion Fab system in the ORC cleanroom which can hold 4 inch wafer. It can be seen that the sidewall of the signal line has a straight profile compared to the ground plane which has more angled anisotropic side walls. Furthermore, the etch rate was not uniform across the wafer. After stripping the resist, the etch depth at the centre of the wafer was measured to be 2.5µm while the etch depth at the edge was only 2.13µm. The etch rate was therefore higher around the centre of the wafer compared to the edges. Thus etching through into the underlying silicon dioxide layer was required to avoid short circuits in the electrode structures placed at the outer areas of the wafer. Selectivity for the IonFab system is 1:1 which means it will etch all materials at the same rate; making the choice of resist thickness crucial.

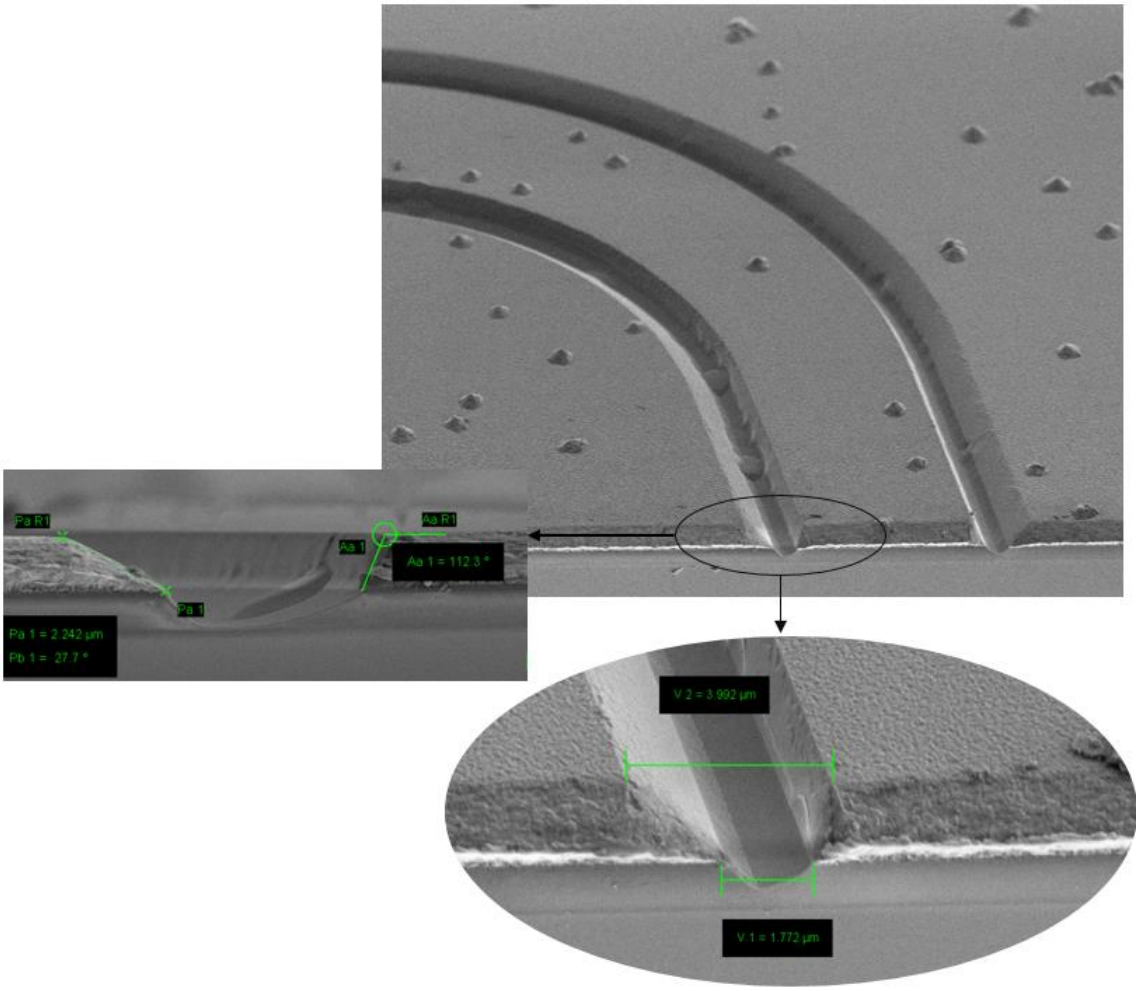


Figure 5-20–shows the close up of the bend with smallest dimension (2µm) on the wafer

Figure 5.20 shows the round bend with 2µm gap (smallest gap in the mask) etched using IBE. Due to the anisotropic profile the width of the metal at the top was about 4µm, whereas the bottom of the metal it was around 2µm (as can be seen from figure 5.20 zoom), i.e. the metal top has twice the width. The issues such as redeposition and shadowing in IBE has been reported in the literature [31]. Redeposition occurs when the material from the trench settles on the side walls leading to sloped walls. This usually is resolved by tilting and rotating the substrate while etching. However, the issue with stands if the aspect ratio is high. In the case of the high aspect ratio, shadowing on one side wall will also occur giving two different angles. Figure 5.21 shows the IBE configuration under tilt and rotation and illustrates the issue.

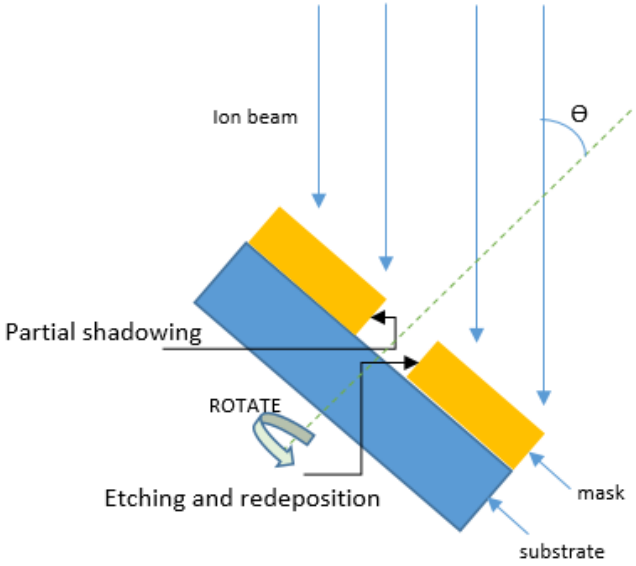


Figure 5-21–IBE etching with tilt and rotation [31].

The Ionfab one plus at the nanofabrication cleanroom is capable of handling upto 8 inch wafers and has a bigger chamber when compared with the ORC ionfab produced by the same manufacturer. Etching was carried out at 3 different angles (0°,20° and 45°) so see its effect on the side wall angles. All three different angles gave the same sidewall angle of 40°. Figure 5.22 show the ionfab etch with a 20° tilt. The angles of all the sidewalls were found to be about 40 degrees.

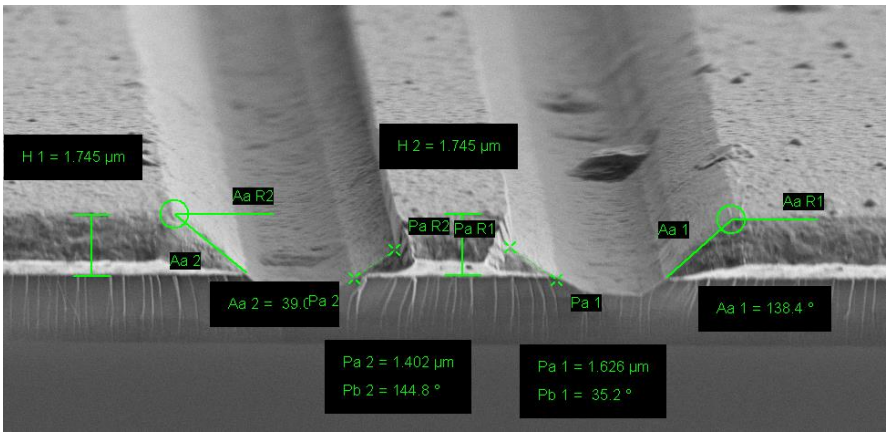


Figure 5-22–shows ionfab etch 6 inch wafer etch using 20 degree tilt

In IBE etching, the selectivity, uniformity and anisotropy were found to be an issue. Selectivity is important if these electrodes are to be fabricated on top of modulator and anisotropy will affect the electrical performance significantly. This led to exploring other possible etching method i.e. ICP.

5.4.2 ICP etching

To achieve vertical side walls and more uniform etch rates throughout the wafer, the Oxford instruments plasma lab OIPT SYS380 tool for ICP (inductively coupled plasma) etching was used for the fabrication of these small dimensions. In this technique, RF power is applied to the coil which produces a high density plasma through electromagnetic induction. This generates a high density of ions of reactive gas which are directed and accelerated towards the substrate. The plasma does not only contain ions but also free radicals and by products. An increase in the momentum transfer from ions to the substrate is possible by increasing the RF platen power which results in an increase in the so called milling effect. On the other hand, increasing the ICP power increases collisions of gas molecules producing more charged particles (electrons and reactive ions) which results in an increase in the chemical etch rate. Thus the RF power controls the physical etch while chemical etching is controlled through the ICP power. Pressure inside the chamber is dictated by the flow rates of the gases and the throttle valve on the exhaust which is also defined in the recipe. Argon is used to stabilise and homogenise the plasmas which will otherwise oscillate [18], and will also affect the etching parameters such as etch profile. The etch profile can therefore be controlled by adjusting flow rates of gases, RF power, ICP power, pressure, and also by the table temperature. The table temperature is the temperature at which the wafer is held.

Helium is also flowed onto the backside of the wafer to provide cooling. The flow rate of the helium is adjusted according to the set the table temperature. Available gases for the metal ICP are inert (Ar), oxidising (O_2), and corrosive (Cl_2, HBr, $SiCl_4$). Chlorine based and bromine based chemistries are used to etch metal since fluorine based aluminium etches are non-volatile [17]. As a starting point an available recipe for aluminium (which used chlorine [15]) was selected. When aluminium reacts with chlorine, it forms aluminium hexa-chloride ($2Al + 3Cl_2 \rightarrow Al_2Cl_6$) [19].

The ICP parameters were varied to find an optimized recipe for anisotropic Al etch. Chlorine provides a purely chemical etch which could lead to an undercutting effect (isotropic etch)[24]. However, this can be avoided by changing other parameters to get more anisotropic etch [24].The optimized recipe which utilised only Cl_2 to etch Al is shown in table 4.3. Figure 5.23 shows the SEM images as a result of this recipe.

Table 5.1– Recipe for Al using Argon and Chlorine

ICP power: 1000W	**RF power: 200W**	**Cl_2:50sccm** **Ar:12.5sccm**	**Temp: 20°C**	**Etch time:2min**

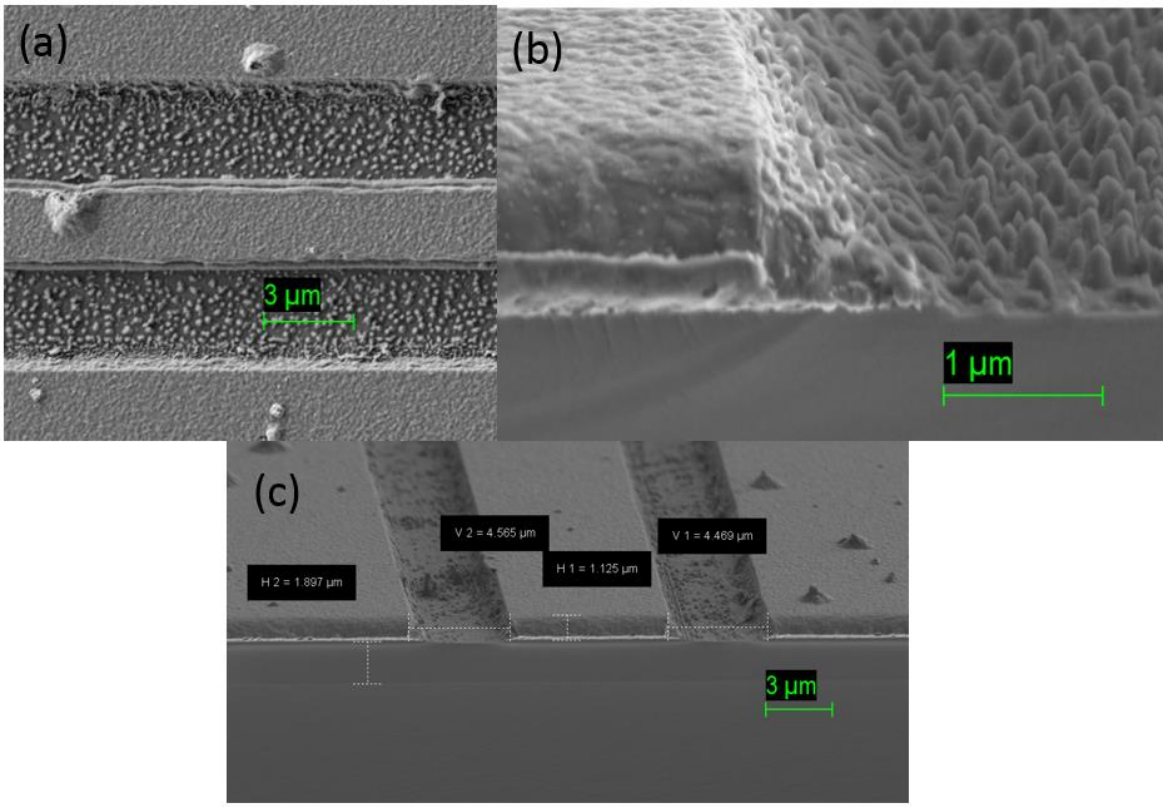


Figure 5-23–(a) top view electrode, (b)shows close up of the pillars and (c) shows the profile of the etch

Figure 5.23(a) shows material in the etched regions, which was found to be aluminium oxide. Aluminium forms a native oxide layer (few nano-metre) when exposed to air or water ($2Al + 3O_2 \rightarrow 2Al_2O_3$) [19] but Cl_2 does not etch Al_zO_3 (aluminium oxide). This then acts like a hard mask (micro-masking) hence pillars are formed (figure 5.23(b)). The sidewall etch profile is at almost vertical (figure 5.23(c)). Usually, BCl_3 is used to remove the native aluminium oxide layer from trenches [16] and scavenge any moisture[24]. Any moisture in the chamber may inhibit etching [24]. Since BCl_3 was not available, HBr (Hydrogen bromide) was used to see if it could remove the pillars. The H in HBr reacts with photoresist [20], which will cause polymerization of the sidewall and gives a more anisotropic etch [21] [24]. The recipe is given in table 5.2 which uses an etchant gas mixture of chlorine and HBr.

Table 5.2– Recipe for Al using Argon, HBr and Chorine

ICP Power: 800W	**RF power: 30W**	**Cl_2=10sccm** **HBr=50sccm** **Ar=10sccm**	**Temp: 40°C**	**Etch time:4min**

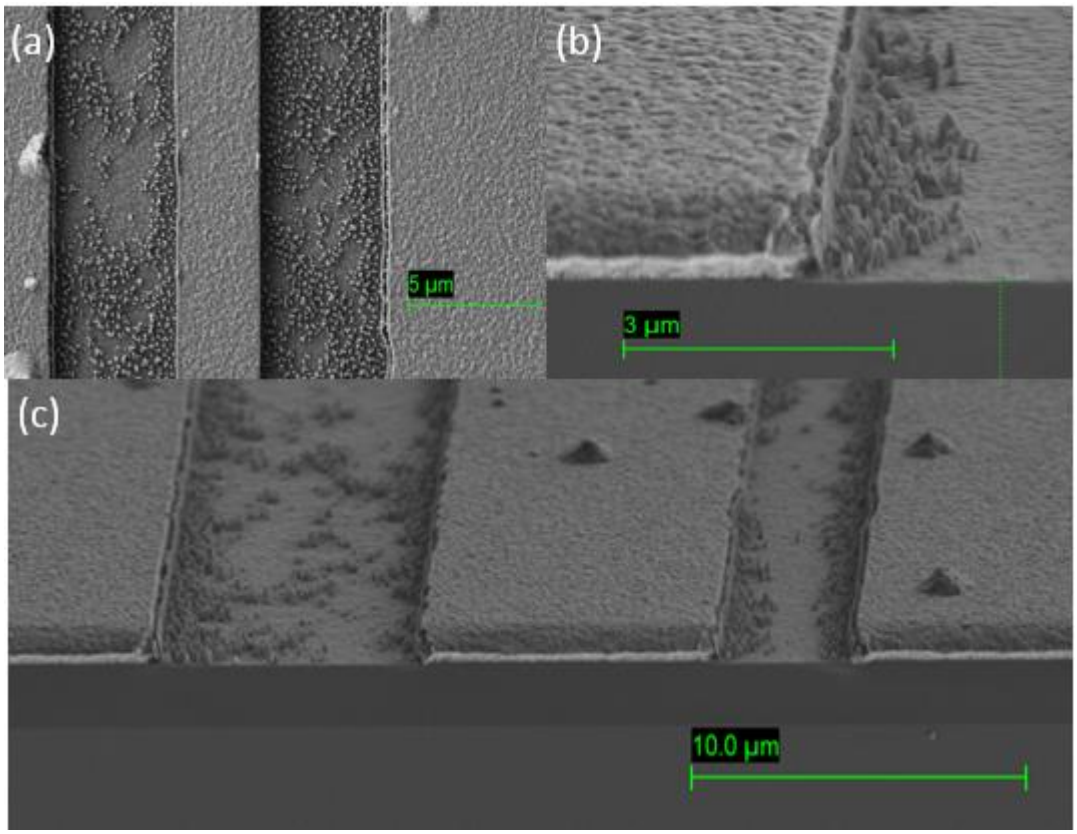


Figure 5-24–(a) top view of electrode, (b)shows close up of the pillars and (c) shows the profile of the etch

Figure 5.24 shows SEM images when HBr was used. It can be seen the number of pillars have decreased. Figure 5.24(b) shows the side wall and a close up of the pillar. The sidewalls for the etch were vertical as shown in figure 5.24(b) and (c). When the Al layer was in the order of 200nm, the pillars was not observed, but when the thickness of the Al increases in order of 1000nm then this issue arises again.

Next, the less commonly used gas mixture of silicon tetra-chloride ($SiCl_4$) and chlorine (Cl_2) was tried as an etchant for aluminium to see if this mixture is useful in avoiding/reducing pillar formation. This is because $SiCl_4$ etches aluminium oxide [22] and so it was thought that adding it to the gas mixture (Cl_2 and Ar) might etch away the Al_2O_3 pillars that are formed during Al etch via Cl_2 and Ar. $SiCl_4$ is also known to have similar scavenging ability to BCl_3 [23]. By using $SiCl_4$, the pillar effect was completely eliminated however the vertical sidewall profile was affected. Experiments were then carried out to achieve high selectivity vertical side walls using $SiCl_4$. These will be discussed below in “variations of parameters for ICP etching”.

5.4.2.1 Effects of resist on ICP process

The use of photo-resist as a mask is economical and simple compared with hard mask but it can also result in rough edges [25] as shown in figure 5.25(a). Figure 5.25 shows an ICP etch (using the

same recipe) for two different photo-resists with different thicknesses: 1.3µm of S1813 and 2.45µm of S1828. While the exact reason for the rough edges in the case of S1813 is not known due to the complex ICP process, it is believed that this happens because the resist profile is curved after the hard bake implying that the resist is thinner around the sidewall regions. This results in the resist being etched around the sidewall regions causing the underlying aluminium to be exposed to ICP etching in these regions; hence the observed needle type structures in figure 5.25(a). On the other hand S1828 is thick enough (even in the sidewall regions) to withstand etching resulting in a good sidewall profile (figure 5.25(b).

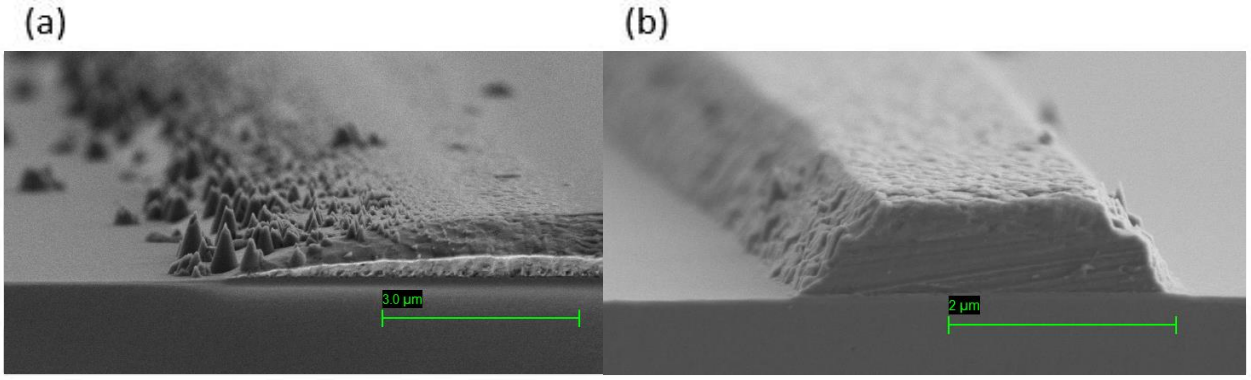


Figure 5-25–(a) shows the etch with S1813 resist (b) shows etch with S1828 using the same recipe.

A similar result, regarding resist thicknesses, was also obtained when a different ICP recipe was used. In figure 5.26 (a) was obtained after ICP etching of the S1813 resist. This time, the region around the resist was completely etched away resulting in a polished metal top. On the other hand the thick S1828 resist was able to withstand etching from the top (see figure 5.26 (b)).

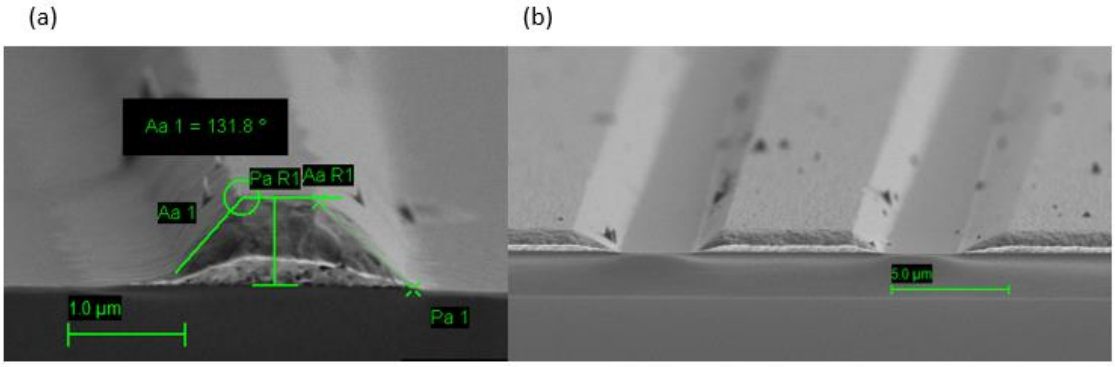


Figure 5-26– (a) shows the etch with S1813 resist (b) shows etch with S1828. Both images were obtained using same ICP etch recipe.

The wafer is maintained at temperature during etching using a chiller. If the sample is placed onto a carrier wafer then heat transfer from the sample to carrier wafer can be an issue due to trapped air between the two. This means the sample may not be maintained at the table temperature (carrier wafer temperature). In this case, the high temperature of the sample (due to the

surrounding plasma) can burn the resist resulting in a deformed pattern transfer. This has also been observed to lead to holes in the metal that was otherwise protected by the resist. Thus it is necessary to use thermal conductive paste between carrier wafer and the sample.

5.4.2.2 Variation of parameters for ICP etching

To obtain a vertical profile using $SiCl_4$, one parameter was varied at a time to see how it affects profile angle, etch rate, selectivity and texture. Each parameter and its effects will be discussed in this section and all accompanying images can be found in the Appendix. An anisotropic profile with high selectivity will be presented as the result of this experiment.

Table temperature:

As discussed earlier, the wafer temperature needs to be kept low enough so that the photo-resist neither flows nor corrodes. The table temperature controls the volatility of gases and by-products which means that the chemical etch will be highly affected by temperature. This will then affect selectivity, sidewall profile, as well as surface roughness [26]

The table temperature for the ICP etcher was varied from 5°C to 80°C. The graph in figure 5.27 shows the effects of varying temperature on the profile while keeping all other parameters constant. These parameters are shown in table 5.3. As the temperature increases, the sidewall angle decreases. The angle is measured from the surface of the metal, which means to get completely vertical profile, an angle of 90° is required. The angles were measured using an SEM with an error of ±2 degrees. Temperatures between 5°C to 40°C show no difference in profile angle, within the error range. As the temperature rises to 60°C a noticeable improvement of the angle was observed (i.e. more vertical), while the sidewalls became rougher. Upon further increasing the temperature to 80°C the profile angle appears to improve substantially compared to 60°C, however, both selectivity and roughness increase within the range 60-80 °C which is why the profile angle appears to improve. It was also found that at 80°C, damage was caused to the SiO_2 layer and approximately 300nm of SiO_2 was etched away. The best table temperature was found to be between 20°C to 40°C. As these temperature the profile angle, selectivity and surface roughness were found to acceptable.

Table 5.3– ICP parameters used while varying the temperature

ICP power:1000W	**RF power: 200W**	**Cl_2:50sccm** **$SiCl_4$:15sccm** **Ar:12.5sccm**	**pressure: 5mTorr**

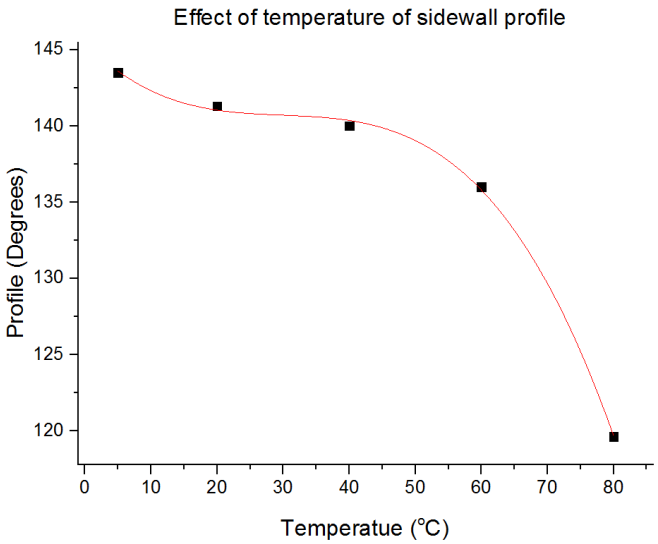


Figure 5-27– Effects of temperature variation on sidewall profile using ICP

Chamber Pressure:

Chamber pressure controls the amount of the gas (ions) available in the chamber. It is adjusted by shutting the throttle valve or adding more gas [27]. The pressure was varied between 3mTorr and 8mTorr while keeping all other parameters constant as shown in table 5.4. At 3mTorr, the sidewall profile was found to be 127.7°±2° with smooth sidewalls. At 5mTorr, the profile angle increased to 141.3°±2°, and the sidewalls were still found to be smooth. When the pressure was increased to 7mTorr the profile angle of the sidewalls improved to 130°±2° but the sidewalls were found to be rough. At 8mTorr, the slope of the sidewall increased to 140.4°±2° and gave a rougher profile as compared with 7mTorr. The oxide layer was also etched away meaning the selectivity decreased. One of the effects of increasing chamber pressure is increased ion scattering collisions. This alters the path of incoming ions. In theory, this will give rise to lateral etching (undercut) [27]. At 7mT, ion induced roughness of the metal layer was observed. At 8mT, chamber pressure was found to be high and high bombardment of ions caused damage to the oxide layer with significantly decreased selectivity against the mask and oxide layer. Hence the maximum usable, and optimized chamber pressure was found to be 5mT. Lower pressure was found to improve anisotropy as this minimises scattering [26].

Table 5.4– ICP parameters used while varying the chamber pressure

ICP power: 1000W	**RF power: 200W**	**Cl_2:50sccm** **$SiCl_4$:15sccm** **Ar:12.5sccm**	**Temp: 20°C**

Gas flows:

The ratio of gases used in the process has a significant effect on the profile of the sidewalls. Thus different flow rates were studied to find the optimized gas ratio. The ratio of gas determines the selectivity between the mask and oxide layer, the etch rate and the profile of the sidewalls. Table 5.5 shows that the remaining parameters that were kept constant.

Firstly, Argon was varied from 5sccm to 25sccm. At 5sccm, the sidewalls were found to be rough and the measured sidewall angle was 138.7°±2°. At 12.5sccm, the sidewalls were found to be polished and the sidewall angle was 141.3°±2°. At 25sccm, the angle improved to 126°±2°, but deposition of contaminant residues were found on the surface. Hence the best profile was given by 12.5sccm of argon.

$SiCl_4$ was varied between 5sccm and 30sccm. The maximum allowed SiCl4 flow rate is 30sccm. At 5sccm, the angle was found to be 151.1°±2 while the metal protected was also etched away and spike like roughness was also caused. This means, this recipe was less selective for the resist but was found to be selective towards silicon dioxide layer. Between 15sccm to 30sccm, the profile angle was not affected but the 15sccm gave most selectivity as well as more polished sidewalls. Optimized flow rate for $SiCl_4$ was found to be 15sccm.

Chlorine gas flow was also varied between 15sccm and 50sccm (maximum allowed flow rate). At 15sccm the selectivity was found to be very poor towards both resist and silicon dioxide. Most of the resist-protected metal was etched away leaving behind rough metal. The oxide was etched by ~300nm. At 25sccm the profile angle increased to 159.1°±2 but was found to be selective towards the oxide layer. At 35sccm the selectivity for silicon dioxide and resist was found to be poor (a similar effect to 15sccm). 50sscm flow rate gave a better profile (profile angle of 141.3°±2) as compared with other flow rates and gave a very selective etch.

Table 5.5–ICP parameters used while varying the gas flows

ICP power: 1000W	**RF power: 200W**	**Pressure: 5mTorr**	**Temp: 20**°C

ICP power and RF power:

ICP power controls the plasma (ions) density present in the chamber whereas RF power is applied to the wafer electrode and it controls the energy with which ions strike the substrate [26]. In other words, ICP power controls ionization occurrence. As ICP power increases, the number of

ions present in the plasma will also increase. In turn, this will increase chemical (vertical and lateral) as well as physical etching. As physical etching increases the process becomes less selective and will etch away the mask much faster. This will also slow the passivation of the sidewalls (for sidewall protection) [27] and increases etch rates. If ICP power is first considered, figure 5.28 shows the graph of profile angle versus the ICP power. ICP power was varied between 700W and 1400W. A polynomial fit was used for the graph as there is an error of ±2° while measuring the angle. Up to 1200W, the selectivity was found to be good towards the resist and the increase in number of ions with increasing ICP power improved the profile. Varying ICP power had no impact on the selectivity towards the oxide layer. The profile was found to be very smooth (polished) between 700W and 1000W. At 1200W, the sidewalls were not smoothened but produced roughness of the metal with a sidewall angle of 113.3°±2°. At 1400W, the selectivity towards the mask caused an increase in roughness and the sidewalls were found to be jiggered. Hence, the maximum threshold as well as the optimized profile was found to be at 1200W.

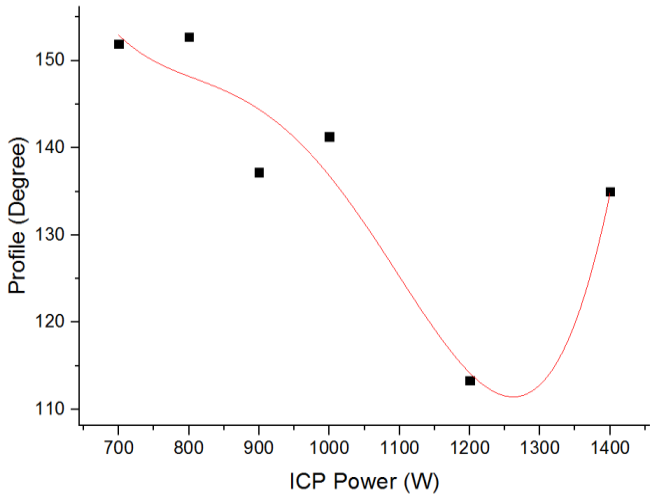


Figure 5-28– Graph showing the profile angle versus the ICP power using ICP with polynomial fit

RF power increases the electric field between the electrode and the plasma which means that more energy will be given to the ions which in turn increases the milling effect [27]. RF power was varied between 30W and 200W. At 30W grass type structures were found between the gaps of metal signal and ground planes while the sidewalls were still angled. At 30W, insufficient milling was observed. At 100W and 150W, the etching was very high and random. The only acceptable etch was found to be at 200W RF power.

As the result of varying all the parameters, the optimal recipe using $SiCl_4$ and Cl_2 was found and is presented in table 5.6. The etch obtained using this recipe can be seen in figure 5.29.

Table 5.6– Optimised recipe for Al using Argon, $SiCl_4$ and Chorine

ICP Power: 1200W	**RF power: 200W**	**Pressure=5mTorr**	**$SiCl_4$ =15sccm** **Cl_2=50sccm** **Ar=12.5sccm**	**Temp: 20°C**	**Etch time:3min for 1000nm Al**

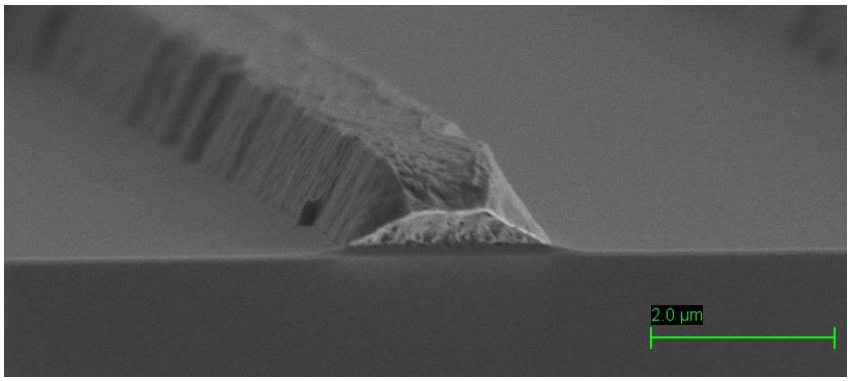


Figure 5-29– SEM image of the profile achieved using optimum recipe.

As seen earlier, using Cl_2/HBr to etch aluminium gave a very good profile angle but nano pillars were found between the metal's gaps whereas Cl_2/ $SiCl_4$ got rid of pillars and gave a very selective etch but had an angled side wall. The best angle achieved was found to be 113.3°±2°. As a result, a 2 step etch was considered which utilized both recipes. As the first step Cl_2/ $SiCl_4$ was used for 1 minute to ensure the breakthrough of aluminium oxide and to scavenge moisture. As the main etch step, Cl_2/HBr recipe for 4 minutes was used to achieve straight sidewalls. This resulted in a vertical profile. Figures 5.30 (a) shows SEM image of the two step etch while in (b) a close up image shows the measured profile angle (99.4°±2°). Figure 5.30 (c) and (d) (close up) show the metal etch on modulator by CEA LETI for comparison. As a result of this experiment, the Al etch of industrial standard was achieved.

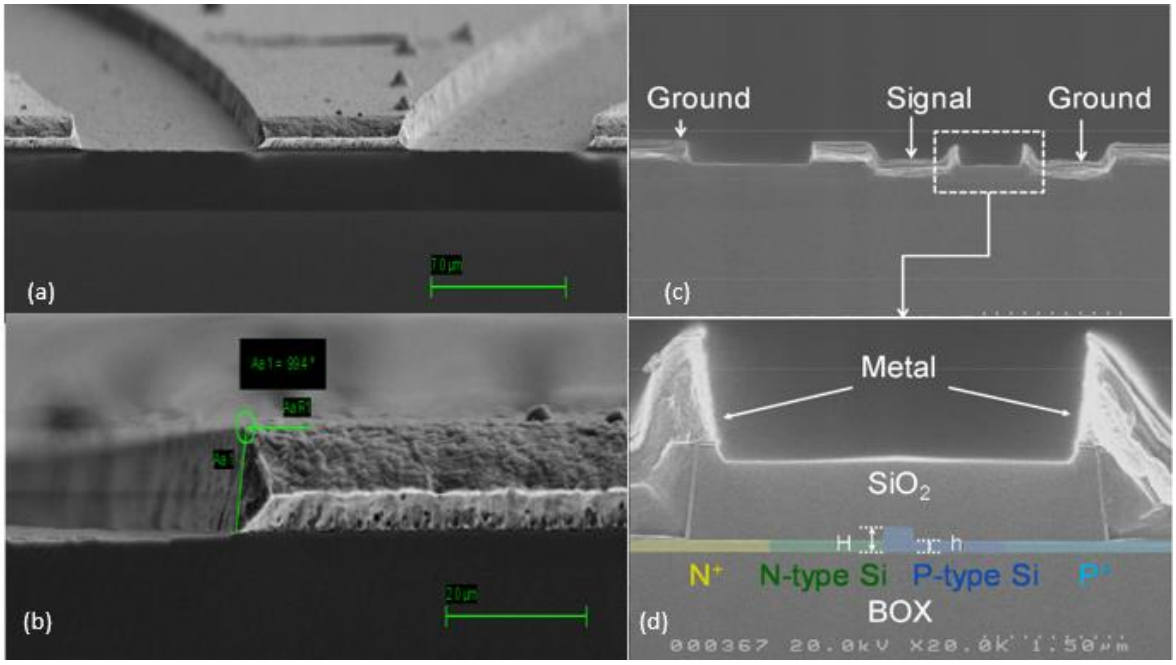


Figure 5-30– (a) and (b) shows the SEM image of the profile for 2 step etch and (c) and (d) shows SEM image of metal etch by CEA LETI

5.5 Slow wave electrode

The slow wave electrode structure was fabricated on the slow wave modulator to reduce the mismatch between the optical and electrical velocity. Figure 5.31 shows a slow wave modulator top view where the electrode metal layer is visible. This was fabricated by CEA LETI (fabrication foundry) and was used as a starting sample.

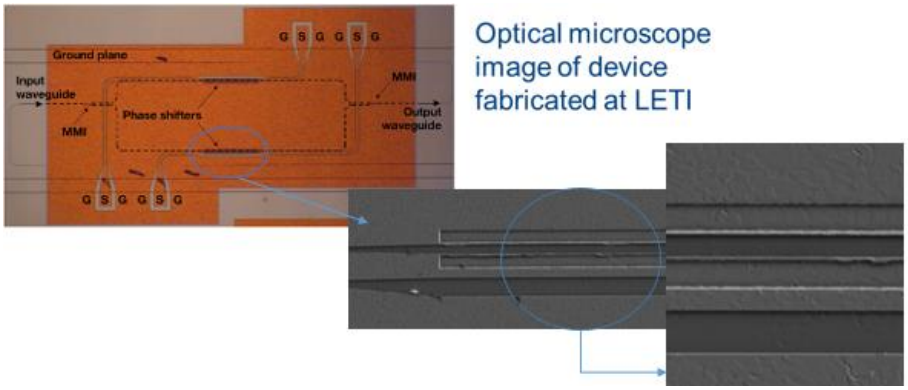


Figure 5-31– Slow wave modulator

An overview of the fabrication steps required for slow wave structure for electrodes is shown in Figure 5.32. First a silicon dioxide layer (image 2, figure 5.32) was sputtered onto the slow wave modulator using a Leybold Helios sputtering tool. The deposition rate for silicon dioxide has already been discussed in section 5.2. Different thicknesses of silicon dioxide were chosen and sputtered on various samples to change the slowing down factor. An aluminium layer was then

sputtered using the same tool with a thickness of 1µm. Next photolithography was performed to transfer the pattern onto the sputtered metal followed by a metal etch to form the floating corrugated slow wave structures. The same procedure for silicon dioxide was then followed and silicon dioxide was wet etched to expose the probing pads. The discussion on the study of wet etching of the sputtered silicon dioxide layer can be found in section 5.4. Figure 5.32(images 6) shows the microscopic image of slow wave structure on top of phase shifter after fabrication.

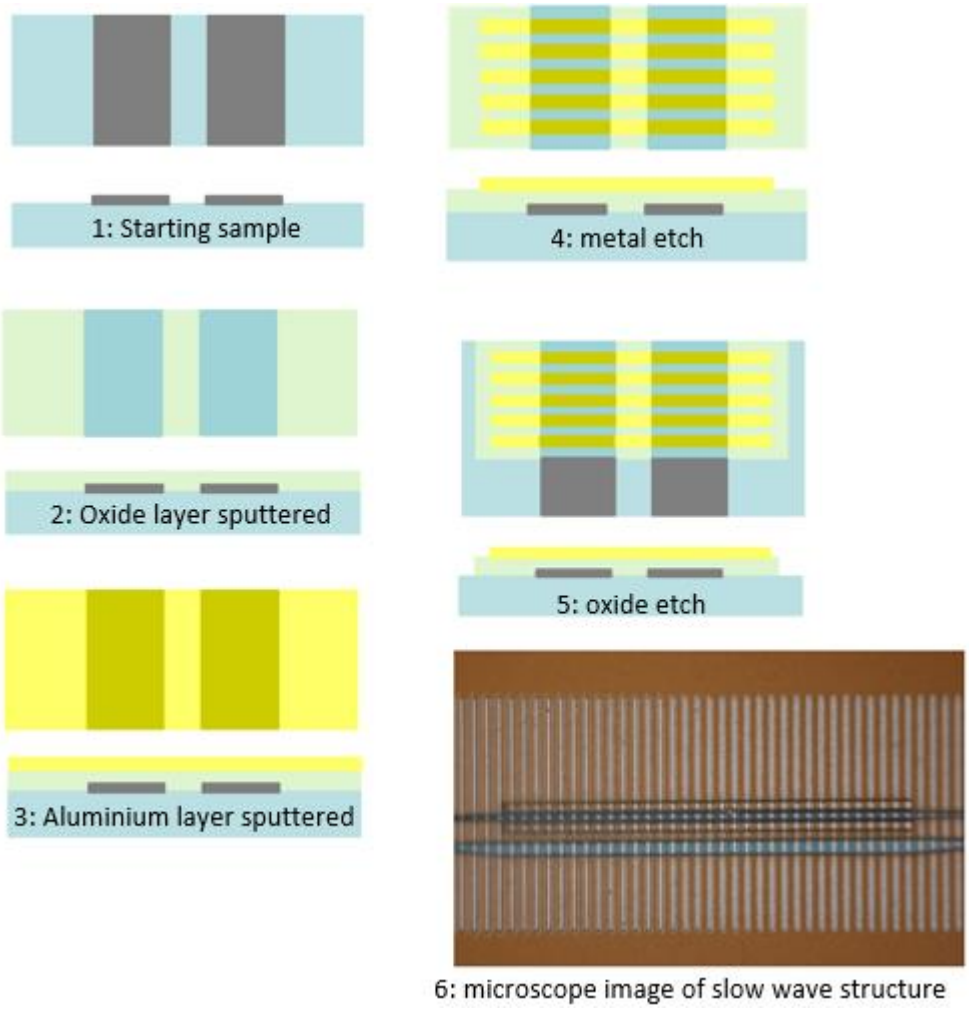


Figure 5-32– Fabrication process for slow wave electrode

Sputtering method was adapted to achieve conformal step coverage as shown in figure 5.33.

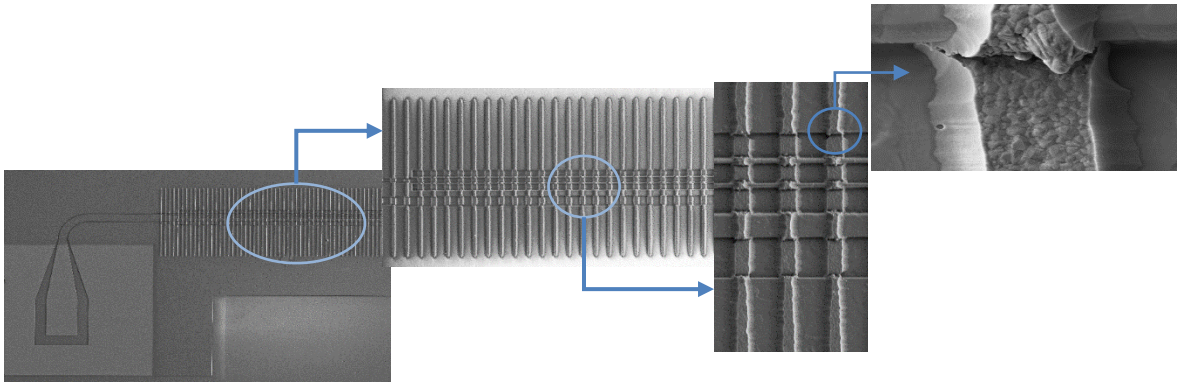


Figure 5-33– SEM image of the fabricated slow wave structure for electrode

Successful fabricated devices were achieved for characterization as a result of three different process flows. These consisted of fabrication of slow wave structure for electrode on top of slow wave modulator and the other two processes were carried out on silicon wafers. As a result of fabrication, the optimized recipe of aluminium was achieved as well as the Al surface morphology was also studied with the aim of improving it. The next chapter will go through the characterization of the devices fabricated, which includes bends, tapers, electrodes and slow wave structure for electrode.

References

[1] S.P.Morgan, "Effect of surface roughness on eddy current losses at microwave frequencies," J. Applied Physics, vol.20, Apr.1949, pp. 352-362

[2] E. Hammerstad and O. Jensen, "Accurate models of computer aided microstrip design," IEEE MTT-S Int. Microw. Symp. Dig., May 1980, pp. 407-409.

[3] S. Groisse, I. Bardi, O. Biro,K. Preis, and K. R. Richter, "Parameters of lossy cavity resonators calculated by the finite element method," IEEE Trans. On Magnetics, vol. 32, no.3, May 1996, pp. 894-897

[4] A F. Horn, J W Reynolds and J C Rautio," Conductor profile effects on the propagation constant of microstrip transmission lines", IEEE Microwave Symposium Digest, 2010, pp. 868-871

[5] B. Cao Martin, C. J. Tracy, J. W, Mayer, and L. E. Hendrickson, "A comparative study of hillock formation in aluminium films", Thin solid films, vol 271, Dec 1995, pp. 64-68

[6] S-J Hwang, J-H Lee, C-O Jeong, and Y-C Joo, "Effect of film thickness and annealing temperature on hillock distributions in pure Al films", Science direct, vol 56, 2007, pp. 17-20

[7] K. Y. Wong, "Stress relieving by concurrent resputtering from deposited layer", US4891112A patent, 2 Jan 1990, pp.1-5

[8] K-H Jang, S-J Hwang and Y-C Joo, "Effect of Capping Layer on Hillock formation in thin Al films", Metals and materials international, vol. 14, no. 2, 2008, pp. 147-150

[9] http://web.stanford.edu/class/ee311/NOTES/Interconnect%20Al%20Slides.pdf Accessed on 03/04/2015

[10] T M B Masound, A Tarazona, E Jaberanasary, X Chen, G T Reed, G Z Mashanovich and H M H Chong, ' Hot-wire polysilicon waveguides with low deposition temperature' , Optical Letters, vol. 38, no. 20, 2013, pp.4030-4032

[11]Sami Franssila, 'Introduction of micro fabrication' John Wiley and Sons Ltd, 2004, pp. 103

[12]Sami Franssila, 'Introduction of micro fabrication' John Wiley and Sons Ltd, 2004, pp.107

[13]V Lindroos, M Tilli, A Lehto and T Motooka,'Handbook of silicon based MEMS materials and technologies', Elsevier Inc., 2010, pp.335-336

[14] V Lindroos, M Tilli, A Lehto and T Motooka,'Handbook of silicon based MEMS materials and technologies', Elsevier Inc., 2010, pp.334

[15] http://www.mmf.montana.edu/files/MMF/Aluminum%20Cl2%20Etch%20Recipe_0.pdf Accessed on 17/04/2015

[16] R.A. Levy. 'Microelectronic materials and processes', Kluwer academic publishers, 1989, 1st edition, pp.486

[17] J. W. Coburn and H F Winters, 'Plasma Etching-A discussion of mechanisms' Journal of Vacuum science and technology, vol.16, no.2, 1979, pp.391-403

[18] Daniel L Flamm and Vincent M. Donnelly, 'The design of plasma etchants', Plasma chemistry and plasma processing, vol. 1, no.4, 1981, pp.330

[19] A. J. van Roosmalen , J.A.G. Baggerman and S..J.H. Btrader, 'Dry etching for VLSI', updates in applied physics and electrical technology, Plenum Press, New York, 1991, pp.116

[20] Yoshi Nishi and Robert Doering, 'Handbook of semiconductor manufacturing technology',2nd edition, CRC Press,2008, pp.21-25

[21] Sami Fransssila, 'Introduction to Microfabrication', second edition, John Wiley & Sons, Ltd, 2010, pp.133

[22] P.F. Williams, 'Plasma Processing of Semiconductors, proceedings of the NATO advanced study institute, Kluwer academic publishers, 1997, pp.380

[23] Roland Levy, 'Microelectronic materials and processes, proceedings of the NATO advanced study institute, Kluwer academic publishers, 1989, pp.486

[24] V. M. Donnelly and A. Kornblit, "Plasma etching : Yesterday, today, and tomorrow," Journal of Vacuum science and technology A, vol. 77204, no. August, 2013, pp. 1–48

[25] D. S. Rawal, H. K. Malik, V. R. Agarwal, A. K. Kapoor, B. K. Sehgal, and R. Muralidharan, "BCl3/Cl-2-based inductively coupled plasma etching of GaN/AlGaN using photoresist mask," IEEE Trans. Plasma Sci., vol. 40, no. 9, 2012, pp. 2211–2220

[26] C. Welch, "Oxford Instruments White Paper Nanoscale Etching in Inductively Coupled", Plasmas Oxford Instruments White Paper," 2009

[27] M. Shearn, X. Sun, M. D. Henry, A. Yariv, and A. Scherer, "Advanced Plasma Processing: Etching, Deposition, and Wafer Bonding Techniques for Semiconductor Applications," Semicond. Technol., 2010, pp. 79–104

[28]D. M. Mattox, “Atomic film growth and resulting film properties: residual film stress”, Vacuum technology & coating, Society of vacuum coating, November 2001, pp.1-6

[29] K. Bordo, H-G. Rubahn, “Effect of deposition rate on structure and surface morphology of thin evaporated Al films on dielectrics and semiconductor”, Materials Science, vol 18, no.4, 2012, pp. 313-317

[30] K. Stewart, A. Cuevas, D. Macdonald, J. Williams: "Influence of copper on the carrier lifetime of n-type and p-type silicon", 11th Workshop on Crystalline Silicon Solar Cell Materials and Processes, 2001, pp.212

[31] M. J. Madou, “Fundamentals of microfabrication: the science of miniaturization”, CRC Press LLC, Second edition, 2002, pp.89-93

[32] G.L Vick and K. M. Whittle, “Solid Solubility and Diffusion Coefficients of Boron in Silicon”, Journal of the Electrochemical Society, 1969, vol 116, no. 8, pp.1142-1144

Chapter 6: MEASUREMENT AND DATA ANALYSIS

This chapter presents the measured results based on the simulated structures presented in chapter 4. Firstly, the measurement setup, calibration kit and the importance of calibration is discussed. Secondly the building blocks of the electrode and their responses are analysed. Subsequently, the better electrical performing electrode designs are shown in comparison with a design of Thomson et al.[3] and finally the results of the slow wave structure for the electrode will be presented.

6.1 Electrical measurement setup

All electrical measurements were carried using an Agilent Technologies PNA (Performance Network Analyser) E8361A with operating frequency range 10MHz-67GHz. PNA is capable of accurately characterize the electrical circuits by measuring the S-parameter (discussed in chapter 4) of the device under test (DUT). Nowadays, PNA comes with user friendly interface which allows easy control of measurement. However, external software can also be used to carry the measurement. In this case, WinCal XE 4.2 software is used to read data from the PNA and carry the measurements. In theory, the PNA should have a perfect load which implies there should be no reflection due to the load. If PNA has the perfect load then only PNA will reflect the true loss. Unfortunately, every system has losses and are not perfect hence the calibration is required to eliminate such losses which are not coming from DUT. The losses which needs to be calibrated out comes from setup, cables, probing station and imperfections of the PNA. PNA has an internal guided user interface to aid calibration but WinCal XE 4.2 can also be used for automated calibration. The WinCal XE 4.2 was used since it provides more flexibility in calibration, it ensures that the calibration provides repeatability each time, and checks the calibration against an acceptable/good range of values already present in the WinCal XE 4.2. The measurement carried out were wafer scale using a CASCADE MICROTECH (summit 12000B) probing station (as shown in figure 6.1) controlled by Nucleus automated software. Nucleus controls the microscope, wafer stage and the vacuum to hold the wafer/DUT in place. On wafer measurement requires the use of the probes which are placed directly on the wafer to characterize the DUT. Hence, CASCADE MICROTECH infinity ground-signal-ground (GSG) probes with 100µm pitch were used to carry the on wafer measurement.

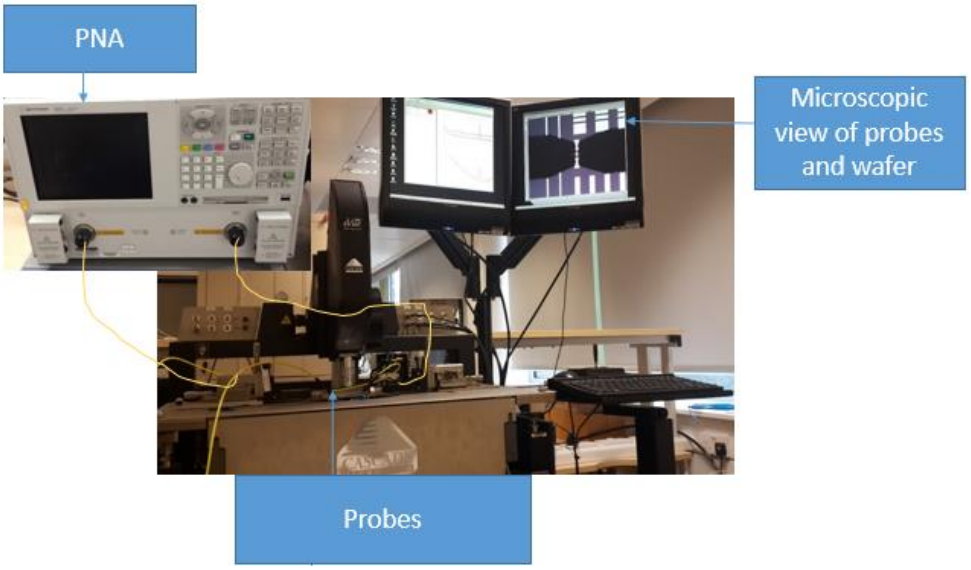


Figure 6-1– PNA network analyser E8361A setup used for measuring S parameter.

6.2 Calibration

To reflect the loss due to the device under test (DUT), calibration is carried out which eliminates the losses contribution due to the setup. The calibration takes places where the calibration standards are added. The calibration will establish a reference plane where the standards are added. This means all the losses up to the reference plane will electrically be removed and the PNA measurement will reflect the losses between the reference planes. Figure 6.2 shows block diagram of the setup where fixture A represents cable and probe so does the fixture B.

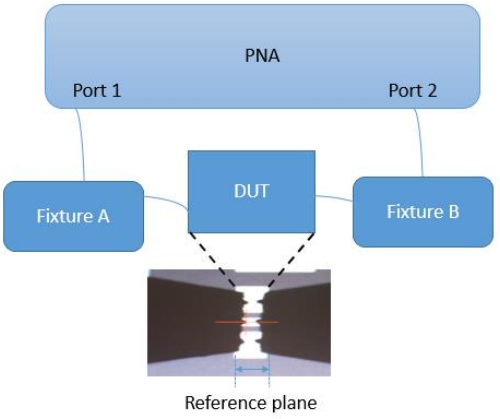


Figure 6-2 – Block diagram shows the reference plane

The PNA was calibrated using a CASCADE MICROTECH impedance standard substrate. The PNA is characterized by measuring the known calibration set (such as short, open, through and load)

following which the error terms are eliminated mathematically by the PNA to reflect the response of the DUT. The full 2-port calibration was carried out so that all S parameters (S21, S12, S11, and S22) were calibrated. The full 2-port calibration is highest in accuracy as compared to one port calibration as it removes the directivity error, source/load match error, reflection/transmission matching error and cross-talk. Whereas, calibrating one port only corrects the reflection measurement on one port where the calibration is carried out. The type of calibration which can be carried out using the impedance standard substrate or on-wafer calibration are LRM (thru-reflect-match), LRRM (thru-reflect-reflect-match), SOLT (short-open-load-thru), TRL (thru-reflect-line) and SOLR (short-open-load-reciprocal). When carrying the calibration, special care has to be taken as the calibration is sensitive to probing locations hence it is important to verify the calibration with respect to repeatability and reproducibility.

TRL calibration was developed by NIST (National Institute of Standards and Technology) in 1979 [1]. LRRM and SOLT use a pair of 50 Ohm resistors to define the impedance of the line whereas in TRL the characteristic impedance is defined by a set of coplanar lines of different lengths. The TRL calibration method is based on transmission line calibration standards which includes non-zero length thru or zero length thru, reflection (short and open) and three line standards. The thru standard needs to have a different length to the line standards where electrical length is well defined. This will set the reference plane, and the characteristic impedance will be worked out from the thru and line standards. Wider bandwidth calibrations require more than one line standard and the overlap of each line's bandwidth to ensure calibration accuracy at bandwidth edges. For example minimum of three Line standards are required to cover the whole frequency range 10GHz to 40GHz. This is discussed further in the design of TRL standard.

The optimum LINE standard is 90° (λ/4) of insertion phase at the centre frequency relative to the thru standard. The difference between line and thru standard should be between 20° to 160° and should not be 180° (λ/2) with respect to each other. The allowed electrical length difference over the frequency range is 20° to 160°. Hence, 90° represents the centre electrical length which should be used at centre frequency. This allows to carry the calibration over maximum frequency range using Line standard. If the difference is 180° between thru and line, the phase information will be similar and it will behave as a non-zero line or an open. The reflect standard can be either an open or a short, but an open has the advantage that it operates over a wider bandwidth range for probes [4]. The same reflect (open or a short) should be used for both ports. The reference impedance (Z_O) value is defined by the thru, match and the line standard and the value is entered into the system. Reflection is defined by Reflect (short or open) and the delay value is also entered into PNA.

Chapter 6

Design of the optimal length for the TRL standard:

The geometrical mean will give the breaking frequencies for designing the line standards. For a 10GHz to 40GHz frequency range, the geometrical mean=$\sqrt{f_1 f_2}$=20GHz. For a 20GHz to 40GHz frequency range, the geometrical mean=$\sqrt{f_1 f_2}$=28.28GHz. Thus three lines standards will be required for calibration of 10GHz to 40GHz frequency range. Then the centre frequencies are found for the three lines as follows:

10GHz – 20GHz Centre frequency =15.00GHz,

20GHz-28.28GHz Centre frequency=24.14GHz,

28.28GHz-40GHz Centre frequency =34.14GHz

The coplanar waveguide dimensions were found using the LineCal by Agilent technologies to give characteristic impedance Z_o (50Ω) suitable for on wafer calibration using 100GSG probes. The coplanar waveguide dimensions found were Gap (G) =35.0µm, Width=52.8µm where metal Thickness (T) is equal to 2µm and the Height (H) of the substrate is 675µm.

Now the physical length is worked out at the centre frequency for the electrical length to be equal to the optimum length of 90° (λ/4). So at the central frequency (15GHz), for an electrical length=90° the physical length is 2013.8µm. Further calculations are made to make sure that the whole frequency range is between 20° to 160°. In the case where the central frequency is equal to 15GHz, the frequency range it should cover is from 10GHz up to 20GHz. The wavelength is first worked out and then the phase change at lower frequency and upper frequency to see the frequency range is between 20° to 160°.At 10GHz, λ_g = 12083.0µm and at 20GHz, λ_g = 6041.5µm. Therefore the phase change at the frequency range can be worked out using $\emptyset = \frac{360°l}{\lambda_g}$. At 10GHz, the phase change =60° and at 20GHz, the phase change= 120°. The same method is adapted for other two line. For a centre frequency equal to 24.14GHz when the electrical length =90°, the physical length is equal to 1251.5µm. At 20GHz, λ_g = 6041.5µm and at 28.28GHz λ_g is equal to 4272.6µm giving phase change equal to 74.6° and 105.4° respectively. At 34.14GHz for an electrical length =90°, the physical length is equal to 884.8µm. At 28.28GHz, λ_g = 4272.6µm and at 40GHz λ_g is equal to 3020.7µm giving a phase change equal to 74.6° and 105.5° respectively. The frequency ranges for all three line standard

satisfies the condition mentioned above which is the phase change is between 20° to 160°. Figure 6.3 show the mask design and fabricated TRL calibration set.

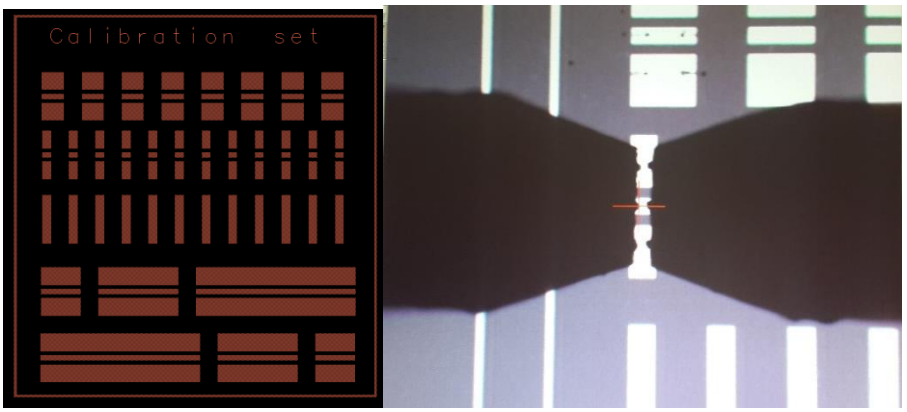


Figure 6-3–Left: The mask design for TRL calibration set, Right: the image of TRL calibration set under measurement

TRL calibration is well suited for on-wafer calibration. This is because the TRL standards are very simple and requires only one metal layer only and does not require any resistors to be mounted. The primary drawback of TRL calibration is that it is bandwidth limited. It is also not a redundant standard which means only one standard is used to define the impedance resulting into errors caused by metal contact repeatability. Hence more care is required during calibration in order to achieve repeatability.

SOLT is the most commonly used calibration. It is a simple, redundant standard (uses more than one standard to define impedance) and is not bandwidth limited, however, it requires very well defined standards. Thus SOLT is more suitable if calibration is carried out with a highly accurate impedance standard for example the CASCADE MICROTECH impedance standard substrate (ISS) which is used in this work.

For boarder frequency ranges, SOLT calibration was carried out with an automated calibration process using the Auto-Cal option available on WinCal. SOLT showed better repeatability compared to LRRM in the comparison carried out by Safwat and Hayden of CASCADE MICROTECH [2]. The reproducibility was better for LRRM when compared with SOLT. This is due to relatively high sensitivity to the probe position in the case of SOLT that is a consequence of parasitic inductance and capacitance. Parasitic inductance arises due to the short and the load, whereas parasitic capacitance is due to the open circuit. These values are given by the manufacturers of probes and ISS and they are used for more accurate calibration. Table 6.1 shows the maximum measurement error carried out by CASCADE MICROTECH for the frequency range 0.4GHz - 40GHz [2].

Table 6.1–maximum errors bound for SOLT and LRRM between 0.4GHz - 40GHz (reproduced from [2])

	LRRM (dB)	SOLT (dB)
Repeatability(measurement system drift only)	0.0048	0.0032
Reproducibility (probe realignment)	0.014	0.033
Load (≈25µm change in overlap)	0.014	0.052
Short (≈25µm change in overlap)	0.01	0.14
Thru delay (0.1ps change in definition)	0.025	0.028
Open (Probes in air vs open pads)	0.05	0.75

This measurement (table 6.1) suggests that LRRM is a better calibration in comparison to SOLT over the required frequency range (100MHz-40GHz) as LRRM gives lower error bound. The uncertainty in the SOLT calibration data is associated with the sensitivity of SOLT to probe positioning [2].

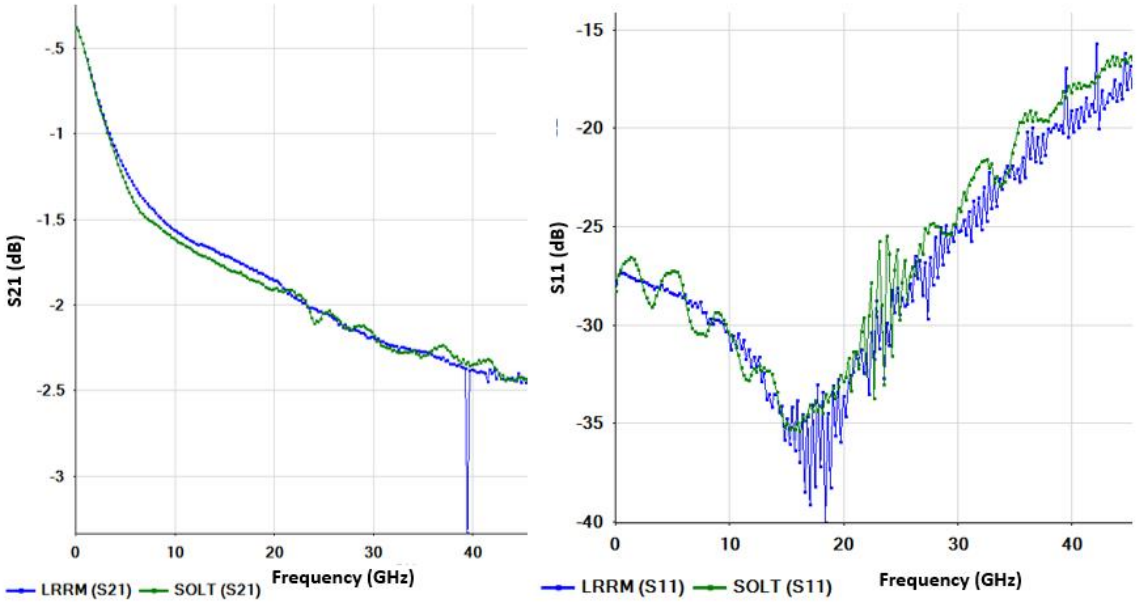


Figure 6-4– Measurement results of same line measured under LRRM and SOLT calibration settings

Nevertheless, SOLT calibration carried out by the author showed 0.02 dB thru line error at 67GHz and 0.017 dB thru line error at 40GHz which is much lower than that found by CASCADE MICROTECH.

For the LRRM calibration the thru line error was found to be 0.12 dB at 67GHz and 0.1 dB at 40GHz. The nominal difference was found by comparing measurement results up to 40GHz of the same transmission line under SOLT and LRRM calibration. The author found both SOLT and LRRM to be competitive up to 40GHz in overall measurement results (figure 6.4). SOLT shows fluctuations after 20GHz whereas LRRM gives much smoother response.

6.3 Bends

This section contains the experimental results obtained from different electrode bend designs discussed in chapter 4. It will first look at experimental results for the thick bend and later the thin bend will be analysed and the best bend will be suggested to be used for the modulator electrode design. Mitre edged, square and rounded bend structures with a different number of bends were compared with a straight electrode of equivalent length. The simulation results (chapter 4) of the bends for the thick bend (signal=60µm gap=35µm) showed no loss due to the bend wil be added to the electrode. Whereas the simulation result for the thin bend (signal=3 µm gap=5 µm) demontrated loss will be added due to the bend. The round bend gave the highest loss whereas mitred bends showed insignificant loss (refer to section 4.3).

Let us first consider thick bends. The measured S21 and S11 results for the thick mitred, square and round bend loss are shown in figure 6.5. For each bend type, structures which have a different number of the bends are measured together with straight coplanar lines of equivalent length for comparison. The notation used is ‘4BND’ stands for 4 bends and ‘4STR’ stands for equivalent length of straight line throughout this section. The measured result shows the same trend as the simulated results in that negligable loss was added due to the thick bend (figure 4.7,section 4.2) . In addition no significant reflection loss due to the thick bend was seen.

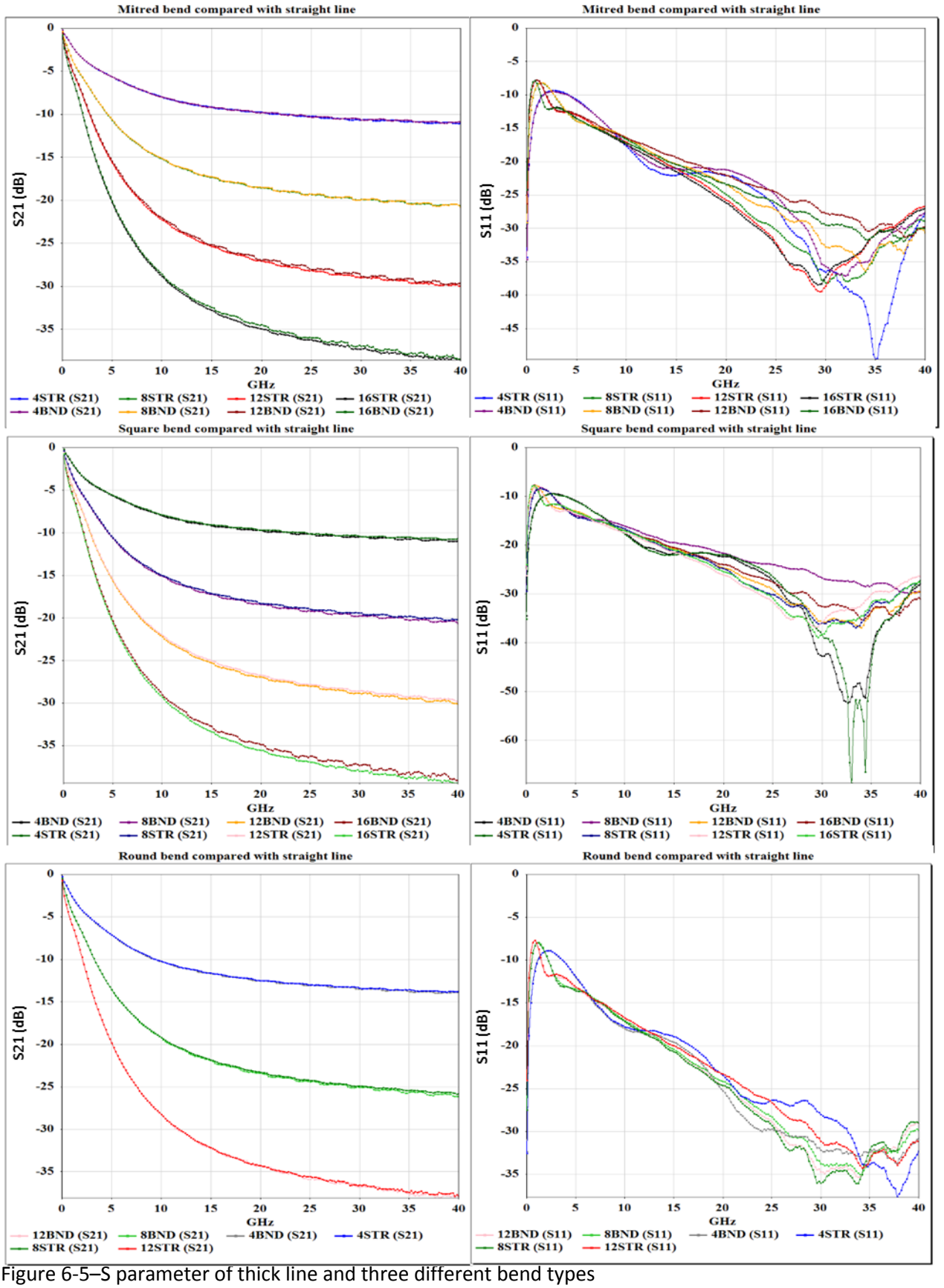


Figure 6-5–S parameter of thick line and three different bend types

Now consider thin round bend and the measurement results for round thin bend is shown in figure 6.6. The reflection loss (S11) was below -13dB for the whole range of structures as evident from the right image of figure6.6, denoting an overall good impedance match. The insertion loss per bend is very low. For example, in the case of 4 bends; the loss at 40GHz is 0.2dB, which is 0.05dB per bend the loss per bend would works out to be ~1% loss of the signal due to the bend. This loss is due to some signal reflected back at the bend.

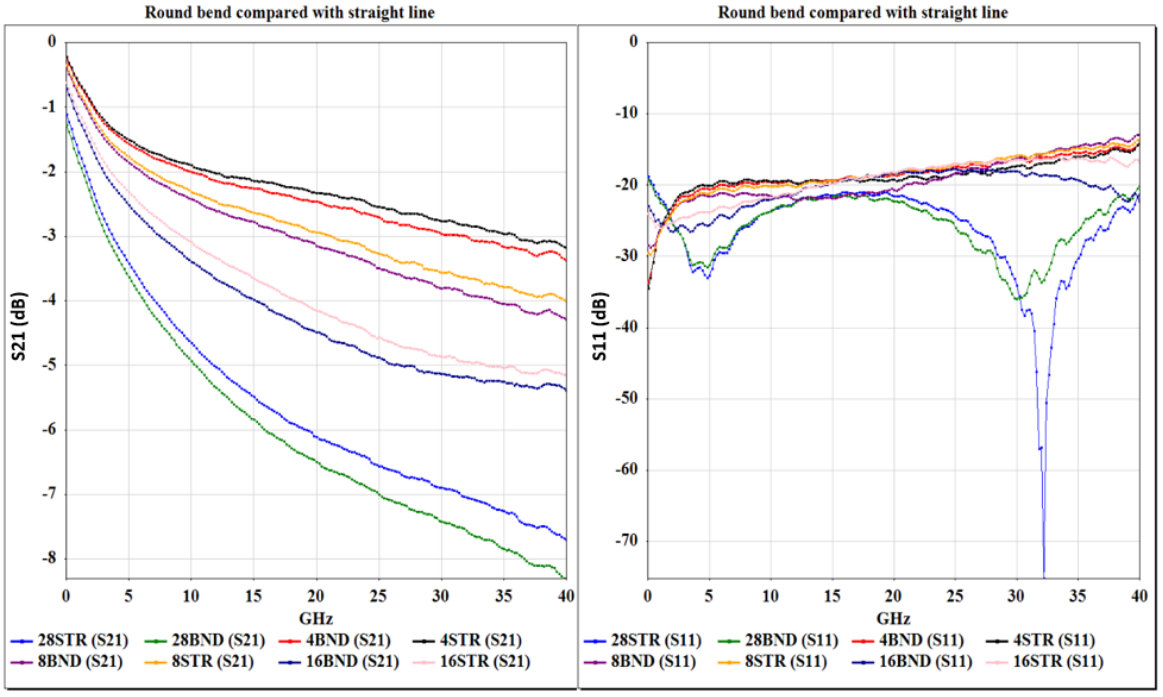


Figure 6-6– Left: insertion loss (S21) of thin round bend and straight line Right: Reflection loss (S11) of the same structure.

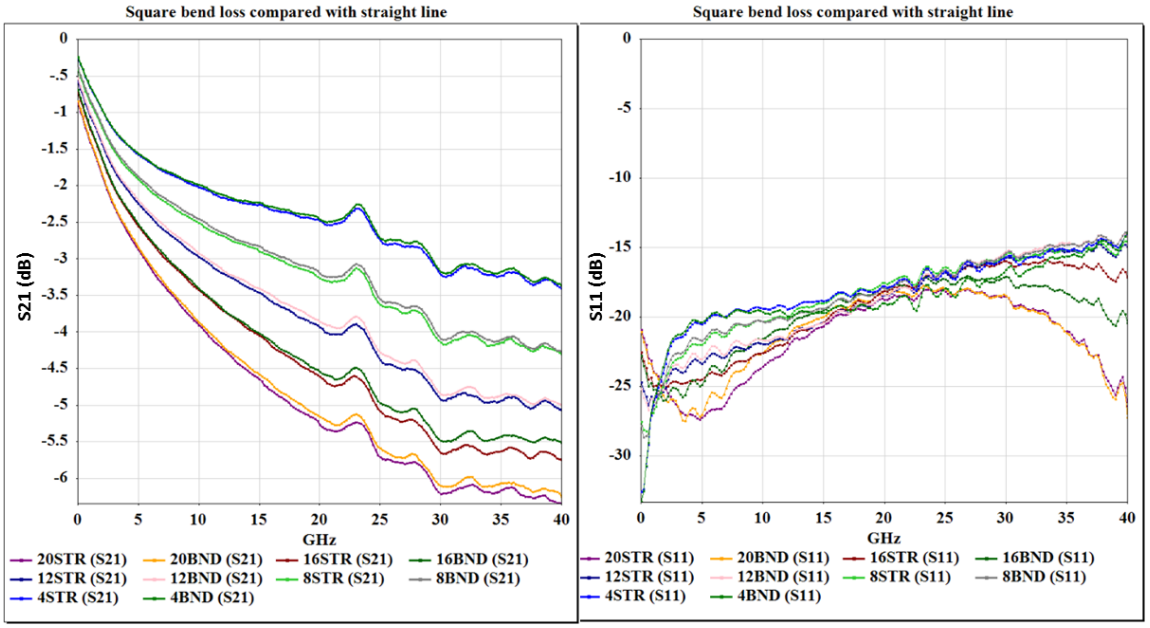


Figure 6-7– Measurement results comparing the square bend with straight lines of equivalent length. S21 (left) and S11 (right)

The measured S21 and S11 for the thin square bend are shown in figure 6.7. The square bend results show that practically no loss due to the bend was added to the the transmission loss upto 12 bends. For example 4 Bends (4BND) and equivalent straight line (4STR) shows overlap for the transmission loss (left graph in figure 6.7).The negligible loss observed for 16 bends (giving the loss of 0.01dB/bend) and 20 bends (giving the loss of 0.0075dB/bend). Since the measurement was carried out on even number of bends oriented in the opposite direction due to which the path difference effect is cancelled out giving virtually no loss. The reflection loss (right image figure 6.7) is measured to be below -14 dB for the whole range which indicates the good impedance match. The ripple effect was observed above 20GHz, is due calibration sensitivities towards the equipment discrepancies. Even a slight change in temperature will change the impedence of the cables, and at higher frequencies this change becomes more evident thus the ripple effect occurs in the results.

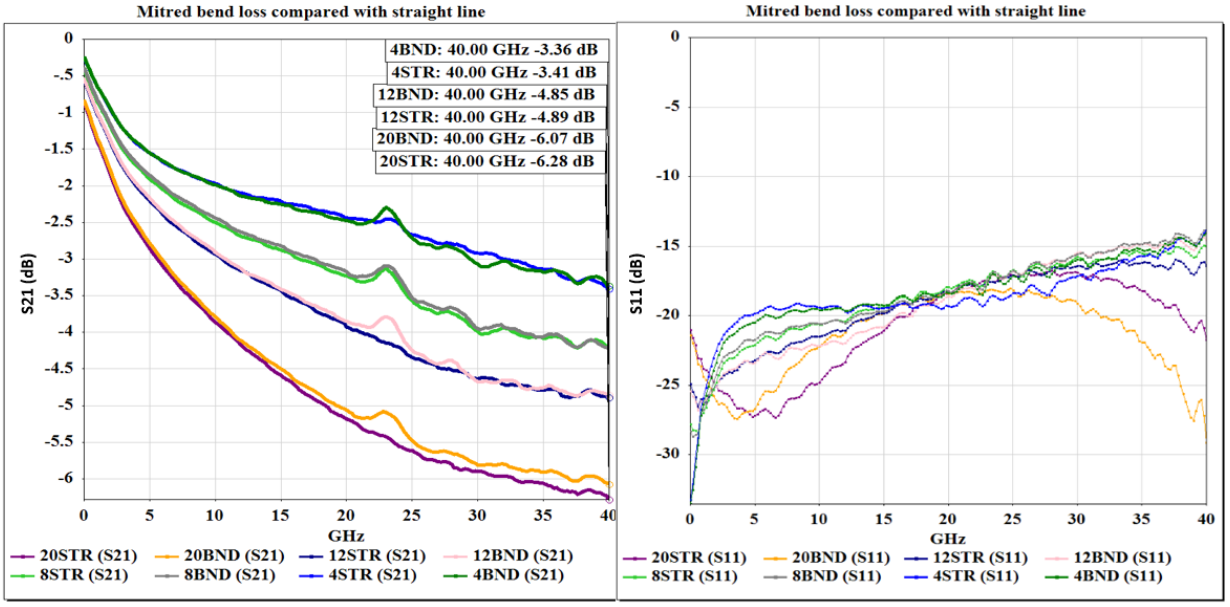


Figure 6-8– Measurement results comparing the mitred bend with straight lines of equivalent length. S21 (left) and S11 (right)

The measurement result for the mitred bend loss compared with a straight coplanar line is shown in figure 6.8 which also indicates virtually no additional loss is caused due to the bend. Overall, good overlap between the bend and straight coplanar line for the complete frequency range can be observed. Again the ripple effect can be observed. The measured results indicate that the bend will not add significant loss when the number of bends is reasonably low (for example in a typical modulator electrode just 2 bends are used). At higher frequencies, the loss due to the bends becomes more evident and with the increasing number of bends. In the case of 2 bends for the electrode design up to 40 GHz, the bend would not add signifcant loss further to the length of transmission line required to form the bend. The reflection loss for mitred bends are below 14dB for the whole frequency range.

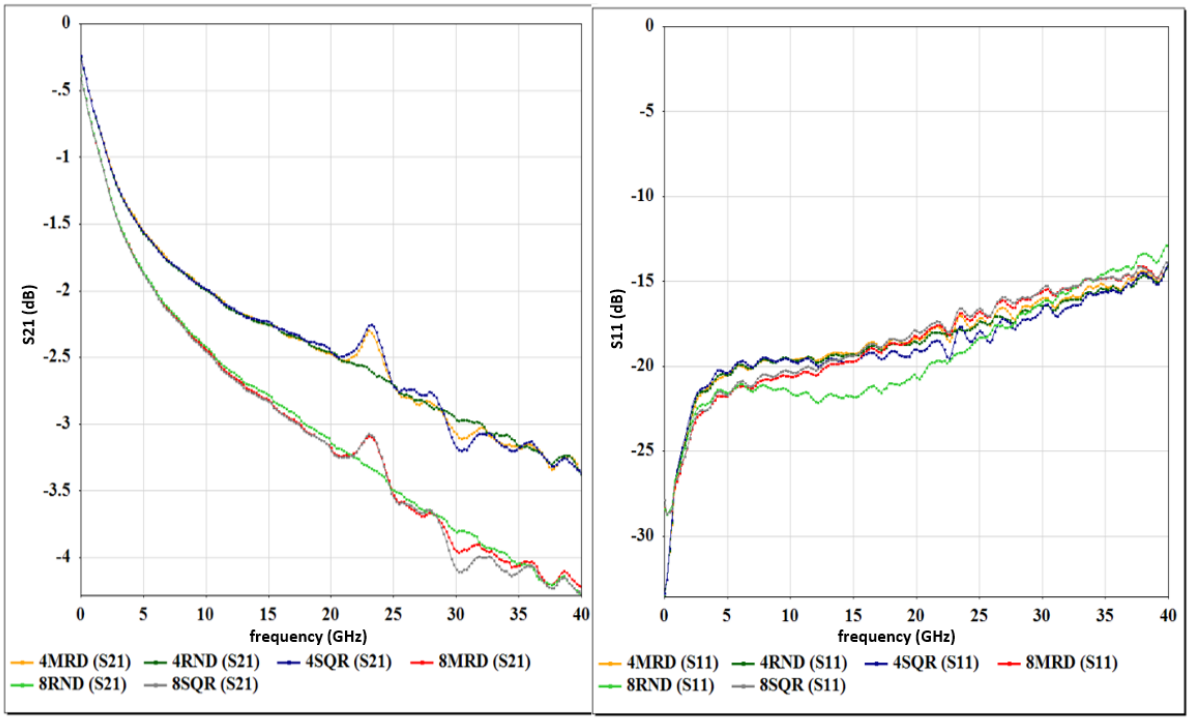


Figure 6-9– Measurement results directly comparing three types of bends S21 (left) and S11 (right)

The figure 6.9 shows S parameters of mitred, round and square bends allowing a direct comparison, where '4MRD' stands for 4 mitred bends, '4RND' stands for 4 round bends and '8SQR' stands for 8 square bends. The loss due to the bends upto 40GHz has been measured. The bends do not cause any impedance mismatch thus no significant reflection was observed. At this scale, no loss due to the bend is visible upto 12 bends and has negliable contribution when the number of bends is increased beyond 12 bends.

Table 6.2 compares all different bends considered in this project. If the comparsion is drawn between rounded thin and rounded thick bend then the loss per unit length is found to be lower for the rounded thick bend. This is because the thick line is less resistive hence the loss due to resistivity of the coplanar line is lower. This is also the case when mitred thick is compared with mitred thin and square thick with square thin. However when the loss per bend is calculated the loss per bend for the thick bend is significantly higher than thin bend as the thick bend requires much longer line. Therefore it can be concluded that the type of bend will have no impact on results as long as an even number of bends oriented in opposite direction is used and the thin line bend would be preferred as this will require shorter additional length so the loss per unit length and the footprint will be kept low.

Table 6.2– Summary of measured results of different bend type

Bend type	Number of bends	Total length (μm)	Loss/mm(dB)	Loss/bend (dB)	Loss at 40GHz (dB)	Peak reflection loss (dB)
Mitred thick	**4**	**4370**	**2.22**	**2.43**	**-9.71**	**-9.49**
Mitred thin	**4**	**1122**	**2.35**	**0.66**	**-2.64**	**-12.99**
Square thick	**4**	**4370**	**2.24**	**2.45**	**-9.79**	**-9.30**
Square thin	**4**	**1122**	**2.35**	**0.66**	**-2.64**	**-12.79**
Round thick	**4**	**5600**	**2.19**	**3.07**	**-12.29**	**-8.69**
Round thin	**4**	**1070**	**2.43**	**0.65**	**-2.61**	**-13.31**

6.4 Slow-wave structure

This section will go through the measured results of the slow wave electrode structure. The slow wave structure is used to match the velocity of electrical drive signal with the optical signal for slow light modulator. Figure 6.10 shows the SEM image of the slow wave modulator after slow wave structure was added to the modulator.

The optical response of the device is shown in figure 6.11 where the different regions of operation are clearly marked. The graph shows normalized power (dB) versus wavelength. Referring to the slow wave region, the group index of the device increases towards the bandgap. In other words, as the wavelength decreases in the slow wave region, the group index increases and the light matter interaction increases. As it moves to high group index region, the mismatch between the speed of the electrical signal and optical slow wave increases but by adding the slow wave structure of the electrical signal, this mismatch is decreased.

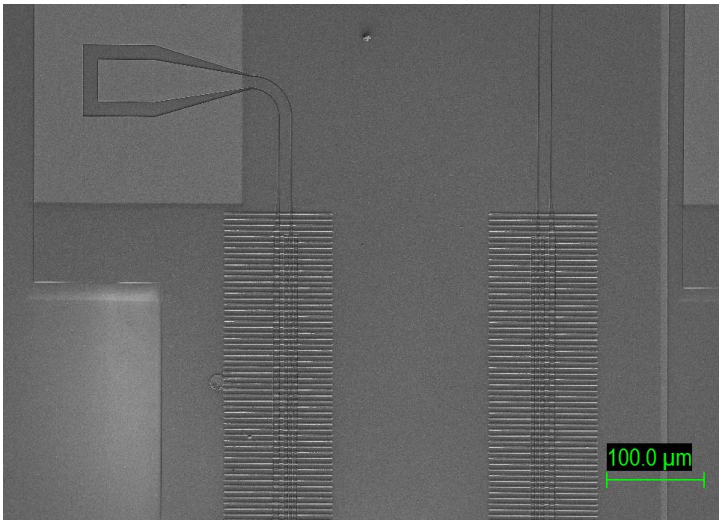


Figure 6-10 – SEM image of the slow wave modulator

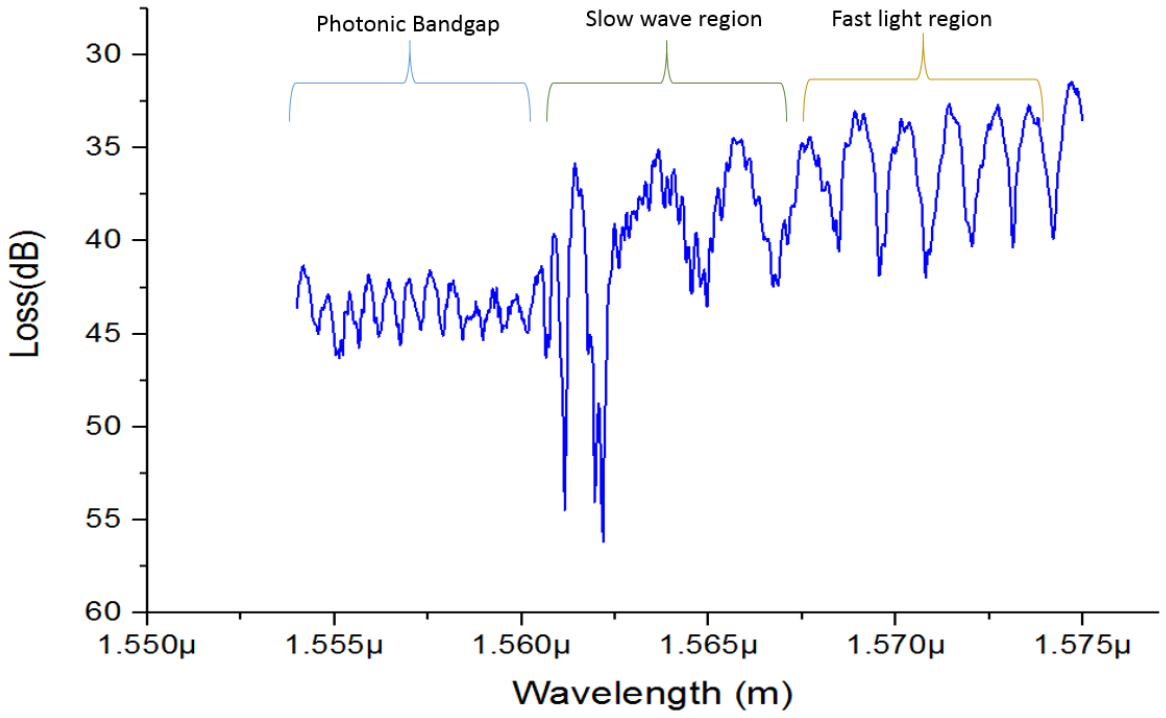


Figure 6-11– Normalized power versus wavelength

Initially, the slow wave electrodes were fabricated on a slow wave modulator with poor optical performance used as an initial analysis of electrical performance.

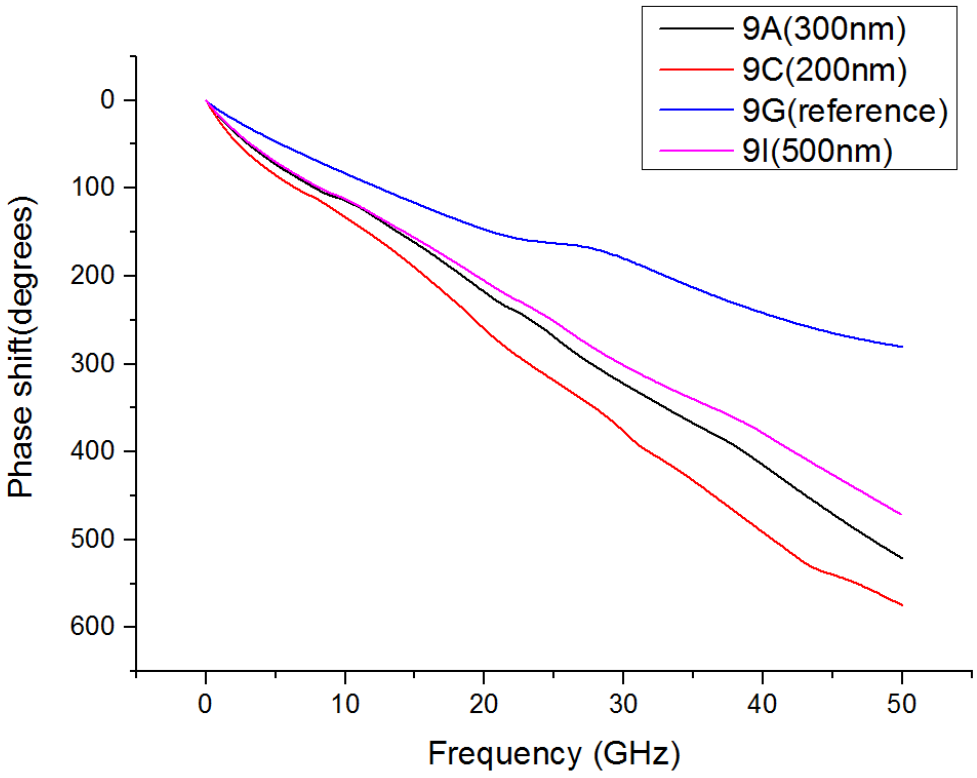


Figure 6-12– Measured electrical phase versus frequency for initial slow wave structure

The electrical phase of the slow-wave modulator of a 1mm long electrode was then measured (figure 6.12) and the velocity calculated and used as a reference (9G in figure 6.12). A phase of 284° was measured and the reference velocity calculation is therefore as shown below:

$$\lambda_g = L\left(\frac{360}{\emptyset}\right)$$

$$\lambda_g = 1000\mu m\left(\frac{360}{284}\right) = 1.27 \times 10^{-3}$$

$$v = f\lambda_g$$

$$v = 50G(1.27 \times 10^{-3}) = 0.63 \times 10^{8} m/s$$

The velocity of the 1mm long reference electrode was found to be $0.63 \times 10^{8} m/s$ at 50GHz. The slow wave structure was then fabricated on to the electrode. The slow wave electrical structure was formed of metal strips on top of a silicon dioxide layer which was

deposited on the original existing electrodes. The slowing down factor (capacitance) was controlled by varying the dielectric (silicon dioxide) between the existing electrodes and the corrugated metal strips. In the case of a 200nm silicon dioxide layer (9C in figure 6.12), for example, a phase of 558.4° was measured. The velocity from the electrical measurement is then,

$$\lambda_g = L\left(\frac{360}{\emptyset}\right)$$

$$\lambda_g = 1000um\left(\frac{360}{558.36}\right) = 6.45 \times 10^{-4}$$

$$v = f\lambda_g$$

$$v = 50G(6.45 \times 10^{-4}) = 0.32 \times 10^{8} m/s$$

Table 6.3– Calculated slowing down factor for different dielectric thickness from measured response

	Silicon Oxide thickness (nm)	Velocity (m/s) @50GHz	Slowdown factor @50GHz
Reference 9G	0	0.63×10^{8}	
9C	200	0.31×10^{8}	2.03
9A	300	0.35×10^{8}	1.8
9I	500	0.37×10^{8}	1.7

Table 6.6 shows calculated slowing down factors from the measured response. The measurement results show that the velocity changes from 0.63×10^{8} to 0.31×10^{8}. This indicates a slowdown factor of 2. The trend of measured results agrees with simulation results –i.e. a decrease in thickness of silicon dioxide, increases the slowing down factor (table 6.3) - but the simulation results suggest a

slowing down factor of 2.91 rather than 2. Only the active region of the electrode was simulated with simplifications made to the substrate due to limitations of the simulations software, which probably accounts for the discrepancy. The simulation run time was also decreased significantly by choosing this method. Considering all of the limitations of the software the measured results still gave reasonably good agreement with simulated result, both showing a significant improvement.

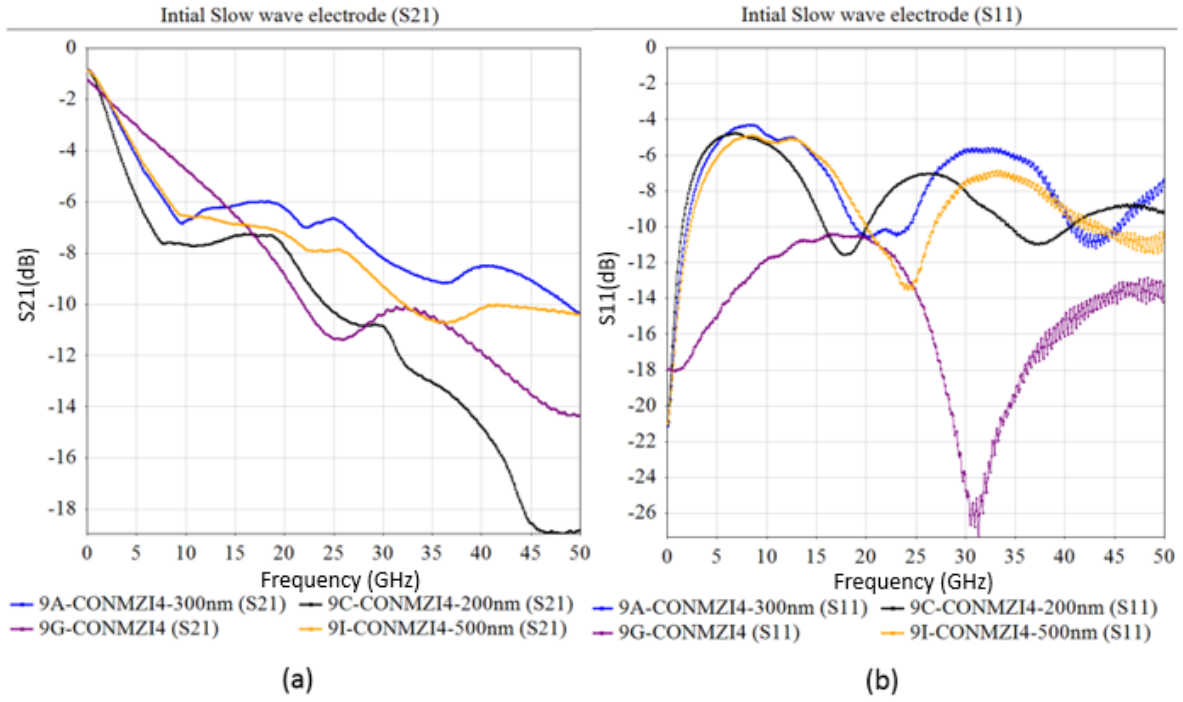


Figure 6-13– (a) measured S21 for initial slow wave structure (b) S11 for initial slow wave structure

Figure 6.13 shows the electrical measurement (insertion loss and the reflection loss) for the initial slow wave modulator where device 9G (purple curve) is the reference. The refection loss for the reference is below -10dB whereas the reflection loss for the slow wave electrode (shown in figure 6.13 (b)) has increased due to impedance match by added capacitance of the slow wave structure. However, looking at insertion loss presented in figure 6.13(a), device 9A gives transmission loss similar to reference device in spite of increased reflection loss. This is because, the substrate loss has been reduced as less electrical fields penetrates into lossy substrate.

After the electrical performance was verified via electrical measurement then optical measurements were carried out on slow wave modulator devices to find those which have optimal performance optically and also to determine the operating wavelength of the device. As a result, three further devices with good optical responses were selected for processing as final devices and electrical measurement was then conducted.

Electrical measurement of phase of the electrodes on the final devices are shown in figure 6.14. When the silicon dioxide thickness was 500nm a slowdown factor of 1.57 was calculated whereas the slow done factor measured on the initial fabricated samples was found to be 1.7 for 500nm. This implies that the fabrication of the slow wave structure has a very high impact on the slowing down factor. The metal strips of the slow wave structure were wet etched in the previous case whereas the later samples were dry etched which caused the difference in the measured results. The capacitance of the corrugated structure causes the change in phase of transmitted signal. A change in dimensions of corrugated structure will therefore cause a change in capacitance. The width and thickness of the metal strips of the corrugated structure are 2µm. The wet etching process is isotropic and therefore undercuts the mask thus changing the effective width of the metal strips. The dry etching process is largely anisotropic and therefore the width of the features is largely retained. The difference in the etching profiles of the metal strips can explain the different in phase change.

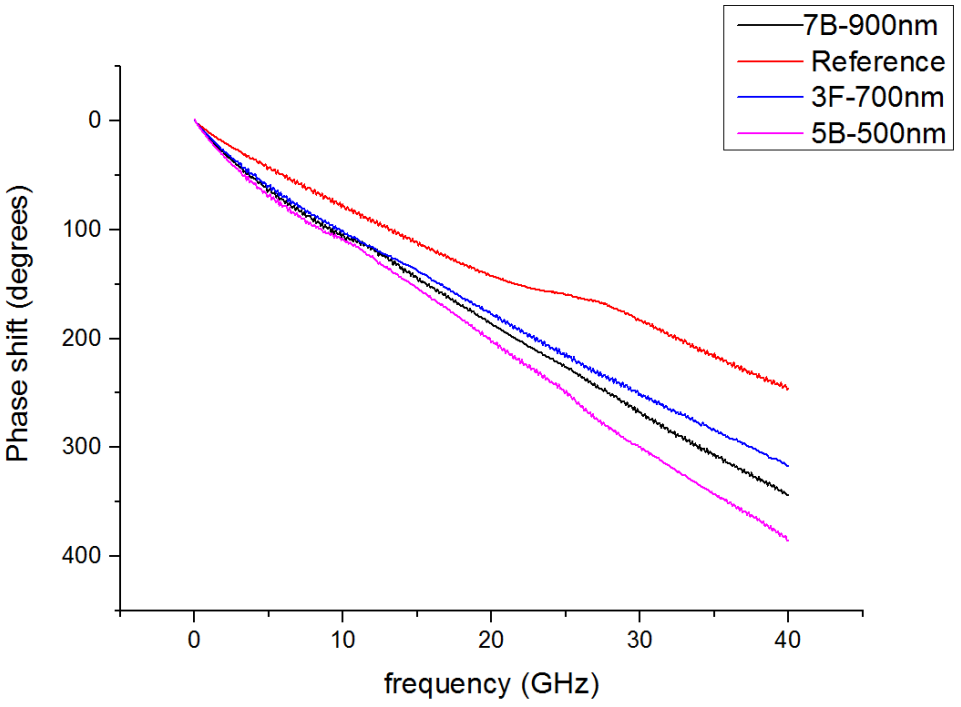


Figure 6-14– Measured transmission line phase for slow wave modulator

The slowing down factors for device 3F with a silicon dioxide layer of 700nm was found to be 1.265 and device 7B with a silicon dioxide layer of 900nm was found to be 1.367 referring to the figure 6.14.

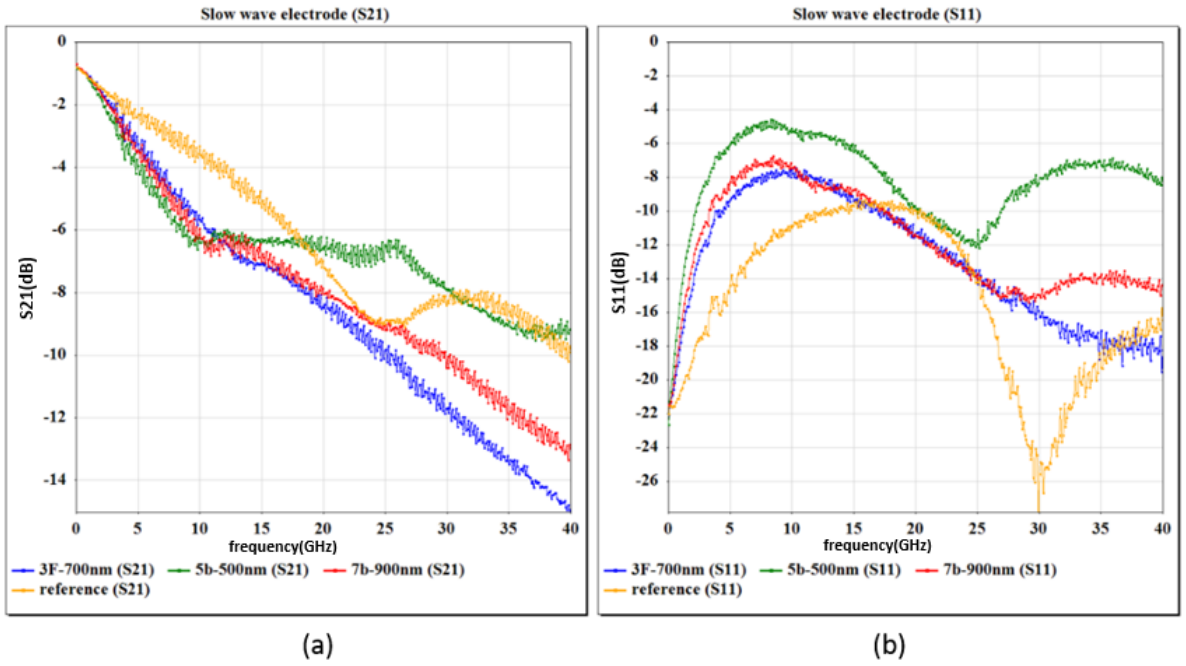


Figure 6-15– (a) Insertion loss and (b) reflection loss for slow wave modulator

The capacitance of the line is varied to slow down the wave via adding the corrugated metal layer on top of an oxide. The impedance also varies and will cause an impedance mismatch, resulting in greater signal reflection. Figure 6.15 shows the insertion loss and reflection loss for the slow wave modulators. The reflection loss for the reference (yellow curve in figure 6.15(b)) is below -10dB which denotes reasonably good impedance match. When the slow structure was added to the electrodes then the reflection loss increased for all slow wave modulators denoting the impedance mismatch. However, the results reflect that not only the slowing down factor is 1.57 for the 5B but also the overall transmission loss is similar to the reference. This is due to the reduction in substrate loss even through the reflection loss has increased.

Optical measurements were repeated after the fabrication of the slow wave electrode to see if the fabrication had any impact on optical performance. The results shown in figure 6.16 reflects that the fabrication of slow wave structure can have no impact on the optical operation of the device 7B. Unfortunately the other two fabricated samples the slow wave optical response had been damaged by the fabrication of the slow wave electrode structure, so no comparison was possible.

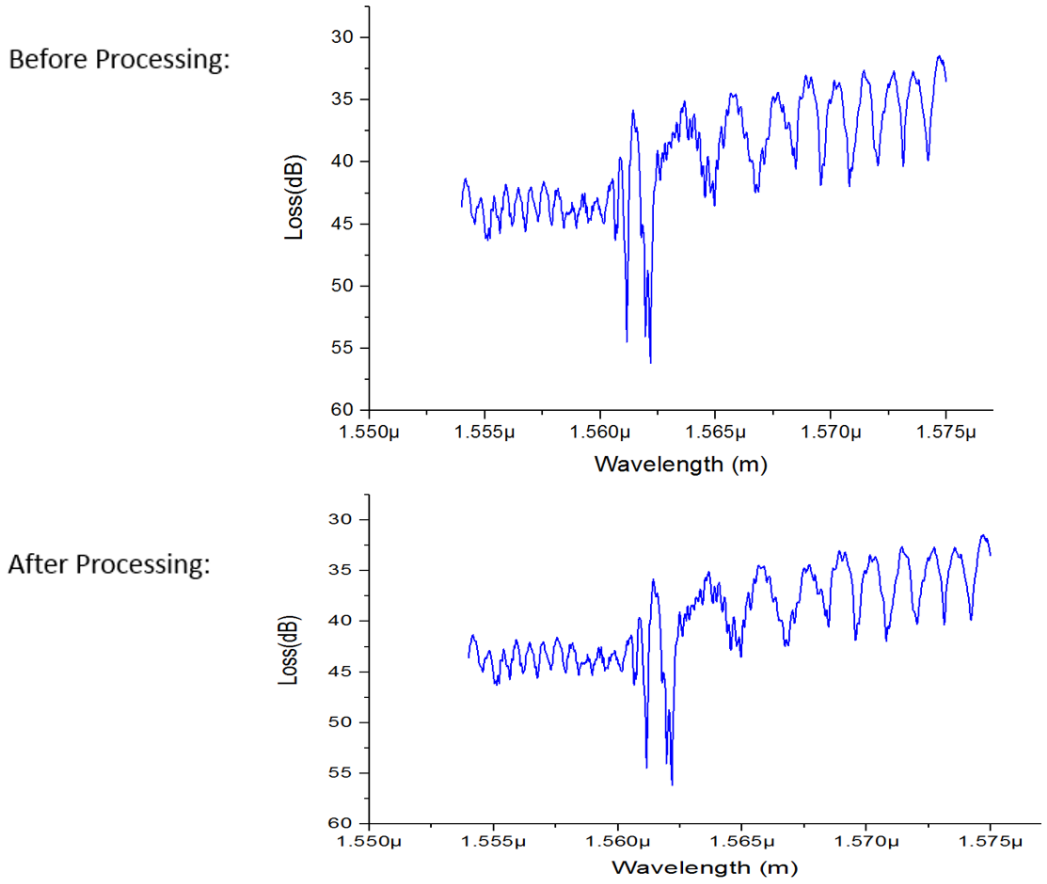


Figure 6-16– Optical measurement of device 7B before and after fabrication

The modulation bandwidth of the devices can be limited by either a velocity mismatch between the optical and electrical signals or by RF transmission loss. The graph in figure 6.17 shows a graphical representation of the bandwidth vs group index performance of the device. The bandwidth limitation before the slow wave structure is added to the modulator is represented in the graph as solid lines. It can be seen that with a low optical group index the device is limited by the RF transmission loss which stays constant with optical group index. At a certain optical group index, velocity mismatch becomes the dominant bandwidth limiting mechanism and therefore from this point the modulation bandwidth decreases with increasing optical group index. When the slow wave structure is added, the reflection loss is increased (as shown in figure 6.15(b)) due to the increase in capacitance which slows the electrical signal down but also gives higher reflection loss. This increase in reflection (and therefore transmission loss) will give a lower modulation bandwidth in the low optical group index regime as represented in the graph as red dotted line. At the same time, the limitation due to the velocity mismatch with increasing optical group index is decreased since the electrical wave is now travelling slower as represented in figure 6.17 as yellow dotted line. For this

reason it should still be theoretically possible to see an improvement in the modulation bandwidth when the modulator is operated at a high optical group index despite the increased transmission loss. Therefore, we can conclude that if the slow down enhancements to the electrodes were included at the design stage, rather than being retrofitted, the overall performance would be improved.

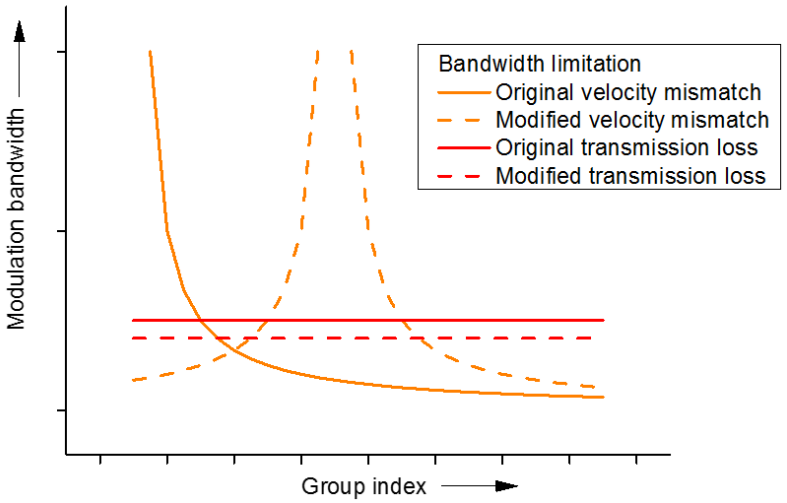


Figure 6-17– Graph explaining the bandwidth limitation

This is evident from figure 6.18 which shows optical eye diagrams of Device 7B which was reversed biased at 2.5V and is of the 1mm modulator length at 2 different wavelengths each corresponding to a quadrature operating point (decreasing wavelength corresponds to increasing group index in this case)In the low group index regime (higher wavelength) the eye shape and opening is poor as the device bandwidth is limited by velocity mismatch since the optical wave is propagating faster (figure 6.18(a))than the electrical wave. As the group index is increased (decreasing wavelength) the optical wave becomes slower and better matched with the velocity of the electrical wave on the slow wave electrodes. As a result an improvement in eye shape and opening can be observed (figure 6.18b). Thus showing an improved performance with an increase in group index.

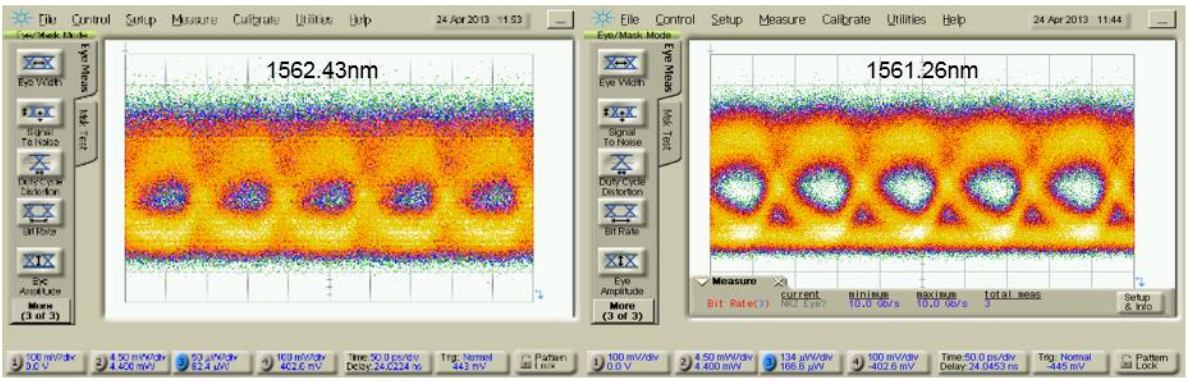
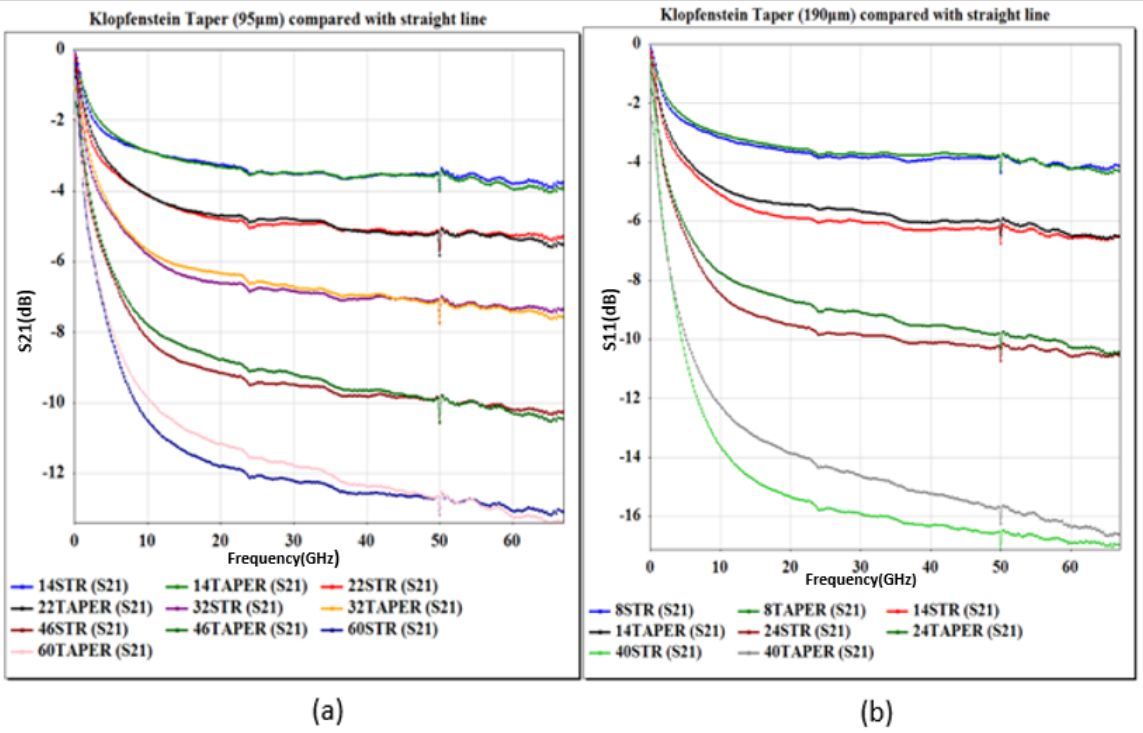


Figure 6-18– Eye diagrams for device 7B with modulator length of 1mm and 2.5V bias (a) at 1562.42nm wavelength (b) at 1561.26nm wavelength

The slow wave structure on device 7B gives a slowdown factor of 1.367 which does not give a massive improvement to the mismatch but this ensures that the reflection loss is also kept low enough to see an improvement. It is appreciated that observing optical eye diagrams are not the ideal method to conclusively confirm an improvement in performance and ideally electro-optic bandwidth measurements would have been taken, however unfortunately this facility was not available.

6.5 Tapers

This section will present the measured results of different types of tapers such as Klopfenstein tapers(k tapers) (refer to chapter 4), exponential tapers, and triangular tapers. Different lengths of tapers were measured and were compared against striaght coplanar line of the same length to calculate the loss due to the taper.



(a) (b)

Figure 6-19– (a) insertion loss for 95 µm K taper compared with straight coplanar line (b) insertion loss for 190µm K taper compared with straight coplanar line

Lets first consider measurement results of the k tapers compared with the straight lines shown in figure 6.19. Figure 6.19 (a) shows the length of one taper is equal to 95µm and on the right the taper length is equal to 190µm. '12Taper' shown in the figure is abbreviated for 12 tapers and '12STR' is the equivalent length of a straight coplanar line for 12 tapers. If 60 tapers of 95µm length (pink response in figure 6.19a) are compared with the straight coplanar line (blue response in figure 6.19a), then it can be seen the loss of 60 taper is lower compared with coplanar line up to 50GHz. At 50GHz, the 60 tapers and straight line has the same loss. After 50GHz, the loss due to the taper starts to increase more than the straight coplanar line. Now consider 40 tapers of 190µm length (grey response in figure 6.19b) and equivalent coplanar line shown as green in the same figure. It can be seen again the transmission loss of the 40 taper is less than coplanar line but for the whole measured range (100MHz to 67GHz) in this case. If the measurement is conducted beyond 67GHz, then the loss of 40 taper should intersect with coplanar line loss (predicted to be in the range of 70GHz to 75GHz). The intersection point for short taper (95 µm) is at 50GHz whereas the for longer taper (190µm), it is above 70GHz. This is because the longer taper provides a better match. If less number of taper are considered for example 14 K tapers shown in figure 6.19a and the equivalent straight line, the overall attenuation loss and the behaviour of the line is almost the same over the frequency range considered. The electrode requires only 2 tapers hence it can be concluded that the loss due to 2 K taper will be insignifiant operating up to 67GHz

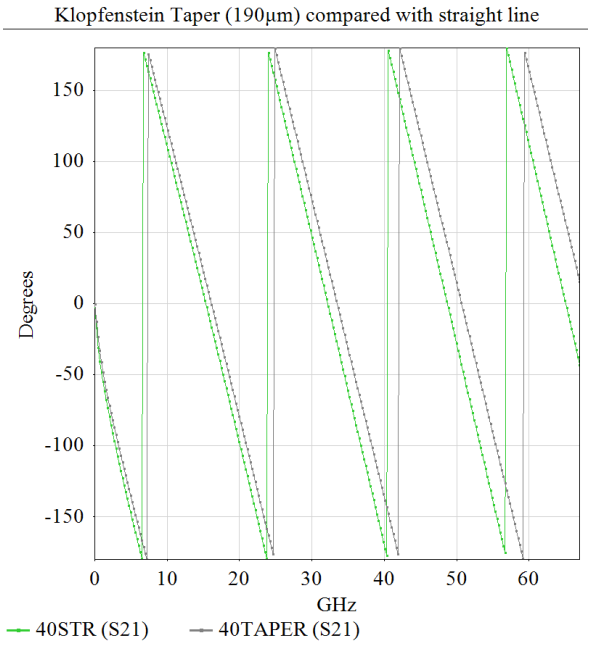


Figure 6-20– Phase for 40 tapers compared with coplanar line

Even though, the characteristic impedence is maintained throught out the taper, S21 show different response of the taper when compared with the coplanar line of the same length. The reason for it can be explained when the phases of the taper and equivalent line are compared. Figure 6.20 show the phase for 40 tapers compared with coplanar line for 190µm K taper. As the wave travels through the taper, the phase difference between the coplanar line and taper increases. The wave travels faster through the taper than the coplanar line. This is because the ratio of the capacitance and inductance has decreased. However, If the phase velocities are computed for both then it can be seen there are not significantly different. At 67GHz, the phase velocity of the taper is found to be 1.35×10^8m/s whereas coplanar line is equal to 1.299×10^8m/s.

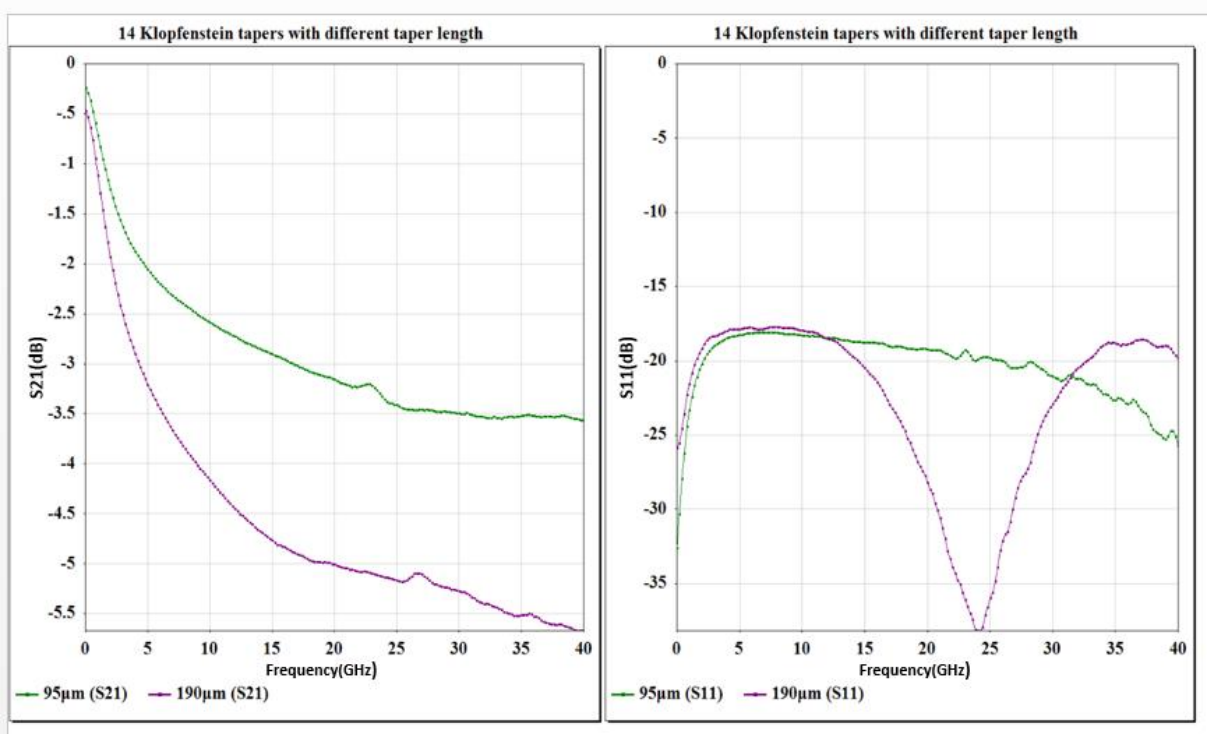


Figure 6-21– S21 (left) and S11 (right) for 14 K tapers of two different lengths.

Figure 6.21 shows the measured response of 14 Klopfenstein tapers with two taper lengths (95 µm and 190 µm). It can be observed that the 95µm length gives lower loss per unit length compared with 190 µm taper. Even though a longer taper length gives less loss since the tapering angle is less steep, the total transmission loss due to the increased length is significantly higher which denotes that the short taper is will give better overall performance as indicated in figure 6.21. In other words, the line itself is quite lossy and the wave has to propagate along longer length in the case of 190 µm, thus the loss is higher. At 40GHz, the 95µm long taper gives a loss of 0.25dB/taper whereas the 190µm taper give a loss of 0.41dB/taper. The reflection for both tapers is below -17dB which means for the both tapers have overall good match over the required frequency range.

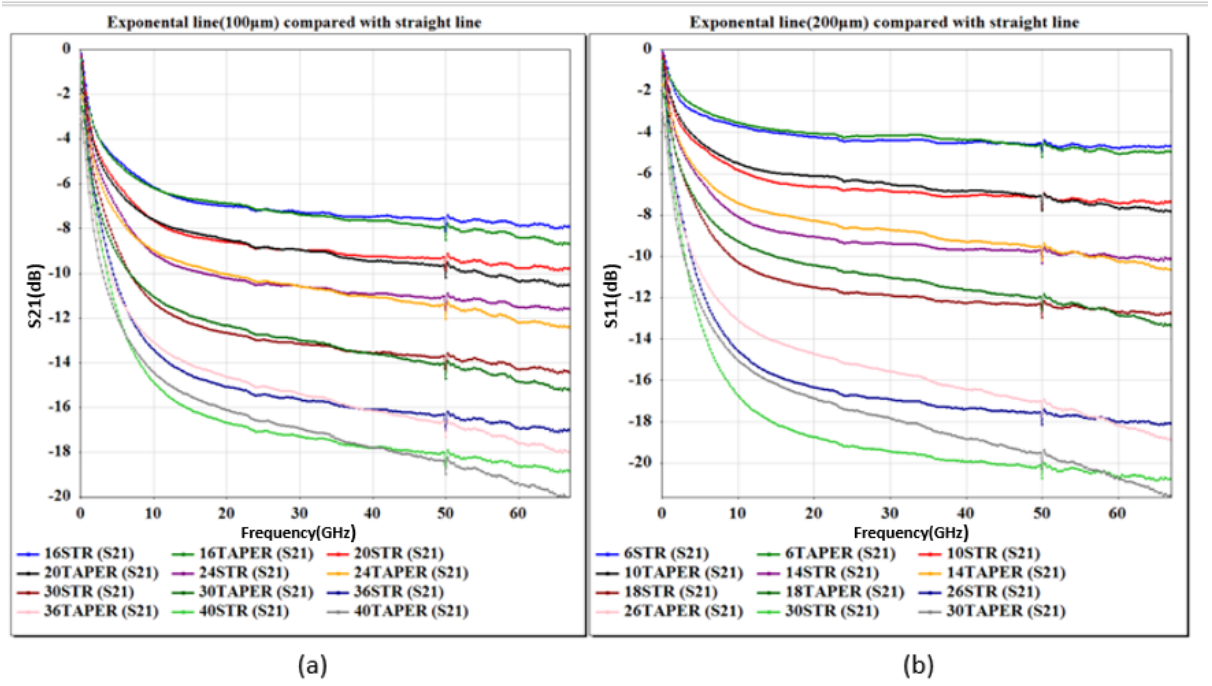


Figure 6-22 – Exponential taper measurement results (a) S21 for 100µm taper length compared with coplanar line (b) S21 for 200µm taper length compared with coplanar line

Figure 6.22(a) shows the results for 100µm long exponential tapers compared with coplanar lines of equivalent length. Consider 40 tapers shown in grey and coplanar line of equivalent length shown in light green in figure 6.22(a). This time the intersection of both curves are at 40GHz. After 40GHz, the loss due to the taper increases. Whereas for the K taper the intersection point was found to be 50GHz for similar length of the taper. Also the intersection point for 200µm expontential taper was found to be at 58GHz whereas for the K taper was predicted to be above 70GHz. Which indicates that K taper has better performance when compared with the expontential taper.

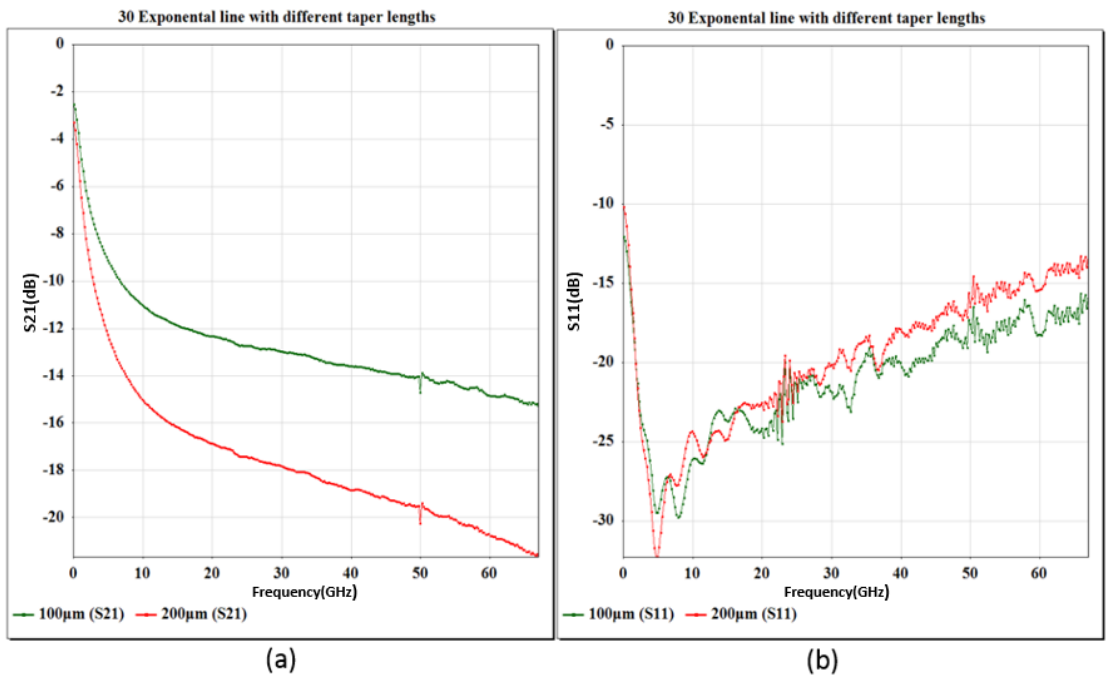


Figure 6-23– (a) S21 direct comparsion for 30 exponential taper with 100µm and 200µm. (b) S11 for 30 exponental taper with 100µm and 200 µm

Figure 6.23 shows the direct comparsion for 30 exponential tapers with length of 100µm and 200µm. The results again reflect the same tend as for the K- taper. The S11 for the exponential taper is -10dB (figure6.23b) whereas for the K taper, it is equal to -17dB for the whole range.

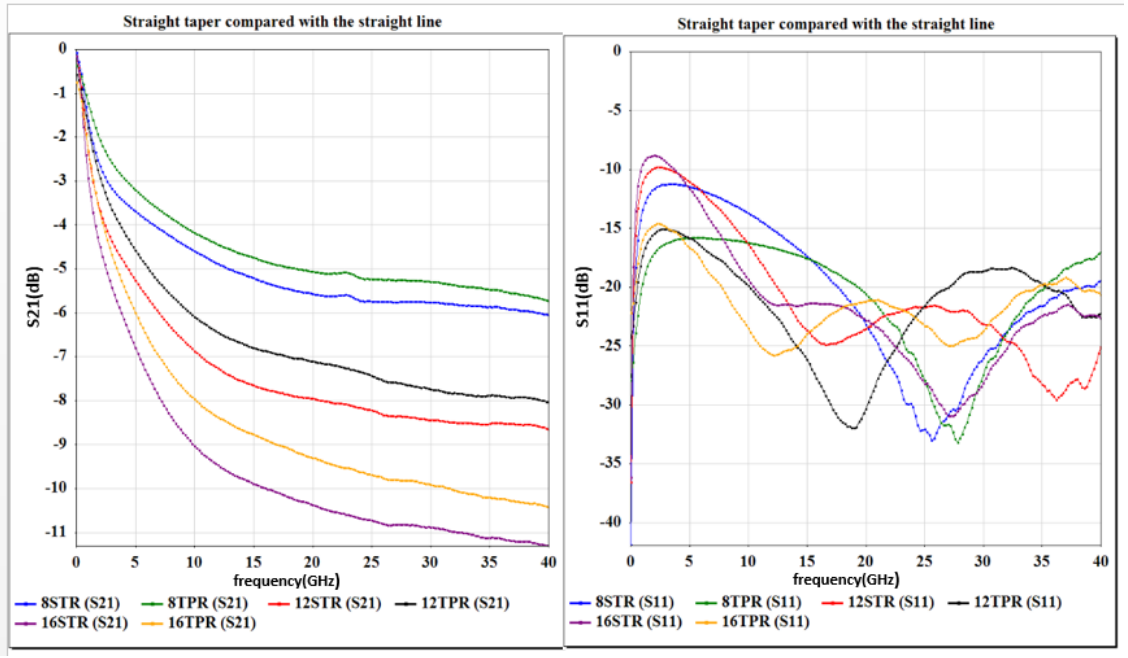


Figure 6-24– Straight taper measurement results compared with straight line. Left graph: S21, right graph: S11

Figure 6.24 shows straight taper compared with the equavilent coplanar line. The straight taper measurement results show a similar trend to exponential taper and K taper but gave higher loss. The reflection loss for the whole frequency range was found to be below -15dB.

When the tapers were compared directly and loss per length from the above graphs were calculated at 40GHz then the roll-off characteristics of insertation loss of all the tapers were found to be the same. Table 6.4 shows the summary of measured results of different types of tapers. The exponential taper for the 100µm gave the loss of 2.08dB/mm and for 200µm, the loss of 1.99dB/mm (table 6.4) . The K-taper with 95µm and 190µm gave loss of -2.07dB/mm and -1.97dB/mm respectivily (table 6.4). The straight taper with 100µm gave the loss of 2.08dB/mm. For the required frequency range (0GHz to 40GHz), the loss due to the tapers has no significant impact. Nevertheless, the K-taper with 190µm length gave the least loss per length but 95µm K taper (0.26dB/taper) would be the preferred taper as the the overall length is halfed which will give significantly decrease in added loss (table 6.4) due to added length. The same trend was observed in the case of doped wafers but with a higher transmission loss which is caused by increased substrate loss.

Table 6.4– Summary of measured results of the different type of tapers

Taper type	Number of tapers	Taper length (µm)	Total length (µm)	Loss/mm(dB)	Loss/taper(dB)	Loss at 40GHz (dB)	Peak reflection loss (dB)
Exponential	**16**	**100**	**3580**	**2.08**	**0.47**	**-7.45**	**-15**
Exponential	**14**	**200**	**4640**	**1.99**	**0.66**	**-9.27**	**-15.33**
Klopfenstein	**14**	**95**	**1730**	**2.07**	**0.26**	**-3.58**	**-16**
Klopfenstein	**14**	**190**	**3050**	**1.97**	**0.47**	**-6.02**	**-16**
Straight	**16**	**200**	**5020**	**2.08**	**0.65**	**-10.43**	**-14.57**

6.6 Electrode

This section will look at the overall electrode design which is made up of all the elements discusssed in the previous sections. The modulator electrode is made up of a thin line, bends, tapers and a thick line. It will particularly look at the electrode aligned to a current modulator chip so that the electrodes could be directly be fabricated on top of the modulators without making changes to the modulator design. The chip has four different lengths of phase modulator,0.25mm, 0.5mm, 1mm and 3.5mm. However, the actual electrode required to drive the modulator is longer due to the

bends, tapers and probing pads. The electrode design is compared with the electrodes presented by Thomson et al. [3]. Their design was added to the mask and directly compared with other electrode designs by the author (figure 6.25). The measurement results shown in figure 6.26 are a comparison of the two different designs with the design of Thomson et al. [3].

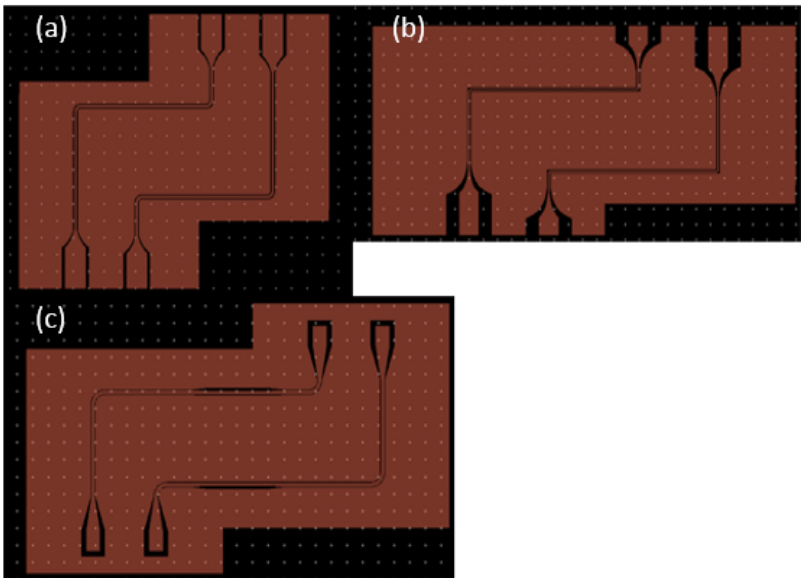


Figure 6-25–(a) Design A, (b) Design B and (c) Thomson et al. design

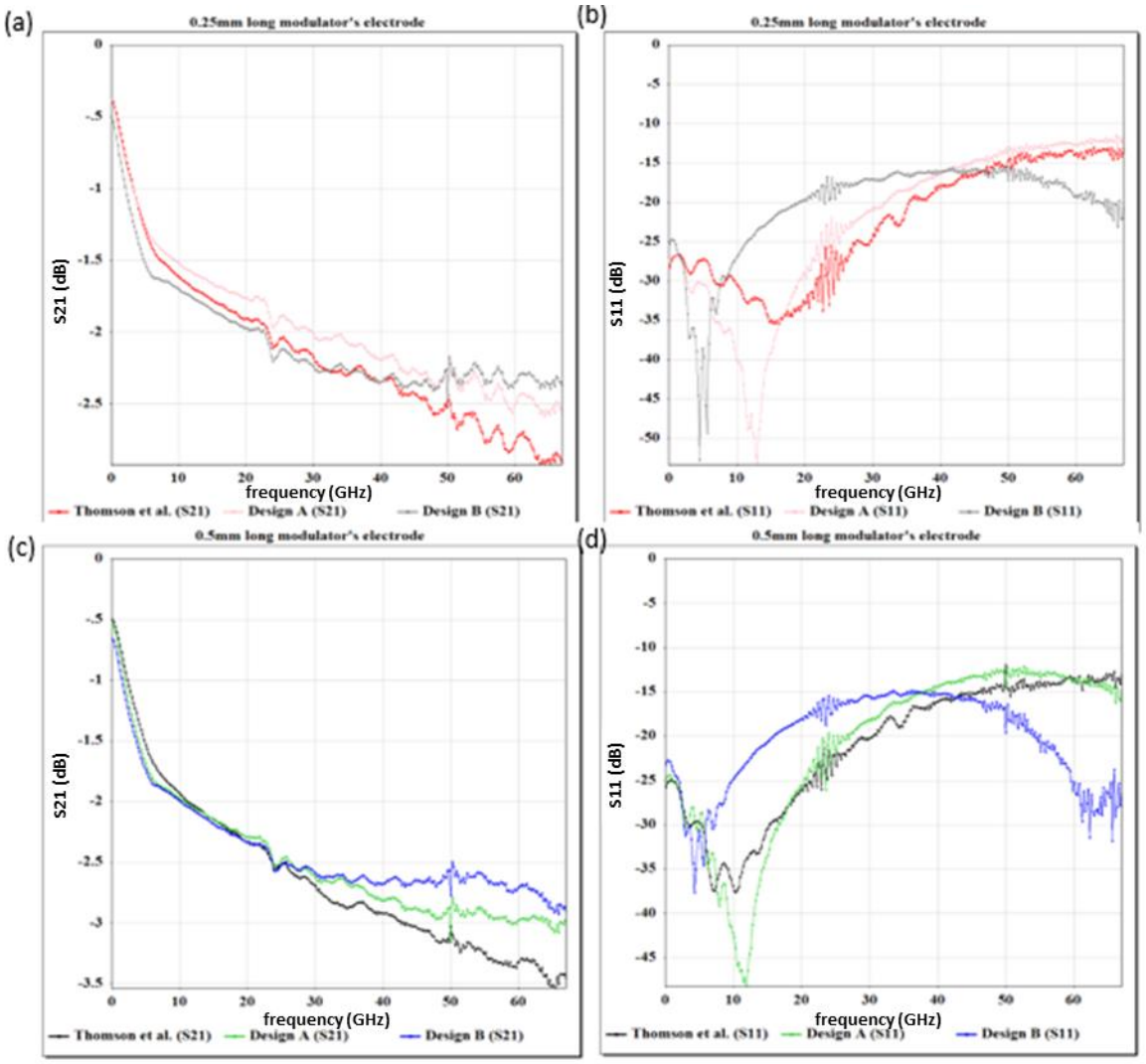


Figure 6-26– (a) S21 for 0.25mm modulator (b) S11 for 0.25mm modulator (c) S21 for 0.5mm modulator and (d) S11 for 0.5mm long modulator

Even though, the active region of the modulator is 0.25mm, the total length of the electrode is increased to 1.25mm or more, depending on the electrode design. Figure 6.26 shows the measured results of the two electrode designs compared with the electrode design of Thomson et al. [3], for two different lengths of modulators. The graphs in figure 6.26(a) and (b) show the S parameters for the 0.25mm long modulator and the graphs (c) and (d) show the results for a 0.5mm long modulator. For the 0.25mm long modulator, design A gave the best overall response up to 40GHz. From 40GHz up to 67GHz, design B gave better response in comparison to the other two electrodes. For 0.5mm, no difference in performance of the three electrodes can be seen from 100MHz up to 20GHz. As frequency increases beyond 20GHz, the losses due to the elements in the design becomes more evident. The insertion loss of design B is equal to 2.9dB at 67GHz whereas it is 3.45dB for the design

of Thomson et al. [3]. 3dB point is when the signal drops to $\frac{1}{\sqrt{2}}(0.707)$ in magnitude. The 3dB point for 0.5mm long modulator, Thomson et al. [3] is at 42.8GHz, Design A is at 58.93GHz whereas for Design B it is beyond 67GHz. At 67GHz, the loss is equal to 2.90dB for Design B. This shows an improvement of at least 10GHz.Therefore, the new designs both provide significantly enhanced performance at higher speeds (30GHz and beyond), which are key speeds for silicon photonics devices.

Table 6.5– Summary of loss per unit length for 0.25mm long modulator

For 0.25mm	40GHz	67GHz
Design A	1.752dB/mm	2.056dB/mm
Design B	1.88dB/mm	1.896dB/mm
Thomson et al.	1.88dB/mm	2.32dB/mm

Table 6.6– Summary of loss per unit length for 0.5mm long modulator

For 0.50mm	40GHz	67GHz
Design A	1.87dB/mm	1.99dB/mm
Design B	1.786dB/mm	1.933dB/mm
Thomson et al.	1.946dB/mm	2.3dB/mm

Table 6.5 and Table 6.6 shows a summary of the loss per unit length for 0.25mm and 0.5mm respectively at 40GHz and 67GHz as extracted from figure 6.26. Again, it can be seen that Design B from both lengths of the modulators give the least loss per unit length.

6.7 Discussion

It was found that a bend will add no loss to electrode as long as even number of the bends are used. The loss due to the taper was found to be negligible under the frequency range considered. Therefore, K taper with 95µm length can be preferred as this reduces the loss per taper. As a results,

final electrode designs were presented and performance was measured against Thomson et al. [3]. The new electrode design 3dB point for 0.5mm long modulator exceeds the frequency beyond 67GHz were the 3 point for the Thomson et al. [3] was measured at 42.8GHz. This will improve the bandwidth of the silicon optical modulator.

A slow wave structure applicable to slow modulators has successfully been demonstrated. As a result, the electrical signal has been slowed down to reduce the mismatch with optical group velocity. This allows to achieve high bandwidth as well as reduced device foot print. The measurement results show that if further optimization is carried out on the slow wave electrode then the total transmission loss (substrate loss and impedance mismatch) can be reduced while achieving the velocity match between electrical and optical signal.

References

[1] C. A. Hoer and G. F. Engen, 'Thru-Reflect-Line, An improved technique for calibrating the dual six-port automatic network analyser' IEEE Trans. Microwave theory tech., vol.27, issue 12, 1979, pp.987-993

[2]Amr M. E. Safwat, and Leonard Hayden, "Sensitivity Analysis of Calibration Standards for SOLT and LRMM", Cascade Microtech., 2001, pp.1-10

[3] A. Brimont, D. J. Thomson, P. Sanchis, J. Herrera, F. Y.Gardes, J. M. Fedeli, G. T. Reed, and J. Martí, 'High speed silicon electro-optical modulators enhanced via slow light propagation', Optics Express, Vol. 19, Issue 21, 2011, pp. 20876-20885

[4]Joel P. Dunsmore, "Handbook of microwave component measurements: with advanced VNA Techniques", John Wiley & Sons, Ltd, 2012, pp.14

Chapter 7: Conclusion

Silicon travelling wave modulators have shown tremendous progress over the last decade and due to their high speeds and bandwidth, have proven to be a viable solution to the copper interconnect problem. These silicon modulators require electrodes and optimization of their design is as crucial as that of the optical part of the modulator. This is because losses associated with the electrode will affect the modulator's bandwidth and therefore its overall performance. The dominant electrode loss is due to the substrate itself and a review on microwave transmission lines in this study has concluded that the conductance and/or resistance per unit length is highly dependent on the type of substrate used. Further, the dimensions of the line also play a role in contributing to losses and these findings were found to be applicable to our modulator's electrodes.

Early research on coplanar bends suggested methods like air bridges and dielectric overlay to reduce the loss around the bend, which require extra fabrication steps. However, in this work it has been shown through characterisation of three different bends (round, mitred and square) on SOI that the loss due to the bend is insignificant as long as an even number of bends are used in the frequency range 100MHz and 40GHz.

Fabrication consisted of three different process flows. Two of these processes started with a bare silicon wafer while the third process required the fabrication of a slow wave structure, which was fabrication on top of the slow wave modulator. As part of the fabrication process, optimized recipes had to be developed as these recipes were not available at the start of the project. The optimized recipe for etching a thick Al layer with available process gases was found which is comparable with industrial fabrication (for example CEA Leti). The vertical profile angle of 99.4°±2° with good selectivity of electrode was achieved.

Hillock formation occurs when Al is deposited on top of silicon dioxide as a result of a stress relaxation mechanism which arises due to differences in thermal expansion coefficients of the two materials. Studies on hillock formation have suggested that they could potentially increase the conductor loss by a factor of 3 at higher frequencies. Annealing of hillocks was done in this work in order to see if the hillock density would decrease as has been suggested in some early studies. However, it was found that annealing is ineffective in reducing hillocks. In contrary it increases the size of hillocks even when annealed for short times (15mins). Beyond 380°C, cracks

started to appear due to stress relaxation mechanism. Nevertheless, metal stacks were able to resolve the issue of hillock formation. For this reason, the metallization layer of CMOS process consisted of many layers of different metals with different conductivities. The effective method to incorporate the conductivity of metal stack to get more accurate results for simulation has been demonstrated.

Conventionally straight coplanar tapers are used and are present in most libraries of RF/Microwave simulators, however, not much literature is available on different coplanar taper types. For this reason, different tapers with different lengths were studied over a broad frequency range. As a result of theoretical and experimental results the K taper of 95µm length was preferred since this taper gives the lowest loss per taper in comparsion to other tapers. After separate analysis of each electrode element, the relative improvement of electrode design compared to that of Thomson et al. [6] was presented and the operating frequency was improved from 42.8GHz to 67GHz (or beyond). This translates into higher key speeds of silicon electro-optic modulators where only the electrode design is altered without the need to change current mask design.

The slow wave modulator are capable of achieving higher phase shift for a given voltage, which in turn reduces the footprint of the device. Thus holds the potential of improving the figure of merit of modulator immensely; if the velocity match between electrical and optical signals are optimized which is retaining the performance. Consequence of this lead to theoretical study of various slowing down structures where the slowing down factor of slotted ground plane was found to be restricted to 1.34. The slow wave structures currently used for modulators, such as T shaped structures have also shown limited slowing down factors [5]. Whereas if the corrugated floating metal on top of an oxide layer presented in this work has shown slowing down factor of 3 or more to be achievable which is needed for velocity matching in the case of slow wave modulators. This proposed method is not only capable of achieving very high slowing down factors but also capable of reducing the substrate loss where the substrate loss is the dominant loss. On the contrary, this technique does give rise to induced eddy currents, which in turn causes loss, but the loss is found to be much lower than the substrate loss. For this reason, overall attenuation of the electrode will be reduced as well as electrode loss per unit length will be reduced as shorter length will be required to achieve the phase shift. To the author's best knowledge, this is the first time this type of slow wave structure has been applied to the modulator electrodes. Further simulation results suggests that if the electrode design is changed, then the impedance mismatch resultant from adding the metal strips can be reduced whilst achieving a high slowing down factor. Hence the further work proposed will be optimization of

the electrode impedance to improve the performance.

References

[1]L. Yang, T. Hu, R. Hao, C. Qiu, C. Xu, H. Yu, and Y. Xu, “Low-chirp high-extinction-ratio modulator based on graphene – silicon waveguide,” vol. 38, no. 14, 2013, pp. 2512–2515

[2]M. Lauermann, S. Wolf, P. C. Schindler, R. Palmer, S. Koeber, D. Korn, L. Alloatti, T. Wahlbrink, J. Bolten, M. Waldow, M. Koenigsmann, M. Kohler, D. Malsam, D. L. Elder, P. V Johnston, N. Phillips-sylvain, P. A. Sullivan, L. R. Dalton, S. Member, and J. Leuthold, “40 GBd 16QAM Signaling at 160Gb/s in a Silicon-Organic Hybrid Modulator,” vol. 33, no. 6, 2015, pp. 1210–1216

[3]Y. Tang, J. D. Peters, and J. E. Bowers, “Over 67 GHz bandwidth hybrid silicon electroabsorption modulator with asymmetric segmented electrode for 13 μm transmission,” Optical Express, vol. 20, no. 10, 2012, pp. 11529,

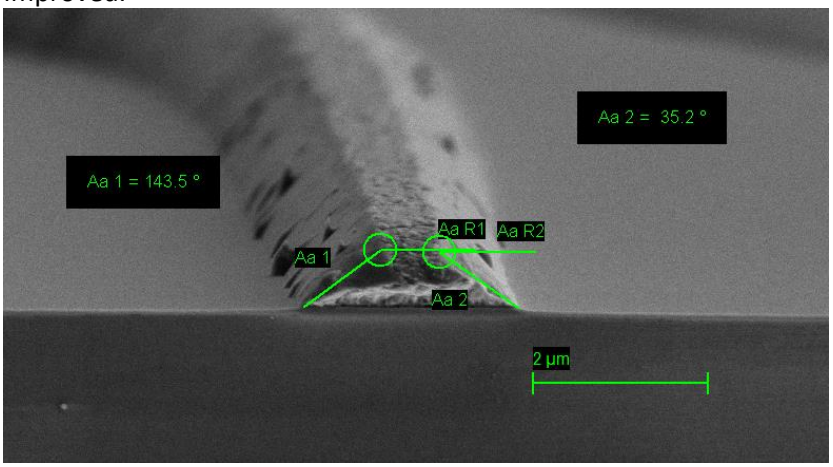
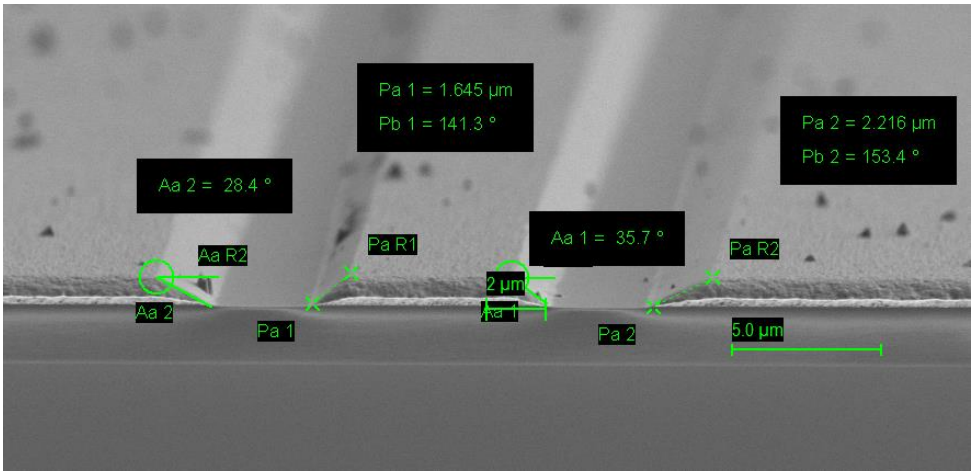
[4]Hao Xu, Xianyao Li, Xi Xiao, Peiji Zhou, Zhiyong Li, Jinzhong Yu, and Yude Yu, “High-speed silicon modulator with band equalization”, Optics Letters, Vol. 39, No. 16, August 15 2014, pp. 4839-4842

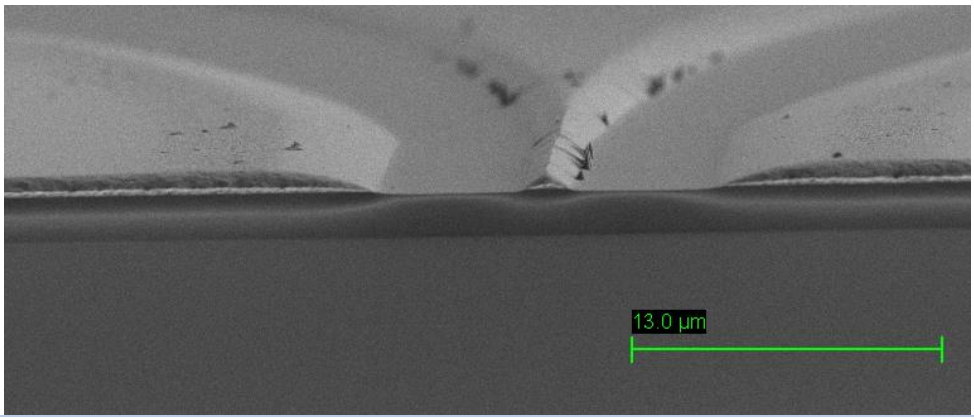
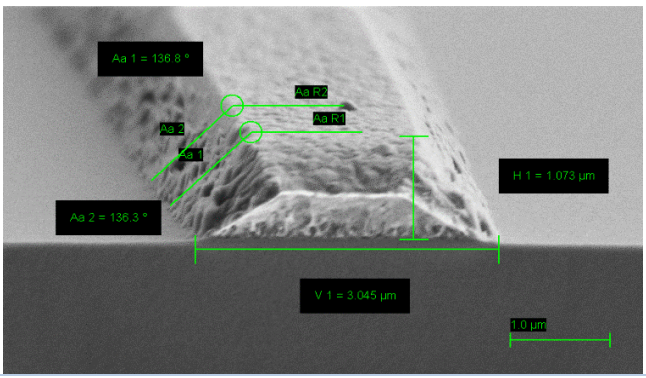
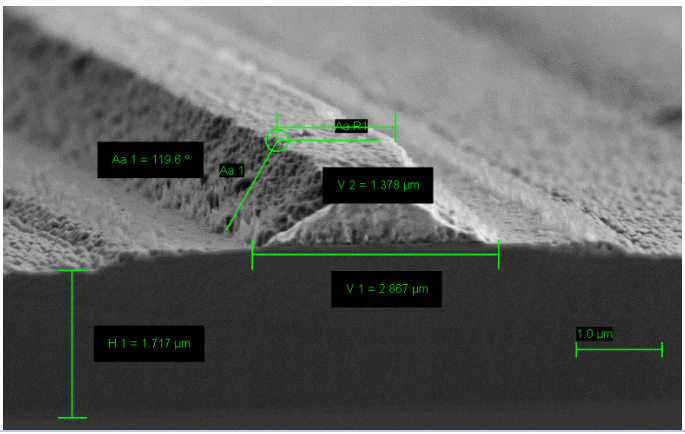
[5] David Patel, Samir Ghosh, Mathieu Chagnon, Alireza Samani, Venkat Veerasubramanian, Mohamed Osman, and David V. Plant, “Design, analysis, and transmission system performance of a 41 GHz silicon photonic modulator” , Optics Express, Vol. 23, No. 11, 1 Jun 2015, pp. 14263-14287

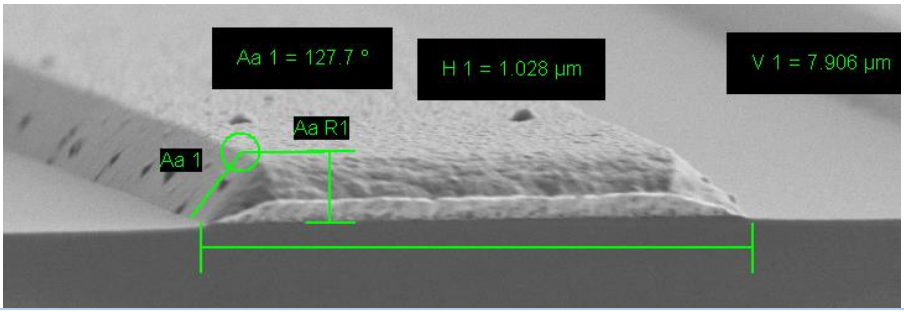
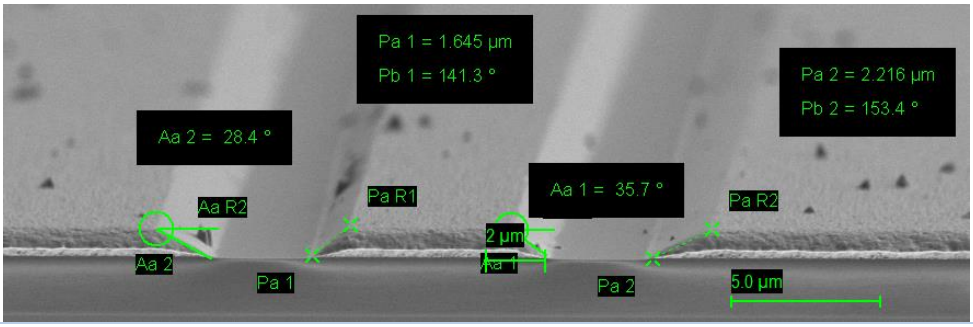
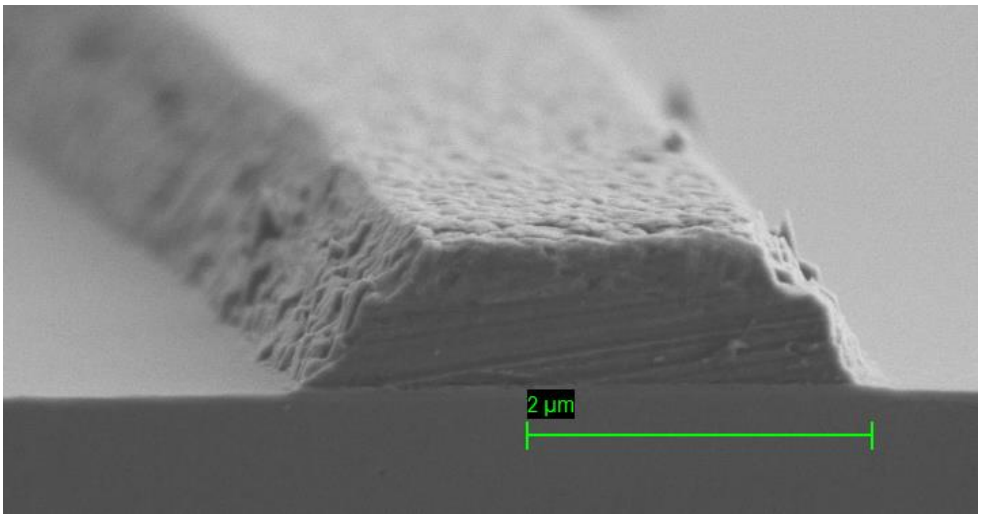
[6] A. Brimont, D. J. Thomson, P. Sanchis, J. Herrera, F. Y.Gardes, J. M. Fedeli, G. T. Reed, and J. Martí, ‘High speed silicon electro-optical modulators enhanced via slow light propagation’, Optics Express, Vol. 19, Issue 21, 2011, pp. 20876-20885

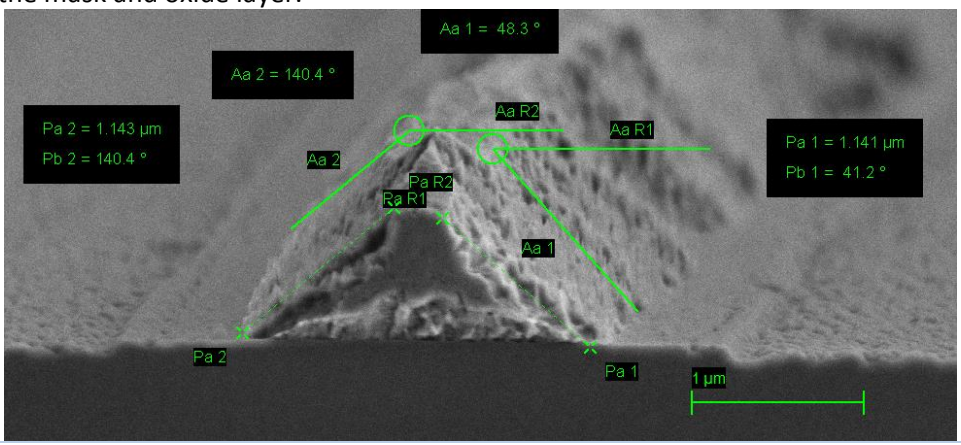
Appendix A : ICP etching supplementary information

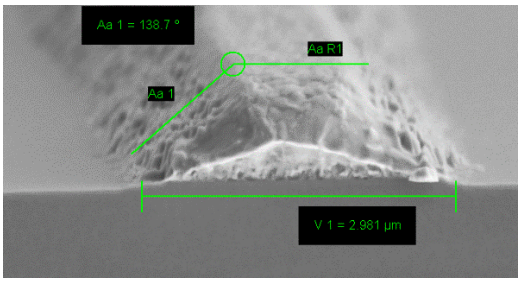
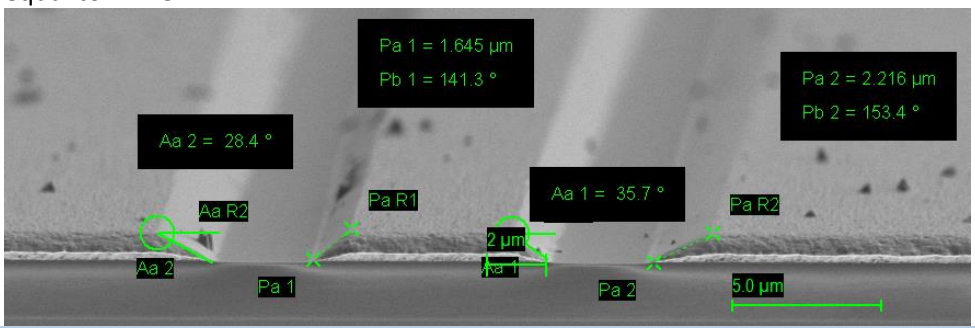
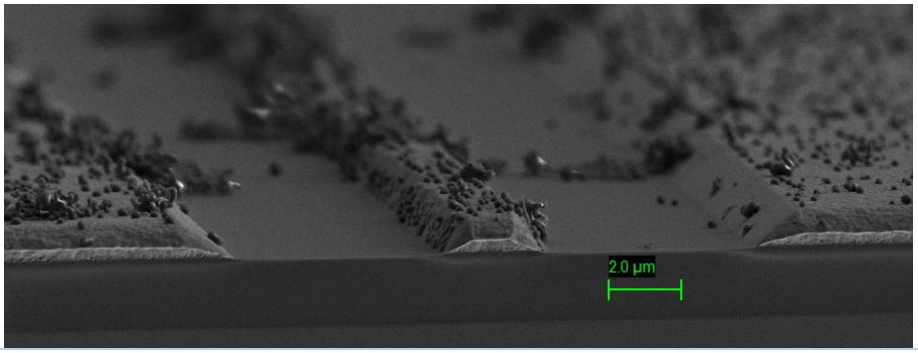
The experiment was carried out to optimize the ICP recipe where one parameter was varied while keeping other parameters constant. Refer to section 5.4.2 on page 120.

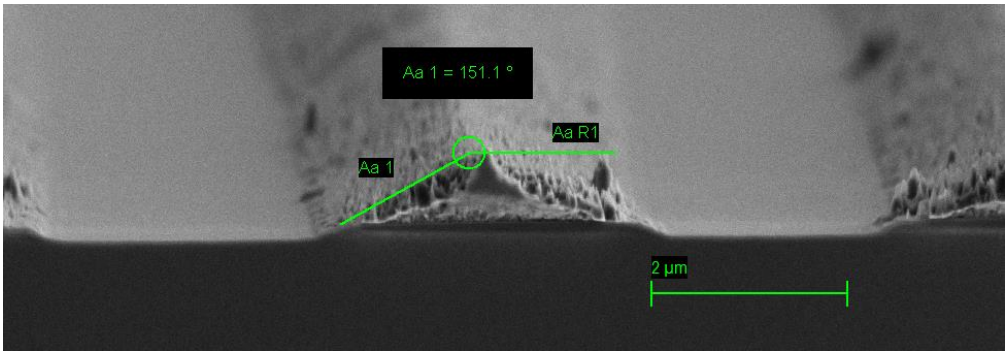
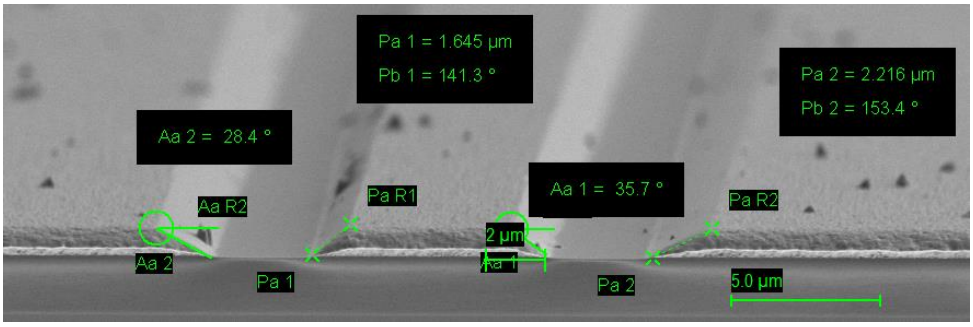
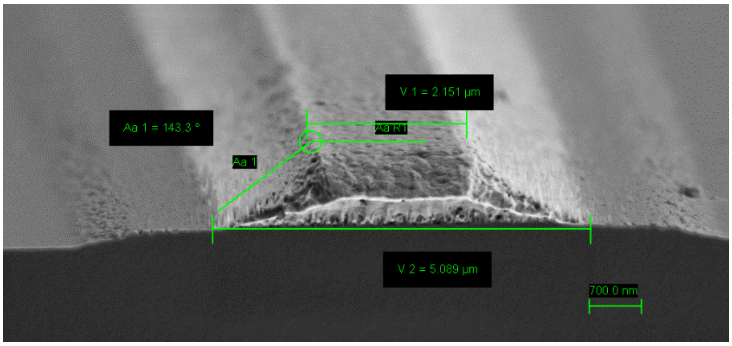
Temperature	SEM
5°C	When the table temperature was set to 5°C, showed the good selectivity but the sidewall profile was equal to 143° hence the sidewall profile angle needs to be improved. 
20°C	At 20°C, the selectivity was still maintained but sidewall angle almost shows negligible improvement. 

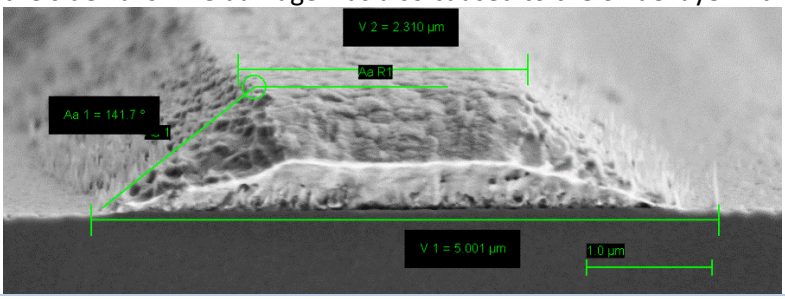
40°C	At 40°C, the selectivity against oxide layer was found to be good while the improvement to the sidewall angle was minimal. 
60°C	At 60°C, the selectivity was found to be good while the side wall profile improved to 136° but the sidewalls were found to be be rough. 
80°C	At 80°C, the selectivity was affected causing the damage to the oxide. The sidewalls of the metal was also found to be rough but the side wall angle was found to be 119.6°±2°. 

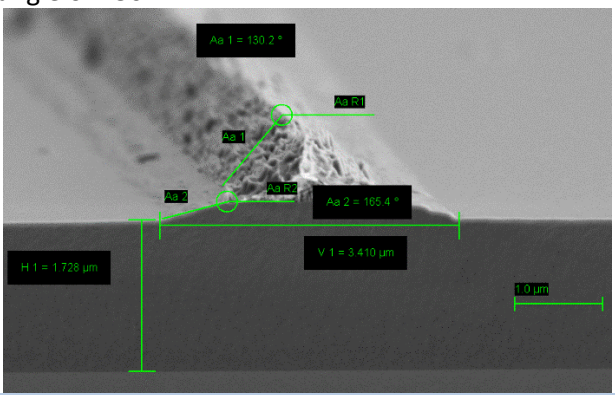
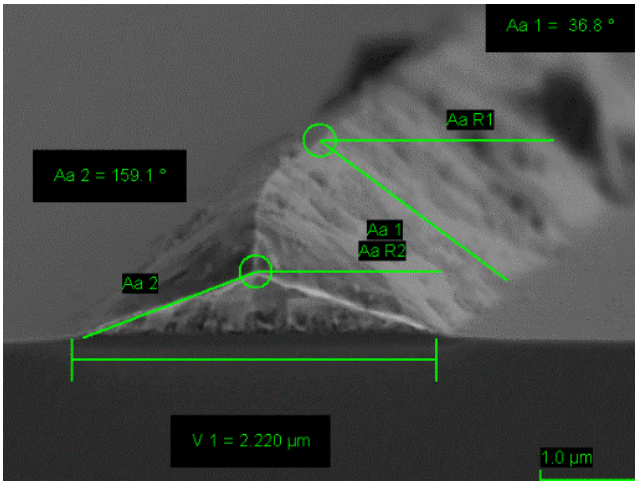
Pressure (mTorr)	SEM
3mT	At 3mTorr, the sidewall profile was found to be 127.7°±2° with smooth sidewalls as well as the selectivity was found to be good 
5mT	At 5mTorr, the profile angle increased to 141.3°±2°, and the sidewalls were still found to be smooth while maintaining the good selectivity. 
7mT	At 7mTorr, the profile angle of the sidewalls improved to 130°±2° but the sidewalls were found to be rough while maintaining the good selectivity. 

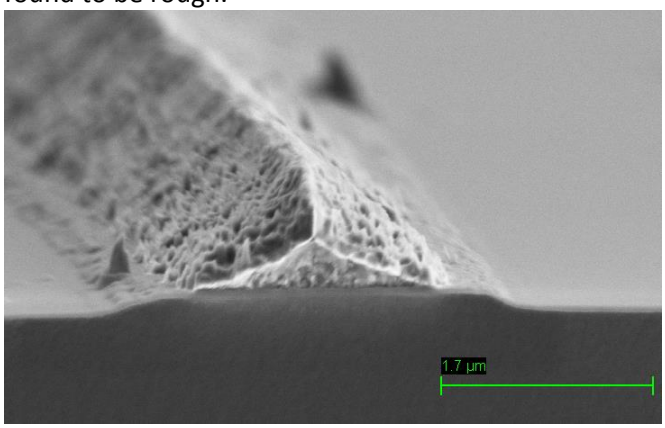
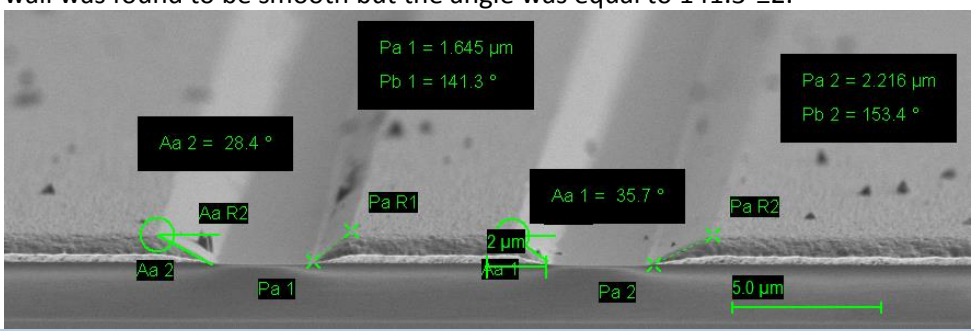
8mT	At 8mT, chamber pressure was found to be high and high bombardment of ions caused damage to the oxide layer with significantly decreased selectivity against the mask and oxide layer. 

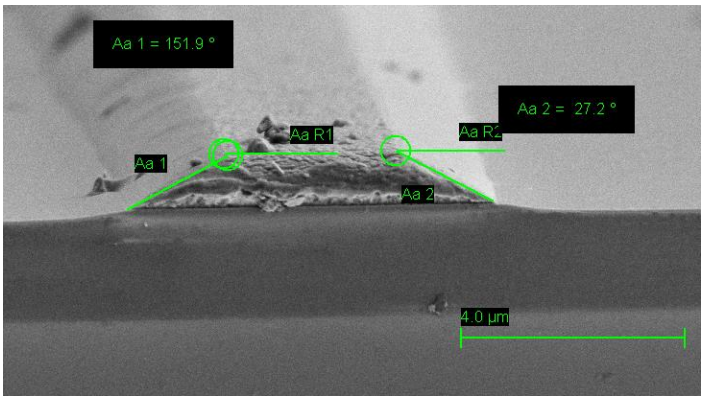
Argon (sccm)	**SEM**
5	At 5sccm, the sidewalls were found to be rough and the measured sidewall angle was 138.7°±2°. 
12.5	At 12.5sccm, the sidewalls were found to be polished and the sidewall angle was equal to 141.3°±2°. 
25	At 25sccm, the angle improved to 126°±2°, but deposition of contaminant residues were found on the surface. 

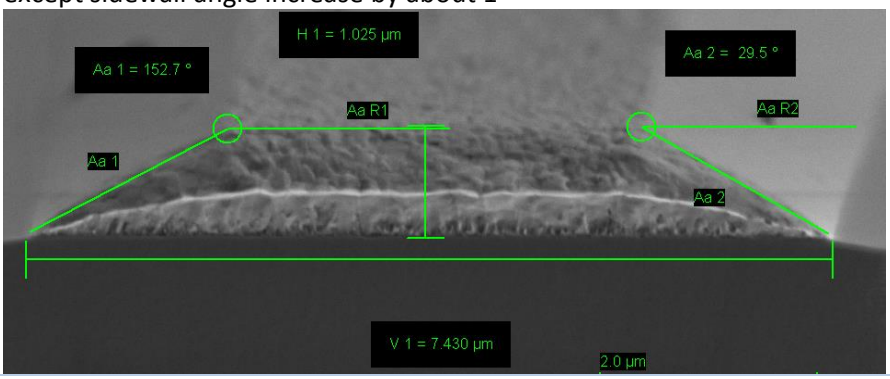
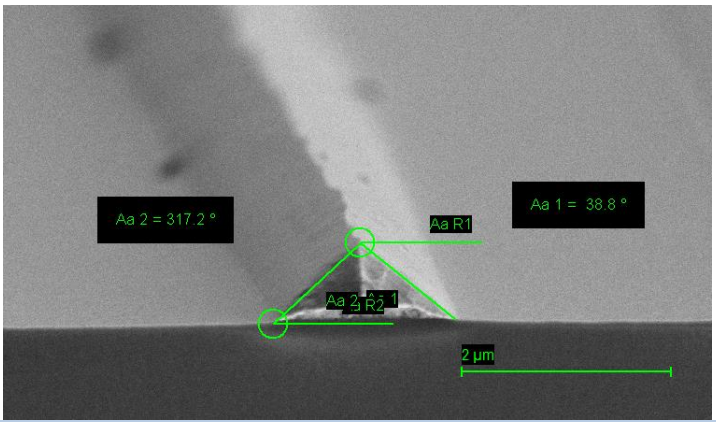
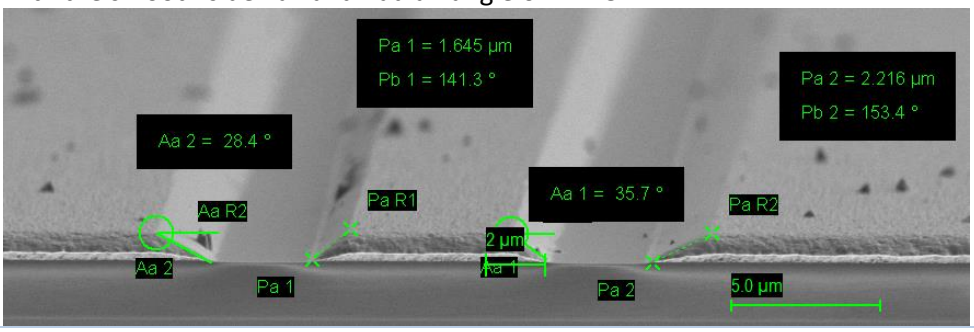
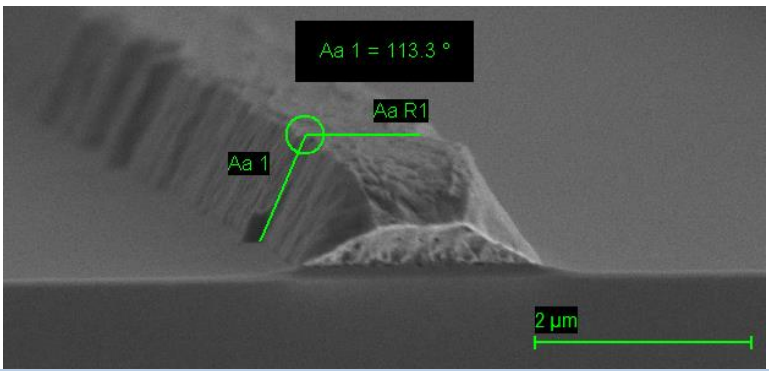
$SiCl_4$ (sccm)	SEM
5	At 5sccm, the angle was found to be 151.1°±2 while the metal protected was also etched away and spike like roughness was also caused due to less selectivity towards the photoresist. 
15	At 15sccm, the angle was found to be 141.3°±2 while the selectivity was found to be good against the mask as well as the oxide layer. No roughness was either caused. 
20	At 20sccm, the angle was found to be 143.3°±2 while spike like roughness was also caused to the sidewalls due to less selectivity towards the photoresist. The selectivity for oxide was also found to be poor. 

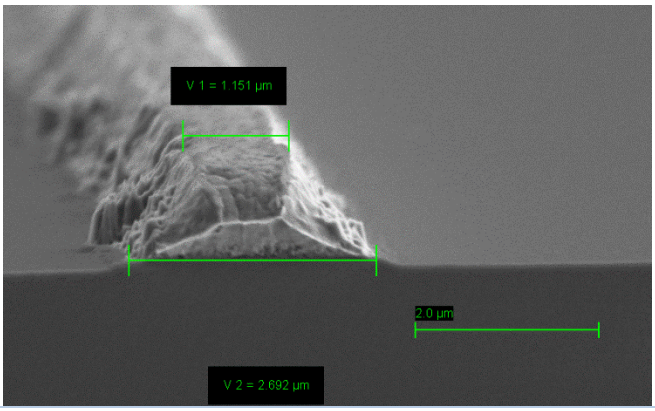
30	At 30sccm, the angle was found to be 141.7°±2 while the roughness was caused to the sidewalls. The damage was also caused to the oxide layer making it rougher. 

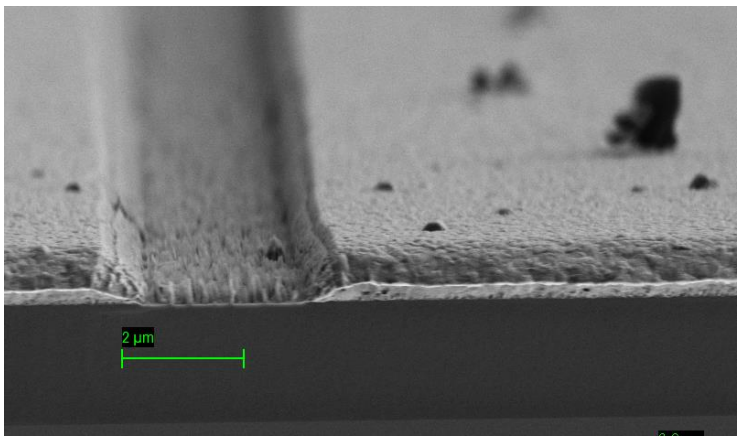
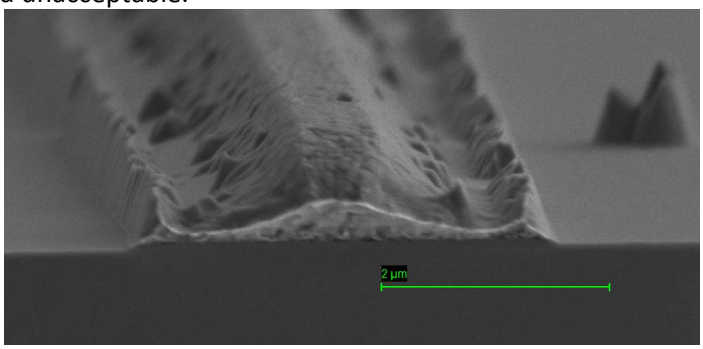
Chlorine (sccm)	
15	The selectivity was found to be very poor towards the resist and oxide. The damage to the oxide was not caused. The sidewall profile was found to be very rough with an angle of 130.2°±2. 
25	Even though with an increased flow rate the selectivity improved as well as the sidewalls were found to be smooth but the side wall angle was increased to 159.1°±2. 

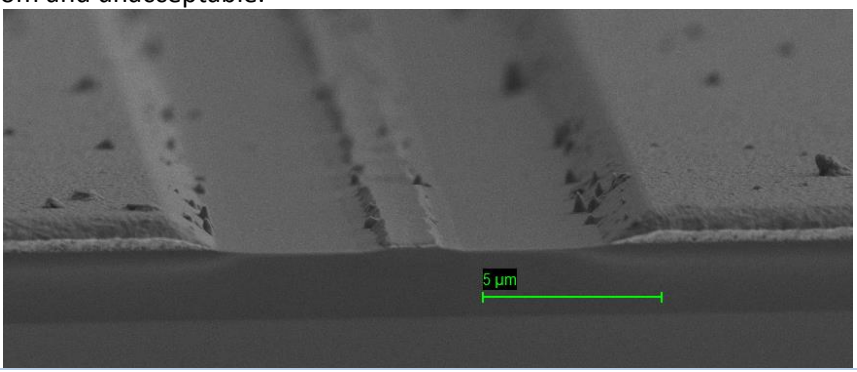
35	The selectivity towards the photo-mask decreased as well as towards the oxide but the damage was not caused to the oxide layer and the sidewall profile was found to be rough. 
50	The selectivity towards the mask as well as the oxide layer improved, the side wall was found to be smooth but the angle was equal to 141.3°±2. 

ICP power (W)	SEM
700	When ICP power was set to 700W, selectivity towards the photoresist as well as the oxide was found to be acceptable and the side walls of the profile was very smooth but had an increased side wall angle (151.9°±2). 

800	When the power was increased to 800W, no much difference was observed except sidewall angle increase by about 1° 
900	At 900W, the sidewalls were found to be smooth and is a selective recipe but the sidewall angle increased significantly to 317.2°±2° 
1000	The selectivity against the oxide as well as the photo-resist was found to be good with the smooth sidewall and had an angle of 141.3°±2. 
1200	The selectivity was found to be good as well as the side wall angle was reduced to 113.3°±2 and the sidewall were fairly smooth as well. 

1400	The selectivity of the photomask was affected hence effecting the profile of the metal. The selectivity towards the oxide was found to be good with no damage caused. 

RF power (W)	**SEM**
30	Grass type structures were found between the gaps of metal signal and ground planes while the sidewalls were still angled and insufficient milling was observed. 
100	The selectivity against oxide layer was good but the etching was found to be random and unacceptable. 

150	The selectivity against oxide layer was good but the etching was found to be random and unacceptable. 
200	The selectivity against the oxide as well as the photo-resist was found to be good with the smooth sidewall and has an angle of 141.3°±2.