UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL SCIENCE AND ENGINEERING

School of Electronics and Computer Science

Au-compensated High Resistivity Silicon for Low Loss Microwave Devices - Suppression of Parasitic Surface Conduction Effect

by

Nur Zatil Ismah Hashim

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ABSTRACT

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AU-COMPENSATED HIGH RESISTIVITY SILICON FOR LOW LOSS MICROWAVE DEVICES - SUPPRESSION OF PARASITIC SURFACE CONDUCTION EFFECT

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Deep-level doping compensation process using elemental gold is used to create high resistivity silicon substrate for microwave application. Gold atoms are introduced into low resistivity Czochralski silicon substrates through an ion-implantation process and activated via high-temperature annealings. The highest substrate resistivity recorded for optimised substrates is 60 kΩ-cm. A constant attenuation value of 0.19 dB/mm is measured at 20 GHz for a bias voltage range of -6 V to +6 V, for coplanar waveguides fabricated on this type of substrate, indicating full suppression of parasitic surface conduction effect at microwave frequencies. The attenuation results are supported by the capacitance-voltage characteristics, where the substrate is seen to be insensitive towards bias voltage. Based on a finite element analysis, this effect is caused by the reduced number of free carriers in the substrate and the increased interface trap densities at the oxide-silicon interface. Optimisation of substrate-processing stages are presented in this work. It is shown that the combination of slow-cooling and quenching for activation annealing provide a higher resistivity enhancement and a lower attenuation compared to single annealing. The removal of the near surface gold to increase substrate's resistivity is found to be unnecessary as it does not provide reduced attenuation. It can therefore be avoided to reduce process complexity. The influence of oxide type is studied, and thermal oxidation is seen to be unsuitable for oxide passivation. Bias-dependent attenuation characteristics suggest gold out-diffusion during the high-temperature treatment. Reactively sputtered oxides do, however, give excellent performance. In addition to coplanar waveguides attenuation responses, quality factor performance of meander inductors fabricated on gold-compensated high resistivity silicon substrate is evaluated. A higher quality factor is recorded for all inductance values for Au-compensated high resistivity silicon compared to Float-zone silicon. The highest quality factor value of 14 is measured for 0.7-nH inductors.

Declaration of Authorship

I, Nur Zatil Ismah Hashim , declare that the thesis entitled *Au-compensated High Resistivity Silicon for Low Loss Microwave Devices - Suppression of Parasitic Surface Conduction Effect* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

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List of Publications

N.Z.I. Hashim, Abuelgasim A., De Groot C.H., (2013) **Coplanar waveguides on gold-doped high resistivity silicon for 67-GHz microwave application**, *RF and Microwave Conference (RFM),2013 IEEE International*, Penang, Malaysia.

Abuelgasim A., **N.Z.I. Hashim**, Chong, H.M.C., Ashburn, P., De Groot C.H., (2014) **Low loss 67-GHz coplanar waveguides and spiral inductors on 100 kΩcm gold-doped high resistivity Cz-Silicon**, *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2014 IEEE 14th Topical Meeting on*, Newport Beach, California, USA.

N.Z.I. Hashim, Abuelgasim A., De Groot C.H., (2015) **Low loss microwave substrate using deep-level doping compensation**, *NANO Day Poster Session*, Southampton, United Kingdom.

N.Z.I. Hashim, Abuelgasim A., De Groot C.H., (2014) **Suppression of parasitic surface conduction in Au-compensated high resistivity silicon for 40-GHz RF-MMIC application**, *Microwave Conference (APMC), 2014 Asia-Pacific*, Sendai, Japan.

K. Mallik, A. Abuelgasim, **N.Hashim**, P.Ashburn, C.H. de Groot, (2014) **Analytical and numerical model of spiral inductors on high resistivity silicon substrates**, *Solid-State Electronics*, 93, 43-48.

N.Z.I. Hashim, Abuelgasim A., De Groot C.H., (2015) **Suppression of parasitic surface conduction in Au-compensated high resistivity silicon for microwave application**, *ECS Industrial Advisory Board Poster Session*, Southampton, United Kingdom.

N.Z.I. Hashim, Abuelgasim A., De Groot C.H., (2015) **Gold-compensated high resistivity silicon as low loss microwave substrate**, *IEEE Transactions on Microwave Theory and Techniques* (To be submitted).

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"Life is a great big canvas, and you should throw all the paint you can on it."

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List of Acronyms

BiCMOS	Bipolar CMOS
BESOI	Bonded and etched back silicon-on-insulator
BOX	Buried oxide
Cz-Si	Czochralski-silicon
CBCPW	Conductor-backed coplanar waveguide
CMOS	Complementary metal-oxide semiconductor
CPW	Coplanar waveguide
CV	Capacitance-voltage
Fz-Si	Float-zone silicon
FIPOS	Full isolation by porous oxidised silicon
HR-Si	High resistivity silicon
IPD	Integrated passive devices
ISM	Industrial, scientific and medical
ITRS	International Technology Roadmap for Semiconductors
pMOS	Metal-oxide-semiconductor with n-type silicon substrate
MOS	Metal-oxide-semiconductor
PARMS	Plasma-assisted magnetron sputtering
PECVD	Plasma-enhanced chemical vapour deposition
PSC	Parasitic surface conduction
RAE	Rotating analyser ellipsometer
RLGC	Resistance, Inductance, Conductance, Capacitance
SEM	Scanning electron microscope
SIMOX	Separation by implantation of oxygen
SOI	Silicon-on-insulator
SOA	Silicon-on-anything
SOS	Silicon-on-sapphire
SOZ	Silicon-on-zirconia
TSV	Through-silicon via
VNA	Vector network analyser

Contents

Chapter 1

Introduction

1.1 High resistivity substrate for low-loss microwave application

The need for high-speed electronic devices and circuits has augmented the development of monolithic microwave integrated circuits (MMICs), whereby the production of CMOS and BiCMOS transistors have been made capable of operating at microwave frequencies (ranging between 300 MHz - 300 GHz) [1]. The integration of microwave circuitry has led to the incorporation of wireless communication in today's cellular (or mobile) and data communication network. Applications of these include (but are not limited to) the operation of Wi-Fi and Bluetooth in the ISM band range [2] for unlicensed usage.

In order to operate in such a super high frequency (SHF) environment, MMIC devices need to be fabricated on low loss, high resistivity substrates. This is achieved by having a significantly reduced number of background free carriers in the substrate, which contribute to substrate losses at high frequency operation. The use of high resistivity substrates for microwave application has been proven to aid improvement on noise isolation and to provide high power transmission efficiency. This will benefit passive components and interconnectors for example, planar inductors, capacitors, coplanar waveguides and microstrips [3–6].

The production of high resistivity substrates for MMIC applications has always been associated with III-V semiconductor materials such as GaAs, GaN and InP, due to the wide band-gap nature of the compound substrates. Having a wide energy band-gap ensures suppression of electrical current conduction which consequently leads to substrate isolation from device operation [7]. Despite their semi-insulating properties, the complexity in creating compound semiconductors (for example, lattice-mismatch problems) increases fabrication cost. Perceiving this as an undesirable factor, silicon, came back into the picture offering less complexity and lower fabrication and manufacturing costs.

However, creating very high resistivity bulk Si substrates is not straightforward since the presence of background carriers generated during monocrystalline Si growth hindered its potential development as a microwave substrate. This is because background carriers in bulk Si create significant current conduction paths that contribute to substrate losses at microwave range. To solve this issue, silicon-on-anything (SOA) and silicon-on-insulator (SOI) technologies were introduced, where the former was realised by transferring silicon-based, fully-processed ICs, onto material such as glass [8, 9].

The latter was firstly introduced with thin film Si being chemically vapour-deposited on highly-insulated elements such as sapphire and zirconia to form silicon-on-sapphire (SOS) [10] and silicon-on-zirconia (SOZ) [11]. Instead of depositing thin film Si on top of other insulators, an alternative approach, known as FIPOS and SIMOX, can be used in which a thin layer of Si film is separated from its bulk structure by oxidised [12] or implanted SiO_2 [13], respectively. Apart from the mentioned methods, more commercially available SOI were introduced through wafer-bonding techniques called Bonded and Etched Back SOI (BESOI) [14] and Smart Cut^{TM} [15]. Two Si wafers, including one which has been oxidised or implanted, were bonded together. The upper top undergoes thinning process until the required thickness is achieved for BESOI, or just above the implanted area for the case of Smart-Cut^{TM}.

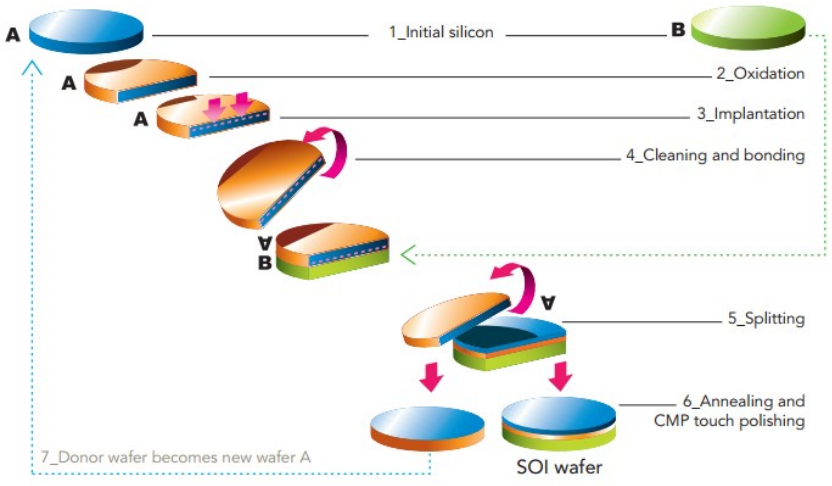


Figure 1.1: Smart Cut^{TM} process engineered by Soitec Inc. for production of SOI wafers [15]

Despite extensive research conducted on SOI technology to create silicon-based microwave substrates, self-heating issues and its associated thermal breakdown caused by separation of devices from bulk Si structures have always been a pressing matter [16–20]. Having thinner SOI oxides to solve thermal isolation problems however will only reduce substrate's isolation from eddy currents. Hence, there continues to be a constant need

to develop high resistivity bulk Si substrate as an alternative to SOI wafers, thereby eliminating the structural complexity.

1.2 Silicon as microwave substrate

International Technology Roadmap for Semiconductors (ITRS) has underlined the importance of high resistivity silicon substrates for integration of passive components in mixed analog/digital RF CMOS devices [21]. Although the emphasis is on compound Si and SOI technology, research on high resistivity bulk Si substrate is becoming increasingly important given its reduced structure complexity, which is translated into reduced fabrication cost.

The basic principle of creating high resistivity bulk Si substrates is to reduce the concentration of background free carriers that provide alternative current conduction paths inside the substrate and consequently generate losses at microwave frequencies. The presence of these parasitic carriers originates from inevitable contamination that occurs during monocrystalline Si growth in the Czochralski process (Cz-Si).

Figure 1.2 illustrates Czochralski crystal-pulling process used to produce monocrystalline Si ingots. High purity polycrystalline Si, called electronic grade silicon are filled into a silica (or quartz) crucible and melted over a high temperature before being pulled out through a crystal-orientated seed to create Si ingot of a specific pulling rate-dependent diameter.

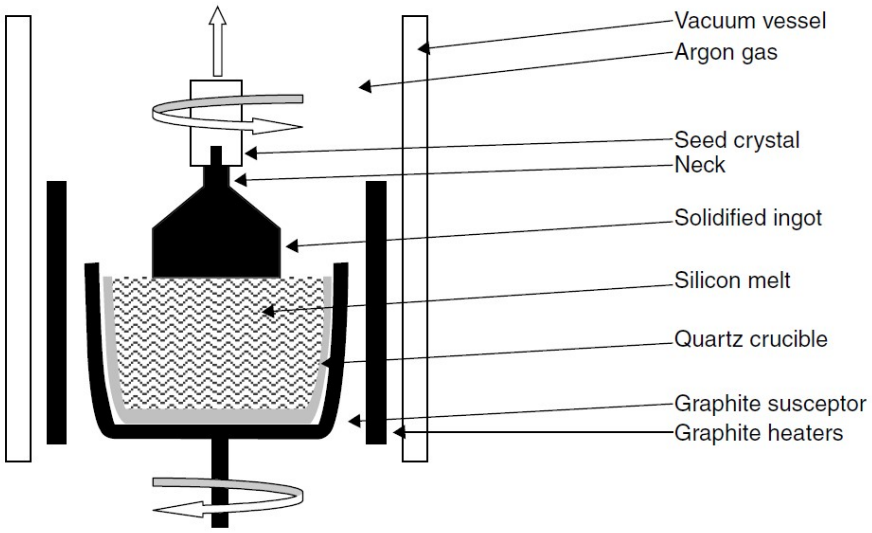


Figure 1.2: Czochralski silicon process [22]

One source of contaminations comes from the silica crucible that holds the melt. During high temperature treatment, the crucible is slightly dissolved and releases 5 to 20 of parts

per million atoms (ppma) oxygen which will then be transported around the vessel in the form of silicon monoxide. In addition to oxygen, a reaction between the crucible and the graphite susceptor (located underneath the crucible to provide mechanical strength) produces carbon monoxide. Apart from oxygen and carbon, low-level contamination also comes from impurities such as boron and phosphorus due to the incorporation of these elements used to generate doped Si substrates for electrical modulation.

The quickest solution to address this issue would be to use the Float-zone (Fz-Si) method for growing Si, where the absence of a silica crucible reduces the level of contamination in the growth process. Nowadays, Float-zone silicon wafers with bulk resistivities up to 70 kΩ-cm, called HiRes^{TM}, are commercially available for the use of microwave circuits and devices in GHz and THz range [23]. However, the largest wafer diameter produced so far using this method is 8". From manufacturing point of view, this means an increase in production cost since, the current standard wafer size for modern CMOS processing is 12" [24]. For a large-scaled, low-cost production, the only alternative to Fz-Si still is Cz-Si. Since growth contamination in Cz-Si is unavoidable, research has been done in terms of modification of its crystalline structure to reduce mobile background free carriers in Cz-Si substrates, and therefore increasing the substrate's bulk resistivity.

One way to achieve this is by employing the proton implantation method. The basic principle of this method is bombardment of protons through the Si surface into its bulk structure, creating defects that trap mobile carriers, stopping them from conducting freely inside the structure. In 1978, Aoki *et al.* proposed the growth of high resistivity silicon through an oxygen or nitrogen ion beam implantation technique [25]. Using an implantation energy of 200 keV, oxygen was injected through polycrystalline silicon, amorphous silicon and a single crystal layer, to produce semi-insulating Si layer, with resistivities between 10^7 to 10^{11} Ω-cm.

The work was followed by Li *et al.* in 1989 where they managed to produce a silicon layer with a resistivity of 10^3 Ω-cm, through proton-implantation at an energy of 180 keV, followed by two-step annealing process [26]. The formation of a buried defect layer and impurity-gettering create a defect-free zone at the top of the silicon layer. In 1998, Liao made use of a higher implantation energy (30 MeV) to accelerate protons and create deep level traps in a lightly-doped silicon wafer, increasing its resistivity to 10^6 Ω-cm [27]. Using a slightly lower implantation energy than Liao i.e. 10 MeV, and adding a two-step annealing process in his work, Wu *et al.* [28] succeeded in producing silicon wafer of the same resistivity. Rashid *et al.* reported a resistivity value of 10^5 Ω-cm, achieved through their six-step implantation method using an implantation energy of 17.4 MeV [29].

Successful attempts in creating high resistivity bulk Cz-Si has led to its potential as a microwave substrate, comparable to commercially available semi-insulating III-Vs and SOIs. However, focussing on increasing bulk resistivity is not the only issue that matters

in developing low loss microwave substrate. The existence of parasitic surface conduction (PSC) at bulk Si surface causes degradation of overall substrate's resistivity and introduces additional losses for devices operating at high frequency.

1.3 Parasitic surface conduction effect in bulk high resistivity silicon substrate

Parasitic surface conduction (PSC) effect was first explained by Reyes *et al.* where an increase in coplanar waveguide (CPW) attenuation was reported in both work for CPWs fabricated on high resistivity Si substrates [30, 31]. According to Reyes, there exists a formation of either accumulation or inversion at the Si surface which can potentially cause a drop in surface resistivity and eventually contribute to an increase in losses. In 1999, Wu *et al.* presented quantitative analysis for Reyes' hypothesis, confirming the existence of a low resistivity region at oxide-semiconductor surface, due to population of carriers during accumulation or inversion [32].

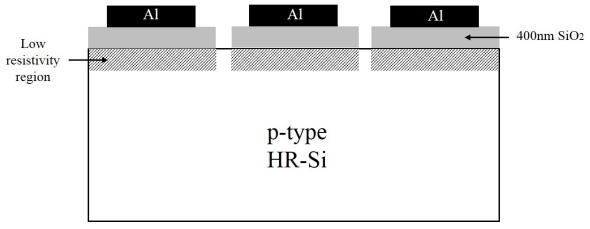


Figure 1.3: Non-continuous oxide pattern between HR-Si substrate and CPW conductor line [32].

He also proposed the use of a non-continuous oxide pattern to reduce attenuation loss since losses due to the inversion layer, situated right beneath the CPW lines, were said to be insignificant. It was said that the loss was mainly contributed to the continuous oxide pattern. In addition to that, non-continuous patterns allow DC-blocking role to be taken by the readily formed thin layer native silicon oxide when exposed to air at room temperature. The proposed structure is shown in Figure 1.3, where the loss was recorded to decrease from 18 to 3 dB/cm at 30 GHz.

However, this has not been seen as an ideal, reliable and repetitive solution. Later the same year, Gamble *et al.* came up with the idea of introducing a high density of traps in between the oxide-silicon interface in order to trap electrons and prevent low resistivity areas, whilst still having a continuous oxide to act as the passivation layer [33]. A 0.6-μm-thick polycrystalline silicon was used as the trapping layer to give an attenuation loss of 1.08 dB/cm at 30 GHz, a value lower than the one obtained by Wu. Following Gamble's work, more work has been conducted on introducing trap-rich layers to surface-passivate high resistivity silicon. Lue incorporated a 300-nm-thick polysilicon film beneath a 100-nm-thick SiO_2 layer, obtaining low insertion loss [34]. The same thickness of polysilicon

layer was suggested by Lederer *et al.* to be used as surface-passivation layer after they successfully simulated the impact of interface-related oxide charges associated with high resistivity SOI substrate [35].

Apart from depositing a poly-Si layer to suppress surface charge accumulation, high dose of Ar-implantation was also taken as an approach by utilising the bombardment of Ar atoms onto the silicon surface and forming an amorphised layer in between oxide and silicon substrate, providing a high density trap region. In Jansman's work, an implantation dose of 10^{15} cm^{-2} was introduced at the interface followed by annealing to restore silicon crystallisation. As a result, an indistinguishable quality factor value was obtained for 3-nH-inductor with Argon-passivated layer on a high resistivity silicon substrate in comparison to inductors on an alumina substrate [36]. Using the same implantation dose, an attenuation value of 0.2 dB/mm was obtained at 30 GHz for CPW configured baluns implemented in Valletta's work [37]. In 2005, Spirito *et al.* showed the potential of thin amorphous layer formed using Ar-implantation technique by obtaining an attenuation loss of 0.15 dB/mm at 30 GHz for its coplanar lines fabricated on high resistivity silicon along with other passive and active device structure realised from their in-house bipolar process called DIMES-04 [38].

In 2011, Chen *et al.* has established a new method in enhancing surface passivation and it was done by making use of the deposition of nanocrystalline silicon layer using hot-wire chemical vapour deposition proposed by Li *et al.* in 2008 [39]. A 100-nm-thick nanocrystalline silicon was deposited in between a high resistivity silicon substrate and 300-nm-thick SiO_2 layer. The attenuation of CPW fabricated on this structure was measured to be 1.05 dB/cm at maximum frequency of 20 GHz [40]. Later that year, Wang increased the thickness of nanocrystalline silicon layer to 400 nm and managed to further reduce the attenuation to only 0.69 dB/cm at 20 GHz, showing the effectiveness of nanocrystalline silicon in suppressing surface conduction effect, caused by bias-induced charges associated at oxide-semiconductor interface [41].

To date, the proposed solutions involve an additional layer to be incorporated in between Si substrate and SiO_2 (such as polySi and amorphous Si) to introduce a high density of traps, to trap carrier charges from accumulating at the surface. Apart from the thermal stability issues revolving around amorphous Si, the added cost in terms of processing time and tackling complexity during wafer processing, especially stages related to poly-Si deposition, have led to serious setbacks. Hence, a completely different approach to provide an alternative solution for PSC suppression associated with high resistivity bulk Si substrates would be desirable.

In this work, suppression of PSC is being achieved by a concept called deep-level doping compensation method, where it comprises of Au atoms being introduced into Si substrates through ion-implantation process and activated via subsequent thermal annealing procedure. Implementing this method eliminates issues related to damaging Si surface,

through bombardment of atoms that occur during the Si-amorphisation process.It also avoids the underlying physical and chemical complexities seen when using additional poly-Si or nanocrystalline Si layers on top of high resistivity Si substrates.

Using low-cost Czochralski-processed Si substrates as the starting material, deep-level doping compensation approach is seen as a promising candidate to create high resistivity Si wafers with full suppression of PSC effect, with a less-complex process procedures contributing to reduced fabrication costs.

1.4 Thesis outline

The potential of deep level doping compensation method to suppress parasitic surface conduction effect on high resistivity bulk silicon substrates for microwave application is being studied in this work. Electrical and microwave components were designed, software-simulated and fabricated onto Au-compensated high resistivity bulk Si substrates (HR-Si) to observe its potential as low-loss microwave substrate by providing a more conducive platform for reduction of background free carriers and suppression of PSC-dependent charge carriers inside Si substrates.

Chapter 2 explains the underlying theory and potential microwave applications of high resistivity Si substrates developed through deep-level doping compensation method. An in-depth analysis on the creation of Au-compensated HR-Si substrates is discussed in the later section, which include the introduction of Au atoms into Si through ion implantation and its subsequent activation annealing procedures.

Chapter 3 discusses the electrical and microwave components used in this work with the basic metal-oxide-silicon structure; capacitors, coplanar waveguides and meander inductors. The chosen design for each components is explained and examined before being carefully realised onto Au-compensated HR-Si substrates through a series of fabrication processes. Capacitor structure was used to characterise the behaviour of bias-dependent charge carriers associated with Si-SiO_2 interface whereas coplanar waveguides and meander inductors were used to study the microwave loss properties of Au-compensated Si substrates with relation to PSC effect at the Si surface.

Chapter 4 evaluates the effect of surface charges from capacitance-voltage characterisation measured on the fabricated capacitor structures. Formation of charges at Si-SiO_2 interface provides an insight regarding the bahaviour of charge carriers in Au-compensated HR-Si substrates with application of DC bias.

Chapter 5 examines the potential suppression of PSC effect using Au-compensated HR-Si substrates, where coplanar waveguides were used as the analysed structure. Microwave loss properties of this particular structure are discussed with respect to DC bias influence.

Characterisation of effective substrate resistivity is included at the end of the section to quantify the effect of PSC on Au-compensated HR-Si.

Potential application of Au-compensated HR-Si substrates as microwave substrate is further illustrated in Chapter 6. Microwave characteristics in terms of Q factor performance of meander inductors are being analysed in this chapter with the effect of PSC suppression on performance of integrated passive components is evaluated.

Last but not least, Chapter 7 represents the summary of work presented in the thesis.

Chapter 2

Realisation of Au-compensated High Resistivity Silicon

Deep-level doping compensation method is used in this work to develop high resistivity Si substrates for microwave application. Elemental gold (Au) is used to compensate for background free carriers in low resistivity Czochralski silicon substrates, by creating deep level traps inside Si band gap and enhancing substrate's resistivity. Using this method, Au is introduced into Si via ion-implantation process and activated through high-temperature annealing procedure to achieve optimum level of compensation.

2.1 Impurities in Silicon

Pure (or intrinsic) Si contains no impurities and is electrically insulating due to substrate having a very low number of electrons and holes inside the structure. Figure 2.1 shows the band diagram of intrinsic Si, where E_{g} is the forbidden band gap, and E_{C} and E_{V} represent the bottom edge of conduction band and the top edge of valence band, respectively. Fermi level, E_{i} lies right in the middle of E_{g} showing the intrinsic nature of this structure.

Figure 2.1: Si band diagram with E_{g}=1.11eV

The intrinsic concentration of Si can be expressed as a function of temperature, as given by Misiakos [42]:

$$n_i(T) = 5.29 \text{ x } 10^{19} \, (\frac{T}{300})^{2.54} \exp(-\frac{6726}{T}) \tag{2.1}$$

Using Misiakos' equation, n_{i} is found to be 9.696 x 10^9 cm^{-3} at room temperature and the corresponding intrinsic Si substrate resistivity is 2.3 x 10^5 Ω-cm.

In reality however, it is almost impossible to have pure Si without impurities, considering the unavoidable, contaminated environment of the growth of its monocrystalline structure inside silica crucible. Even if that is not the case, impurities are often deliberately introduced during Si growth to provide electrical modulation of the substrate by generating a controlled number of free carriers. This process is called doping. Generation of free carriers occurs as a result of impurities or dopants undergoing ionisation process, where electrons (holes) are excited to conduction band (valence band) during ionisation.

There are two types of impurities; shallow impurities and deep impurities. The former require small energy that is equal to thermal energy (kT) to ionise due to energy level being close to band edges whereas the latter, having energy level situated far from band edges are harder to ionise and require at least five times the thermal energy for that.

Shallow impurities in Si are always associated with dopants introduced from Group III or Group V elements to produce p-type or n-type Si. During ionisation, Group III dopants accept electrons from Si and therefore are called acceptors. As a result, substrate becomes p-type. On the other hand, Group V dopants readily give up electrons to Si to become donors and make it n-type.

Figure 2.2 illustrates energy band diagrams of Si with the introduction of shallow dopants from Group III (e.g. Boron) acceptors and Group V (e.g. Phosphorus) donors. Donor level, E_{D} and acceptor level, E_{A} are generated inside Si forbidden band gap, subsequently shifting Fermi level, E_{i} near conduction band and valence band, respectively. Ionisation of shallow donors causes electrons to be promoted from E_{D} to E_{C} whilst ionisation of shallow acceptors causes holes to fall down from E_{A} to E_{V}. In both cases, they have become carriers which are free to conduct within the bands. The corresponding conductivity of the substrate is then given by:

$$\sigma_e = nq\mu_e \tag{2.2}$$

$$\sigma_h = pq\mu_h \tag{2.3}$$

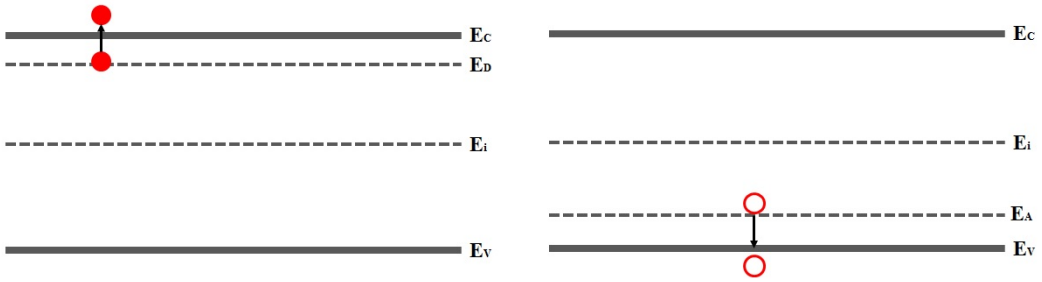


Figure 2.2: Energy band diagram of Si with dopant impurities. (*Left*) N-type doping by shallow donors. (*Right*) P-type doping by shallow acceptors.

for n-type and p-type Si, respectively. n and p are electron and hole concentrations, with each representing majority carriers in that particular Si substrate. q is electronic charge given by 1.6 x 10^{-19} C, whilst μ_e and μ_h correspond to electron and hole mobilities at room temperature.

When shallow donors and shallow acceptors co-exist together inside Si, compensation of doping occurs. Electrons contributed from donor atoms fall into E_{A} and ionise acceptor atoms without generating any free carriers. Their concentration determines the resultant type of Si. If donor concentration, N_{D} is much larger than acceptor concentration, N_{A}, the substrate becomes n-type and vice versa. However, if there are equal numbers of N_{D} and N_{A}, full compensation happens and Si has a complete absence of free carriers. Figure 2.3 shows compensation doping process when N_{D}>N_{A}. As can be seen from the figure, some of the electrons from E_{D} ionise all acceptor atoms located in E_{A} and the remaining ones are promoted to conduction band.

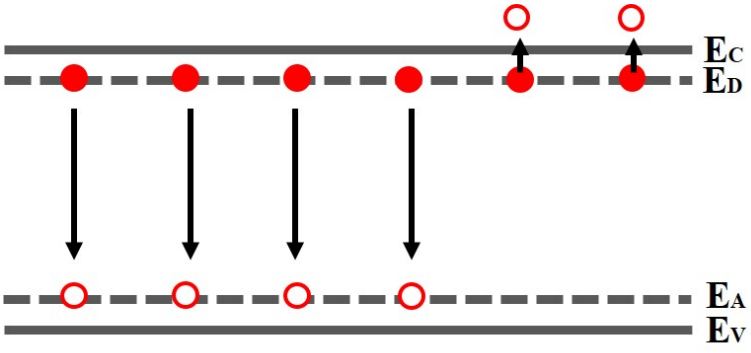
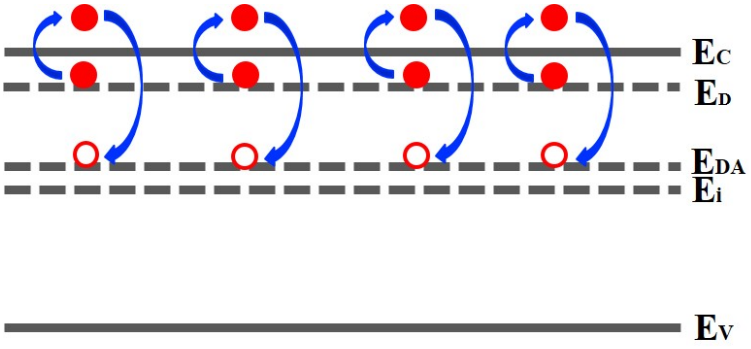


Figure 2.3: Compensation doping process in Si for N_{D}>N_{A}.

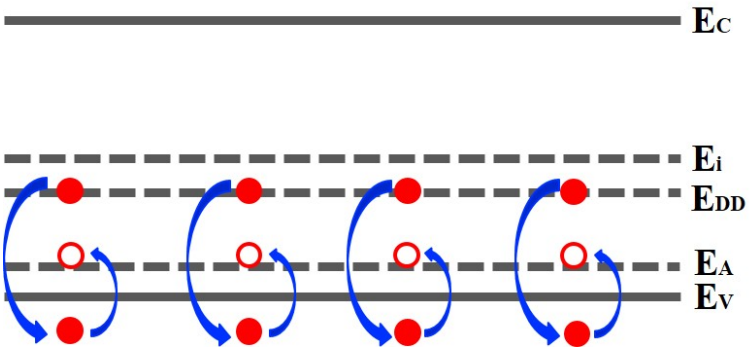
2.2 Deep Level Doping Compensation

Compensation doping can also occur between shallow impurities and deep impurities where the process is illustrated in Figure 2.4. Shallow donors are being compensated by deep acceptors, N_{DA} whereas shallow acceptors are being compensated by deep donors, N_{DD}.

For compensation of shallow donors by deep acceptors, N_{DA} are negatively charged and attracting minority carrier holes to be trapped at $E_{\mathrm{DA}}{}^{-}$ level. Electrons from E_{D} which are initially excited to conduction band fall down to this level and recombine with holes. Meanwhile, the positively charged N_{DD} in the latter case are trapping minority carrier electrons at $E_{\mathrm{DD}}{}^{+}$ level whilst majority carrier holes fall into valence band at the same time. The trapped electrons subsequently fall into valence band to recombine with holes. In both cases, no generation of free carriers occurs.



(a) Shallow donors are compensated by deep acceptors, N_{DA}



(b) Shallow acceptors are compensated by deep donors, N_{DD}

Figure 2.4: Compensation doping process between shallow impurities and deep impurities.

The reduced generation of free carriers achieved from deep level doping compensation has become the basis of developing new method in producing high resistivity Czochralski silicon. Deep levels introduced into Si bandgap pin the Fermi level near intrinsic and trap carriers inside Si lattice. Hence, Si substrate with high resistivity can be achieved.

Study shows that transition elements are potential candidates for this method [43]. The key points in realising deep level doping compensation using transition metal elements are the amount of energy required to induce ionisation i.e. deep level position, and suitable dopant concentration to produce optimum compensation [44]. The first step is to determine the Fermi level and this can be done by solving the charge neutrality equation given by:

$$p + \sum_i N_{D_i}^+ - n - \sum_j N_{A_j}^- = 0 \tag{2.4}$$

where $N_{D_i}^+$ and $N_{A_j}^-$ is the ith ionised donor and jth ionised acceptor concentration for a total impurity density of N_{D_i} and N_{A_j} respectively. For the purpose of this work, it is assumed that only a pair of donor and acceptor levels are created by deep level dopants in Si bandgap. Hence, the terms can be dropped to N_D^+ and N_A^-, where the expressions are derived as [45]:

$$N_D^+ = \frac{N_D}{1 + g_D e^{E_F - E_D/kT} + e^{2E_F - E_A - E_D/kT}} \tag{2.5}$$

$$N_A^- = \frac{N_A}{1 + g_A e^{E_A - E_F/kT} + e^{E_A + E_D - 2E_F/kT}} \tag{2.6}$$

As for free hole and electron concentrations, n and p, the expressions are given by:

$$n = N_C e^{-(E_C - E_F)/kT} \tag{2.7}$$

$$p = N_V e^{-(E_F - E_V)/kT} \tag{2.8}$$

where k is the Boltzmann constant and T is the temperature taken as 300 K (room temperature). N_C and N_V are effective density of states in the conduction band and valence band respectively. In the case of silicon, these values are taken as 2.8 x 10^{19} cm^{-3} for N_C and 1.04 x 10^{19} cm^{-3} for N_V at room temperature [46]. Conduction band energy level, E_C equals energy band gap of silicon, which is 1.12 eV, with respect to $E_\mathrm{V} = 0$ eV.

Equations above have been used together to solve for Equation 2.4 to find p and n. Once these values have been found, resistivity, ρ can be calculated using:

$$\rho = \frac{1}{\sigma} = \frac{1}{nq\mu_e + pq\mu_h} \tag{2.9}$$

where μ_e and μ_h are electron and hole mobility respectively. To analyse the impact of incorporating deep level impurity to compensate for shallow levels in Si, calculations have been done for p-type Si, Boron-doped with minimum concentration of 10^{13} cm^{-3} at $T = 300$ K. Acceptor energy level of Boron in Si was taken to be $E_V + 0.045$ eV and g_D and g_A are 2 and 4 respectively.

There were two variables that have been considered in this study:

1. Deep donor energy level below E_C
2. Concentration of deep donor impurities in Si

Figure 2.5 shows the corresponding Si resistivity at 300 K with respect to the concentration of donor impurity, with generic energy level positions below conduction band edge, E_D.

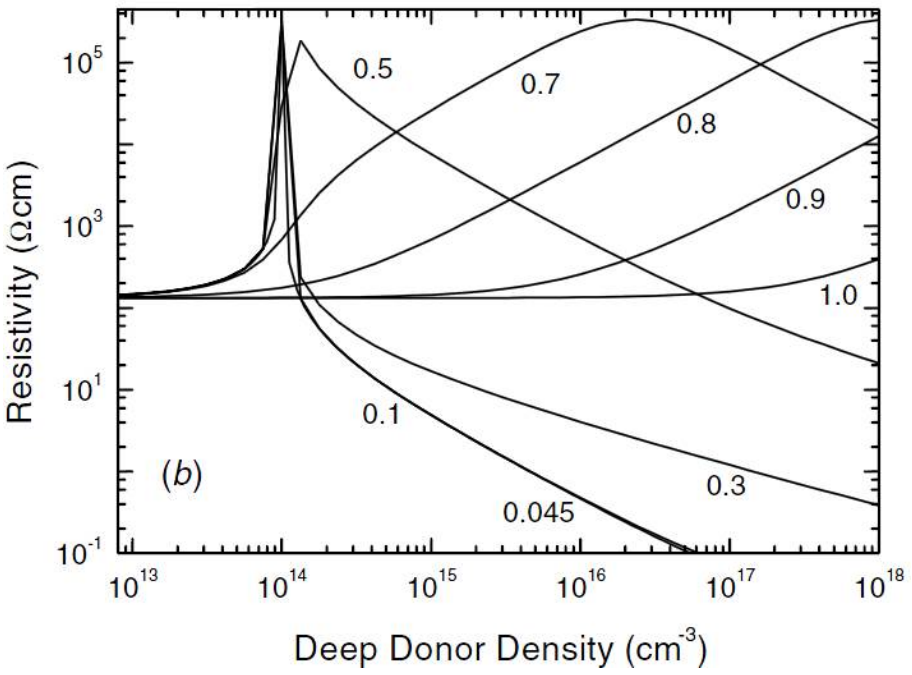


Figure 2.5: Calculated resistivity as a function of donor impurity concentrations for background B concentration of 10^{14} cm^{-3} at generic E_D [44].

From the figure, it can be seen that the resistivity increases with increasing donor concentration until it reaches a maximum value, and then falls back. Initially, N_D is insufficient to compensate for background Boron acceptors hence, resistivity is still low due to undercompensation. Optimum compensation occurs when resistivity reaches its maximum value, indicating that the number of donors exist exactly compensate for shallow Boron acceptors whilst overcompensation due to excess number of ionised donors happens when resistivity starts to decline with higher concentration of deep donor, making it prone to becoming n-type.

Element and site	**Donor level below N_C**	**Acceptor level above N_V**
Co	0.89	0.82
Pd	0.84	0.90
Au	0.78	0.56
Ag	0.75	0.55

Table 2.1: Substitutional position of energy levels of transition elements in Si [43].

Shallow donors can be distinguished from the figure (E_D<0.3), in which the maximum resistivity has a sharp peak and the value occurs when donor concentration equals background Boron concentration, $N_D = N_A$. The reason is that, donor energy level is nearer to conduction band than intrinsic Fermi level, hence, almost all donors get ionised and take part in compensating for shallow acceptors. A slight increase in concentration after this will cause overcompensation and change the material to n-type. However, for E_D≈0.5, energy level is closer to intrinsic Fermi level compared to conduction band. Less fraction of ionised donor indicates gradual change in compensation and therefore, resistivity remains high over a wider range of donor concentration, provided that N_D>N_A.

Therefore, using sufficiently deep donors, i.e. where E_D≈0.5, a value of 5 x 10^5 Ω-cm can be achieved for p-type Si without the need of tight control over donor concentration as the resistivity will remain high over a range of relatively low concentration values. According to Mallik *et al*, the same conclusion can be drawn in the case of n-type Si, where a sufficiently deep acceptor can be used to achieve high resistivity n-Si without the need of tight control over its concentration.

This study has been extended by including a number of transition elements, having relatively deep donor and acceptor levels in Si. Table 2.1 shows the substitutional position of energy levels of the elements. Using the equations gathered earlier in this section, a graph of Si resistivity at 300 K is drawn as a function of Au, Ag, Co and Pd for three different background Boron concentrations; 10^{13}, 10^{14} and 10^{15} cm^{-3}. The results are shown in Figure 2.6.

As can be seen in the figure, the addition of deep dopant Au, Ag, Co and Pd into Si increases the resistivity of silicon with at least three orders of magnitude. In general, resistivity starts to increase at a value of $N_D = N_A$ and remains high over a range of concentrations, confirming the initial trend observed in Figure 2.5. Hence, these elements are suitable for deep level doping compensation technique to compensate for shallow acceptor/donor levels in silicon and increase its resistivity, with particularly the Au and Ag acceptor levels near midgap being very suitable.

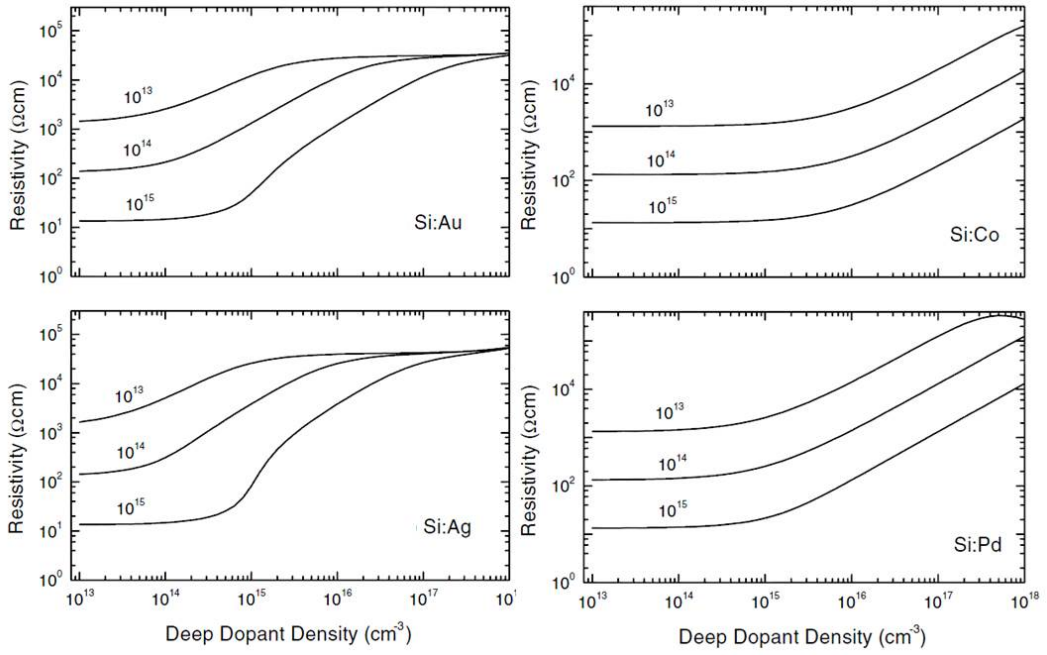


Figure 2.6: Calculated Si resistivity as a function of Au, Ag, Co and Pd for three different background B concentrations [44].

2.3 Gold (Au) as Deep Level Dopant

Au has been chosen as the deep level element in this work. Apart from the apparent reasons discussed before i.e. less need for tight control over dopant concentration and minimal overcompensation effect, Au-doping has been successfully proven to be able to increase resistivity of silicon in experimental observations done previously [45], [47]. Wang *et al.* has shown that a value of 100 kΩ-cm can be achieved by introducing deep level Au atoms into silicon wafer through diffusion process. Jordan *et al.* has also managed to produce a gold-doped silicon wafer with resistivity of 180 kΩ-cm through deposition using E-beam or thermal evaporation and high-temperature annealing to in-diffuse Au into the substrate [48]. There was no evidence reported for the potential of Pd as deep level dopant, and even though there were evidences for Ag and Co in [49] and [50], the potential of Au as deep level dopant is still comparatively more well-studied and has provided the strongest basis for the production of high resistivity silicon for microwave application through deep level doping compensation technique.

Collin *et al.* reported that Au introduces equal concentrations of donor and acceptor levels and since Au atoms act as recombination centers in silicon, they generate a pair of energy levels; acceptor state at ionisation energy of 0.54 eV from conduction band and donor state at ionisation energy of 0.33 eV from valence band [51]. According to Bemski *et al.*, these ionised states do not exist with the presence of one another [52]. In other words, the only active state in n-type Si will be the acceptor level at 0.54 eV from conduction band and the only active state in p-type Si will be the donor level at 0.33

eV from valence band. Therefore, unlike Manganese which only creates deep level donor in Si and can only compensate for p-type Si [53], Au can compensate for both n- and p-type Si due to its deep level nature in both conditions. Not only that it can enhance silicon resistivity, a large range of concentration can be used to achieve this, making it desirably beneficial during wafer-processing stage.

Au can occupy both, interstitial and substitutional sites in silicon [54] but deep levels in silicon are created only by Au occupying substitutional sites. Hence the diffusion process needs to be well controlled to achieve the required substitutional positions. Since substitutional Au has lower diffusivity than interstitial Au [55–57], diffusion of Au occurs, first, predominantly in the interstitial sites before exchange of sites takes place, and the occupancy becomes subsitutional. At temperature above 800 °C, the interchange between interstitial Au and substitutional Au is controlled by the 'kick-out' mechanism [58]. This means that Au diffuses through lattice interstitial, kicks out a silicon atom and substitute for its lattice position, where it is relatively immobile. The mechanism can be shown as:

$$Au_i \Leftrightarrow Au_s + I \tag{2.10}$$

where I is self-interstitial silicon. Figure 2.7 in the next page illustrates the mechanism in three subsequent processes.

The out-diffusion of self-interstitial silicon to the silicon surface act as infinite sink, resulting in a 'U-shaped' concentration profile. Figure 2.8 shows spreading resistance profiles of silicon substrates implanted with different doses of Au and annealed at 950 °C measured by our group in University of Southampton [59]. It can be seen that Au concentration is the lowest at the center of the substrate, indicating longer time taken to reach its substitutional solid solubility value. Meanwhile, concentration at front and back surfaces are the highest due to rapid diffusion of interstitial Au into silicon and out-diffusion of self-interstitial silicon to the surfaces.

Jordan calculated the solubility of Au in silicon for a practical limit of Boron concentration in Czochralski silicon, [B] = 5 x 10^{13} cm^{-3} for temperature ranging between 400 °C to 1400 °C using thermodynamic data from Schröter [43] and Au-Si phase diagram taken from [60]. From Figure 2.9, it can be seen that a certain temperature is required to introduce a specific amount of Au into silicon to increase silicon resistivity and that its solubility increases with temperature until it reaches a plateau at T = 1300 °C for [Au] = 3 x 10^{16} cm^{-3} before slowly declining at temperature above that. To achieve a minimum resistivity of 3 kΩ-cm required for low microwave absorption loss [31, 61, 62], a temperature of around 800 °C is required. This value corresponds to the minimum temperature where 'kick-out' mechanism takes place. A higher temperature to create high resistivity substrate is however preferable.

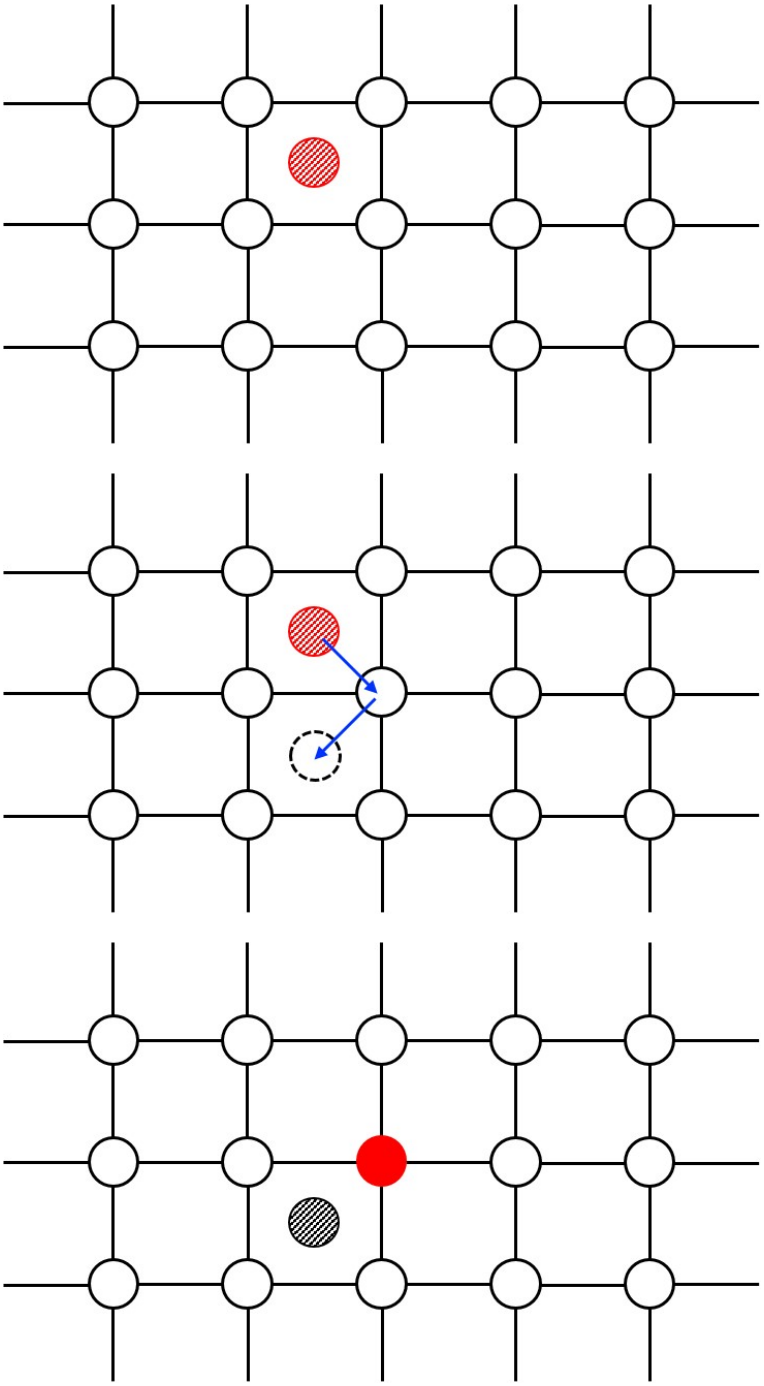


Figure 2.7: 'Kick-out' mechanism in Si by Au atoms. (*Top*) Diffusion of Au atom in Si by occupying interstitial site. (*Middle*) Au atom kicks out Si atom to occupy substitutional site. (*Bottom*). Au atom in substitutional site with self-interstitial Si.

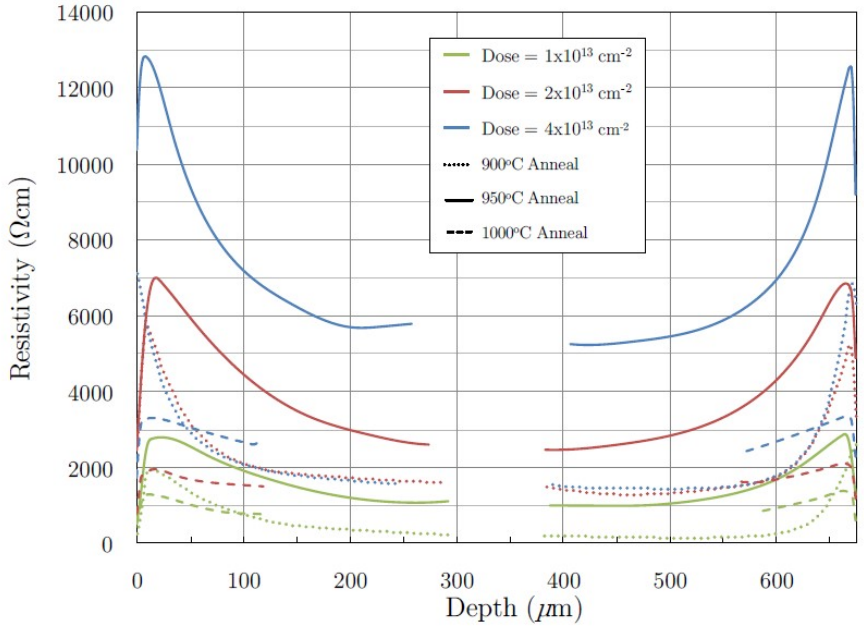


Figure 2.8: Spreading resistance profiles of Au-implanted Si samples annealed at 950 °C as measured in [59].

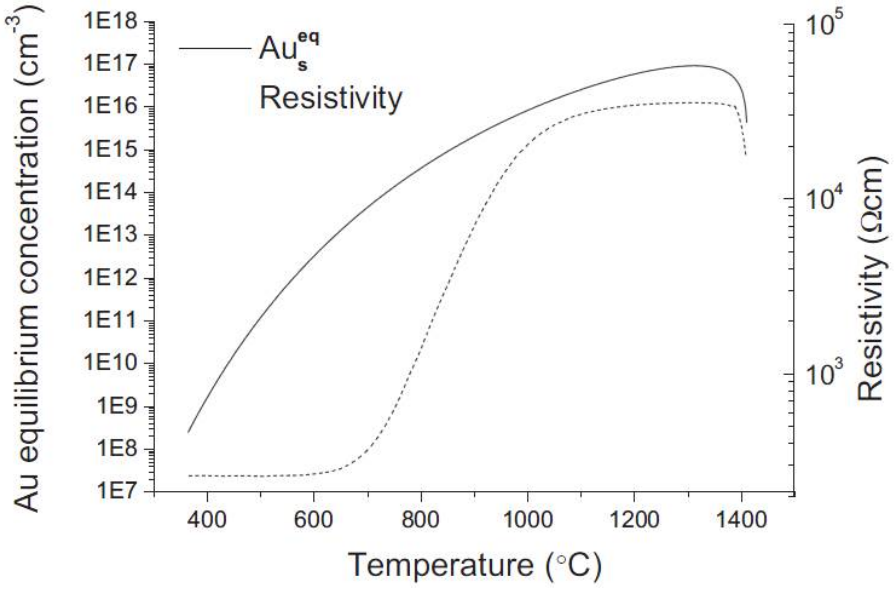


Figure 2.9: Calculated solubility of Au in Si and its corresponding resistivity [48].

2.4 Implementation of Au-compensated HR-Si in microwave technology

High solubility implies high diffusivity [63]. The high diffusivity nature of Au serves as an excellent metallisation contact material but is detrimental for silicon wafer-processing, as Au may diffuse into the active region on silicon substrate, degrading device performance through unwanted compensation or trappings. In response to this, the applications of Au-compensated HR-Si substrates are only focussing on specific RF-MMIC technology such as integrated passive devices (IPDs) [64, 65] and 3D-integration using Through-Si vias (TSV) [66], as well as the realisation of SOI devices with buried oxide (BOX) as diffusion barrier in between handle and active Si wafers [47, 48]. The incorporation of Au-compensated Si into these technologies was based on one principle, and that is to have active devices as far away as possible from the substrate to prevent it from 'killing' those devices. Figure 2.10 illustrates the potential applications of Au-compensated Si substrates in microwave technology.

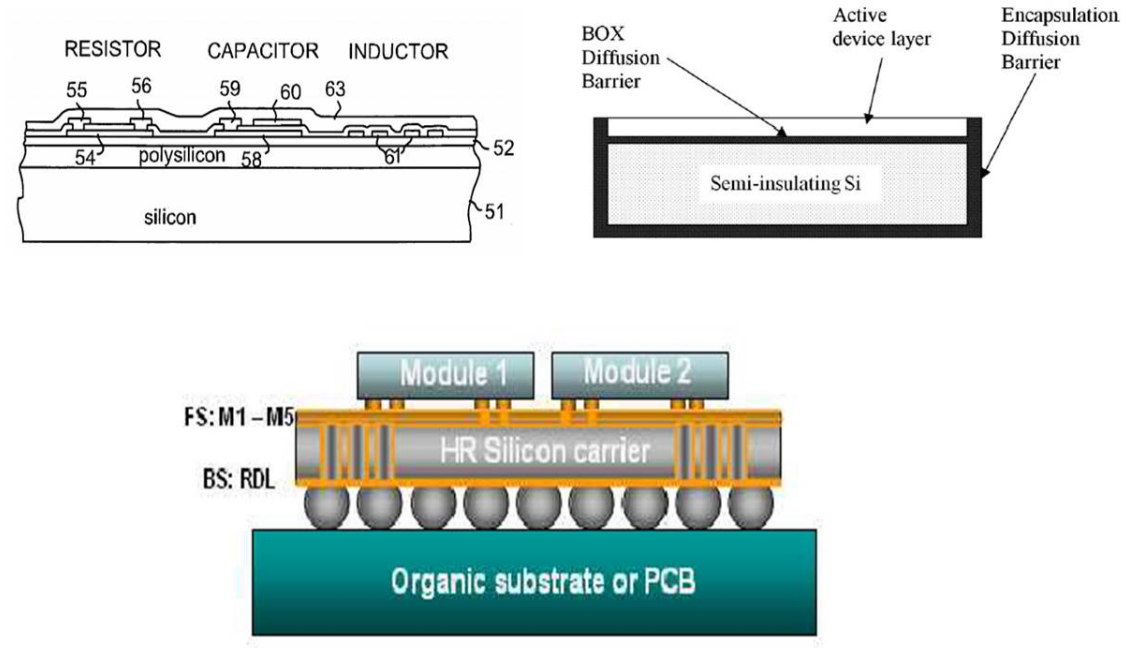


Figure 2.10: Potential applications for implementation of Au-compensated Si substrate. (Top left) Integrated Passive Devices [65]. (Top right) SOI device with BOX [48]. (Bottom) TSV for 3D-integration [66].

Efforts have been made in our group to initiate the use of Au-compensated HR-Si as microwave substrates where integration of low-loss coplanar waveguides and high Q-factor spiral inductors were successfully achieved [67,68]. We reported an observed losses of 0.3 dB/mm at 67 GHz for coplanar waveguides fabricated on naked Au-compensated HR-Si substrates and improved Q-factor performances of 50-nH spiral inductors. The

results are shown in Figure 2.11, Figure 2.12 and Figure 2.13 where the explanation of these characteristics follows from the rest of the thesis.

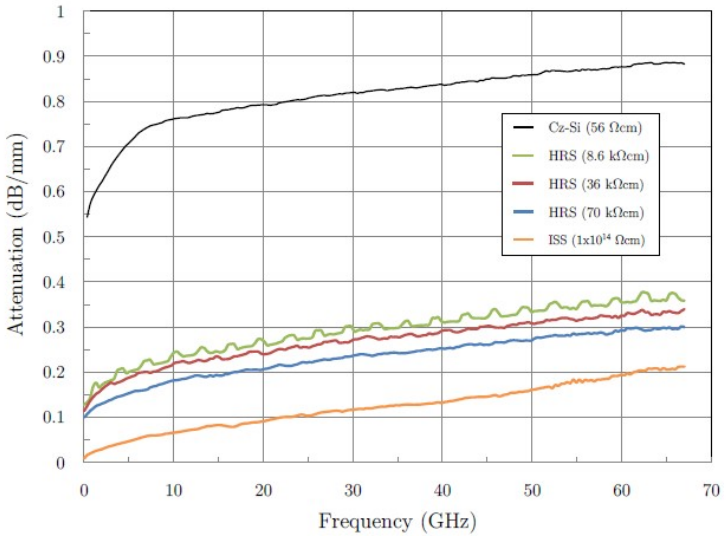


Figure 2.11: Reduced CPW attenuation loss on Au-compensated Si substrate achieved by Hashim *et al.* [67].

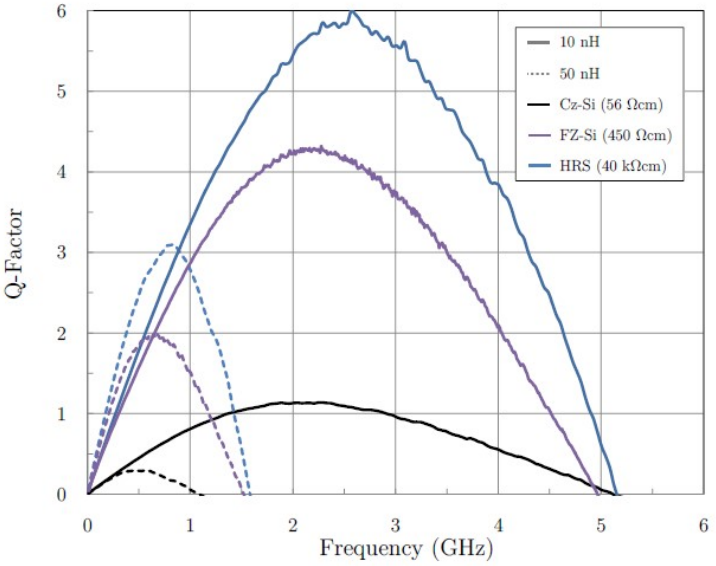


Figure 2.12: Improved Q factor of wire-bonded overpass spiral inductors on Au-compensated Si substrate achieved by Abuelgasim *et al.* [68].

Despite the promising results shown in this previous work to illustrate the potential of deep-level doping compensation method in reducing substrate losses in microwave frequency, a critical issue associated with silicon substrate has not been addressed. As explained in Chapter 1, high resistivity Si substrate suffers from parasitic surface conduction. Field-dependent charges will accumulate at silicon-oxide interface to form a low resistivity region which then contributes to additional losses at microwave frequency and counter-acting the beneficial effect of having high resistivity Si substrate. A high

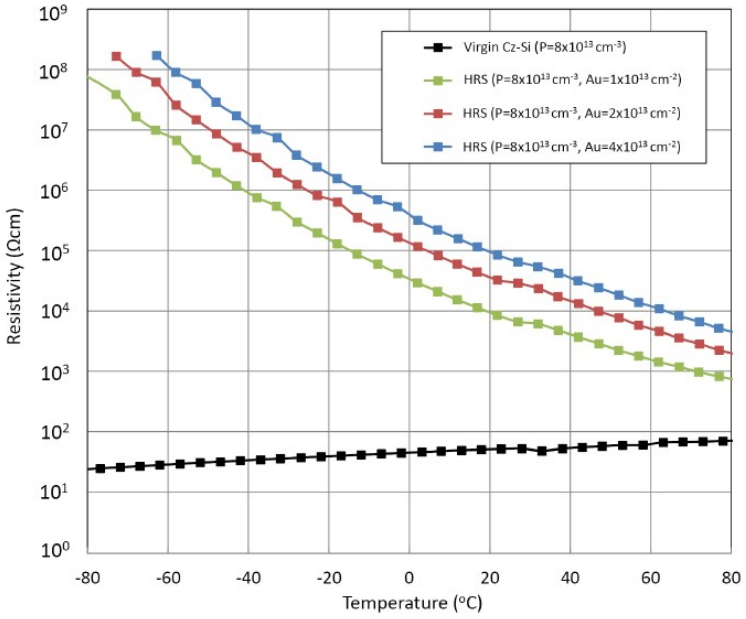


Figure 2.13: Resistivity as a function of temperature for standard Cz-Si and Au-compensated HR-Si substrates with three different implantation doses [68].

resistivity substrate that losses its characteristic upon application of bias voltage is a meaningless improvement.

2.5 Developing Au-compensated High Resistivity Silicon Substrates

One way to prevent charge formation hence suppressing PSC effect is to introduce high density of traps at silicon surface. To tackle this issue, Au-compensated HR-Si substrates created through deep-level doping compensation technique will be utilised to observe its potential to serve as a trapping platform for PSC-dependent interface charges in bulk Si substrate. The first step in creating PSC-free Au-compensated HR-Si substrates is to optimise Au-implantation process and its activation-annealing procedure.

In order to do that, 6-inch Czochralski-grown silicon wafers with $< 100 >$ crystal orientation have been chosen as the starting materials. The wafers were n-type, Phosphorus-doped having average wafer thickness of 675 μm with nominal resistivity ranging between 50-60 Ω-cm. 20-nm-thick sacrificial oxide has been grown on top of the wafers through dry oxidation process in Tempress furnace at 1000 $^{\circ}$C for 15 minutes to provide protection against implantation damage and to prevent out-diffusion of gold during subsequent annealing process.

Au atoms were introduced at the backside of the wafers with dose of 4 x 10^{13} cm^{-2} at an energy of 100 keV using ESPRC ion-implantation facility located at the University

of Surrey. Once implanted, the wafers were treated under annealing condition of 950 °C for 1 hour in Argon environment to activate the Au dopants. The implantation details and annealing temperature were optimised values obtained in [68]. Accordingly, the combination of this particular implantation dose and annealing temperature provides the highest resistivity enhancement.

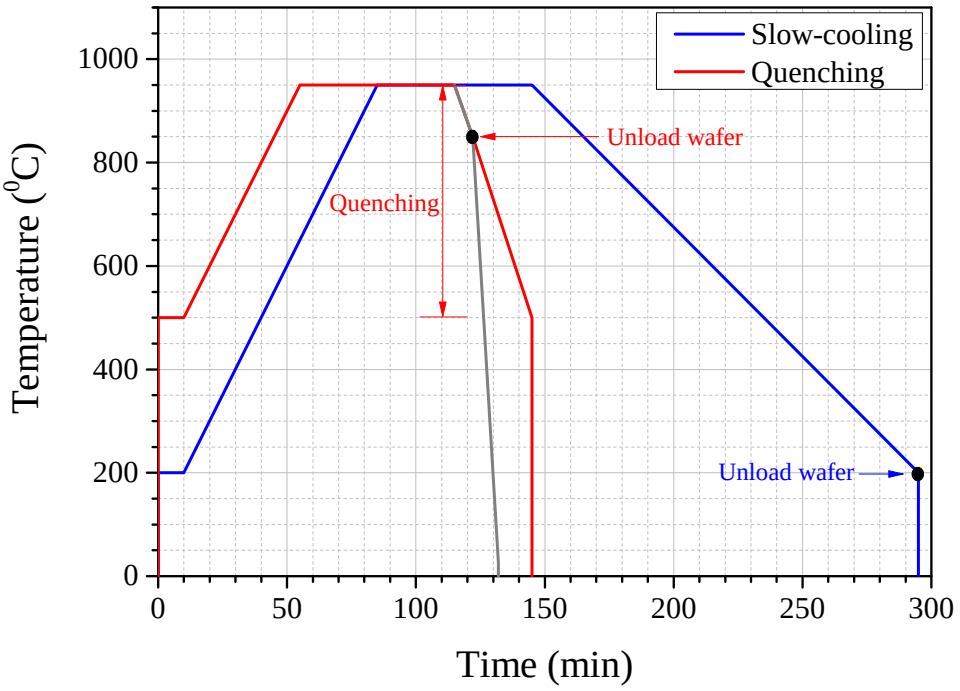


Figure 2.14: Temperature process flow in the furnace for annealing slow-cooling and quenching conditions of Au-compensated HR-Si substrates. The grey line represents the actual temperature gradient of wafers after being taken out from the furnace in quenching condition.

By keeping the annealing time and temperature to be the same, annealing condition is further optimised in this work with three different conditions being considered. The first and second conditions are called slow-cooling and quenching process respectively, by which the implanted wafers in former condition were put under slow-rate cooling temperature environment whereas wafers in latter condition underwent rapid cooling after annealing took place in the furnace. The third condition is the combination of both processes, where the implanted wafers go through two annealing process with different cooling conditions; firstly with slow-cooling and secondly with quenching.

Figure 2.14 describes temperature process flow in the furnace in both slow-cooling and quenching environment. In slow-cooling, furnace temperature was heated from 200 °C to 940 °C at a temperature gradient of 10 °C/min followed by a 5 °C/min gradient from 940 °C to 950 °C before annealing took place. After an hour has elapsed, the temperature was brought back to the initial value of 200 °C at a rate of 5 °C/min

all the way down. In the quenching process, the heating procedure was identical to the one in slow-cooling until annealing took place. After annealing completed, furnace temperature was brought down at a rate of 15 °C/min with the wafers taken out at 850 °C to assist the quenching process.

After annealing took place, the sacrificial oxide grown earlier was removed through wet-etching in buffered 20:1 hydrofluoric acid (HF) until hydrophobic. The chemical reaction involved:

$$SiO_2(s) + 6HF(aq) \rightarrow H_2SiOF_6(aq) + 2H_2O(aq) \tag{2.11}$$

Once oxide was removed, four-point-probe measurement was conducted to find the resistivity of the wafers. The reason for this immediate action was to ensure good electrical contact between the probe and the substrate, right before native oxide started to grow on the silicon. A Jandel RM3-AR four-point-prober was used to measure sheet resistance at the front and the back of each wafer at five different points, covering the whole surface area. The values were then averaged and multiplied by average wafer thickness of 675 μm to find the resistivity of front side and backside of the wafers.

Table 2.2 shows the difference in resistivity enhancement measured for these three different conditions. First of all, it is evident that the resistivity at the front of the wafer reflects the resistivity at the back indicating that the kick-out diffusion mechanism is present. Also can be seen from the table, the highest resistivity enhancement was obtained from the combination of both slow-cooling and quenching annealing conditions. To explain this matter further, this process will be broken down into two individual annealing condition, first being slow-cooling then followed by quenching.

In slow-cooling, interstitial Au atoms start to diffuse after $T = 600$ °C into Si crystals before substituting for Si self-interstitials at temperature above 800 °C. This is when the resistivity starts to change and substitutional Au atoms are compensating for the free carriers and thermal donors to increase bulk resistivity of Si. However, maximum compensation only occurs during the one-hour annealing at 950 °C, the highest temperature reached during the whole procedure. When the cooling process starts, temperature is brought down to initial value of 200 °C at a very slow rate. This causes some of the Au atoms to give up their substitutional positions and de-compensate, reducing the resistivity. Not only that, a generation of thermal donors might also contribute to resistivity reduction when furnace cools down below 500 °C. Having said that, resistivity does not reach its undoped value (shown by resistivity of 1-2 kΩ-cm measured in slow-cooling condition in Table 2.2), indicating that the remaining substitutional Au atoms are still electrically active and able to compensate.

In the quenching process, the substitutional Au atoms do not have enough time to decompensate and so, will remain in their substitutional positions until after the wafers

Annealing Procedure	**Resistivity (kΩ-cm)**	
	FRONT	**BACK**
Slow-cooling	1.54	2.00
Quenching	22.6	21.7
Slow-cooling + Quenching	37.0	32.0

Table 2.2: Four-point-probe resistivity measurement result for wafers underwent slow-cooling, quenching or both before Au layer removal through wet-etching. Measurements were conducted at the front and the back sides of the wafers with pristine resistivity value of 50-60 Ω-cm.

were unloaded at 850 °C. Unloading the wafers at this temperature also prevents the generation of thermal donors, which will provide the wafers with significant increase in resistivity due to full compensation at 950 °C.

In the third condition where both processes were combined, implanted wafers were provided with a so-called 'elevated threshold' before going through second annealing procedure involving quenching. The slightly enhanced resistivity obtained from slow-cooling was brought into quenching environment to serve as threshold resistivity before second annealing took place. As a result, more Au atoms get compensated and give rise to higher resistivity. Based on these observations, it was decided to proceed with combined annealing condition for all further processed wafers.

Subsequent to the removal of the sacrificial oxide and the resistivity measurements, a Au-surface etch was performed to remove any potential conductive layer due to an excess of Au. The surface etch was performed through wet-etching using gold etchant with a mixing ratio of KI : I_2 : H_2O = 4g : 1g : 40g for a duration of 1 minute. The reaction that has taken place was:

$$2Au(s) + I_2(aq) \rightarrow 2AuI(aq) \tag{2.12}$$

Once the residual Au had been removed from the wafers, resistivity of the wafers were measured again at room temperature using the four-point-prober. Table 2.3 shows the numerical resistivity values obtained from four-point-probe measurement. Comparison between resistivity before and after Au-etch in the table shows an increase of almost twice the value measured before Au-etch. The result is consistent with the finding in [69], indicating the presence of Au surface layer that has been removed via wet-etching process. Increase in resistivity indicates reduction in the number of free carrier concentration. Table 2.4 gives evidence on the reduction of background carrier concentration, where the values were calculated using Equation 2.9 as stated in Section 2.2 previously. Since carrier mobility in Au-compensated HR-Si substrate does not vary from the one in uncompensated Si at room temperature [69], μ_e was taken to be 1400 cm^{-2}/V_s [70]. As can

Wafer	Resistivity (kΩ-cm)			
	FRONT		BACK	
	Before	After	Before	After
1	43.2	74.9	37.9	75.6
2	44.8	75.9	39.8	73.9
3	41.6	79.9	33.7	78.8
4	24.0	44.4	22.8	43.7
5	23.3	42.8	22.3	43.0
6	28.7	40.6	30.1	40.3
MEAN	34.3	60.0	31.1	60.0
STANDARD DEVIATION	10.0	18.9	7.43	18.6

Table 2.3: Four-point-probe resistivity values measured at the front and the back sides of Au-compensated HR-Si substrates developed through combined annealing procedures. Results include measurements done before and after Au-etching.

Substrate Type	Etching	ρ (kΩ−cm)	n (cm^{-3})
Au-compensated HR-Si	Au-etched	60.0	6.0 x 10^{10}
Au-compensated HR-Si	–	35.0	2.0 x 10^{11}
Float-Zone	N/A	0.36	1.2x10^{13}

Table 2.4: Calculated free carrier concentrations in Au-compensated HR-Si substrates and Float-zone Si substrates using Equation 2.9.

be seen from the table, majority carrier concentrations are comparatively lower in Au-compensated Si substrates compared to Float-zone Si substrate, where a reduction close to a power of three can be observed in Au-etched, Au-compensated HR-Si substrate. The value approaches the level of intrinsic Si, as mentioned in Section 2.1.

2.6 Summary

Deep-level doping compensation method is used to create high resistivity Si substrates. Au was implanted into 50 Ω-cm Czochralski-Si substrates at the backside of the substrates with a dose of 4 x 10^{13} cm^{-2} at an energy of 100 keV. The implanted substrates were then put under three different annealing procedures with the annealing treatment kept at a temperature of 950 °C for one hour. The highest increase in resistivity is seen for substrates that underwent combined annealing procedure consisting of slow cooling and quenching, indicating the importance of slow-cooling process to act as an 'elevated threshold' for subsequent quenching process in the annealing treatment. Au-etching provides an additional increase in resistivity, due to removal of an inactive Au surface layer on Si surface. The highest recorded resistivity is seen for Au-compensated HR-Si substrates developed through combined annealing procedure with Au-etching effect with a typical value of 60 kΩ-cm and a maximum value of 80 kΩ-cm.

Chapter 3

Design and Fabrication of Microwave Devices

Parasitic surface conduction on Au-compensated Si-based microwave devices were evaluated and quantified using metal-oxide-silicon structures. Three types of devices were designed and fabricated in this work; capacitors, coplanar waveguides and meander inductors with the incorporation of back metallisation of the structure to allow back-biasing of devices during electrical and microwave characterisations. Electrical characterisations on capacitor structure were used to evaluate surface charge effects in Au-compensated HR-Si whereas microwave characterisations on coplanar waveguides and meander inductors were useful for observing the potential suppression of parasitic surface conduction using this type of substrate.

3.1 Capacitor design

Square-shaped capacitors were designed. Eight different sizes of capacitors were included to observe its scaling property with respect to area. Apart from lithography checking, the significance of analysing this property is to enable the extraction of oxide thickness, t_{ox} from oxide capacitance, C_{ox} equation given by:

$$C_{ox} = \frac{\epsilon_o \epsilon_r A}{t_{ox}} \tag{3.1}$$

where ϵ_o and ϵ_r are permittivity of free-space and relative permittivity of SiO_2 respectively, and A is the capacitance area. Table 3.1 summarises the set of capacitors designed in this work and their corresponding patterns are shown in Figure 3.1.

Capacitor pad	Capacitance area, A (mm^2)
1	0.04
2	0.09
3	0.16
4	0.25
5	0.36
6	0.49
7	0.64
8	0.81

Table 3.1: Set of capacitors designed with eight different pad sizes.

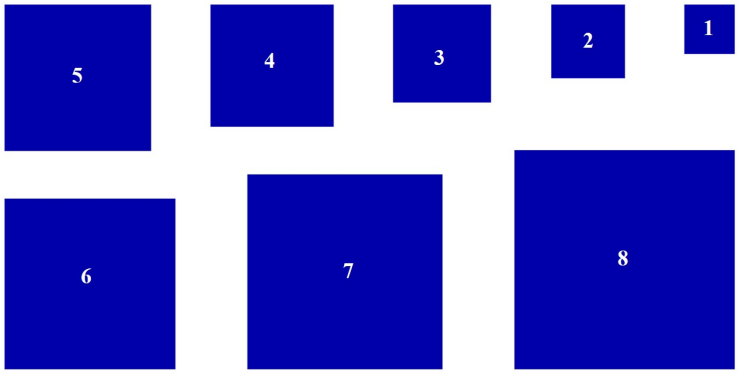


Figure 3.1: Photolithographic mask patterns of square-shaped capacitors.

3.2 Coplanar waveguide design

Back metallisation leads to conductor-backed coplanar waveguides (CBCPWs) design instead of conventional CPWs. Figure 3.2 shows schematic configuration of a CBCPW with central signal strip of width S and two upper grounds, one on each side of the strip with signal-to-ground spacing of W.

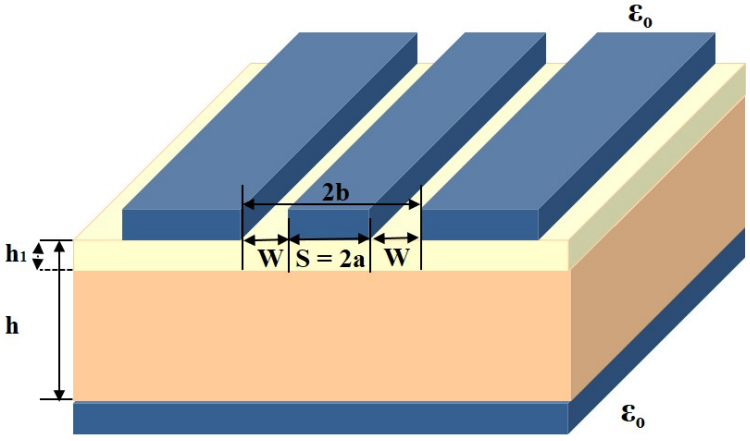


Figure 3.2: Schematic diagram of conductor-backed CPW.

For a CBCPW without top cover, the corresponding propagation mode is shown in Figure 3.3. As can be seen in the figure, some of the wave propagate from signal line to the lower ground plane, a pattern not observed in conventional CPW. In addition to this, the presence of oxide layer might also have an influence on the wave propagation, since the wave needs to travel through two mediums with different dielectric constants.

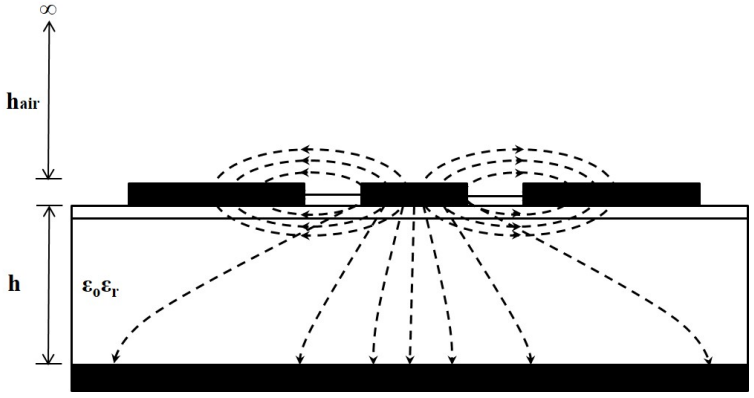


Figure 3.3: Propagation mode of a CBCPW placed on air (without top cover).

Effective dielectric constant, ϵ_{eff} and characteristic impedance, Z_o of the CPW lines are two important parameters that determine the transmission efficiency of the device, where the former is defined by the thickness and dielectric constant of the substrate whilst the latter is defined by the planar dimension of the signal and ground lines.

A 50-Ω Z_o was chosen to match the output impedance and input impedance of the source and the load of the Agilent VNA ports, respectively, for maximum power transmission. To analytically express ϵ_{eff} and Z_o of a conductor-backed CPW on SiO_2 and Si substrates, considerations were first made on conventional open-air CPW structure (without back metallisation) on a double-layer dielectric substrate. Having a much lower dielectric constant compared to Si, the significance of oxide thickness affecting ϵ_{eff} and Z_o was rightfully studied. Two cases were considered; (i) open CPW on SiO_2 and finite Si substrates and (ii) open CPW on infinitely thick Si substrate.

For case (i),

$$\epsilon_{eff} = 1 + \frac{(\epsilon_{Si} - 1)}{2} \frac{K(k_1)}{K(k_1')} \frac{K(k_o')}{K(k_o)} + \frac{\epsilon_{SiO_2} - \epsilon_{Si}}{2} \frac{K(k_2)}{K(k_2')} \frac{K(k_o')}{K(k_o)} \tag{3.2}$$

For case (ii),

$$\epsilon_{eff} = \frac{(\epsilon_{Si} + 1)}{2} + \frac{\epsilon_{SiO_2} - \epsilon_{Si}}{2} \frac{K(k_2)}{K(k_2')} \frac{K(k_o')}{K(k_o)} \tag{3.3}$$

where:

$k_o = a/b$

$k_1 = \frac{sinh(\frac{a\pi}{2h})}{sinh(\frac{b\pi}{2h_1})}$

$k_2 = \frac{sinh(\frac{a\pi}{2h_1})}{sinh(\frac{b\pi}{2h_1})}$

$k_n^{'} = \sqrt{1-k_n^2}$ (n=0,1,2,..)

and K(k) is the complete elliptic integral of the first kind.

For both cases, the expression of Z_o is given by:

$$Z_o = \frac{30\pi}{\sqrt{(\epsilon_{eff}+1)/2}} \frac{K(k_o^{'})}{K(k_o)} \tag{3.4}$$

These expressions were obtained based on the extension of Wen's analysis [71] on conventional CPW and the details can be found in [72–75]. By having ϵ_{Si} and ϵ_{SiO_2} to be 11.9 and 3.9, respectively, h-h_1 = 675 μm, h_1 = 200 nm and width S of central line strip as 50 μm (chosen to reduce difficulty in line-probing for value less than that), the corresponding value of signal-to-ground spacing, W for a 50-Ω CPW line was found iteratively to be 30 μm for both case (i) and case (ii). This indicates that for a 200-nm-thick SiO_2, 675 μm Si substrate can already be considered infinite.

Figure 3.4 shows how ϵ_{eff} (and correspondingly Z_o) of CPW changes with oxide thickness on thick Si substrates. ϵ_{eff} will maintain a constant value of 6.45 for $h_1 < 2$ μm and then starts to decrease until it reaches a constant value of 2.45 for thicker h_1. In addition to this observation, ϵ_{eff} could not be found for $h_1 < 56$ nm due to hyperbolic function limitation in k_1 and k_2 expressions. Hence, it is safe to assume SiO_2 of thickness below 2 μm to be negligible for a 675-μm-thick Si substrate.

Assuming an infinitely thick Si substrate as the dielectric layer, analytical expressions for ϵ_{eff} and Z_o for CPW that consider back metallisation are given as follows [76]:

$$\epsilon_{eff} = \frac{1+\epsilon_{Si}\frac{K(k_0^{'})}{K(k)}\frac{K(k_3)}{K(k_3^{'})}}{1+\frac{K(k_0^{'})}{K(k)}\frac{K(k_3)}{K(k_3^{'})}} \tag{3.5}$$

and

$$Z_o = \frac{60\pi}{\sqrt{\epsilon_{eff}}} \frac{1}{\frac{K(k)}{K(k^{'})}+\frac{K(k_3)}{K(k_3^{'})}} \tag{3.6}$$

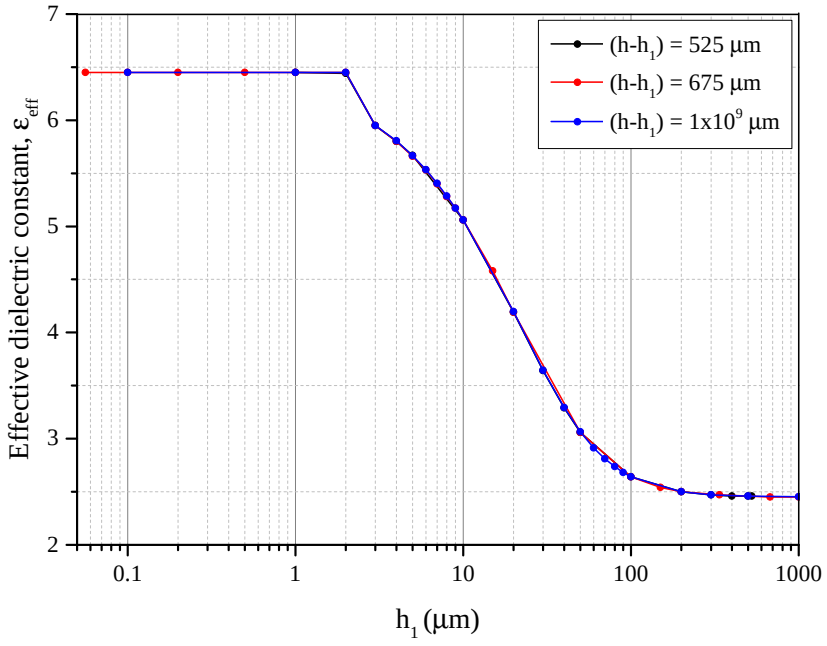


Figure 3.4: Analytical values of effective dieletric constant for conventional open-air CPW (with dimension of $S = 50\mu$m and $W = 30\mu$m) as a function of oxide thickness on different Si substrates.

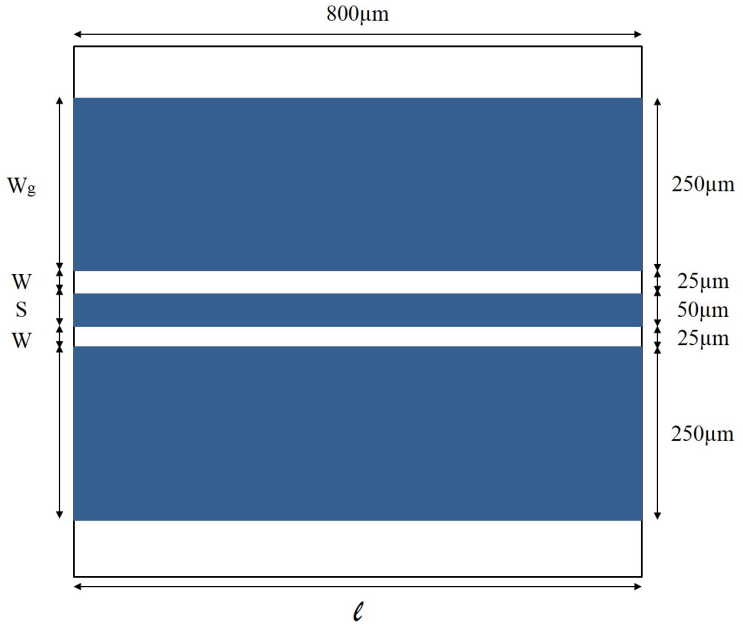
where:

$k_3 = \frac{tanh(\frac{a\pi}{2h})}{tanh(\frac{b\pi}{2h})}$

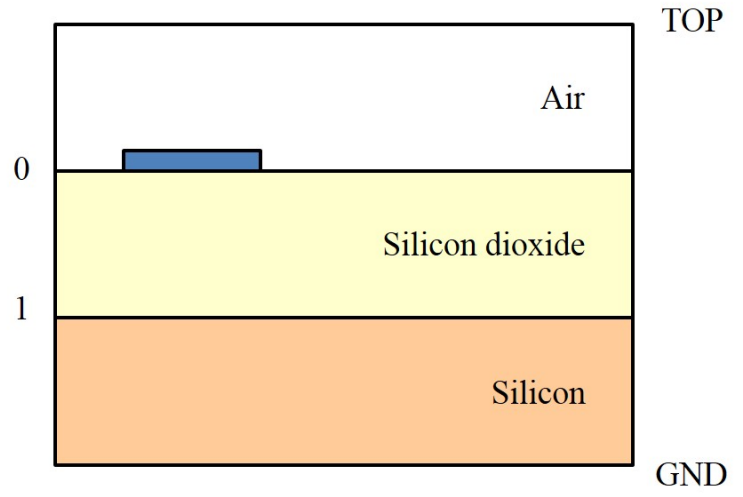
Putting in the values for $\epsilon_{Si} = 11.9$, $h = 675$ μm and $S = 50$ μm ($S = 2a$) into the expressions, W for 50-Ω CBCPW on a 675-μm-thick Si substrate was still found to be 30 μm using an iterative method.

Before this design was realised on the photolithographic mask, simulations were conducted using SONNET's electromagnetic (EM) software to evaluate the chosen dimension. Figure 3.5 shows planar and cross-sectional views of CBCPW constructed in SONNET. Width of upper ground lines, W_g was arbitrarily chosen to be 250 μm, a value large enough to provide sufficient space for probes of different pitch to be used during experimental measurement. Simulation was performed up until 40 GHz with varying W considered.

Figure 3.6 and Figure 3.7 show the return loss and insertion loss obtained from the simulated results. For a 50-Ω line, lowest return loss was observed for $W = 25$ μm, and comparable insertion loss was seen for $W = 30$ μm and $W = 25$ μm. The simulated result was slightly different from the value theoretically calculated previously, where $W = 30$ μm was said to be the optimum value. After careful consideration made, it was decided to use $W = 25$ μm to tolerate possible inconsistency that might occur during



(a) Planar view



(b) Cross-sectional view

Figure 3.5: Structural dimension of CBCPW simulated in SONNET (not to scale).

fabrication process, especially during photolithographic-patterning stage. Also, $W = 25$ μm seems to be a logical intermediate in the range of $20 < W < 30$ μm based on the responses seen in the figures.

Photolithographic mask pattern for the stated dimension of CBCPW was constructed with four different CPW lengths; 800 μm, 1600 μm, 3200 μm and 6400 μm using Tanner EDA's L-Edit software and the designed pattern is shown in Figure 3.8. Variation in lengths was included to observe scaling property of CPW loss with respect to its length.

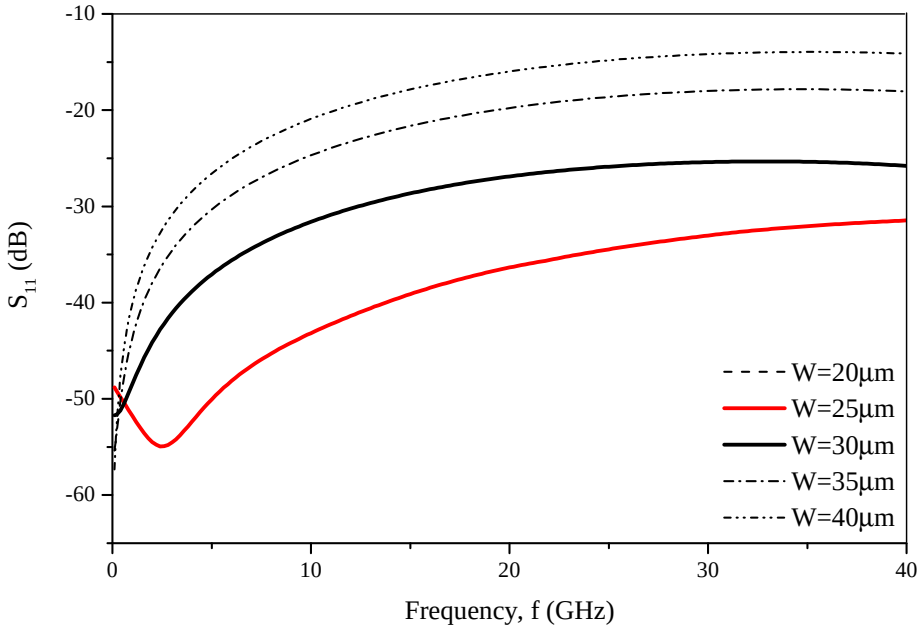


Figure 3.6: Return loss for different W obtained from SONNET for 800-μm conductor-backed CPW with 20 nm SiO_2 on a 675-μm silicon substrate.

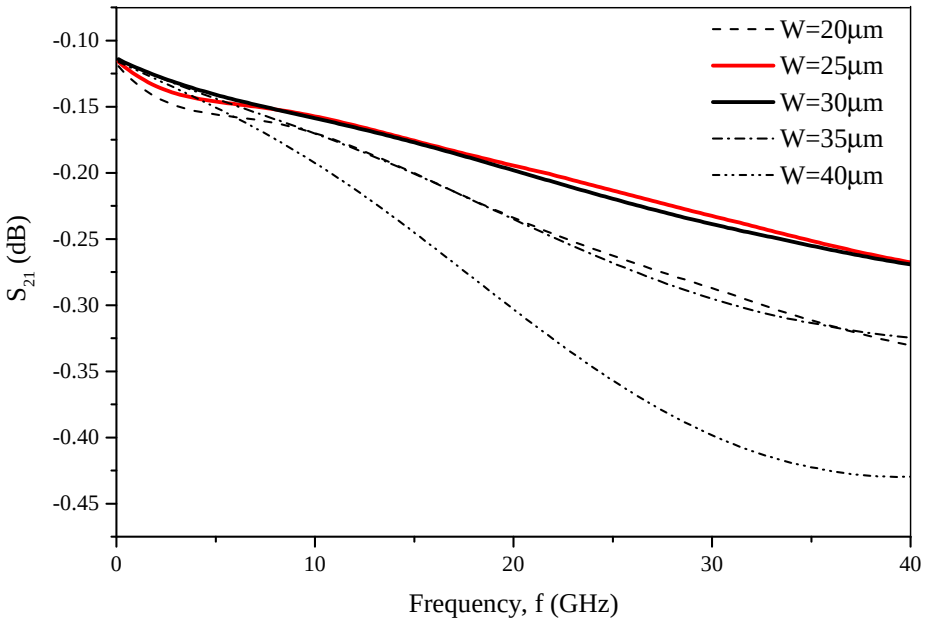


Figure 3.7: Insertion loss for different W obtained from SONNET for 800-μm conductor-backed CPW with 20 nm SiO_2 on a 675-μm silicon substrate.

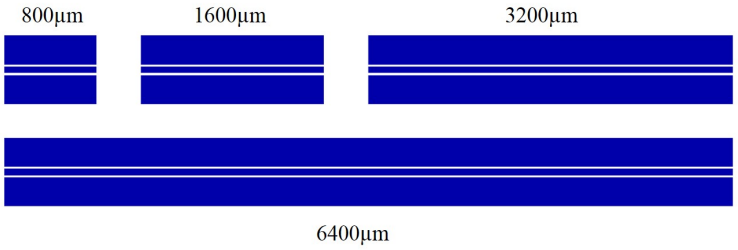


Figure 3.8: Photolithographic mask pattern for CBCPWs

3.3 Meander inductor design

A planar inductor with a meander structure was chosen in this work. Despite weaker quality factor performances obtained in comparison to spiral-shaped inductor, meander structure provides simple planarity with only one metal level of fabrication required. A schematic structure of a meander inductor is illustrated in Figure 3.9. Its inductance value can be determined by a total summation of individual self-inductance, $L_{selftot}$ and mutual inductance between each conductive line and its neighbouring line within the meander structure, M_{tot}:

$$L_{tot} = L_{selftot} + M_{tot} \tag{3.7}$$

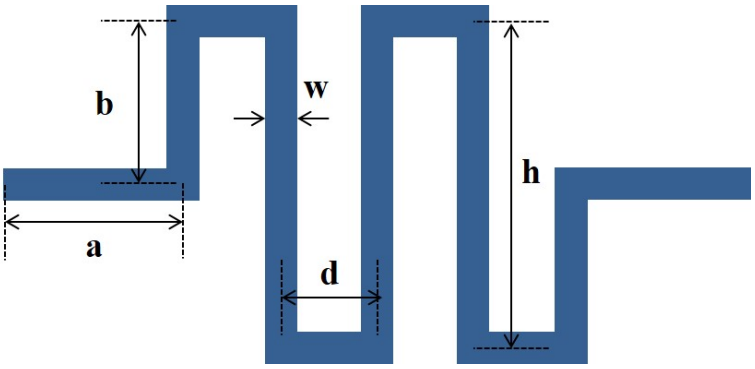


Figure 3.9: Meander inductor structure with its designated dimension

The starting point of examining total inductance value would be the derivation of individual self-inductance, L_{self}. According to Greenhouse *et al.* [77], all inductors can be decomposed into straight conductor lines (as shown in Figure 3.10, having an expression as shown in Equation 3.8:

$$L_{self}(\mu H) = 0.002l[ln(\frac{2l}{GMD}) - 1.25 + \frac{AMD}{l} + (\frac{\mu}{4})T] \tag{3.8}$$

where l is the length of conductive line segment (in cm), GMD and AMD are the geometric and arithmetic mean distance of the line's cross section, μ is magnetic permeability

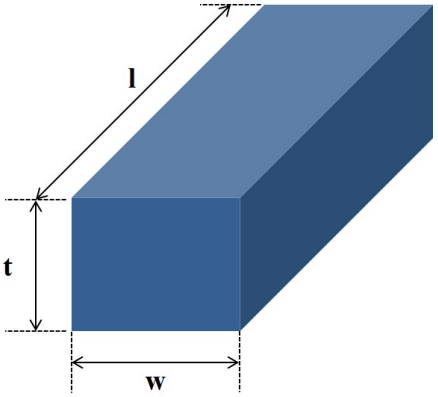


Figure 3.10: Cross-section of a straight conductor line used in self-inductance of a meander inductor design analysis.

of conductor material, and T is the frequency-dependent correction factor. To simplify the expression further, μ and T are taken to be 1, whereas GMD and AMD used were $0.223(w+t)$ [77] and $(w+t)/3$ [78] respectively. Hence, the equation becomes:

$$L_{self}(\mu H) = 0.002l[ln(\frac{2l}{w+t}) + 0.50049 + (\frac{w+t}{3l})] \tag{3.9}$$

To calculate total self-inductance of a meander inductor, L_{self} of all individual segment lines are added up to give:

$$L_{selftot} = 2L_a + 2L_b + NL_h + (N+1)L_d \tag{3.10}$$

where N is the total number of longest segments found in the structure and $L_{a,b,h,d}$ are self-inductance of segments with length a,b,h and d respectively, as shown in Figure 3.11 below.

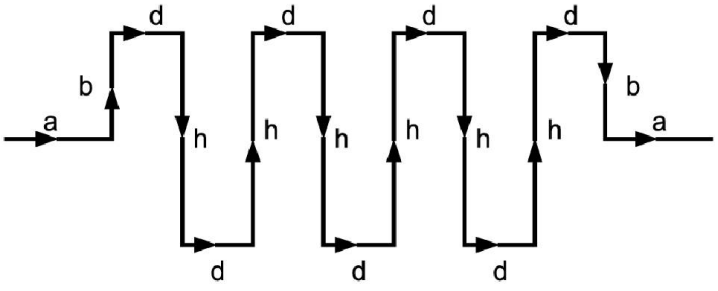


Figure 3.11: Geometrical dimension of a meander inductor.

As for M_{tot}, mutual inductance between two neighbouring line segments needs to be analysed first. For two segments with equal length, l, placed opposite one another and separated by distance r (shown in Figure 3.12), mutual inductance between these two lines is given by [79]:

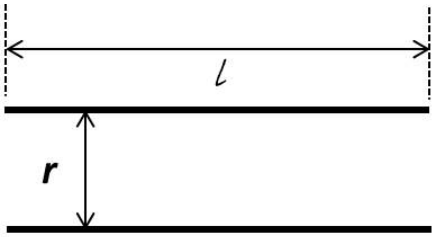


Figure 3.12: Two neighbouring line segments for mutual inductance analysis.

$$M_C(l,r) = \pm\frac{\mu_0}{2\pi} l[ln(\frac{l}{r} + \sqrt{1+(\frac{l}{r})^2}) - \sqrt{1+(\frac{r}{l})^2} + \frac{r}{l}] \tag{3.11}$$

The polarity of M_C depends on the the direction of current flow in both directions [80]; $+M_C$ if same current direction and -M_C if opposite current direction. For line segments with perpendicular current direction, $M_C = 0$. For segments with one line longer than the other, M_C is negative provided the currents are flowing in different directions. Hence, M_{tot} can be obtained by summing up $+M_C$ and -M_C contributed by all segments in the meander structure:

$$M_{tot} = M_C(+ve) + M_C(-ve) \tag{3.12}$$

where the expression has been expanded analytically in [78] to give a more accurate representation of mutual inductance calculation. However, the expansion of Grover's theory for mutual inductance calculation in Stojanovic's work has been found to be a time-consuming analysis with complicated extended expressions. Since the exact inductance value was not considered to be crucial in this scope of work, it was then decided to switch to using simple monomial form of expression which can also be found in his work. Even though it has been said that the least relative error of using this expression will be maximally up to 12%, it was still considered acceptable to be used in this work. The monomial expression of meander inductor's inductance was then given by:

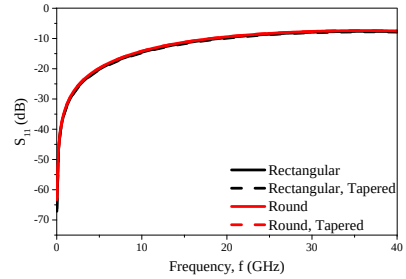
$$L_{mon}(nH) = 0.00266 \cdot a^{0.0603} \cdot h^{0.4429} \cdot N^{0.954} \cdot d^{0.606} \cdot w^{-0.173} \tag{3.13}$$

with all layout dimensions in μm unit. Inductance values calculated using the L_{mon} expression are tabulated for different variable parameter in Table 3.2 which corresponds to different dimension of meander structure. In addition to the values shown, a couple of altered designs have been included as part of the considerations. One is to taper coplanar-to-meander transition lines with a chosen arbitrary angle of 7° whereas another design considers rounded-shape meander turns instead of rectangular turns. Both designs were incorporated to eliminate discontinuity losses at 90° turns. For the altered designs, inductance value for inductor with the same dimension as mentioned in

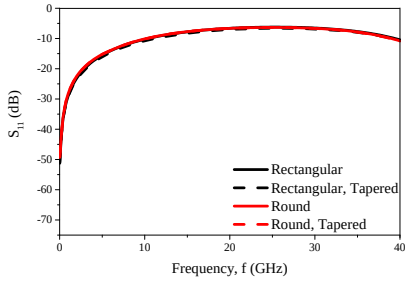
Name	**a (μm)**	**h (μm)**	**N**	**d (μm)**	**w (μm)**	**L (nH)**
M1	140	320	1	80	40	0.70
M2	140	320	2	80	40	1.25
M3	140	320	3	80	40	1.61
M4.5	162	336	8	48	24	2.08
M6	158.5	343	11	34	17	2.44

Table 3.2: Dimensions of different types of meander inductor designed in this work using monomial expression.

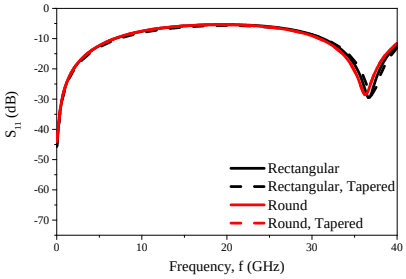
the table was assumed to be identical to ease the design process. Similar to the CPW case, SONNET simulations were performed on all designed structures. Return loss and insertion loss of simulated structures are shown in Figure 3.13 and Figure 3.14.



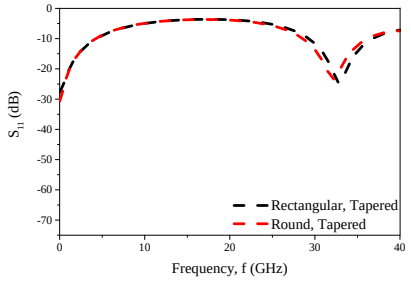
(a) 0.7-nH inductor



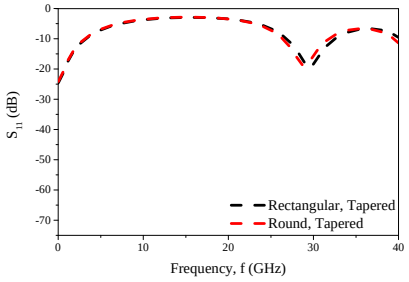
(b) 1.25-nH inductor



(c) 1.61-nH inductor



(d) 2.08-nH inductor

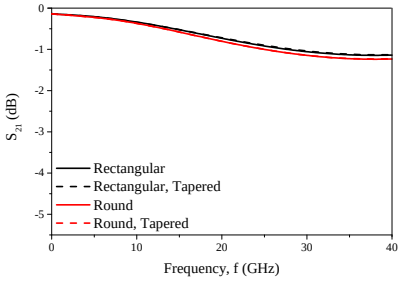


(e) 2.44-nH inductor

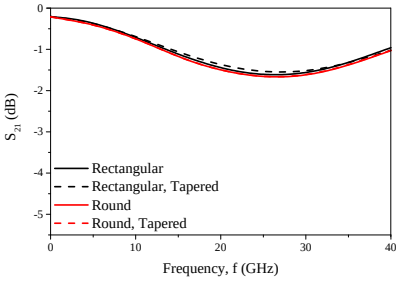
Figure 3.13: Return loss for meander inductors obtained from SONNET simulation.

Return loss characteristics of all structures show very high reflection with nearly -5 dB value seen throughout the whole frequency range, indicating 30% of input power are being reflected by the devices. However, high rejection is seen for structures with values $\geq$ 1.61 nH where a bandwidth of 3 GHz is observed for return loss of -20 dB.

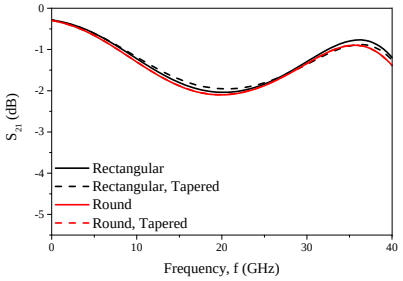
In terms of insertion loss, the structures depict inductor's behaviour where the loss increases with increasing frequency. As frequency goes up, inductive reactance of the structures becomes more significant hence translates into higher insertion loss. Nevertheless, for structures with values $\geq$ 1.61 nH, the loss oscillates at higher frequencies and reaches a certain bandwidth where the values are at the minimum. The frequency range at which this behaviour is observed is the same as the one seen in return loss characteristics shown in Figure 3.13.



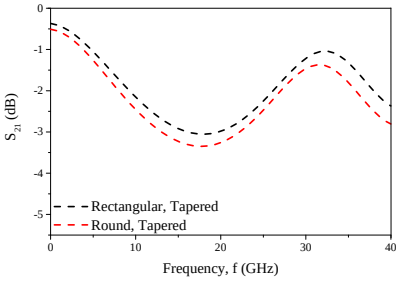
(a) 0.7-nH inductor



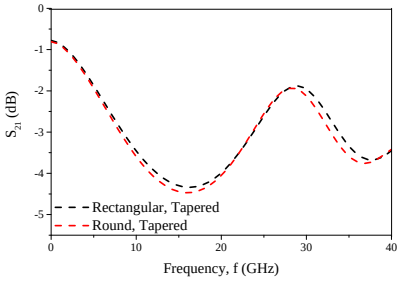
(b) 1.25-nH inductor



(c) 1.61-nH inductor



(d) 2.08-nH inductor



(e) 2.44-nH inductor

Figure 3.14: Insertion loss for meander inductors obtained from SONNET simulation.

The discussed designs were then realised on photolithographic mask and the patterns are as shown in Figure 3.15 to Figure 3.19.

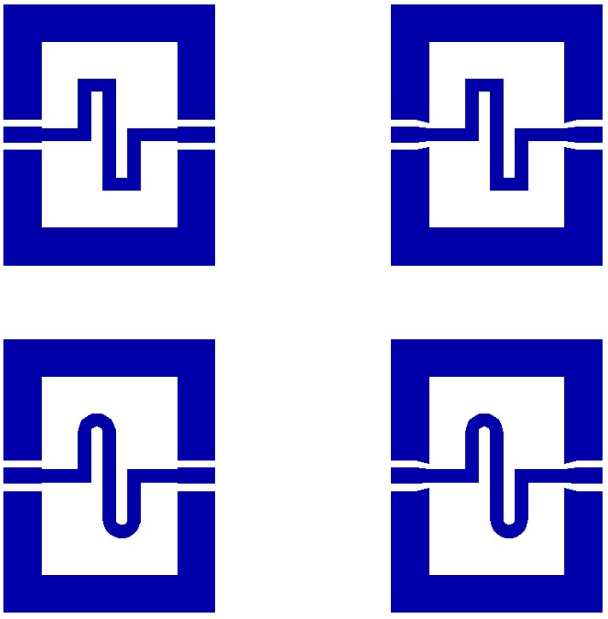


Figure 3.15: 0.7-nH-inductor ($N = 1$) with rectangular (top) and round (bottom) shapes, having a 90° discontinuity (left) or tapered (right) CPW-to-meander line. (From top LHS) M1, M1T, M1S and M1ST.

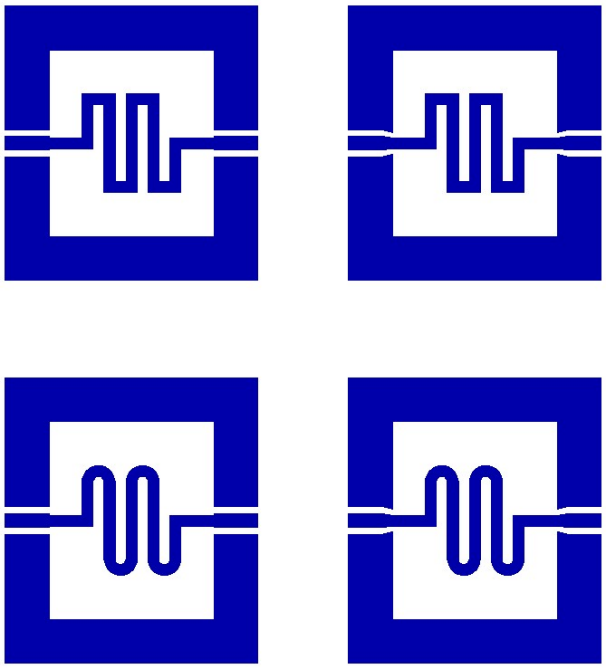


Figure 3.16: 1.25-nH-inductor ($N = 2$) with rectangular (top) and round (bottom) shapes, having a 90° discontinuity (left) or tapered (right) CPW-to-meander line. (From top LHS) M2, M2T, M2S and M2ST.

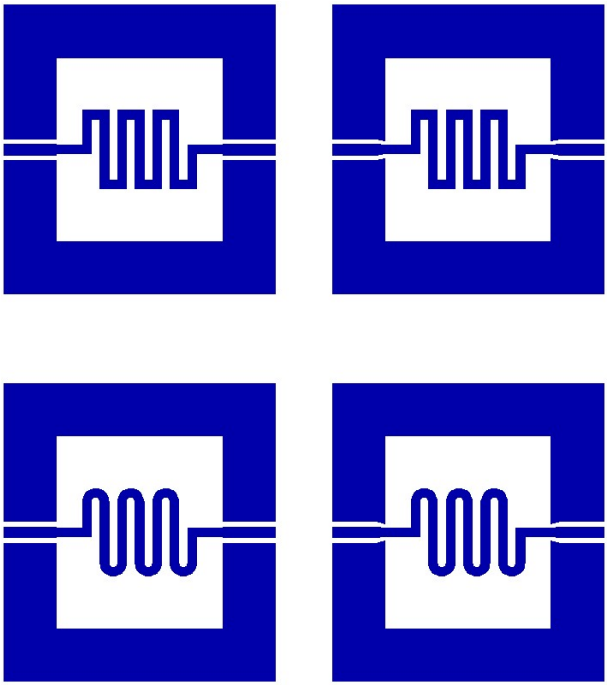


Figure 3.17: 1.61-nH-inductor ($N = 3$) with rectangular (top) and round (bottom) shapes, having a 90° discontinuity (left) or tapered (right) CPW-to-meander line. (From top LHS) M3, M3T, M3S and M3ST.

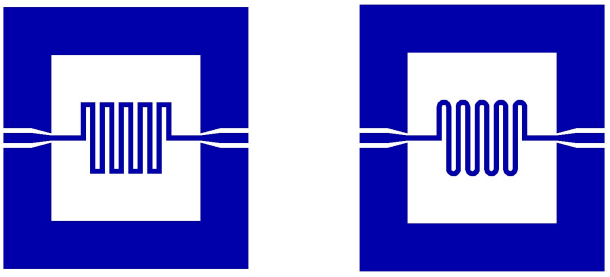


Figure 3.18: 2.08-nH-inductor ($N = 8$) with rectangular (left) and round (right) shapes, having a tapered CPW-to-meander line. (From Left) M4.5T and M4.5ST.

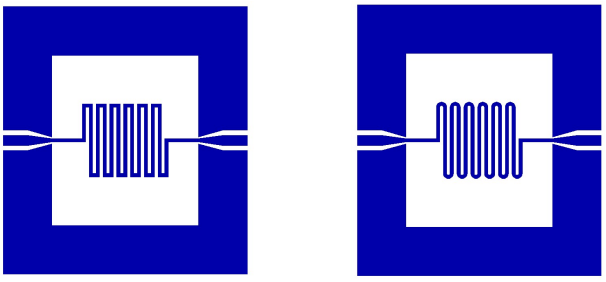


Figure 3.19: 2.44-nH-inductor ($N = 11$) with rectangular (left) and round (right) shapes, having a tapered CPW-to-meander line. (From Left) M6T and M6ST.

3.4 Fabrication of devices on Au-compensated HR-Si substrates

The design of capacitors, coplanar waveguides and meander inductors as discussed in the previous sections were put into realisation by fabricating them onto Au-compensated HR-Si substrates. The basic cross-sectional metal-oxide-silicon structure of devices on Au-compensated HR-Si substrates is as shown in Figure 3.20.

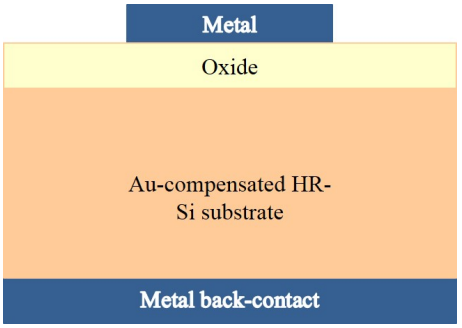


Figure 3.20: Cross-sectional structure of a metal-oxide-semiconductor devices on Au-compensated HR-Si substrates.

Before fabrication took place, a number of considerations have been made in order the achieve the main objectives of studying PSC effect and observing potential PSC suppression using Au-compensated HR-Si substrates. The variables considered in this work are summarised in Figure 3.21 where the rationale of each variable is explained as follows:

1. The inclusion or the exclusion of Au-etching in the fabrication process to see whether Au-surface layer formed by inactive gold atoms after annealing at high temperature will be able to contribute to the trapping layer at the interface [69].
2. Presence of oxide to study the potential formation of surface charges at the oxide-semiconductor interface that causes PSC.
3. Types of oxide grown or deposited to determine whether the quality of oxide used in the structure is directly related to the density of surface charges formed at the interface.
4. Oxide layer thickness to observe the optimum value of passivation needed by Au-compensated HR-Si.

A set of Au-compensated HR-Si substrates were used as the base substrates for microwave devices, each of which has been allocated different fabrication details to reflect the mentioned variables. The details are summarised in Table 3.3 and the overall process flow of fabrication process is illustrated in Figure 3.22.

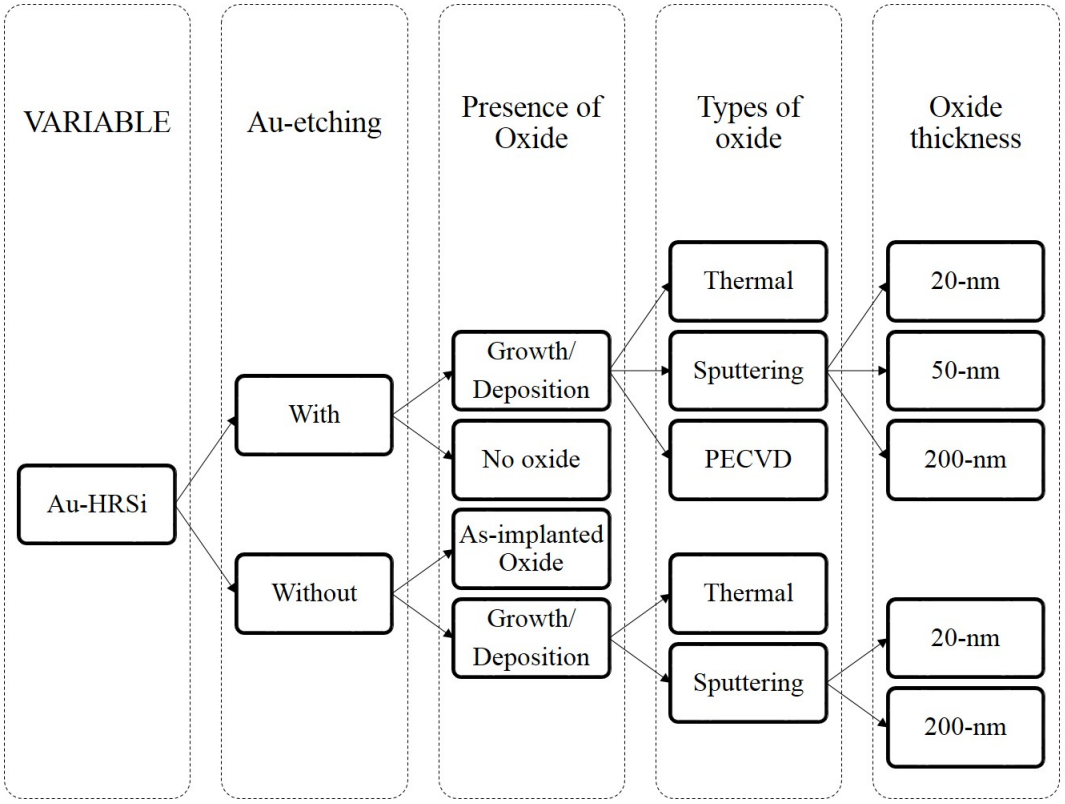


Figure 3.21: Variables considered in fabrication of microwave devices on Au-compensated HR-Si substrates.

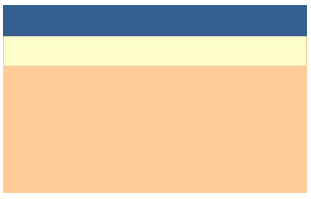
Wafer	Au-etching	Oxide Deposition/Growth	Oxide thickness
1	Au-etched	No Oxide	-
2	Au-etched	Thermal	20nm
3	Au-etched	Sputtered	20nm
4	Au-etched	Sputtered	50nm
5	Au-etched	Sputtered	200nm
6	Au-etched	PECVD	50nm
7	Not etched	Thermal	20nm
8	Not etched	Sputtered	20nm
9	Not etched	Sputtered	200nm
10	Not etched	Sacrificial	20nm

Table 3.3: Wafer splits for fabrication of passive components on Au-implanted high resistivity silicon.

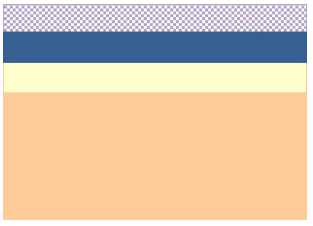
The first step in the fabrication process involved the growth/deposition of insulating SiO_2 layer on top of the silicon wafer. There were three types of oxidation process considered in this fabrication; thermal oxidation, sputtering and plasma-enhanced chemical vapour deposition (PECVD). The first oxidation process involves the growth of silicon dioxide through high temperature environment in a furnace, where the operating temperature ranges between 800-1200 °C. Thermal oxidation consists of two types, wet oxidation and dry oxidation, where the latter has slower oxidation rate with better oxide quality.

(a) Au-Si substrate with thickness 675μm

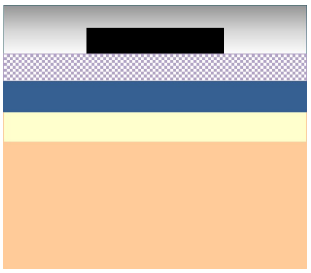
(b) Silicon Dioxide Growth/Deposition



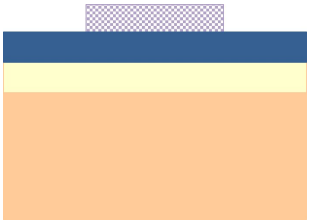
(c) Aluminium Front Contact Deposition by Evaporation



(d) Photoresist-coating followed by Soft-baking at 95^0C

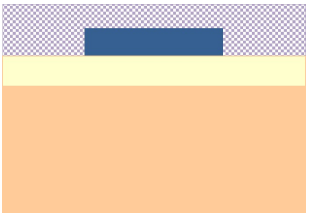


(e) Mask-aligning using EVG6200

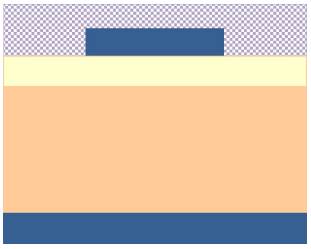


(f) UV-exposure followed by Photoresist Development

(g) Aluminium-etching



(h) Front Spin Resist followed by Soft-baking at 95^0C



(i) Aluminium Back Contact Deposition by Evaporation

(j) Front Resist Stripping

Figure 3.22: Summary of fabrication steps of metal-oxide-semiconductor on Au-compensated HR-Si substrates

Oxidation process	**Thermal**	**Reactive sputtering**	**PECVD**
Advantage	Highest-quality oxide	High uniformity, fast, good adhesion	Low temperature
Disadvantage	High temperature, high equipment maintenance	Ionic bombardment damage, high equipment and source maintenance	Chemical and particulate contamination, low density

Table 3.4: Comparison between thermal oxidation, reactive sputtering and PECVD for silicon dioxide deposition.

As for sputtering process, it is a form of physical vapour deposition, where the basic principle of operation is to excite solid target material through a flux of ejected target atoms on a heated substrate, forming a thin film layer on top of the substrate. In this fabrication, a reactive sputtering process was employed through Plasma-Assisted Magnetron Sputtering (PARMS) technology, that is based on repeated two-step process. The first process is reactive deposition of a thin silicon layer with controlled oxygen atmosphere followed by RF plasma assist process with reactive oxygen. The process continues until the required layer is achieved i.e. through time-control or an optical monitoring system. Meanwhile, PECVD is a low-temperature, chemical vapour deposition process where source gas is decomposited by plasma on the substrate. Typical operating temperature is very much lower than thermal oxidation (300-400 °C) however, the deposited oxide quality is doubtful due to chemical and particulate contamination, as well as density issues. Comparison between these three types of oxidation is shown in Table 3.4.

Silicon oxide was grown thermally on two wafers via dry oxidation process in a Tempress furnace at a temperature of 1000 °C for 9 minutes to achieve a nominal oxide thickness of 20 nm. Growth rate was taken to be 2.2 nm/min, determined by thermal oxidation of a bare silicon wafer which was conducted right before the actual oxidation took place to ensure optimum rate was used at a given temperature and gas environment in the furnace. The chemical reaction for a dry oxidation is:

$$Si(s) + O_2(g) \rightarrow SiO_2(s) \tag{3.14}$$

A nominal oxide thickness of 50 nm was deposited on one wafer using an OIPT System 100 PECVD machine for 49 seconds. In this process, a combination of silane and nitrous oxide have been used as the source gases to deposit silicon dioxide at a pressure of 1000 mT and RF power of 20 W. Similar to thermal oxidation, deposition rate was first determined by depositing silicon dioxide on a bare silicon wafer, giving a value of 1.03 nm/s.

Five wafers have undergone oxide-sputtering process using the Leybold Helios reactive sputterer. Time was varied to achieve different SiO_2 thicknesses, based on a deposition rate of 0.55 nm/s specified by the deposition recipe. In addition, one wafer was further processed without any SiO_2 layer and one was left with the sacrificial oxide deposited during the implantation process in the development of Au-compensated HR-Si substrates as described in Section 2.5 of Chapter 2.

Following the oxide deposition, the thickness of the deposited film was measured using an ellipsometer. This technique consists of a rotating analyzer ellipsometer(RAE) configuration that is used to measure the change in light polarisation when light passes through the sample surface (in this case, silicon dioxide layer) and gets reflected [81]. Once the sample is measured, a sample model will be generated and fitted to the experimental data, allowing the unknown parameter of oxide thickness to vary until the best match between these data is achieved.

A full 6-inch scan was conducted on all oxide-deposited and oxide-grown wafers. The angle of travelling and reflected light was set to be 65° and mean squared values (MSEs) for all wafers are below 10. The model used to fit the 20-nm-thick and 50-nm-thick was 'Silicon with Thermal Oxide' model whereas the one used to fit 200-nm-thick oxide was 'Silicon with Transparent Film'. Both models were the basic models embedded in CompleteEASE software, a software integrated with the Woollam M-2000 spectroscopic ellipsometer which was used in this measurement. Figure 3.23 illustrates the example of thickness patterns obtained from the three aforementioned types of oxide deposition. Comparing the pattern, the thermal oxide has the highest thickness towards the top edge of the substrate whereas the highest thickness for sputtered and PECVD oxide can be seen at the center of the substrate. These trends are reasonable, considering the angle of substrate inside the chamber for growth or deposition of oxide. During thermal oxidation, substrates were placed vertically in a wafer 'boat' with dummy wafers and since flow of oxygen came mostly from above inside the furnace, greater oxygen exposure were received by the edges of the substrates in comparison to the center, resulting in decreasing concentration of oxide growth from the edges towards the center. Meanwhile, for deposited oxide, ionic bombardment (for sputtering) and decomposition of precursors (for PECVD) occurred directly on top of substrate's surfaces (due to the horizontally-placed positions inside the chamber), causing the center of the substrate to receive slightly higher deposition compared to the edges.

Table 3.5 compares the nominal with the estimated values obtained from ellipsometry measurement. With reference to the table, the estimated oxide thickness obtained from sputtered oxide wafers differ significantly, especially for 200-nm-thick oxide with a reduction of 15 percent from the required thickness. The discrepancy can be explained by incorrect deposition rate used to determine deposition time required for a certain oxide thickness value. The actual deposition rate for silicon dioxide in Helios sputterer was hence 0.46 nm/s, instead of the stated 0.55 nm/s. A similar approach as the one used

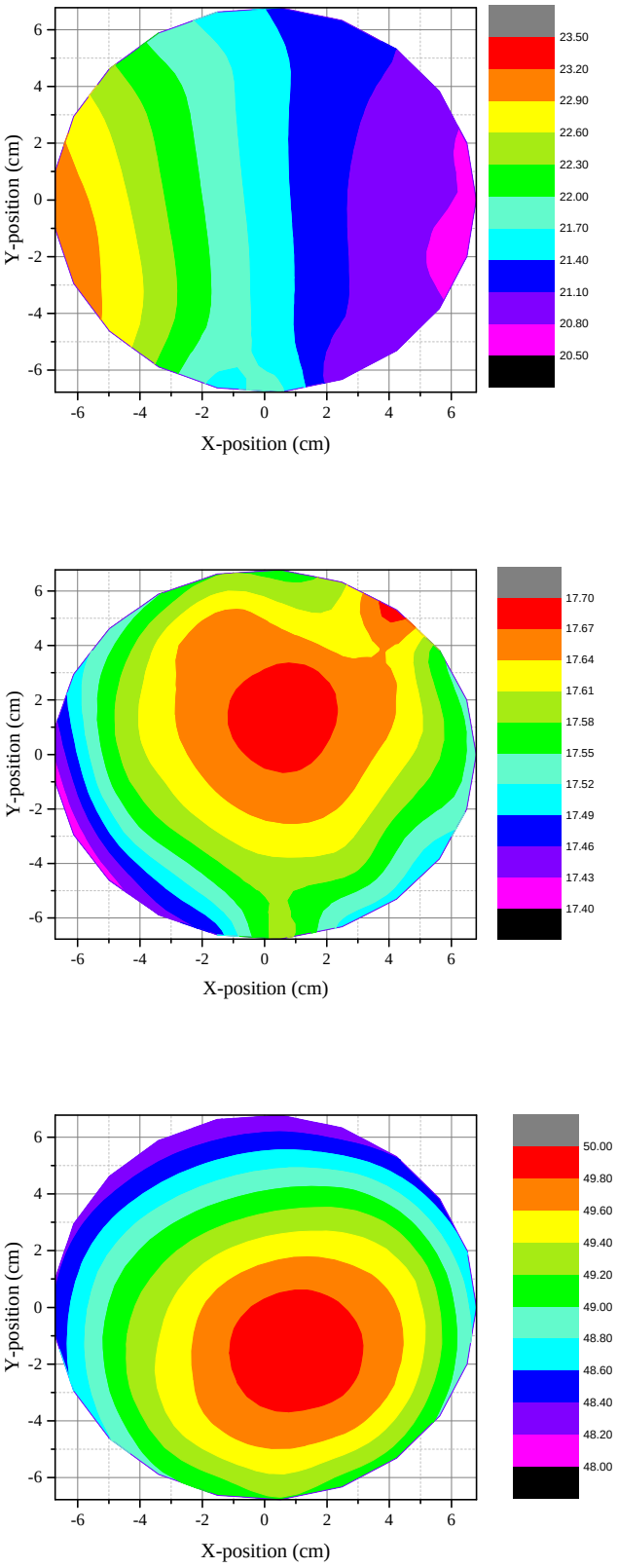


Figure 3.23: Oxide thickness pattern measured from ellipsometry. (*Top*) Thermal oxide with nominal t_{ox} of 20 nm. (*Middle*) Sputtered oxide with nominal t_{ox} of 20 nm. (*Bottom*) PECVD oxide with nominal t_{ox} of 50 nm.

WAFER	**PROCESS**	**THICKNESS (nm)**	
		Nominal	Ellipsometry
2	Thermal	20	20
3	Sputtered	20	18
4	PECVD	50	38
5	Sputtered	200	172
6	Sputtered	50	49
7	Thermal	20	20
8	Sputtered	20	18
9	Sputtered	200	172

Table 3.5: Comparison between nominal and estimated oxide thickness measured by ellipsometer.

for oxide growth rate and PECVD-deposition rate (i.e. using a bare silicon wafer to determine actual deposition rate) should have been taken for the case of oxide-sputtering before actual deposition process was done. However, since the thickness variable can easily be compensated for in further analysis, it was decided to keep the sputtered-oxide thickness values as they were.

After measuring the oxide layer thickness, front contact deposition took place by evaporating 1 μm of aluminium, Al on top of the silicon dioxide using a Leybold LAB700 at a deposition rate of 0.5 nm/s. Next fabrication stage involved photolithographic patterning of the metal-oxide-semiconductor structures, where the photolithographic mask used to fabricate these devices was designed using two-dimensional Tanner EDA's L-Edit IC design software. Figure 3.24 shows a single chip design consisting of four sets of capacitors, two sets of coplanar waveguides and five sets of meander inductors with different inductance values.

The front side of the wafers were coated with positive resist (S1813) using a spin-coater integrated in the EVG150 robotic resist processing station, before they were exposed through EVG6200 Infinity robotic mask-aligner for 3.5 seconds through mask-aligning procedure. The exposed resist was then developed in MF-319 developer for 35 seconds to wash away the 'unwanted' pattern, leaving only the pattern covered by the mask. Aluminium-etching took place after that by emerging the patterned wafers into aluminium etchant solution (orthophosphoric acid) at 40^0C for 4 minutes to ensure all aluminium was removed. The etch rate was determined to be 355 nm per minute.

The wafers were then front spin resist-coated to protect front contact from damage before deposition of a 500-nm-thick aluminium at the back of the wafers (as the back contact) using the Leybold Helios reactive sputterer took place for 2137 seconds as the deposition rate was observed to be 0.234 nm/s. To remove the native oxide at the back of the wafer, the wafers were wet-etched in buffered 20:1 hydrofluoric acid (HF) for 30 seconds, or until hydrophobic, beforehand. The last stage involved in this process was

to strip off the resist protecting the front contact and this has been done by dipping it into fuming nitric acid (FNA) solution for 1 minute.

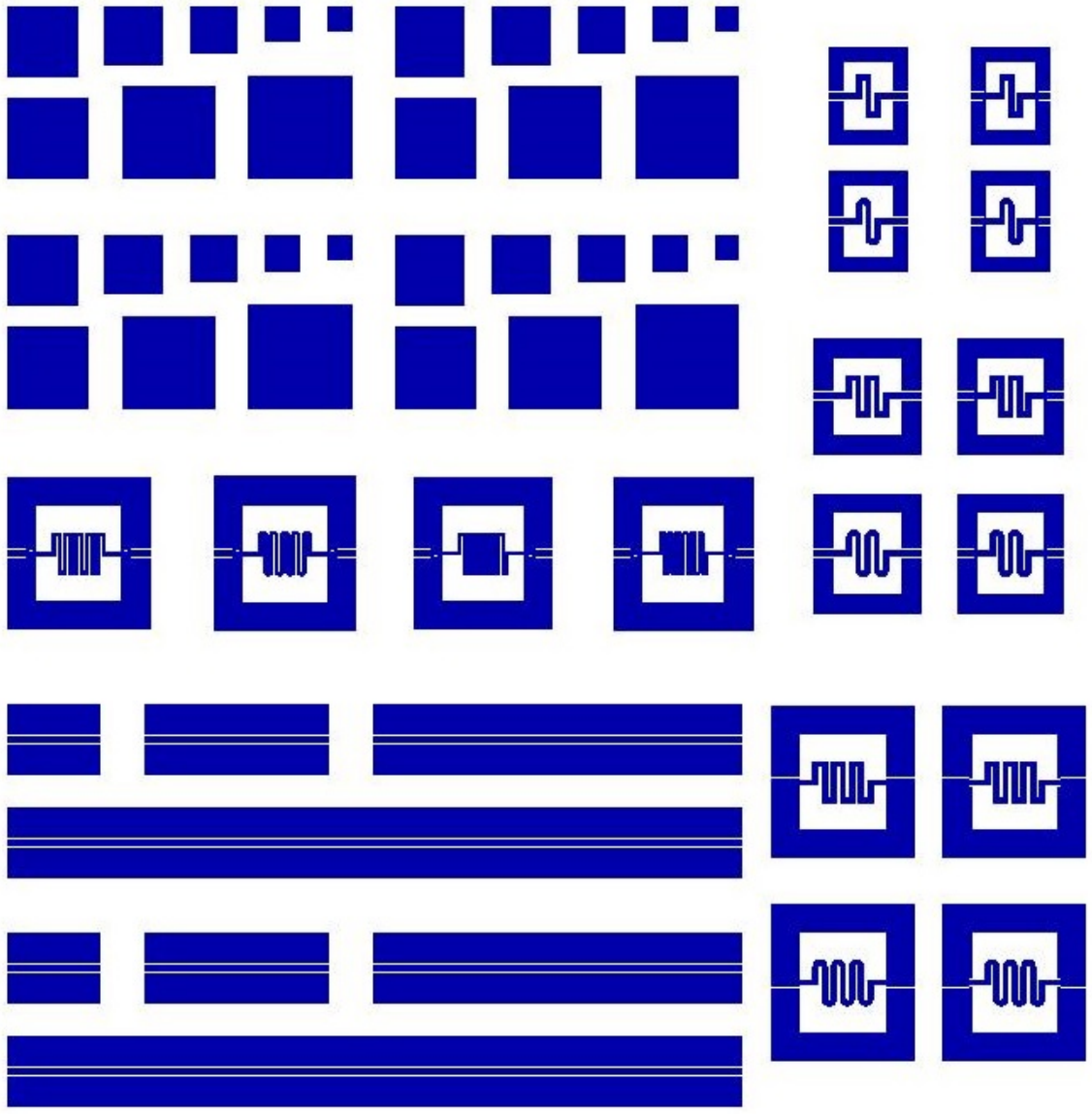


Figure 3.24: Photolithographic mask layout for a single chip design consists of squared capacitors, coplanar waveguides and meander inductors

Figure 3.25 shows scanning electron microscope (SEM) images of deposited Al metal contact and SiO_2 where the measured thicknesses are in good agreement with nominal values of 1 μm and 20 nm respectively.

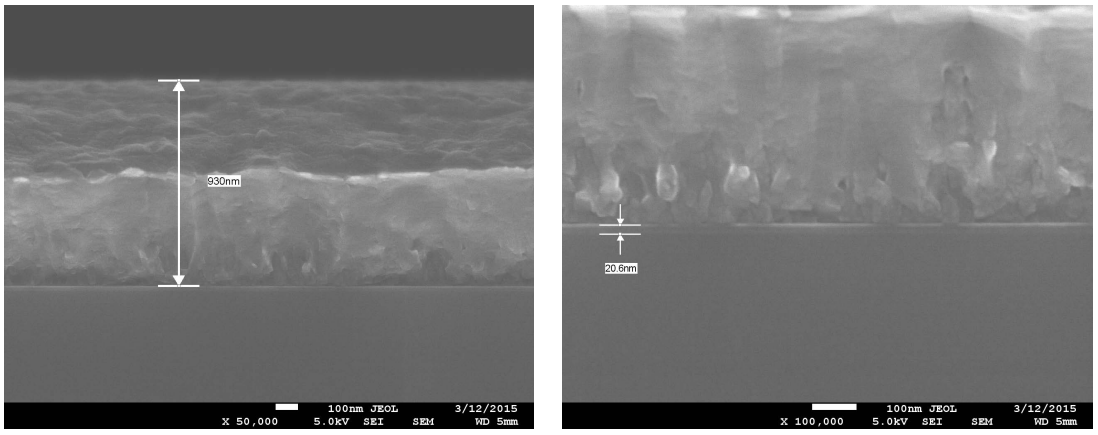


Figure 3.25: SEM images of (*Top*) deposited front contact Aluminium with nominal thickness of 1 μm and (*Bottom*) SiO_2 with nominal thickness of 20 nm.

Another set of SEM images were illustrated in Figure 3.26 for CPWs fabricated in this work with signal line S and signal-to-ground spacing W observed to be within 10% tolerance level.

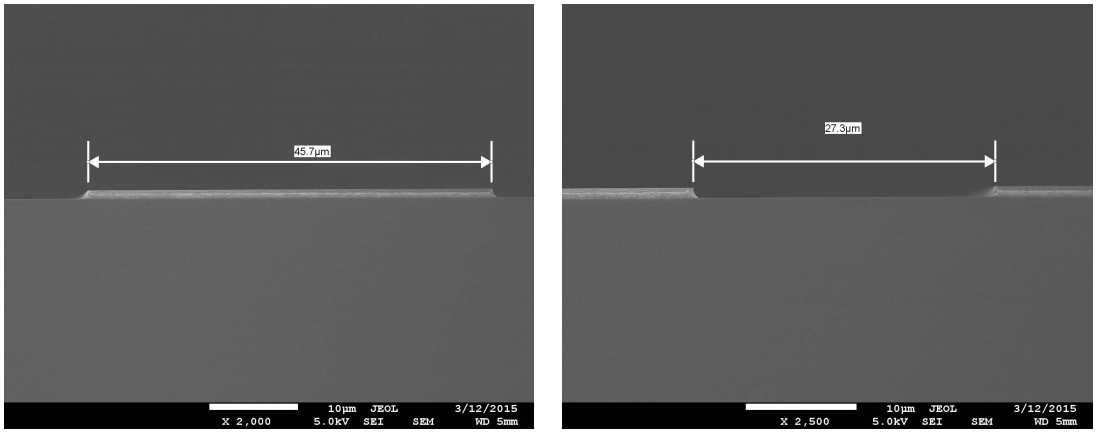


Figure 3.26: SEM images of (*Top*) signal line S and (*Bottom*) signal-to-ground spacing W of CPWs fabricated in this work.

Microscopic images of fabricated devices are shown in Figure 3.27, Figure 3.28 and Figure 3.29. Images on the left were taken after photolithographic patterning process whereas images on the right represent the actual structures after all fabrication processes were completed.

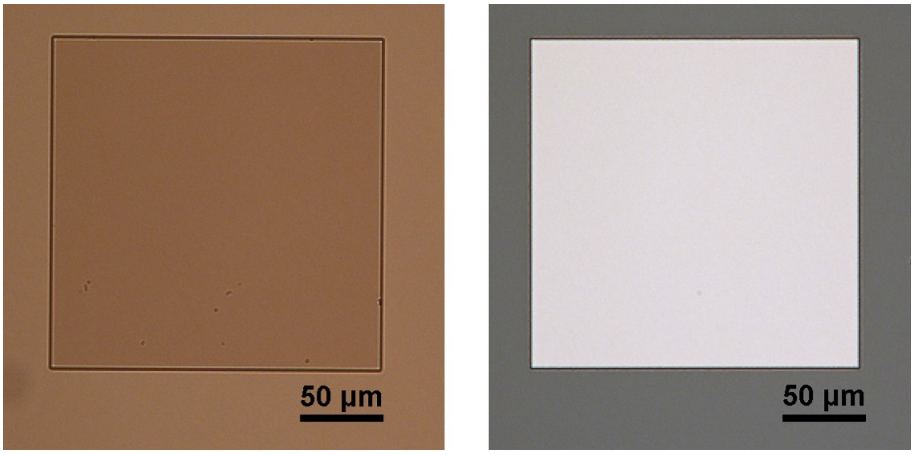


Figure 3.27: Microscopic image of a 0.04-mm^2 capacitor. (Left) Before Al-etching (Right) After Al-etching.

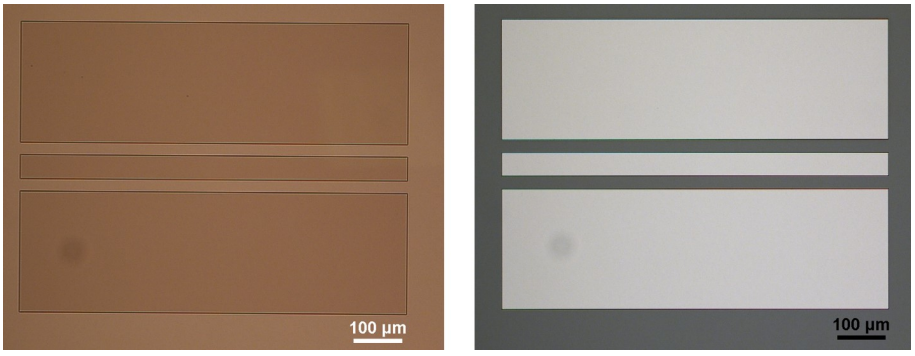


Figure 3.28: Microscopic image of an 800-μm coplanar waveguide. (Left) Before Al-etching (Right) After Al-etching.

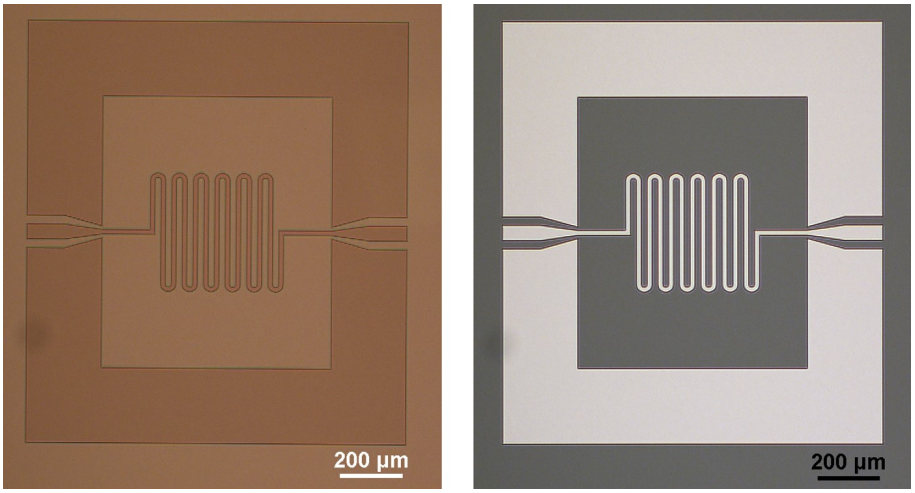


Figure 3.29: Microscopic image of a 2.44-nH meander inductor. (Left) Before Al-etching (Right) After Al-etching.

3.5 Summary

Planar capacitors, coplanar waveguides and meander inductors were designed. Backside metallisation was considered in the design where the designed structures were optimised to provide a sufficient platform for the study of PSC suppression on Au-compensated HR-Si substrates. All design were realised onto photolithographic mask before fabrication of devices took place.

Chapter 4

Evaluation of Surface Charge Layers in MOS Capacitors on High Resistivity Silicon

The effect of surface charge layers in bulk HR-Si substrate will be studied in this chapter where the passivated oxide layer deposited on top of Si substrate will induce charges inside Si structure to move near oxide-silicon interface to form a layer of low resistivity region under the influence of electric field. Formation of accumulation or inversion regions at silicon surface defy the functionality of its highly-resistive bulk nature to reduce substrate losses at microwave frequency.

Metal-oxide-silicon structure analysis are used to observe the behaviour of field-dependent charge at the oxide-silicon interface which contribute to parasitic surface conduction phenomenon in microwave devices. Its capacitance-voltage characteristic reveals the amount of carrier charges as well as the movement of majority and minority carriers in relation to the nature of the applied bias, hence, giving good estimates of their presence at the Si-SiO_2 interface.

4.1 Surface Conduction Effect Associated with Thermally Oxidised Silicon

The basic structure of a MOS capacitor consists of an insulating oxide layer, sandwiched between a metal contact and a semiconductor substrate. In order to have an Ohmic contact at the back of the semiconductor, a second metal layer can be formed as the back contact. This capacitor will be connected to a voltage source to form an electrical connection and to provide the means for electrical characterisation of the structure.

Figure 4.1 shows the structure of a pMOS capacitor that will be discussed in this section, where the semiconductor substrate is an n-type doped substrate with a silicon dioxide, SiO_2 insulating layer and an Aluminium metal contact. Since it is a pMOS capacitor, holes are the minority carriers that contribute to the inversion layer of this structure. Voltage, V is applied to the capacitor through the Al contact and d is the thickness of the oxide layer, which will be considered as the separation distance between Al metal and n-type substrate.

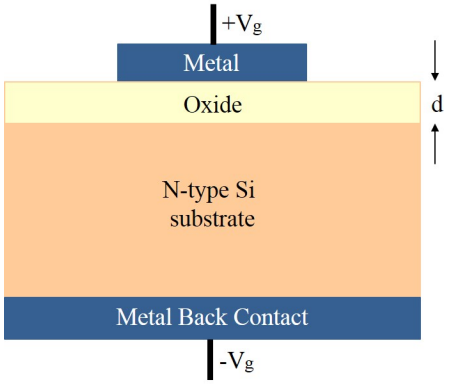


Figure 4.1: MOS Capacitor

There are three basis of operation involved with regards to a simple MOS structure named accumulation, depletion and inversion. Before going into further details about these bias-dependent operations, it is equally important to firstly define ideal MOS conditions when no electric field is applied, i.e. at $V = 0$. Figure 4.2 shows the energy-band diagram of an ideal pMOS at zero bias condition, where it can be seen that the energy band is flat (flatband condition), indicating no energy difference between metal work function, Φ_m and semiconductor work function, Φ_s that can be defined as:

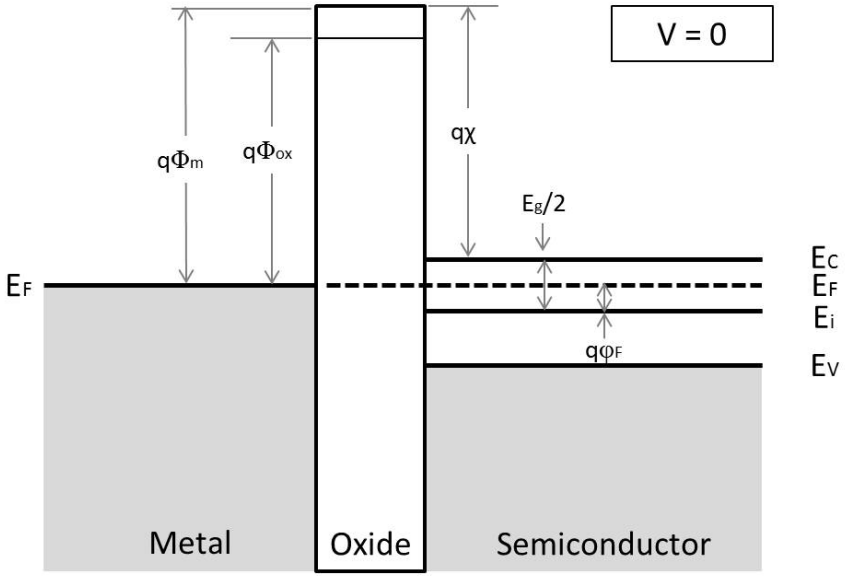


Figure 4.2: Energy-band diagram of a pMOS structure at zero bias condition

$$\Phi_S = \chi + \frac{E_g}{2q} - \phi_F \tag{4.1}$$

where χ is the electron affinity, E_g is the intrinsic band gap energy, q is the eletronic charge and ϕ_F is the bulk Fermi potential, given by:

$$|\phi_F| = \frac{kT}{q} \ln \frac{N_d}{N_i} \tag{4.2}$$

Another condition of an ideal MOS includes a perfectly insulating oxide layer that provides carrier transport barrier at any biasing condition due to it being infinitely resistive, separating the charges in the semiconductor and the equal-but-opposite-sign charges on the metal surface. These are the only charges that can exist in the structure as far as the ideal condition is concerned.

Figure 4.3 illustrates the energy band diagrams for an ideal MOS under bias condition. When a positive bias voltage is applied to the metal contact on a pMOS structure ($V > 0$), the top of conduction band, E_C bends towards Fermi level, attracting majority carriers (electrons) to the oxide semiconductor surface, forming an accumulated layer of carriers. This structure is now in the *accumulation* mode. When a negative bias is applied ($V < 0$), the bands bend upward (where the top of conduction band bends away from Fermi level), causing the electrons to be depleted from the surface and leaving behind ionised positive donors, N_d in the depleted region. This is called *depletion* mode. When a strong negative bias is applied, the bands bend further upward until the intrinsic level, E_i below Fermi level crosses over, causing minority carriers (holes) inside the semiconductor substrate to form an inversion layer at the surface to maintain charge neutrality equilibrium that the ionised donors were not longer able to maintain. This is the *inversion* mode, and the surface is said to be 'inverted'.

As mentioned previously, flatband occurs ideally at zero bias when the device is in thermal equilibrium. However, Φ_m and Φ_s are generally not equal, hence, a certain level of bias has to be applied to obtain the flatband condition. The corresponding voltage is termed as *flatband voltage*, and is defined as the difference between Φ_m and Φ_s.

$$V_{FB} = \Phi_M - \Phi_S \tag{4.3}$$

By taking into account Equation 4.1 and Equation 4.2, the full expression for flatband voltage becomes:

$$V_{FB} = \Phi_M - (\chi + \frac{E_g}{2_q} - \frac{kT}{q} \ln \frac{N_d}{N_i}) \tag{4.4}$$

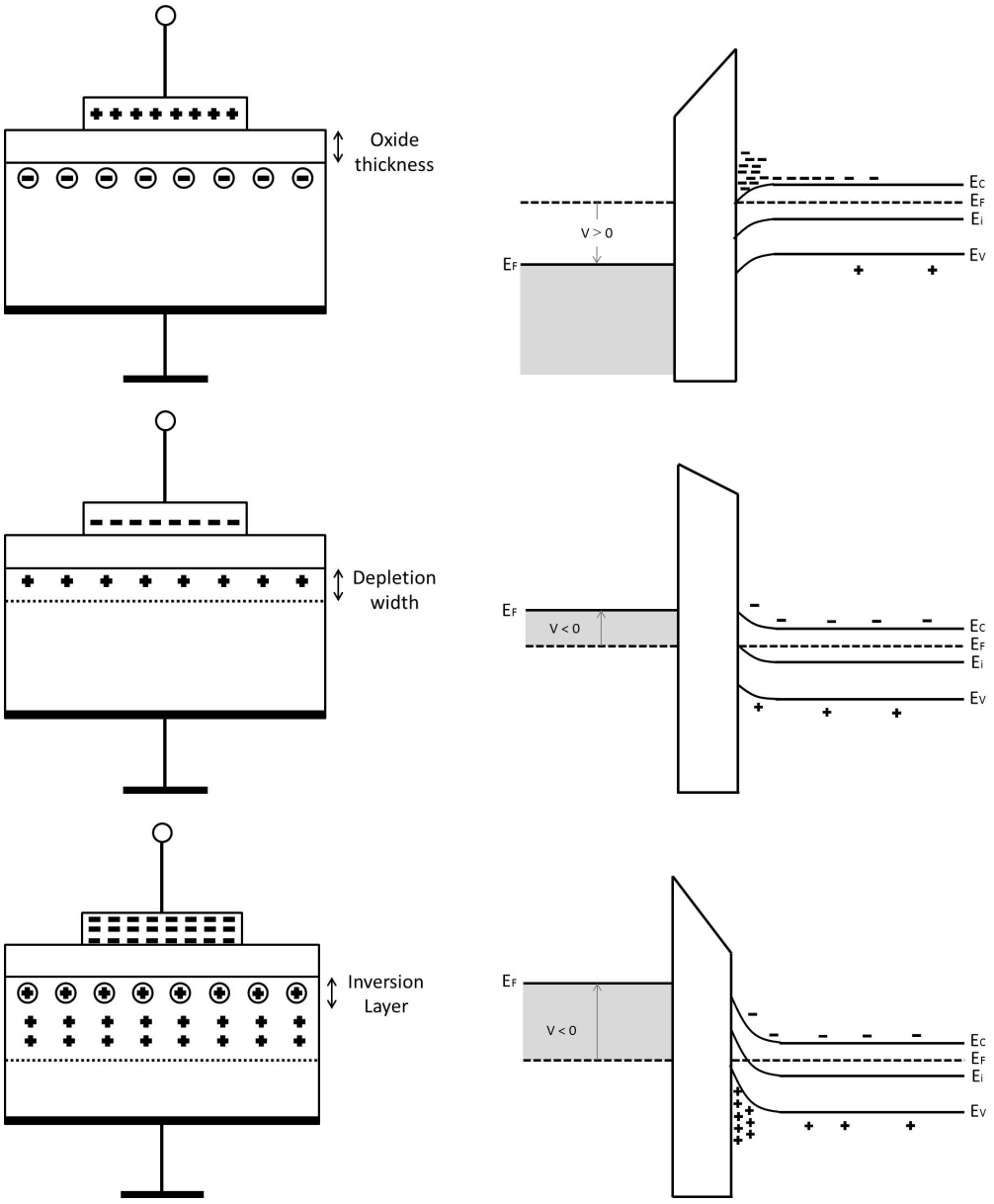


Figure 4.3: Cross-sectional pMOS and energy-band diagram under (*top*) accumulation; (*middle*) depletion and (*bottom*) inversion mode

for an n-type substrate where N_d is the donor density and N_i is the intrinsic density of the semiconductor.

Threshold condition is achieved when minority carrier electrons start to form an inversion layer in between oxide-semiconductor interface and depletion layer region. *Threshold voltage* is defined as the voltage for which hole density (minority carrier density) at the surface equals electron density (majority carrier density) for n-type substrate, a condition where the total potential across the surface equals twice the bulk Fermi potential.

$$\phi_s = -2\phi_F \tag{4.5}$$

Before deriving its expression, several assumptions have to be made. Firstly, this condition occurs under full depletion approximation where the semiconductor is fully-depleted before inversion layer charges start to form. In addition to that, the inversion layer charge is assumed to be zero below threshold and is proportional to V_g beyond threshold.

With reference to Equation 4.5, the expression for maximum depletion width when threshold condition is achieved can be expressed as:

$$x_{d,T} = \sqrt{\frac{2\epsilon_s \left(2\left|\phi_F\right|\right)}{qN_d}} \tag{4.6}$$

where ϵ_s is the permittivity of the semiconductor, and since:

$$Q_{d,T} = qN_d x_{d,T} \tag{4.7}$$

the depletion layer charge at threshold is expressed as:

$$Q_{d,T} = \sqrt{4\epsilon_s qN_d \left|\phi_F\right|} \tag{4.8}$$

Beyond threshold, the total charge in the semiconductor has to balance out the total charge on metal electrode, Q_M:

$$Q_M = -\left(Q_d + Q_{inv}\right) \tag{4.9}$$

where Q_{inv} is the inversion layer charges. In accordance to the following expression for gate voltage,

$$V_G = V_{FB} + \phi_s + \frac{Q_M}{C_{ox}} \tag{4.10}$$

Equation 4.9 is substituted into the equation, yielding:

$$V_G = V_{FB} + \phi_s - \frac{Q_d + Q_{inv}}{C_{ox}} \tag{4.11}$$

In depletion, $Q_{inv} = 0$ so the expression becomes:

$$V_G = V_{FB} + \phi_s - \frac{\sqrt{2\epsilon_s \phi_s qN_d}}{C_{ox}} \qquad for \qquad 0 \leq \phi_s \leq 2\phi_F \tag{4.12}$$

In inversion, the expression is further extended to:

$$V_G = V_{FB} + \phi_s - \frac{\sqrt{2\epsilon_s \phi_s q N_d}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} \tag{4.13}$$

Referring to the assumptions made earlier, it is believed that beyond threshold, inversion layer charges contribute to the change in gate voltage. Hence the first three terms in Equation 4.13 are referred to as the voltage required for threshold condition to occur, and by bringing in the potential equality expression for threshold condition (Refer Equation 4.5), threshold voltage, V_T can be expressed as

$$V_T = V_{FB} - 2\left|\phi_F\right| - \frac{\sqrt{4\epsilon_s q N_d \left|\phi_F\right|}}{C_{ox}} \tag{4.14}$$

MOS capacitance can be obtained from capacitance-voltage (C-V) measurements, where it can provide information on gate oxide thickness and substrate doping concentration (as far as wafer processing is concerned) as well as the threshold voltage and flatband voltage for device characterisation purposes. C-V measurement is a frequency-dependence measurement, in which the corresponding capacitances at inversion (where the dependence primarily occurs) are divided into two types. The first type is called low-frequency capacitance where thermal equilibrium is maintained at all times and minority carrier charges are able to respond to the applied AC signal. High-frequency capacitance, on the other hand, occurs when minority carrier charges are unable to respond to the fast-switching behaviour of the AC signal, hence only a small variation of charges is obtained in comparison to the ones occurred in depletion layer region.

A simple capacitance model can be constructed to illustrate the MOS structure, based on the assumptions made earlier, which consists of two capacitors, representing the oxide capacitance, C_{ox} and depletion layer capacitance, C_d respectively. These two capacitors are arranged in series connection and the circuit is shown in Figure 4.4.

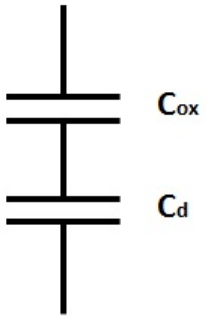


Figure 4.4: Simple Capacitance Model for MOS structure.

An ideal MOS curve for a pMOS operation is shown in Figure 4.5. The application of positive gate voltage causes accumulation of electrons at the surface of the semiconductor substrate. In this condition, the total capacitance is close to the oxide capacitance and therefore, the corresponding maximum capacitance C_{max} of the structure is C_{ox}. As the positive voltage is reduced, electrons move away from the surface and a layer of depleted electrons is created. This region adds to the dielectric region in series with the oxide, reducing total capacitance to $C_{ox}//C_d$.

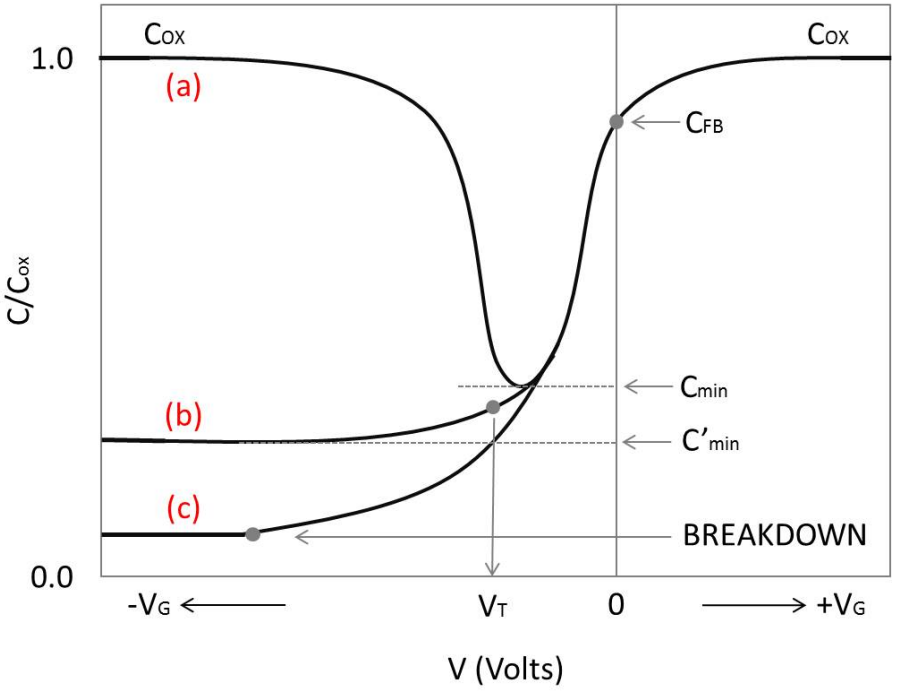


Figure 4.5: C-V Characteristics for Low Frequency and High Frequency Capacitance of a Simple Model pMOS capacitor. (a) Low Frequency (b) High frequency (c) Deep Depletion [82].

When the voltage reaches the threshold condition, inversion occurs and capacitance reaches its corresponding minimum value, C_{min} but when this occurs, capacitance is no longer dependent on the gate voltage, rather on the frequency of the applied AC signal. For low frequency capacitance, minority carriers (in this case, holes) are being added and removed from the inversion layer in response to the infinitesimally slow AC signals, resulting in an increase in total capacitance up to a value close to oxide capacitance again. This corresponds to curve (a) in Figure 4.5 where $C_{LF(inv)} = C_{ox}$.

When high frequency AC signal is applied to the device, inversion layer charges can no longer respond to the signal and remain constant at its DC value. Variation of depletion layer charges occurs around maximum depletion width, $x_{d,T}$ as the AC signal oscillates. Total capacitance consists of $C_{ox}//C_{d,min}$ (shown by curve (b)).

Curve (c) refers to *deep depletion capacitance*, where the total capacitance reduces further than C'_{min} due to the increasing depletion layer width that is beyond its maximum

value as the voltage reduces. This phenomena occurs as holes are not generated fast enough to keep up to the fast-changing AC signal to form an inversion layer hence, causing the depleted region to be extended further. In this case, total capacitance would be very much less than C'_{min} until it reaches a breakdown. To reduce this effect and allow full inversion, capacitance-voltage measurement needs to be done by sweeping the DC voltage from inversion to accumulation, and light needs to be present before the measurement takes place.

The ideal MOS structure discussed earlier assumes a perfectly insulating layer in between metal contact and semiconductor substrate that is infinitely resistive. Unfortunately, this is not the case in reality since oxidation of silicon introduces defects in the Si-SiO_2 interface, where electrically-conducting and non-conducting charges exist. The associated charges affect MOS performance in such a way that an inversion or accumulation layer can form at zero or low bias thus, creating a layer of low resistivity region at the interface and altering bias-dependent capacitance characteristics. This causes unreliable wafer-processing and device performance. Figure 4.6 illustrates four types of charges associated with oxidised silicon.

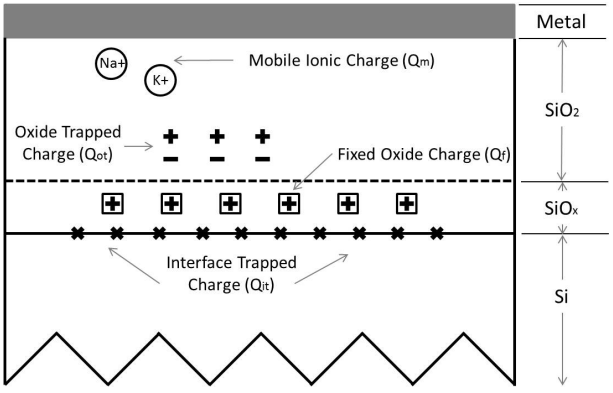


Figure 4.6: Associated Charges at Si-SiO_2 interface [82].

Interface trapped charge, D_{it} exists at the interface, within the forbidden gap due to structural defects, metal impurities and other radiation-caused effects. Unlike oxide charges, this type of charge can be electrically active i.e. becomes positive donor trap by giving up an electron or negative acceptor trap by accepting an electron. Hence, it can be neutralised by low temperature annealing under hydrogen environment at 450 °C. It affects MOS capacitance is such a way that there is a change of charges when the interface-trap level crosses the Fermi level with the application of electric field, altering the MOS characteristic by stretching out the curve obtained from low frequency capacitance-voltage measurement.

Meanwhile, *fixed oxide charge*, Q_f is usually caused by structural defects in silicon during the oxidation process and is located within 2.5 nm of the silicon-silicon dioxide interface [83]. Its density depends on oxidation ambient and temperature, cooling condition and silicon orientation, and is very little affected by the oxide thickness and doping type or

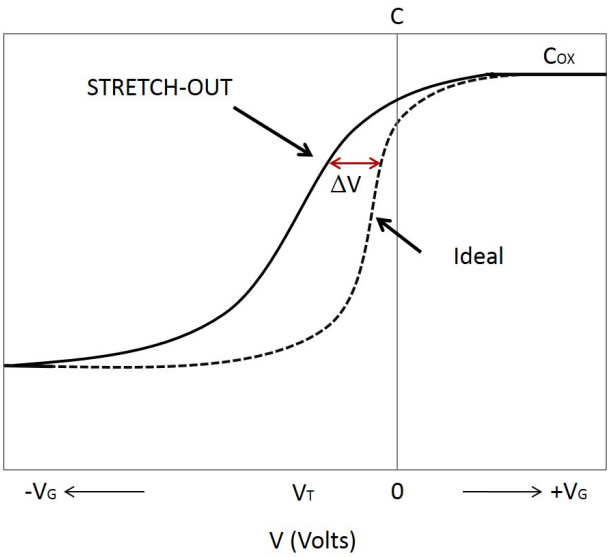


Figure 4.7: Stretch-out capacitance-voltage curve due to interface trapped charge.

concentration. Q_f can be negative, though this type of charge generally appears to be positive. The occurrence of Q_f can be observed from capacitance-voltage curve through a voltage shift, of which the direction of the shift is type-dependent; a left shift for $+Q_f$ and a right shift for $-Q_f$.

For an n-type substrate with $Q_f = 0$, the application of negative bias will require equal amount of positive donor charges to compensate for the negative metal gate charges to satisfy charge neutrality equation. For the same type of substrate with $+Q_f$, this is partly the case. When negative bias is applied to the metal gate, the compensation will first come from $+Q_f$ and the rest will be filled by the positive donors (n-type). When this happens, the depletion width region will become thinner (due to less donor charges needed to balance out the charges on metal gate) hence the capacitance in depletion and weak inversion at any given voltage will be much higher than that from the substrate with $Q_f = 0$. This causes the capacitance-voltage curve to shift to the left. On the other hand, when a negative bias is applied to an n-type substrate with $-Q_f$, more positively-charged donors are required to compensate for the additional charges incurred by $-Q_f$ hence creating thicker depletion width at the interface. The capacitance in the depletion and weak inversion decreases at any given bias, causing the curve to shift to the right. Figure 4.8 shows the curve-shifting of n-type MOS.

Apart from fixed oxide charge, there are two other types of charges associated with oxide layer named *oxide trapped charge* and *mobile ionic charge*, Q_{ot} and Q_m respectively. Oxide trapped charge occurs due to defects in the silicon dioxide layer, and it can be charged by introducing electrons or holes into the oxide. As for the mobile ionic charge, it is commonly associated with the contamination of alkali metal ions (coming from metal

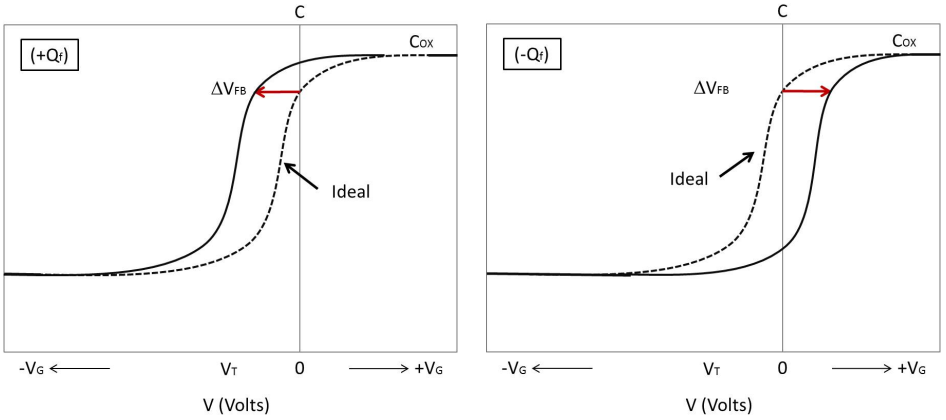


Figure 4.8: C-V curve shift due to fixed oxide charge for n-type semiconductor. (*Left*) with $+Q_f$. (*Right*) with $-Q_f$.

gate contact) [84]. These two charges add to the contribution of fixed oxide charge towards capacitance-voltage curve shift, giving total voltage shift:

$$\Delta V = \Delta V_f + \Delta V_m + \Delta V_{ot} = \frac{Q_o}{C_i} \tag{4.15}$$

where Q_o is equivalent to the sum of effective net oxide charge per unit area given by Q_f, Q_m and Q_{ot}.

4.2 Capacitance-Voltage Characterisation

Basic setup for C-V measurement consists of device under test (DUT), connected in parallel to the C-V meter and DC power source, as shown in Figure 4.9. DC bias voltage is applied across DUT and the capacitance across it is measured by the C-V meter with the application of AC signal with frequencies ranging between 10 kHz to 10 MHz, depending on the C-V meter used in the measurement. DC bias is then swept through a range of voltage to allow the capacitor structure to be at its three operating region, named accumulation, depletion and inversion.

In this measurement, high frequency C-V measurements have been conducted on all fabricated wafers using an Agilent 4279A C-V meter, controlled by HP Visual Engineering Environment (VEE). Each measurement consisted of a voltage being applied to the back contact of the wafer with respect to the top aluminium contact, with DC voltage swept through from inversion to accumulation at a frequency of 1 MHz in the presence of light to avoid deep depletion effect as mentioned earlier. The application of voltage was through the back contact due to the larger contact area in comparison to the top aluminium contact, hence providing better electrical current flow on such a small area.

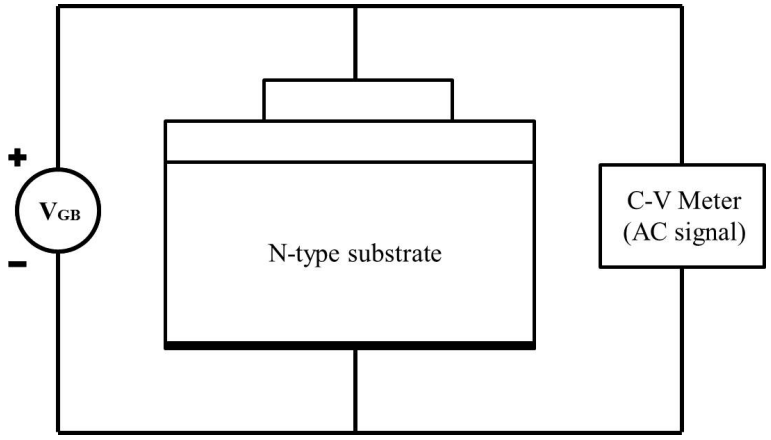


Figure 4.9: C-V measurement circuit for a pMOS capacitor structure

The presence of internal inductance and parasitic capacitance were offset by performing open-circuit and short-circuit calibration on the C-V meter, with measured inductance value below 30 mH and capacitance value of less than 0.5 pF.

Figure 4.10 shows the accurate small-signal equivalent circuit model of a MOS capacitor, where it consists of a parallel combination of frequency-dependent device capacitance, C and effective leakage resistance, R_p connected in series with substrate and gate resistance, R_s. For a highly-resistive substrate-based device, leakage resistance becomes less significant and device is dominated by substrate resistance. The equivalent circuit model can be simplified to a series connection of C_s and R_s, ignoring the small effect of R_p, as shown in the same figure. In C-V measurement setting, a series mode is chosen to obtain a more accurate reading, in which it takes into account the highly resistive nature of the substrate.

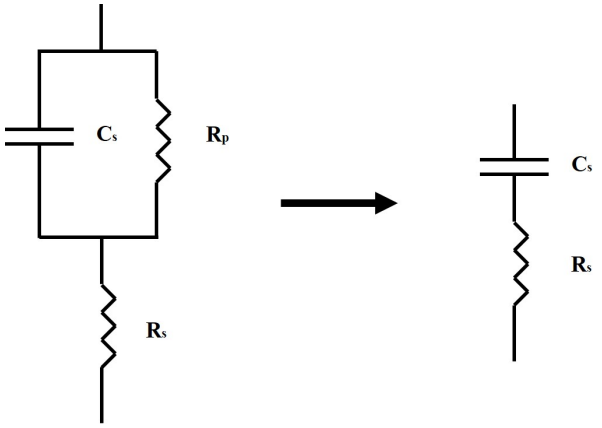


Figure 4.10: (*Left*) Small-signal equivalent circuit model of a MOS capacitor. (*Right*) Circuit representation in MOS capacitor for series mode measurement.

Based on the measurements, area-dependence capacitance measured at strong accumulation ($V > 3$ V) were characterised for capacitors on all substrates to observe its

Oxide Type	**Oxide Thickness (nm)**		
	Nominal	**Ellipsometry**	**Electrical**
Thermal oxide	20	20	34.5
Sputtered oxide	200	172	173

Table 4.1: Oxide thickness comparison between values calculated from C-V measurement data and ellipsometry measurement for Float-zone Si substrates.

relationship with pad size area. For capacitors on Float-zone Si substrates, capacitance scales linearly with area, regardless of oxide types and thicknesses as shown in Figure 4.11. Using the same equation, oxide thickness which represents the separation distance, d was extracted from the gradient of C-A graph (since maximum capacitance in accumulation should be equal to oxide capacitance). By having ϵ_o = 8.85 x 10^{-12} Fm^{-2} and ϵ_{ox} = 3.9, the thickness of oxide layer was calculated and shown in Table 4.1. It can be seen from the table that t_{ox} values obtained from electrical measurement are within tolerable range with the ellipsometry and nominal values hence, C_{acc} equals C_{ox} for capacitors on Float-zone Si substrates.

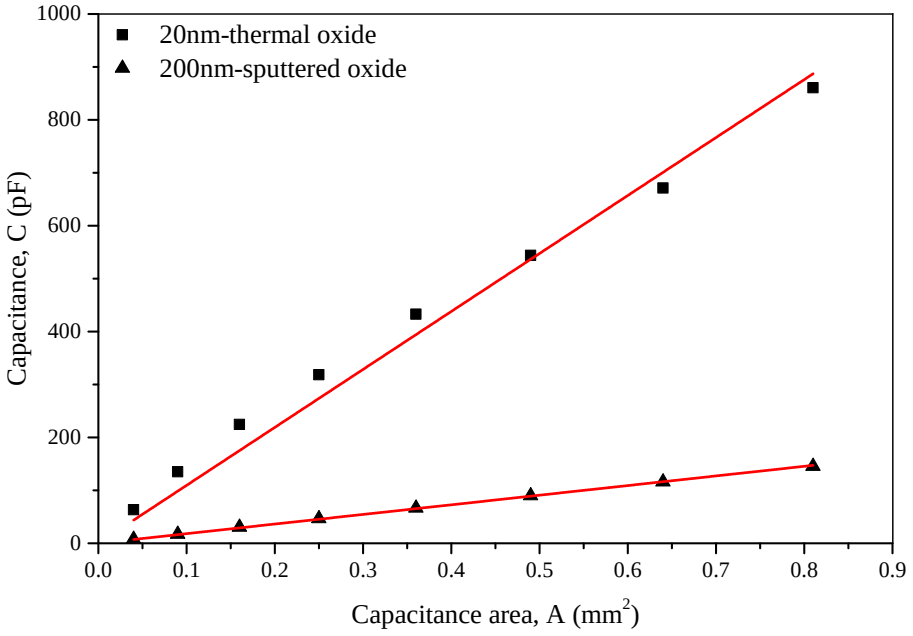


Figure 4.11: Area-dependence capacitance graph for capacitors measured on Float-zone Si substrates with 20-nm-thermal oxide and 200-nm-sputtered oxide.

The same analysis was conducted for capacitors on Au-compensated HR-Si substrates, where the area-dependence graphs are as shown in Figure 4.12. Even though the nominal t_{ox} is the same for all structures, their capacitance values indicate differently, in which the highest capacitance was observed for substrates with thermal oxide. The lowest capacitance values with less than 10 pF were seen for substrates with sputtered oxide, where the values almost reach the parasitic capacitance measured during calibration. In

Substrate Type		Oxide Thickness (nm)		
Etching	**Oxide**	**Nominal**	**Ellipsometry**	**Electrical**
Au-etched	Thermal	20	20	493
Au-etched	Sputtered	20	17.6	34500
–	Thermal	20	20	345
–	Sputtered	20	17.5	8630
–	As-implanted	20	20	4930

Table 4.2: Oxide thickness comparison between values calculated from C-V measurement data and ellipsometry measurement for Au-compensated HR-Si substrates with 20-nm-oxide.

terms of its relationship with area, capacitors on substrates with thermal oxide (with Au-etch or without Au-etch) have lower linearity level in comparison to the ones on substrates with as-implanted oxide and sputtered oxide. Nonetheless, extraction of t_{ox} was performed on these C-A graphs and the values are shown in Table 4.2 where it can be clearly seen that the extracted values are far off the nominal and ellipsometry range. This shows that the approximation of $C_{acc} = C_{ox}$ does not hold true for Au-compensated HR-Si substrates.

To illustrate this matter further, C-V characteristics were summarised in Figure 4.13 for devices with t_{ox} = 20nm. It can be clearly seen that C_{max} in accumulation region for devices on all Au-compensated HR-Si substrates were significantly lower than C_{max} achieved by devices fabricated on Float-zone Si substrates, especially for the ones with

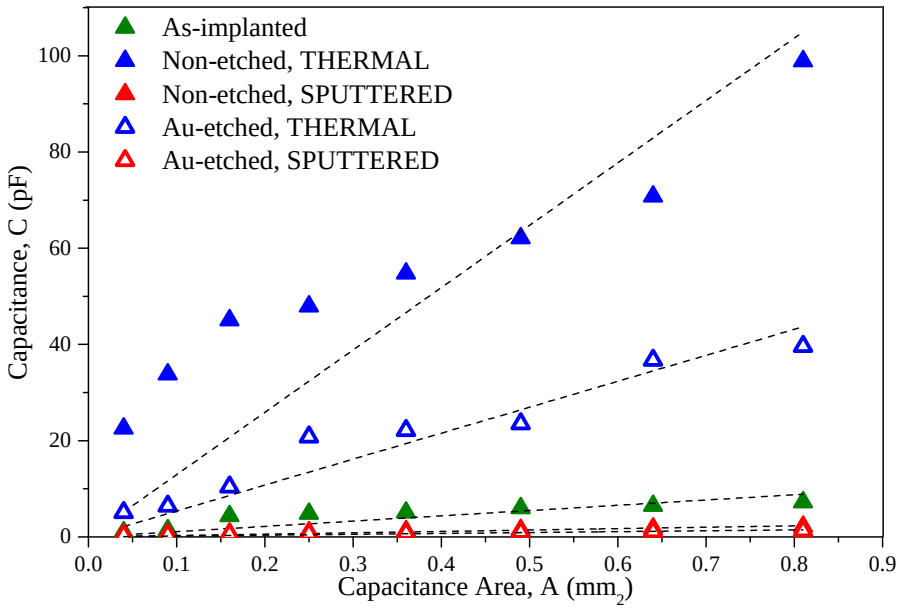


Figure 4.12: Area-dependence capacitance graph for capacitors measured on Au-compensated HR-Si substrates with 20-nm-oxide.

sputtered oxide and sacrificial oxide. Even in the inversion region, the capacitance was observed to be slightly below the ones on Float-zone Si substrates despite having the same nominal oxide thickness. The differences observed can be explained by the high resistive nature of Au-compensated HR-Si substrate in comparison to the 360-Ω-cm Float-zone Si substrates, as shown in the next section.

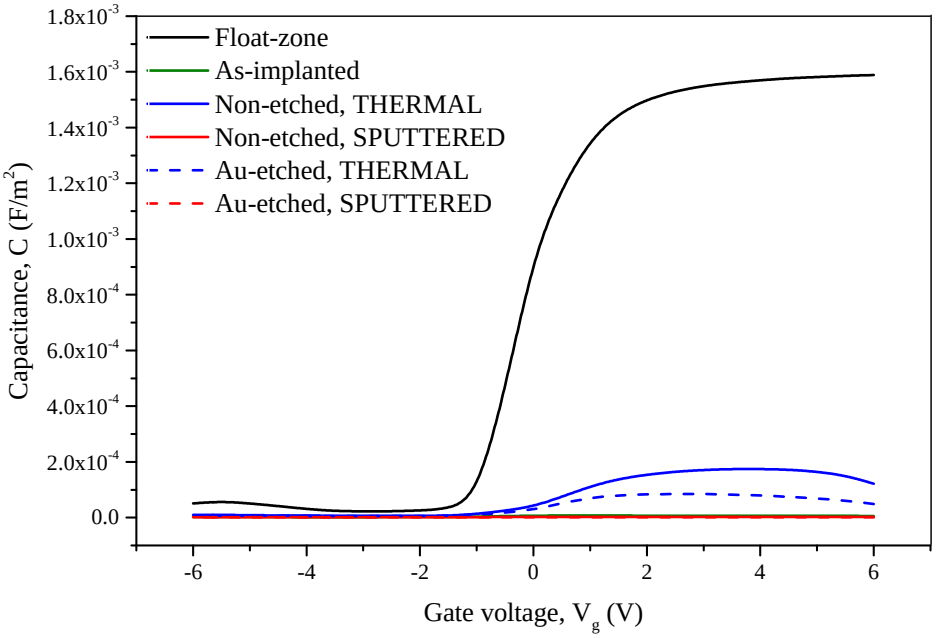


Figure 4.13: C-V characteristics for capacitors with t_{ox} = 20 nm on Au-compensated HR-Si substrates ($\rho >>$ 10 kΩ-cm) and Float-zone Si substrates (ρ = 360 Ω-cm).

4.3 C-V Simulation of MOS Capacitors on High Resistivity Substrates

The effect of increasing substrate resistivity on C-V characterictics was analysed using 2D-TCAD process and device simulation software, SILVACO. For process simulation, ATHENA is used to model metal-oxide-semiconductor device structure that includes oxidation process, ion implantation/diffusion of dopants, and metal deposition, in addition to choosing the right base wafer material substrate. ATLAS is required for device simulation, where the frequency-dependent CV characteristics of the modelled structure was consequently derived.

Structure initialisation of a MOS capacitor in ATHENA can be broken down into several steps, all of which form the important parts of cleanroom processing stage. The steps were summarised in a process flow required for the simulation and shown in Figure 4.14 below. Other steps in Figure 3.22 showing the actual fabrication process flow were not

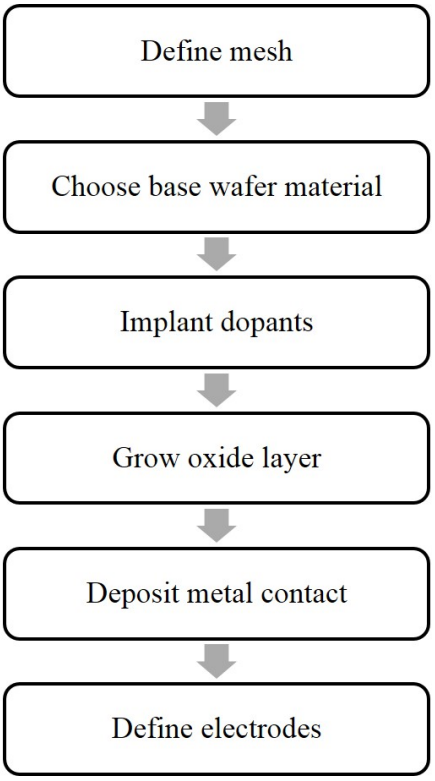


Figure 4.14: Process flow required for simulation of a MOS capacitor.

included in this simulation analysis since those steps do not affect C-V characteristic of the structure.

The mesh was defined such that the cross-sectional area of the analysed substrate and the number of lines required in x and y directions were sufficiently densed to represent the actual size of the wafer substrate and to reduce analysis time. Since it was a 2D simulation, the width of the structure was set to be 1 μm by the software.

To make it n-type, the base structure was implanted with phosphorus. Different concentration was used in each simulation to vary substrate resistivity (i.e. high concentration of phosphorus indicates low resistive substrate, and vice versa) and observed the effect it has on the C-V curve.

Then, a 20-nm-thick oxide was deposited on top of the doped substrate, followed by aluminium contact deposition of 1 μm thickness. The values were chosen to match fabrication specifications. The MOS structure created in ATHENA is shown in Figure 4.15, complete with its defined mesh. A high frequency capacitance-voltage measurement was conducted for the structure using ATLAS at 1 MHz with bias voltage ranging from -6V to 6V. Figure 4.16 shows the effect of increasing substrate resistivity on the C-V curve obtained from ATLAS simulation.

As can be seen in Figure 4.16, increasing substrate resistivity results in lower accumulation capacitance, suppressing the curve until it is even barely noticeable for ρ_{sub}

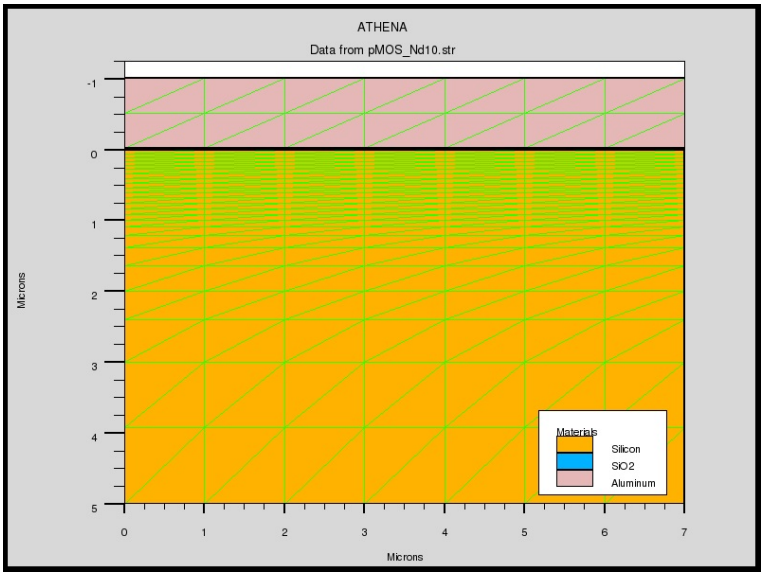


Figure 4.15: MOS structure created in ATHENA.

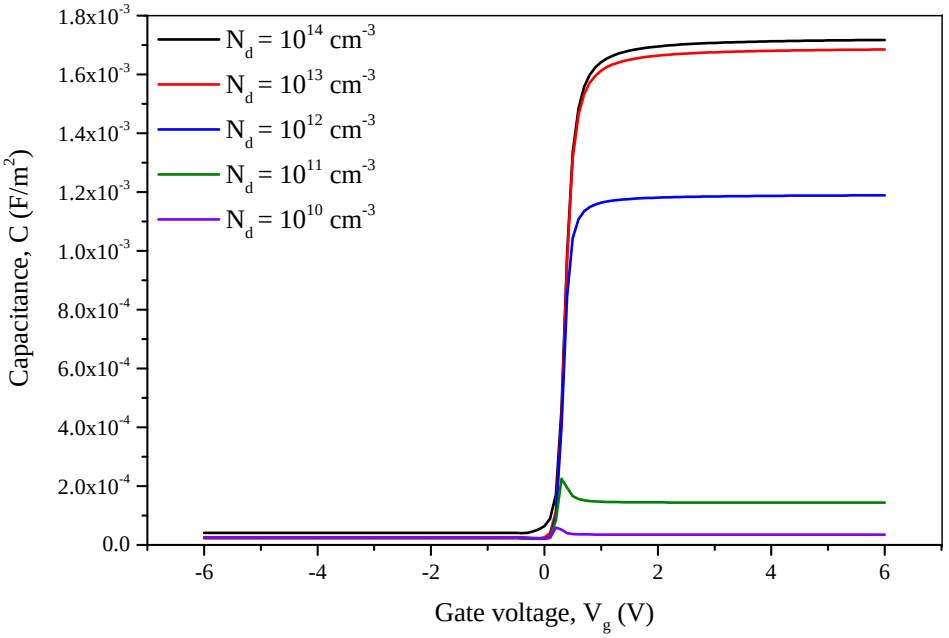


Figure 4.16: Effect of varying substrate resistivity on high frequency C-V characteristics.

= 450 kΩ-cm. These results confirm the suppressed experimental curves obtained for Au-compensated HR-Si substrates. This is explained by longer Debye length in higher resistivity substrates [85]. If Debye length is larger than oxide thickness, the length at which free carrier charges respond to electric field will be far from oxide-silicon interface, causing lower C_{max} in accumulation region.

However, difference in C-V characteristics observed between Au-compensated HR-Si

substrates with different oxides have yet to be explained, considering that ρ_{sub} are the same regardless of oxide type deposited/grown on the substrates. Figure 4.17 shows the relationship between C_{acc} and the corresponding free carrier concentration, n tabulated in Table 2.4 in Chapter 2. Increasing (decreasing) n further than 2 x 10^{13} cm^{-3} (6 x 10^{10} cm^{-3}) will result in maximum (minimum) C_{acc}. Comparing the experimental values, n values for Au-compensated HR-Si substrates with thermal oxide (with and without Au-etching) match comparatively well with simulation values whereas n values for Au-compensated HR-Si substrates with sputtered oxide are significantly lower than simulation values. This dissimilarity will be discussed in the next section where the surface charge effect at Si-SiO_2 interface is being explained.

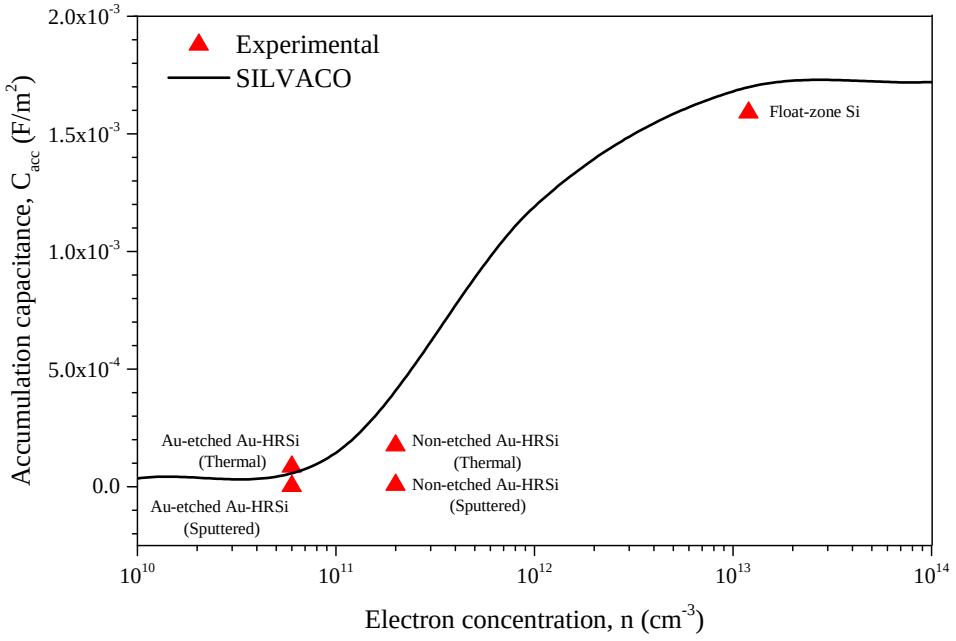


Figure 4.17: The relationship between C_{acc} and majority carrier concentration, n in silicon substrate for pMOS capacitor with 20-nm-thick oxide.

4.4 Surface Charge Effects at Si-SiO_2 Interface

To analyse surface charge effects at the Si-SiO_2 interface, experimental results obtained from capacitors fabricated on Float-zone Si substrates and Au-compensated HR-Si substrates were compared with SILVACO simulation results. Figure 4.18 and Figure 4.19 illustrate the comparison made on C-V curves for MOS capacitors fabricated on Float-zone Si with oxide thickness of 20 nm and 200 nm respectively. Experimental curves in both figures were negatively shifted and stretched out with respect to the simulated curve, indicating the existence of positively fixed oxide charges Q_f and interface trapped charges D_{it} at the Si-SiO_2 interface.

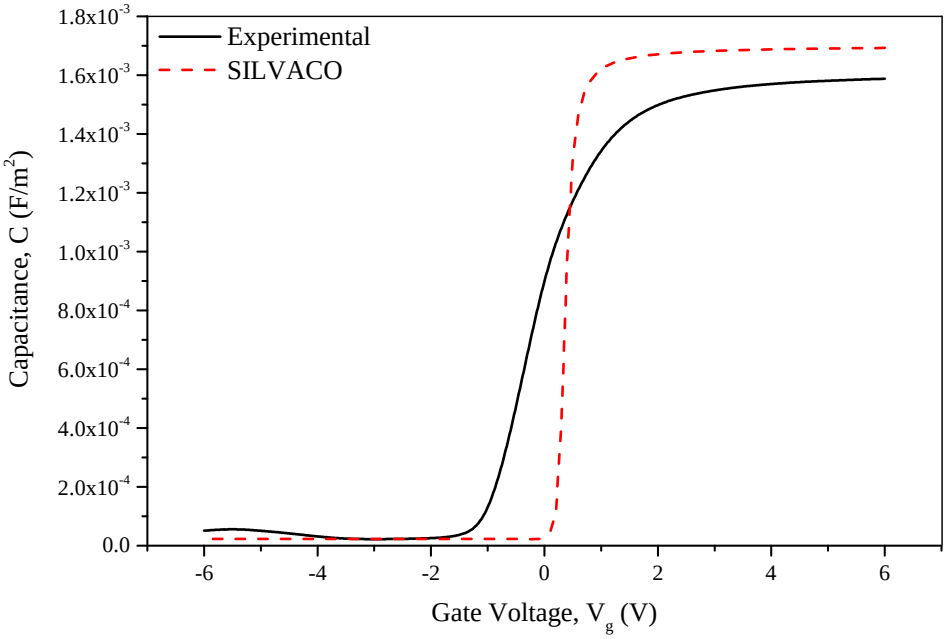


Figure 4.18: Experimental and Simulated C-V characteristics for MOS capacitor on 20nm-thermal oxide, Float-zone Si substrate.

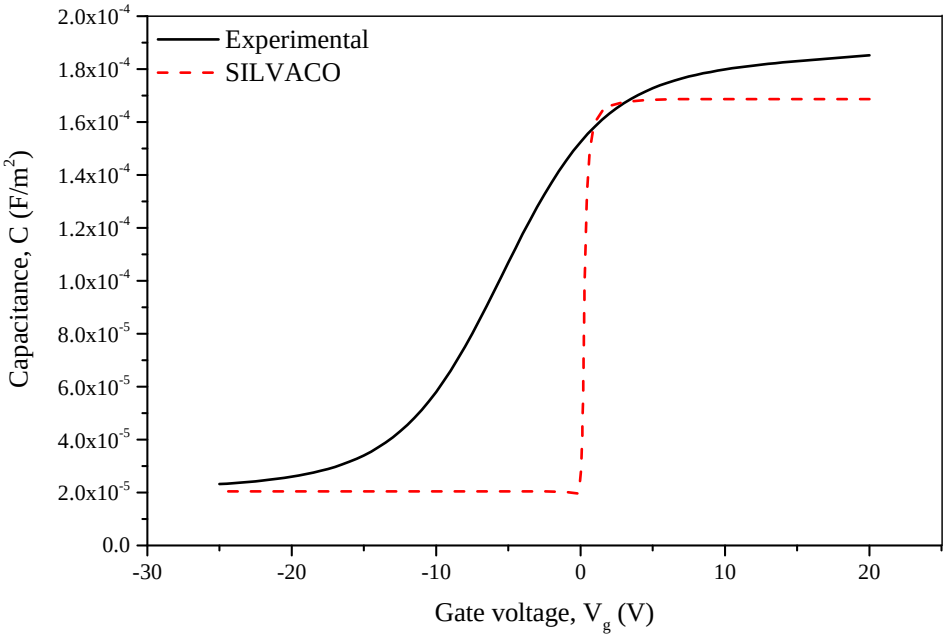


Figure 4.19: Experimental and Simulated C-V characteristics for MOS capacitor on 200nm-sputtered oxide, Float-zone Si substrate.

Oxide type	**Nominal t_{ox} (nm)**	$V_{T(exp)}$ (V)	$V_{T(sim)}$**(V)**	N_{SS} **(cm^{-2})**
Thermal	20	−1.5	−0.15	1.46 x 10^{12}
Sputtered	200	−13	−0.30	1.37 x 10^{12}

Table 4.3: Net oxide charge density determined for Si-SiO_2 interface layer of MOS structure fabricated on Float-zone Si substrates.

Numerical analysis has been done on these characterictics to quantify Q_f at the interface which have caused the negative voltage shift on the curve. The corresponding net oxide charge density, N_{SS} can be expressed as:

$$N_{SS} = \frac{C_{ox}\Delta V_T}{q} \tag{4.16}$$

where ΔV_T is taken to be the difference in threshold voltage obtained from electrical measurement and simulation whereas C_{ox} is the nominal oxide capacitance per unit area. Table 4.3 shows the result of the analysis based on the C-V curves. The values of N_{SS} obtained from both substrates are almost similar, which shows that the type of oxide or its thickness do not affect Q_f. However, the large stretch-out of V_T seen for capacitors with 200nm-sputtered oxide indicates higher D_{it} for sputtered oxide in comparison to thermal oxide.

The same analysis was performed on Au-compensated HR-Si substrates, with and without Au-etching effect. Figure 4.20 shows the C-V characteristics for capacitors on Au-etched Au-compensated HR-Si substrates with 20 nm thermal and sputtered oxide. With regards to Au-compensated HR-Si substrate with thermal oxide, the characteristic shows evidence of the existence of Q_f and D_{it}, where V_T is observed to be shifted to -1.5V and its curve is stretched-out with respect to SILVACO simulation curve. Since the amount of V_T shift is the same as the one seen in Fz-Si substrate (refer Table 4.3), N_{SS} due to Q_f in Au-compensated Au-HRSi substrates is said to be equal to the ones in Fz-Si substrates. In addition to that, experimental C_{max} reaches simulated C_{max} though the value does not saturate at increased positive bias. Deep-depletion effect is also apparent in the inversion region even though all measurements were conducted in light environment. Meanwhile, for Au-etched Au-compensated HR-Si with sputtered oxide, the characteristic curve was flatted-out to portray its non-responsive nature towards AC signal.

Similar observations were concluded from C-V characteristics for capacitors on Au-compensated HR-Si without Au-etching as shown in Figure 4.21. The only difference observed is that C_{max} from the experimental curve for Au-compensated HR-Si with thermal oxide does not even reach C_{max} of simulation at all, illustrating possible existence of another layer which is also depleted from carrier charges and consequently contributing to longer Debye length.

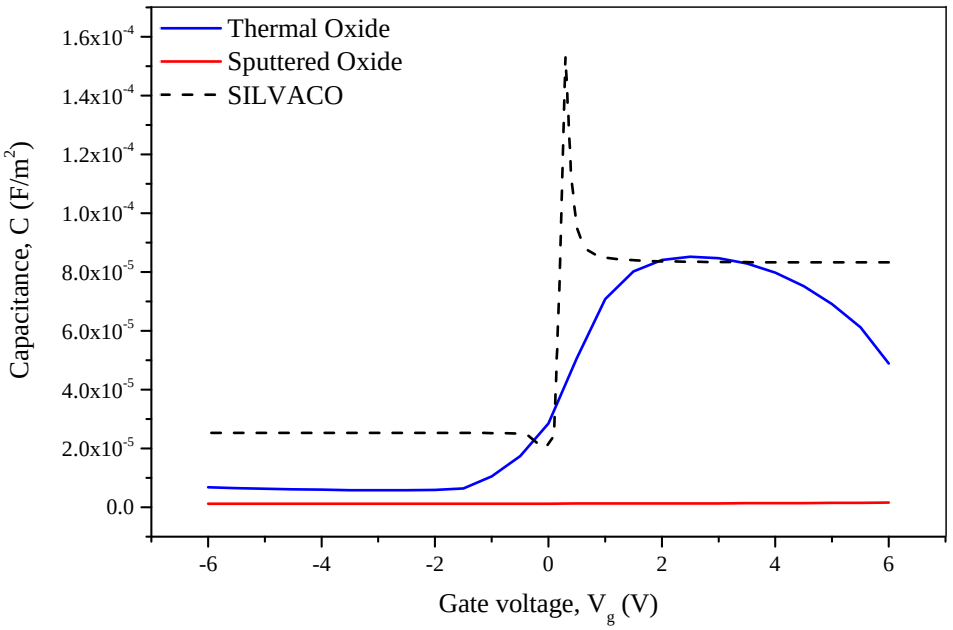


Figure 4.20: C-V characteristics for MOS capacitors on Au-etched Au-compensated HR-Si substrates with 20-nm-oxide.

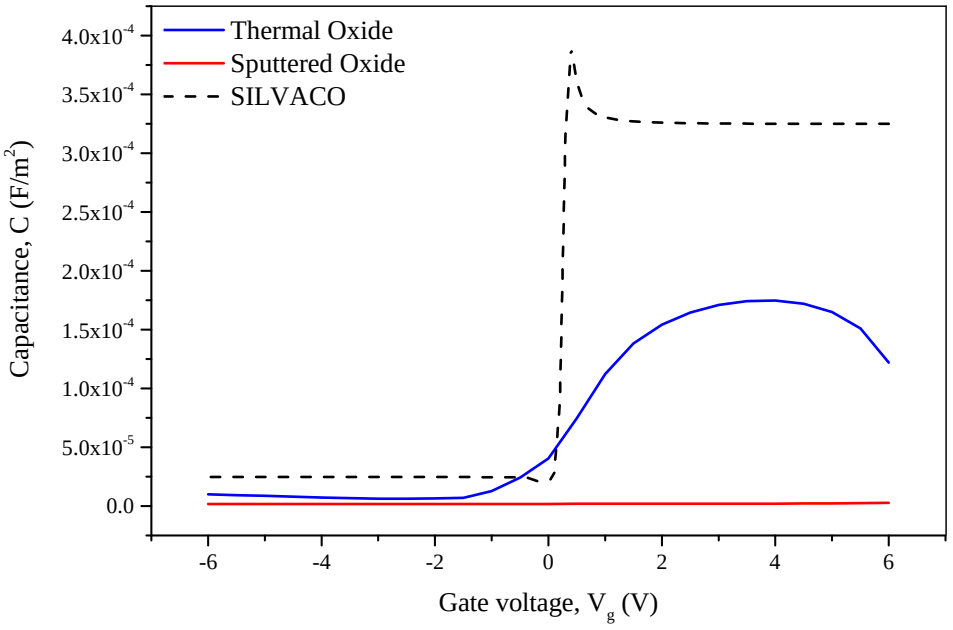


Figure 4.21: C-V characteristics for MOS capacitors on non Au-etched Au-compensated HR-Si substrates with 20-nm-oxide.

4.5 Summary

Capacitance-voltage characteristics of Au-compensated HR-Si substrates were studied in this chapter, where the approximation of $C_{acc} = C_{ox}$ is shown to be invalid due to the high resistivity nature of the substrates and longer Debye length. SILVACO simulations were conducted to show the effect of high resistivity substrates on C-V characterisations. Suppression of accumulation response is seen for high resistivity substrates especially when the value starts to reach 45 kΩ-cm, confirming the experimental C-V suppression shown by Au-compensated HR-Si substrates. Analysis on surface charge effect on Au-compensated HR-Si substrates shows potential suppression for substrates with sputtered oxide where non-responsive C-V curves were obtained at range of voltage measured.

Chapter 5

Suppression of Parasitic Surface Conduction using CPW Loss Analysis

As has been discussed in the previous chapter, capacitance-voltage characteristics for MOS structure fabricated on Au-compensated Si substrates show reduced dependency on bias voltage, indicating the possibility of PSC suppression at Au-compensated Si substrate surfaces. In this chapter, microwave characteristics of coplanar waveguides are used to evaluate the potential of Au-compensated Si substrates to suppress PSC effect and increase substrate resistivity effectively to ensure low-loss microwave performance is achieved.

For the purpose of this work, conductor-backed coplanar waveguides were designed and fabricated on top of Au-compensated Si substrate where particular attention has been paid on the planar dimension of the CPW structure to minimise losses contributed by impedance-mismatching. The losses measured are hence, mostly coming from the substrates. Microwave measurements were conducted to analyse attenuation loss of coplanar waveguides and to evaluate factors affecting loss characteristics of these devices on Au-compensated Si substrate.

5.1 Attenuation Loss Mechanism of a Coplanar Waveguide

Coplanar waveguide transmission lines are used to transmit microwave frequency signals in MMICs technology. Unlike microstrip lines, coplanar waveguides offer reduced complexity in terms of fabrication and circuit integration due to the ground lines being on the same plane as its signal line. In addition, its planar dimension can be designed

in such a way to fit any required characteristic impedance hence the risk of impedance-mismatching between source and load can be reduced.

Schematic structure of a conventional CPW on a naked substrate without top cover is shown in Figure 5.1 where the ground lines, G have the same planarity as the signal line denoted by S. Travelling wave propagates in the outward direction from signal line to ground lines through the air and into the substrate, as shown in Figure 5.2.

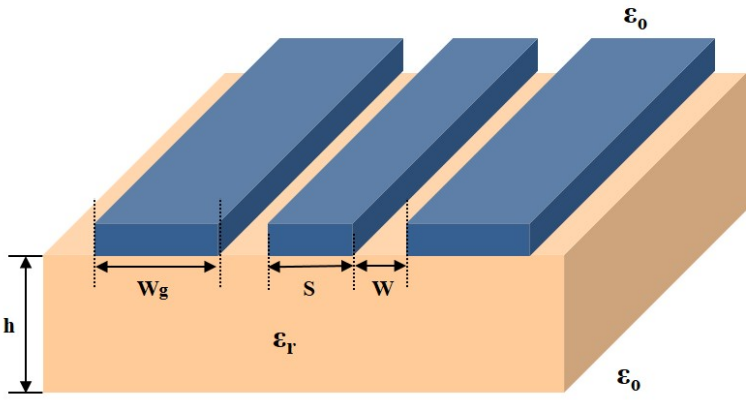


Figure 5.1: Conventional CPW on a naked substrate without top cover [86].

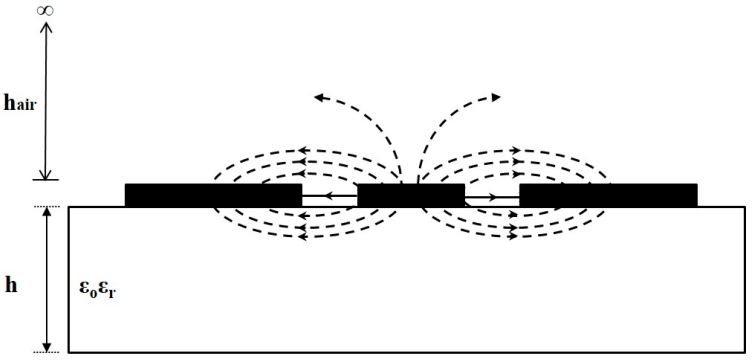


Figure 5.2: Electric field distributions for CPW in even mode [86].

Full signal transmission is not achievable in any transmission line structure including CPW. Therefore, losses are introduced. Apart from radiation losses, there are two main mechanisms of CPW losses; ohmic and dielectric, which represent losses associated with CPW metal conductor lines and substrate's finite resistance, respectively [86]. The expression for conductor loss in CPWs (in dB/length) is given by:

$$\alpha_c = \frac{8.68 R_S \sqrt{\epsilon_{r,eff}}}{240\pi K(k) K(k')(1-k^2)} [\Phi(S) + \Phi(W)] \tag{5.1}$$

where:

$$\Phi(x) = \frac{1}{x}\left[\pi + ln\left(4\pi\frac{x}{t}\frac{1-k}{1+k}\right)\right] \tag{5.2}$$

$$k = \frac{S}{S+2W} \tag{5.3}$$

$$k^{'} = \sqrt{1-k^2} \tag{5.4}$$

and *K(k)* is the complete elliptic integral of the first kind and $\epsilon_{r,eff}$ is the effective permittivity of the structure. R_S is metal surface resistance represented by:

$$R_S = \sqrt{\pi f \rho \mu_o} \tag{5.5}$$

where f is the operating frequency, ρ is metal resistivity and μ_o is vacuum permeability given by 4πx10^{-7} H/m. Based on the relationships seen in Equation 5.2 to Equation 5.5, α_c shows strong dependency on CPW dimension and metal resistivity and is shown to be directly proportional to $\sqrt{f}$.

Meanwhile, substrate loss, α_d contributed by substrate's finite resistance is given by [86] (in dB/length):

$$\alpha_d = 27.3\frac{\epsilon_r}{\sqrt{\epsilon_{r,eff}}}\frac{\epsilon_{r,eff}-1}{\epsilon_r-1}\frac{tan\delta}{\lambda_o} \tag{5.6}$$

where λ_o is wavelength of free-space and tan δ is dielectric loss tangent of the semiconductor expressed by [87]:

$$tan\delta = tan\delta_d + \frac{\sigma}{\omega\epsilon_o\epsilon_r} \tag{5.7}$$

As can be seen in Equation 5.7, there are two parts of losses in semiconductor. tan δ_d represents intrinsic loss coming from pure semiconductor whereas the latter part of the equation is contributed extrinsically by doping property of semiconductor, mainly originating from free charge carriers. For doped semiconductor substrate operating in high frequency range, tan δ_d is considered to be small and can be neglected [88]. Assuming a thick substrate ($h \to \infty$), Equation 5.6 can be simplified to give [89]:

$$\alpha_d = 8.68\frac{30\pi}{\sqrt{\epsilon_{r,eff}\rho_{Si}}} \tag{5.8}$$

where ρ_{sub} is substrate resistivity. From the expression, substrate loss is seen to be inversely proportional to ρ_{sub} indicating the importance of having substrate with high resistivity to reduce total CPW losses.

Apart from the losses coming from α_c and α_d, there is another contribution that makes up the total CPW losses in silicon-based MMICs (SiMMICs) circuit application and that is called bias-dependent interface loss as discussed in [31]. Interface losses in CPW occur as a result of PSC effect where the movement of charge carriers at the interface due to change in electric field creates a low resistivity region at the silicon surface with the magnitude of loss generated depends greatly on bias voltage. This loss can only be analysed qualitatively from microwave characterisation where the total attenuation loss of a CPW is obtained [32, 90, 91].

For a two-port S-parameter measurement, the expression for CPW attenuation can be derived from Beer-Lambert law [92]:

$$\frac{I_l}{I_o} = 10^{-\alpha l} \tag{5.9}$$

where I_l is the intensity of transmitted power through CPW line with length l and I_o is the intensity of incident power. It can be further expanded to give:

$$\frac{I_l}{I_o} = \frac{I_l}{I - R} = \frac{I_l/I}{1 - R/I} = 10^{-\alpha l} \tag{5.10}$$

with I total power supplied by VNA and R is the reflected power. The numerator of the third expression represents the fraction of transmitted power through the system from port 1 to port 2 whereas the denominator represents the fraction of reflected power back to port 1 with respect to total power generated. The fractional terms can be translated into magnitude of S_{21}, in the former case and S_{11} for the latter, giving $|S_{12}|^2$ and $|S_{11}|^2$ respectively.

Hence, the expression can be re-written as:

$$\left[\frac{|S_{21}|^2}{1 - |S_{11}|^2}\right] = 10^{-\alpha l} \tag{5.11}$$

As a result, total attenuation loss of a CPW in dB per unit l can be expressed as:

$$\alpha = -\frac{10}{l} log_{10}\left[\frac{|S_{21}|^2}{1 - |S_{11}|^2}\right] \tag{5.12}$$

Another way of characterising CPW losses through S-parameter measurements can be done by using the distributed-element CPW transmission line model analysis. In this analysis, complex propagation loss and characteristic impedance of the line can be determined,

5.2 Characterisation of CPW Loss using Transmission Line Model

Coplanar waveguide transmisssion line for microwave application is considered as a distributed-element network since the smallest physical dimension of the line is comparable to the wavelength range of operation. However, the structure can be treated as a lumped-element model which can be represented by an equivalent circuit model for an infinitesmal length denoted by Δx. Figure 5.3 shows the representation of CPW transmission line which consists of a combination of *R, L, G* and *C* components.

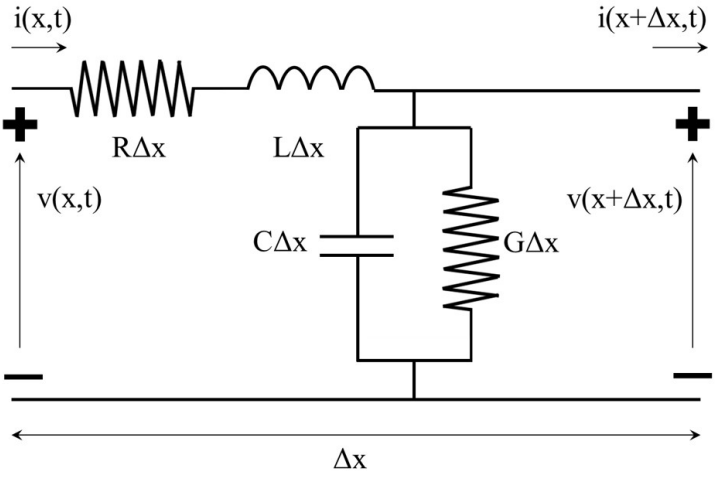


Figure 5.3: Lumped-element equivalent circuit model for an incremental length of a distributed-element CPW transmission line.

R and *G* represent losses associated with metal conductor lines and dielectric of the structure surrounding the lines whereas *L* and *C* are self-inductance and shunt capacitance between two conductor lines which are in close proximity with each other. By making use of Kirchhoff's first and second laws, the equivalent circuit model shown above can be used to derive complex propagation constant, γ and characteristic impedance, Z_L of the line, which give [93]:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{5.13}$$

$$Z_L = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{5.14}$$

where α and β are attenuation constant and phase constant respectively.

Rearranging equations Equation 5.13 and Equation 5.14 will then provide R, L, G and C expressions in terms of γ and Z_L as depicted below:

$$R = Re(\gamma \cdot Z_L) \tag{5.15}$$

$$L = \frac{Im(\gamma \cdot Z_L)}{\omega} \tag{5.16}$$

$$G = Re(\frac{\gamma}{Z_L}) \tag{5.17}$$

$$C = \frac{Im(\frac{\gamma}{Z_L})}{\omega} \tag{5.18}$$

where ω is the angular frequency given by 2πf.

Extraction of γ and Z_L can be obtained from on-wafer microwave characterisation, where two-port, frequency-dependent S-parameter are measured by a vector network analyser (VNA). Under perfectly-matched transmission line condition, power transfer ratio is equal to 1 where there is no reflection of transmission signal at both ports and transmitted power at one port is reciprocal to one another [94]. This means that losses are attributed purely from metal and dielectric of the structure to give:

$$S_{11} = S_{22} \tag{5.19}$$

$$S_{21} = S_{12} \tag{5.20}$$

By taking into account power losses due to reflected signal at both ports individually (represented by reflection coefficient Γ) and by considering $Z_o = 50\ \Omega$ as VNA's reference impedance, γ and Z_L expressions in terms of S-parameter values can be found from [95]:

$$e^{-\gamma L} = \left(\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm \sqrt{\frac{(S_{11}^2 - S_{12}^2 + 1)^2 - (2S_{11}^2)}{(2S_{21})^2}} \right)^{-1} \tag{5.21}$$

$$Z_L = Z_o\sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} \tag{5.22}$$

As have been stated in Equation 5.13, total attenuation loss, α is the real part of γ and is measured in nepers/length. To quantify the value in dB/length,

$$\alpha\,(\text{dB/length}) = \alpha\,(\text{Np/length})\;\text{x}\;\frac{20}{\ln 10} \tag{5.23}$$

Both Equation 5.12 and Equation 5.23 can be used to extract the total attenuation loss of CPW from S-parameter measurements. S-parameter data extracted from SONNET simulation conducted on metal-oxide-silicon CPW structure with 200 μm on varying substrate's resistivities were used to verify both expressions before they were used in the experimental analysis. Figure 5.4 shows the comparison between Equation 5.12 obtained from Beer-Lambert law and Equation 5.23 extracted from the real part of complex γ. Based on the figure, the responses obtained from Beer-Lambert expression are very much similar to the ones obtained from γ expression. For ease of analysis, Equation 5.12 from Beer-Lambert law was used to extract attenuation losses of CPWs measured in this work.

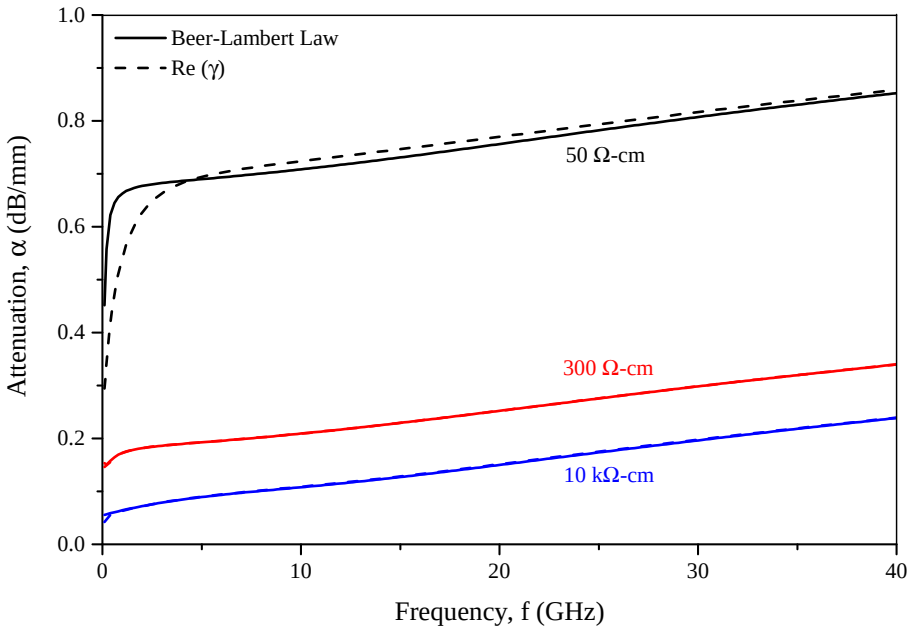


Figure 5.4: Attenuation losses of CPWs obtained analytically from SONNET simulations on CPW structures with 200-μm oxide on varying substrate resistivities. Comparisons are made between values obtained from Equation 5.13 extracted from Beer-Lambert law and Equation 5.23 extracted from complex γ.

5.3 Attenuation Loss of CPW on Au-compensated HR-Si Substrates

S-parameter measurements was conducted using an Agilent Technologies E8691A Vector Network Analyser (VNA) to obtain attenuation coefficient. It was calibrated using impedance standard substrate (ISS) containing Au S-O-L-T (Short-Open-Load-Thru) calibration structures and 50 Ω Au CPWs on a 1 x 10^{14} Ω-cm alumina substrate with dimension almost identical to the CPWs on Au-compensated HR-Si substrates. The contacts on the structure were made using probes with a Ground-Signal-Ground (GSG) configuration operating up until 67 GHz, a Cascade Microtech Summit 12000B-AP semi-automatic probe station and the VNA. All measurements were repeated on at least 6 nominally identical devices as shown in Appendix C. Distribution was very narrow and typical device has been taken for analysis.

After calibration, S-parameters for CPWs of different lengths were measured over a frequency range of 0.01 to 40 GHz. Return loss and insertion loss responses for 6400 μm CPW on Float-zone Si and Au-compensated HR-Si substrates with oxide thickness of 20 nm is shown in Figure 5.5 and Figure 5.6 respectively. Low return loss was observed for all devices (less than -10 dB) indicating less than 10% of input power was reflected and good impedance-matching was achieved with CPW dimensions worked out in previous chapter. With regards to signal power transmission, a significantly higher insertion loss was seen for devices on Float-zone Si substrates in comparison to devices on Au-compensated HR-Si substrates. Since similar CPW dimensions are used on both substrates, the additional losses are considered to be originated from the substrate itself.

CPW attenuation for frequencies up to 40 GHz was calculated using responses obtained in S-parameter measurement and by manipulating attenuation expression as shown and explained in Section 5.1. Attenuation measured at 1, 10, 20 and 40 GHz was plotted as a function of CPW length for devices on all Au-compensated HR-Si substrates. Figure 5.7 illustrates the proportionality of CPW attenuation with its length that was seen on each individual substrate, regardless of oxide type. Attenuation responses for devices on Float-zone Si substrates with 20 nm thermal oxide are included as comparison. It suffices to say that CPW attenuation is directly proportional to its length for all substrates, taking out of account a few outliers spotted in several figures. Also, the level of attenuation is observed to be lower than CPWs on Float-Zone Si for all Au-compensated Si substrates.

CPW attenuation per unit length (unit dB/mm) was then tabulated as a function of frequency, as illustrated in Figure 5.8. For the 20-nm-thick oxide, attenuation loss for CPWs on Au-compensated HR-Si substrates are seen to be 50% lower than CPWs fabricated on Float-zone Si substrates at all frequencies, supporting the results shown previously.

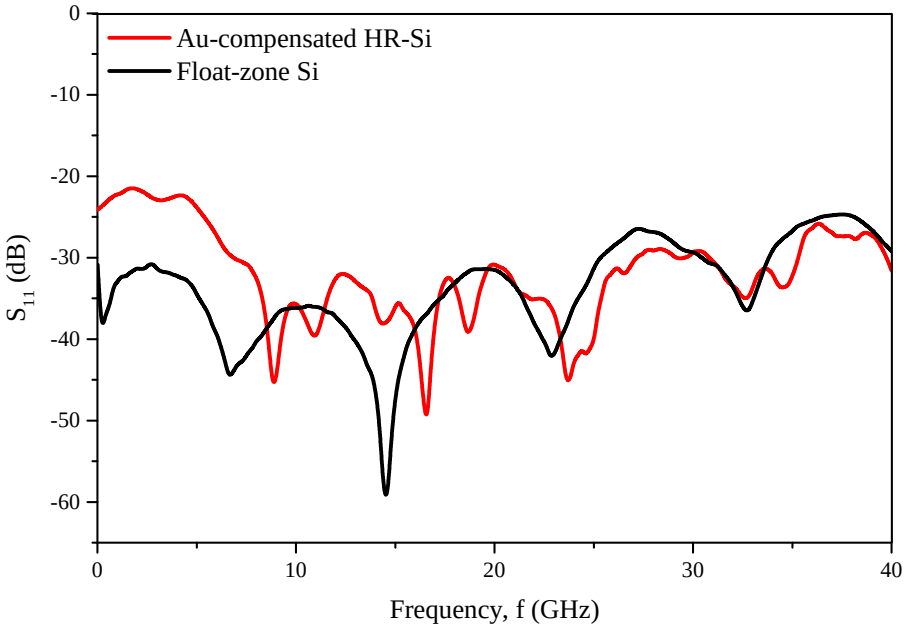


Figure 5.5: Experimental return loss for 6400 μm CPW with 20-nm-thick sputtered SiO_2.

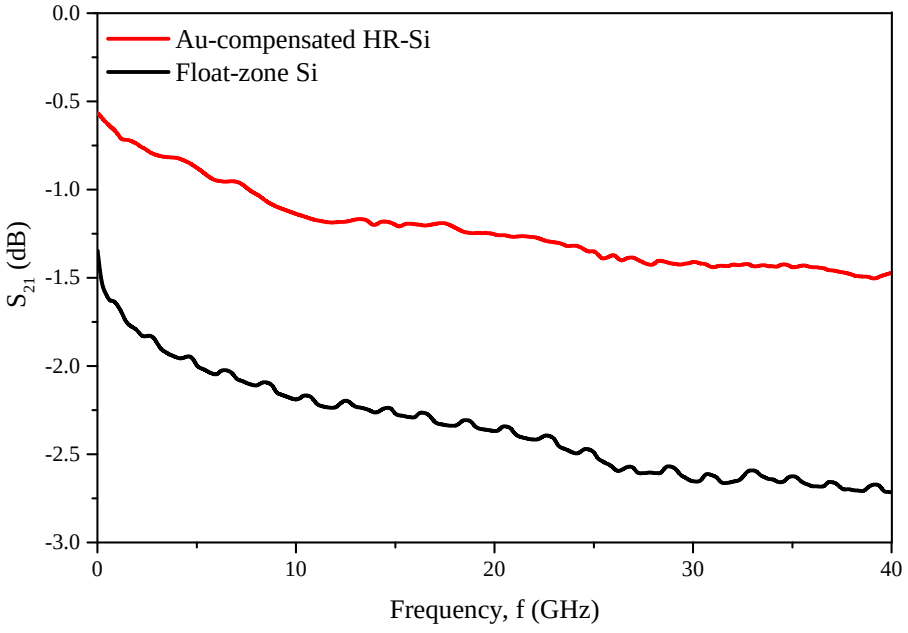


Figure 5.6: Experimental insertion loss for 6400 μm CPW with 20-nm-thick sputtered SiO_2.

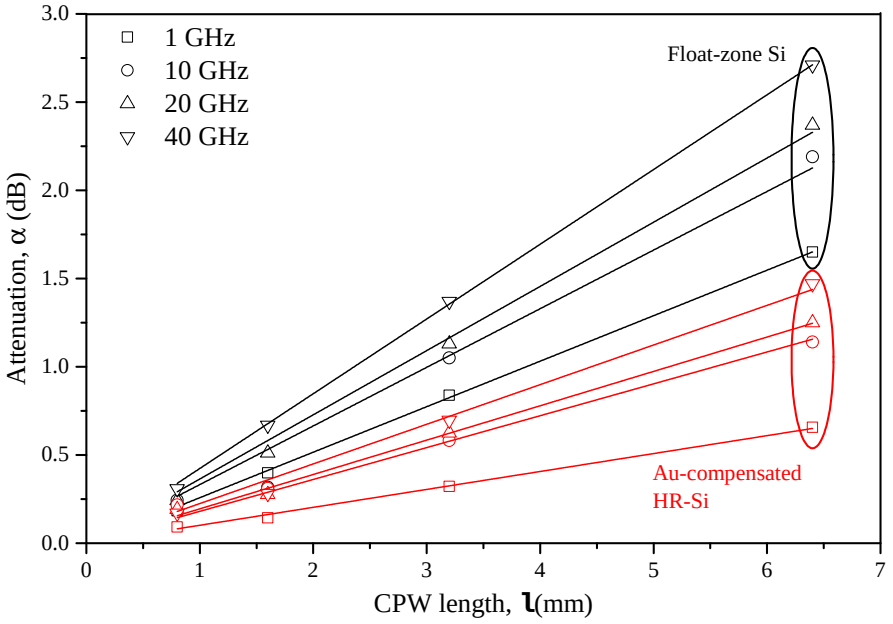


Figure 5.7: Attenuation loss as a function of length for CPWs on Au-compensated HR-Si and Float-zone Si substrates with 20nm SiO_2.

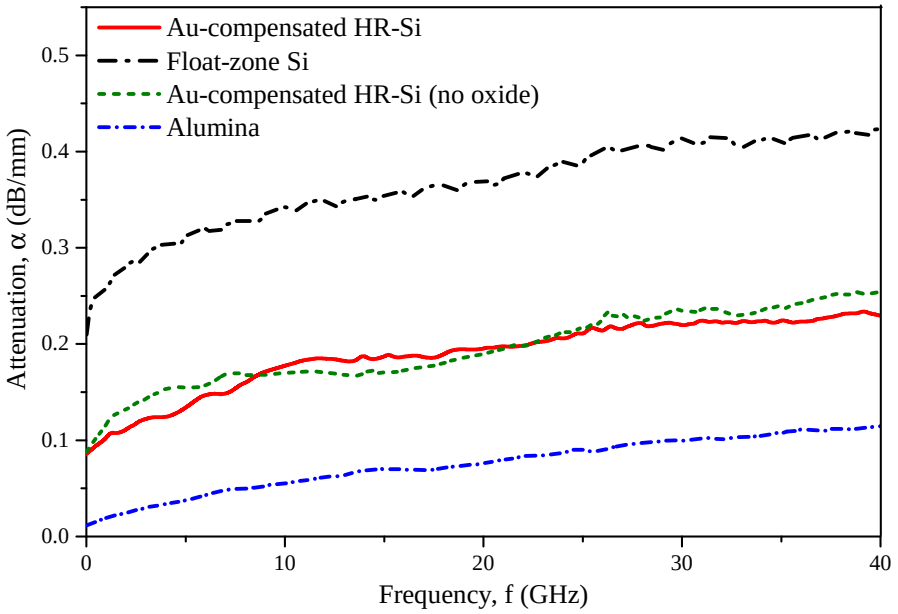


Figure 5.8: Attenuation loss as a function of frequency for CPWs on various substrates with 20nm SiO_2.

This is due to Au-compensated HR-Si substrates being higher in resistivity compared to Float-zone Si substrates, with reduced number of background free carriers. The observed attenuations are only twice the values obtained from CPWs fabricated on alumina substrates and are comparable to CPWs on naked (without oxide) Au-compensated HR-Si substrates, suggesting the potential of Au-compensated HR-Si substrates to suppress PSC-dependent charges at Si-SiO_2 interface.

5.4 Suppression of Parasitic Surface Conduction (PSC) using Au-Si Substrates

To further investigate the potential of Au-compensated Si substrate to suppress parasitic surface conduction effect at Si-SiO_2 interface, bias-dependent RF measurements were conducted by back-biasing CPW structure with a constant DC gate voltage ranging between +6 V and -6 V, where accumulation and inversion are suspected to occur. Figure 5.9 shows the variation in CPW attenuation with respect to gate voltage on Au-compensated HR-Si substrates and Float-zone Si substrates. Attenuation responses for CPWs on TOPSIL's Float-zone HiRes^{TM} substrates with resistivity > 10 kΩ-cm are also included as comparison.

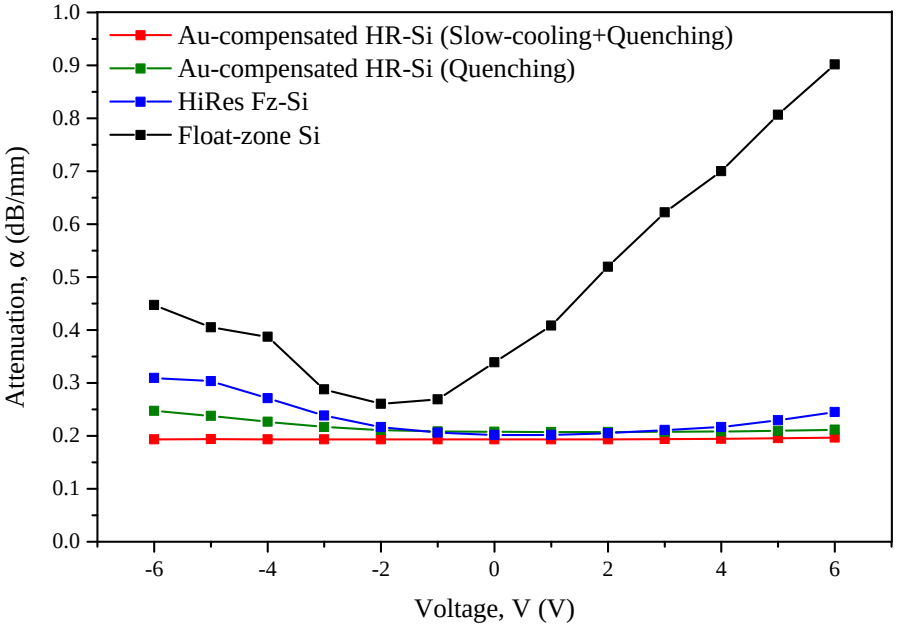


Figure 5.9: Attenuation loss as a function of voltage of CPWs on Au-compensated HR-Si substrates developed through different annealing procedures, i.e. quenching or the combined procedure of slow-cooling and quenching. Included as comparisons are responses for CPWs on Float-zone Si and TOPSIL's HiRes Fz-Si.

With regards to attenuation of CPWs on Float-zone Si substrate, it is shown that attenuation loss increases strongly with increasing positive and negative bias, having its minimum value between -1 V to -3 V. The lowest attenuation region corresponds to the depletion state of the structure, whereas the additional losses incurred by the incremental positive and negative voltages refer to accumulation and inversion states, respectively. As can be seen in the corresponding C-V characteristics in Section 4.2 of the previous chapter, these additional losses are due to the parasitic surface conduction (PSC) layer formed at the Si-SiO_2 interface. The higher attenuation seen in accumulation compared to inversion occurs due to majority carrier electrons having higher mobility than minority carrier holes, which results in higher conduction and more loss.

Similar dependency with less magnitude is seen in attenuation for CPWs on HiRes Fz-Si substrates. However, stronger bias-dependency response is shown in the inversion region in comparison to the accumulation region, contradicting the trend seen in the standard Float-zone Si substrates. The lesser magnitude observed in accumulation is due to the high resistivity nature of HiRes Fz-Si substrates, where reduced number of majority carriers exist in the substrates in comparison to the ones in the standard Float-zone Si, preventing full accumulation. On the contrary, minority carrier concentration remains unchanged and still contribute to the formation of charges at the interface when negative bias is applied due to PSC effect. Hence, an increase in loss is observed in the inversion region.

On the other hand, attenuation loss responses for CPWs on Au-compensated HR-Si substrates developed through combined annealing procedures show virtually no dependency on applied bias voltage where a constant attenuation of 0.19 dB/mm is measured throughout the whole region of interest. Apart from the small dependency occurring in the inversion region, CPW attenuations on Au-compensated HR-Si substrates developed through quenching procedure also show no responses towards gate voltage especially in the accumulation region with slightly higher losses measured at all voltages in comparison to the aforementioned Au-compensated HR-Si substrates. The higher values seen in accumulation can be explained by its lower resistivity measured in Section 2.5 of Chapter 2 where a larger concentration of carriers contribute to the losses, whereas the small dependency nature in inversion region indicates that PSC effect is not being fully suppressed by this type of substrates. Nevertheless, the bias-dependent CPW attenuation on these substrates is still very much lower than the ones observed for HiRes Fz-Si and Float-zone Si substrates regardless of annealing procedure used to develop Au-compensated HR-Si substrates. This non-responsive behaviour towards applied bias voltage demonstrates the possibility of PSC suppression at the surface of bulk Au-compensated HR-Si substrates.

The potential of Au-compensated HR-Si substrates developed through combined annealing procedures to suppress PSC effect is further studied through the effect of Au-etching at the Si surface. Figure 5.10 illustrates the responses measured for CPWs on Au-etched

and non Au-etched Au-compensated HR-Si substrates with 20 nm sputtered oxide, where both responses are within 5% of each other and both show less than 1% dependency on voltage. However, it is interesting to see that a slightly higher loss is recorded by Au-etched Au-compensated HR-Si substrates at all measured voltages despite of it having higher resistivity compared to non-etched substrates. Even though an identical trend is observed in both responses which indicate negligible effect of Au-etching on PSC suppression, this observation shows that the existence of Au surface layer might actually help in increasing surface resistivity of Si substrates hence reducing total attenuation loss of the CPWs.

Attenuation responses measured in the presence of light are also included in the figure where increase in attenuation occurred for both cases; with Au-etching or without Au-etching. Absorptions of photons from the light source creates additional electron-hole pairs in Si, hence increasing carrier conduction path and generating more losses inside the substrates. Therefore, measurements are best performed in the dark to prevent these additional generation of carriers and to maintain a high level of measurement accuracy.

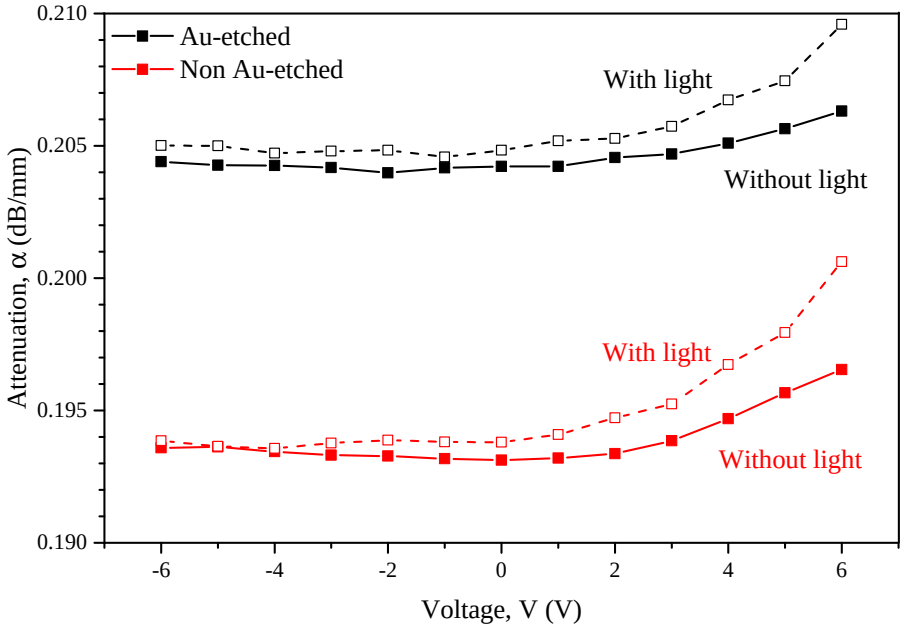


Figure 5.10: Effect of Au-etching and presence of light on CPW attenuation as a function of gate voltage for Au-compensated HR-Si substrates with 20 nm sputtered oxide.

The effect of oxide type on bias-dependent CPW attenuation on Au-compensated HR-Si substrates is demonstrated in Figure 5.11, where thermal oxide and sputtered oxide are being considered. Contrary to the non-responsive nature seen for CPWs on Au-compensated HR-Si substrates with sputtered oxide, it is distinctly shown that a significant bias-dependency response occurred in CPWs on Au-compensated HR-Si substrates

with thermal oxide and the magnitude of dependency is almost similar to the ones measured for structures on Float-zone Si substrates. The increase in attenuation due to thermal oxidation might be caused by the high temperature associated with the oxidation process. The oxidation process at 950 °C can have led to the out diffusion of Au while reducing the temperature after oxidation process at 950 °C at slow, constant rate for a certain time duration increases the chance of thermal donor formations as well as decompensation of substitutional Au atoms in Si. These two factors will contribute to increasing attenuation in accumulation and inversion. On the other hand, oxide deposited through sputtering underwent low-temperature processing environment that preserves the Au-compensation inside bulk Si substrates. Another plausible reason is that there is a difference in interface trap densities introduced in the growth/deposition processes itself, as proposed by Lederer *et al.* [91]. Given that deposited oxide produces higher trap density compared to thermally-grown oxide, more free carriers will be trapped at the interface, increasing the resistivity of the region hence reducing the dependency of losses on applied bias voltage. This explanation is probably only secondary.

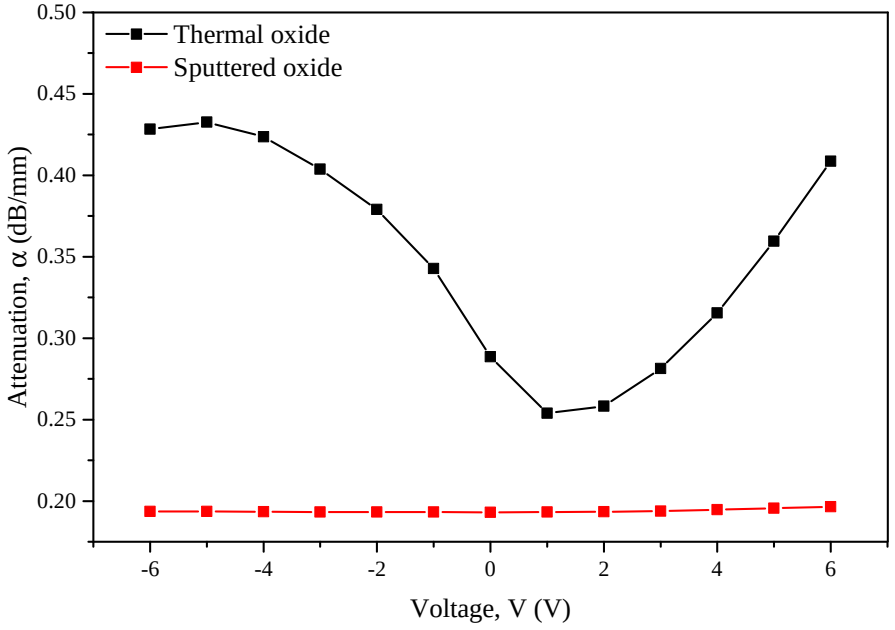


Figure 5.11: Effect of oxide type on CPW attenuation as a function of gate voltage for Au-compensated HR-Si substrates with 20nm oxide.

$\alpha_{max}/\alpha_{min}$ ratio is introduced to quantify the variation in CPW attenuation with respect to applied bias voltage measured at a certain frequency [96]. A ratio of 1 implies no variation in CPW attenuation and the values are said to be bias-independent whereas any values larger than 1 indicate bias-dependent nature of CPW attenuation. Attenuation with bias-independent nature provides a strong indication of PSC suppression since losses due to movement of charges near Si-SiO_2 interface are not detected at any V_g in the measured range.

Substrate	**Annealing**	**Au-etching**	**Oxide**	***α_{meas} (dB/mm)**	$\alpha_{max}/\alpha_{min}$
Fz	-	-	Th	0.34	3
HiRes	-	-	Sp	0.20	1.53
Au-Si	SC+Q	Yes	Sp	0.20	1.01
Au-Si	SC+Q	No	Sp	0.19	1.01
Au-Si	SC+Q	No	Th	0.29	1.70
Au-Si	Q	No	Sp	0.21	1.19

Table 5.1: Summary of results for CPW attenuation on Au-compensated HR-Si substrates with 20nm oxide. SC+Q: slow-cooling+quenching; Q: Quenching; Th: Thermal oxide and Sp: Sputtered oxide. *α_{meas} relates to 0V and 20GHz values. $\alpha_{max}/\alpha_{min}$ is the voltage dependency of the attenuation.

Table 5.1 summarises the attenuation results and the ratios obtained for all Au-compensated HR-Si, Float-zone Si as well as HiRes Fz-Si substrates. From the table, it is clear that CPW attenuations on Float-zone Si and HiRes Fz-Si substrates are strongly bias-dependent. Similar observations are also made for CPWs on Au-compensated HR-Si substrates developed through quenching process and CPWs on Au-compensated HR-Si substrates with thermal oxide. On the other hand, a ratio of 1 is seen for CPWs on Au-compensated HR-Si substrates with sputtered oxide regardless of Au-etching effect, demonstrating bias-independent nature of the structure, together with the lowest actual attenuation. Therefore, it can be said that Au-compensated HR-Si substrates can potentially suppressed PSC effect at the bulk Si surface.

5.5 Effective Resistivity of Au-compensated HR-Si

Previous sections discuss reduced CPW attenuation using Au-compensated HR-Si at 0V for 0.01 - 40 GHz range, and its independency on DC bias, which translates into elimination of both substrate and interface losses of a CPW. The elimination of bias-dependent interface losses indicates the potential of Au atoms to act as trapping charges, preventing the formation of low resistivity region near Si-SiO_2 interface and suppressing the effect of parasitic surface conduction.

However, the losses measured so far have taken into account total attenuation loss of the structure including line conductor loss, whose effect is highly influential on high resistivity substrate at GHz range. To specifically address this PSC issue and to study its potential suppression using Au-compensated HR-Si, a new Figure-of-Merit (FoM) called *effective resistivity* introduced by Lederer *et al.* is used in this work [35], where the level of PSC effect is being quantified.

Effective resistivity, ρ_{eff} forms the basis of a new characterisation method that takes into account all factors affecting the performance of a coplanar structure on a Si substrate, which include, the formation of fixed oxide charges and interface trap charges at Si-SiO_2

interface, the application of DC bias voltage on the substrate, the oxide thickness used as well as device's geometrical dimension on the substrate. The term 'effective' indicates that the inhomogeneous structure (in this case, the inhomogeneous nature is due to the multi-layer stack of SiO_2 and HR-Si with different ϵ_r) will be treated as homogeneous structure with identical microwave losses.

To objectify this parameter, a CPW transmission line model will be used in this analysis, where its equivalent RLGC circuit parameters are defined from complex propagation constant, γ and characteristic impedance, Z_o of the line obtained from S-parameter measurements, as discussed in Section 5.2. The extraction of these parameters are then used to derive a full-length expression of ρ_{eff}, where the characterisation of actual surface resistivity of bulk HR-Si takes place. Consequently the values are analysed to quantify the effect of parasitic surface conduction (PSC) on Au-compensated HR-Si substrates.

Effective resistivity for an inhomogeneous structure as derived by Lederer *et al.* is given by [35]:

$$\rho_{eff} = \frac{1}{\sqrt{\epsilon_{r,eff}}} \left(\frac{\epsilon_{r,eff} - 1}{\epsilon_{r,Si} - 1} \right) \frac{\sqrt{C_o}}{\epsilon_o} \frac{\sqrt{C_{tot}}}{G_{tot}} \tag{5.24}$$

where C_{tot} and G_{tot} are extracted from S-parameter data measured or simulated from inhomogeneous structure.

Equation 5.24 shows that the effective resistivity is strongly dependent on $\epsilon_{r,eff}$ and C_o of the structure. However, since the same geometrical line dimension is used on all analysed substrates and the variation of oxide thickness considered in this work are within the range where $\epsilon_{r,eff}$ remains unchanged, these two parameters will be kept constant throughout the whole analysis in this chapter alongside ϵ_o and $\epsilon_{r,Si}$. Therefore, the only dependency of ρ_{eff} will be coming from measured (or simulated) capacitance and conductance of the inhomogeneous structure.

To clearly demonstrate the relationship between ρ_{eff} and attenuation losses, Equation 5.24 is simplified as derived in Appendix A. The simplified expression is shown below:

$$\rho_{eff} = \frac{\sqrt{2}}{\sqrt{\epsilon_o \epsilon_{r,Si}}} \frac{\epsilon_{r,Si} - 2}{\epsilon_{r,Si} - 1} \frac{\sqrt{50}}{\sqrt{2\pi f}} \frac{\sqrt{\beta}}{\alpha} \tag{5.25}$$

Based on this expression, ρ_{eff} is seen to be linearly dependent on the square-root of phase shift, $\sqrt{\beta}$ and inversely proportional to attenuation, α. To validate this expression, ρ_{eff} for varying substrate resistivity were calculated based on Equation 5.24 and Equation 5.25, where the characteristics are shown in Figure 5.12. The simplified values are within 5%-tolerance, indicating it being a good approximation to the actual ρ_{eff}

expression. Also, the initial claim of ρ_{eff} dependency on α and β (hence, CPW losses) is now verified. SONNET simulation results discussed in the same Appendix A further quantify the dependency of ρ_{eff} on $\sqrt{\beta}$, showing that ρ_{eff} is purely dependent on α. Further simulations on the way to change β in tunable LCR circuits is given in Appendix B.

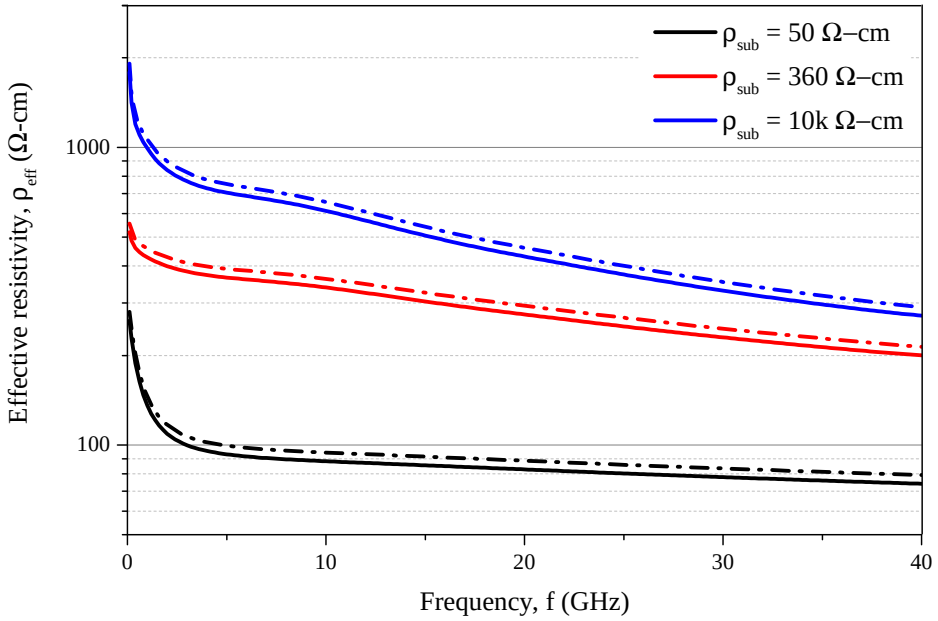


Figure 5.12: Effective resistivity calculated based on full expression in Equation 5.24 (solid lines) and simplified expression in Equation 5.25 (dotted lines) for SONNET-simulated Al-Si CPWs with different ρ_{sub}.

Figure 5.13 illustrates the extraction of effective resistivity measured for Au-compensated HR-Si, HiRes Fz-Si and Float-zone Si substrates at 0V with varying frequency up to 40 GHz. ρ_{eff} for all substrates shows strong dependence on frequency in the lower part of the range (less than 10 GHz) due to the frequency-dependent nature of C and G. At higher frequencies when dielectric relaxation is reached, C dominates the structure and ρ_{eff} stabilises. Figure 5.14 shows the variation of ρ_{eff} with applied gate voltage at 20 GHz, a frequency where ρ_{eff} has sufficiently stabilised. In the figure, ρ_{eff} for Float-zone Si substrates vary significantly with applied V_g with maximum peak of 250 Ω-cm seen at V_g = -2 V. This corresponds to the lowest attenuation recorded in Figure 5.9, where the structure is said to be in depletion state. Also in agreement with the mentioned figure, ρ_{eff} decrease to a greater extend in the accumulation region ($V_g > 0$ V) in comparison to inversion region ($V_g <$ -2 V). For these particular substrates, ρ_{eff} gives a reasonable representation of PSC effect where surface resistivity was reduced by one-third of the originally four-point-probe-measured ρ_{DC} of 360 Ω-cm to $\rho_{eff,max}$ of 250 Ω-cm.

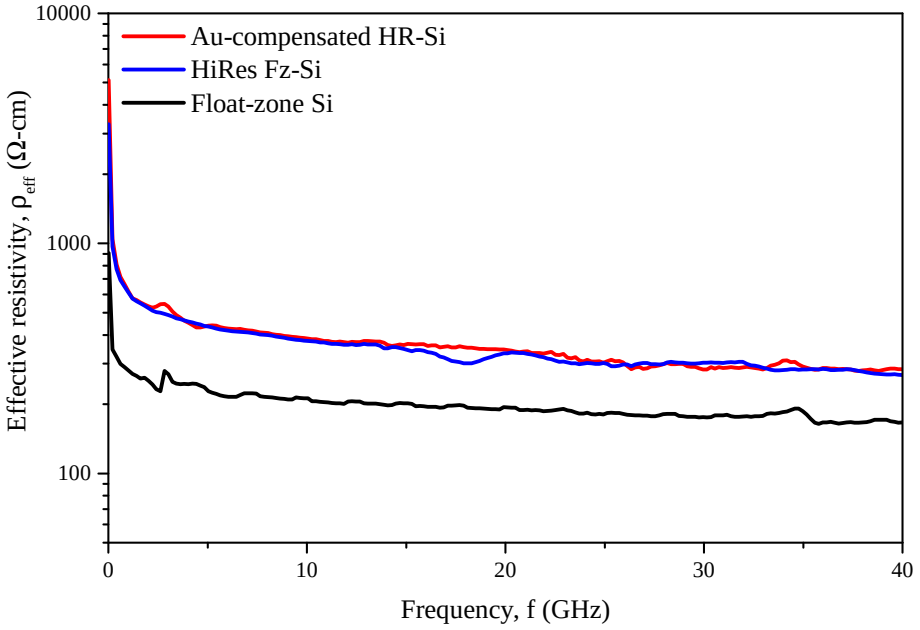


Figure 5.13: Experimental DC effective resistivity, ρ_{eff} of different types of silicon substrates as a function of frequency calculated using Equation 5.24.

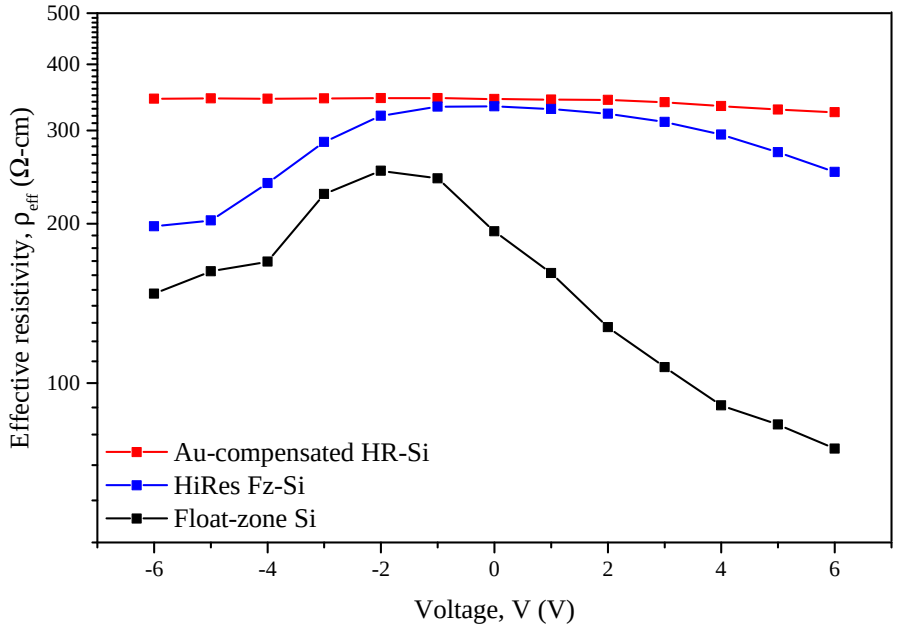


Figure 5.14: Experimental variation of ρ_{eff} of different types of silicon substrates with applied gate voltage, V_g at 20 GHz.

Meanwhile, ρ_{eff} for HiRes Fz-Si substrates show an extreme reduction from ρ_{DC} of nominally 10 kΩ-cm to $\rho_{eff,max}$ of only 330 Ω-cm between -1 V to 1 V, even though the trend corresponds to the reciprocal of bias-dependent attenuation shown in Figure 5.9. Similar observation is made for ρ_{eff} of Au-compensated HR-Si where the values are very much less than the measured ρ_{DC} but with no dependency recorded as portrayed in the same previously mentioned figure. The reason for this discrepancy is related to the high resistivity nature of HiRes Fz-Si and Au-compensated HR-Si substrate and contact probe sensitivity during S-parameter measurement [97]. At very high frequencies, parasitic series resistance becomes comparable to substrate's bulk resistance hence a very sensitive probing method needed to be incorporated to obtain the accurate value of C and G.

Nevertheless, the trends shown by these three substrates provide the rough idea on how PSC regulates the resistivity of bulk Si substrates. When gate voltage is applied, the induced PSC-dependent charges at the Si surface introduce a low resistivity region in between oxide and Si substrates. Depending on the magnitude and polarity of V_g, the existence of low resistivity region at the interface reduces the effective resistivity of Si bulk structure and increases the total microwave losses. With relation to the responses seen in the figure, significant dependency of ρ_{eff} on V_g can be seen for Float-zone Si and HiRes Fz-Si substrates, which are directly translated to substrates' dependency on PSC whereas the flat, stabilised ρ_{eff} values seen for Au-compensated HR-Si substrates indicate the non-responsive nature of Au-compensated HR-Si substrates towards PSC.

5.6 Summary

Microwave characteristics of conductor-backed coplanar waveguides on Au-compensated Hr-Si substrates were measured under DC bias influence to observe potential PSC suppression at microwave frequency range, where the effect is most prominent. Full suppression of PSC-dependent charges is seen for non Au-etched, Au-compensated HR-Si substrates developed through combined annealing procedure with constant attenuation of 0.19 dB/mm is measured throughout the whole voltage range at 20 GHz to give a unity $\alpha_{max}/\alpha_{min}$ ratio. Similar non-dependency nature is not observed for compensated substrates developed through single annealing procedure, with $\alpha_{max}/\alpha_{min}$ value larger than 1 was calculated at the same frequency. Therefore it is shown that the combined annealing procedure provides higher density of traps inside Si substrate in comparison to substrates developed through single quenching procedure. Meanwhile, the effect of Au-etching on suppression of PSC was also observed, in which it demonstrates similar non-dependency nature but with higher attenuation level of 0.21 dB/mm at 20 GHz. Therefore, Au-etching step in fabrication of devices for microwave application can be neglected to improve microwave performance as well as to reduce complexity of fabrication process. In addition to that, oxide type also plays an important role in suppressing

PSC effect on Au-compensated HR-Si substrates. Thermal oxide is seen to be incompatible to be used as oxide passivation layer due to its high processing temperature which has caused abruptions in compensated Au behaviour. As a result, bias-dependent attenuation characteristics for substrates with thermal oxide are shown to be of similar trend to the ones observed in Float-zone Si and have $\alpha_{max}/\alpha_{min}$ ratio as high as the one calculated for HiRes Fz-Si substrates. Meanwhile, the extraction of substrate's effective resistivity show major discrepancy value-wise, however, the trend illustrated on bias-dependent effective resistivity characteristics for Au-compensated HR-Si substrates is in agreement to the previously discussed results, in which a constant value of ρ_{eff} is calculated throughout the whole voltage range, demonstrating suppression effect on PSC using these particular substrates.

Chapter 6

Improving Quality Factor of Meander Inductors

The potential of Au-compensated HR-Si substrates to suppress parasitic surface conduction effect was successfully shown in the previous chapter, where attenuation characteristics of conductor-backed coplanar waveguides were used as the tool to observe and quantify the reduced effect of PSC using high resistivity substrates developed through deep-level doping compensation method. In this chapter, Au-compensated HR-Si substrates will be used as the base substrate for the initial development of 3D-integrated passive components in Si-based MMICs technology. Taken as the most straighforward passive device to be designed and analysed, meander inductors were chosen. It has several advantages in comparison to spiral structures including reduced level of lithography (with only one metal layer required) and reduced amount of mutual inductance due to its uni-directional current. The ability of this structure to provide an accurate representation of material properties especially in the near-surface region becomes the solid basis of using this particular structure in this work, where potential PSC suppression using Au-compensated HR-Si substrate for microwave application is being studied.

Q-factor analysis is used to characterise the performance of meander inductors on oxidised Au-compensated HR-Si substrates, where microwave measurements were conducted for extraction of S-parameter data. To start, this chapter will discuss the theory and extraction of Q factor from S-parameter data. It will be followed by experimental analysis and discussion on the extracted Q-factor parameter.

6.1 Quality factor of a Meander Inductor

Meander inductor is a planar inductor typically used in MMIC technology, as an alternative to the more popular choice of spiral-shaped inductors. Based on the previously mentioned advantages over spiral inductors, this particular device has been used and its corresponding microwave performance was evaluated through a parameter called quality factor, Q. Figure 6.1 shows the schematic diagram of a meander inductor designed and fabricated on Au-compensated HR-Si substrates.

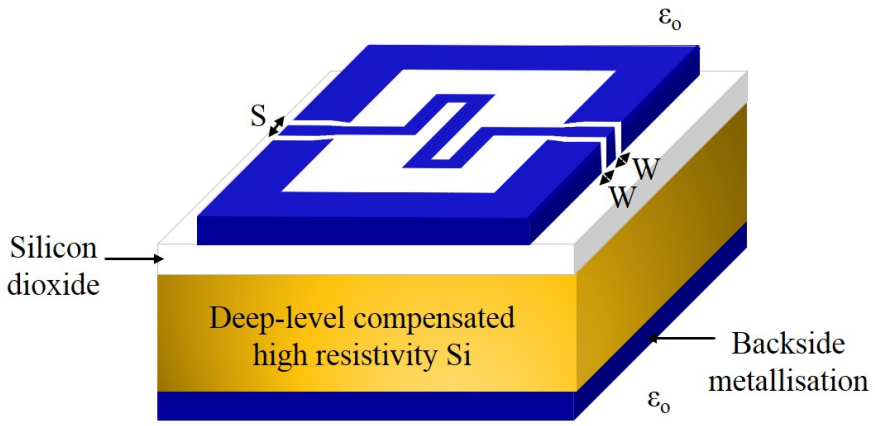


Figure 6.1: 3D schematic diagram of a 1-turn rectangular-shaped meander inductor fabricated on Au-compensated HR-Si substrates with SiO_2 thickness of 20 nm. The corresponding inductance value is 0.7 nH.

Quality factor is a dimensionless ratio that determine the performance of capacitors and inductors, where energy is being predominantly stored. The fundamental relationship between Q and energy is given by:

$$Q = 2\pi \frac{\text{energy stored per unit cycle}}{\text{energy dissipated per unit cycle}} \tag{6.1}$$

By putting inductors into context, Q-factor is defined as the ratio between the inductive part and the resistive part of the inductor, where the energy is being stored and dissipated in the component, respectively. For the device to behave as an inductor, the minimum value has to be at least 1, though the current development on design optimisation and substrates innovation have made it possible to achieve values of Q-factor larger than 15 [98–101]. The expression can also be translated into the ratio of meander's imaginary impedance to real impedance [102], which gives:

$$Q = \frac{X_L}{R} = \frac{|\mathrm{Im}\,[Z]|}{\mathrm{Re}\,[Z]} \tag{6.2}$$

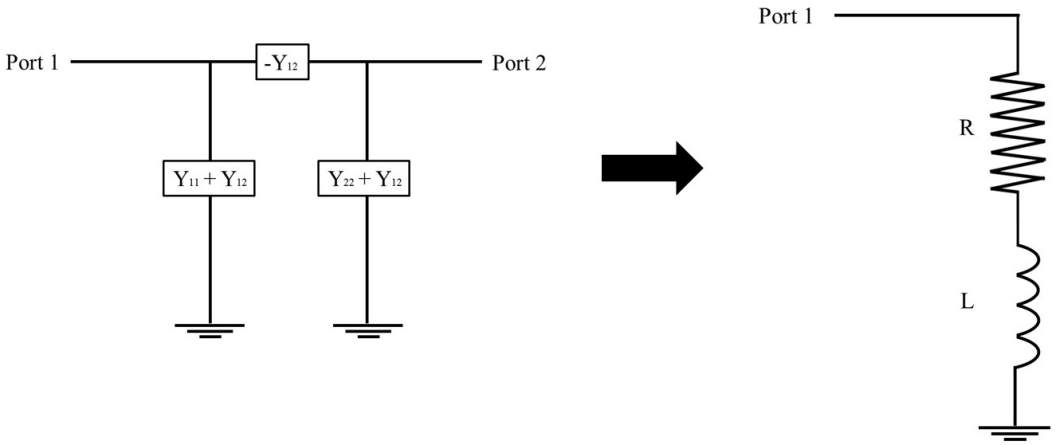


Figure 6.2: π-equivalent circuit for a passive reciprocal two-port network is reduced to a single-ended configuration to calculate Q-factor of a meander inductor [103]. In this configuration, port 2 is grounded and the circuit consists of the parallel connection of $-Y_{12}//(Y_{11}+Y_{12})$. Since the components of Y_{12} cancel out each other, the circuit only sees Y_{11} connected to ground.

where X_L is the inductive reactance, R is the resistance and Z is the total impedance given by:

$$Z = R + jX_L \tag{6.3}$$

Equation 6.2 is derived from the reduced π-equivalent circuit for a passive reciprocal two-port network [103]. For a single-ended reduced π-equivalent circuit configuration as depicted in Figure 6.2,

$$Z = R + jX_L = \frac{1}{Y_{11}} \tag{6.4}$$

Putting in Equation 6.4 into Equation 6.2 gives [104]:

$$Q = \frac{|\mathrm{Im}\,[1/Y_{11}]|}{\mathrm{Re}\,[1/Y_{11}]} \tag{6.5}$$

In this work, Q-factors are analysed through two-port S-parameter measurement data. Y_{11} can be directly calculated from S-parameter using the following expression [105]:

$$Y_{11} = \frac{[(1 - S_{11})(1 + S_{22}) + (S_{12}S_{21})]}{[(1 + S_{11})(1 + S_{22}) - (S_{12}S_{21})]} \tag{6.6}$$

6.2 S-parameter Measurement Setup & Results

To calculate Q-factor of meander inductor and consequently evaluate its performance on Au-compensated HR-Si substrates, S-parameter measurements were conducted on all fabricated structures mentioned in Section 3.3 of Chapter 3 using Agilent Technologies E8691A Vector Network Analyser (VNA). The calibration setup for this measurement was the same as the one required for CPW attenuation loss measurement (refer Section 5.3 in Chapter 5). After calibration, S-parameter responses for all fabricated meander inductors were measured over a frequency range of 0.01 - 40 GHz.

Return loss for meander inductors fabricated on Au-compensated HR-Si and Float-zone Si substrates are shown in Figure 6.3 to Figure 6.7. The recorded values are in good agreement with SONNET simulation for all inductance values and structures. These observations confirm that at least 30% of power is being reflected back to the port by the devices, regardless of the shape of meander turns or tapering options used. It shows that high level of impedance-mismatching still occurs and further optimisation needs to be done on the design to improve this.

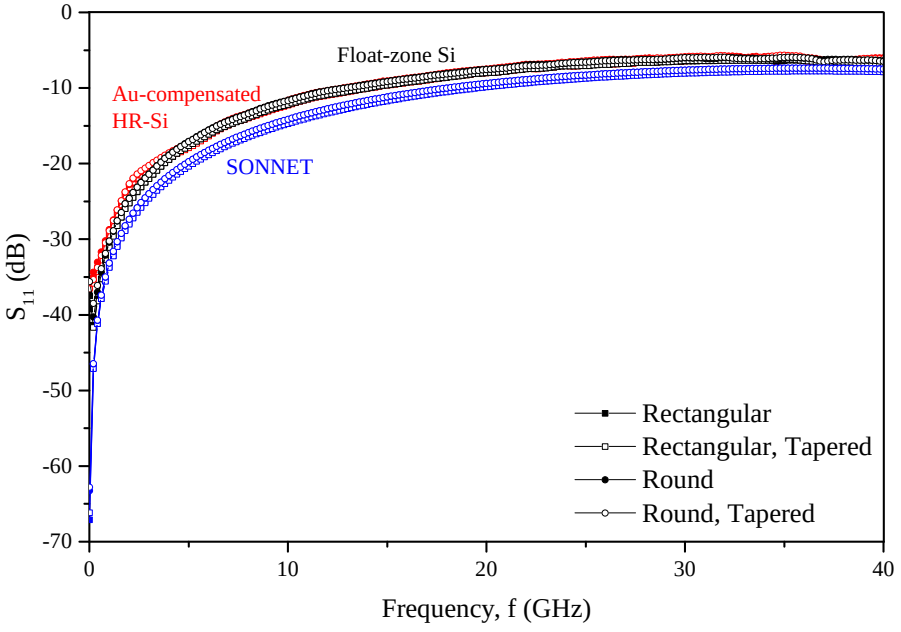


Figure 6.3: SONNET-simulated and measured return loss of 0.7 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates. Curves reflecting different shapes of the inductor result in near identical curves and are not individually visible.

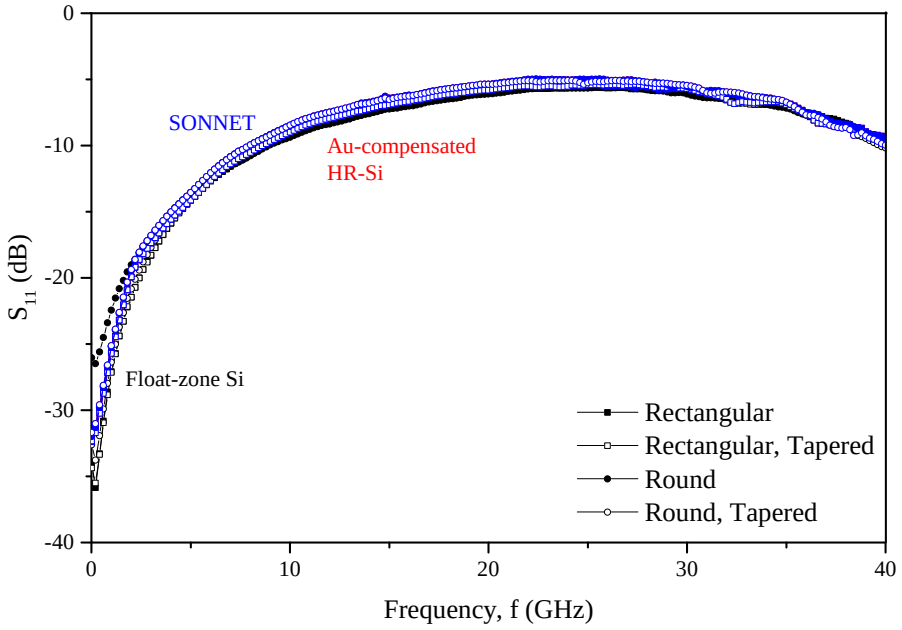


Figure 6.4: SONNET-simulated and measured return loss of 1.25 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates. Curves reflecting different shapes of the inductor result in near identical curves and are not individually visible.

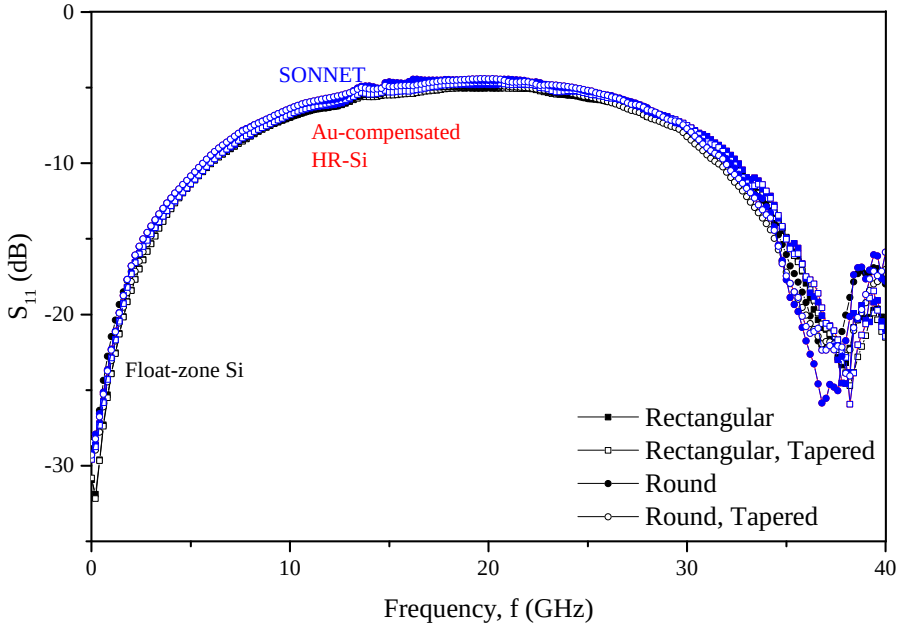


Figure 6.5: SONNET-simulated and measured return loss of 1.61 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates. Curves reflecting different shapes of the inductor result in near identical curves and are not individually visible.

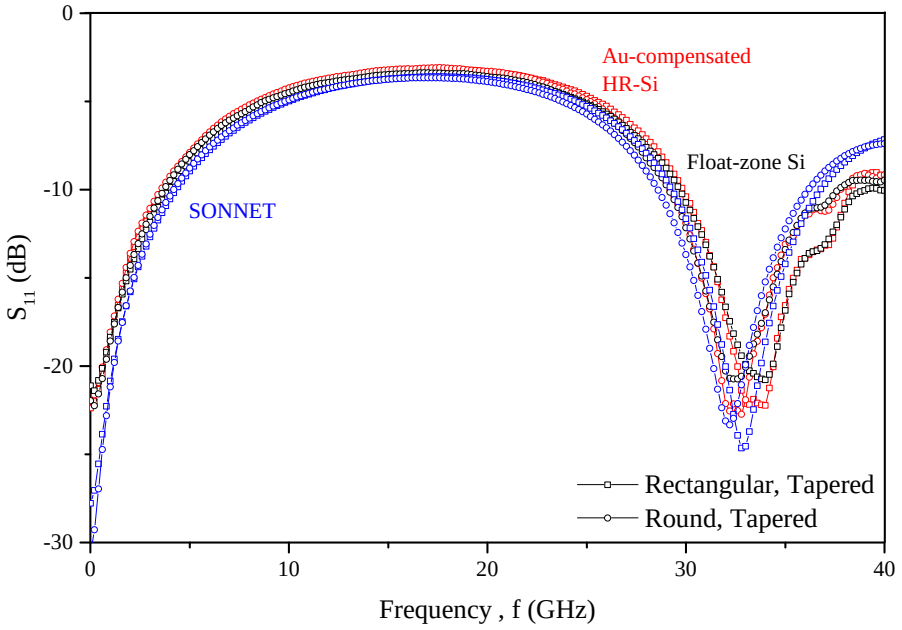


Figure 6.6: SONNET-simulated and measured return loss of 2.08 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates. Curves reflecting different shapes of the inductor result in near identical curves and are not individually visible.

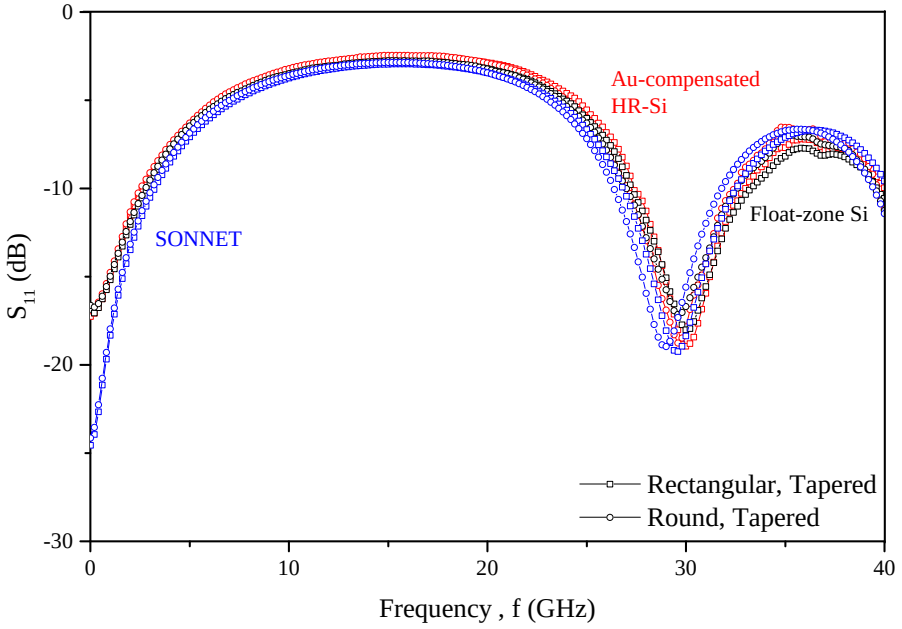


Figure 6.7: SONNET-simulated and measured return loss of 2.44 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates. Curves reflecting different shapes of the inductor result in near identical curves and are not individually visible.

Figure 6.8 to Figure 6.12 show the insertion loss response of the devices. Increasing the inductance values causes an increase in insertion loss. The reason for this is that an increase in length with increasing number of turns will cause more losses during signal transmission, similar to CPWs.

Compared to SONNET, experimental responses for devices on both Au-compensated HR-Si and Float-zone Si substrates show higher losses, most probably due to parasitic components which are not considered in SONNET. However, devices on Au-compensated HR-Si substrates are seen to have lower insertion loss in comparison to the ones on Float-zone Si substrates. This could be due to higher substrate resistivity provided by Au-compensated HR-Si. It is also interesting to note that meander inductors with round turns have higher insertion loss than devices with rectangular turns for all measured inductance values, in both experimental and simulated responses. This can be explained again by the difference in paths length which in turns affects the resistive part of meander inductors. Round turns have longer paths therefore contributing to higher insertion loss compared to rectangular turns. In terms of tapering options, the losses are seen to be comparable to the non-tapered ones, indicating the negligible effect of adding the tapered line at CPW-to-meander transition.

For Q-factor analysis in the next section, the focus will be narrowed down to meander inductors with rectangular turns and tapered transition since this particular design provide the lowest insertion loss and accommodate the only available fabricated design for higher inductance values, i.e. the 2.08 nH and 2.44 nH inductors.

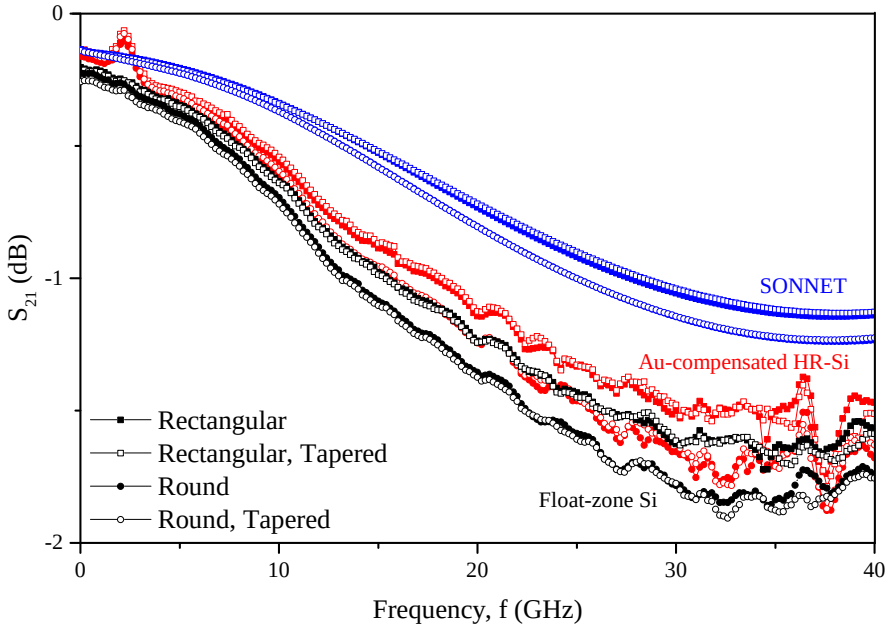


Figure 6.8: SONNET-simulated and measured insertion loss of 0.7 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

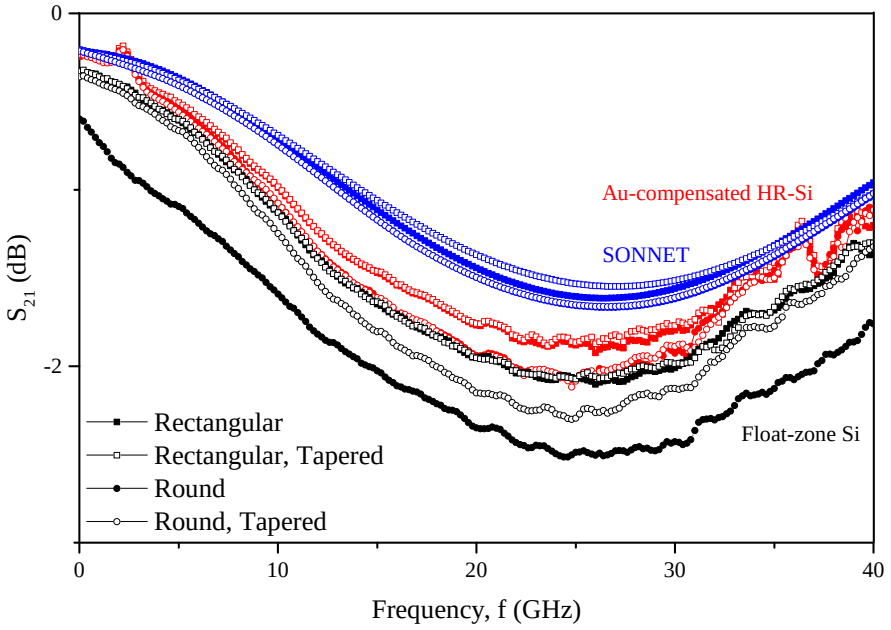


Figure 6.9: SONNET-simulated and measured insertion loss of 1.25 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

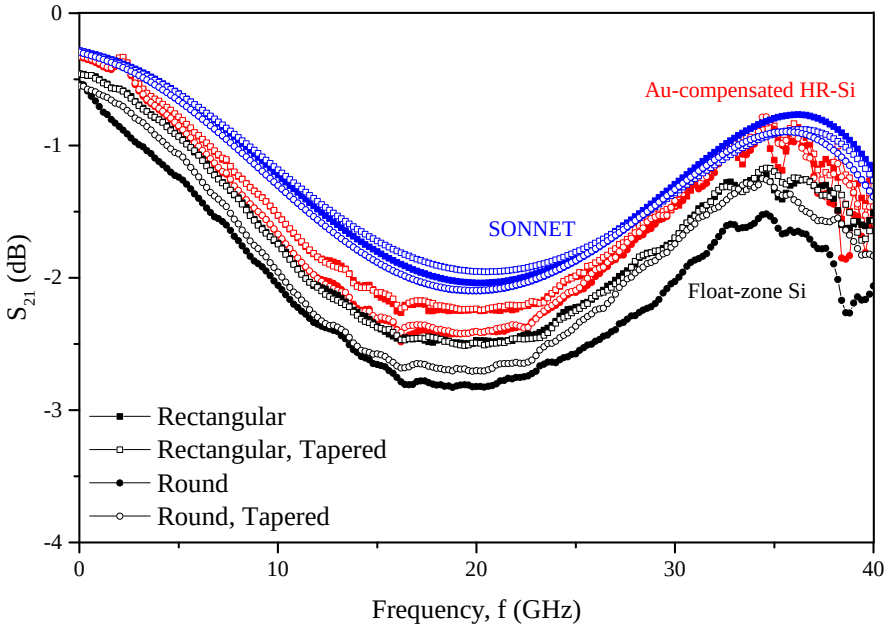


Figure 6.10: SONNET-simulated and measured insertion loss of 1.61 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

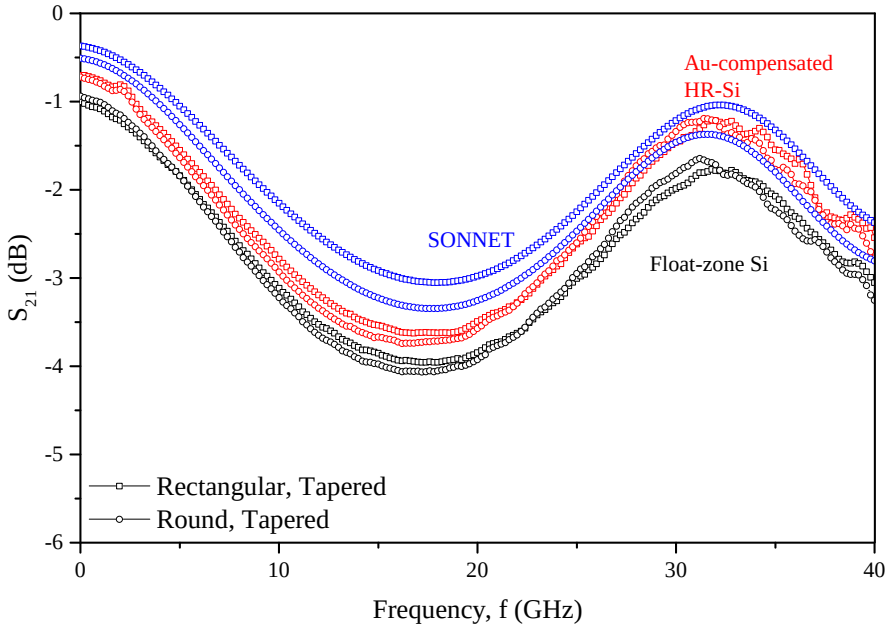


Figure 6.11: SONNET-simulated and measured insertion loss of 2.08 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

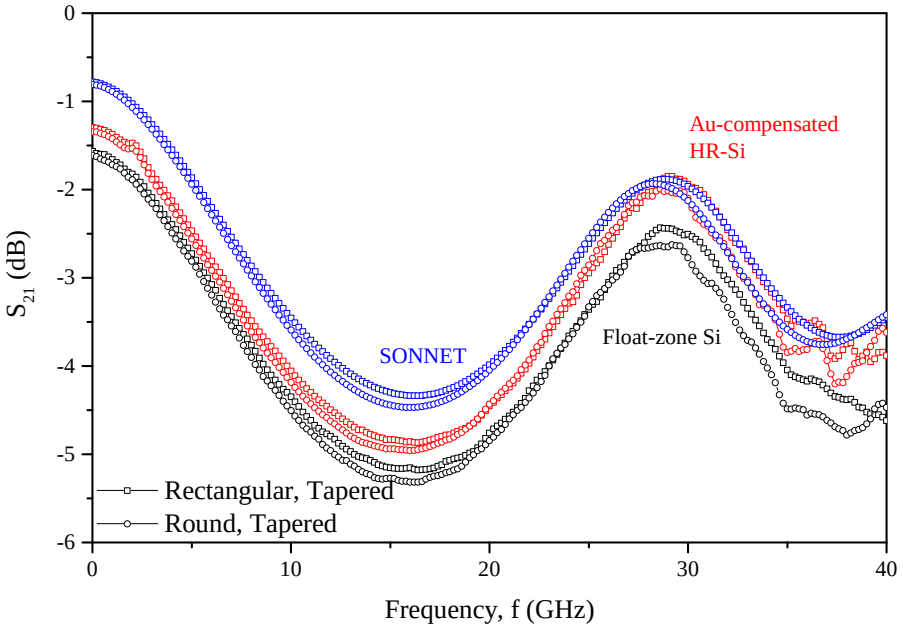


Figure 6.12: SONNET-simulated and measured insertion loss of 2.44 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

6.3 Quality factor of Meander Inductor on Au-Si substrate

Quality factor Q of a meander inductor was determined using Equation 6.5. As mentioned previously, Q-factor analysis in this work will only focus on tapered-line meander structure with rectangular turns. The results are shown in Figure 6.13 to Figure 6.17.

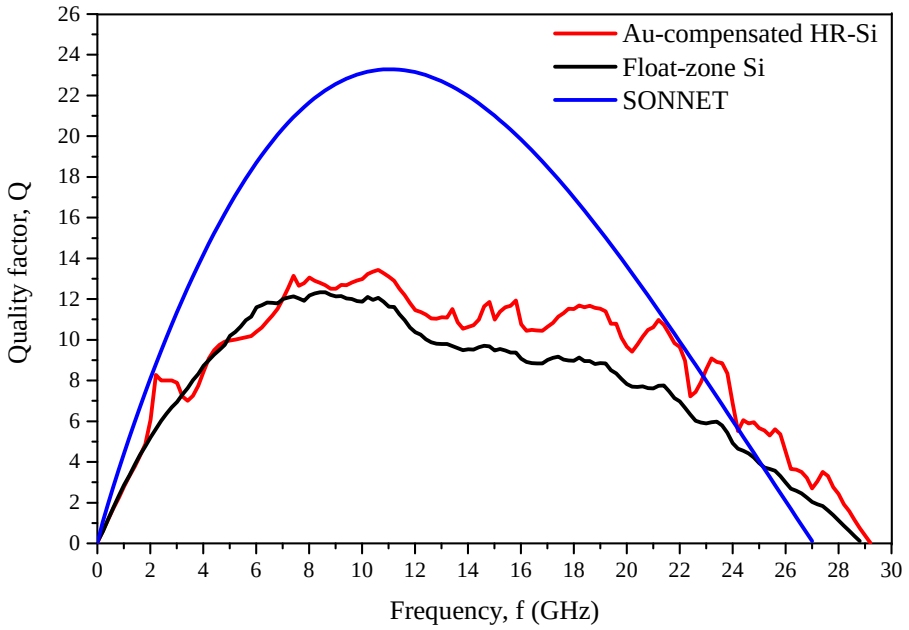


Figure 6.13: Measured Q-factor of 0.7 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

All responses show decreasing maximum Q-factor Q_{max} with increasing inductance value, and the experimental results are consistent with the simulations. The lower values seen in experimental Q_{max}, however, can be explained by the parasitic components which are not considered in SONNET, as explained in the insertion loss responses. Q-factor for devices on Au-compensated HR-Si substrates are seen to be higher than the ones measured on Float-zone Si substrates at all measured inductance values with the highest Q being 14, for the 0.7 nH meander inductors. This difference between HR-Si substrates and Float-zone Si substrates is caused by the previously discussed insertion loss where losses measured for devices on Au-compensated HR-Si substrates are lower than Float-zone Si due to the substrates having higher resistivity than the latter. Based on these results, it can be concluded that the use of Au-compensated HR-Si substrates as microwave base substrates is shown to be effective for meander inductor's application due to its higher level of performances compared to Float-Zone Si. The consistency achieved by experimental losses in comparison to simulated losses provides confirmation that the fabrication of these inductors met design expectation.

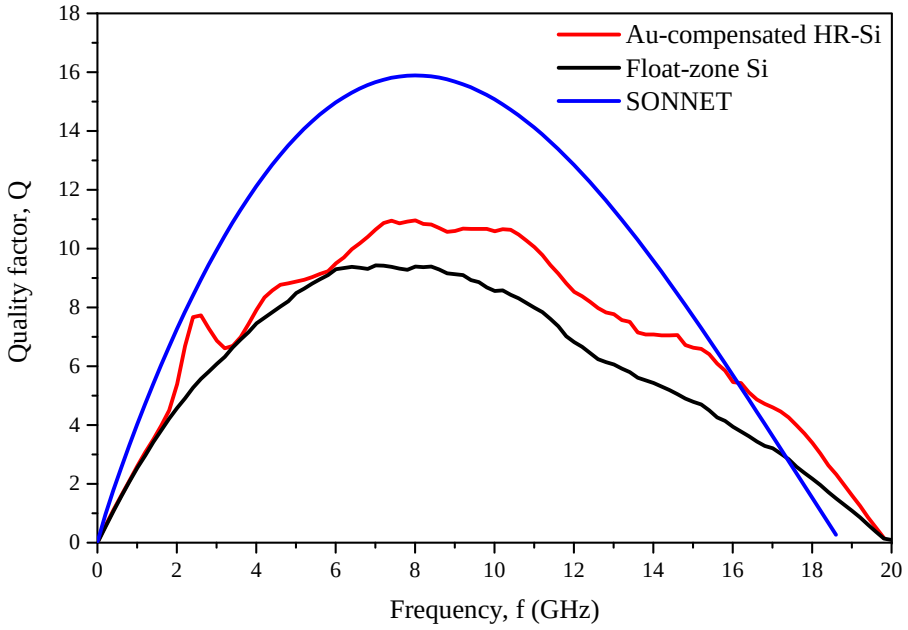


Figure 6.14: Measured Q-factor of 1.25 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

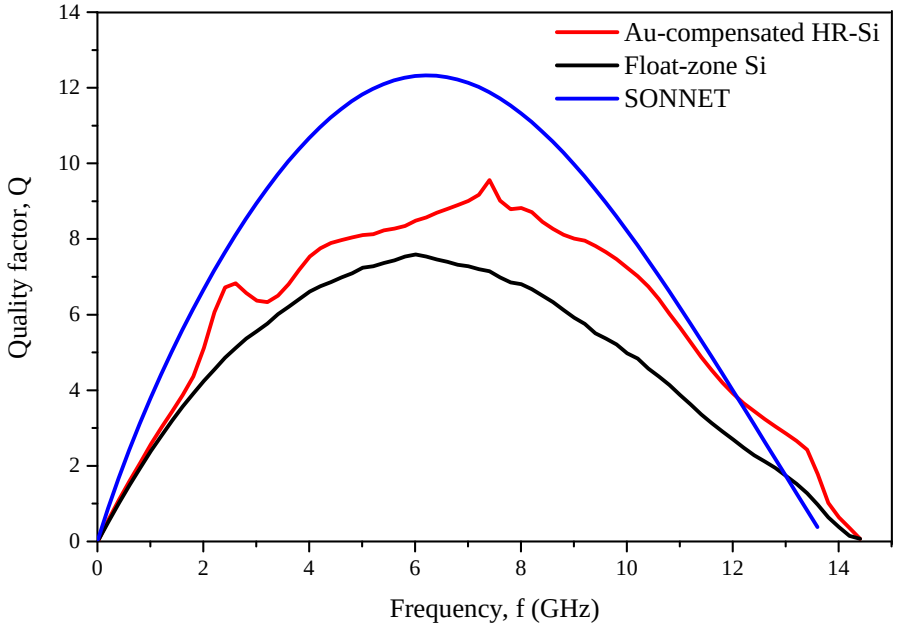


Figure 6.15: Measured Q-factor of 1.61 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

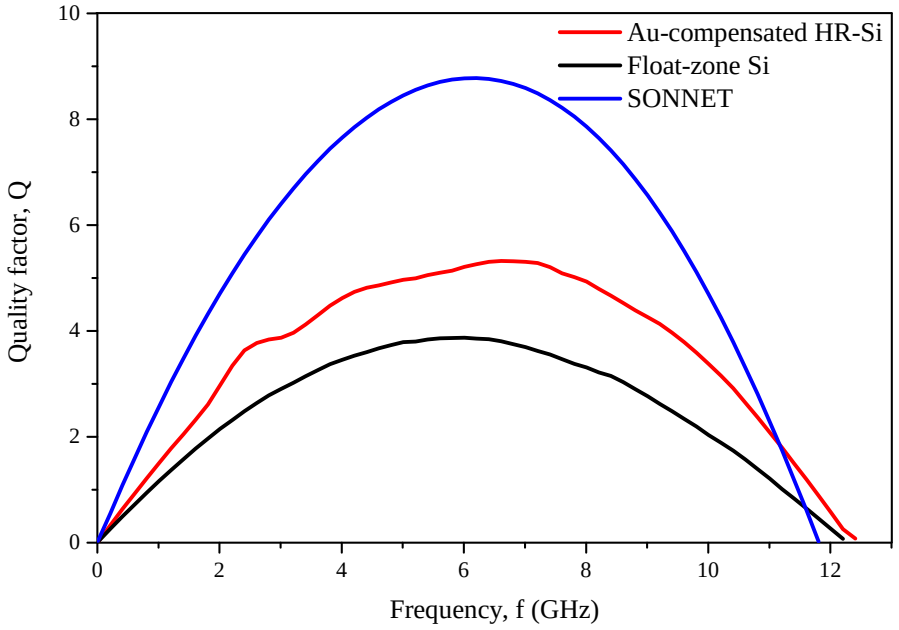


Figure 6.16: Measured Q-factor of 2.08 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

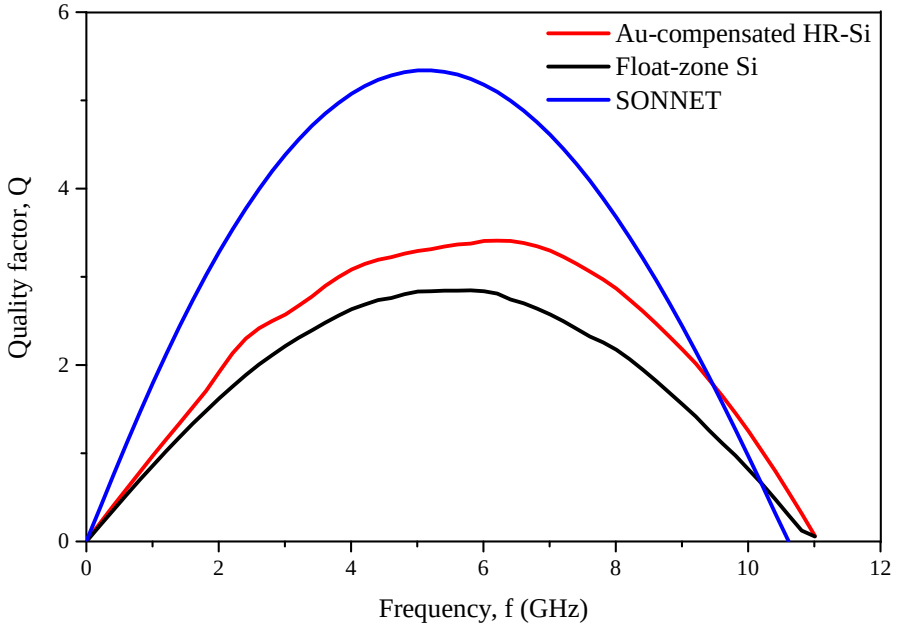


Figure 6.17: Measured Q-factor of 2.44 nH meander inductors on Float-zone Si and Au-compensated HR-Si substrates.

6.4 Summary

Q-factor performances of meander inductors fabricated on Au-compensated HR-Si substrates were measured and analysed to observe the substrate's potential to serve as microwave substrate for the purpose of integration of passive devices. Based on the results, it is shown that Q-factor values of devices on the Au-compensated HR-Si substrates are higher than devices fabricated on the Float-zone Si substrates for all inductance values, with the highest value of $Q = 14$ for the 0.7 nH inductor.

Return loss and insertion loss responses also show that rounded-turn meander inductors produce higher losses in comparison to rectangular-turn due to increase in current paths length. In addition, tapering option has negligible effect on signal tranmission level since the losses recorded for tapered-line meander inductors are seen to be comparable to non-tapered line meander inductors.

Chapter 7

Summary & Outlook

7.1 Summary

High resistivity substrates are desirable in microwave application to provide low loss performance. In order to create high resistivity substrates, low concentration level of background free carriers needs to be achieved. In this thesis, a high resistivity substrate is developed through a concept called deep-level doping compensation, where background free carriers in Si are compensated by elemental Au.

The concept consists of Au atoms compensating for the carriers by providing deep levels near Si mid band gap and trapping them from freely conducting in the conduction band. For optimum compensation, Au atoms are introduced into Si using ion-implantation technique and activated via high temperature annealing procedure. The diffusion process occurs through 'kick-out' mechanism, by which a Au atom kicks out Si atom from its lattice configuration and occupies the substitutional position inside Si lattice. For optimum compensation, Au atoms are introduced into Si using ion-implantation technique and activated via high temperature annealing procedure. In this work, a gold dose of 4 x 10^{13} cm^{-2} were injected through the backside of Czochralski-silicon substrates with nominal resistivity of 50 Ω-cm. The implanted substrates were then annealed at 950 °C in an Argon environment to activate the Au dopants. As a result, the substrate resistivity was successfully enhanced to as high as 80 kΩ-cm, with an average value of 60 kΩ-cm for optimised implanted substrates.

Upon application at high frequency range, high resistivity silicon substrates suffer from parasitic surface conduction, an effect that is bias-dependent, and occurs primarily due to carriers near the Si surface during accumulation and inversion. The accumulation and inversion of charges at the silicon surface creates a low resistivity surface region which consequently increases substrate losses. This defeats the purpose of creating high resistivity Si in the first place.

To address this issue, Au-compensated high resistivity silicon substrates developed in this work are studied for its potential suppression of parasitic surface conduction using deep-level doping compensation method. Metal-oxide-semiconductor (MOS) capacitors are fabricated on Au-compensated HR-Si substrates to study the surface charge effect associated with high resistivity substrates at the Si-SiO_2 interface. Capacitance-voltage characteristics of the devices show non-typical high frequency behaviour, with accumulation capacitance significantly less than the oxide capacitance. The smaller accumulation capacitance seen in the measurements is caused by the reduction of majority free carriers and the correspondingly longer Debye length in high resistivity substrates. Comparing the experimental results with the simulation results, capacitance obtained from experiments are observed to be lower in all regions, indicating the potential of the substrate to suppress the surface charge effect.

Microwave characterisations were used as a tool to evaluate the parasitic surface conduction effect on high resistivity silicon substrates under DC bias influence. Coplanar waveguides were fabricated to observe the attenuation characteristics of the devices on Au-compensated high resistivity silicon substrates. Under zero bias condition, the measured attenuations of CPWs on oxidised substrates are comparable to the attenuations of CPWs on naked substrates, and are very much lower than the ones on oxidised Float-zone Si substrates. These observations show the initial potential of parasitic surface conduction suppression, with a recorded low attenuation of 0.19 dB/mm at 20 GHz. Full suppression of the effect is successfully observed through microwave characterisations under DC bias influence. Unlike the bias-dependent attenuation values seen for CPWs on 360 Ω-cm and 10 kΩ-cm Float-zone Si substrates, a constant attenuation value of 0.19 dB/mm at 20 GHz is achieved throughout the whole range of bias voltage for CPWs on Au-compensated high resistivity silicon substrates.

To reach this successful result, several process innovations have been designed and achieved. One of the key innovations is the optimisation of the activation annealing procedure. Three different annealing treatment conditions were introduced; slow-cooling, quenching and the combined procedure of slow-cooling and quenching. Slow-cooling alone leads to very limited compensation. The highest resistivity enhancement is achieved for substrates developed through the combined procedure. In terms of microwave device characteristics, CPWs fabricated on substrates developed through the combined procedure show full suppression of parasitic surface conduction with measured $\alpha_{max}/\alpha_{min}$ ratio of 1 whereas CPWs fabricated on substrates developed through the single quenching procedure show a slight attenuation-dependency with $\alpha_{max}/\alpha_{min}$ ratio of 1.19. Based on these observations, the activation annealing is best conducted through the combined procedure of slow-cooling and quenching to provide optimum resistivity enhancement and low loss microwave characteristics.

Another essential point is the significance of the Au surface layer. Removing this Au layer at the silicon surface by wet-etching helps to increase substrate resistivity. The

resistivity is increased to almost double the values before Au-etching. However, from a microwave point of view, full suppression of parasitic surface conduction is seen in both cases, with and without Au-etching. Actually, the attenuation losses of CPWs fabricated on substrates without Au layer removal are lower than the ones on substrates with Au layer removal, indicating that the existence of a Au layer at the silicon surface provides additional benefits. Therefore, the Au surface removal through wet-etching is not required to improve microwave performance, leading to reduced complexity in the fabrication process.

The type of oxide used as the passivation layer also has an important role in suppressing parasitic surface conduction using Au-compensated high resistivity silicon substrate. The effect is fully suppressed on substrates with sputtered oxide with $\alpha_{max}/\alpha_{min}$ ratio of 1, whereas a strong bias-dependent attenuation characteristic is seen on substrates with thermal oxide, with a recorded $\alpha_{max}/\alpha_{min}$ ratio of 1.70. The increase in attenuation and its bias-dependent characteristics for the latter oxide are contributed to the high processing temperature during oxidation, which lowers the substitutional Au concentration.

Having presented the points above, suppression of parasitic surface conduction in bulk high resistivity silicon can be achieved via deep-level doping compensation technique. The highest level of microwave performance is observed for non Au-etched, Au-compensated high resistivity silicon substrate developed through the combined annealing procedure of slow-cooling and quenching with sputtered oxide. The best value is 0.19 dB/mm at 20 GHz and is constant throughout the whole range of voltage measured, indicating full suppression of the effect. Microwave performance of meander inductors fabricated on these Au-compensated high resistivity silicon substrates were evaluated to further indicate the potential of the substrate. The quality factor of these inductors are higher than those fabricated on Float-zone silicon substrates. The best value of Q-factor is 14, for a 0.7-nH inductor.

In conclusion, increased performance of microwave devices fabricated on Au-compensated high resistivity silicon provides a clear demonstration of the effectiveness of the deep-level doping compensation method in providing an alternative to the currently available microwave substrates, offering reduced fabrication complexity and lower manufacturing cost.

7.2 Outlook

Based on the current achievements reported for deep level doping compensation, a number of recommendations have been made to increase the practicality of Au-compensated high resistivity silicon as a microwave substrate.

First and foremost, there is a need to address the thermal budget issues arisen from wafer-processing and fabrication stages. The high-temperature treatment incorporated during annealing and thermal oxidation procedures have greatly influenced the behaviour of Au atoms in silicon. For example, in annealing, the difference in cooling rate causes the wafer resistivity to vary from one another, giving a direct, qualitative indication of Au-compensation process level in silicon. Similar observation is made with thermal oxidation, only that the effect is later seen in microwave characterisation, where the parasitic surface conduction is still visible for high resistivity substrate with thermal oxidation, unlike the substrates with sputtered oxide. In order to tackle this problem, a quantitative approach is required in order to fully understand the behaviour of Au atoms in silicon and its consequent compensation process.

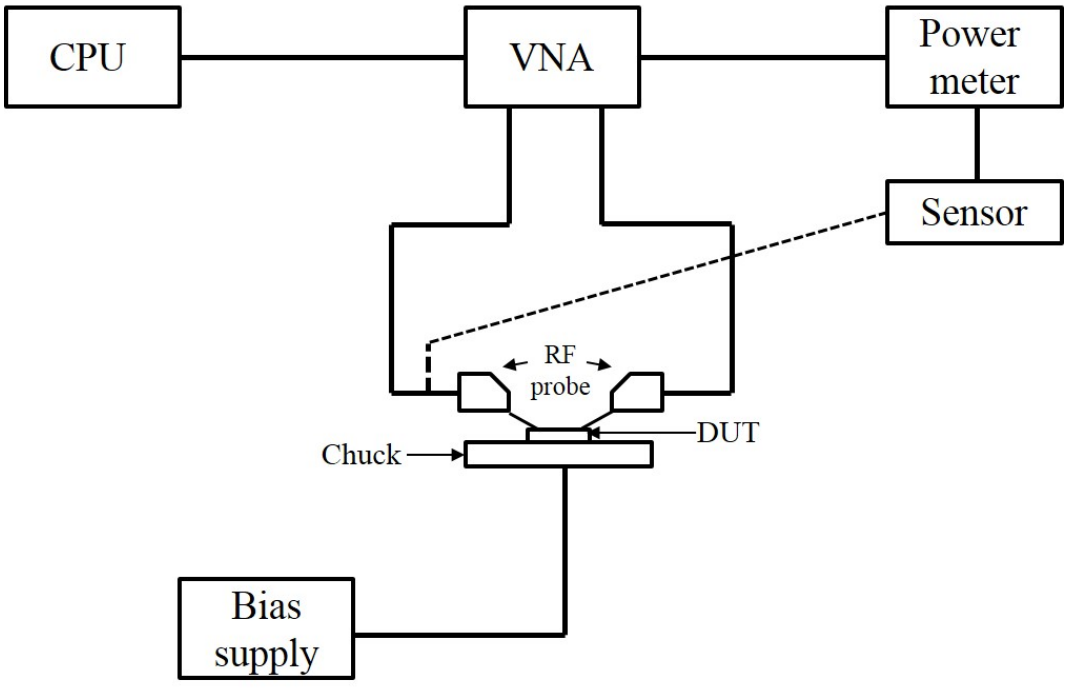


Figure 7.1: Proposed power sweep measurement setup for harmonic distortion back-contact measurement on transmission lines fabricated on Au-compensated high resistivity silicon.

Apart from the increase in microwave losses, parasitic surface conduction in bulk high resistivity silicon substrate also affects the linearity of passive devices in wireless system and data communication network. Non-linear harmonic distortions originated from parasitic surface conduction in bulk silicon substrates has been discussed in [106–108],

where its occurrence is said to be detrimental to the system, if the power level is higher than the ones in other microwave circuitries and active components. It is therefore important to observe this non-linear behaviour in Au-compensated high resistivity silicon to ensure full suppression of parasitic surface conduction is by all means, achieved. Kerr *et al.* proposed the power sweep measurement setup used to measure second and third harmonic distortion level of transmission line fabricated on passivated bulk high resistivity silicon [109]. However, the setup can be altered to employ the back metallisation of the microwave structure in this work. The proposed setup for measurement using back contact is as shown in Figure 7.1.

The proposed work can then be utilised to form the solid basis of fully incorporating this substrate into microwave applications such as integrated passive devices and through-silicon-vias for 3D-integration.

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Appendix A: Extraction of Effective Resistivity using CPW Transmission Line

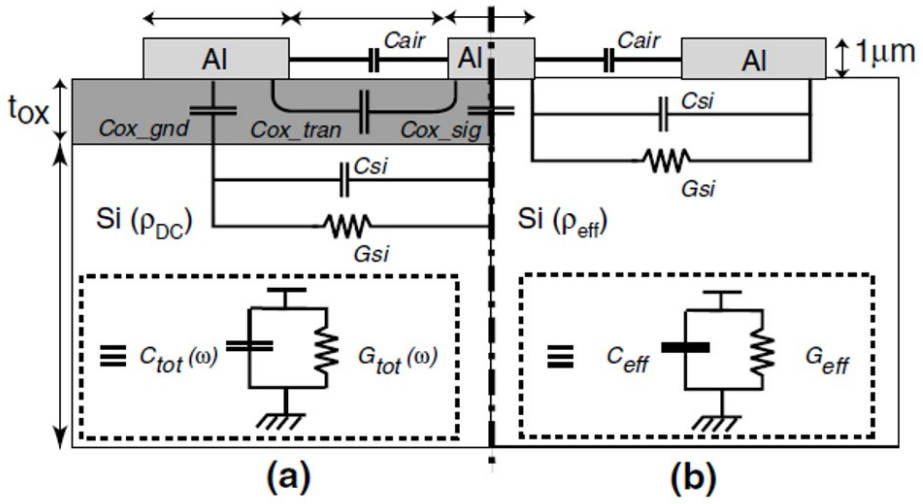

Figure 7.2: Cross-section of CPW on (a) an inhomogeneous Si substrate and (b) a homogeneous substrate for effective resistivity modelling [35].

Figure 7.2 illustrates the cross-sectional structure of CPW on inhomogeneous and homogeneous Si substrates analysed in this work. SiO_2 with $\epsilon_r = 3.9$ is used as passivation layer on the inhomogeneous structure with metal thickness of 1μm and CPW line dimension as mentioned in the figure. Backside metallisation is not considered in this analysis, and based on previous chapter, it is permissible to do so for a thick Si substrate. Equivalent circuit elements are modelled for both structures and are simplified as shown in the insets, where their microwave losses are considered to be the same. For low-loss CPW transmission line (i.e. R<<ωL and G<<ωC), α in Equation 5.13 can now be reduced to:

$$\alpha = \frac{R}{2}\sqrt{\frac{C}{L}} + \frac{G}{2}\sqrt{\frac{L}{C}} \tag{7.1}$$

Assuming R to be the same for both cases (same Al metal line hence same conductor loss, α_C), the expression can be further approximated below to give substrate loss of:

$$\alpha_{inh} \approx \frac{G_{tot}}{2}\sqrt{\frac{L}{C_{tot}}}; \qquad \alpha_{eff} \approx \frac{G_{eff}}{2}\sqrt{\frac{L}{C_{eff}}} \tag{7.2}$$

for inhomogeneous CPW structure and effective structure, where only substrate losses are considered and L is identical (due to same geometrical CPW dimension used). Since substrate losses are also assumed to be the same, the relationship between inhomogeneous and effective structure is found to be:

$$G_{eff} = G_{tot}\sqrt{\frac{C_{eff}}{C_{tot}}} \tag{7.3}$$

Effective capacitance, C_{eff} can be expressed in terms of air-filled capacitance, C_o using [110]:

$$\epsilon_{r,eff} = \frac{C_{eff}}{C_o} \tag{7.4}$$

where ϵ_{eff} is the effective relative permittivity and can be written down in terms of $\epsilon_{r,Si}$ and filling factor, q:

$$\epsilon_{r,eff} = 1 + q(\epsilon_{r,Si} - 1) \tag{7.5}$$

Meanwhile, the expression for effective conductance, G_{eff} is as follows:

$$G_{eff} = q\frac{C_o}{\epsilon_o \rho_{eff}} \tag{7.6}$$

where ρ_{eff} represents the effective resistivity of the structure.

Based on the expressions shown in Equation 7.3 to Equation 7.6, the equivalent effective resistivity for an inhomogeneous structure is derived as:

$$\rho_{eff} = \frac{1}{\sqrt{\epsilon_{r,eff}}}\left(\frac{\epsilon_{r,eff} - 1}{\epsilon_{r,Si} - 1}\right)\frac{\sqrt{C_o}}{\epsilon_o}\frac{\sqrt{C_{tot}}}{G_{tot}} \tag{7.7}$$

where C_{tot} and G_{tot} are extracted from S-parameter data measured or simulated from inhomogeneous structure.

Equation 7.7 shows that effective resistivity is strongly dependent on $\epsilon_{r,eff}$ and C_o of the structure. However, since the same geometrical line dimension is used on all analysed substrates and the variation of oxide thickness considered in this work are within the range where $\epsilon_{r,eff}$ remains unchanged, then these two parameters will be kept constant throughout the whole analysis in this chapter alongside ϵ_o and $\epsilon_{r,Si}$. Therefore, the only dependency of ρ_{eff} will be coming from measured (or simulated) capacitance and conductance of the inhomogeneous structure. Revisiting previous section where C and G are derived from γ and Z_c, and that $\alpha_{c,inh}$ and $\alpha_{c,eff}$ are the same, ρ_{eff} can then be said to be purely dependent on the losses contributed by PSC effect.

To demonstrate the relationship between ρ_{eff} and CPW losses, Equation 7.7 is simplified with a number of considerations made. First of all, by only considering an infinitely thick Si substrate and ignoring backside metallisation, the structure can be treated as a direct Al-Si CPW with effective relative permittivity [110]:

$$\epsilon_{r,eff} \approx \frac{\epsilon_{r,Si}}{2} \tag{7.8}$$

and the corresponding C_o for the case of $S_{CPW} >> W_{CPW}$ is:

$$C_o = 4\,\epsilon_o \frac{K(k_o)}{K(k_o')} \approx 4\,\epsilon_o \tag{7.9}$$

Since $\gamma = \alpha + j\beta$ and Z_c is assumed to be 50Ω, expressions for G_{tot} and C_{tot} shown in Equation 5.17 and Equation 5.18 respectively can be further broken down into:

$$G = Re\left(\frac{\gamma}{Z_c}\right) = \frac{\alpha}{50} \tag{7.10}$$

$$C = Im\frac{\left(\frac{\gamma}{Z_c}\right)}{2\pi f} = \frac{\beta}{100\pi f} \tag{7.11}$$

Substituting Equation 7.10 and Equation 7.11 into Equation 7.7 gives:

$$\rho_{eff} = \frac{\sqrt{2}}{\sqrt{\epsilon_o \epsilon_{r,Si}}} \frac{\epsilon_{r,Si} - 2}{\epsilon_{r,Si} - 1} \frac{\sqrt{50}}{\sqrt{2\pi f}} \frac{\sqrt{\beta}}{\alpha} \tag{7.12}$$

where ρ_{eff} is seen to be linearly dependent on $\sqrt{\beta}$ and inversely proportional to α and $\sqrt{f}$.

SONNET simulation was performed on an oxide-free Al-Si CPW structure to verify the connection between ρ_{eff} and CPW losses (α and β). Geometrical CPW dimension as explained in Figure 3.5 in Chapter 5 was used in this simulation work, with SiO_2 layer

removed. ρ_{sub} was varied between 50 Ω-cm (low-resistivity substrate) and 10k Ω-cm (high-resistivity substrate) and the corresponding α and β were analysed and shown in the graphs below.

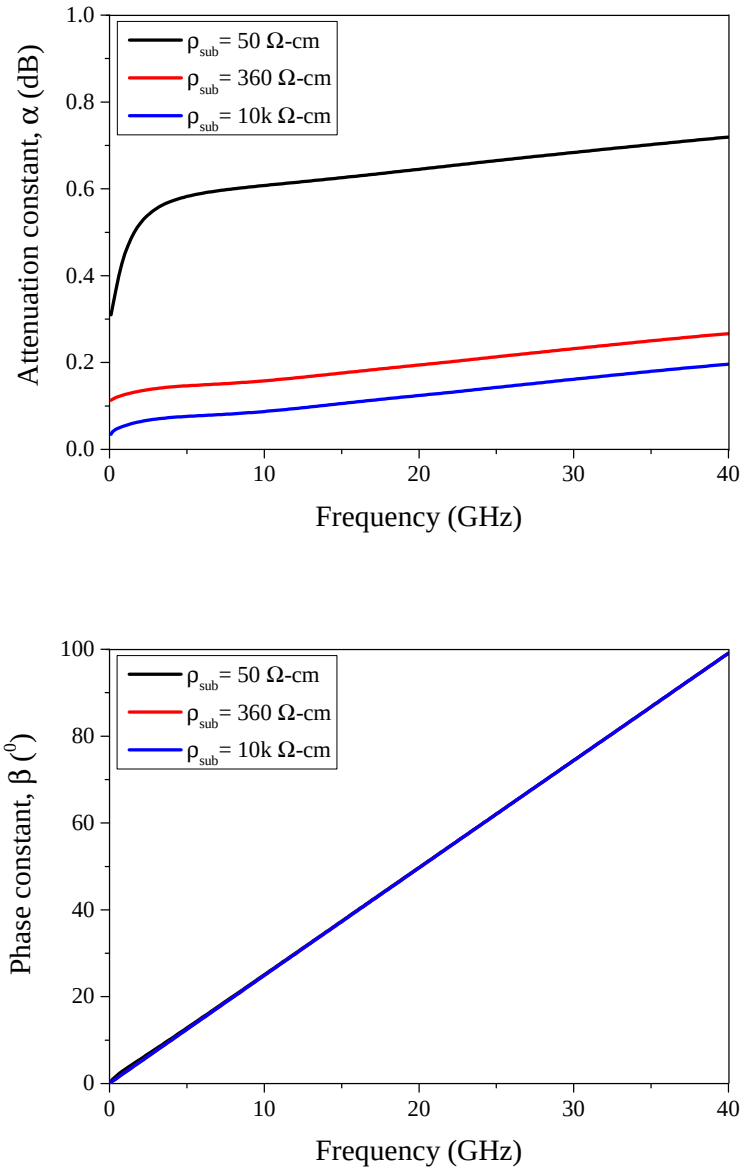

Figure 7.3: α (*Top*) and β (*Bottom*) obtained from SONNET simulations of oxide-free Al-Si CPWs with different Si substrate resisitivy, ρ_{sub}.

Figure 7.3 shows the exact representation of α and β for varying ρ_{sub}, where an increase in attenuation loss is observed for lower resistivity substrate and a consistent phase constant is obtained for all ρ_{sub}. Since it is an oxide-free Al-Si structure, the difference in α is due to the difference in substrate loss, α_d where PSC is not considered. Hence, lower resistivity substrate produces higher substrate losses and consequently higher attenuation losses. As for the phase constant, the consistency occurs due to all structures

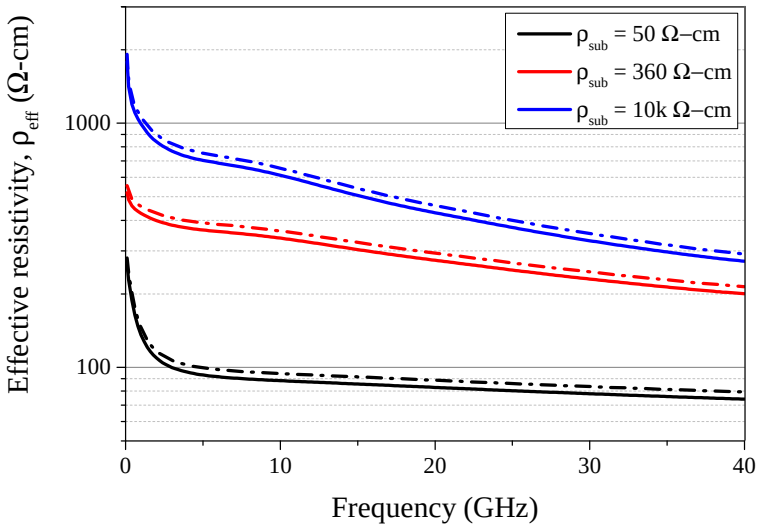

Figure 7.4: Effective resistivity calculated based on full expression in Equation 7.7 (solid lines) and simplified expression in Equation 7.12 (dotted lines) for SONNET-simulated Al-Si CPWs with different ρ_{sub}.

having similar $\epsilon_{r,eff}$ and so not much change can be seen after varying ρ_{sub}. Meanwhile, Figure 7.4 compares the values of ρ_eff calculated based on full expression and simplified expression. The simplified values are within 5%-tolerance, indicating good approximation on the actual ρ_{eff} expression. Also, the initial claim of ρ_{eff} dependency on α and β (hence, CPW losses) is now verified. However, by analysing the earlier responses of α and β, it is predicted that ρ_{eff} has a stronger dependency on α considering that β might remain constant due to unchanged $\epsilon_{r,eff}$ in all of the analysed structures.

To illustrate this matter further, a SiO_2 layer was added in between Si substrate and Al metal lines to show the effect of changing (or otherwise, not changing) $\epsilon_{r,eff}$ on α and β and the results are illustrated in Figure 7.5 and Figure 7.6. In Section 3.2 of Chapter 3, $\epsilon_{r,eff}$ is said to remain unchanged for t_{ox}<2μm on an infinitely-thick Si substrate. In this simulations, both α and β are in agreement with the statement and the values only start to change when t_{ox}=2μm for both ρ_{sub} of 50Ω-cm and 10kΩ-cm.

For the case of α, the value reduces because SiO_2 thickness at this point is thick enough to change the dynamic effect of substrate loss due to substrate's conductivity and that since the layer is considered to be a perfect insulator with zero conductivity in SONNET, PSC effect is assumed to be non-existent from the simulation's perspective.

As for β, the observed reduction is due to the decrease in $\epsilon_{r,eff}$ when t_{ox} reaches 2μm and so, since all analysed structure will have an oxide layer of less than 2μm, $\epsilon_{r,eff}$ and consequently, β are considered to be the same. Therefore, for this scope of work, ρ_{eff} can be said to be solely dependent on α, where losses due to PSC effect can be studied.

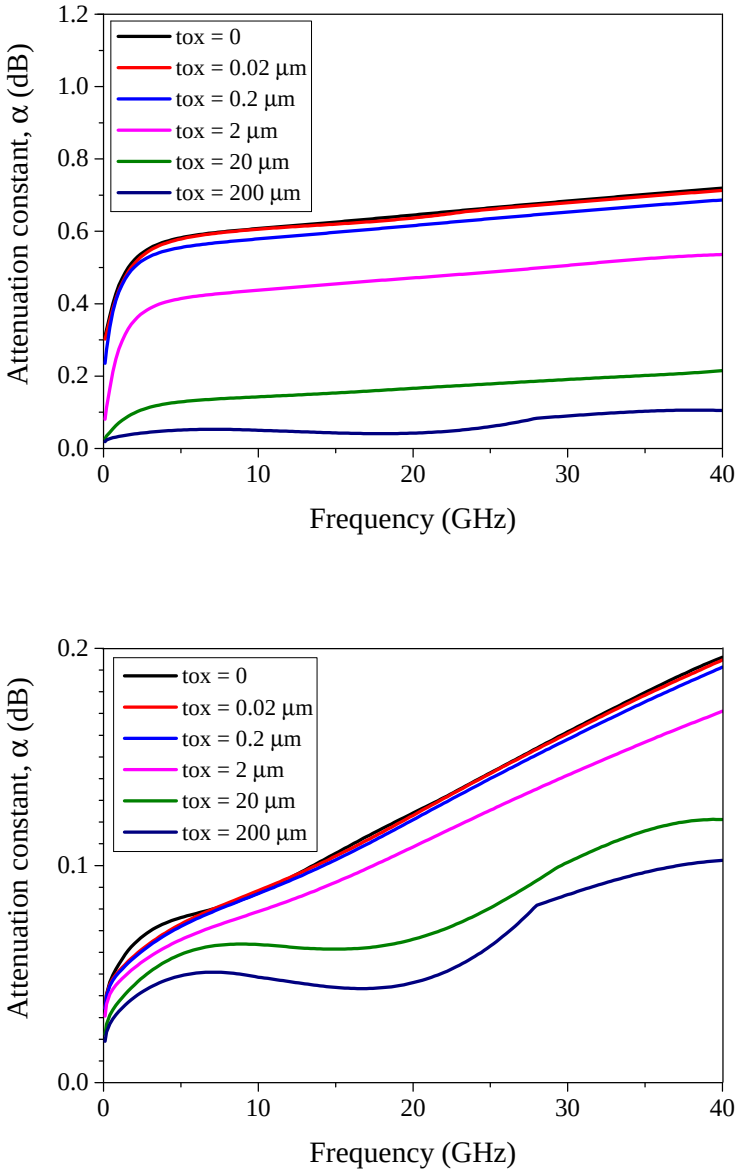

Figure 7.5: Attenuation constant, α for varying t_{ox} on ρ_{sub} = 50Ω-cm (*Top*) and ρ_{sub} = 10kΩ-cm (*Bottom*).

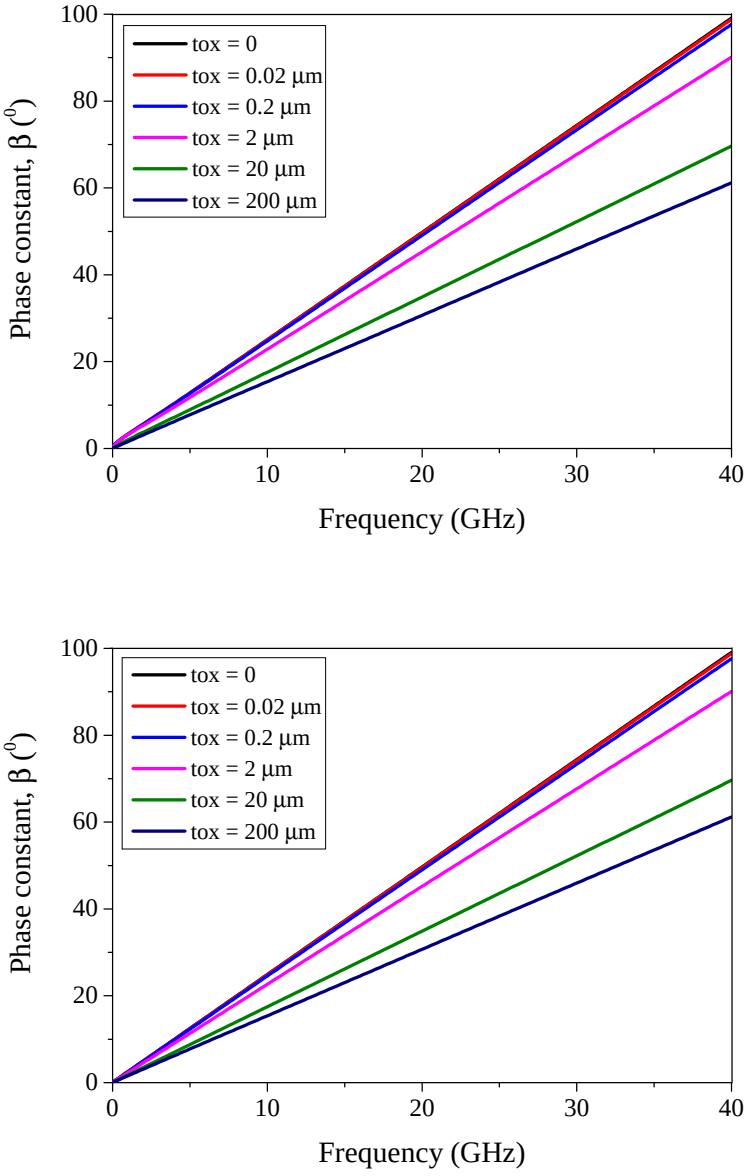

Figure 7.6: Phase constant, β for varying t_{ox} on ρ_{sub} = 50Ω-cm (*Top*) and ρ_{sub} = 10kΩ-cm (*Bottom*).

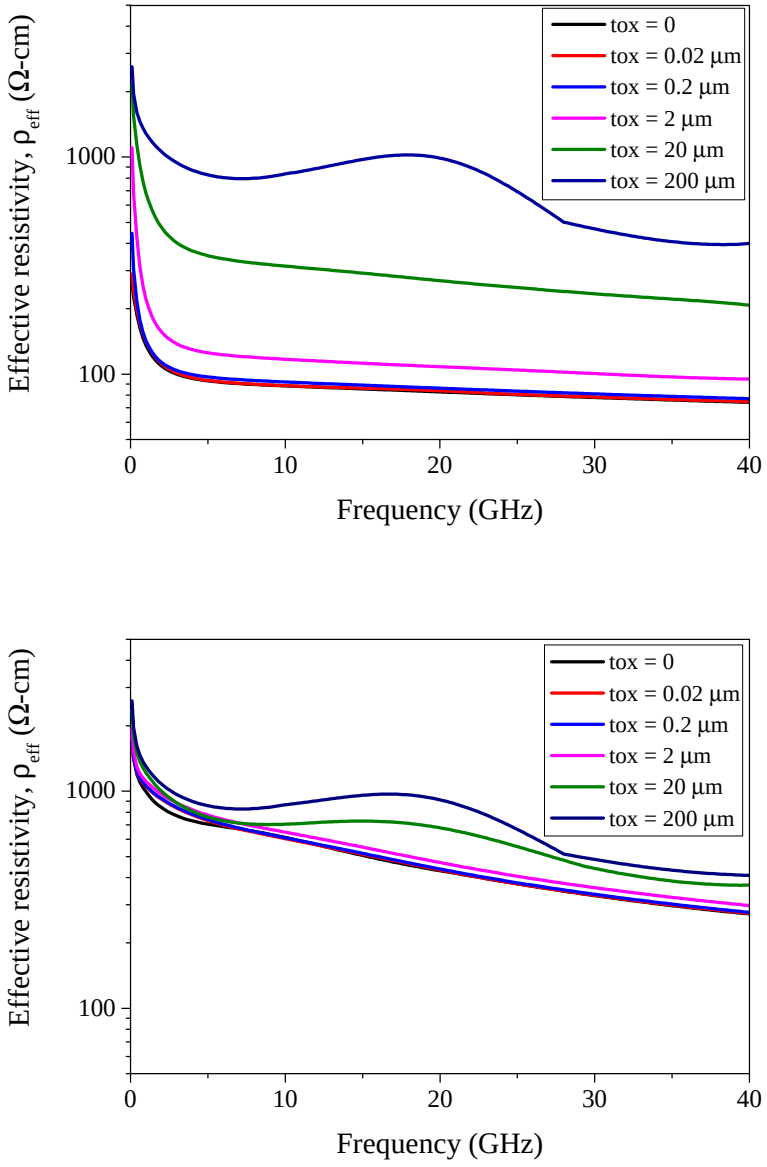

Figure 7.7: Corresponding effective resistivity, $\epsilon_{r,eff}$ for varying t_{ox} on ρ_{sub} = 50Ω-cm (*Top*) and ρ_{sub} = 10kΩ-cm (*Bottom*).

Appendix B: RLC Circuit Analysis using SONNET

Top view of tunable device structure used in this simulation is shown in Figure 7.8. A square-shaped parallel plate capacitor is incorporated in the middle of CPW line, with tapering included to provide smoother signal transmission and reduce power loss.

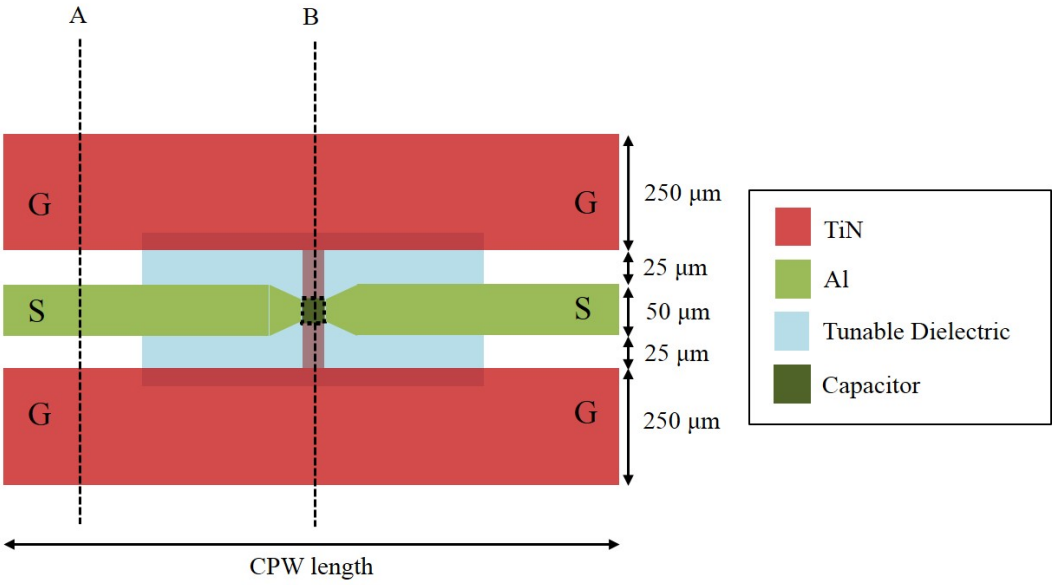

Figure 7.8: (Top view) Tunable device structure using parallel plate capacitor with G-S-G configuration. Signal width, S, ground width, W_g and signal-to-ground spacing, W values are similar to the ones used in Chapter 5. For parallel plate capacitor, a square-shaped structure is used.

Cross-sectional views of the structure shown in the above figure are illustrated in Figure 7.9. Al metal signal line is slightly elevated as seen in (A), however the structure still behaves as CPW transmission line with return loss and insertion loss values are similar to non-elevated structure (results not shown here). Cross-sectional view at (B) portrays parallel plate capacitor structure with Al and TiN act as metal plates and a 50nm-thick dielectric is sandwiched between them.

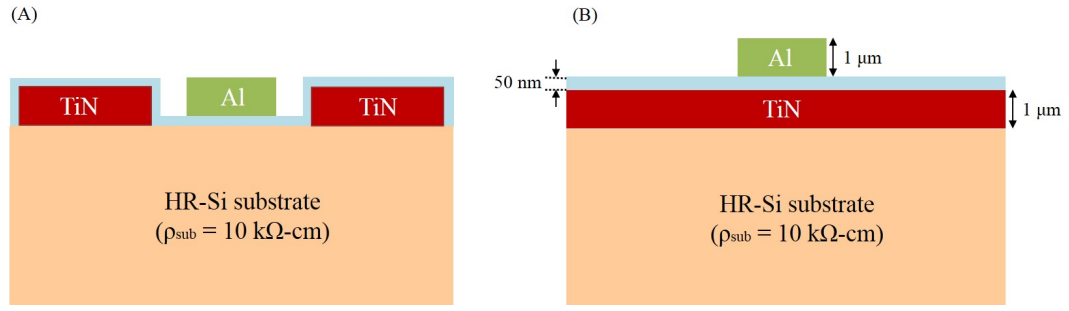

Figure 7.9: Cross-sectional views of tunable device structure at (A) and (B) as depicted in Figure 7.8. Dielectric, ϵ_r thickness is 50 nm, whereas Al and TiN thickness are set to be 1 μm.

Unfortunately, the proposed structure cannot be designed conformally in SONNET due to software's limitation hence the design was altered to accommodate this. The new design is shown in Figure 7.10 with cross-sectional view at position (B) is kept the same.

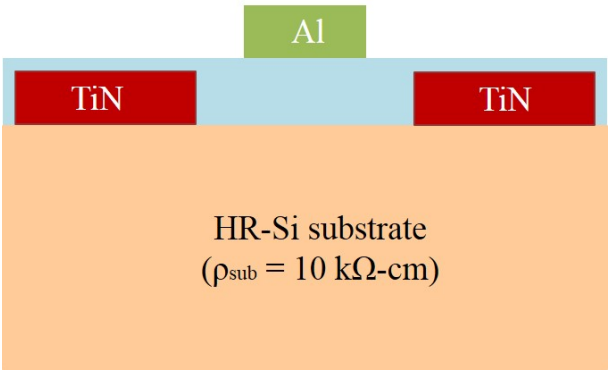

Figure 7.10: New design at (A) to accommodate SONNET's limitation on conformal design.

3D image of simulated device is depicted in Figure 7.11. Device was analysed through S-parameter measurements for frequencies between 0.01 to 40 GHz and the resulted current density for 4 μm^2 capacitor with ϵ_r of 3.9 at 40 GHz is shown in Figure 7.12. The inset shows maximum amount of current flows through the middle part of the structure, indicating possibility of capacitive behaviour.

Return loss, insertion loss and phase shift responses for 4 μm^2 capacitor structure with different ϵ_r were extracted from S-parameter data and are plotted in Figure 7.13. Return loss decreases with increasing ϵ_r before it starts to make a significant increase at higher ϵ_r (in this case, when $\epsilon_r = 400$). The same observation is made for insertion loss response where the losses are comparable for $\epsilon_r \leq 20$ but it starts to increase rapidly for $\epsilon_r = 400$. For the case of phase shift, linear relationship is seen for increasing frequency and the value increases with increasing ϵ_r for a fixed frequency value.

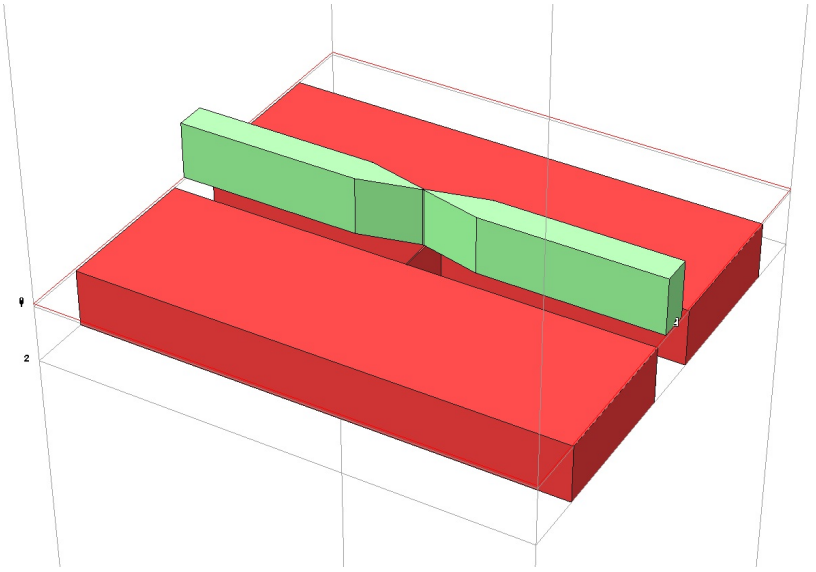

Figure 7.11: 3D image of tunable device structure studied and simulated in SONNET.

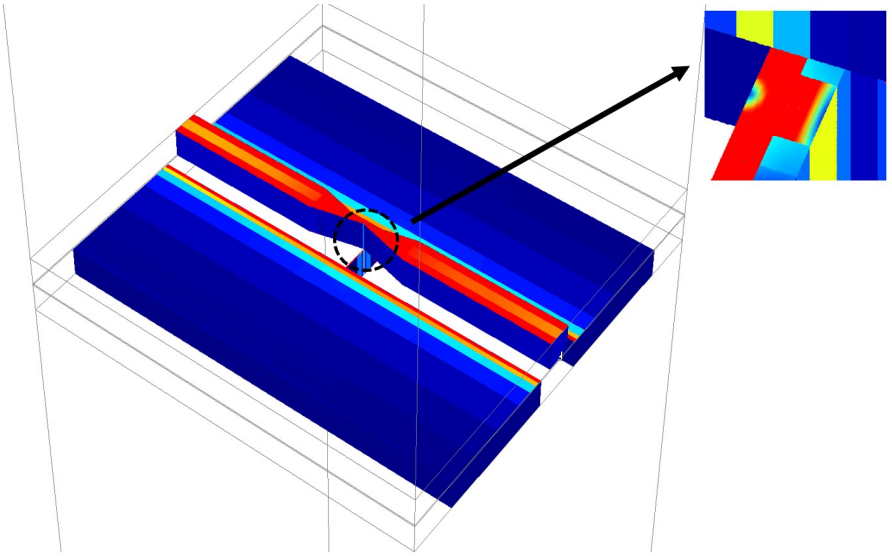

Figure 7.12: Current density at 40 GHz for 4 μm^2 capacitor with ϵ_r of 3.9 (similar to dielectric permittivity of SiO_2. Structure is seen to behave like a capacitor at this frequency.

Another set of simulation was conducted for a 25 μm^2 capacitor with the results shown in Figure 7.14. Similar observation is made for return loss and insertion loss, where the values start to increase when $\epsilon_r = 20$. Interestingly for phase shift response, a linear relationship is not observed for $\epsilon_r \geq 50$ rather, the value reaches a plateau at a certain frequency and the frequency at which the value settles is lowered with increasing ϵ_r.

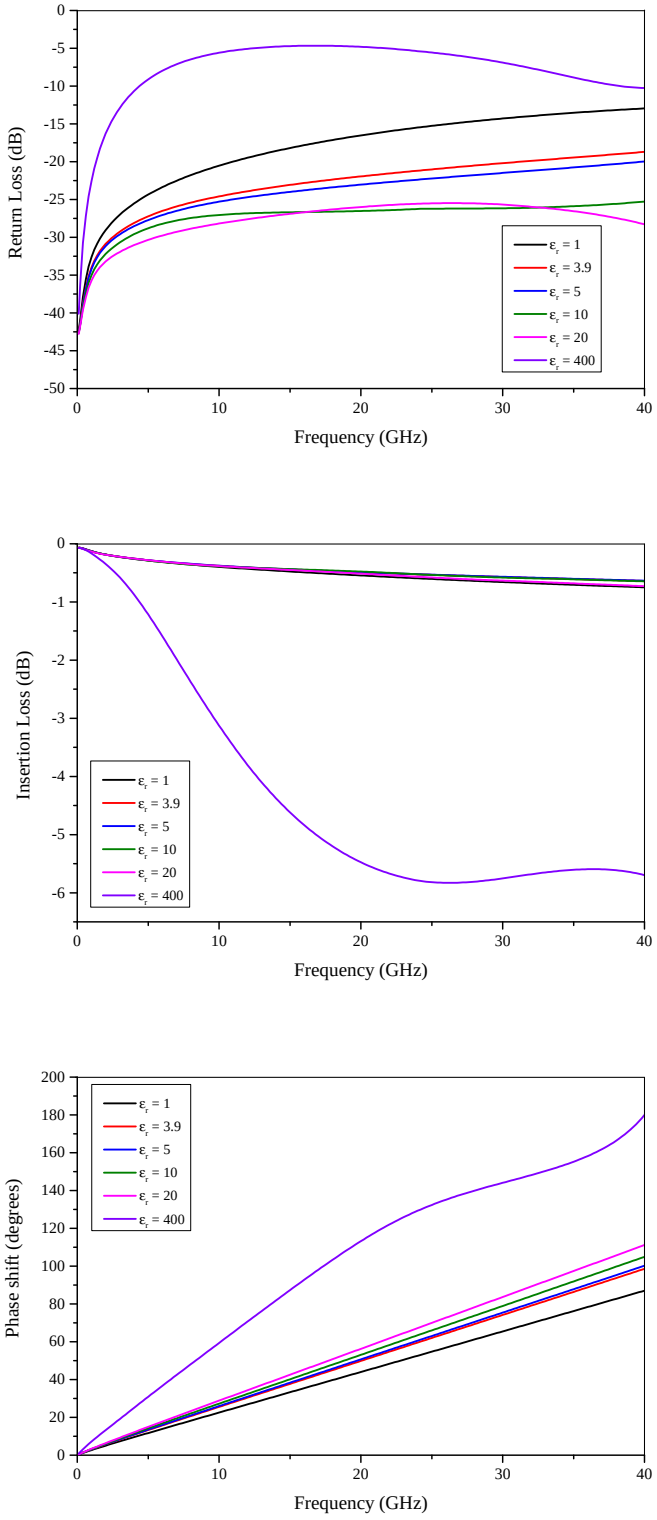

Figure 7.13: Return loss, insertion loss and phase shift of tunable device structure with 4 μm^2 square-shaped, parallel plate capacitor for varying ϵ_r.

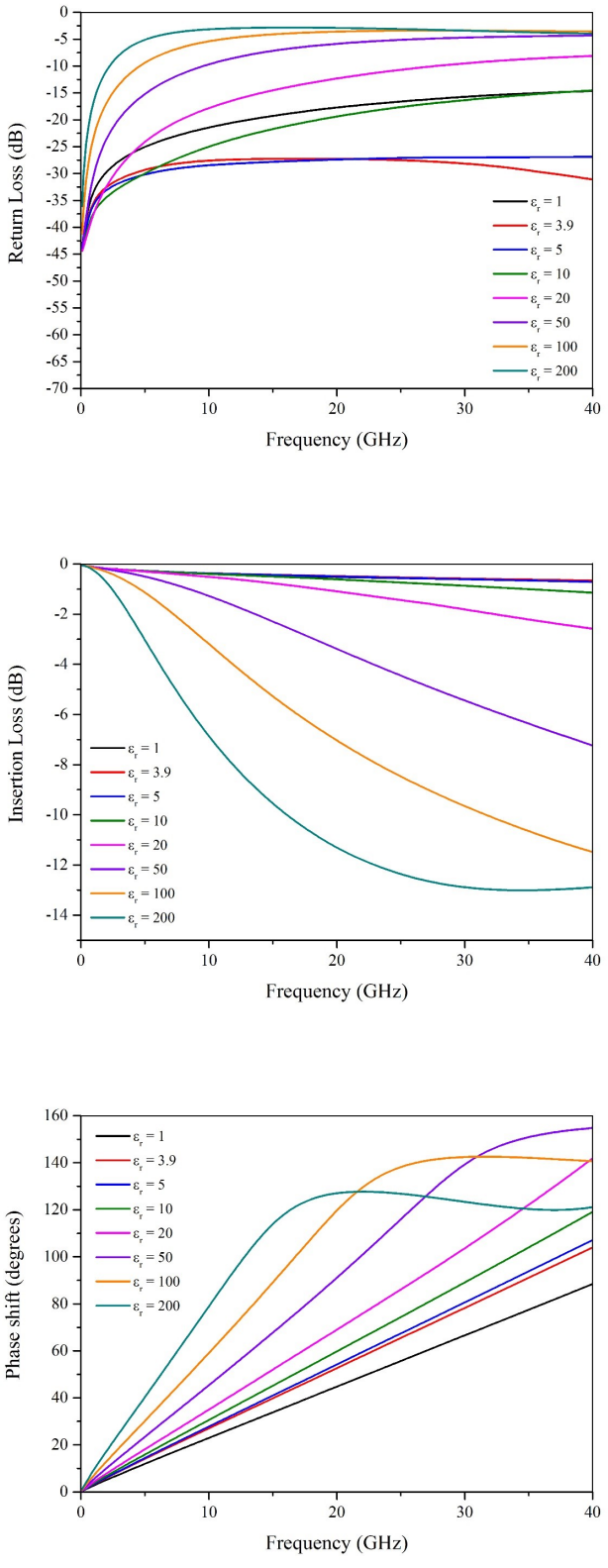

Figure 7.14: Return loss, insertion loss and phase shift of tunable device structure with 25 μm^2 square-shaped, parallel plate capacitor for varying ϵ_r.

Appendix C: Attenuation characteristics for CPWs

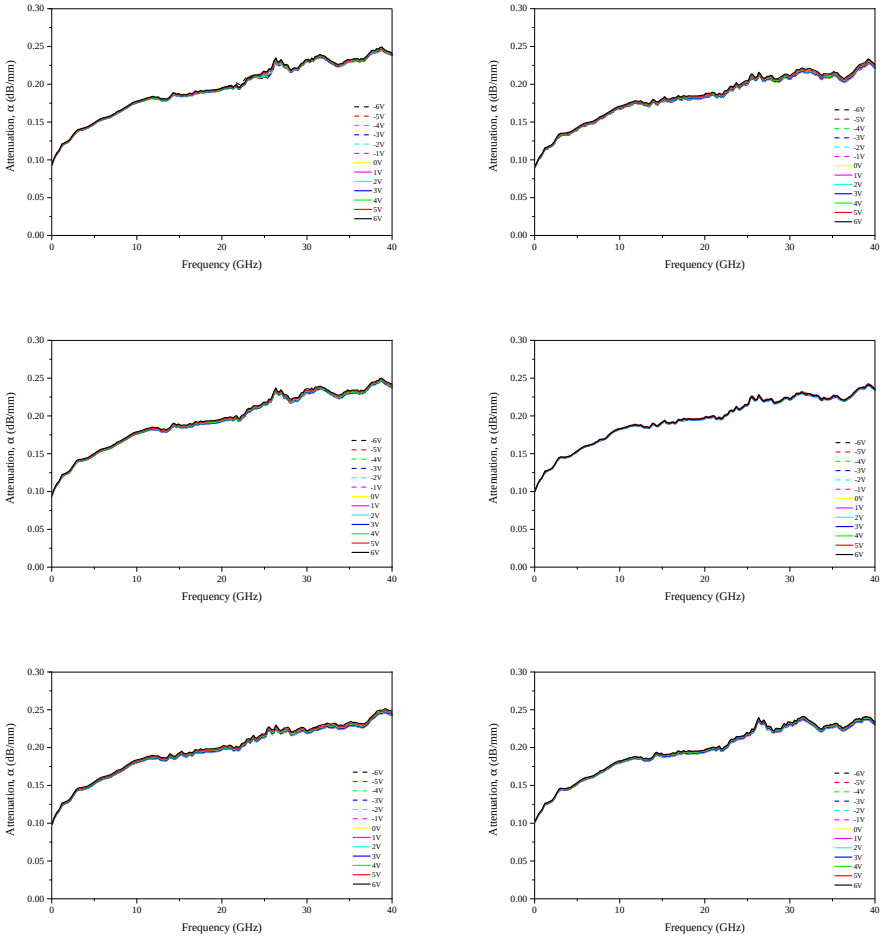

Figure 7.15: Au-compensated HR-Si substrates developed through combined annealing procedure and without Au-etching effect

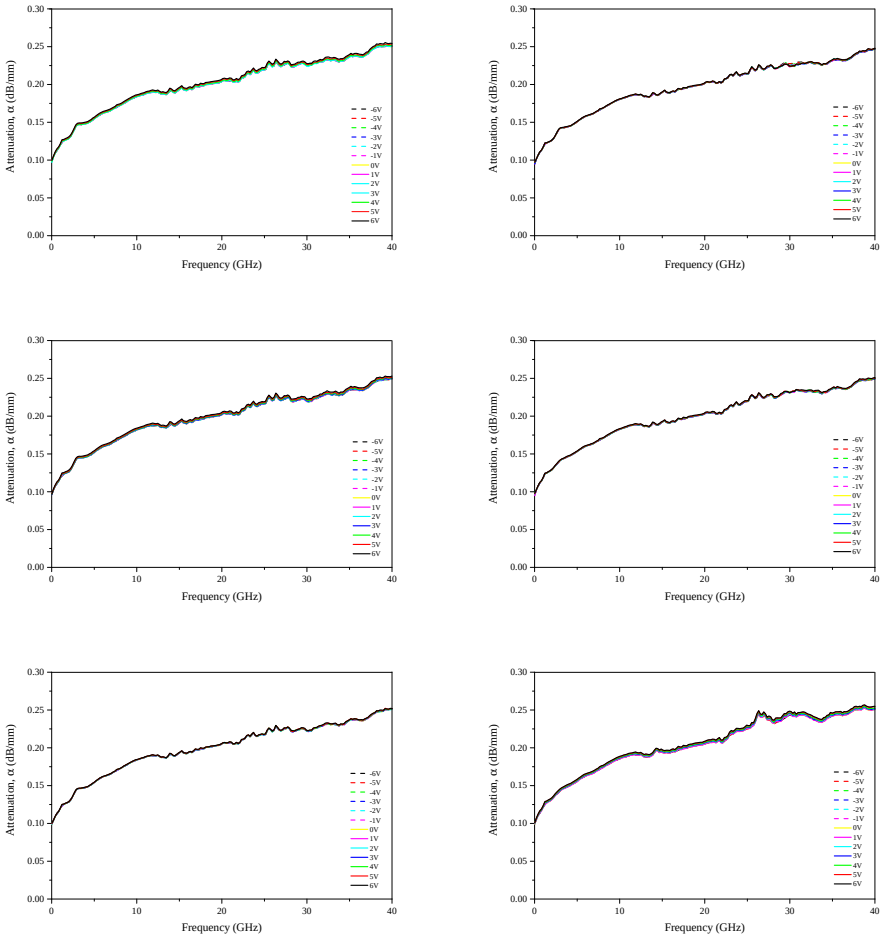

Figure 7.16: Au-compensated HR-Si substrates developed through combined annealing procedure and with Au-etching effect

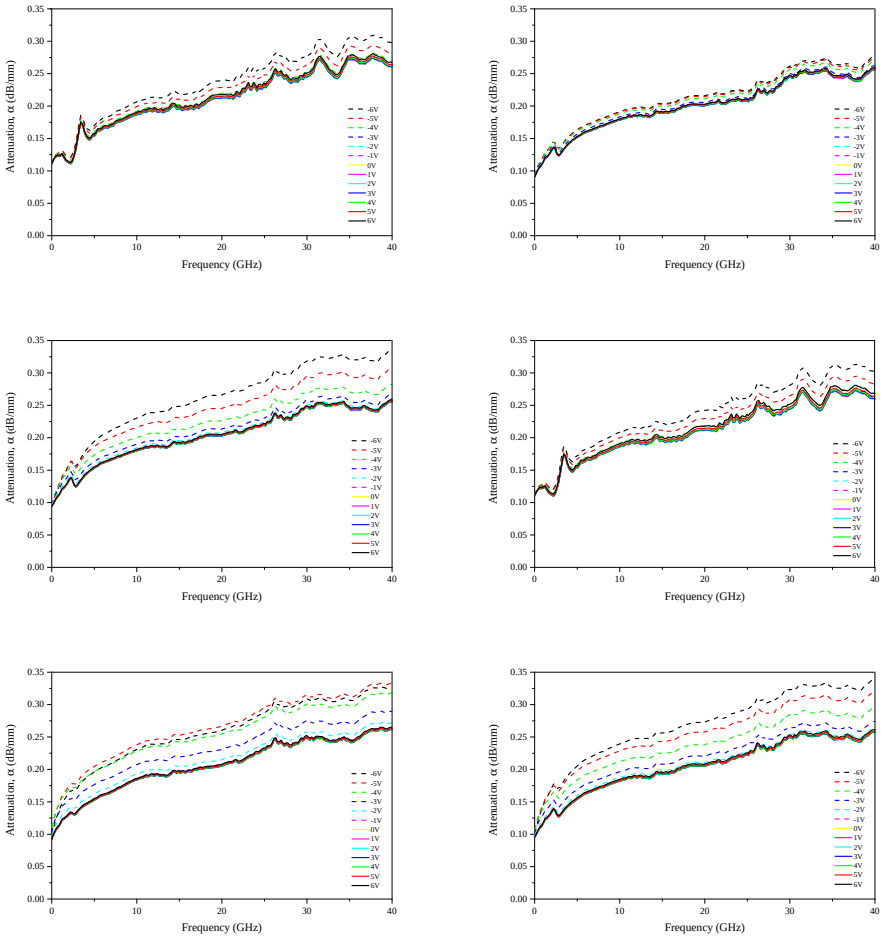

Figure 7.17: Au-compensated HR-Si substrates developed through quenching annealing procedure and without Au-etching effect

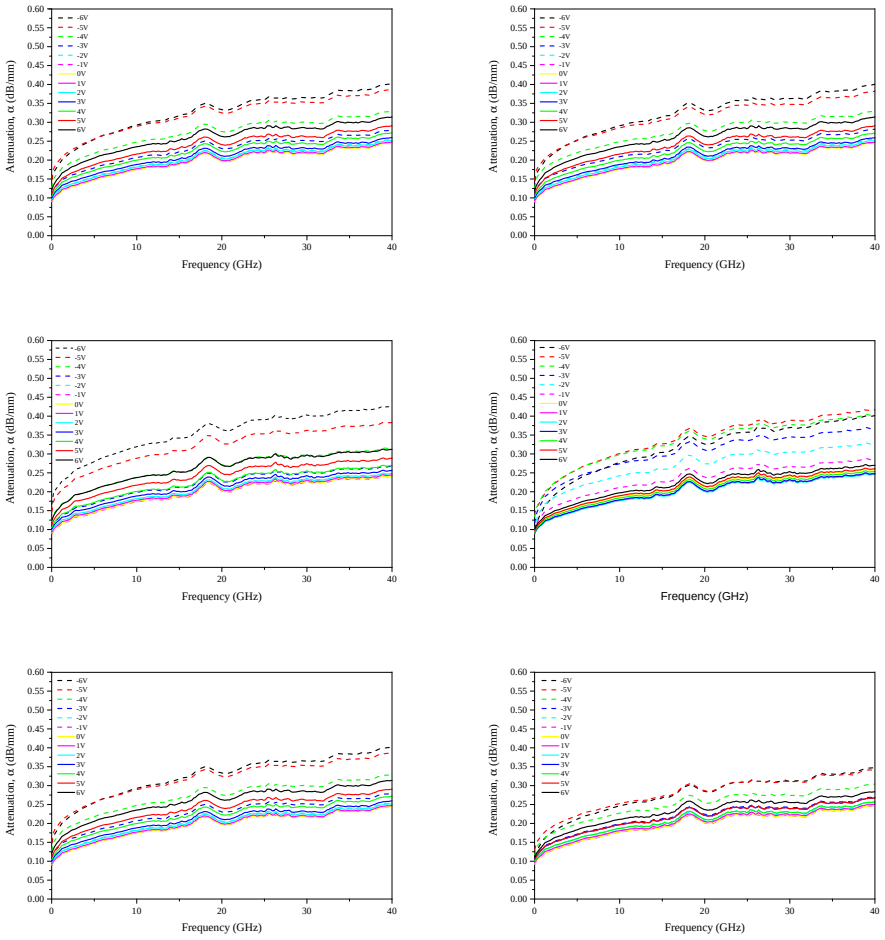

Figure 7.18: HiRes Float-zone Si substrates

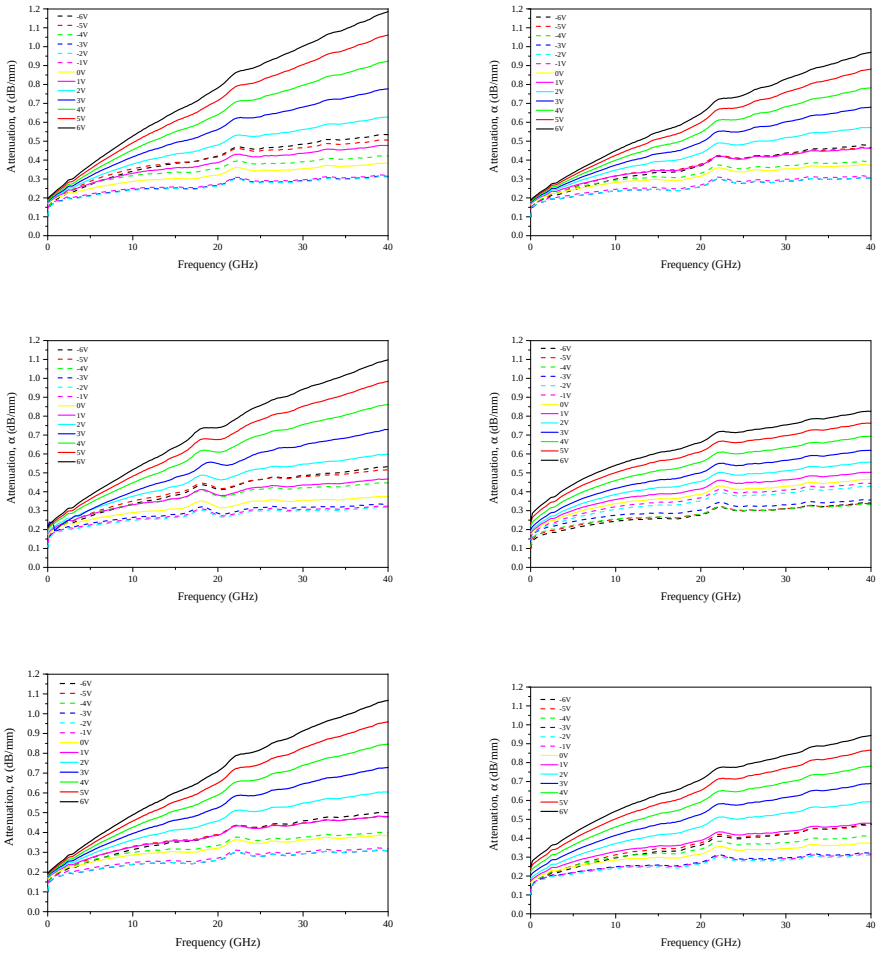

Figure 7.19: Float-zone Si substrates