

Design and characterization of low-loss 2D grating couplers for silicon photonics integrated circuits

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ABSTRACT

We present the characterization of Silicon-on-insulator (SOI) photonic-crystal based 2D grating-couplers (2D-GCs) fabricated by CEA-Leti in the frame of the FP7 Fabulous project, which is dedicated to the realization of devices and systems for low-cost and high-performance passives-optical-networks. On the analyzed samples different test structures are present, including 2D-GC connected to another 2D-GC by different waveguides (in a Mach-Zehnder like configuration), and 2D-GC connected to two separate 2D-GCs, so as to allow a complete assessment of different parameters. Measurements were carried out using a tunable laser source operating in the extended telecom bandwidth and a fiber-based polarization controlling system at the input of device-under-test. The measured data yielded an overall fiber-to-fiber loss of 7.5 dB for the structure composed by an input 2D-GC connected to two identical 2D-GCs. This value was obtained at the peak wavelength of the grating, and the 3-dB bandwidth of the 2D-GC was assessed to be 43 nm. Assuming that the waveguide losses are negligible, so as to make a worst-case analysis, the coupling efficiency of the single 2D-GC results to be equal to -3.75 dB, constituting, to the best of our knowledge, the lowest value ever reported for a fully CMOS compatible 2D-GC. It is worth noting that both the obtained values are in good agreement with those expected by the numerical simulations performed using full 3D analysis by Lumerical FDTD-solutions.

Keywords: silicon photonics, high speed link, short reach optical connections

1. INTRODUCTION

During the last decade Silicon Photonics (Si-Photonics) technology established as mature technology for the fabrication of low cost-scalable miniaturized optical components [1]. Silicon-on-insulator (SOI) technology has been widely accepted as the ideal fabrication platform for silicon photonics components providing a CMOS compatible, high-index contrast basic building block. A wide range of extremely high performing SOI-devices for the new generation optical communications, have already been demonstrated such as ultra-low loss waveguides [1], optical filters [1], high speed optical transceiver [2] as well as nonlinear-based components for all optical signal processing [3], [4]. However the practical implementation of silicon photonics transceivers is still facing relevant challenges, and consistent research effort are devoted to the integration of components and devices that are required to be compatible with the existing optical fiber networks [5].

One of the main challenges related to the design and fabrication of Si-Photonics-based devices is that of identifying structures allowing to couple light from a single mode optical fiber to sub-micrometer scale SOI waveguides with very high efficiency [5]. Different coupling approaches have been proposed in the last decade such as butt-coupling, polymer-assisted inverse coupling and grating assisted light coupling. Even though butt coupling schemes could reach very high coupling efficiencies, they are not commonly perceived by the scientific community, and by the main Si-Photonics

companies, as a viable solution for the mass-production scale silicon photonic products. This is mainly due to the fact that they require relatively high complexity fabrication steps, not fully compatible with the CMOS technology. Furthermore this approach entails the use of lensed optical fibers, which are not practical for device-packaging purposes. On the other hand, grating assisted coupling schemes, attracted considerable attention in the last few years because of their ability to utilize standard single mode optical fiber, and their flexibility for the final packaging step [5]. Si-Photonics grating couplers (GCs) can be lithographically realized on a SOI wafer and etched down by using standard CMOS compatible dry-etching techniques. The generated devices are generally quite tolerant to fabrication imperfections and alignment tolerances making them the ideal candidate for the next-generation devices.

Significant coupling efficiency enhancement have been reached in the last years by several groups, showing a maximum coupling ratio coefficient of 92 % [6]–[9], when the most sophisticated 1D non uniform apodized with Bragg back-reflector is employed; nevertheless this kind of grating allows efficient coupling only of a single polarization-component of the input radiation. Fully CMOS-compatible 1D-grating have also been successful demonstrated providing coupling efficiency up to 70% [10]. Although the practical implementation of efficient 1D grating has been widely demonstrated and accepted by the scientific community, they still exhibit a strong sensitivity to the optical input fiber state of polarization, making them not suitable for many intra-system applications. In order to overcome this limitation 2D-gratings could be explored. Such devices are classically formed by orthogonally superimposing two 1D gratings, forming an optical component that can couple the incoming light, independently from its state of polarization, into two waveguides that support the fundamental TE optical mode. A crucial figure of merit for such components is represented by the total coupling efficiency (i.e. the sum of the coupling efficiency of each arm) as well as by the optical bandwidth and its sensitivity to the state of polarization of the incoming light beam. CMOS compatible 2D-GCs have been demonstrated showing overall efficiencies up to 37% [7], [11].

By conducting a rigorous campaign of 3D simulations, exploiting the FDTD technique, of photonic-crystal-based gratings we theoretically shown that the efficiency of such devices could be improved by adopting an optimal configuration of hole-depth, hole radius and grating pitch [12]. In this work we show the experimental demonstration of a fully CMOS compatible optimized 2D-GCs showing, to the best of our knowledge, the highest coupling efficiency ever reported in literature along to a very low input state of polarization sensitivity. This result makes the 2D-GCs an ideal candidate for high density, CMOS compatible, polarization insensitive, applications.

2. DEVICE DESIGN AND FABRICATION

The proposed device is a 2D uniform grating coupler designed by conducting an extensive campaign of full 3D-FDTD simulations, employing the commercial Lumerical[®] software. The full design optimization procedure has been extensively described in a previous work from our research group [12] showing that a full 3D simulation approach is required in order to find the best design parameters. We show in Fig. 1 a schematic of the designed device, highlighting the parameters that have been varied as a consequence of the numerical-simulations campaign for device optimization.

The 2D grating cross section is shown in Fig.1 (inset). A thick Silicon substrate is topped by a 2 μm SiO_2 layer, where a 220 nm silicon layer is assumed to form the guiding layer. A 750 nm top oxide layer is considered as cladding material to meet the standard process flow employed by CEA-Leti in their laboratories. The simulated fiber source is placed at $\theta = 15^\circ$ with respect to the normal-incident axis (z axis in Fig.1), positioned on the plane that bisects the two grating arms (i.e. the plane is normal incident to the grating plane and at 45° with respect to both x and y axis).

The optical mode is simulated by employing a Gaussian source centered at a wavelength of $\lambda = 1550$ nm with a Mode Field Diameter (MDF) of 10.4 μm . In Fig. 1, CE_x and CE_y represent the normalized coupled light intensity for each arm,

respectively. The total coupling efficiency is thus defined as $CE_T = CE_x + CE_y$. Our simulations have been conducted by considering a total simulated volume of $15 \mu\text{m} \times \mu\text{m} \times 5 \mu\text{m}$ that fully surrounds the 2D grating coupler region.

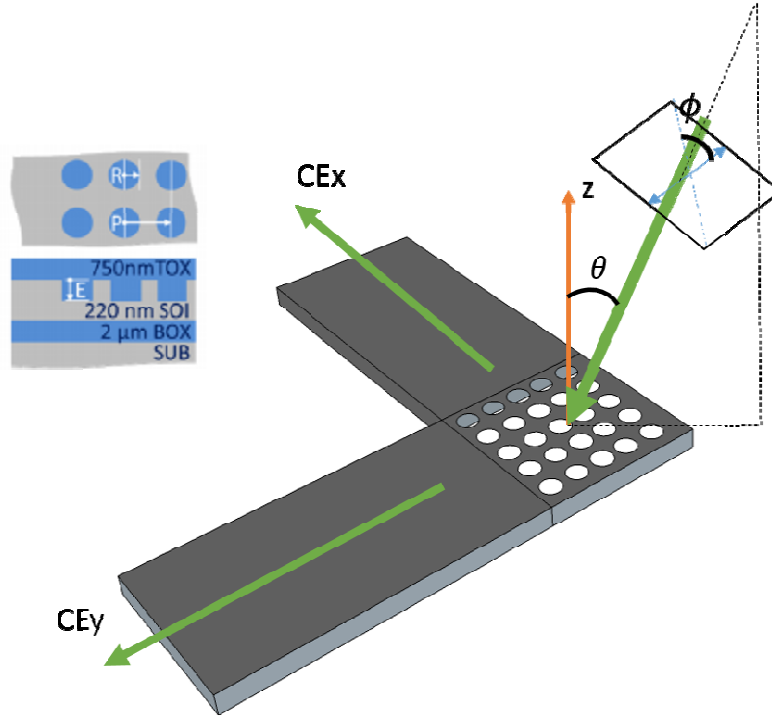


Fig. 1: 2D uniform grating coupler scheme.

In order to reduce computational requirements, an integrated conformal mesh algorithm has been used, allowing us to use a higher spatial resolution for regions where the refractive index variations are stronger while a relaxed resolution has been employed for regions in which the refractive index difference is moderate. Before launching the simulation campaign, convergence tests were conducted to assess the ability of our mesh algorithm to accurately describe the electromagnetic scenario. By analyzing simulations data we assessed the 2D-GC parameters combination that lead to the best CE_T .

Table 1 summarizes the parameters that have then be submitted to the CEA-Leti fabrication cleanroom for the real device fabrication.

Table 1: Optimized 2D SOI Grating Coupler Parameters

Si-thickness (S)	220 nm
BOX Thickness	2.0 μm
Etch Depth (E)	120 nm
Pitch (P)	630 nm
Radius (R)	179 nm
CE_T	-3.2 dB (47 %)
PDL	-0.4 dB
Footprint	12 $\mu\text{m} \times 12 \mu\text{m}$

The device was fabricated starting from a commercial SOI wafer composed of a 2 μm thick Buried Oxide Layer (BOX) covered by a 220 nm thick crystalline silicon layer. The Si layer was patterned by means of a backend compatible 193 nm Deep UV lithography machine, which defined both the waveguide and grating patterns. A first etching step was then performed to define the grating coupler final device, employing an etching depth of 120 nm. After a deposition of a silica hard mask a second etching steps was done down to the BOX (etch depth 220 nm) to define the Si-nanowire

vertical pattern. A 750 nm Top Oxide layer (TOX) was finally deposited on the wafer acting as protective layer and giving more mechanical stability to the final sample.

3. EXPERIMENTAL CHARACTERIZATION

The test structure shown in Fig. 2 was designed to assess the CE_T of a single 2D-GC by assuming that the multimode waveguide propagation losses are negligible, thus allowing to obtain a worst-case evaluation of the 2D-GC losses, as all the waveguide losses are included in the CE_T coupling losses. By properly setting the input fiber polarization, it is possible to assess the CE_T of a single 2D-GC by measuring the total insertion loss (IL) between the *Input Grating* coupler (point 1) and one of the *Output Grating* couplers (both point 2 and 3 are suitable depending on the input polarization) by assuming that $CE_T = IL / 2$.

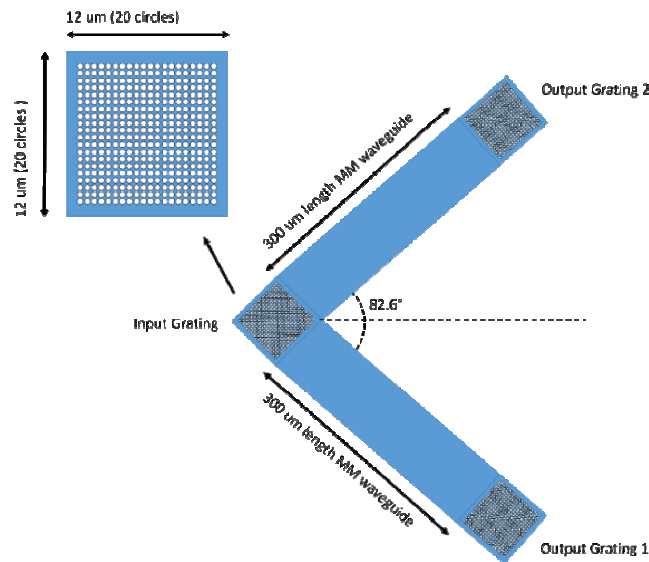


Fig. 2: Test structure to assess the single port CE

The experimental set-up used to perform all the measurements is shown in Fig.3. As a very accurate total loss measurement is required we used an OSA (sensitivity high at resolution of 0.01 nm) to measure both the input and the output power. The input optical beam was generated by means of an isolated External Cavity Laser (ECL) tunable in the range from 1510 nm to 1590 nm (laser linewidth <100 kHz).

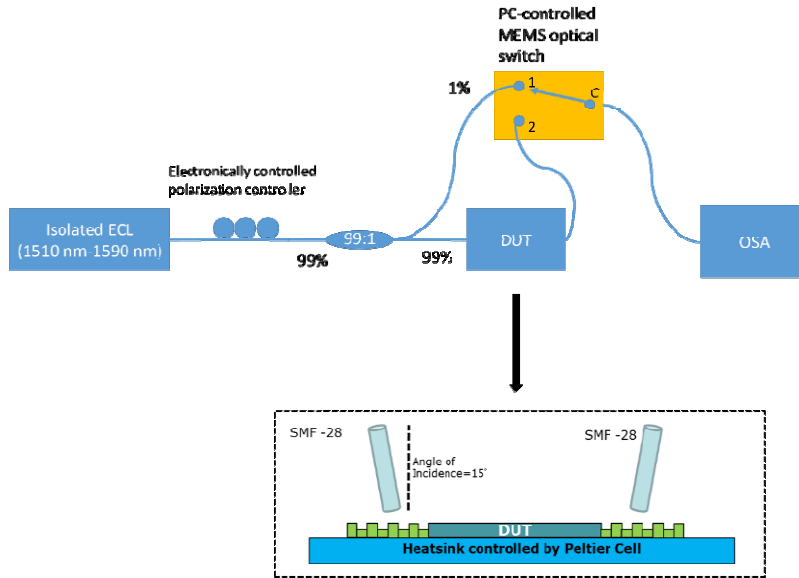


Fig. 3: Experimental set-up scheme. ECL: External Cavity Laser, PM: Power Meter, DUT: Device Under Test, OSA: Optical Spectrum Analyser.

The ECL-generated light was sent to an electronically-controlled fiber-based polarization controller that is able to generate every state of polarization across the Poincare sphere. A fiber coupler was then used to tap the 1% of the light, while the remaining 99% is sent to the Device Under Test (DUT) by means of a vertical coupling scheme (see Fig. 5 inset). The 1% was sent to an optical switch (MEMS activated), allowing us to carefully measure with the same OSA (to avoid possible mis-calibration issues) the optical beam power, at both the input and output of the experimental setup. For this reason also the output fiber was connected to the optical switch. The normalized efficiency measured at each port by optimizing the launching polarization is shown in Fig.4.

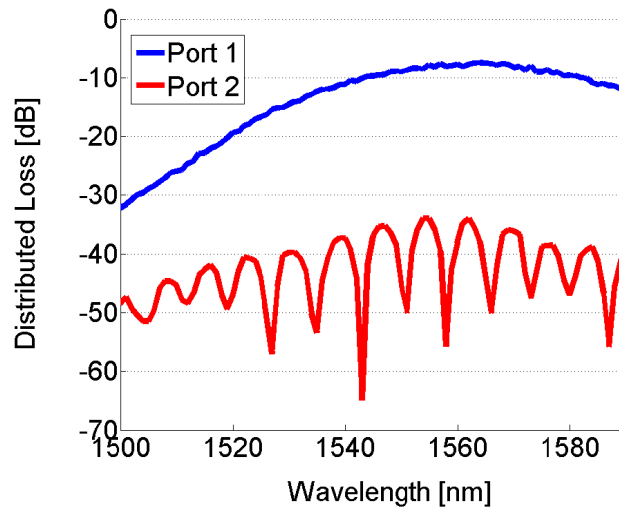


Fig. 4: Coupling Efficiency measured at Port 1 and Port 2 of the structure shown in Fig. 2

As can be seen from the graph shown in Fig.4, the maximum CE_T measured at the port 1 is equal to -3.75 dB which the highest value reported in literature for a CMOS compatible Si-Photonics 2D-GC to the best of our knowledge. The coupling bandwidth could be also estimated by analyzing the figure. The 3-dB bandwidth, centered at 1560 nm, was measured to be 44 nm.

As a second step we also measured the CE when a closed-loop structure is used. The device used for the measurements is composed by two 2D-GC connected via two single mode silicon waveguides, as depicted in Fig. 5.

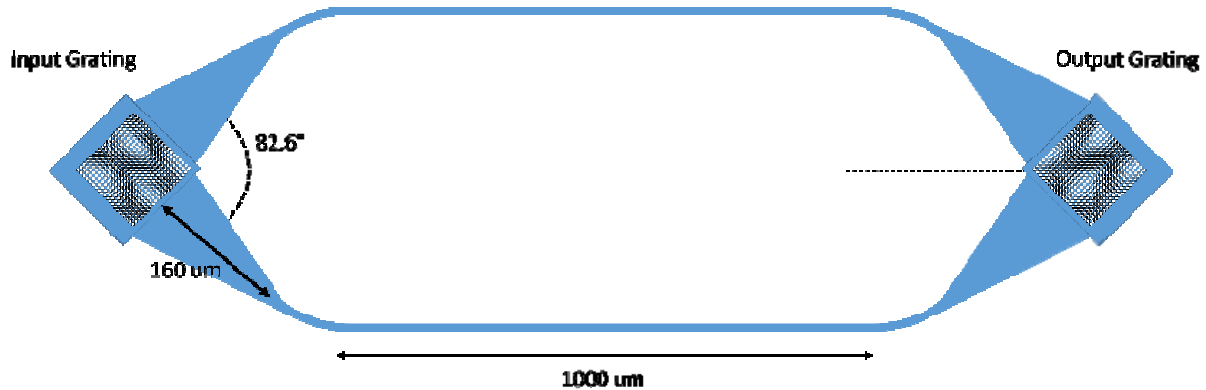


Fig. 5: Closed-loop test structure

The total IL (measured as the ratio between the power measured at the output fiber to the power measured at the input fiber by using the scheme depicted in Fig.3) was measured to be -8.94 dB. It is worth underlining that this value takes into account not only the 2D-GC loss, but also both the taper and the silicon waveguides losses.

4. CONCLUSION

In this work we experimentally demonstrated a high-efficiency 2D grating coupler that exhibited a maximum 2D-GC to 2D-GC coupling efficiency of -3.75 dB which is the highest value measured for a CMOS compatible two dimensional grating coupler. A closed-loop structure was also investigated, showing a total distributed losses of -8.94 dB with a coupling bandwidth of 44 nm at a 3 dB level.

5. ACKNOWLEDGMENTS

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