

Data-Driven Control: The Full Interconnection Case

Thabiso Maupong and Paolo Rapisarda

Abstract—We show how to compute a controller directly from data for a class of linear-time invariant systems. To do this, we use the interconnection paradigm where the control variables and to-be-controlled variables coincide, i.e. full interconnection. We also illustrate this process with an example.

Index Terms—Data-driven control, behaviours, interconnection, annihilators.

AMS Subject—93C05, 93C55.

I. INTRODUCTION

Consider given: observed noise free trajectories from a linear time-invariant unknown system; an “example trajectory” of the desired controlled system. We show how to find a *representation* of a controller that implements the desired controlled system. We call this approach *data-driven control*, as in [3].

Data-driven control has been studied from different points of view and different names, for example data-based control [6]; model-free control [1] and unfalsified control [5]. In [1], [3], [6] system data is used to find control inputs, whereas in [5] input/output data is used to falsify a control law from a set of available admissible control laws. We have shown in [4], that under suitable conditions, we can find a controller that implements a desired controlled system directly from data. We use the *interconnection* paradigm, see [9], to find a controller directly from data for both the general interconnection, i.e., when the system variables are split into *control variables* and *to-be-controlled variable* and the full interconnection case. In this paper, we further study the full interconnection case. We prove necessary and sufficient conditions suitable for finding a controller from data using full interconnection. Then, under such conditions, we present an algorithm. We also present an example to illustrate this procedure.

The structure of this paper is as follows. In Section II we introduce some background material including the notation used and some relevant concepts of the behavioral approach. In Section III we cover some aspects of control as interconnection, focusing mainly on full interconnection. Then, in Section IV we formally state the full interconnection data-driven control problem and present our solution to the problem. In Section V we provide an example. Finally, in Section VI we give some conclusions.

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II. BACKGROUND

A. Notation

We denote the space of w dimensional real vectors by \mathbb{R}^w and that of $g \times w$ real matrices by $\mathbb{R}^{g \times w}$. $\text{colspan}(A)$ denotes the subspace consisting of all linear combination of the columns of A and $\text{leftkernel}(A)$ denotes the subspace spanned by all vectors v such that $vA = 0$. $\text{col}(A, B)$ is the matrix obtained by stacking the matrix $A \in \mathbb{R}^{g_1 \times w}$ over $B \in \mathbb{R}^{g_2 \times w}$. The ring of polynomials with real coefficients in the indeterminate ξ is denoted by $\mathbb{R}[\xi]$ and the set of $g \times w$ matrices in the indeterminate ξ is denoted by $\mathbb{R}^{g \times w}[\xi]$. Let $R := R_0 + \dots + R_L \xi^L \in \mathbb{R}^{g \times w}[\xi]$ with $R_L \neq 0$ then L is the degree of R , denoted by $\deg(R)$. The set of all maps from \mathbb{Z} to \mathbb{R}^w is denoted by $(\mathbb{R}^w)^\mathbb{Z}$. The collection of all linear, closed, shift-invariant subspaces of $(\mathbb{R}^w)^\mathbb{Z}$ equipped with the topology of pointwise convergence is denoted by \mathcal{L}^w . The *backward shift* σ is defined by $(\sigma f)(t) := f(t+1)$.

B. Linear difference behaviors

We define a *dynamical system* as $\Sigma = (\mathbb{T}, \mathbb{W}, \mathfrak{B})$, with \mathbb{T} the *time axis*, \mathbb{W} the *signal space* and $\mathfrak{B} \subseteq \mathbb{W}^\mathbb{T}$ the *behavior*. Let $\mathbb{T} = \mathbb{Z}$ and $\mathbb{W} = \mathbb{R}^w$. We consider a class of systems whose behavior is a subspace of \mathcal{L}^w , i.e., \mathfrak{B} is linear, shift invariant and closed. It has been proven in Prop. 4.1A pp. 232-233 of [8] that if $\mathfrak{B} \in \mathcal{L}^w$ then there exists $R \in \mathbb{R}^{g \times w}[\xi]$ such that

$$\mathfrak{B} := \{w : \mathbb{Z} \rightarrow \mathbb{R}^w \mid R(\sigma)w = 0\},$$

where the operator $R(\sigma)$ is called *polynomial operator in the shift* and $R(\sigma)w = 0$ is called *kernel representation*. Henceforth we write $\mathfrak{B} = \ker(R(\sigma))$. R induces a *minimal representation* if no other kernel representation of \mathfrak{B} has less than g rows. It has been proven in [9] Prop. 1, p. 331 that if $R, R' \in \mathbb{R}^{g \times w}[\xi]$ are both minimal, then $\mathfrak{B} = \ker(R(\sigma)) = \ker(R'(\sigma))$ iff there exists a *unimodular* matrix (see Lemma 6.3-1, p. 375 of [2]) $U \in \mathbb{R}^{g \times g}[\xi]$ such that $R = UR'$.

$\mathfrak{B} \in \mathcal{L}^w$ is *controllable* if for any two trajectories $w_1, w_2 \in \mathfrak{B}$ there exists $t_1 \geq 0$ and $w \in \mathfrak{B}$ such that $w(t) = w_1(t)$ for $t \leq 0$ and $w(t) = w_2(t-t_1)$ for $t \geq t_1$. We denote by $\mathcal{L}^w_{\text{contr}}$ the collection of all controllable elements of \mathcal{L}^w .

Let $L \in \mathbb{N}$. The restriction of trajectories of \mathfrak{B} on the interval $[1, L]$ is defined by

$$\mathfrak{B}_{|[1,L]} := \{w : [1, L] \rightarrow \mathbb{R}^w \mid \exists w' \in \mathfrak{B} \text{ s.t. } w(t) = w'(t) \text{ for all } 1 \leq t \leq L\}.$$

The integer L in the above equation is called the *lag*. We denote by $\text{L}(\mathfrak{B})$ the smallest L such that $[w]_{[t, t+L]} \in$

$\mathfrak{B}_{|[t,t+L]}$ for all $t \in \mathbb{T} \Rightarrow [w \in \mathfrak{B}]$. Equivalently, $L(\mathfrak{B})$ is the smallest degree over all R such that $\mathfrak{B} = \ker(R(\sigma))$. We also use the following integer invariants: $n(\mathfrak{B})$, *McMillan degree*, the smallest state-space dimension among all possible state representations of \mathfrak{B} ; and $l(\mathfrak{B})$, the *shortest lag* described as follows. Let $\mathfrak{B} = \ker(R(\sigma))$ and define the degree of each row of R to be the largest degree of the entries. Then the minimum of degrees of the rows of R is the minimal lag associated with R and $l(\mathfrak{B})$ is the smallest possible minimal lag over all R such that $\mathfrak{B} = \ker(R(\sigma))$. Hence, all kernel representations of \mathfrak{B} has rows of lag at least $l(\mathfrak{B})$.

Let $w \in \mathfrak{B}$. A partition of $w := (w_1, w_2)$ is an *input/output* partition if w_1 is *maximally free* i.e., $\pi_{w_1}(\mathfrak{B}) = (\mathbb{R}^m)^\mathbb{Z}$, where $\pi_{w_1}(\mathfrak{B}) := \{w_1 \mid \exists w_2 \text{ s.t. } (w_1, w_2) \in \mathfrak{B}\}$, and w_2 contains no free components (see pp. 243-244 of [8]). Then w_1 is an input and w_2 an output. We denote by $p(\mathfrak{B})$ the *output cardinality*, i.e. number of outputs and $m(\mathfrak{B})$ *input cardinality*, the number of inputs.

C. Annihilators and fundamental lemma

The *module of annihilators* of \mathfrak{B} is defined by $\mathfrak{N}_{\mathfrak{B}} := \{n \in \mathbb{R}^{1 \times w}[\xi] \mid n(\sigma)\mathfrak{B} = 0\}$. Let $\mathfrak{B} = \ker(R(\sigma))$, then $\mathfrak{N}_{\mathfrak{B}}$ is equal to the $\mathbb{R}[\xi]$ -submodule of $\mathbb{R}^{1 \times w}[\xi]$ generated by the rows of R , see [10] pp. 83-84. The set of annihilators of \mathfrak{B} of degree less than $j \in \mathbb{Z}_+$ is defined by $\mathfrak{N}_{\mathfrak{B}}^j := \{r \in \mathbb{R}^{1 \times w}[\xi] \mid r \in \mathfrak{N}_{\mathfrak{B}} \text{ and } r \text{ has degree } \leq j\}$. Let $r_1, \dots, r_i \in \mathfrak{N}_{\mathfrak{B}}^j$ and $\tilde{r}_1 \dots \tilde{r}_i$ be the coefficients of r_1, \dots, r_i . Then $\mathfrak{N}_{\mathfrak{B}}^j$ is the set containing $\tilde{r}_1 \dots \tilde{r}_i$.

Definition 1: Let $L \in \mathbb{N}$. The *Hankel matrix* associated with a vector $w(1), \dots, w(T)$ for $T > L$ is defined by

$$\mathfrak{H}_L(w) := \begin{bmatrix} w(1) & w(2) & \dots & w(T-L+1) \\ w(2) & w(3) & \dots & w(T-L+2) \\ \vdots & \vdots & \dots & \vdots \\ w(L) & w(L+1) & \dots & w(T) \end{bmatrix}.$$

Definition 2: A vector $\tilde{u} = \tilde{u}(1), \tilde{u}(2), \dots, \tilde{u}(T)$ is *persistently exciting* of order L if $\mathfrak{H}_L(\tilde{u})$ is full row rank.

Now we state the *fundamental lemma* cf. [11].

Lemma 1: Assume $\mathfrak{B} \in \mathcal{L}_{\text{contr}}^w$. Let $\tilde{w} = \tilde{w}(1), \tilde{w}(2), \dots, \tilde{w}(T) := \text{col}(\tilde{u}, \tilde{y})$, $\tilde{w} \in \mathfrak{B}_{|[1,T]}$ such that $\tilde{u}(k) \in \mathbb{R}^{m(\mathfrak{B})}$ and $\tilde{y}(k) \in \mathbb{R}^{p(\mathfrak{B})}$ for $1 \leq k \leq T$. Finally, let $L \in \mathbb{N}$ such that $L > L(\mathfrak{B})$. If \tilde{u} is persistently exciting of order $L + n(\mathfrak{B})$, then $\text{colspan}(\mathfrak{H}_L(\tilde{w})) = \mathfrak{B}_{|[1,L]}$ and $\text{leftkernel}(\mathfrak{H}_L(\tilde{w})) = \tilde{\mathfrak{N}}_{\mathfrak{B}}^L$.

Proof: See Th. 1 pp. 327-328 of [11]. \blacksquare

Under the conditions of Lemma 1, for all $\tilde{w}' \in \mathfrak{B}_{|[1,L]}$ there exists $\tilde{v} \in \mathbb{R}^{T-L+1}$ such that $\tilde{w}' = \mathfrak{H}_L(\tilde{w})\tilde{v}$. Moreover, we can recover from \tilde{w} the laws of the system \mathfrak{B} that generated \tilde{w} . This leads us to following definition.

Definition 3: Let $L \in \mathbb{N}$ such that $L > L(\mathfrak{B})$ and $T \in \mathbb{N}$ such that $T \gg L$. Then $\tilde{w} \in \mathfrak{B}_{|[1,T]}$ is *sufficiently informative* about \mathfrak{B} if $\text{colspan}(\mathfrak{H}_L(\tilde{w})) = \mathfrak{B}_{|[1,L]}$ and $\text{leftkernel}(\mathfrak{H}_L(\tilde{w})) = \tilde{\mathfrak{N}}_{\mathfrak{B}}^L$.

III. FULL INTERCONNECTION

In the following discussion we assume that the plant behavior, the controller behavior and the controlled behavior

are all elements of $\mathcal{L}_{\text{contr}}^w$. Let the to-be-controlled *plant behavior* be described by

$$\mathcal{P} := \{w : \mathbb{Z} \rightarrow \mathbb{R}^w \mid w \text{ satisfies the plant equations}\}$$

and a to-be-designed controller defined by the *control behavior*

$$\mathcal{C} := \{w : \mathbb{Z} \rightarrow \mathbb{R}^w \mid w \text{ satisfies the controller equations}\}.$$

The interconnection of the plant and the controller through the w denoted by $\mathcal{P} \wedge_w \mathcal{C}$ results in the w 's obeying both the laws of the plant and the controller. Therefore the *controlled behavior* is defined by

$$\mathcal{D} := \{w : \mathbb{Z} \rightarrow \mathbb{R}^w \mid w \in \mathcal{P} \text{ and } w \in \mathcal{C}\} = \mathcal{P} \cap \mathcal{C}.$$

It has been shown in [12], Theo.1 p. 62 that a controller \mathcal{C} implementing \mathcal{D} exists iff $\mathcal{D} \subseteq \mathcal{P}$.

Let $\mathfrak{N}_{\mathcal{P}}, \mathfrak{N}_{\mathcal{C}}$ and $\mathfrak{N}_{\mathcal{D}}$ be the module of annihilators associated with \mathcal{P}, \mathcal{C} and \mathcal{D} , respectively. To prove necessary and sufficient conditions for \mathcal{C} to implement \mathcal{D} via full interconnection consider the follow lemmas.

Lemma 2: Let $R_C \in \mathbb{R}^{c \times w}[\xi]$, $R_P \in \mathbb{R}^{p \times w}[\xi]$ and $R_D \in \mathbb{R}^{g \times w}[\xi]$ where $c, p, g \in \mathbb{N}$, be such that $\mathcal{C} = \ker(R_C(\sigma))$, $\mathcal{P} = \ker(R_P(\sigma))$ and $\mathcal{D} = \ker(R_D(\sigma))$. Then the following statements are equivalent,

- 1) $\mathfrak{N}_{\mathcal{P}} + \mathfrak{N}_{\mathcal{C}} = \mathfrak{N}_{\mathcal{D}}$
- 2) there exist $F_1 \in \mathbb{R}^{g \times c}[\xi]$ and $F_2 \in \mathbb{R}^{g \times p}[\xi]$ such that $F_1 R_C + F_2 R_P = R_D$.

Lemma 3: Let r_1, \dots, r_p and c_1, \dots, c_g be bases generators of $\mathfrak{N}_{\mathcal{P}}$ and $\mathfrak{N}_{\mathcal{C}}$, respectively. Assume that $\mathfrak{N}_{\mathcal{P}} + \mathfrak{N}_{\mathcal{C}} = \mathfrak{N}_{\mathcal{D}}$, then $\{r_1, \dots, r_g, c_1, \dots, c_g\}$ is a basis of $\mathfrak{N}_{\mathcal{D}}$ iff $\mathfrak{N}_{\mathcal{P}} \cap \mathfrak{N}_{\mathcal{C}} = \{0\}$.

In the following theorem we prove necessary and sufficient conditions for \mathcal{C} to implement \mathcal{D} via full interconnection.

Theorem 1: Let $\mathcal{C} = \ker(R_C(\sigma))$, $\mathcal{P} = \ker(R_P(\sigma))$ and $\mathcal{D} = \ker(R_D(\sigma))$. Assume that R_D, R_P and R_C induce minimal representations, and that $\mathfrak{N}_{\mathcal{P}} \cap \mathfrak{N}_{\mathcal{C}} = \{0\}$. Then a controller \mathcal{C} implements \mathcal{D} iff $\mathfrak{N}_{\mathcal{P}} + \mathfrak{N}_{\mathcal{C}} = \mathfrak{N}_{\mathcal{D}}$.

Proof: (Only if) Assume that \mathcal{C} implements \mathcal{D} , then $\mathcal{C} \cap \mathcal{P} = \ker(\begin{bmatrix} R_C(\sigma) \\ R_P(\sigma) \end{bmatrix})$. Since $\mathcal{D} = \ker(R_D(\sigma))$ then $\ker(R_D(\sigma)) = \ker(\begin{bmatrix} R_C(\sigma) \\ R_P(\sigma) \end{bmatrix})$. Therefore there exists $F \in \mathbb{R}^{p \times c}[\xi]$ such that $R_D = F \begin{bmatrix} R_C \\ R_P \end{bmatrix}$. Partition the columns of $F := [F_1 \ F_2]$ accordingly with respect to the rows of R_C and R_P . Then $R_D = F_1 R_C + F_2 R_P$. Now it follows from Lemma 2 that $R_D = F_1 R_C + F_2 R_P$ which implies that $\mathfrak{N}_{\mathcal{P}} + \mathfrak{N}_{\mathcal{C}} = \mathfrak{N}_{\mathcal{D}}$. (If) From Lemma 2 $\mathfrak{N}_{\mathcal{P}} + \mathfrak{N}_{\mathcal{C}} = \mathfrak{N}_{\mathcal{D}}$ implies that there exist $F_1 \in \mathbb{R}^{g \times c}[\xi]$ and $F_2 \in \mathbb{R}^{g \times p}[\xi]$ such that $F_1 R_C + F_2 R_P = R_D$. Now, $R_D = [F_1 \ F_2] \begin{bmatrix} R_C \\ R_P \end{bmatrix}$ with $[F_1 \ F_2] \in \mathbb{R}^{g \times (c+p)}[\xi]$. By the assumption that R_D, R_P and R_C are minimal, and that $\mathfrak{N}_{\mathcal{P}} \cap \mathfrak{N}_{\mathcal{C}} = \{0\}$ then $c + p = g$ moreover, since $\mathfrak{N}_{\mathcal{D}} = \mathfrak{N}_{\mathcal{P}} + \mathfrak{N}_{\mathcal{C}}$ then $[F_1 \ F_2]$ is unimodular. Consequently, $\ker(R_D(\sigma)) = \ker(\begin{bmatrix} R_C(\sigma) \\ R_P(\sigma) \end{bmatrix})$ which implies that $\mathcal{D} = \mathcal{P} \cap \mathcal{C}$. \blacksquare

IV. DATA-DRIVEN FULL INTERCONNECTION

We state the data-driven full interconnection problem and present our solution.

Problem 1: Let $T \in \mathbb{N}$ be “sufficiently large”. Given sufficiently informative trajectories $\tilde{w} \in \mathcal{P}$ and $\tilde{w}_d \in \mathcal{D}$, both of length T . Find a minimal representation of \mathcal{C} such that $\mathcal{P} \wedge_w \mathcal{C} = \mathcal{D}$.

Let $\mathfrak{N}_{\mathcal{P}}, \mathfrak{N}_{\mathcal{C}}$ and $\mathfrak{N}_{\mathcal{D}}$ be the module of annihilators of \mathcal{P}, \mathcal{C} and \mathcal{D} , respectively. Under assumption of Theo. 1, to find \mathcal{C} we first find bases generators of $\mathfrak{N}_{\mathcal{P}}$ and $\mathfrak{N}_{\mathcal{D}}$. Then, under the assumptions of Lemma 3, we compute a basis generator for $\mathfrak{N}_{\mathcal{C}}$. To find bases of $\mathfrak{N}_{\mathcal{P}}$ and $\mathfrak{N}_{\mathcal{D}}$ we use the fact that \tilde{w} and \tilde{w}_d are sufficiently informative, therefore $\text{leftkernel}(\mathfrak{H}_L(\tilde{w})) = \tilde{\mathfrak{N}}_{\mathcal{P}}^L$ and $\text{leftkernel}(\mathfrak{H}_L(\tilde{w}_d)) = \tilde{\mathfrak{N}}_{\mathcal{D}}^L$ where $L \in \mathbb{Z}_+$ is greater than both $L(\mathcal{P})$ and $L(\mathcal{D})$. A procedure for finding minimum lag bases generators has been illustrated in Algorithm 2, p. 679 of [7].

Our solution to Problem 1 is summarised in Algorithm 1. Note that in Algorithm 1 we denote by $\mathfrak{N}_{\mathcal{C}}^n$ a set of annihilators of \mathcal{C} of degree n .

Remark 1: In Problem 1, we assumed that observed trajectories are of sufficiently large length T , whereas Algorithm 2, p. 679 of [7] is under the assumptions that observed trajectories are of infinite length. This brings about the issues of how large is sufficiently large and of consistency. We do not address these issues in this paper, but reserve them for future research, along with the effect of noise on observed data.

We now prove the correctness of Algorithm 1.

Proposition 1: Let $\tilde{w} \in \mathcal{P}$ and $\tilde{w}_d \in \mathcal{D}$ be sufficiently informative about their respective behaviors. Assume that r_1, \dots, r_g and a_1, \dots, a_t in Algorithm 1 are minimum lag bases of $\mathfrak{N}_{\mathcal{P}}$ and $\mathfrak{N}_{\mathcal{D}}$, respectively, and that \mathcal{C} implements \mathcal{D} then $\mathfrak{N}_{\mathcal{C}}$ in Algorithm 1 is a module of annihilators of \mathcal{C} that implements \mathcal{D} .

Proof: The fact that r_1, \dots, r_g and a_1, \dots, a_t in Algorithm 1 are minimum lag bases of $\mathfrak{N}_{\mathcal{P}}$ and $\mathfrak{N}_{\mathcal{D}}$ follows from Theo. 14, p. 679 of [7]. Furthermore, the fact that \mathcal{C} implements \mathcal{D} follows from Theo. 1. Now, let $a_{l'_1}, \dots, a_{l'_q}$ and r_{l_1}, \dots, r_{l_k} as in step 1 of Algorithm 1. Denote by $\mathfrak{N}_{\mathcal{D}}^n$ and $\mathfrak{N}_{\mathcal{P}}^n$ a set containing $a_{l'_1}, \dots, a_{l'_q}$ and r_{l_1}, \dots, r_{l_k} , respectively and $\mathfrak{N}_{\mathcal{C}}^n$ set of annihilators of \mathcal{C} of degree n . Since a_1, \dots, a_t is a basis of $\mathfrak{N}_{\mathcal{D}}$ then $\mathfrak{N}_{\mathcal{C}} \cap \mathfrak{N}_{\mathcal{D}} = \{0\}$ which implies that $\mathfrak{N}_{\mathcal{C}}^n \cap \mathfrak{N}_{\mathcal{P}}^n = \{0\}$ therefore in Algorithm 1 if $k = q$ then $a_{l'_1}, \dots, a_{l'_q} \in \mathfrak{N}_{\mathcal{P}}^n$. Hence, $\mathfrak{N}_{\mathcal{C}}^n = \{0\}$. Now, if $k = 0$ and $q \neq 0$, then $a_{l'_1}, \dots, a_{l'_q} \in \mathfrak{N}_{\mathcal{D}}^n$ such that $a_{l'_1}, \dots, a_{l'_q} \notin \mathfrak{N}_{\mathcal{P}}^n$ implies that $a_{l'_1}, \dots, a_{l'_q} \in \mathfrak{N}_{\mathcal{C}}^n$, therefore $\mathfrak{N}_{\mathcal{C}}^n = \{a_{l'_1}, \dots, a_{l'_q}\}$. Finally, $k < q$ means $\mathfrak{N}_{\mathcal{D}}^n$ has more annihilators of degree n than $\mathfrak{N}_{\mathcal{P}}^n$, therefore some of them belong to $\mathfrak{N}_{\mathcal{C}}^n$. Denote by $\tilde{\mathfrak{N}}_{\mathcal{P}}^n$ and $\tilde{\mathfrak{N}}_{\mathcal{D}}^n$ sets containing $\tilde{a}_{l'_1}, \dots, \tilde{a}_{l'_q}$ and $\tilde{r}_{l_1}, \dots, \tilde{r}_{l_k}$, respectively. Since $\mathfrak{N}_{\mathcal{C}}^n \cap \tilde{\mathfrak{N}}_{\mathcal{P}}^n = \{0\}$ then $\mathfrak{N}_{\mathcal{C}}^n \cap \tilde{\mathfrak{N}}_{\mathcal{D}}^n = \{0\}$. Moreover, $\mathfrak{N}_{\mathcal{P}} + \mathfrak{N}_{\mathcal{C}} = \mathfrak{N}_{\mathcal{D}}$ implies that $\mathfrak{N}_{\mathcal{P}}^n + \mathfrak{N}_{\mathcal{C}}^n = \mathfrak{N}_{\mathcal{D}}^n$ hence $\tilde{\mathfrak{N}}_{\mathcal{P}}^n + \tilde{\mathfrak{N}}_{\mathcal{C}}^n = \tilde{\mathfrak{N}}_{\mathcal{D}}^n$. Since $\tilde{\mathfrak{N}}_{\mathcal{C}}^n \cap \tilde{\mathfrak{N}}_{\mathcal{P}}^n = \{0\}$, $\tilde{\mathfrak{N}}_{\mathcal{P}}^n + \tilde{\mathfrak{N}}_{\mathcal{C}}^n = \tilde{\mathfrak{N}}_{\mathcal{D}}^n$, and $\tilde{r}_{l_1}, \dots, \tilde{r}_{l_k}$ is a basis of $\tilde{\mathfrak{N}}_{\mathcal{P}}^n$ then the projection matrix P exists and $\tilde{u}_1^\top, \dots, \tilde{u}_x^\top$ are the coefficients vectors of annihilators of \mathcal{C} of lag n . Hence

Input : $\tilde{w} \in \mathcal{P}$ and $\tilde{w}_d \in \mathcal{D}$

Output : $\mathfrak{N}_{\mathcal{C}}$

Assumptions: Theorem 1 and Lemma 3

- 1 Determinations of bases of $\mathfrak{N}_{\mathcal{P}}$ and $\mathfrak{N}_{\mathcal{D}}$
 - i. Using Algorithm 2, p. 679 of [7] determine minimum lag bases r_1, \dots, r_g and a_1, \dots, a_t of $\mathfrak{N}_{\mathcal{P}}$ and $\mathfrak{N}_{\mathcal{D}}$, respectively.
 - ii. Define $\tilde{r}_1, \dots, \tilde{r}_g$ and $\tilde{a}_1, \dots, \tilde{a}_t$ as the coefficients of r_1, \dots, r_g and a_1, \dots, a_t respectively.
 - iii. Define $d_m := \deg(a_m)$ for $m = 1, \dots, t$, $\mathfrak{t} := \{1, 2, \dots, t\}$ and $\mathfrak{g} := \{1, 2, \dots, g\}$. Let $d = \max(d_1, \dots, d_m)$.
- 2 Compute steps 3-4 recursively starting from $n = 0$ to d .
- 3 Classifying $\tilde{r}_1, \dots, \tilde{r}_g$ and $\tilde{a}_1, \dots, \tilde{a}_t$ by their lags
 - i. choose $l_1, \dots, l_k \in \mathfrak{g}$ such that $\tilde{r}_{l_1}, \dots, \tilde{r}_{l_k}$ are all of lag n . If there is no $\tilde{r}_{l_1}, \dots, \tilde{r}_{l_k}$ of lag n set $k = 0$.
 - ii. choose $l'_1, \dots, l'_q \in \mathfrak{t}$ such that $\tilde{a}_{l'_1}, \dots, \tilde{a}_{l'_q}$ are all of lag n . If there is no $\tilde{a}_{l'_1}, \dots, \tilde{a}_{l'_q}$ of lag n set $q = 0$.
- 4 Compute coefficients of $\mathfrak{N}_{\mathcal{C}}^n$ as follows
 - if** $k = q$ **then**
 $\mathfrak{N}_{\mathcal{C}}^n := \{0\}$
 - else if** $k = 0$ and $q \neq 0$ **then**
 $\tilde{a}_{l'_1}, \dots, \tilde{a}_{l'_q}$ defines the coefficients of annihilators of \mathcal{C} of degree n , therefore define $\mathfrak{N}_{\mathcal{C}}^n := \{a_{l'_1}, \dots, a_{l'_q}\}$.
 - else if** $k < q$ **then** Define the matrix A whose columns are $\tilde{r}_{l_1}, \dots, \tilde{r}_{l_k}$ as
$$A := \begin{bmatrix} \tilde{r}_{0_{l_1}} & \dots & \tilde{r}_{0_{l_k}} \\ \vdots & \dots & \vdots \\ \tilde{r}_{n_{l_1}} & \dots & \tilde{r}_{n_{l_k}} \end{bmatrix};$$
Define a projection matrix $P := A[A^\top A]^{-1}A^\top$;
Define $H := [\tilde{a}_{l'_1} - P\tilde{a}_{l'_1}, \dots, \tilde{a}_{l'_q} - P\tilde{a}_{l'_q}]$;
Compute x rank of H and compute the SVD of $H = U\Sigma V^\top$;
Partition $U = [U_1 \ U_2]$ where U_1 has x columns;
The columns of $U_1, \tilde{u}_1^\top, \dots, \tilde{u}_x^\top$ defines the coefficients of annihilators of \mathcal{C} of degree n , therefore define $\mathfrak{N}_{\mathcal{C}}^n := \{u_1, \dots, u_x\}$;
 - end** ;
- 5 Specification of $\mathfrak{N}_{\mathcal{C}}$
 - i. Define $\mathfrak{N}_{\mathcal{C}} := \bigcup_{k=0}^d \mathfrak{N}_{\mathcal{C}}^k$

Algorithm 1: Solution of Problem 1

$$\mathfrak{N}_{\mathcal{C}}^n = \{u_1, \dots, u_x\}.$$

V. EXAMPLE

We consider a simple example of power factor rectification. Let the circuit in Fig. 1 be the to-be-controlled system with $w = \text{col}(i_z, i_v, i_s, v)$, $\mathfrak{m}(\mathcal{P}) = 2$ and $\mathfrak{p}(\mathcal{P}) = 2$. The input/output variables are i_s, v and i_z, i_s , respectively. To generate $\tilde{w} \in \mathcal{P}$ with $T = 200000$ samples, the circuit in Fig. 1 is simulated in Matlab Simulink with sampling rate of $5\mu\text{s}$. To guarantee that \tilde{w} is sufficiently informative i_s and v are generated by current and voltage sources which are driven by a random number generator so that both are persistently exciting of sufficiently high order. The values of R, L and C are $100\Omega, 0.01\text{H}$ and 0.001C , respectively.

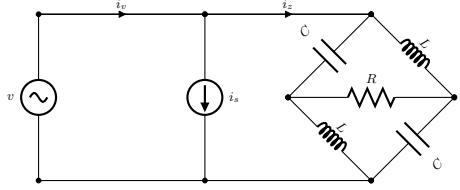


Fig. 1. To-be controlled system

The controlled system, i.e. circuit with the correct power factor, is chosen as in Fig. 2. $w_d = \text{col}(i_z, i_v, i_s, v)$, with $\mathfrak{m}(\mathcal{D}) = 1$ and $\mathfrak{p}(\mathcal{D}) = 3$. To generate $\tilde{w}_d \in \mathcal{D}$ the circuit in Fig. 2 is simulated like the one above but this time with only v generated by voltage sources which is driven by a random number generator. The values of R, L and C are the same while $L_f = 0.001\text{H}$ and $R_f = 0.4252\Omega$

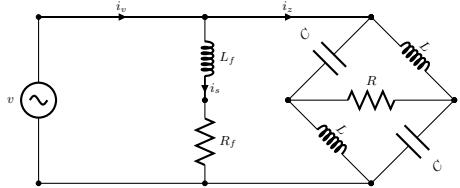


Fig. 2. Example of controlled system

Using Algorithm 1, $\mathfrak{N}_{\mathcal{P}}$ has 2 basis generators, one of degree 0 and the other 2. $\mathfrak{N}_{\mathcal{D}}$ has 3 basis generators, one of degree 0, and others of degree 1 and 2. Hence, the generator of $\mathfrak{N}_{\mathcal{D}}$ of degree 1 belongs to $\mathfrak{N}_{\mathcal{C}}$. Consequently, a controller representation is

$$\begin{bmatrix} -\frac{322\sigma}{1611} + \frac{266}{1155} & \frac{322\sigma}{1611} - \frac{226}{1155} & -\frac{965\sigma}{2414} + \frac{452}{1155} & -\frac{151\sigma}{10180} - \frac{151}{10180} \end{bmatrix} \begin{bmatrix} i_z \\ i_v \\ i_s \\ v \end{bmatrix} = 0$$

We verify the controller above by interconnecting it with the to-be-controlled systems then comparing the impulse response with that of the controlled system. The impulse responses coincide as shown in Fig. 3.

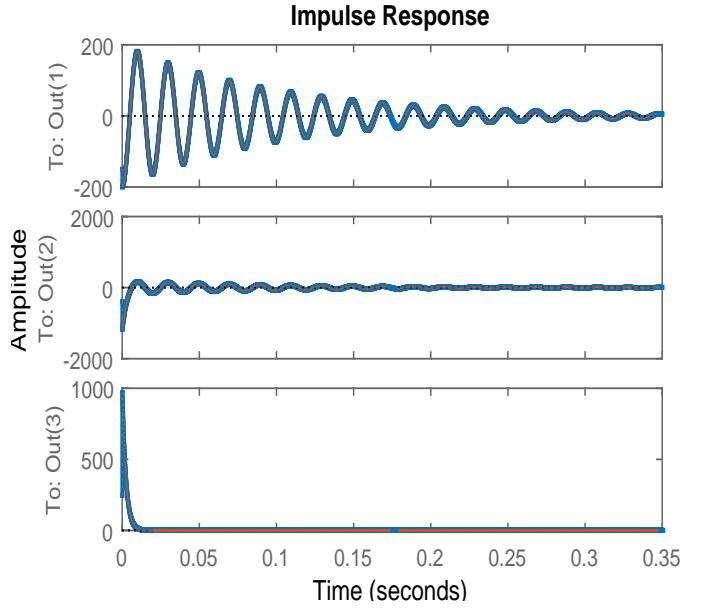


Fig. 3. Impulse responses of the to-be-controlled system interconnected with computed controller (blue) and that of the controlled system (red)

VI. CONCLUSIONS

We have proved necessary and sufficient data-driven conditions for a controller to implement the desired controlled behavior via full interconnection. Then, under those conditions, we illustrated how the controller can be computed directly from data. As a matter of future research we intend to investigate whether such data-driven approach can be extended to two-dimensional systems and be applied to boundary condition control problems.

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