FILE
ID102.

INTERNAL DOCUMENT 238

I.O.S.

SEADATA MONITOR SYSTEMS

K.G. BIRCH

June 1985

[*This document should not be cited in a published bibliography, and is supplied for the use of the recipient only*].

NATURAL ENVIRONMENT RESEARCH COUNCIL

INSTITUTE OF OCEANOGRAPHIC SCIENCES

INSTITUTE OF OCEANOGRAPHIC SCIENCES

Wormley, Godalming,
Surrey GU8 5UB
(042-879-4141)

(Director: Dr. A. S. Laughton, FRS)

Bidston Observatory,
Birkenhead,
Merseyside L43 7RA
(051-653-8633)
(Assistant Director: Dr. D. E. Cartwright, FRS)

SEADATA MONITOR SYSTEMS

K.G. BIRCH
June 1985

Internal Document No. 238

Institute of Oceanographic Sciences,
Wormley, Godalming, Surrey GU8 5UB.

INDEX

Seadata Monitors

Introduction

Many oceanographic systems use Seadata Cassette Loggers, but to be able to test and calibrate the equipment prior to recording periods it is necessary to be able to read the data passed to the logger easily and quickly. Monitors are commercially available but do not provide the flexibility necessary for in-house developments and are expensive.

The first hardware display system was built to assist in the development of the I.O.S. Vector Averaging Electromagnetic Current Meter (VAECM), but it has been used in several applications. This has now been complemented by a computer based display system which allows for the data to be processed to a directly useable value, i.e. addition of calibration constants, etc.

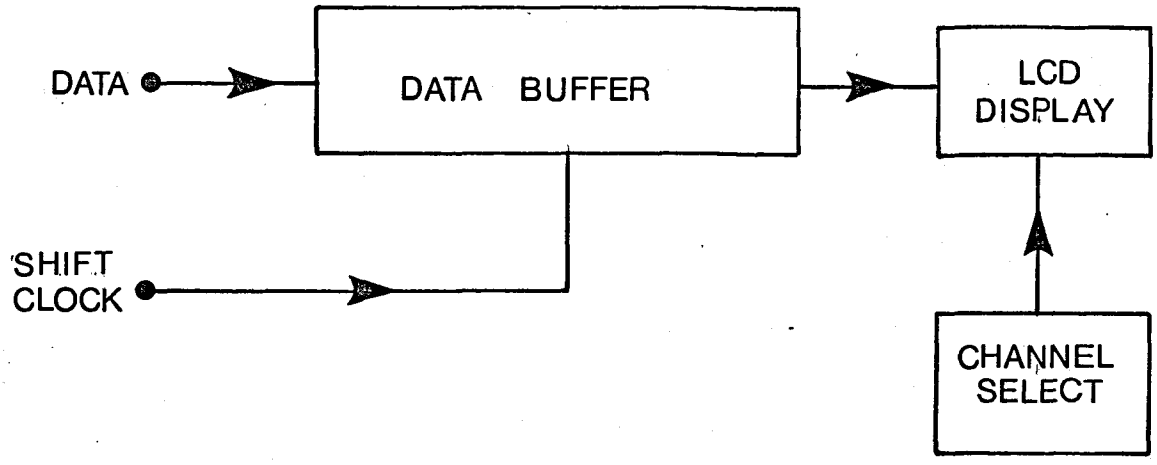
Hardware System Description

The hardware design performs in two functional modes (see figures 1 & 2), the input of data (mode 1) and the display of selected data within the data frame (mode 2).

The data input to the monitor is obtained from the serial data line to the Seadata logger. The Seadata shift clock, initiated by the user's system's record request command, is used to clock the system's data into the logger registers and into the monitor's 284 bit buffer simultaneously. At the end of each data record, or upon the update switch being pressed, the 4 hex digit LCD display is updated with the $4N^{th}$, $(4N+1)^{th}$, $(4N+2)^{th}$ and $(4N+3)^{th}$ nibbles of data, where N is selected by two hex thumbwheel switches (N=0 being the first word of the record). Whilst in the display mode the data is recirculated giving the facility to read 4 nibble "data words" in any order until the next data frame is available.

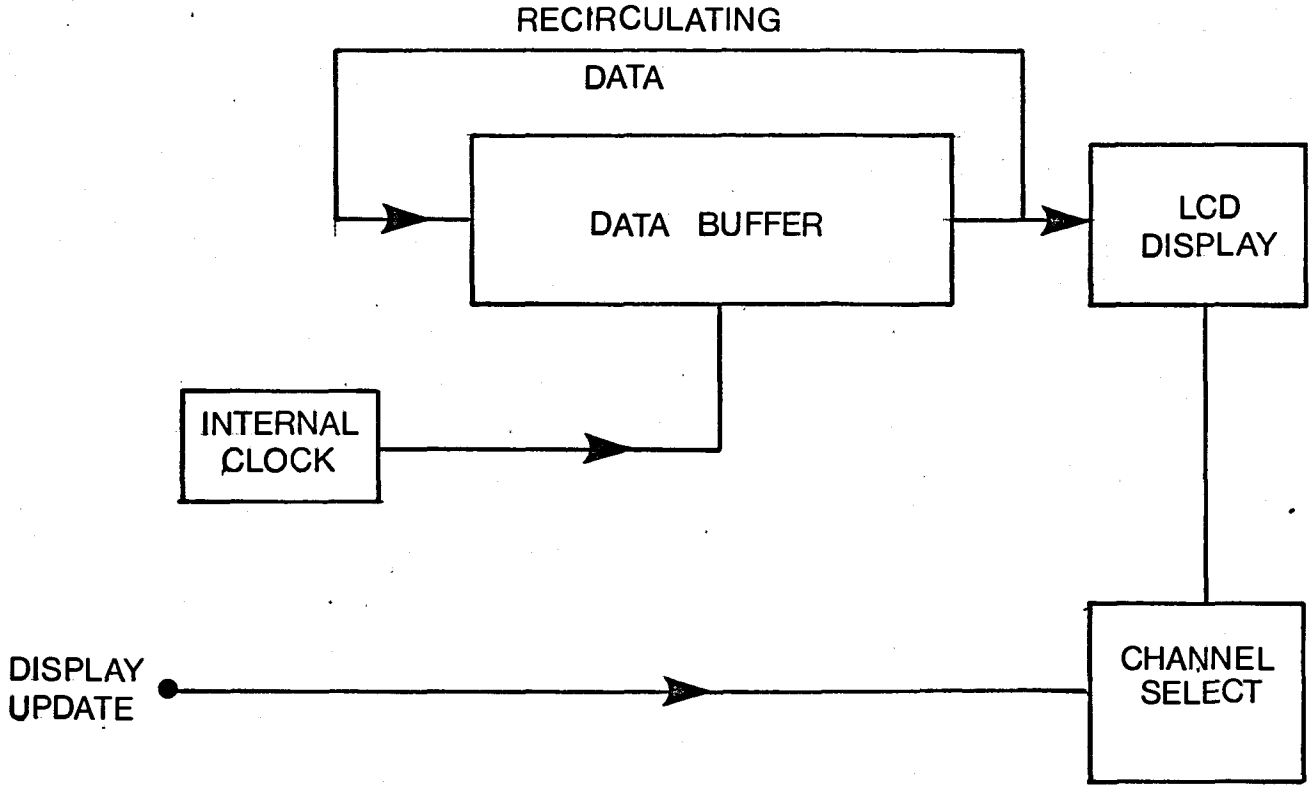
The hardware does not need any prior knowledge of the length of the data stream, but it assumes that the data words will be 16 bits long; up to

MODE 1



DATA INPUT - FIGURE 1

MODE 2



DATA DISPLAY - FIGURE 2

24 data words can be accommodated.

The input of a new data frame has priority over the display of data and updating of the display is inhibited during the acquisition period.

Circuit Description

The input of data is controlled by the Seadata Logger Shift Clock which presents the data in 4 bit serial nibbles to the data buffer. The first shift clock pulse resets the latch IC 5a; this inhibits the data recirculation by disabling IC 1 gate b and the update switch via IC 4 gate d. Latch IC 5a also enables IC 1 gate a, allowing the data to enter the data buffer via IC 1 gate c.

The data buffer ICs 7, 8 and 9 are dual 64 bit serial input/output shift registers with IC 2 gates a/b and c/d providing delays for the data clock. The first shift clock pulse also triggers IC 12, a retriggerable monostable, whose Q output is differentiated to generate the reset for the word counter IC 16 and the preset enable for IC 10 & 23 which determine the position of the data in the buffer. The $\bar{Q}$ of IC 12 is buffered by IC 19 a & b to drive a bugger to indicate a new data frame. The differentiated $\bar{Q}$ of IC 12 is used to generate a new display cycle, updating the previously selected data word immediately the data input mode is completed.

There is no inbuilt knowledge of the length of the data frame, therefore it is necessary for the circuitry to compute the exact location of the data within the data buffer. This is achieved by dividing the Seadata clock by 16 in IC 16 whose Q4 output clocks down IC 10 & 23, which are preset to 18 HEX (24 DECIMAL) at the start of each new data frame input mode. The binary value on the outputs of IC 10, 23 after the input mode is completed represents the location of the start of the new data record within the buffer. By adding this binary offset to the data word selected on the front panel thumbwheel switches, using two four bit adders ICs 13 & 14, the number of 16 bit words in the buffer which have to be skipped is

obtained.

The display of data is achieved by two methods. There is the automatic update of the previously selected word (as mentioned earlier) and the display of any word selected by the operator. The two methods differ only in the source of the update command. Whether automatic or operator demand, the update initiate signals are OR diode gated D2 & D3 to cause the display to be refreshed.

In the update mode, after the channel has been selected the position is calculated by IC 13 & 14, the depressing of the update button sets IC 5a. The binary position of the data in the buffer i.e. outputs IC 13 & 14 is preset into IC 11 on the positive going edge of the $\bar{Q}$ output of IC 5b (IC 5b is a monostable, triggered by the differentiated $\bar{Q}$ output of IC 5a). The setting of IC 5a enables IC 6 gate d, which causes the free running astable composed of IC 4 gates a, b and c (recirculating clock) to clock the data buffer. The data is recirculated via IC 1 gate b, which is enabled when IC 5a is set.

The recirculating clock is counted by IC 15 whose Q4 output is used to clock IC 11, a binary down counter, and the Q8 and Q9 outputs are gated by IC 1 to reset IC 5a at the completion of a display update, i.e. after a complete recirculation of the 284 bit register. The carry output of IC 11 pin 14 gates the recirculating clock at IC 4 gate c, so that the selected data is clocked into IC 25 (serial/parallel converter). This gated clock is counted by IC 24 whose Q2 output clocks IC 27, a Johnson counter. The first four outputs from IC 27 go high consecutively after the respective nibbles of data have been clocked into IC 25. The outputs of IC 27 are differentiated to provide the digit selects for the Liquid Crystal Display driver, ICL 7211, at times when the 4 data digits are present at the parallel outputs of IC 25.

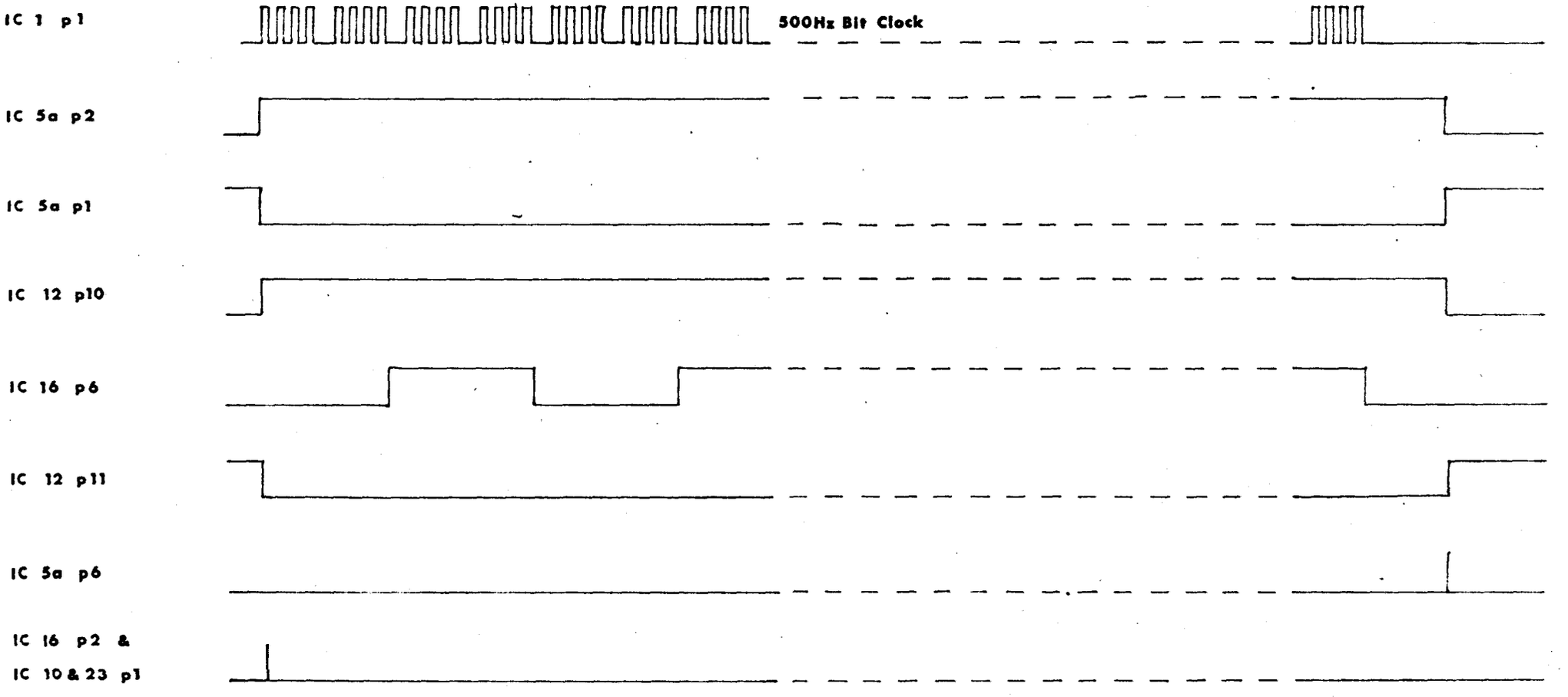
Power Supplies

The most practical method of ensuring compatibility between signal voltage levels (clock and data) is to use the instrument under test to provide the supply to the monitor unit. The alternative is to use an internal supply (battery if portability is required), but in both cases the value of R1 and R3 will have to be adjusted to suit.

When using the instrument supply, R1 should be set to 10k, R3 to 0 and C1 to 1n0. Using an internal supply the voltage swing of the input signals must be adjusted (using R1, R2 and R3, R4 as potential dividers), so that the voltage levels as measured across R2 and R4 do not exceed the digital supply of the monitor unit. C1 is used to delay the data by about 5-10 microseconds relative to the clock; typical delay = $0.7\ C1\ \frac{R1R2}{(R1+R2)}$

It should also be noted that the input voltage levels must not be lower than the digital supply as no provision is made for increasing the input signal levels.

Mode 1 – Data Input



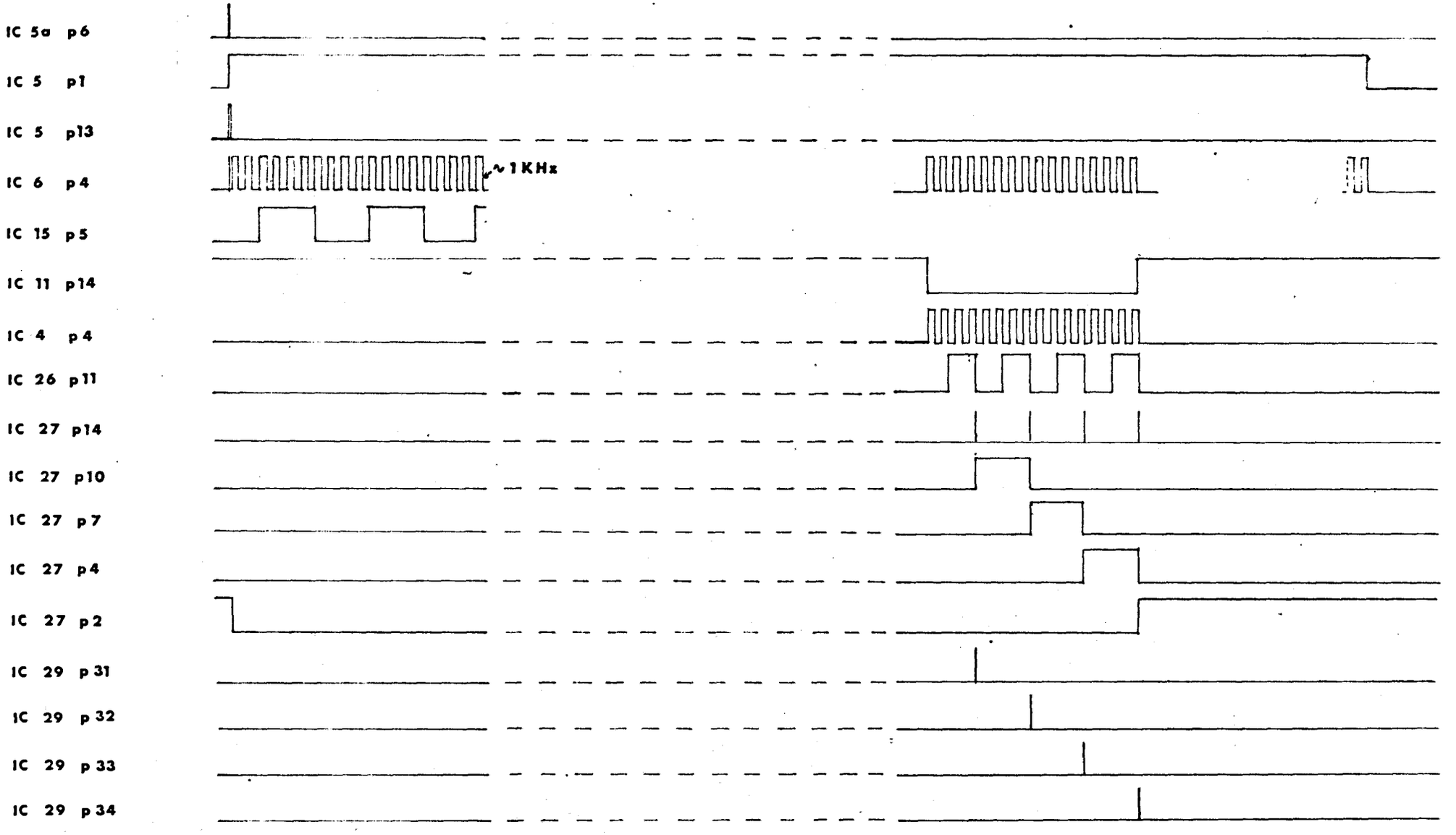
...ITUTE OF OCEANOGRAPHIC SCIENCES

TITLE

Seadata Monitor

Timing dia. 1

Mode 2 – Data Display

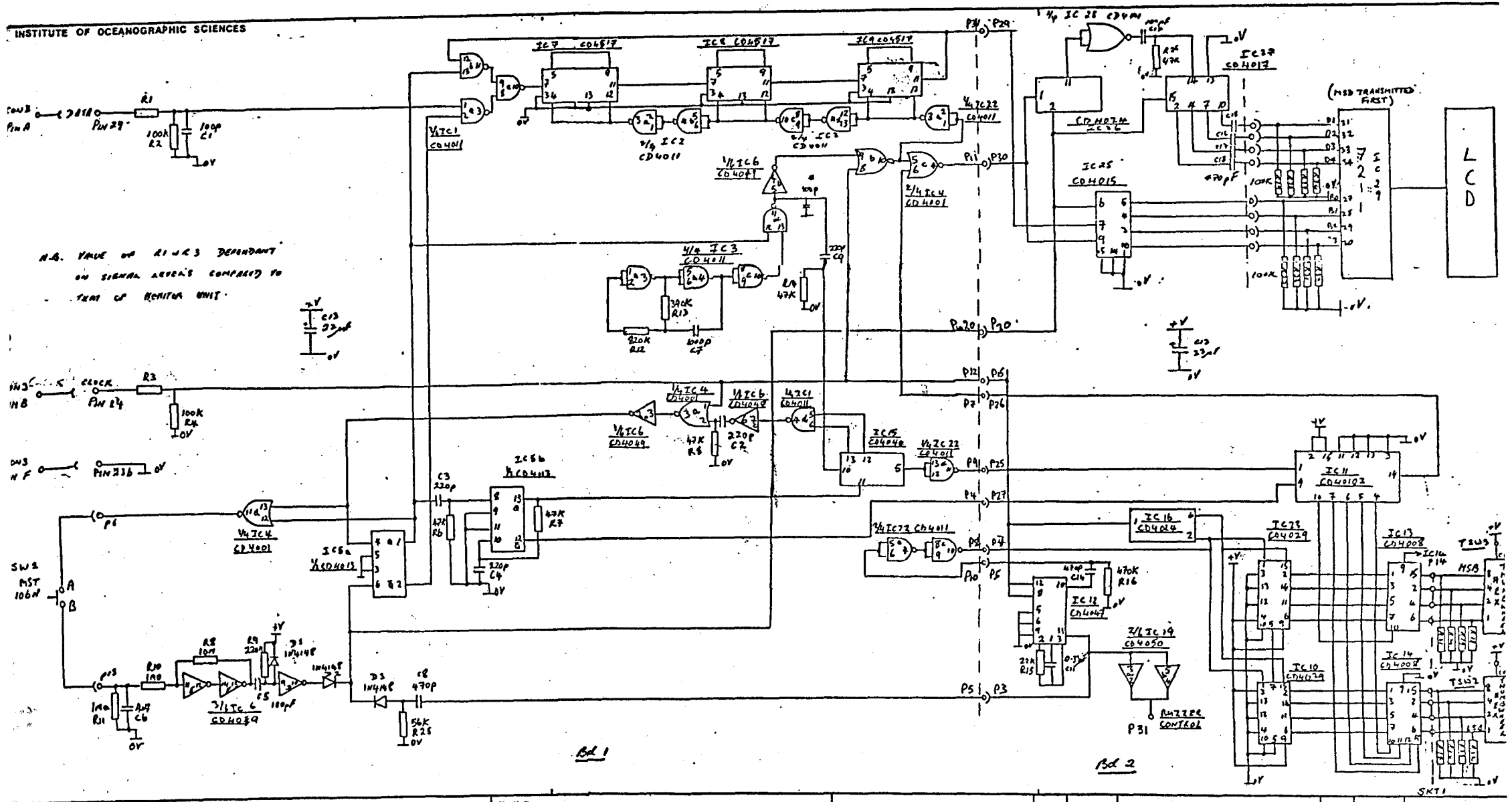


INSTITUTE OF OCEANOGRAPHIC SCIENCES

TITLE

Seadata Monitor

Timing dia. 2



INSTITUTE OF OCEANOGRAPHIC SCIENCES	TITLE: SEA DATA MONITOR UNIT (EUROCARD VERSION)						CIRCUIT No.
		100p" DEGLITCH PREVIOUSLY ADDED		8/7/82			
		DIGIT SELECT REVERSE ORDER		8/7/82			
		LINKED 4008 CARRY IN/OUT		8/7/82			SHEET No.
		AMENDMENT	ISSUE	DATE	AMENDMENT	ISSUE	DATE

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	▲ TRADE OR SUPPLIERS NAME	REFERENCE No.	
IC1	INTEGRATED CIRCUIT			CD 4011 BE	R.C.A		
IC2	— " —			CD 4011 BE	"		
IC3	— " —			CD 4011 BE	"		
IC4	— " —			CD 4001 BE	"		
IC5	— " —			CD 4013 BE	"		
IC6	— " —			CD 4049 BE	"		
IC7	— " —			CD 4517 BE	"		
IC8	— " —			CD 4517 BE	"		
IC9	— " —			CD 4517 BE	"		
IC10	— " —			CD 4029 BE	"		
IC11	— " —			CD 40103 BE	"		
IC12	— " —			CD 4047 BE	"		
IC13	— " —			CD 4008 BE	"		
IC14	— " —			CD 4008 BE	"		
IC15	— " —			CD 4040 BE	"		
IC16	— " —			CD 4024 BE	"		
IC23	— " —			CD 4029 BE	"		
IC25	— " —			CD 4015 BE	"		
IC26	— " —			CD 4024 BE	"		
IC27	— " —			CD 4017 BE	"		
IC28	— " —			CD 4001 BE	"		
IC29	— " —			7211	INTERSIL	FARNELL CODE 7211IPL	
LCD 1	LIQUID CRYSTAL DISPLAY				R.S. COMPONENTS	STK No 587-305	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

SEADATA MONITOR UNIT (EUROCARD VERSION) LCD

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S./

COMPILED BY KJB DATE 10/6/85 SHEET No. 1

ISSUED FOR ORDER No. FOR UNITS

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
R1	RESISTOR	100K	1/4 W	METAL FILM MR 25	WELWYN		
R2	"	100K	"	"	"		
R3	"	100K	"	"	"		
R4	"	100K	"	"	"		
R5	"	47K	"	"	"		
R6	"	47K	"	"	"		
R7	"	47K	"	"	"		
R8	"	10M	1/2 W	CARBON FILM CFR	"		
R9	"	220K	1/4 W	METAL FILM MR25	"		
R10	"	1MΩ	"	"	"		
R11	"	1MΩ	"	"	"		
R12	"	820K	"	"	"		
R13	"	390K	"	"	"		
R14	"	47K	"	"	"		
R15	"	22K	"	"	"		
R16	"	470K	"	"	"		
R17	"	100K	"	"	"		
R18	"	100K	"	"	"		
R19	"	100K	"	"	"		
R20	"	100K	"	"	"		
R21	"	100K	"	"	"		
R22	"	100K	"	"	"		
R23	"	100K	"	"	"		
R24	"	100K	"	"	"		
R25	"	56K	"	"			

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

SEADATA MONITOR UNIT (EUROCARD VERSION) LCD

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S./

COMPILED BY K.B.S DATE 10/8/85 SHEET No. 2

ISSUED FOR ORDER No. FOR UNITS

WORKING OVELINE 0706/87

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
R26	RESISTOR	47K	1/4 WATT	METAL FILM MR25	WELWYN		
R27	"	100K	"	— " —	"		
R28	"	100K	"	— " —	"		
R29	"	100K	"	— " —	"		
R30	"	100K	"	— " —	"		
R31	"	100K	"	— " —	"		
R32	"	100K	"	— " —	"		
R33	"	100K	"	— " —	"		
R34	"	100K	"	— " —	"		
C1	CAPACITOR	100pF		FKC3 160V	WIMA		
C2	"	220pF		— " —	"		
C3	"	220pF		— " —	"		
C4	"	220pF		— " —	"		
C5	"	100pF		— " —	"		
C6	"	4700pF		— " —	"		
C7	"	1000pF		— " —	"		
C8	"	470pF		— " —	"		
C9	"	220pF		— " —	"		
C10	"	470pF		— " —	"		
C11	"	0·33μF		MKC-4 250V	"		
C12	"	22μF		TANTHALUM BEAD		RS STK No. 102-718	
C13	"	22μF		" "		— " —	
C14	"	100pF	±10%	FKC3 160V	WIMA		
C15	"	470pF		" "	"		

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

SEADATA MONITOR UNIT (EUROCARD VERSION) LCD

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S./

COMPILED BY KGB DATE 10/6/85 SHEET No. 3

ISSUED FOR ORDER No. FOR UNITS

WOKING DYELINE 0705/82

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
C16	CAPACITOR	470pF	±10%	FKC 3 160V	WIMA		
C17	"	470pF		— " —	"		
C18	"	470pF		— " —	"		
D1	DIODE	1N4148			TEXAS		
D2	"	1N4148			"		
D3	"	1N4148			"		
SW3	SWITCH	N/O CONTACTS				RS STK No 337-914	
CON 1A	PCB MOUNTED			DIN 41612 CLASS III		RS STK No 471-519	
CON 1B	CHASSIS FIXED			— " —		— " — 471-525	
CON 2A	PCB MOUNTED			— " —		— " — 471-519	
CON 2B	CHASSIS FIXED			— " —		— " — 471-525	
CON 3A	MULTIPOLE CONNECTOR			MIL-C-26482	CANNON TYPE	— " — 466-618	
CON 3B	— " —			— " —	— " —	— " — 466-646	
TSW1	THUMBWHEEL SWITCH			HEX SUB MINATURE		RS STK No 337-431	
TSW2	— " —			— " —		— " — 337-431	
	END CHEEKS			— " —		— " — 337-419	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

SEADATA MONITOR UNIT (EUROCARD VERSION) LCD

INSTITUTE OF OCEANOGRAPHIC SCIENCES

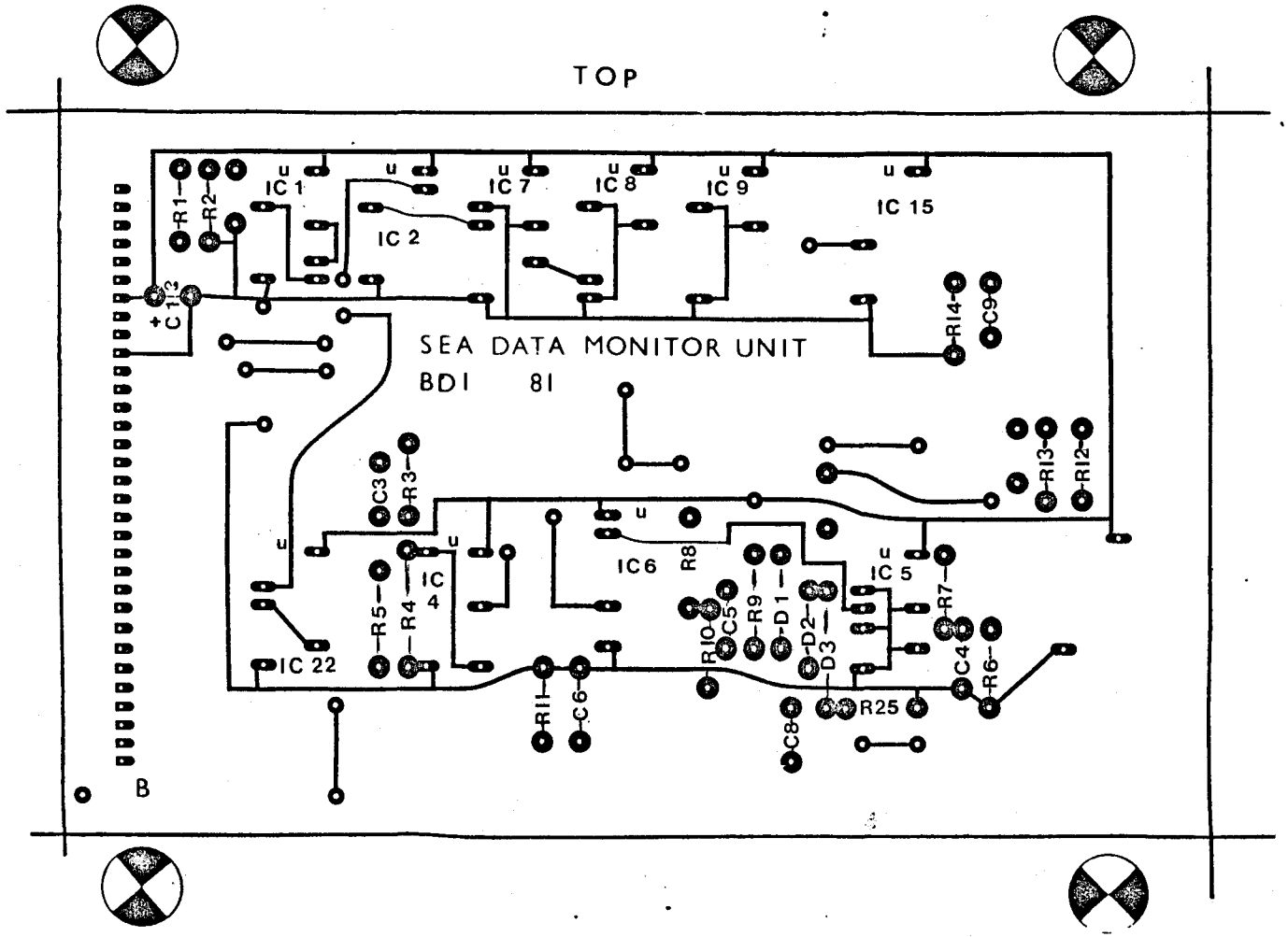
ELECTRONICS COMPONENTS FOR DRG. No. I.O.S./

COMPILED BY KJB DATE 10/6/85 SHEET No. 4

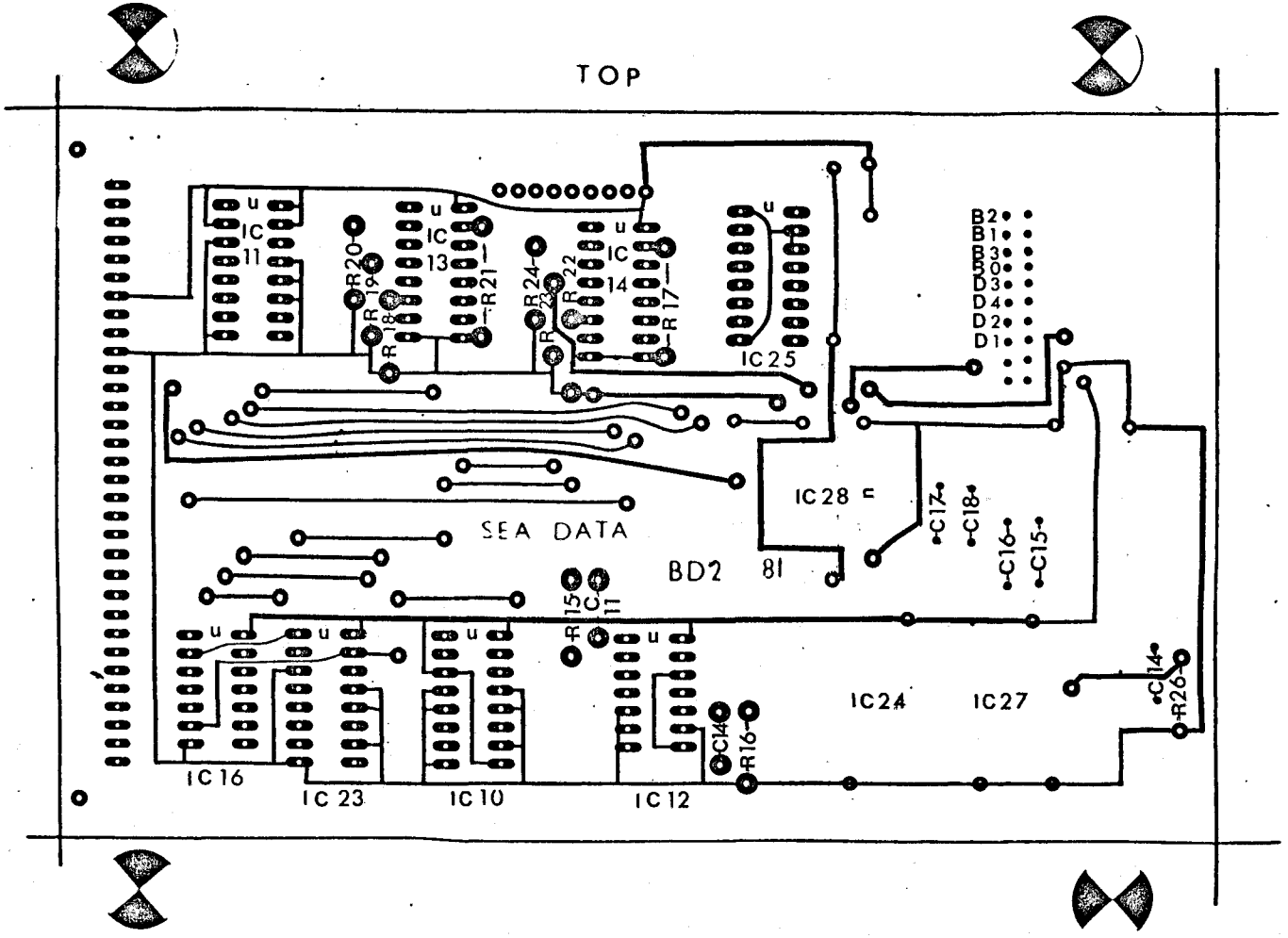
ISSUED FOR ORDER No. FOR UNITS

WOKING OYELINE 0708/82

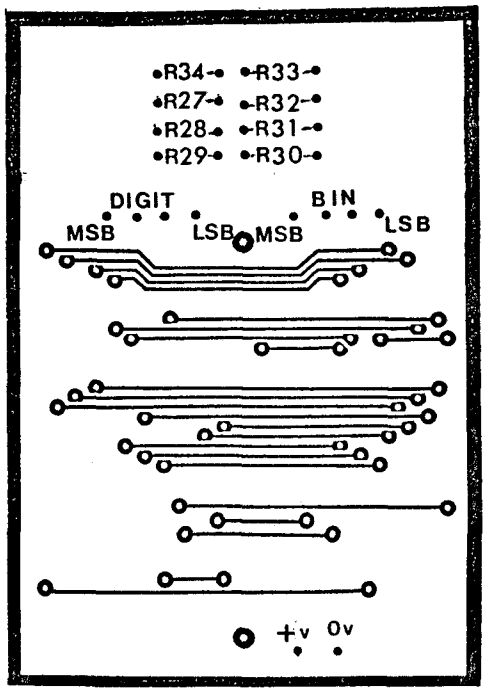
SEADATA MONITOR UNIT Bd 1



SEADATA MONITOR UNIT Bd 2



SEADATA MONITOR UNIT LIQUID CRYSTAL DISPLAY



Wiring Schedule

	Pin	Destination
Con 1 Fixed	1-3	n/c
	4	Con 2 Pin 27
Layer A	5	Con 2 Pin 3
	6	SW1 Contact A
	7	Con 2 Pin 26
	8	Con 2 Pin 7
	9	Con 2 Pin 25
	10	Con 2 Pin 5
	11	Con 2 Pin 30
	12	Con 2 Pin 15
	13	SW1 Contact B
	14	Con 3 Pin B
	15-19	n/c
	20	Con 2 Pin 20
	21,22	n/c
	23	Con 3 Pin F
	24-28	n/c
	29	Con 3 Pin A
	30	n/c
	31	Con 2 Pin 29
	32	n/c
Layer B	1-22	n/c
	23	0V
	24,25	n/c
	26	+V
	27-32	n/c

Con 2 Fixed

Layer A	1-2	n/c
	3	Con 1 Pin 5
	4	n/c
	5	Con 1 Pin 10
	6	n/c
	7	Con 1 Pin 8
	8-14	n/c
	15	Con 1 Pin 12
	16-19	n/c
	20	Con 1 Pin 20
	21,22	n/c
	24	n/c
	25	Con 1 Pin 9
	26	Con 1 Pin 7
	27	Con 1 Pin 4
	28	n/c
	29	Con 1 Pin 29
	30	Con 1 Pin 11
	31,32	n/c
Layer B	1-22	n/c
	23	0V
	24,25	n/c
	26	+V
	27-32	n/c

	Pin	Function	Destination
Con 3	A	Data	Con 1 Pin 29
	B	Shift Clock	Con 1 Pin 14
	C-E	n/c	
	F	0V	Con 1 Pin 23
Skt 1	1	'1' MSD	TWS 1 '1'
	2	'2'	" " '2'
	3	'4'	" " '4'
	4	'8'	" " '8'
	5	'1' LSD	TWS 2 '1'
	6	'2'	" " '2'
	7	'4'	" " '4'
	8	'8'	" " '8'
	9	+V	Common of TWS 1 & TSW 2

Power Supply Connections

0V	+V
Con 1 p 23 Layer B	Con 1 p 26 Layer B
Con 2 p 23 Layer B	Con 1 p 26 Layer B
LCD 0V	LCD +V

Computer Display System

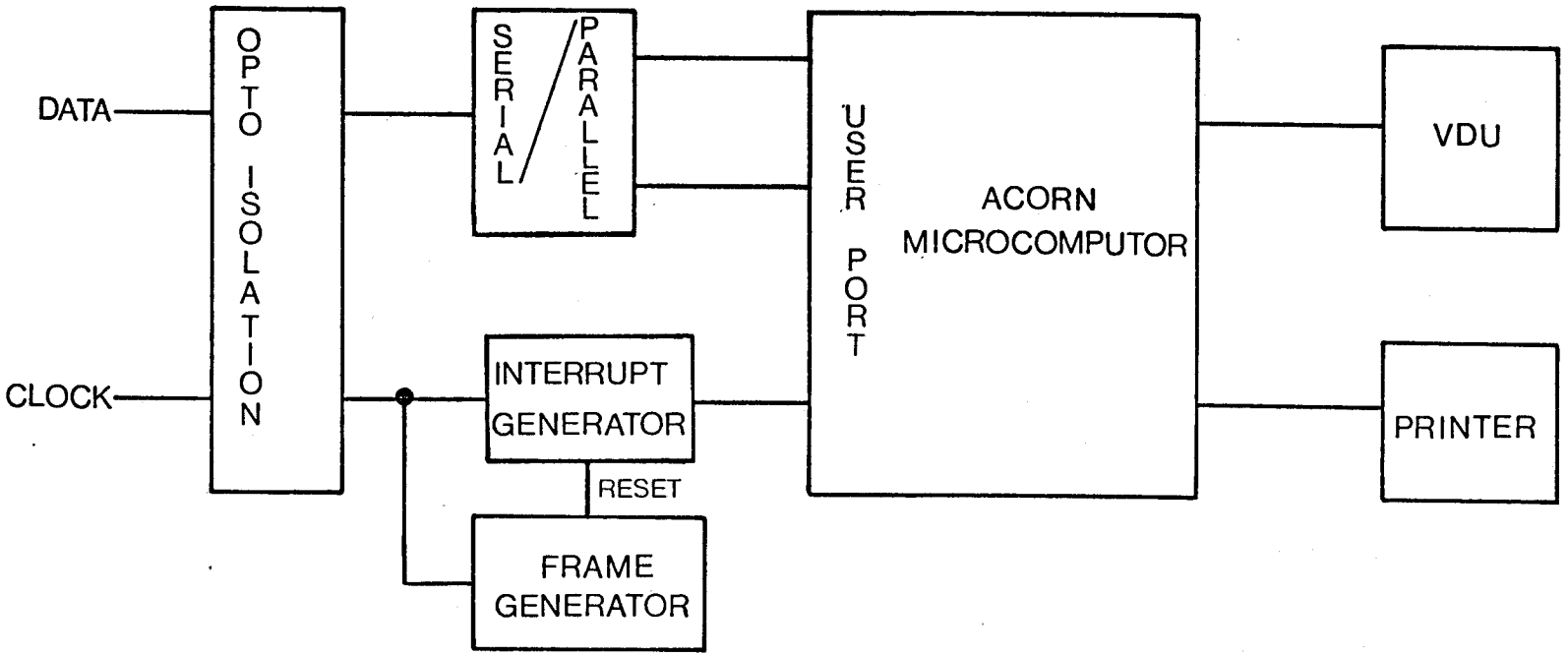
The hardware monitor unit has three major shortcomings: (i) it displays data in hexadecimal, (ii) it displays only one channel at a time, (iii) no hard copy is available. These three features are all easily rectified with use of a computer-based system.

The system described here is based on Acorn BBC Model B, with a purpose-built interface and interrupt driven software.

The data and shift clock derived from the Seadata Logger each drive six buffers connected in parallel IC 1 and IC 2 with the commoned outputs driving an LED in an opto-isolator. The buffers of IC 1 and IC 2 are used in parallel to ensure that enough current is provided to allow the phototransistor to switch at high speed. The output from the opto-isolators is buffered by IC 5a and b to improve the signal rise and fall times. The rising edge of the shift clock is used to trigger a retriggerable monostable IC 7, which acts as a frame detector and remains high for the duration of data input. The shift clock is counted by IC 6, a binary counter, with the Q3 output differentiated to provide a pulse after each eight shift pulses. This pulse is buffered by IC 5c to generate an interrupt strobe for the data into the Computer User Port.

Whilst the shift clock is counted by IC 6 it is also used to clock the data into IC 8, a serial/parallel convertor. The parallel outputs of IC 8 are buffered by IC 5d and IC 6a, b, c, d, e and f and together with the interrupt strobe drive the Computer User Port.

The software as listed provides the means to read the 16 bit binary data into the computer in two bytes. The input of the data under interrupt control is written in assembler, with the display of the data in Basic. The program makes no attempt to retain the values of the data and should any use, other than visual display of the data, be required, further programming will be necessary. The software will accept any number of 16



COMPUTOR DISPLAY- FIGURE 3.

bit data words but the number of data words must be correct within the software before the program is used (i.e. CN = number of 16 bit data words). The data is written to the Computer Display with the hexadecimal values converted to decimal. There are five data words per line and between each data frame is a blank line. With this format and a 24 word frame length (Seadata maximum), the display can show four data frames at one time. If a hard copy of the data is required this can be obtained using a printer.

Power Supplies

The input buffers, IC1, IC2 and the LEDs in opto-isolators are powered by the logging system with the remainder of the circuit powered by +5 volts from the BBC. The isolation of the two supplies means there is no logging system 0V connected to Mains earth and any differences in voltage levels between the logging system and BBC can be neglected.

>

Program to Read Binary Data from User Port

and Display the Data in Decimal Values

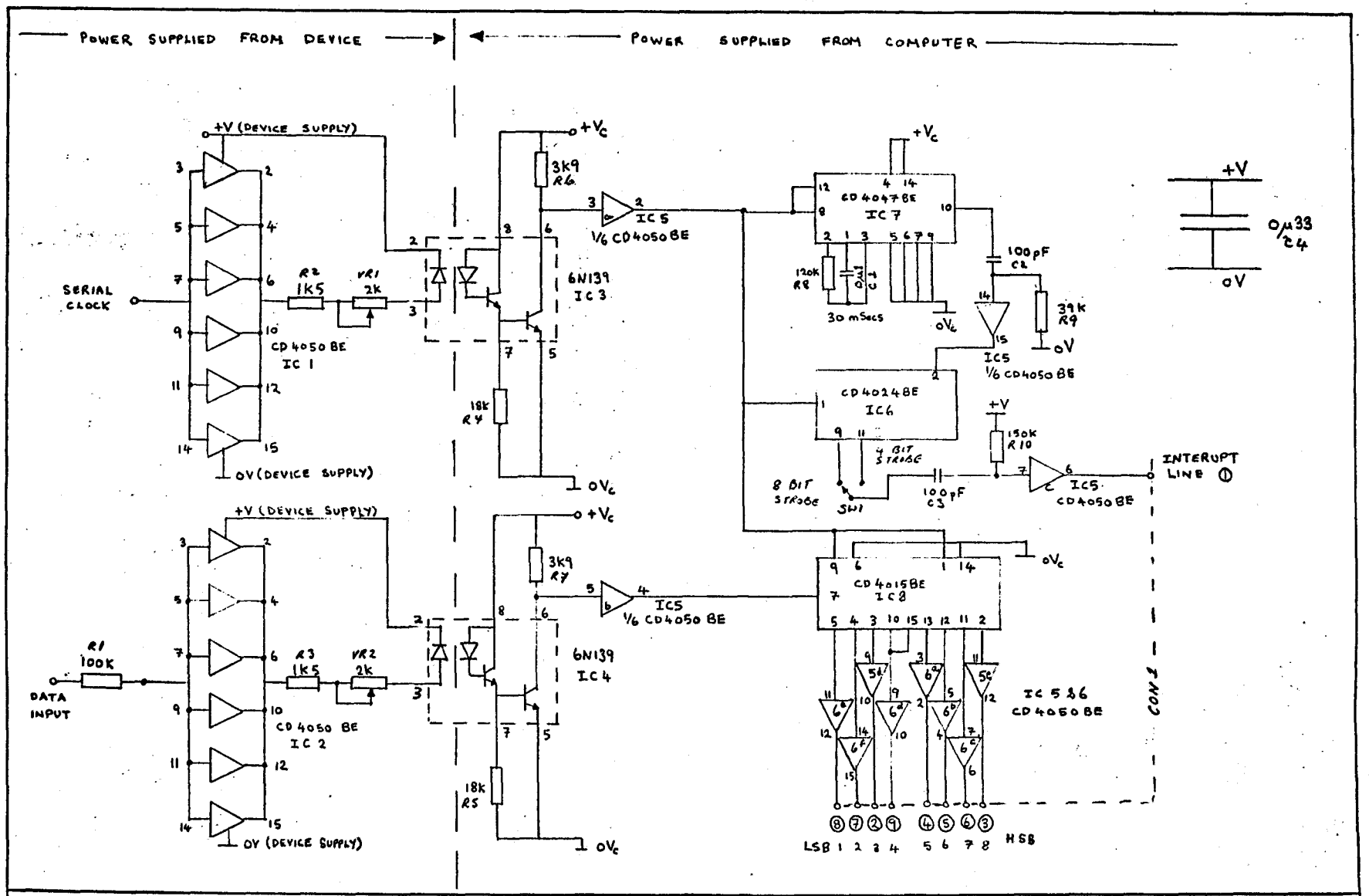
```
 10 REM
 20 REM PROGRAM LIST 16 BIT BINARY DATA
 30 REM
 40 REM NUMBER OF CHANNELS IS SET BY CN
 50 REM
 60 DIM INIT 300
 70 DIM STORE 60
 80 CN=8
 90 F=STORE+(CN*2)-1
100 @%=08
110 IRQ2V=&0206
120 OSBYTE=&FFF4
130 FOR I%= 0 TO 2 STEP 2
140 P%=INIT
150 [OPT I%
160.INIT  LDA £&00
170       STA &8F
180       STA &8E                    \RESET POINTERS AND FLAGS
190       STA &8B
200.SYNC  LDA £&00
210       STA &FE64                  \LOAD LOW BYTE TIMER
220       LDA £&80
230       STA &FE65                  \LOAD HIGH BYTE TIMER
240       LDA &FE60                  \RESET INTERRUPT FLAG
250.WAIT  LDA £&10
260       BIT &FE6D
270       BNE SYNC                   \DETECT CB1 TIMER RESET
280       LDA £&40
290       BIT &FE6D
300       BVC WAIT                   \DETECT TIME OUT
310       LDA £&30
320       STA &8F                    \SET DATA REQUIRED FLAG
330       RTS
340.RUPT  PHA:TXA:PHA:TYA:PHA        \SAVE REGISTERS
350       LDA &8E                    \LOAD STORAGE PTR
360       TAX                        \INTO X REG
370       LDA &FE60                  \READ INPUT PORT
380       STA STORE,X                \STORE DATA
390       INC &8E
400.FINAL PLA:TAY:PLA:TAX:PLA        \RESTORE REGISTERS
410       RTI
420.GO    LDA £&97:LDX £&6C          \SELECT PCR ON USER VIA
430       LDY £0:JSR OSBYTE          \SET UP TO DETECT H-L TRANS.
440       LDA £&97:LDX £&6E          \SELECT IER ON USER VIA
450       LDY £&6F:JSR OSBYTE        \ENABLE CB1 INTERRUPTS ONLY
460       LDA £&97:LDX £&6E          \SELECT IER ON USER VIA
470       LDY £&90:JSR OSBYTE        \ENABLE CB1 INTERRUPTS
480       LDA £RUPT MOD 256:STA IRQ2V \CHANGE IRQ2 VECTORS TO
490       LDA £RUPT DIV 256:STA IRQ2V+1\ POINT TO ROUTINE 'RUPT'
500       RTS                         \BACK TO BASIC
```

```
510 ]NEXT I%
520 CALL GO
530 CALL INIT
540 IF ?&8E>CN*2-1  THEN 550 ELSE 540
550 FOR I=STORE TO F STEP 2
560 PRINT ?I*256+?(I+1);:
570 NEXT
580 PRINT:PRINT:
590 GOTO 530
```

Software Descriptions

Lines 60-70	Dimension Storage Space for Assembled Machine Code programs, and raw data storage area.
Lines 80-90	Set number of 16 bit data words by CN, and hence the number of bytes to each data frame is calculated.
Line 100	Sets the Monitor Format output code to 5 digits and three blank characters.
Lines 130-150	Start Assembler loop.
Lines 160-190	Initialises the storage pointer and data frame flag.
Lines 200-240	Sets the interval timer.
Lines 250-330	WAIT. Detects the absence of interrupts. If an interrupt is detected the timer is reset and the software continues to wait for a gap in the interrupt. This software establishes synchronisation between the processor and the Seadata logger.
Lines 340-410	RUPT. This routine is called each time an interrupt is generated. The registers are saved at the start and replaced at the end of interrupt servicing. The User Port data is read and stored in location STORE which is indexed by register X.
Lines 420-500	GO. The User Port is set to detect the interrupts and the interrupt vectors are set to point to the routine RUPT.
Line 510	End of the Assembler loop.
Line 520	Calls routine GO to initiate User Port and interrupt vectors.
Line 530	Calls initialisation of pointers and flags and then detects synchronisation with data gap in between data frames.

Line 540	Waits until correct number of bytes has been acquired, then the display data frame is initiated.
Lines 550-580	This loop displays the byte data in decimal values and resets the data storage pointer.
Line 590	Returns the program to await the start of a new data frame.



8 BIT PARALLEL INTERFACE TO COMPUTER

INSTITUTE OF OCEANOGRAPHIC SCIENCES.

ISSUED TO		DRAWING No. I.O.S./
REVISED	DRAWN BY KGB	DATE 3/4/84 SHEET No.
	ISSUED	FOR ORDER No. FOR UNITS

Wolsing Dyeline 0707/83

A3 PB2038

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
IC1	INTEGRATED CIRCUIT			CD4050 BE	R.C.A		
IC2	" "			CD4050 BE	R.C.A		
IC3	" "			6N139	H.P		
IC4	" "			6N139	H.P		
IC5	" "			CD4050 BE	R.C.A		
IC6	" "			CD4024 BE	R.C.A		
IC7	" "			CD4047 BE	R.C.A		
IC8	" "			CD4015 BE	R.C.A.		
VR1	POTENTIOMETER.	2KΩ	0.5W	T75-207	DUBILIER	FARNELL CODE T75-207 2K	
VR2	"	2KΩ	0.5W	" "	"	" " " " "	
R1	RESISTOR	10K	¼W	METAL FILM MR25	WELWYN		
R2	"	1KΩ	"	" " "	"		
R3	"	1KΩ	"	" " "	"		
R4	"	18KΩ	"	" " "	"		
R5	"	18KΩ	"	" " "	"		
R6	"	3K9	"	" " "	"		
R7	"	3K9	"	" " "	"		
R8	"	100KΩ	"	" " "	"		
R9	"	39KΩ	"	" " "	"		
R10	"	150KΩ	"	" " "	"		
C1	CAPACITOR	0.1	10%	MKS2	WIMA	FARNELL CODE 143-680	
C2	"	100pF	10%	61232 /006 INV	STC		

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

SEADATA - COMPUTER INTERFACE

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S./

COMPILED BY KAS DATE 10/6/85 SHEET No. 1

ISSUED FOR ORDER No. FOR UNITS

WORKING OUTLINE ONLY

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
C3	CAPACITOR	100pF	10%	8123Z /COG 100V	S.T.C		
C4	"	0·33mF	10%	MKC 4	WIMA		
CON 1	PCB CONNECTOR	20 WAY	IDC	ITT-CANNON - G		R.S. COMPONENTS STK No. 467-346	
CABLE	RIBBON CABLE	20 WAY				" — 360-122	WHEN CONNECTORS ARE MOUNTED ON RIBBON CABLE THE INTERFACE PLUGS DIRECTLY INTO BBC USER PORT
CON 2	RIBBON CABLE MTD	20 WAY				" — 467-289	
CON 3	" " "	20 WAY				" — 467-289	
SW1	SWITCH	SPCO		ULTRA MINATURE		" — 334-224	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

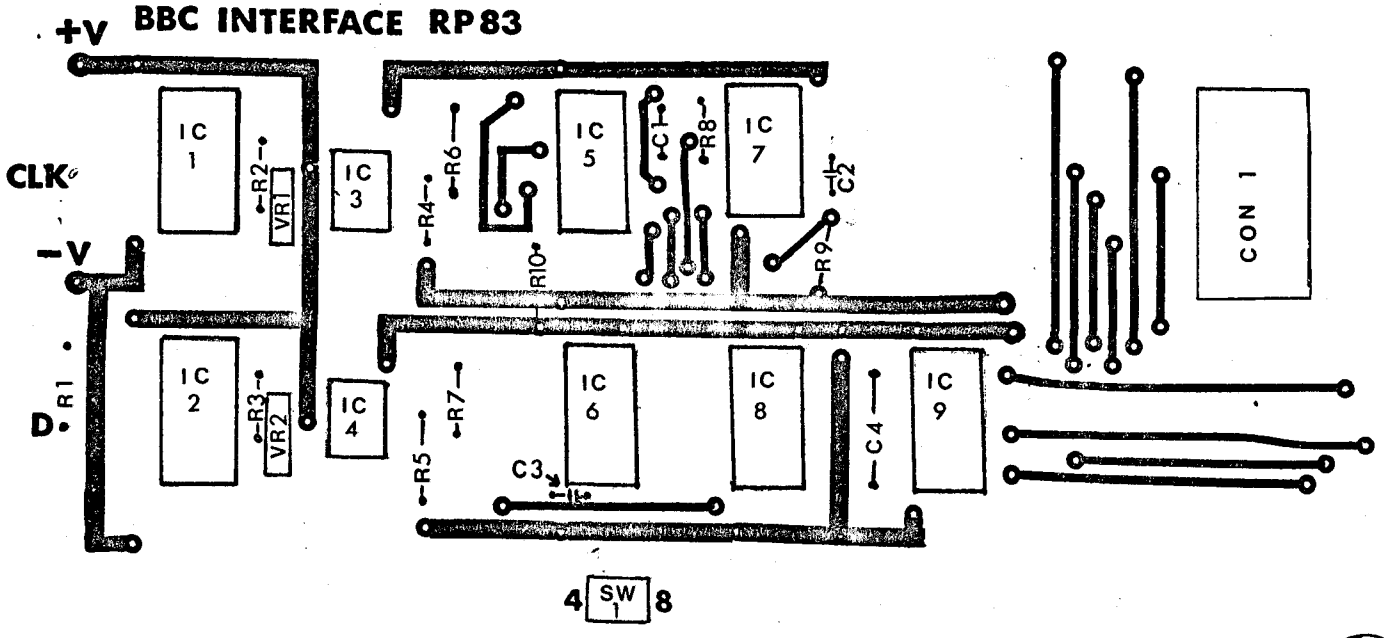
SEADATA — COMPUTER INTERFACE

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S./

COMPILED BY KJB DATE 10/1/85 SHEET No. 2

ISSUED FOR ORDER No. FOR UNITS


BBC INTERFACE RP83
+V
CLK
-V
D
IC 1
IC 2
IC 3
IC 4
IC 5
IC 6
IC 7
IC 8
IC 9
CON 1
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
C1
C2
C3
C4
VR1
VR2
4
SW 1
8