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I.O.S.

A Digital Data Logging System for the Neil Brown Temperature, Conductivity and Depth Probe

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CTD-DIGIDATA LOGGER

1. INTRODUCTION

In recent years, the Neil Brown Conductivity, Temperature and Depth probe (CTD) has become increasingly used by a growing number of oceanographic disciplines, both as a stand alone instrument and as a package. Until this time, there were two ways in which the vast amount of data generated could be logged for subsequent processing.

The prime logging/processing was usually handled by Shipborne Computing facilities. These would both store, average and calibrate data, and produce real time plots of the various parameters. However, due to logistic problems, or the use of the CTD system on very small ships, it was not always possible or desirable to have these computing facilities. A secondary system was then used whereby the raw frequency shift key modulated data (FSK) was recorded on a high quality audio tape recorder. This recorder was also used with computing facilities to provide a back up in the event of equipment failure.

There were a number of drawbacks to this approach, firstly any data had to be replayed through the CTD deck unit in real time, secondly there was no time reference or header information. This made it difficult to align the data with any navigational information, and thus made interpretation of the data more difficult.

Choice of system

To overcome these problems, it was decided to produce a logging system that could store the data in a form that was both easily transportable over a range of computers, contain time information and allow verification of the data thus stored.

The data rates, typically 15 data words/frame at 16 frames/second, may not seem particularly high, but it has to be borne in mind that a CTD may be carried in a towed vehicle behind a ship for up to 4 days or more at a time. This results in the need to store very large amounts of data.

The storage medium does not have to be small, but it must be compatible with both shipborne and other mainframe facilities at the Institute. To this end, it was decided to adopt nine track magnetic tape as a standard.

This has a number of advantages, namely low cost, moderate capacity and is widely used. There are some disadvantages, however, these being relatively slow access speed compared with other media, such as hard discs. Large numbers of tapes, plus backup copies, also need to be stored.

Method

Having decided on magnetic tape as the storage medium, there are then a number of ways in which the data can be presented to the tape transport. The prime consideration is to avoid any loss of data during the write operation, thus it is necessary to buffer the incoming data. The chosen DIGIDATA system used is commercially available, and consists of a 1K double buffered memory, driving the tape transport through a formatter and allowing data to be transferred to tape from one buffer, whilst writing to the second.

The CTD data is transmitted up the sea cable in an 11 bit serial, FSK modulated format. This consists of two frequencies, i.e. two cycles of 6.6 kHz to represent a one, and one cycle of 3.3 kHz to represent a zero. This signal is then demodulated by the CTD deck unit, producing a standard 11 bit serial data stream, consisting of two start bits, eight data bits and one stop bit. The baud rate however is non-standard. The data words are eight bit binary, and are converted to Binary Coded Decimal (BCD) by the CTD deck unit for subsequent display in engineering units.

This leaves us with a number of possible ways to manipulate the data. The first, and one of the more economical methods as far as efficient use of tape is concerned, is to store the data in its binary form. This however presents some problems for inputting time and header information into the data stream. A second option is to store the data in binary, but add the header information in ASCII code. The use of mixed coding does however complicate decoding of the tapes.

It was decided therefore to write data entirely in ASCII. This would use approximately 2.5 times more tape, but does provide an easily read format. Conversion of the BCD data supplied by the deck unit to ASCII is very easy, only three fixed bits need be added to the BCD, to give the corresponding ASCII code. The format finally chosen is as follows.

Header

This is comprised of eighty characters in total. The header consists of a real time clock of eight characters, in the form HH;MM;SS. This is followed by sixty four characters in a free field format, entered from a keyboard. A further eight characters are added, making the total up to eighty. For technical reasons, seven are placed before the time word and one after the free field. Eighty characters have been chosen to allow the total to be eventually read in groups of five.

Data

The data parameters presented by the deck unit require five ASCII characters to represent a maximum of 65535, this being the largest number output by any one channel of the CTD underwater unit. It can be seen that allowing both the header and data to be read in fixed group sizes without loss of registration is a distinct advantage in later processing.

The number of data characters are fixed to allow the nearest whole number of data frames to be written. A typical data frame for a deep CTD would consist of seven words, viz:- Frame Sync, Pressure, Temperature, Conductivity, Transmittance, Oxygen Current and Oxygen Temperature. Thus a convenient choice of record length would be 990 characters. This allows 80 for the header and 910 for data, this being divisible by 7*5, to give 26 whole data frames. The time word is updated with each new block and inserted into the header, this being the reason the header is written every record.

In practice a number of CTDs are used, each with different frame size and construction. The record length can be changed easily by a set of switches in the hardware.

Header display

As the header is only eighty characters long, of which 64 can be input by the user, it was decided that for both economical and technical reasons, a full dedicated terminal was unnecessary. A visual record of the header is produced by the hardware, and displayed on a laboratory oscilloscope. This approach then satisfies the two requirements of providing header display and service equipment. This system is also used to display and verify data tapes.

2. HARDWARE DESCRIPTION

Introduction

Figure 1 shows the block diagram and data flow of the interface. Characters are entered either via a keyboard, or as data read from previously recorded tapes. These characters are then stored in temporary shift registers. They are then passed to the X, Y, Z character generator for display on the oscilloscope. All sixty four characters of the temporary store are presented in turn to the character generator and the whole display kept refreshed by recirculating the store at around 50 Hz.

Before the complete logging process is commenced, the header is typed in, transferred to a second or header/clock store, and the output from the real time clock added. This produces both the code for transfer to the data stream, and a visual output on a Liquid Crystal Display.

The four bit BCD data from the CTD deck unit for each of the characters in a single parameter are passed to five shift registers, and the extra fixed characters needed to convert BCD to ASCII added at this stage. The transfer of data out of the shift registers does not commence until a strobe generated by the CTD Frame Sync word is present. Each subsequent CTD word is then passed to this unit, together with its appropriate strobe. Output of the final data stream is via a set of electronic switches. These switches allow the header to be first sent to the tape buffer, followed by the data. The timing of these processes is controlled by the record and header bit counters.

3. DETAILED CIRCUIT DESCRIPTION

3.1 Oscillator and strobe display

The function of these circuits is to provide the two master clocks required by various parts of the interface, and to visually display the status of the data word strobes from the CTD deck unit.

Both the 15 kHz and 200 kHz oscillator functions are realised by the use of two Phase-Locked Loop integrated circuits. These ICs are not in fact used in a phase-locked loop mode, but use is made of the Voltage Controlled Oscillator (VCO). Appropriate timing capacitors are connected between pins 6 and 7 of each IC, together with a potentiometer connected from pins 11 to ground. This controls the basic range of frequencies available. The voltage tapped off by a second potentiometer, connected from the positive power rail to ground, holds the VCO input voltage control pin 9 steady, and allows fine control of the output frequencies. The outputs from pins 4 of each VCO drive IC 9/14 and hex input non-inverting buffer, IC 9/9. The two clocks are then passed by IC 9/15 and IC 9/10 to other circuits. The remaining four buffers are used by other circuits.

Twelve identical circuits are used to display the data word strobes, therefore only one will be described. Strobe pulses, when present on pins 3 and 11 of IC 1, cause the Q outputs of IC 1/1 and IC 1/13 to go high. The Q outputs are connected to their respective reset pins IC 1/4 and IC 1/10 by resistors. Capacitors are connected between the reset pins and ground. These control the time taken for the voltage on these pins to rise to a level sufficient to reset the Q outputs low again. The initial short strobe pulses are thus lengthened to drive Light Emitting Diodes via Transistors Tr 1 and Tr 2 to provide the visual display. IC 2 through to IC 6, together with the appropriate components, drive the remaining ten LEDs.

3.2 Character-timebase generator

This circuit performs two functions, viz:-

(a) Generation of the eight by six dot patterns, for the ASCII character set.

(b) Provision of an X-Y timebase and Z, or intensity modulation, to drive an oscilloscope.

Generally, throughout the following descriptions, any reference to integrated circuit connections is as follows, e.g. IC 1/3. This means that pin 3 on integrated circuit number one is being referred to.

A gated 200 kHz square wave drives the clock pin 15 of binary counters IC 1 and IC 28. The Q1, Q2 and Q3 outputs of IC 28 drive three inputs of an eight bit digital to analogue (DAC) convertor via buffers. The gating of the clock is carried out by the Header Store to halt the clock and prevent further action of this circuit, whilst a new character is being entered from the keyboard. As the DAC is clocked, a ramp output is generated from pin 4, and drives an operational amplifier (Op-Amp). This ramp output provides the Y axis drive for the 'scope. The Q4 output of IC 28/2 passes to nor gate IC 17/5. The Master Reset is applied to IC 17/6. This output is inverted by IC 17/1-2 and applied to the reset pin 1 of IC 28, providing a divide by eight counter, and hence steps the Y generator up by the same number.

IC 1 is a second binary counter. The Q4 output of IC 1/2 passes to nor gate IC 3/5. The master reset is also applied to IC 3/6. The output of IC 3/4 is inverted by nor gate IC 3/1-2. The output of IC 3/3 resets IC 1/1, setting the count of IC 1 to zero, thus providing a divide by eight count. The Q4 output of IC 1/2 also clocks IC 2 to produce a lengthened pulse from its Q output. As the Q output goes high, the voltage on the reset pin 4 rises more slowly due to the R/C time constant. The pulse length will be approximately 0.6*R*C.

IC 11 is a ROM, containing the dot patterns for the ASCII character set. When the appropriate code is applied to its input terminals 17 to 22 from the Header Store, the vertical lines of dots for the applied character are output from pins 3 to 9, as the address lines 14, 15 and 16 are strobed. Initially all the address lines are low, thus the left hand line of the character is output. The seven output lines 3 to 9 drive the least significant inputs of an eight bit parallel to serial shift register, IC 12. The Q output of IC 2/1 clocks IC 5/3. The first half of this IC is connected in the same fashion as IC 2. The not Q output clocks the second half of IC 5.

It can be seen that this combination will produce a pulse, whose length is controlled by the second half of the device, but is delayed by the pulse length of the first. This delay circuit is used extensively throughout all of the circuits in the system and will be known as a delay FF. The delayed Q output of IC 5/13 is applied to nor gate IC 3/12. A pulse from the Header Store is applied to IC 3/13. The output of IC 3/10 is applied to the parallel shift pin 9 of IC 12. This parallel shifts the first row of dots generated by IC 11 into IC 12. The alternative shift pulse from the Header Store on IC 3/13 only occurs when a new character has been entered from the keyboard.

The 200 kHz clock drives delay FF IC 4. The Q output of IC 4/13 clocks the dot pattern serially out of IC 12/3. This serial output drives an Op-Amp to provide the intensity modulation for the 'scope. The most significant bit, pin 1 of the shift register, is set high by the Q output of IC 2/13, when IC 2/11 is clocked by a pulse from the Header Store. As characters are entered from the keyboard, a counter which is initially set to 64 is decremented and compared with a second counter, which is incremented as data in the Header Store is recirculated. This produces a row of dots above the character being displayed, and forms a cursor to give a visual indication of the character position in the store, that can be altered by the next key press.

The eighth pulse from IC 1 via IC 2/1 also clocks binary counter IC 9. The Q1, Q2 and Q3 outputs of IC 9 drive the address lines of IC 11 via buffers. The Q3 and Q2 outputs are applied to nand gate IC 8/5 and IC 8/6. The output of IC 8/4 is inverted by IC 8/1-2. This output is then applied to nor gate IC 7/2. This output is then applied to nor gate IC 7/2. The master reset is also applied to IC 7/1. The output of IC 7/3 is inverted by nor gates IC 7/5-6 connected in parallel with IC 7/12-13. The parallel output pulse from IC 7/4 and IC 7/11 resets IC 9/1 to a zero count, and IC 2/10. The Q output of IC 2/13 goes low, turning off the cursor. Delay FF IC 6 is also clocked.

The not Q output of IC 6/12 passes to the Header Store to tell it that the new character has been displayed. This occurs after six pulses. The master reset pressed after power-up sets the Q output of IC 16/1 low. The not Q output of IC 16/2 drives the D input of IC 16/5 and is also sent to an input of the Op-Amp, driving the Y axis and biasing the first line of characters that will be produced towards the top half of the 'scope screen. Thus it can be seen that after each group of eight pulses, the next line of dots will be produced by IC 11 and parallel shifted via IC 5. At the same time, IC 2 clocks the first of a pair of binary dividers, IC 22 and IC 25. The outputs of the dividers drive a DAC to produce the ramp for the X axis drive via an Op-Amp. The Q3 and Q4 outputs of the second counter, IC 22, are applied to nand gate IC 15/12-13. The output of IC 15/11 is inverted by nand gate IC 15/8-9.

The output of IC 15/10 is applied to nor gate IC 17/9. IC 17/8 is driven by the master reset. The output of IC 17/10 is inverted by nor gate IC 17/12-13. The output of IC 17/12 resets both IC 22 and IC 25 to zero count. IC 16/3 is also clocked by IC 15/10. This will occur on the 192nd pulse. As the D input of IC 16/5 is high the Q output of IC 16/1 will be clocked high. Both the D input of IC 16/5 and not Q IC 16/2 will go low. This action results in the X axis being returned to the left hand side of the 'scope screen as IC 22 and IC 25 are reset, and the second line of characters being shifted towards the lower half of the 'scope screen due to not Q of IC 16/2 biasing the Y axis Op-Amp. This process then continues until the next 32 characters have been displayed when the counts of IC 22 and IC 25 become zero again. Once again the Q3 and Q4 outputs of counter IC 22 go high, and clock IC 16/3 via nand gates IC 15/12, IC 15/13 and IC 15/10. As the D input of IC 16/2 is low, the Q output of IC 16/1 goes low. Both the not Q output of IC 16/2 and the D input of IC 16/5 now go high, returning to the top half of the 'scope screen. As the total of 64 characters, counted by IC 25 and IC 22 in two groups of 32, is the same as the 64 stage shift registers on the header store, the display will remain static and synchronised, whilst being constantly refreshed as the whole cycle repeats itself.

3.3 Keyboard/Replay

The keyboard used is a commercially available unit manufactured by C.P. Clare. The coded character outputs from the keyboard are provided by open collector driver ICs. Each input connected to the keyboard is pulled up by a 4k7 resistor to provide the collector load for the driver outputs. IC 1/IC 2 are quad and-or select gates, and switch either output from the keyboard, or characters read from the Digidata buffer, via inverting buffers IC 5. The inversion is performed, as the Digidata uses negative logic.

The Read/Write switch SW 3 is a two way four pole switch used to set up various functions. In the Read position, one pair of poles connects either a low frequency square wave oscillator, or the strobe output from the keyboard to a Darlington pair formed by transistors, Tr 1/Tr 2. This output is passed to the Read A Character (RAC) input of the Digidata buffer.

A second pair of poles is connected to ground, and sets the Digidata buffer Read/Write input to read. The third pair of switches IC 1/IC 2 select characters from the Digidata buffer. The fourth connects Tr 1/Tr 2 to the keyboard strobe.

The oscillator is formed by IC 1 1/2, C1, C2, VR 1 and VR 2, and provides either a 10 or 1 Hz square wave, depending on the position of the 10/1 characters/sec switch SW 1. A third switch, SW 2, selects either the oscillator or the keyboard strobe. In the keyboard position, single step mode is achieved.

The Break key on the keyboard is brought out to drive the delay FF IC 4 and provide a pulse, eventually used to backspace characters written on the 'scope. In the Write position, SW 3 grounds the base of Tr 1, switching off Tr 2. IC 1/IC 2 are switched to keyboard input. The Digidata Read/Write input is put in the write mode, and the keyboard strobe is connected to the Header/Clock store board 5.

3.4 Header store

This circuit performs the function of a temporary store for the 64 character header. The stored header is also passed to the character generator circuit for display. This header is then

eventually transferred to the header/clock store, where it is included in the CTD data stream written to magnetic tape.

The first thing to consider is the effect of any power-up resets. The Q outputs of IC 19/1, IC 19/13, IC 18/1 and IC 25/1 are set to a low state by capacitors connected between the positive rail and their reset pins. Resistors from resets to ground provide a discharge path and control the time constant of the reset function.

All other flip-flops or delay FFs will be automatically reset if any Q output goes high on power-up. Resistors connected between the Q outputs and their reset pins will ensure this, and capacitors from resets to ground will again control the time constants.

After power-up, the two Master reset switches would normally be pressed, resetting binary counters IC 10 and IC 11 to a count of 64, due to the jam inputs being held high initially. Binary counters IC 12 and IC 13 will be reset to a zero state.

The following describes how characters entered from the keyboard are stored.

The state of the 64 stage shift registers IC 1 to IC 7 is initially indeterminate. This means that random ASCII characters will be held in the store to be overwritten later. After each complete character is drawn on the 'scope, a pulse from IC 10 on the character generator clocks pins 2 of IC 1 to IC 7 of the header store. This clocks characters through the shift registers. The Q output pin 6 of each shift register is connected to two and-or select gates IC 8 and IC 9. The kb select pins 14 of these two ICs are held low by the Q output of IC 18/1. The ka select pins 9 of IC 8 and IC 9 are held high due to the inverting action of IC 14/1-2. In this condition, characters from the shift registers will be switched through IC 8 and IC 9, and presented on the input pins 15 of the shift registers. This will continually recirculate the stored characters, providing a synchronised display.

The clock pulse to the shift registers also increments the count of IC 12 and IC 13. After 64 counts the Q3 output of IC 13/14 goes high. This pulse is nor-gated with the master reset by IC 26/1. The output of IC 26/4 is inverted by nor gate IC 26/8-9 and fed back to the reset pins 1 of IC 12 and IC 13, setting the count to zero again.

The first key press applies the key strobe to IC 25/1. The Q output of IC 25/1 goes high, enabling the nand gate IC 14/5. On a count of 64 from IC 13/14, delay FF IC 23 is clocked. The Q output of IC 23/13 is applied to the now enabled nand gate, IC 14/6, and the count of IC 12 and IC 13 reset to zero via nor gates IC 26/6 and IC 26/10. The output of IC 14/4 is inverted by IC 14/1-2 and clocks IC 18/11, IC 19/11 and IC 25/3. This sets the Q output of IC 19/13 high. The not Q output of IC 18/12 clocks IC 17/3. The Q output of IC 17/1 then resets IC 19/4, and IC 19/1 goes low again.

The Q output of IC 19/13 enables nand gate IC 14/8. Due to IC 25/5 going high, the Q output of IC 25/13 is applied to nor gate IC 20/5. The output of IC 20/4 clocks IC 10/15 and decrements its count to 63. The least significant six Q outputs of IC 10 and IC 11 are compared with those of IC 12 and IC 13 by two quad exclusive-or gates, IC 28 and IC 29. When IC 12 and IC 13 reach a count of 63, all the Q outputs of the two sets of counters will be high. The six outputs of IC 28 and IC 29 will then go high. These are gated by a dual quad input nand gate, IC 30. The outputs of these two gates are inverted by nor gates IC 27/5-6 and IC 27/8-9. The two outputs pass to nand gate IC 21/1 and IC 21/2. The output of IC 21/3 is inverted by nor gate IC 27/12-13.

The output of IC 27/11 clocks delay FF IC 22 and also passes to the character generator, IC 2/11. The Q output of IC 2/13 goes high, and sets the most significant bit, pin 1 of IC 12 high. This starts the row of dots at the top of a displayed character, forming the cursor. The Q output of delay FF IC 22 passes to nand gate IC 14/9, already enabled by IC 19/13 going high. The output of IC 14/10 is inverted by nand gate IC 14/12-13. The output of IC 14/11 clocks IC 17/11 and IC 18/3. The Q output of IC 18/1 goes high. The not Q output of IC 17/12 clocks IC 16/3. The Q output of IC 16/1 resets IC 19/10 and the Q output of IC 19/13 now goes low. IC 25/4 is also

reset.

With the Q output of IC 18/1 going high, IC 16/11 goes high. The kb select pins 14 of IC 8 and IC 9 also go high. The ka select pins 9 of IC 8 and IC 9 go low due to the inverting action of nor gate IC 20/8-9. The data output from the and-or select gates IC 8 and IC 9 are now switched from the Q outputs of the 64 stage shift registers to the character being presented by the keyboard.

The not Q output of IC 16/12 is pulsed low by IC 18/1 going high. Nand gate IC 21/6 disables the 200 kHz clock on IC 21/5. This clock output on IC 21/4 is inverted by IC 21/12-13 and drives the character generator circuit. Disabling this clock prevents any further output from being displayed on the 'scope. With IC 18/1 going high, delay FF IC 15 is clocked. The Q output of IC 15/13 passes to the character generator IC 12/9 to parallel shift the first dot row of the new character into IC 12 for subsequent display. The 200 kHz clock to the character generator is only disabled long enough to allow this parallel shift to take place.

The character generator now resumes its operation. As soon as the new character has been completed, IC 10 of the character generator is pulsed. This pulse passes to the clock pins 2 of the 64 stage shift register, and resets the Q output of IC 2 to turn off the cursor. As the new character data are still present on the data inputs 15 of IC 1 to IC 7, this new character is placed in the shift register, and the count of IC 12 and IC 13 is incremented by one. The pulse strobing IC 10 of the character generator also clocks delay FF IC 6 on that circuit. The Q output of this delay FF IC 6/12 passes to the header store and resets IC 18/4, to set the Q output of IC 18/1 low. The kb select pins 14 of IC 8 and IC 9 now go low, with the ka select pins 9 of IC 8 and IC 9 going high. The recirculating mode of the shift registers is now resumed.

The operation of recirculating data and inserting new characters is now clear. To recap, initially the count of IC 10 and IC 11 is 64. The count of IC 12 and IC 13 is zero. The last, or rightmost character of the display, is present on the Q outputs of the shift registers. On a key press, the count of IC 10 and IC 11 is

decremented by one. When the next 63 characters have been recirculated, the first, or leftmost character of the display is present at the input pins of the shift registers.

Data is now switched by IC 8 and IC 9 to the keyboard character. As both groups of counters are at 63, the operation of halting the character generator, clocking the new character into the shift registers and resetting the rest of the circuit is then performed. The count of IC 10 and IC 11 is also decremented to 62, ready for the next character. On the count of IC 10 and IC 11 reaching zero, the Q3 output of IC 11/14 goes high and resets IC 10 and IC 11 via nor gates IC 26/1 and IC 26/12-13 to a count of 64 as the jam inputs are held high.

The only other function to be performed is to allow the cursor to be backspaced, for correction or insertion of new characters anywhere in the shift registers. When the backspace key is pressed, delay FF IC 24 is clocked. The up/down pins 10 of IC 10 and IC 11 now go high, placing them in the count up mode. The output of nor gate IC 20/11 also goes low. This in turn causes the jam inputs of IC 10 and IC 11 to go low, allowing the counter to perform the proper up count.

The Q output of the delay FF IC 24/13 passes to nor gate IC 20/5. The output of IC 20/4 clocks IC 10 and IC 11, incrementing their count by one. Depending upon the number of backspace pulses, the count of IC 10 and IC 11 can be incremented anywhere up to 64, thus controlling the point where the shift registers halt, and characters are inserted.

3.5 CTD data store

The function of this circuit is to transfer the four bit BCD code for each of the five digits of a CTD data word, modify the code to ASCII and present this code, one character at a time, to the header/ clock store.

Initially after power-up, the master reset pulse is applied to nor gate IC 21/2. The output of IC 21/3 is inverted by nor gate IC 21/5-6. The output of IC 21/4 is then applied to the reset pin 1 of binary counter IC 22. The master reset is also applied to nor gate IC 21/9. The output of IC 21/10 is inverted by nor gate IC 21/12-13.

The output of IC 21/11 is then applied to the reset pin 15 of decade counter IC 20. IC 16/3 is also clocked and the Q output of IC 16/1 passes to the record/header counter circuit. This pulse can in fact be ignored during this initial reset period.

The Q output of IC 17/1 is set low by a power-up reset network on the reset pin 4 of IC 17, or when the record/header has clocked both header and data out. The not Q output of IC 17/2 goes high, and is applied to a pair of paralleled inputs of a dual quad nor gate IC 11. The output of this gate is thus held low and inverted by nand gate IC 15/8-9. The output of IC 15/10 thus remains high and holds the reset of IC 16/10 high. The Q output of IC 16/1 is applied to nand gate IC 15/5. Any input from the 15 kHz clock on IC 15/6 will thus be disabled, and hence the five serial shift registers IC 1 to IC 5 cannot be clocked. All of the data word strobes are applied to nand gate invertors IC 6 to IC 8. The subsequent outputs are then applied to or gates IC 9 to IC 10. Nor gate IC 12 further gates the outputs of IC 10/3, IC 10/4, IC 12/4 and IC 12/3. The outputs of or gates IC 9/3, IC 9/4, IC 9/10 and IC 12/11 are gated by the other half of the dual quad input nor gate, IC 11.

The output of IC 11/1 is then inverted by nand gate IC 18/12-13. The output of IC 18/11 then clocks IC 17/11. The Q output of IC 17/13 is applied to the parallel shift pins 9 of the serial shift registers, IC 1 to IC 5. This pulse is also delayed by R15 and C3 and clocks IC 16/11. However, due to the reset pin of IC 16/10 still being held high, no output can occur from IC 16/13.

The Frame Sync strobe applied to nand gate IC 18/5 will only set the circuit in action when IC 18/6 goes high. When data is finally transferred from the header/clock store to magnetic tape, the header is written first under control of the record/header counters. During this period, IC 18/6 is low. On complete transfer of the header, IC 18/6 goes high and the next frame sync pulse is enabled. The output of IC 18/4 is then inverted by nand gate IC 18/1-2. The output of IC 18/3 clocks IC 17/3. The not Q output of IC 17/2 goes low. This output is applied to nand gate IC 11. The output of IC 11/13 now goes high.

Nand gate IC 15/8-9 inverts this pulse and IC 15/10 goes low. This level is applied to the reset of IC 16/10. The frame sync pulse is also applied to the second half of IC 11. This frame sync pulse from IC 11/1 is inverted by nand gate IC 18/12-13. The output of IC 18/11 clocks IC 17/11. The Q output of IC 17/13 is applied to the parallel shift pins 9 of serial shift registers IC 1 to IC 5, loading the frame sync word. The Q output of IC 17/13 is delayed by R15 and C3 before clocking IC 16/11. The Q output of IC 16/13 now goes high and enables nand gate IC 15/5. The four bit code for each of the digits of the frame sync have now been shifted into IC 1 to IC 5, loading the least significant four bits of each shift register. The most significant four bits of each shift register are held permanently high. Thus each register contains an eight code, which is now in ASCII format. The 15 kHz clock on nand gate IC 15/6 now appears on IC 15/4. This clock is now inverted by nand gate IC 15/1-2. At the same time, delay FF IC 14/3 is clocked, together with binary counter IC 22/15. The Q output of delay FF IC 14/13 clocks the shift registers. The data is now serially shifted through each resistor and out through pin 3 of IC 5.

This output is applied to the serial input pin 7 of serial to parallel shift register IC 13. The rising edge of the not Q output of IC 14/12 clocks the serial data into IC 13. After eight pulses, the first of the five eight bit characters has been shifted into IC 13. The Q2 output of binary counter IC 22 now goes high. This output is applied to nor gate IC 21/1. The output of IC 21/3 is inverted by nor gate IC 21/5-6. The output of IC 21/4 resets IC 22/1 to zero count and passes to decade counter IC 20/14, incrementing its count by one. IC 16/3 is also clocked. The Q output of IC 16/1 passes to the record/header bit counters where a track of the number of these clock pulses is kept. During this period, and-or select gates, IC 2 and IC 4 of the header/clock store allow data now present on the eight parallel outputs of IC 13 of the CTD data store to be passed to the magnetic tape. The next eight bits are now serially shifted into IC 13 and the count of IC 20 incremented, together with a further clock pulse to the header/clock store. When the count of IC 20 reaches five, the output from pin 1 of IC 20 is applied to nor gate IC 19/13. The output of IC 19/11 is applied to nor gate IC 19/9. The output of IC 19/10 is now applied to nor gate IC 21/8, whose output

IC 21/10 is inverted by nor gate IC 21/12-13. This output from IC 21/11 now resets counter IC 20 to zero. After five counts of IC 20, all five eight bit characters will have been shifted in turn through IC 13 and written to tape. With each pulse from IC 20/1, a pulse is passed via C7 to IC 11. The output on IC 11/13 inverted by IC 15/8-9 resets IC 16/10, setting the Q output of IC 16/13 low until the next strobe pulse from IC 11/1 via IC 18/12-13 and IC 17/13. This ensures that data is only shifted through IC 1 to IC 5, after the next strobe has indicated that data from the CTD deck unit is valid. This whole process is repeated until a number of data words set by the record/header counters is reached. IC 18/6 then goes low, disabling further transfer of data until the new header with an updated time is written to tape.

3.6 Record/header counters

The function of this circuit is to control the header shift clock, data character clock and to provide the correct record format written to magnetic tape. The length of record required depends upon the number of words in one CTD data frame. This is controlled in such a way as to ensure that a whole number of frames form each record.

On power-up, the Q output of IC 13/1 is set low. The master reset is applied to nor gates IC 10/2, IC 1/12 and IC 1/2. The outputs of IC 10/3, IC 1/11 and IC 1/3 are inverted by nor gates IC 10/5-6, IC 1/8-9 and IC 1/5-6 respectively. The outputs of IC 10/4, IC 1/10 and IC 1/4 set IC 3 Q output low, resets decade counter IC 14 to zero count, and resets IC 7, IC 6 and IC 5 to a count depending upon the status of each jam input.

The Q output of IC 3 sets the kb select pin 14 of quad and-or select gate IC 4 low, and the ka select pin 9 high, via the not Q output of IC 3. IC 4/9 going high, clocks IC 16/3. The Q output of IC 16/1 sends an Inter Record Gap pulse to the tape controller via transistors Tr 9 and Tr 10. At this stage the tape transport will be off-line, so this pulse will be ignored.

Before the circuit is set in action, the header will have been typed in and transferred to the header/clock store by the Load Header sequence.

Operating the Run/Halt switch now grounds the reset pin 4 of IC 13 and clocks IC 13/3 high. The Q output IC 13/1 goes high and the not Q output IC 13/2 goes low. Nand gate IC 15/12 is enabled by IC 13/1. The low Q output of IC 13/2 disables nand gate IC 12/2, thus preventing any Write End of File pulses. The status of the ka and kb select pins of IC 4 is switched from the data character clock on IC 4/1 to the header shift clock on IC 4/15.

As nand gate IC 15/12 is enabled, the 15 kHz header shift clock on IC 15/13 appears on output IC 15/11. The clock is then inverted by nand gate IC 15/8-9. The output of IC 15/10 is then applied to IC 4/1, the clock input of decade counter IC 14/14. The header clock is switched through IC 4/13, to the first stage of the binary counter formed by IC 7, IC 6 and IC 5. IC 16/11 is also clocked, and the Q output of IC 16/13 applied to the Darlington transistor pair, Tr 7 and Tr 8. The collector of Tr 8 drives the Record clock of the tape buffer, thus loading characters from the header/clock store to this buffer. At the same time, the clock output of IC 4/13 is also applied to nand gate IC 15/5. IC 15/6 is enabled by the high level of IC 4/9. The clock output of IC 15/4 is inverted by nand gate IC 15/1-2. The output of IC 15/3 passes to IC 30 of the header/clock store and then on to the 64 stage shift registers IC 21 to IC 27, the eight bit serial shift registers IC 14 to IC 20 and IC 7 to IC 13 to clock the header out.

After ten clock pulses, the carry out of counter IC 14/12 goes high and clocks the second counter IC 8/14. The '0' output of IC 8/3 goes low. This process repeats itself until the '8' output of IC 8/9 goes high. This occurs after a total count of eighty. The output of IC 8/9 is gated through a series of nor gates comprised of IC 9 and IC 10 to the reset pin 15 of IC 8, setting its count to zero. On IC 8 being reset, the '0' output of IC 8/3 goes high. This output is applied to the clock input of IC 3/3. The Q output IC 3/1 goes high and the not Q output IC 3/2 low. The status of the ka and kb select pins of IC 4 now reverses. Nand gate IC 15/6 also goes low. The clock on IC 15/5 is now disabled, preventing any further clock pulses passing to the header/clock store. The Q output of IC 3/1 also passes to the CTD data store IC 18/6. This enables IC 18/5 and allows the Frame Sync strobe to start the process of loading and shifting the CTD

data. The Q and not Q outputs of IC 3 also drive Darlington transistor pairs Tr 4, Tr 3 and Tr 2, Tr 1. Tr 3 and Tr 1 drive LEDs to provide a visual indication of the header and data cycles. The Q output of IC 3/1 is also applied to nor gate IC 1/13. The output of IC 1/11 is thus held low. This output is then inverted by nor gate IC 1/8-9. The output of IC 1/10 is thus held high and holds the first counter IC 14/15 in a reset state, preventing any further count.

The data character clock on pin 1 of IC 4 is now selected by that status of the ka and kb lines. The counters IC 7, IC 6 and IC 4 continue to count these data clock pulses and clock the tape buffer. When the Q3 output of IC 4 goes high, depending upon the status of IC 7, IC 6 and IC 5 jam lines, delay FF IC 2 is clocked. The delayed Q output of IC 2/13 is applied to nor gate IC 10/1. The output of IC 10/3 is inverted by nor gate IC 10/5-7. The output of IC 10/4 now resets IC 3/4, Q output IC 3/1 goes low and not Q output IC 3/2 high. This pulse also passes to IC 17/4 of the CTD data store, setting its not Q output IC 17/2 high. This subsequently prevents further data characters being clocked out.

The Q3 output of counter IC 5 is also applied to the nor gate IC 1/1. The output of IC 1/3 is inverted by nor gate IC 1/5-6. The output of IC 1/4 now resets counters IC 7, IC 6 and IC 5 to their preset counts. As the not Q output of IC 3/2 goes high, after both the header and required amount of data has been clocked, nand gate IC 12/1 goes high. IC 12/2 is disabled by the not Q output of IC 13 being low. However, if the Run/Halt switch is returned to halt, then IC 13/4 would be pulsed high as capacitor C8 charges up the Q output IC 13/1 goes low and not Q output IC 13/2 high. Nand gate IC 12/2 will then be enabled, and at the end of the header-data sequence, IC 12/3 will go low and is inverted by nand gate IC 12/5-6.

The output of IC 12/4 then clocks delay FF IC 11. The Q output of IC 11/13 then pulses the Write End of File line of the tape buffer, via Darlington transistor pair Tr 6 and Tr 5. As IC 4/9 goes high at the end of the header-data sequence, IC 16/3 is clocked. The Q output of IC 16/1 then drives the Inter Record Gap line of the tape buffer, via Darlington transistor pair Tr 9 and Tr 10. This IRG pulse causes the second tape buffer to be selected. The first buffer is then

dumped to magnetic tape. If the Run/Halt switch remains in the run position, then the sequence of header-data output will continue.

3.7 Header/clock store

The function of this circuit is to store the 64 character header initially typed into the header store. Information from the real time clock, plus eight pad characters, are added, bringing the overall header to eighty characters. Switching of characters between header and CTD data, for transfer to the tape buffer, is also accomplished by this circuit.

The only power-up reset performed on this circuit is by the capacitor/resistor network on IC 33/5. The output of IC 33/4 is inverted by IC 33/12-13 to reset IC 28/4 IC 29/4. The Q output of IC 28/1 goes low and the not Q output IC 28/2, D input IC 28/5 and clock input IC 28/11 go high. The Q output of IC 29/1 goes low and the not Q output IC 29/2 high. The ka select pin 9 of and-or select gate IC 30 is set low by IC 28/1 and kb select pin 14 set high.

The clock on paralleled pins 1, 3, 5 and 7 of IC 30 is thus enabled. This clock comes from the record/header counter when the write header mode is in operation, and comprises eighty pulses. However, this clock will not start until the record/header counter is set in the run mode.

When the load header switch is operated, nand gate IC 32/2 is enabled. The circuit now waits until the header store completes a cycle. A pulse from IC 23/13 of the header store signifies this condition and is applied to IC 32/1. The output of IC 32/3 is inverted by nand gate IC 32/5-6. The output of IC 32/4 is then applied to nand gate IC 32/9. This gate is enabled by the high level of IC 29/2. The output of IC 32/10 is inverted by nand gate IC 32/12-13. The output of IC 32/11 now clocks IC 28/2. The Q output of IC 28/1 goes high and the not Q output IC 28/2 low. The state of the ka and kb select pins of IC 30 now reverses, and allows the clock from IC 10 of the character generator to pass. This clock occurs as each character is shifted through the header store and displayed on the 'scope. These clock pulses are applied to the 64 stage shift registers, IC 21 to IC 27 and to eight bit shift registers, IC 14 to IC 20 and IC 7 to IC 13.

The mode control pins 10 of IC 21 to IC 27 are held high by IC 28/2. This places these registers in the load mode. The data input pins 15 of IC 21 to IC 27 are fed in parallel with the data input pins 15 of the header shift registers. Thus with each clock pulse, as the header is recirculated, the registers IC 21 to IC 26 are loaded with this header. On the last or 64th character, nand gate IC 32/1 is again pulsed and IC 28/3 clocked via the other nand gates of IC 32, as before.

The Q output of IC 18/1 goes low and the not Q output IC 18/2 high again. This once again reverses the ka and kb select levels. IC 28/11 is clocked by IC 28/2 going high. The rising edge of the not Q output pulse of IC 28/12 clocks IC 29/11. The Q output of IC 29/13 now clocks IC 29/3. The Q output of IC 29/1 goes high, and turns on an LED via Darlington transistor pair Tr 2 and Tr 1, to show that the header has been loaded. The not Q output of IC 29/2 goes low and disables nand gate IC 32/8, thus preventing any further load header start pulses. The Q output of IC 29/13 being pulsed applies a set pulse to delay FFs IC 31/6 and IC 6/6. The Q output of IC 31/13 is applied to the parallel shift pins 9 of IC 7 to IC 13. This clocks eight null or pad characters into these ICs. The Q output of delay FF IC 6/13 parallel shifts the eight word time information into registers IC 14 to IC 20. On the record/header circuit being placed in the Run mode, the eighty pulse header shift clock is switched by IC 30 to all the registers, due to kb being high. The mode pins 10 of IC 21 to IC 27 are also now high, placing these registers in the recirculate mode.

The data outputs of registers IC 21 to IC 27 are applied to the serial input pins 11 of IC 14 to IC 20. The serial output pins 3 of IC 14 to IC 20 are applied in turn to the serial input pins 11 of IC 7 to IC 13. The serial output pins 3 of IC 7 to IC 13 are then applied to and-or select gates, IC 2 and IC 4. These outputs are also fed back to the recirculate data pins of the 64 stage shift registers.

The kb select pin 14 of IC 2 and IC 4 is held low by the Frame Sync enable from IC 3/1 of the record/header circuit being low. The kb select is inverted by the output of nand gate IC 5/12-13, to drive the ka select. Thus the outputs of registers IC 7 to IC 13 are

switched through IC 2 and IC 4 to inverting buffers and thence to the tape buffer. At the end of eighty shift clock pulses, the Frame Sync enable level from the record header counter goes high. This then reverses the state of the ka and kb lines, and output from the CTD data store is now switched through IC 2 and IC 4. CTD data is now output to tape buffer. A one second pulse from the real time clock is applied to nand gate IC 5/2. IC 5/2 is enabled by the Frame Sync enable level. The output of IC 5/3 is inverted by nand gate IC 5/8-9. The output of IC 5/10 clocks delay FF IC 6. The Q output of IC 6/13 parallel shifts the real time clock during this period. This ensures that the time can only be loaded, either at the end of the initial load header sequence, or during the write data period. This prevents any corruption of the header when it is being written, due to parallel shifting data in, as the registers are being serially shifted out. The process of switching between header and data now continues until the record/header circuit is halted.

Placing the load header switch in the off position connects nor gate IC 33/1-2 to ground. IC 33/3 goes high and drives nor gate IC 33/6 through capacitor C7. The output of IC 33/4 is inverted by nor gate IC 33/12-13. The output of IC 33/11 now resets IC 28 and IC 29. The circuit is now in its initial state and a new header may be loaded, as previously described.

3.8 Real time clock

The function of this circuit is to provide time data for the header/clock store, together with a visual display. Although there are many integrated clock circuits commercially available, output of the actual BCD data for each of the digits is not normally provided. It was decided therefore to construct a purpose-built circuit, which although having a high component count, is in fact quite simple.

The oscillator used is a standard crystal controlled type, formed around an inverting gate, in this case either a nor or nand gate is used. The crystal used is a 32,768 Hz AT cut type. Resistors R2, R3 and R4, together with capacitors C1 and C2, serve to tune the oscillator to a precise frequency. The output of the oscillator nor gate IC 8 is buffered by the remaining nor gates of IC 8.

IC 9, IC 10 and IC 12 are three binary/decade up/down counters. The binary count up mode is selected. Each of these counters divides by 16, to give an overall count of 4096. The carry out of IC 12 clocks a fourth binary counter IC 11 and the Q3 output is taken. This divides by a further eight, bringing the total to 32768, thus providing a one second pulse output.

The first thing to consider is how the clock is initially set up. The seconds, minutes and hours reset switches are placed in the reset position. The high level on the reset seconds switch is applied directly to IC 13/15, resetting its count to zero. Nor gate IC 3/1 goes high and its output IC 3/3 low. This is inverted by nor gate IC 3/5-6, and the high output of IC 3/4 applied to IC 14/1, resetting the tens of seconds counter to zero.

Similarly, the minutes counter IC 15/1 is reset directly by the minutes reset switch. The high level on this switch is applied to nor gate IC 5/13. The output of IC 5/11 is inverted by nor gate IC 5/8-9, and the high level of IC 5/10 applied to IC 16/1, resetting the tens of minutes counter to zero. The high level on the hours reset switch is applied to nor gate IC 1/2. The output of IC 1/3 goes low and is inverted by nor gate IC 1/12-13, whose output IC 1/11 now goes high. This output is applied to both IC 17/1 and IC 18/1, resetting both the hours and tens of hours to zero. The minutes and hours reset switches can now be returned to their off positions, leaving the seconds switch in the reset position.

Having completed the reset operation, the next step is to load a preset time into the hours and minutes counters. The time chosen will be in advance of when the clock is required to start from.

Placing the minutes update switch in the update position applies a high level to nor gate IC 2/5 and a low on IC 2/1. The output of IC 2/3 goes high and feeds back to IC 2/6. The output of IC 2/4 goes low, together with IC 2/2. The low output of IC 2/4 is also applied to IC 2/12. With the one second clock now passing to IC 15/15, the minutes count updates every second. On a count of ten, IC 15 returns to its zero count and the carry out of IC 15/7 clocks the tens of minutes counter. This process will continue until the chosen time is

reached, when the update switch will be turned off. This sets IC 2/5 low and IC 2/1 high. IC 2/3 goes low along with IC 2/6. IC 2/4, IC 2/2 and IC 2/12 go high. The output of IC 2/11 now remains low, and the one second clock is disabled.

The hours update switch, IC 6 and IC 1/9, is connected in exactly the same way, thus allowing the one second clock through IC 6/13 to update the hour counters IC 17 and IC 18. When the required count has been set, all that remains to do is to switch the seconds reset off at the appropriate time to start the clock.

The one second clock is now applied to IC 13/15. This resets to zero after a count of ten, when its carry out IC 15/7 goes high, clocking IC 14/15. The Q1 output of IC 14/6 is inverted by nor gate IC 8/8-9. The output of IC 3/10 is then nand gated with the Q2 and Q3 outputs of IC 14/1 and IC 14/14. On a count of six, the Q2 and Q3 outputs of IC 14 go high, and together with the inverted Q1 output, cause the dual triple input nand gate IC 4/9 to go low. Nor gate IC 2/9 also goes low. The output of IC 2/10 now goes high and clocks the hours counter IC 15/15, via nor gate IC 1/6. The output of IC 4/9 is also inverted by nor gate IC 3/12-13, applying a high level to nor gate IC 3/2. The low output of IC 3/4 is inverted by nor gate IC 2/5-6, and resets IC 14/1 back to zero, with nand gate IC 4 returning to its initial state.

Similarly, the carry out of minutes counter IC 15/7 clocks IC 16/15. Once again, the Q1, Q2 and Q3 outputs of the tens of minutes counter are gated to increment the hours, and reset the tens of minutes to zero.

The Q output of hours counter IC 17 and the Q2 output of tens of hours counter IC 18 both go high on a count of 24. These two outputs are applied to nand gate IC 7/8 and IC 7/9. The output of IC 7/10 is inverted by nand gate IC 7/12-13. This is then nor gated by IC 1/1 and the hours reset. The output of IC 1/3 is inverted by nor gate IC 1/12-13, and applied to both reset pins 1 of IC 17 and IC 18.

The Q1 to Q4 outputs of the seconds, minutes and hours counters drive IC 19, IC 21 and IC 23 respectively. IC 20 and IC 22 are driven

by the Q1 to Q3 outputs of IC 14 and IC 16, whilst only the Q1 and Q2 outputs of IC 18, drive IC 24. IC 19 to IC 24 are identical BCD to seven segment decoder drivers. The decoded outputs of these ICs then drive the Liquid Crystal Display (LCD).

A 64 Hz square wave is taken from the initial divider, IC 12/11, and supplies the AC drive necessary for the LCD display. This 64 Hz square wave is nand gated by IC 7/8 and IC 7/9 to drive the colon, separating the hours, minutes and seconds on the display. The BCD outputs of the counters IC 13 to IC 18 are also output, for inclusion in the header/clock store.

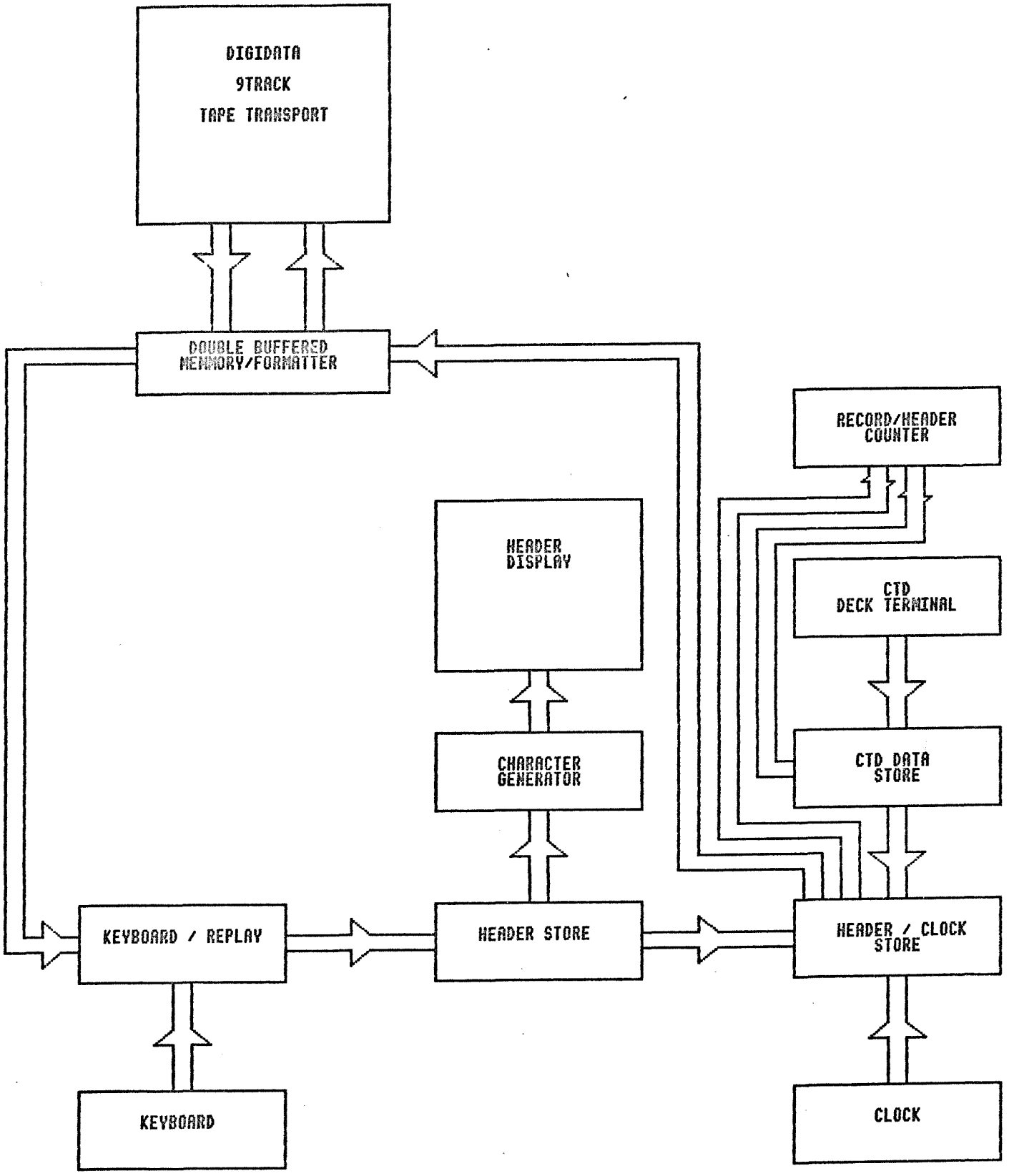
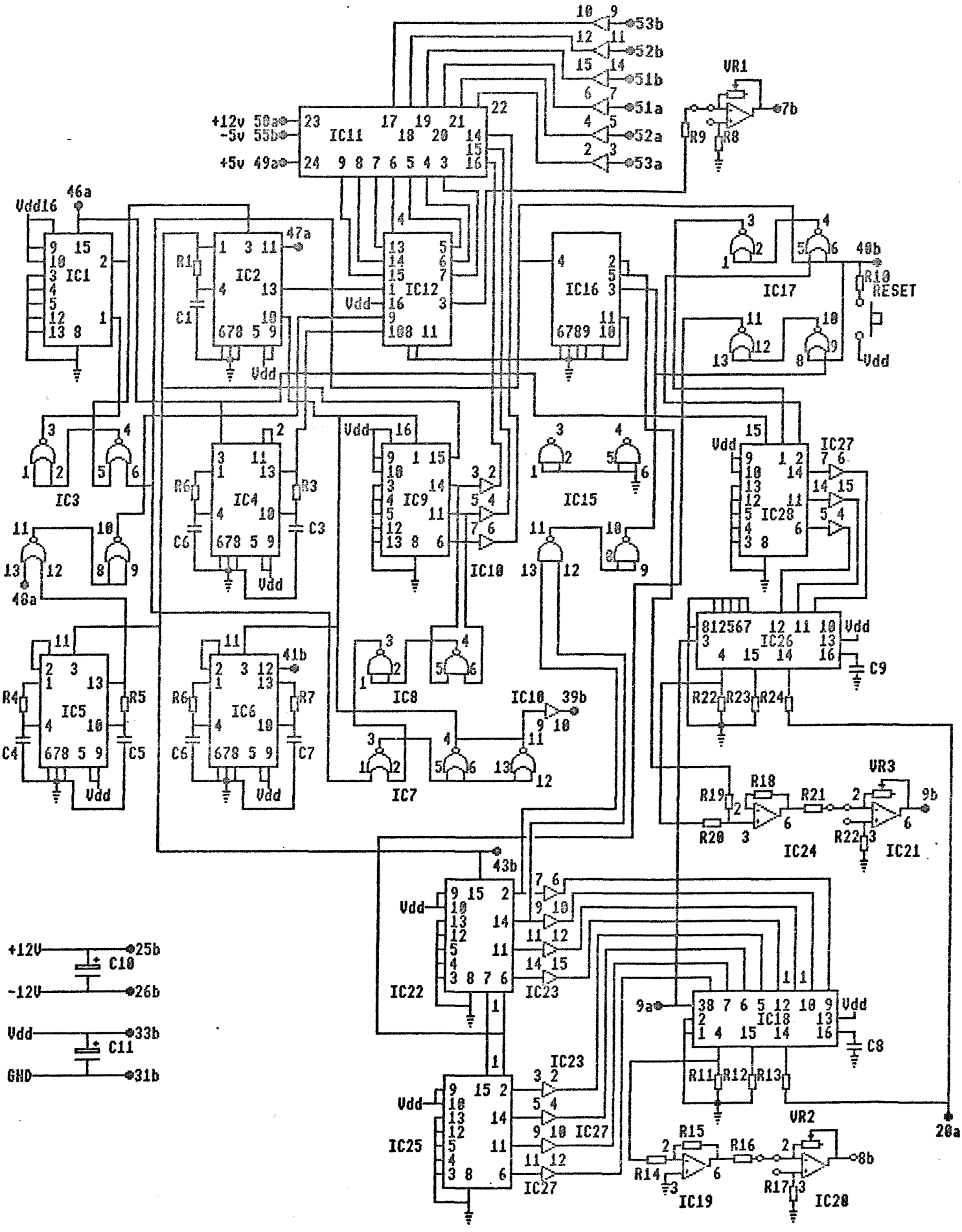


FIG.1

Block Diagram of Digidata - CTD Data Logger.

5. CIRCUIT DIAGRAMS AND PARTS LISTS



S1.DIGIDATA INTERFACE.

Character Generator.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
IC1	INTEGRATED CIRCUIT	CD4029	BINARY/DECIMAL COUNTER	RCA
IC2	,,	CD4013	DUAL D TYPE FLIP FLOP	,,
IC3	,,	CD4001	QUAD 2 INPUT NOR GATE	,,
IC4	,,	CD4013	DUAL D TYPE FLIP FLOP	,,
IC5	,,	CD4013	,,	,,
IC6	,,	CD4013	,,	,,
IC7	,,	CD4001	QUAD 2 INPUT NOR GATE	,,
IC8	,,	CD4011	QUAD 2 INPUT NAND GATE	,,
IC9	,,	CD4029	BINARY/DECIMAL COUNTER	,,
IC10	,,	CD4050	HEX NON INVERTING BUFFER	,,
IC11	,,	2516N	DOT MAT CHARACTER GENr	NATIONAL SEMICONDUCTORS
IC12	,,	CD4021	8 BIT PAR/SER SHIFT REG	RCA
IC13	,,	CD4050	HEX NON INVERTING BUFFER	,,
IC14	,,	u741	OPERATIONAL AMPLIFIER	,,
IC15	,,	CD4011	QUAD 2 INPUT NAND GATE	,,
IC16	,,	CD4013	DUAL D TYPE FLIP FLOP	,,
IC17	,,	CD4001	QUAD 2 INPUT NOR GATE	,,
IC18	,,	MC1408L8	8 BIT DAC	MOTOROLA
IC19	,,	u741	OPERATIONAL AMPLIFIER	RCA
IC20	,,	,,	,,	,,
IC21	,,	,,	,,	,,
IC22	,,	CD4029	BINARY/DECIMAL COUNTER	,,
IC23	,,	CD4050	HEX NON INVERTTING BUFFER	,,
IC24	,,	u741	OPERATIONAL AMPLIFIER	,,
IC25	,,	CD4029	BINARY/DECIMAL COUNTER	,,
IC26	,,	MC1408L6	6 BIT DAC	MOTOROLA
IC27	,,	CD4050	HEX NON INVERTING BUFFER	RCA
IC28	,,	CD4029	BINARY/DECIMAL COUNTER	,,
R1	RESISTOR	10K	1/4 WATT METAL FILM	TYPE MRF4 VARIOUS
R2	,,	10K	,,	,,
R3	,,	4K7	,,	,,
R4	,,	10K	,,	,,
R5	,,	10K	,,	,,
R6	,,	4K7	,,	,,
R7	,,	10K	,,	,,
R8	,,	10K	,,	,,
R9	,,	10K	,,	,,
R10	,,	4K7	,,	,,
R11	,,	1K	,,	,,
R12	,,	1K	,,	,,
R13	,,	1K	,,	,,
R14	,,	33K	,,	,,
R15	,,	33K	,,	,,

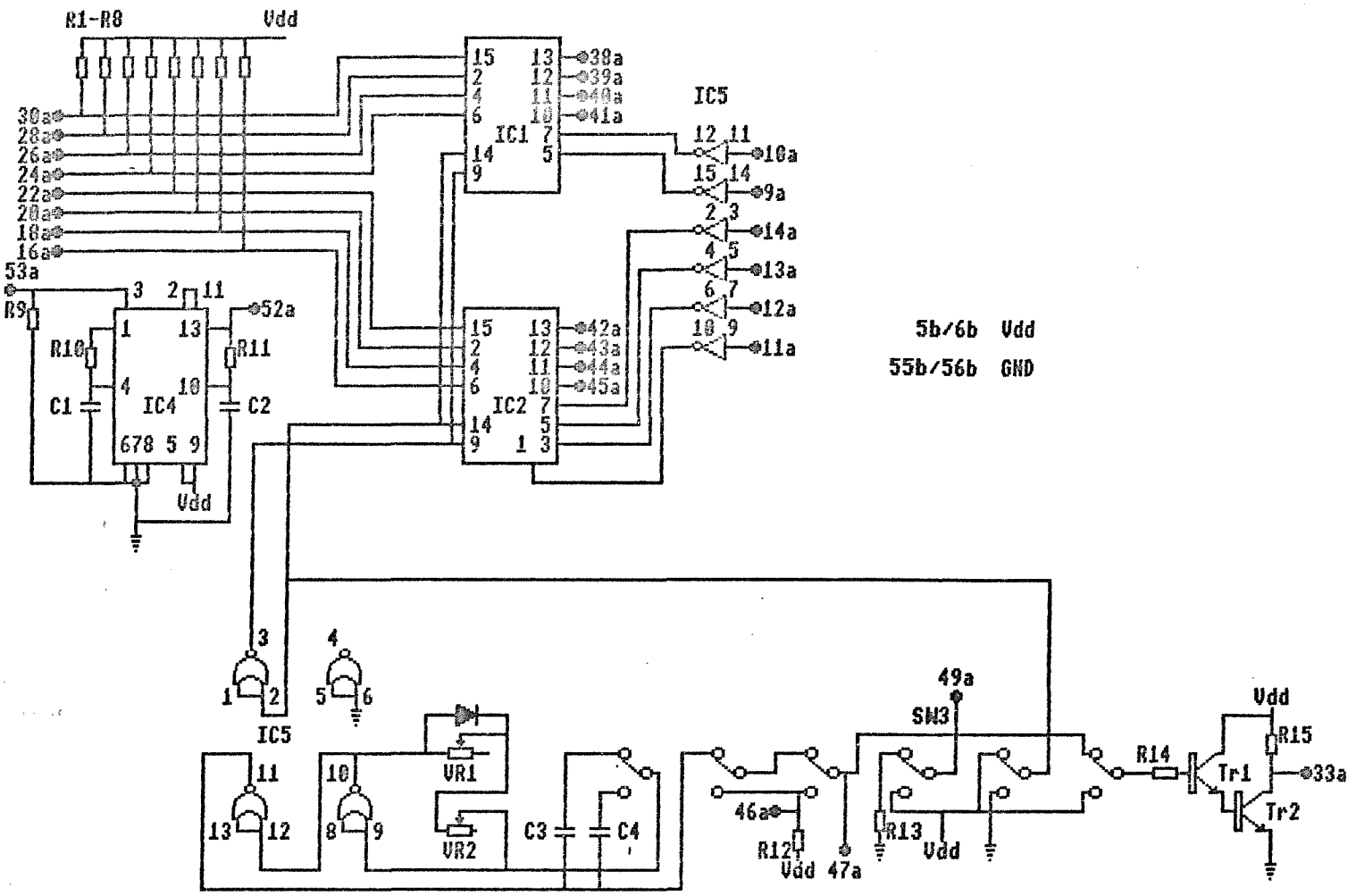
S1.DIGIDATA INTERFACE

Character Generator-Timebase.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
R16	RESISTOR	10K	1/4 WATT METAL FILM	TYPE MRF4
R17	,,	10K	,,	
R18	,,	10K	,,	
R19	,,	10K	,,	
R20	,,	820K	,,	
R21	,,	1K	,,	
R22	,,	1K	,,	
R23	,,	1K	,,	
R24	,,	33K	,,	
R25	,,	33K	,,	
C1	CAPACITOR	100p	CERAMIC 8123Z/COG 10% 100V	STC
C2	,,	100p	,,	,,
C3	,,	47p	POLYESTER TFF 20% 400V	WIMA
C4	,,	220P	CERAMIC 8123Z/COG 10% 100V	STC
C5	,,	100p	,,	,,
C6	,,	470p//47p	,, + POLYESTER TFF 10%	STC + WIMA
C7	,,	100p	CERAMIC 8123Z/COG 10% 100V	STC
C8	,,	100p	,,	,,
C9	,,	100p	,,	,,
C10	,,	100u	TANTULAM BEAD 15V	RS No 102-746
C11	,,	100u	,,	,,
C12	,,	100u	,,	,,
VR1	POTENTIOMETER	100K	CERMET TYPE 81E 1/2 WATT	MORGAN
VR2	,,	100K	,,	,,
VR3	,,	100K	,,	,,
	IC SOCKETS		8 PIN	VERO 19-2176B
	,,		14 PIN	VERO 19-2177H
	,,		16 PIN	VERO 19-2178C
	,,		24 PIN	VERO 19-2182E
SW1	SWITCH	SPDT	BIAS 3A 250V KPA106F	WAYCOM MIN

S1.DIGIDATA INTERFACE

Character Generator-Timebase.



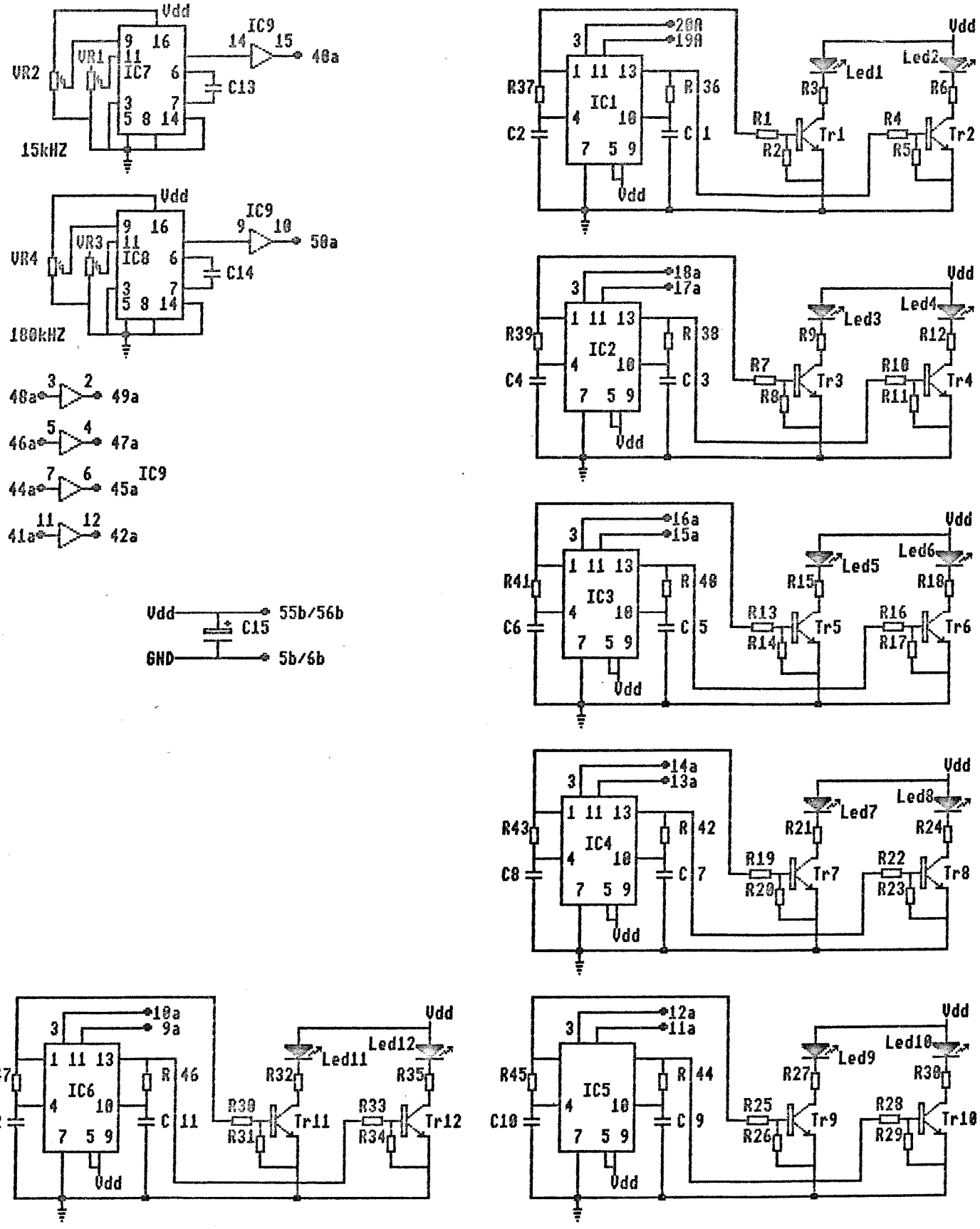
S2.DIGIDATA INTERFACE.

Keyboard Input/Replay.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
IC1	INTEGRATED CIRCUIT	CD4019	QUAD AND/OR SELECT GATE	RCA
IC2	,,	CD4019	,,	,,
IC3	,,	CD4049	HEX INVERTING BUFFER	,,
IC4	,,	CD4013	DUAL D TYPE FLIP FLOP	,,
IC5	,,	CD4001	QUAD NOR GATE	,,
R1-R8	RESISTOR	4K7	1/4 WATT METAL FILM	TYPE MRF4
R9	,,	10K	,,	,,
R10	,,	100K	,,	,,
R11	,,	100K	,,	,,
R12	,,	4K7	,,	,,
R13	,,	4K7	,,	,,
R14	,,	15K	,,	,,
R15	,,	1K	,,	,,
C1	CAPACITOR	.01u	MKS2 10% 63V	WIMA
C2	,,	220p	CERAMIC 8132Z/COG 10% 100V	STC
C3	,,	.033u	MKS2 10% 63V	WIMA
C4	,,	.33u	MKS2 10% 63V	WIMA
VR1	POTENTIOMETER	1M	CERMET TYPE 81E 1/2 WATT	MORGAN
VR2	POTENTIOMETER	1M	CERMET TYPE 81E 1/2 WATT	,,
	IC SOCKETS		14 PIN	VERO 19-2177H
	,,		16 PIN	VERO 19-2178C
TR1	TRANSISTOR		BC109	MULLARD
TR2	,,		BC109	,,
SW1	SWITCH	SPDT	4A 24V MST106D	MAYCOM MIN
SW2	,,	DPDT	4A 24V MST206 M/S	,,
SW3	,,	4PDT	6A 28V	RS No 378-995

S2.DIGIDATA INTERFACE

Keyboard Input-Replay.



S3. DIGIDATA INTERFACE.

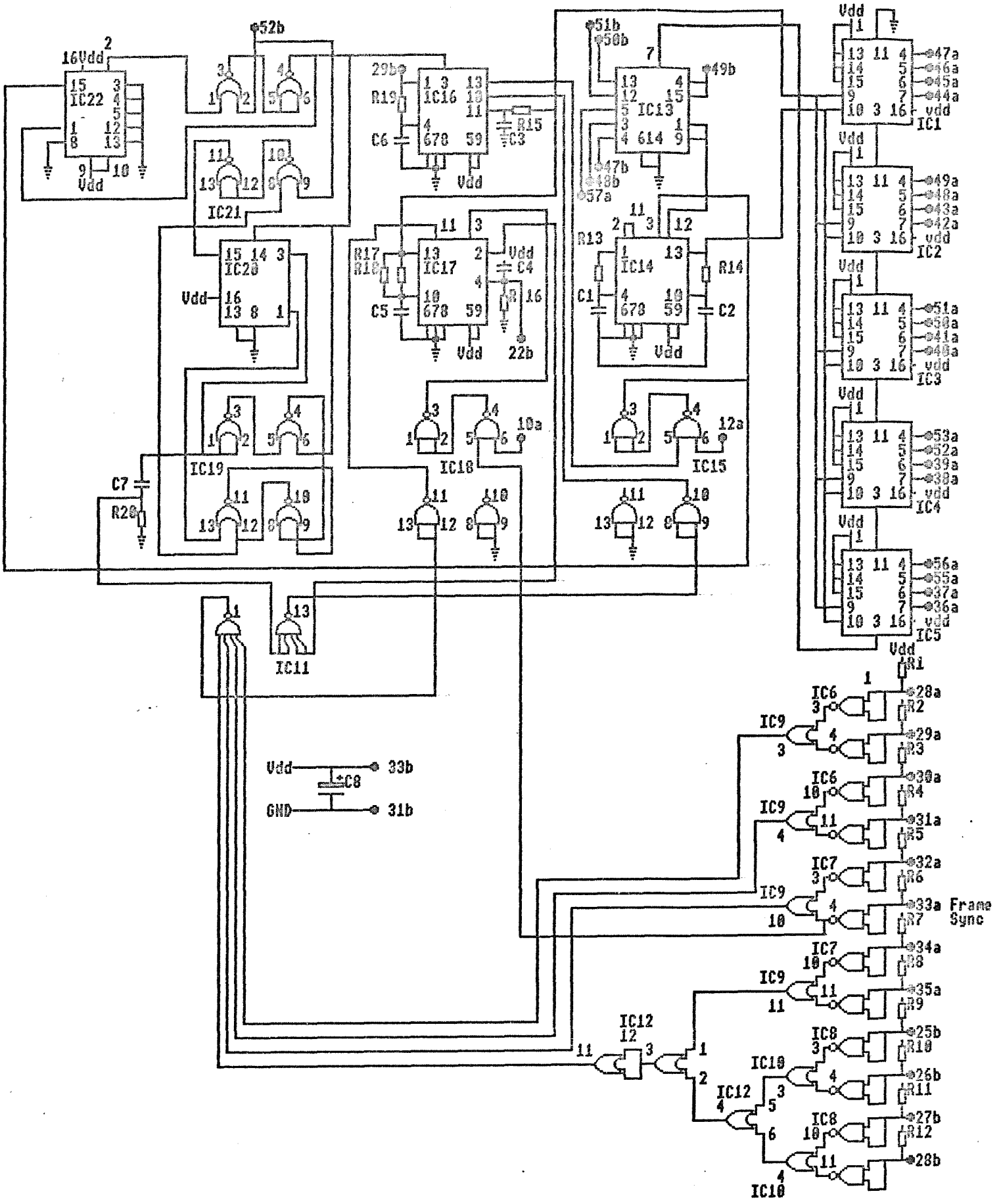
Oscillator and Strobe Display.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
IC1	INTEGRATED CIRCUIT	CD4013	DUAL D TYPE FLIP FLOP	RCA
IC2	"	"	"	"
IC3	"	"	"	"
IC4	"	"	"	"
IC5	"	"	"	"
IC6	"	"	"	"
R1	RESISTOR	82K	1/4 WATT METAL FILM	TYPE MRF4
R2	"	18K	"	"
R3	"	180R	"	"
R4	"	82K	"	"
R5	"	18K	"	"
R6	"	180R	"	"
R7	"	82K	"	"
R8	"	18K	"	"
R9	"	180R	"	"
R10	"	82K	"	"
R11	"	18K	"	"
R12	"	180R	"	"
R13	"	82K	"	"
R14	"	18K	"	"
R15	"	180R	"	"
R16	"	82K	"	"
R17	"	18K	"	"
R18	"	180R	"	"
R19	"	82K	"	"
R20	"	18K	"	"
R21	"	180R	"	"
R22	"	82K	"	"
R23	"	18K	"	"
R24	"	180R	"	"
R25	"	82K	"	"
R26	"	18K	"	"
R27	"	180R	"	"
R28	"	82K	"	"
R29	"	18K	"	"
R30	"	180R	"	"
R31	"	82K	"	"
R32	"	18K	"	"
R33	"	180R	"	"
R34	"	82K	"	"
R35	"	18K	"	"
R36	"	180R	"	"
R37-R48	"	1M	"	"

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
C1-C12	CAPACITOR	.022u	MKS2 10% 63V	WIMA
C13	''	1000p	CERAMIC 8132Z/COG 10% 100V	STC
C14	''	100p	''	''
C15	''	100u	TANTULUM BEAD 15V	RS No 102-746
VR1	POTENTIOMETER	50K	CERMET TYPE 81E 1/2 WATT	MORGAN
VR2	''	''	''	''
VR3	''	''	''	''
VR4	''	''	''	''
TR1-TR12	TRANSISTOR		BC109	MULLARD
Led1-12	LED		MIN LOW CURRENT LED	RS No 588-386
IC7	INTEGRATED CIRCUIT	CD4050	HEX NON INVERTING BUFFER	RCA
	IC SOCKETS		14 PIN	VERO 19-2177H
	''		16 PIN	VERO 19-2178C

S3.DIGIDATA INTERFACE

Oscillator and Strobe Display.



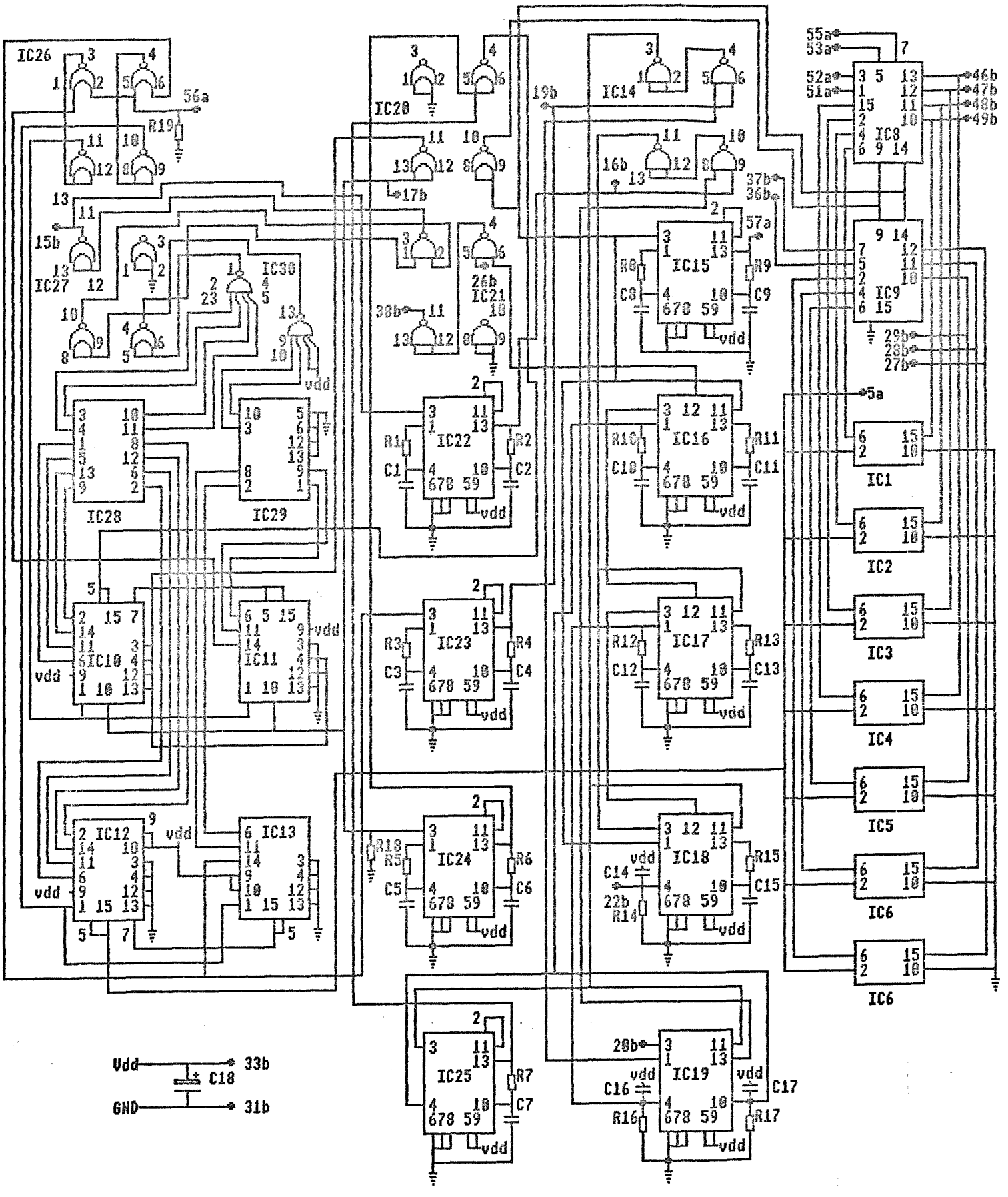
S4. DIGIDATA INTERFACE.

CTD Data Store.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
IC1-5	INTEGRATED CIRCUIT	CD4021	8 BIT PAR/SER SHIFT REG	RCA
IC6-8	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC9	"	CD4071	QUAD 2 INPUT OR GATE	"
IC10	"	"	"	"
IC11	"	CD4002	DUAL 4 INPUT NOR GATE	"
IC12	"	CD4071	QUAD 2 INPUT OR GATE	"
IC13	"	CD4012	DUAL D TYPE FLIP FLOP	"
IC14	"	"	"	"
IC15	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC16	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC17	"	"	"	"
IC18	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC19	"	CD4001	QUAD 2 INPUT NOR GATE	"
IC20	"	CD4017	DECADE COUNTER/DIVIDER	"
IC21	"	CD4001	QUAD 2 INPUT NOR GATE	"
IC22	"	CD4029	BIN/DEC COUNTER	"
R1-12	RESISTOR	33K	1/4 WATT METAL FILM	TYPE MFR4
R13	"	100K	"	"
R14	"	100K	"	"
R15	"	12K	"	"
R16	"	120K	"	"
R17	"	3K3	"	"
R18	"	120K	"	"
R19	"	120K	"	"
R20	"	27K	"	"
C1	CAPACITOR	100p	CERAMIC 8132Z/COG 10% 100V	STC
C2	"	1000p	"	"
C3	"	100p	"	"
C4	"	220p	"	"
C5	"	330p	"	"
C6	"	220p	"	"
C7	"	1000p	"	"
C8	"	100u	TANTULAM BEAD 15V	RS No 102-746
	IC SOCKETS		14 PIN	VERO 19-2177H
	"		16 PIN	VERO 19-2178C

S4.DIGIDATA INTERFACE

CTD Data Store.



S5.DIGIDATA INTERFACE.

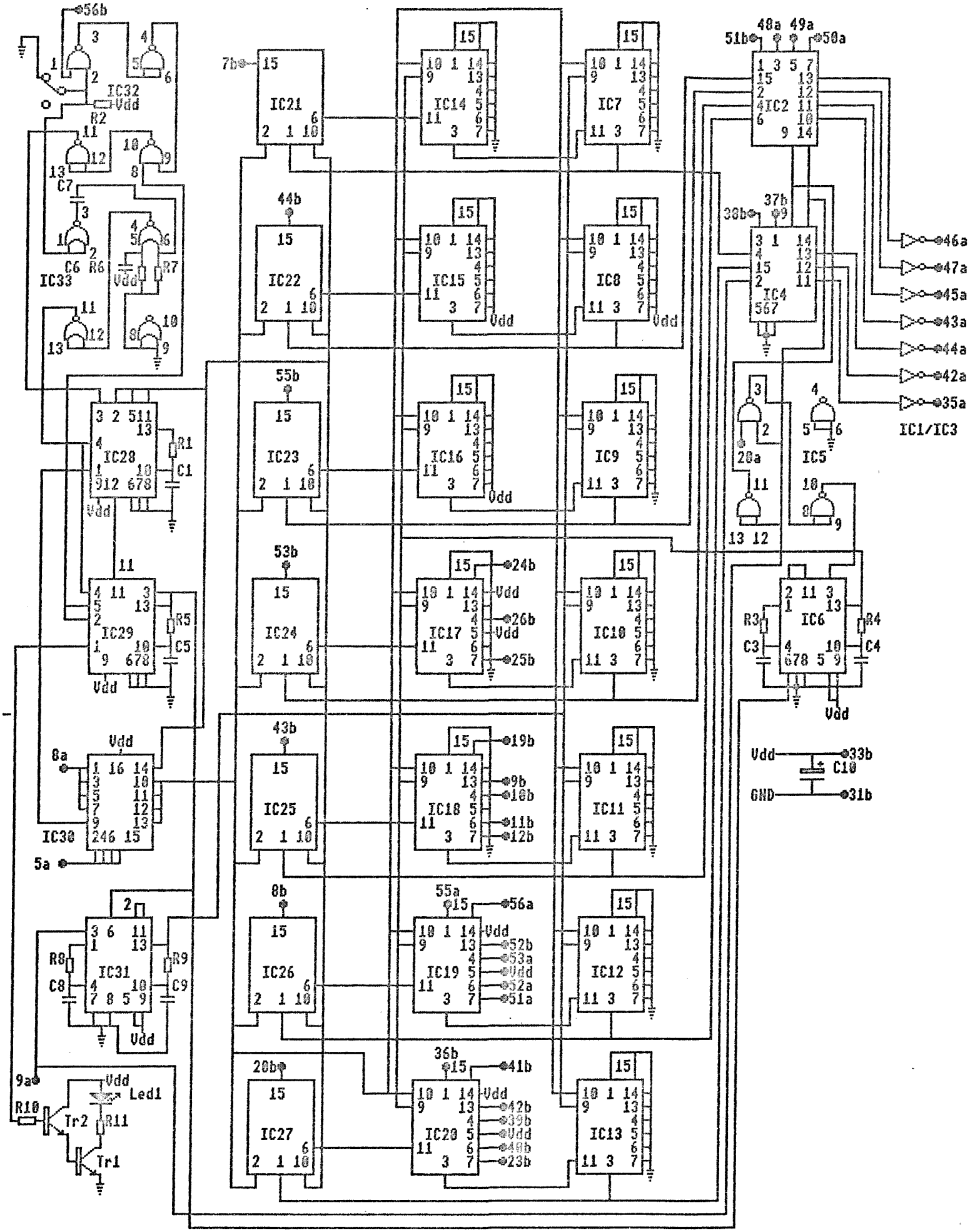
Header Store.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
IC1	INTEGRATED CIRCUIT	CD4031	64 STAGE SHIFT REGISTER	RCA
IC2	"	"	"	"
IC3	"	"	"	"
IC4	"	"	"	"
IC5	"	"	"	"
IC6	"	"	"	"
IC7	"	"	"	"
IC8	"	CD4019	QUAD AND/OR SELECT GATE	"
IC9	"	"	"	"
IC10	"	CD4029	BINARY/DECIMAL COUNTER	"
IC11	"	"	"	"
IC12	"	"	"	"
IC13	"	"	"	"
IC14	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC15	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC16	"	"	"	"
IC17	"	"	"	"
IC18	"	"	"	"
IC19	"	"	"	"
IC20	"	CD4001	QUAD 2 INPUT NOR GATE	"
IC21	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC22	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC23	"		"	"
IC24	"		"	"
IC25	"		"	"
IC26	"	CD4001	QUAD 2 INPUT NOR GATE	"
IC27	"	"	"	"
IC28	"	CD4030	HEX 2 INPUT EXCL OR GATE	"
IC29	"	"	"	"
IC30	"	CD4012	DUAL 4 INPUT NAND GATE	"
R1	RESISTOR	10K	1/4 WATT METAL FILM	TYPE MRF4
R2	"	10K	"	"
R3	"	10K	"	"
R4	"	4K7	"	"
R5	"	10K	"	"
R6	"	10K	"	"
R7	"	10K	"	"
R8	"	4K7	"	"
R9	"	10K	"	"
R10	"	10K	"	"
R11	"	4K7	"	"
R12	"	100K	"	"
R13	"	10K	"	"

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
R14	RESISTOR	100K	1/4 WATT METAL FILM	TYPE MRF4
R15	"	10K	"	"
R16	"	100K	"	"
R17	"	100K	"	"
R18	"	27K	"	"
R19	"	27K	"	"
C1	CAPACITOR	100p	CERAMIC 8123Z/C0G 10% 100V	STC
C2	"	100p	"	"
C3	"	100p	"	"
C4	"	47p	"	"
C5	"	100p	"	"
C6	"	100p	"	"
C7	"	100p	"	"
C8	"	47p	"	"
C9	"	100p	"	"
C10	"	100p	"	"
C11	"	100p	"	"
C12	"	100p	"	"
C13	"	100p	"	"
C14	"	100p	"	"
C15	"	100p	"	"
C16	"	100p	"	"
C17	"	100p	"	"
C18	"	100u	TANTALUM BEAD 15V	RS No 102-746
	IC SOCKETS		14 PIN	VERO 19-2177H
	"		16 PIN	VERO 19-2178C

S5.DIGIDATA INTERFACE.

Header Store.



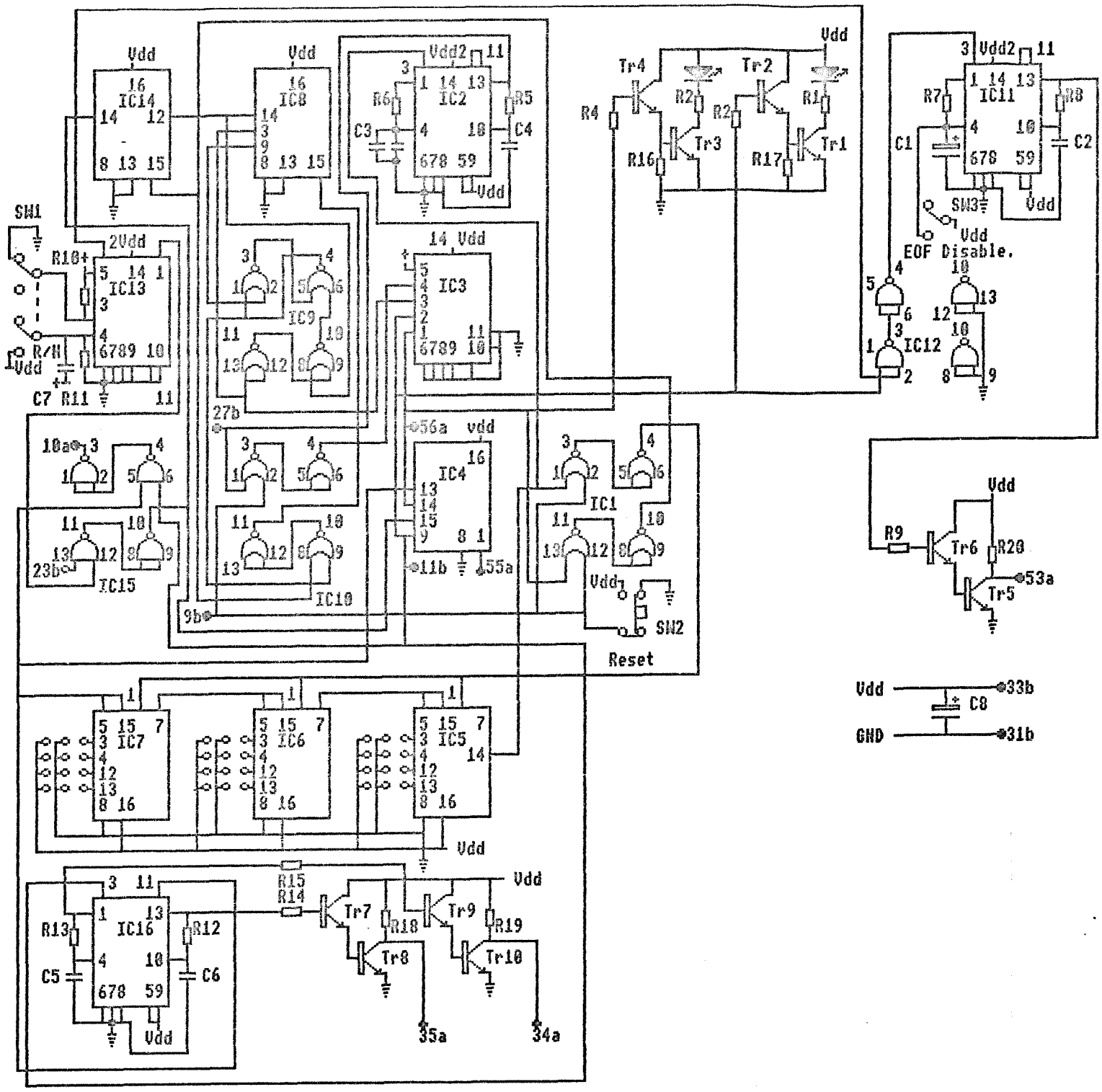
S6.DIGIDATA INTERFACE.

Header/Clock Store.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
IC1	INTEGRATED CIRCUIT	CD4049	HEX INVERTING BUFFER	RCA
IC2	"	CD4019	QUAD AND/OR SELECT GATE	"
IC3	"	CD4049	HEX INVERTING BUFFER	"
IC4	"	CD4019	QUAD AND/OR SELECT GATE	"
IC5	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC6	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC7-20	"	CD4021	8 BIT PAR/SER SHIFT REG	"
IC21-27	"	CD4031	64 STAGE SHIFT REGISTER	"
IC28	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC29	"	"	"	"
IC30	"	CD4019	QUAD AND/OR SELECT GATE	"
IC31	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC32	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC33	"	CD4001	QUAD 2 INPUT NOR GATE	"
R1	RESISTOR	120K	1/4 WATT METAL FILM	TYPE MRF4
R2	"	27K	"	"
R3	"	120K	"	"
R4	"	120K	"	"
R5	"	100K	"	"
R6	"	27K	"	"
R7	"	27K	"	"
R8	"	120K	"	"
R9	"	120K	"	"
R10	"	1M	"	"
R11	"	180R	"	"
C1	CAPACITOR	220p	CERAMIC 8132Z/COG 10% 100V	STC
C2	"	---		"
C3	"	100p	"	"
C4	"	100p	"	"
C5	"	220p	"	"
C6	"	680p	"	"
C7	"	1000p	"	"
C8	"	1000p	"	"
C9	"	100p	"	"
C10	"	100u	TANTULUM BEAD 15V	RS No 102-746
TR1-2	TRANSISTOR		BC109	MULLARD
Led1	LED		LIGHT EMMITTING DIODE	RS No 587-715
SW1	SWITCH	SPDT	4A 24V MST106D	WAYCOM MIN
	IC SOCKETS		14 PIN	VERO 19-2177H
	"		16 PIN	VERO 19-2178C

S6.DIGIDATA INTERFACE.

Header/Clock Store.



S7. DIGIDATA INTERFACE.

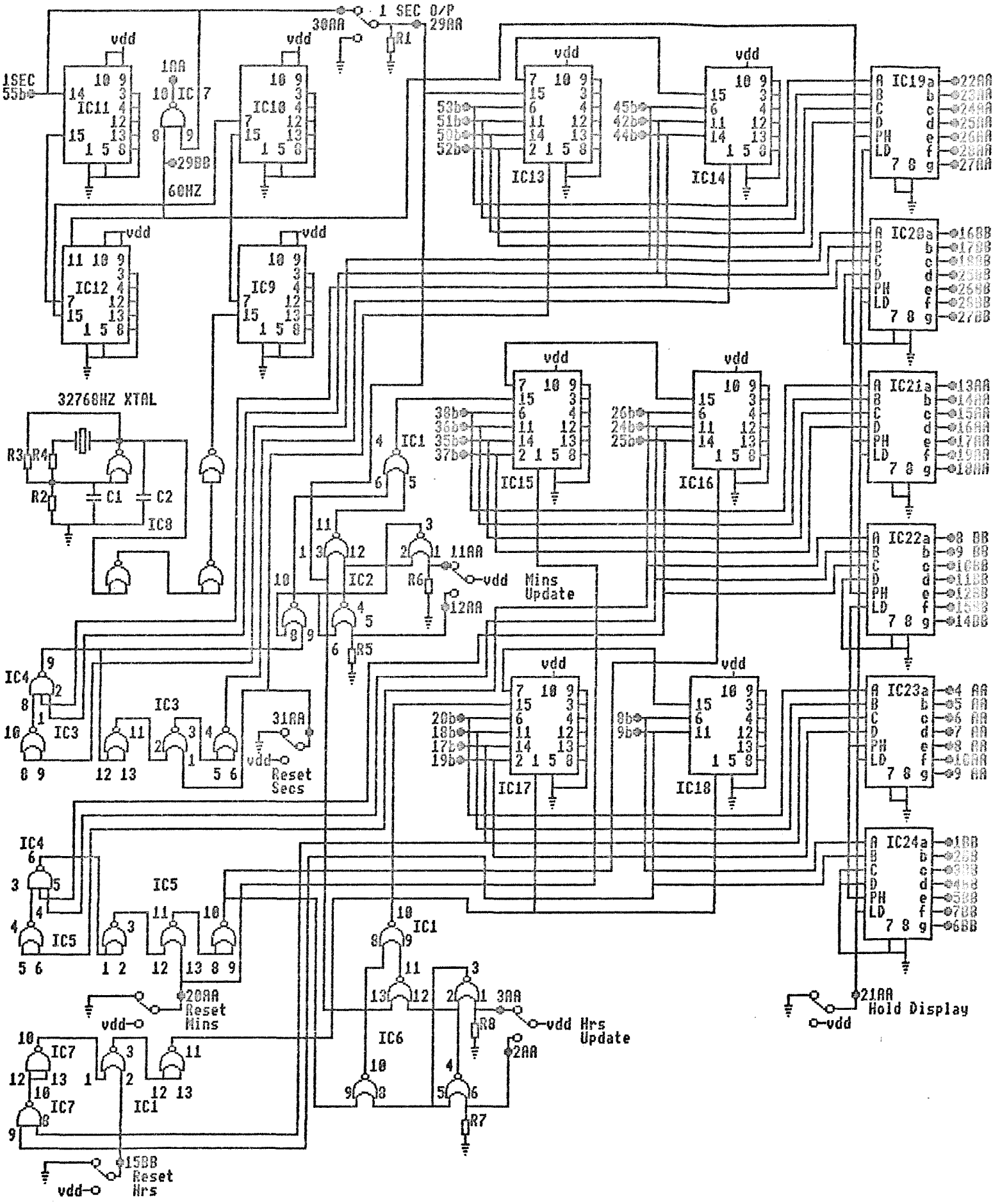
Record/Header counters.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
IC1	INTEGRATED CIRCUIT	CD4001	QUAD 2 INPUT NOR GATE	RCA
IC2	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC3	"	"	"	"
IC4	"	CD4019	QUAD AND/OR SELECT GATE	"
IC5-7	"	CD4029	BIN/DEC COUNTER	"
IC8	"	CD4017	DECADE COUNTER	"
IC9	"	CD4001	QUAD 2 INPUT NOR GATE	"
IC10	"	"	"	"
IC11	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC12	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC13	"	CD4013	DUAL D TYPE FLIP FLOP	"
IC14	"	CD4017	DECADE COUNTER	"
IC15	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC16	"	CD4013	DUAL D TYPE FLIP FLOP	"
R1	RESISTOR	100R	1/4 WATT METAL FILM	TYPE MFR4
R2	"	1M	"	"
R3	"	100R	"	"
R4	"	1M	"	"
R5	"	120K	"	"
R6	"	120K	"	"
R7	"	100K	"	"
R8	"	100K	"	"
R9	"	560K	"	"
R10	"	33K	"	"
R11	"	100K	"	"
R12	"	120K	"	"
R13	"	12K	"	"
R14	"	560K	"	"
R15	"	560K	"	"
R16	"	33K	"	"
R17	"	33K	"	"
R18	"	4K7	"	"
R19	"	4K7	"	"
R20	"	4K7	"	"
C1	CAPACITOR	1u	ELECTROLYTIC 15V	WIMA PRINTLYT
C2	"	.1u	CERAMIC 8132Z/COG 10% 100V	STC
C3	"	220p/330p	"	"
C4	"	220p	"	"
C5	"	330p	"	"
C6	"	220p	"	"
C7	"	220p	"	"
C8	"	100u	TANTALUM BEAD 15V	RS No 102-746

S7.DIGIDATA INTERFACE.

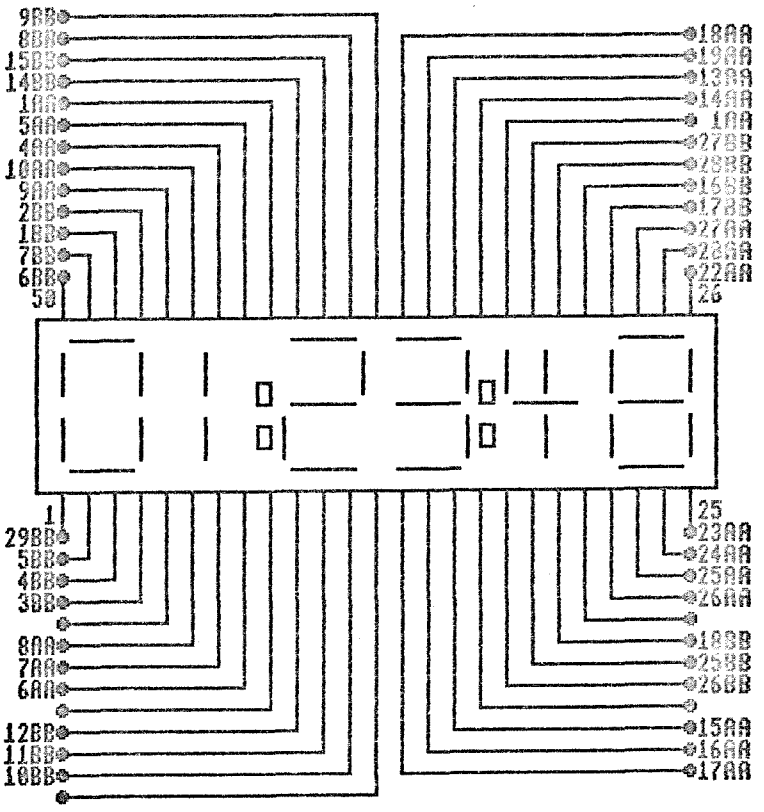
Record/Header Counters.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
TR1-10	TRANSISTOR		BC109	MULLARD
Led1-2	LED		LIGHT EMITTING DIODE	RS No 587-715
SW1	SWITCH	DPDT	4A 24V MST206 N/S	WAYCOM MIN
SW2	,,	SPDT	BIAS 3A 24V KPA106F	,,
SW3	,,	SPDT	4A 24V MST106D	,,
	IC SOCKETS		14 PIN	VERO 19-2177H
	,,		16 PIN	VERO 19-2178C



S8.DIGIDATA INTERFACE.

Clock.



LIQUID CRYSTAL DISPLAY.

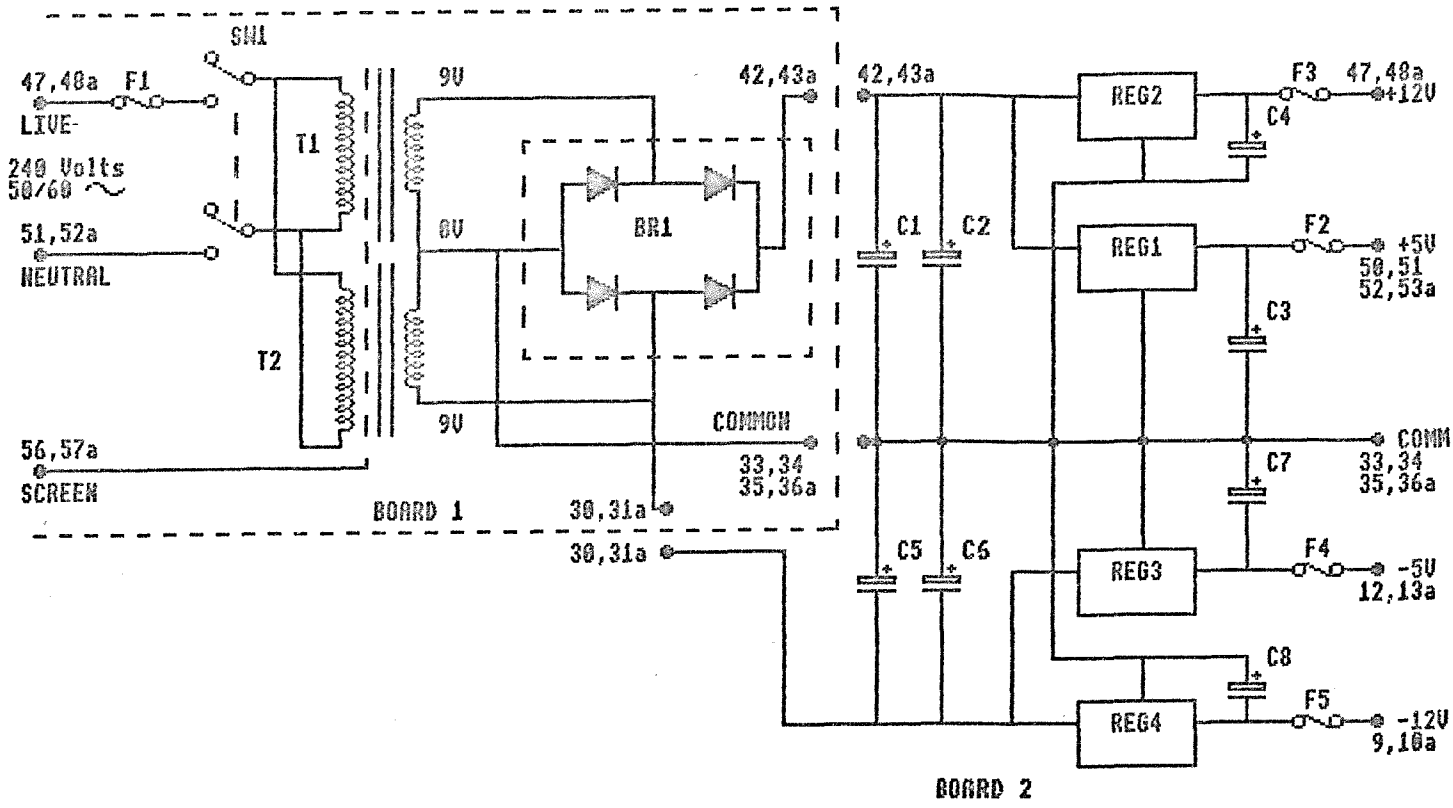
S8.DIGIDATA INTERFACE.

Clock.

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
IC1	INTEGRATED CIRCUIT	CD4001	QUAD 2 INPUT NOR GATE	RCA
IC2	"	"	"	"
IC3	"	"	"	"
IC4	"	CD4023	TRIPLE 3 INPUT NAND GATE	"
IC5	"	CD4001	QUAD 2 INPUT NOR GATE	"
IC6	"	"	"	"
IC7	"	CD4011	QUAD 2 INPUT NAND GATE	"
IC8	"	CD4001	QUAD 2 INPUT NOR GATE	"
IC9-18	"	CD4029	BINARY/DECIMAL COUNTER	"
IC19-24	"	CD4543	7 SEGMENT LCD DRIVER	"
R1	RESISTOR	33K	1/4 WATT METAL FILM	TYPE MRF4
R2	"	5M6	"	"
R3	"	5M6	"	"
R4	"	100K	"	"
R5	"	33K	"	"
R6	"	33K	"	"
R7	"	33K	"	"
R8	"	33K	"	"
C1	CAPACITOR	47p	"	STC
C2	"	1100p	"	"
	IC SOCKETS		14 PIN	VERO 19-2177H
	"		16 PIN	VERO 19-2178C
	ALL SWITCHES	DPDT	4A 24V MST206 N/S	MAYCOM MIN
XTAL	CRYSTAL		32768HZ	RS No 304-447
LCD	LIQUID CRYSTAL DISP		6 DIGIT	VEROSPEED No 89-20765G
	LCD BEZEL			VEROSPEED No 170-1837F

S8.DIGIDATA INTERFACE.

Clock.


SW1
47,48a
F1
LIVE-
240 Volts
50/60
51,52a
NEUTRAL
56,57a
SCREEN
T1
T2
9V
0V
9V
BR1
COMMON
33,34
35,36a
42,43a
30,31a
BOARD 1
42,43a
C1
C2
C5
C6
REG2
REG1
REG3
REG4
C4
C3
C7
C8
F3
47,48a
+12V
F2
+5V
50,51
52,53a
COMM
33,34
35,36a
F4
-5V
12,13a
F5
-12V
9,10a
BOARD 2

PART No	PART	TYPE	DESCRIPTION	MANUFACTURER
REG1	VOLTAGE REGULATOR	78H05	+5V 5 AMP REGULATOR	RS No 307-301
REG2	''	7812	+12V 1 AMP ''	RS No 305-894
REG3	''	7912	-12V 1 AMP ''	RS No 306-055
REG4	''	7905	-5V 1 AMP ''	RS No 306-049
BR1	BRIDGE RECTIFIER	6.6A	6.6 AMP 800V	RS No 262-056
C1	CAPACITOR	47u	TANTULUM BEAD 15V	RS No 101-844
C2	''	47u	''	''
C3	''	0.47u	'' 35V	RS No 101-765
C4	''	0.47u	'' 35V	''
C5	''	47u	'' 15V	RS No 101-844
C6	''	47u	'' 15V	''
TR1-TR2	TRANSFORMER	0-9V	20VA 9V 2.2 AMP	RS No 207-510
SW1	MAINS SWITCH	GUARDED	250V AC 2A	RS No 335-643
	FUSEHOLDERS		250V 16A	RS No 412-863
F1	FUSES	1.25inch	250V 500mA	RS No 412-239
F2-5	''	''	250V 1 AMP	RS No 412-251

6. BACKPLANE WIRING SCHEDULE

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31		1		31	S2-55B,S2-56B 0V
2		32		2		32	
3		33		3		33	S2-6B,S2-5B +5V
4		34		4		34	
5		35		5		35	
6		36		6		36	
7		37		7	Z MOD OUTPUT	37	
8		38		8	HOR' OUTPUT	38	
9	S1-50A	39		9	VERT' OUTPUT	39	S6-5A,S5-5A
10		40		10		40	S5-56A
11		41		11		41	S5-22B
12		42		12		42	
13		43		13		43	
14		44		14		44	
15		45		15		45	
16		46	S5-38B	16		46	
17		47	S5-15B	17		47	
18		48	S5-57A	18		48	
19		49	S9-51A +5V	19		49	
20		50	S9-9A,S1-26B -12V	20		50	
21		51	S5-49B,S6-53B	21		51	S5-46B,S6-43B
22		52	S5-29B,S6-55B	22		52	S5-47B,S6-8B
23		53	S5-28B,S6-44B	23		53	S5-48B,S6-20B
24		54		24		54	
25		55		25	S9-46A +12V	55	S9-12A -12V
26		56		26	S1-9A -12V	56	
27		57		27		57	
28		58		28		58	
29		59		29		59	
30		60		30		60	

S1.DIGIDATA INTERFACE.

Character Generator.

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31		1		31	
2		32		2		32	
3		33	SKT2-1	3		33	
4		34		4		34	
5		35		5	S3-5B,SKT6-1 +5V	35	
6		36		6	S3-6B,SKT6-2	36	
7		37		7		37	
8		38		8		38	
9	SKT1-6	39	S5-35B	9		39	
10	SKT1-5	40	S5-36B	10		40	
11	SKT1-4	41	S5-37B	11		41	
12	SKT1-3	42	S5-51A	12		42	
13	SKT1-2	43	S5-52A	13		43	
14	SKT1-1	44	S5-53A	14		44	
15		45	S5-55A	15		45	
16	SKT6-13	46	SKT6-14	16		46	
17		47	S5-20B	17		47	
18	SKT6-12	48		18		48	
19		49	SKT2-3	19		49	
20	SKT6-11	50		20		50	
21		51		21		51	
22	SKT6-10	52	S5-17B	22		52	
23		53	SKT6-20	23		53	
24	SKT6-9	54		24		54	
25		55		25		55	S3-53B,SKT6-3
26	SKT6-8	56		26		56	S3-56B,SKT6-4
27		57		27		57	
28	SKT6-7	58		28		58	
29		59		29		59	
30	SKT6-6	60		30		60	

S2.DIGIDATA INTERFACE.

Keyboard Input-Replay.

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31		1		31	
2		32		2		32	
3		33		3		33	
4		34		4		34	
5		35		5	S4-33B +5V	35	
6		36		6	S4-33B	36	
7		37		7		37	
8		38		8		38	
9	S4-33A	39		9		39	
10	S4-32A	40	S7-23B,S4-12A	10		40	
11	S4-31A	41		11		41	
12	S4-30A	42		12		42	
13	S4-29A	43		13		43	
14	S4-28A	44		14		44	
15	S4-34A	45		15		45	
16	S4-35A	46		16		46	
17		47		17		47	
18		48		18		48	
19		49		19		49	
20		50	S5-26B	20		50	
21		51		21		51	
22		52		22		52	
23		53		23		53	
24		54		24		54	
25		55		25		55	S4-31B 0V
26		56		26		56	S4-31B
27		57		27		57	
28		58		28		58	
29		59		29		59	
30		60		30		60	

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31	SKT5-4,S3-11A	1		31	S5-31B 0V
2		32	SKT5-5,S3-10A	2		32	
3		33	SKT5-6,S3-9A	3		33	S5-33B +5V
4		34	SKT5-7,S3-15A	4		34	
5		35	SKT5-8,S3-16A	5		35	
6		36	SKT3-20	6		36	
7		37	SKT3-19	7		37	
8		38	SKT3-16	8		38	
9		39	SKT3-15	9		39	
10	S7-56A	40	SKT3-12	10		40	
11		41	SKT3-11	11		41	
12	S7-23B,S3-40A	42	SKT3-8	12		42	
13		43	SKT3-7	13		43	
14		44	SKT3-4	14		44	
15		45	SKT3-3	15		45	
16		46	SKT3-2	16		46	
17		47	SKT3-1	17		47	S6-37B
18		48	SKT3-6	18		48	S6-50A
19		49	SKT3-5	19		49	S6-49A
20		50	SKT3-10	20		50	S6-48A
21		51	SKT3-9	21		51	S6-57B
22		52	SKT3-14	22	S7-27B	52	S7-9B
23		53	SKT3-13	23		53	
24		54		24		54	
25		55	SKT3-18	25	SKT5-9	55	
26		56	SKT3-17	26	SKT5-10	56	
27		57	S6-38B	27	SKT5-11	57	
28	SKT5-1,S3-14A	58		28	SKT5-12	58	
29	SKT5-2,S3-13A	59		29	S7-55A	59	
30	SKT5-3,S3-12A	60		30		60	

S4.DIGIDATA INTERFACE.

CTD Data Store.

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31		1		31	S6-31B +5V
2		32		2		32	
3		33		3		33	S6-33B 0V
4		34		4		34	
5	S6-5A,S1-39B	35		5		35	S2-39A
6		36		6		36	S2-40A
7		37		7		37	S2-41A
8		38		8		38	S1-46A
9		39		9		39	
10		40		10		40	
11		41		11		41	
12		42		12		42	
13		43		13		43	
14		44		14		44	
15		45		15	S1-47A	45	
16		46		16		46	S1-51B,S6-43B
17		47		17	S2-52A	47	S1-52B,S6-8B
18		48		18		48	S1-53B,S6-20B
19		49		19	S6-56B	49	S1-51A,S6-53B
20		50		20	S2-47A	50	
21		51	S2-42A	21		51	
22		52	S2-43A	22	S1-41B	52	
23		53	S2-4A	23		53	
24		54		24		54	
25		55	S2-45A	25		55	
26		56	S1-40B	26	S3-50A	56	
27		57	S1-48A	27	S6-7B	57	
28		58		28	S6-44B,S1-53A	58	
29		59		29	S6-55B,S1-52A	59	
30		60		30		60	

S5.DIGIDATA INTERFACE.

Header Store.

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31	S7-31B	1		31	S7-31B 0V
2		32		2		32	
3		33		3		33	S7-33B +5V
4		34		4		34	
5	S5-5A,S1-39B	35		5		35	
6		36		6		36	S8-8B
7		37		7	S5-27B	37	S4-47B
8	S7-10A	38		8	S5-47B,S1-52B	38	S4-57A
9	S7-56A,S4-10A	39		9	S8-25B	39	S8-38B
10		40		10	S8-35B	40	S8-45B
11		41		11	S8-44B	41	S8-20B
12		42	SKT4-8	12	S8-50B	42	SD8-26B
13		43	SKT4-6	13		43	S5-46B,S1-51B
14		44	SKT4-7	14		44	S5-28B,S1-53A
15		45	SKT4-5	15		45	
16		46	SKT4-3	16		46	
17		47	SKT4-4	17		47	
18		48	S4-50B	18		48	
19		49	S4-49B	19	S8-17B	49	
20		50	S4-48B	20	S5-48B,S1-53B	50	
21		51	S8-51B	21		51	S4-51B
22		52	S8-43B	22		52	S8-24B
23		53	S8-36B	23	S8-53B	53	S5-49B,S1-51A
24		54		24	S8-19B	54	
25		55	S8-9B	25	S8-52B	55	S5-29B,S1-52A
26		56	S8-18B	26	S8-37B	56	S5-19B
27		57		27		57	
28		58		28		58	
29		59		29		59	
30		60		30		60	

S6.DIGIDATA INTERFACE.

Header/Clock Store.

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31		1		31	S8-31B 0V
2		32		2		32	
3		33		3		33	S8-33B,SKT2-2
4		34	SKT2-5	4		34	
5		35	SKT2-4	5		35	
6		36		6		36	
7		37		7		37	
8		38		8		38	
9		39		9	S4-52B	39	
10	S6-8A	40		10		40	
11		41		11		41	
12		42		12		42	
13		43		13		43	
14		44		14		44	
15		45		15		45	
16		46		16		46	
17		47		17		47	
18		48		18		48	
19		49		19		49	
20		50		20		50	
21		51		21		51	
22		52		22		52	
23		53	SKT2-6	23	S4-12A	53	
24		54		24		54	
25		55	S4-29B	25		55	
26		56	S4-10A	26		56	
27		57		27	S4-22B	57	
28		58		28		58	
29		59		29		59	
30		60		30		60	

S7.DIGIDATA INTERFACE.

Record/Header Counters.

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31		1		31	S9-33A,34A 0V
2		32		2		32	
3		33		3		33	S9-50A,51A +5V
4		34		4		34	
5		35		5		35	S6-10B
6		36		6		36	S6-53A
7		37		7		37	S6-26B
8		38		8	S6-36B	38	S6-39B
9		39		9	S6-55A	39	
10		40		10		40	
11		41		11		41	
12		42		12		42	
13		43		13		43	S6-52A
14		44		14		44	S6-11B
15		45		15		45	S6-40B
16		46		16		46	
17		47		17	S6-19B	47	
18		48		18	S5-56A	48	
19		49		19	S6-24B	49	
20		50		20	S6-41B	50	S6-12B
21		51		21		51	S6-51A
22		52		22		52	S6-25B
23		53		23		53	S6-23B
24		54		24	S6-52B	54	
25		55		25	S6-9B	55	S6-20A,30AA
26		56		26	S6-42B	56	
27		57		27		57	
28		58		28		58	
29		59		29		59	
30		60		30		60	

S8.DIGIDATA INTERFACE.

Clock.

A	DESTINATION	A	DESTINATION	B	DESTINATION	B	DESTINATION
1		31	30-31 Board1	1		31	30-31 Board2
2		32		2		32	
3		33	0 Volts,A56-57	3		33	0 Volts
4		34	0 Volts	4		34	''
5		35	''	5		35	'' ,SK4 P15
6		36	''	6		36	'' ,SK3 P21
7		37		7		37	
8		38		8		38	
9	-12 Volts	39		9		39	
10	''	40		10		40	
11		41		11		41	
12	-5 Volts	42	42-43 Board1	12		42	42-43 Board2
13	''	43		13		43	''
14		44		14		44	
15		45		15		45	
16		46	+12 Volts,S1-25B	16		46	
17		47		17		47	
18		48		18		48	250 Volts Live
19		49		19		49	''
20		50	+5 Volts	20		50	
21		51	''	21		51	
22		52	''	22		52	250 Volts Neutral
23		53	''	23		53	
24		54		24		54	
25		55		25		55	
26		56		26		56	Trans' Screen
27		57		27		57	'',A33-34
28		58		28		58	
29		59		29		59	
30		60		30	30-31 Board2	60	