FILE
IS 202

INTERNAL DOCUMENT 231

I.O.S.

I.O.S. F.S.K. DECK UNIT

OPERATING & MAINTENANCE MANUAL

T.J.P.GWILLIAM

[*This document should not be cited in a published bibliography, and is supplied for the use of the recipient only*].

NATURAL ENVIRONMENT RESEARCH COUNCIL
INSTITUTE OF OCEANOGRAPHIC SCIENCES

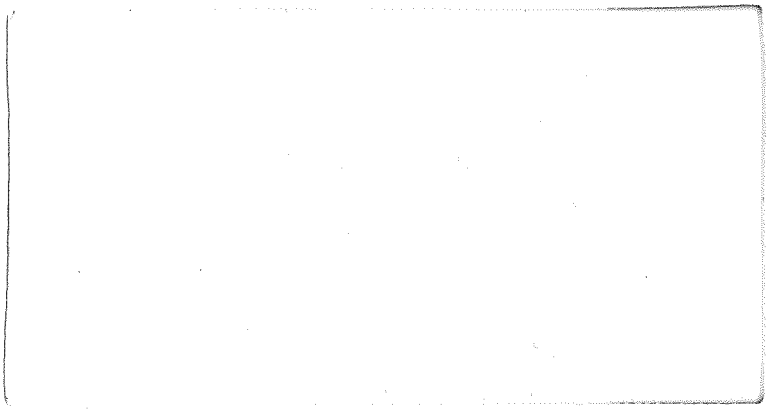
INSTITUTE OF OCEANOGRAPHIC SCIENCES

Wormley, Godalming,
Surrey GU8 5UB
(042-879-4141)

(Director: Dr. A. S. Laughton, FRS)

Bidston Observatory,
Birkenhead,
Merseyside L43 7RA
(051-653-8633)
(Assistant Director: Dr. D. E. Cartwright)

Crossway,
Taunton,
Somerset TA1 2DW
(0823-86211)
(Assistant Director: M. J. Tucker)



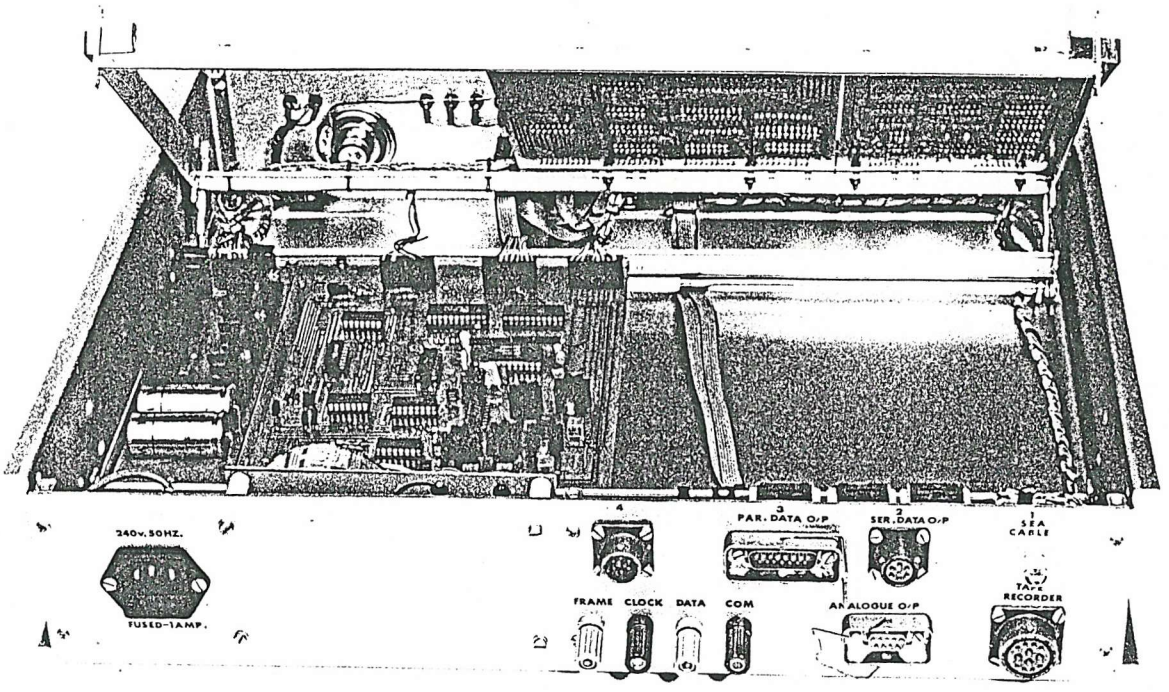
I.O.S. F.S.K.
DECK UNIT

OPERATING & MAINTENANCE MANUAL

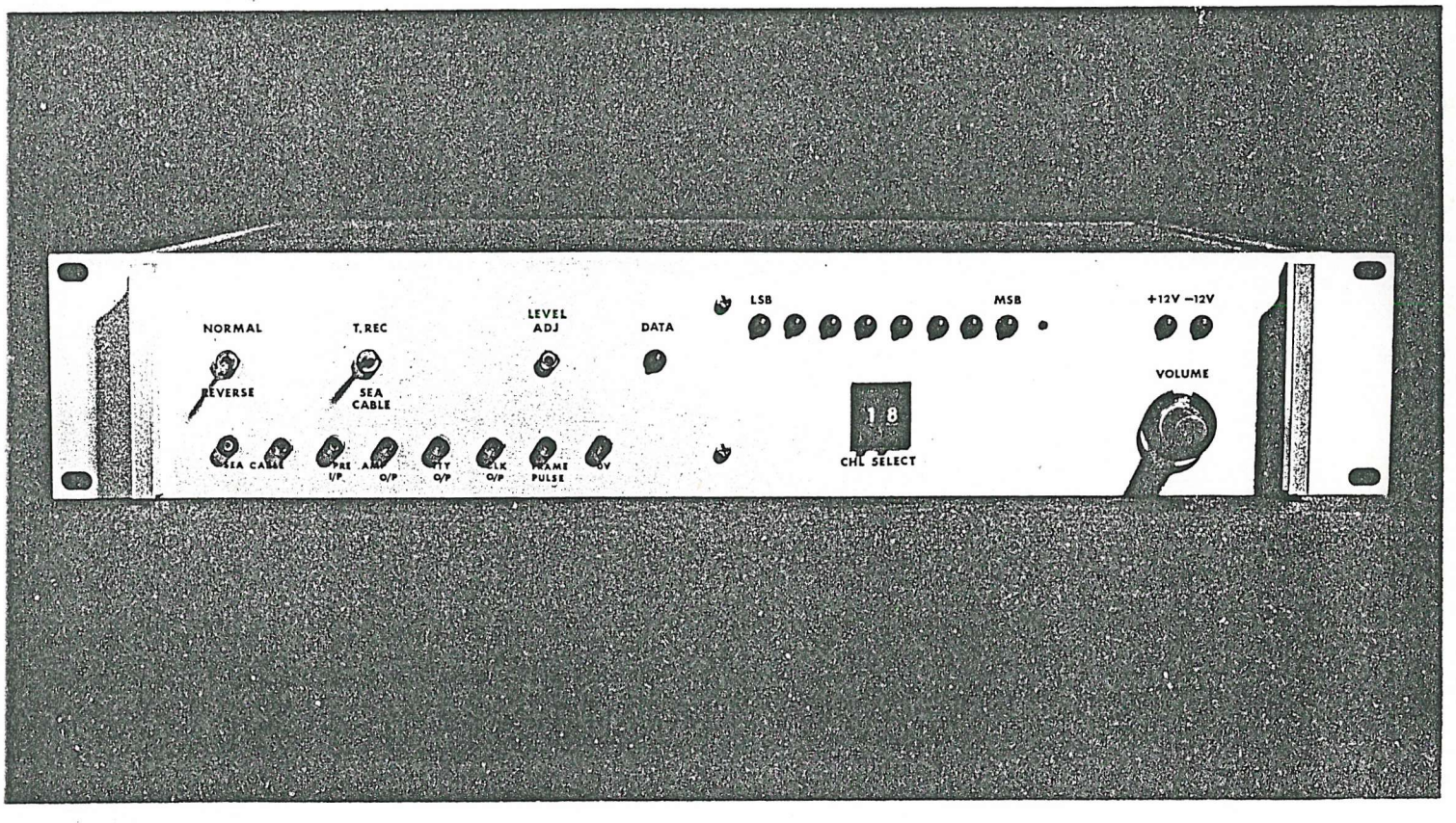
T.J.P.GWILLIAM

INTERNAL DOCUMENT NO.231
1985.

INSTITUTE OF OCEANOGRAPHIC SCIENCES
WORMLEY,GODALMING
SURREY GU8 5UB.



F.S.K. DECK UNIT – BACK PANEL



F.S.K. DECK UNIT – FRONT PANEL

CONTENTS

DRAWING LIST

INTER-CONNECTOR LIST

CIRCUIT DIAGRAMS/COMPONENT SCHEDULES

SPECIFICATION

FUNCTION:	F.S.K. DEMODULATOR
INPUT SIGNAL:	SERIAL 11 BIT WORDS(T.T.Y. FORMAT) MODULATED AS AN F.S.K.SINE WAVE SIGNAL. 2:1 FREQUENCY CHANGE LOW FREQUENCY REPRESENTS '0' LEVEL HIGH FREQUENCY REPRESENTS '1' LEVEL
SIGNAL SOURCE:	
1	UNDER WATER EQUIPMENT VIA SEA CABLE
2	TAPE RECORDER
FREQUENCY RANGE:	LOW FREQUENCY:2KHZ.- 8KHZ. HIGH FREQUENCY:4KHZ.-16KHZ. THIS RANGE CAN BE CHANGED BY MINOR COMPONENT CHANGES
INPUT MINIMIUM SIGNAL LEVEL:	80MV PK/PK.
INPUT IMPEDANCE:	APPROXIMATELY 600 OHMS
OUTPUT SIGNALS:	
1	T.T.Y. DATA (+/-10V) CLOCK (+5.7V) FRAME STROBE (+10V)
2	T.T.Y. DATA (+10V) CLOCK (+5V) FRAME STROBE (+10V)
3	8 BIT PARALLEL DATA (+5V) WORD STROBE (+5V)
4	F.S.K. DATA TO RECORDER
5	5 ANALOGUE OUTPUTS FROM 16BIT(2*8BIT) WORDS
POWER REQUIREMENTS:	240 VOLTS 50/60 HZ. 15 WATTS
DIMENSIONS:	HEIGHT WIDTH DEPTH 88 427.1 373.75 MMS. 3.5 16.75 14.75 INS. FRONT PANEL 19 INCH FITTING
WEIGHT:	10LBS.(4.54KGRM.)

SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

The I.O.S. deck unit described in this manual is an instrument designed to demodulate and process f.s.k. (frequency shift keying) modulated signals from underwater equipment. Interconnection between modulator and demodulator is by a load bearing coaxial type cable 10,000 metres long.

Primarily, the data is processed to provide T.T.Y. data, clock and strobe pulses for further data analysis by computer. Additionally, 8 bit parallel information, for interfacing with microprocessors, and 5 analogue outputs, for use with plotters, are provided.

1.2 GENERAL TECHNICAL INFORMATION

A self explanatory block schematic diagram is shown in figl. This illustrates the general function and the title of the particular printed circuit board (pcb) on which it may be found. From this latter information, the relevant detailed description and circuit diagrams can be located within the manual.

Fig 2 illustrates the signal format of the f.s.k. modulated waveforms. A relatively wide range of frequencies may be accommodated (see specification), for example, the equipment has been found to work satisfactorily with C.T.D. signals.

SECTION 2

SETTING UP OPERATION

2.1 POWER CONNECTION

Connect a 240 volts 50/60 hz. supply to the three pin fused bulkhead connector at the rear of the unit. There is no built-in power switch provided, so on power connection the +/-12 volt led (light emmitting diode) indicators, on the front panel, will indicate the presence of power.

2.2 SIGNAL OPERATION

The fsk signal source can either be the underwater unit via the sea cable or the pre-recorded data from the tape recorder. Both connections are via the rear panel, the sea cable with the B.N.C. coaxial socket (1) and the tape recorder through the Bendix multi-pin socket (5).

Signal source selection and polarity is achieved by the "TAPE RECORDER/SEA CABLE" and the "NORMAL/REVERSE" switches mounted on the front panel. On application of the signal, the data should immediately go into a "locked" mode and the "DATA" indicator,again on the front panel, should pulse at the incoming signal frame rate. If "lock on" information is not achieved then it may be necessary to adjust the preset "SIGNAL LEVEL" potentiometer. It has been found in practice that after the initial setting up, no further adjustment should be necessary. The usual cause for a non locking condition is that signal switches have been incorrectly selected.

Each 8 bit data word can be selected and displayed on the eight front panel leds in a binary format.Word one of the frame signal contains fixed data. For the C.T.D. and F.I.D.O. equipment the binary numbers 15 and 240 are used and these are transmitted on alternate frames. Because this word is identifiable it becomes a useful monitor on the phase and 'locking' capabilities of the incoming signal.
The fsk signal is also coupled through a low power audio amplifier and speaker to provide an aural indication. The "volume" control is mounted on the right hand side of the front panel.

The polarity of the T.T.Y.output data from the unit can be changed to suit the load requirements by switches on the f.s.k. demodulator DK1.

Full details for calibrating the analogue to digital convertor outputs are explained in section 3.4.

SECTION 3

CIRCUIT DESCRIPTION

3.1 F.S.K. DEMODULATOR-DK1

CIRCUIT DIAGRAM-DWPS DM9

The f.s.k. demodulator together with the clock and frame synchronising pulse generators are mounted on pcb DK1. Connections to DK1 are via the connectors CON1 and CON2.

The f.s.k. line signal from the wiper of the preset level control potentiometer, mounted on the front panel, is connected, via 2/7(connector2 pin7), to the input of the pre-amplifier. For satisfactory working, the signal level must be greater than 80mV peak to peak.From experience, the normal levels, working from R.R.S. Discovery with 10,000 metres of cable, have been in excess of 0.5 volts.

The first stage of the demodulator is the signal conditioning section consisting of ic1 and ic2. Ic1 is configured as an a.c. amplifier with back to back diodes in the feedback path to provide a relatively higher gain for low level inputs than for large signals. Ic1 and ic2 are D.C. biassed at half the supply voltage using the resistor network R5 and R6. The output from ic1 is coupled to the inverting input of the comparator ic2 which produces a twelve volt square wave at the output. The output from the comparator is inverted and interfaced to the COSMOS digital circuitry by a 4011 NAND gate, connected as an inverter, and the

output of which is connected to the f.s.k. demodulator proper and the clock generator.

The f.s.k. demodulator circuit consists of ics 3, 4, 5, 6. It is a completely digital system requiring clock pulses at thirytwo times the signal bit frequency for operation. For ease of explanation and understanding, the reader is advised to study the waveform diagram, fig.3, in relation to the circuit. With the reset input of ic4 taken to 0volts the positive edge of clock pulses will switch the counter. On the fourth clock pulse the divide-by 8(Q3) output goes positive and stays at this level for a further 4 pulses when it is switched to 0 volts. If the input signal is a ´1´ then the reset input (signal input) will go positive and reset the counter. If the input signal is a ´0´ the reset stays low and the Q4 output will go positive (when Q3 went low) and remain high for a further 8 clock pulses before the input signal will reset the device. There will only be a reset pulse, from the Q4 output of ic4, when the fsk input signal is a ´0´ thus allowing the counter to count to a total of 16 clock pulses before resetting.Alternatively, with a ´1´ level input, only 8 clock pulses are counted over the period when the input is low.

The Q3, Q4 pulses are NANDed to produce a negative pulse that is connected to the ´D´ input of the ´D´ type latch. This is also connected to the ´EN´ input of the CD4520 (ic4). The clock input signal will then have no effect until the signal input at the reset goes positive. The counter is then reset. When the clock input to the device goes positive the output falls, ic4 is reset and the ´D´ input goes high on the next positive input of

the fsk signal. The Q output of ic6a will then go high. The Q output is then ANDed with the output of the previous NAND gate to increase leading edge pulse width. This will ensure that the final stage will switch on the leading edge of the next clock pulse.

The inverted output from the 'D' type flip flop is the TTY demodulated signal. This is effectively delayed on the input by the periodic time of the lowest frequency of the fsk signal(0 level). Positive or negative output formats can be selected by using the onboard switches, while line drivers provide output levels for the shipboard computer interface(+/-10v)or the F.I.D.O. digital display unit (+10v).

The clock pulses required by the demodulator are derived in the clock generator circuit. This section consists of an RCA phase lock loop(pll), integrated circuit, IC7, and binary divider, IC8. Using the edge controlled phase comparator with the voltage controlled oscillator(vco), the components are selected to lock into the highest modulating frequencies of the input signal(7.292Khz.). In the "lock on" condition the vco output frequency is 116.6 Khz(32 times the signal bit rate). With no signal, the vco will adjust to a frequency of approximately 96 Khz. The frequency lock range of the pll is 96-240 Khz which is equivalent to input signal bit rates of 3 to 7.5 Kbaud. By having this 2:1 "lock in" range it is possible to replay tapes through the system at twice the recorded speed,thus halving the time for replays. For higher baud rate signals it is only neccesary to change components of the pll to provide the correct clock rate to the demodulator.

The binary clock divider, IC8, provides output pulse strings that vary in speed from the signal bit rate to 32 times the bit rate. The times 16 clock pulses are fed to line drivers(IC11) before going to the ship's computer interface. The times 8 clock pulses are also routed through the line drivers (IC11) but are used in the F.I.D.O. display unit for binary to b.c.d. conversion. In order to supply the correct amplitude and polarity to the load,diodes are connected to the output lines to limit the output amplitude excursions.

Apart from the TTY data and clock pulses, the demodulator board also contains the frame synchronising pulse generator. The important characteristic of this pulse is that the positive going edge is synchronised to the negative going edge of the first start pulse of the first word of the TTY data frame. The pulse is derived from the circuit containing IC9,10 and the AND gate consisting of R16 and D5 to D16 inclusive.The frame signal consists of a fixed number of 11 bit words after which continuous '1' level is transmitted until the first word of the next frame.During the transmission of the 11 bit words, one of the inputs to the 12 input AND gate must contain a'0' (the "start" bit) and therefore the AND gate output will be '0'. However, after the last word in the data string has been clocked through the registers, IC9 and IC10, only '1s' will remain in the frame and the gate will respond with a high output level after the twelfth '1' has clocked through.The first pulse of the first word in the frame is the "start pulse" which is at '0' level, diode D5 will respond and the gate output will go to a '0' level. Part of the NAND gate, IC5,is wired as an inverter amplifier

which produces a frame pulse at TP3. Again, as with the clock pulse, this pulse is used with the ship's computer system as well as the F.I.D.O. display unit and line drivers are used to provide the correct amplitude and polarity.

3.2 8 BIT DATA CHL. SELECT UNIT-DK2/1

CIRCUIT DIAGRAM- DWPS DM10

This circuit is used to process the data for display as binary information on the front panel leds, as input data to the digital to analogue converters (DK3/1), and to produce 8 bit parallel data for external microprocessors.

The serial TTY data together with the *16 clock and frame synchronising strobe from the demodulator DK1 are fed into the universal asynchronous receiver transmitter(UART), ic1. For this application, only the receiving section is used. The serial eleven bit word,as shown in fig 3, consists of a start bit, eight data bits and two stop bits. The UART removes the start and stop bits and presents the eight data bits in parallel format on the outputs RBR1 to RBR8, the least significant bit (lsb) at RBR1 and the most significant bit (msb) at RBR8. As well as producing this eight bit information the UART also produces a positive going pulse at DR each time a conversion has been completed. The positive going edge is used to produce a data received reset, DRR, pulse using ic7 as the delay circuit. The DRR pulse clears the DR to a low level allowing the next character to be received. The pulse produced at the DR terminal of the UART is also utilised as a word strobe throughout the remainder of the circuit as well as a data ready signal to the external microprocessor.

The eight bit parallel information produced by the UART is connected to two hex latches on the binary digital to analogue converter pcb, DK3/1. The hex latch, ic2, together with the

inverter amplifiers of ic5 and ic6 supply the data to the microprocessor. The connections used for this data and the "data ready pulse" previously mentioned are via connector 4 on the pcb and plug 3 on the back panel of the unit. The parallel data from the second latch driver, ic3, are connected via series resistors to the front panel leds which will display the binary 8 bit word. The word displayed is selected by the strobe selector switches mounted below the leds on the front panel. The "unit" and "decade" strobes for these switches are derived from the "word strobe" pulse, DR, which is used to clock the dividers ic8 and ic9. The first divider produces 10 decoded decimal output pulses which are the ´0´ to ´9´ unit strobes,and the second divider produces 4 decade strobes, ´0´, ´10´, ´20´, and´30´. The two outputs from the word selector switches are combined in the NAND gate and pulse shaper circuit, ic4, to produce the latching pulse for the l.e.d. driver, ic3. Thus as long as the data frame has less than 39 words then any word can be displayed on the l.e.d. display.

3.3 BINARY D.A.C.+5 OUTPUTS-DK3/1

CIRCUIT DIAGRAM-DWPS DM11

It is often required to display the data on chart recorders, and to this end this unit provides a basic 12 bit digital to analogue conversion on five 16 bit (2+8bit words) channels. The "word pulse",derived from DK2 (8 bit data channel select p.c.b.) is divided down, by ic4 and ic5, to produce unit and decade pulses in a similar manner to,that of ic8 and ic9 of unit DK2/1. The waveforms of the D.A.C.are shown in fig4. Using AND gates with the selected strobes a latching pulse will be produced to latch the least significant 8 bits of data into the data latch ic1. The next strobe will then latch the most significant 8 bits of data in data latch ic2.

The digital to analogue (D.A.C.) integrated chip is the DAC120HCD, ic3, which is a 12 bit device with a conversion time of 200 nanoseconds(10-9 secs). The output voltage span is 10.24 volts corresponding to 1mv/bit of input data. From experience it is found not necessary to use bit 1 (l.s.b.) of the data for display on chart recorders so bit 2 to 13 inclusive of the 16 bit word is connected to the D.A.C. The output from the convertor is connected to the inputs of five "sample and hold" ics of which only the one with the correcly timed strobe will sample and hold the analogue data. The strobes are derived from the same source as that for the data latch strobes mentioned previously and with the F.I.D.O. system, the analogue data is updated every 0.5 second(frame rate).

3.4 DIGITAL TO ANALOGUE CONVERTER (IC3)

SETTING UP INSTRUCTIONS

If it is suspected that the relationship between the output voltage and the digital input data is incorrect then the following method can be used to calibrate the unit.

Switch off the deck unit, remove connector 10 and replace with a connector with 'free' leads to all the data input pins. Switch on the equipment and apply an f.s.k. signal. The output from the DAC and all the analogue outputs should be zero volts. Adjust the "offset" control, P1, mounted on the p.c.b. if zero volts is not achieved.

Connect the free ends of the data input leads to the +5volt supply rail, this simulates 16 bits of data and therefore the output of the DAC and all the five analogue outputs should be 10.24 volts. Adjust the "full scale"control, P2, which is also mounted on the pcb, to bring the output to 10.24 volts if necessary. Recheck the zero output condition. With the DAC correctly set up the output changes 1mv for 1 bit change of input data.

3.5 D.C. SUPPLY SYSTEM-DK5

CIRCUIT DIAGRAM-DWPS DM16

The d.c. supplies necessary to operate the complete deck unit are +/-15volts.+/-12volts and +5 volts. These are derived from a conventional mains supply step down transformer and full wave rectifier circuit, with capacitor filtering. The components are mounted on a p.c.b. at the rear of the unit near the mains input supply socket. This socket contains the 2 amp fuse plus a spare. The 50 hz. supply goes directly to the p.c.b., and the cable kept apart from the other deck unit cables to minimise "pickup". The +/-20 volt unregulated output is connected to the d.c.regulator p.c.b., DK5, via connector 8. This board contains the three pin 78/79 series fixed voltage regulators that provide the required d.c. outputs.

3.6 DATA TRANSFORMER UNIT-DK6

CIRCUIT DIAGRAM-DWPS DM17

The line transformers provide the matching between the sea cable, the tape recorder and the deck unit.

In the normal mode of operation the tape recorder is recording the raw f.s.k. signal in real time. This recording then becomes the back up in the event of failure of the deck unit or the computer system. The tape recorder input transformer, T2, is connected directly across the incoming sea cable at the primary of T1. This latter transformer couples the incoming signal to the f.s.k. demodulator section via the relevant switches and the threshold preset potentiometer on the front panel. T3 handles the replayed signal from the tape recorder and can be routed through to the demodulator by the switches on the front panel. Sometimes it may be necessary to change the polarity of the signal from the transformers and the "normal/reverse" switch on the front panel makes provision for this.

Also mounted on p.c.b. DK6 is an audio amplifier which amplifies the f.s.k. pre-amplifier output to drive a small loudspeaker on the front panel. The audio output provides aural confirmation of signal reception and experience has shown it to be very useful in the detection of abnormal signal patterns.

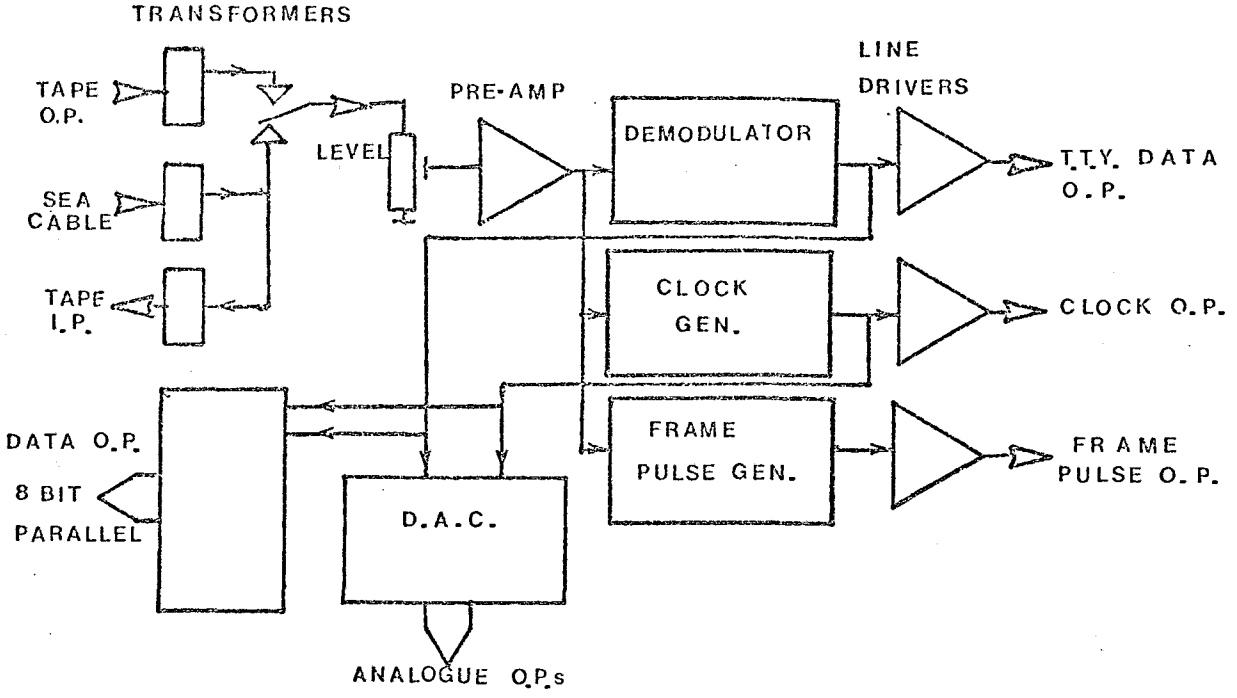


Fig. 1 BLOCK SCHEMATIC - DECK UNIT.

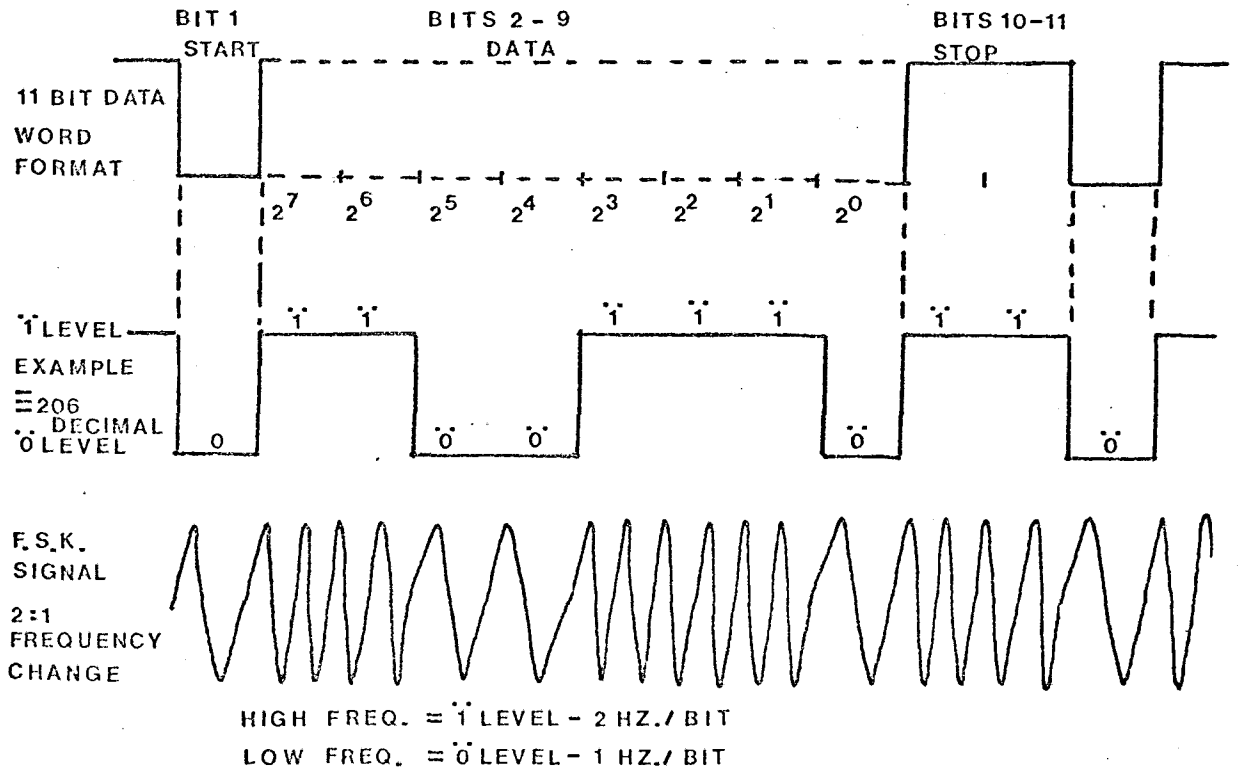


Fig. 2 WORD FORMAT DETAILS.

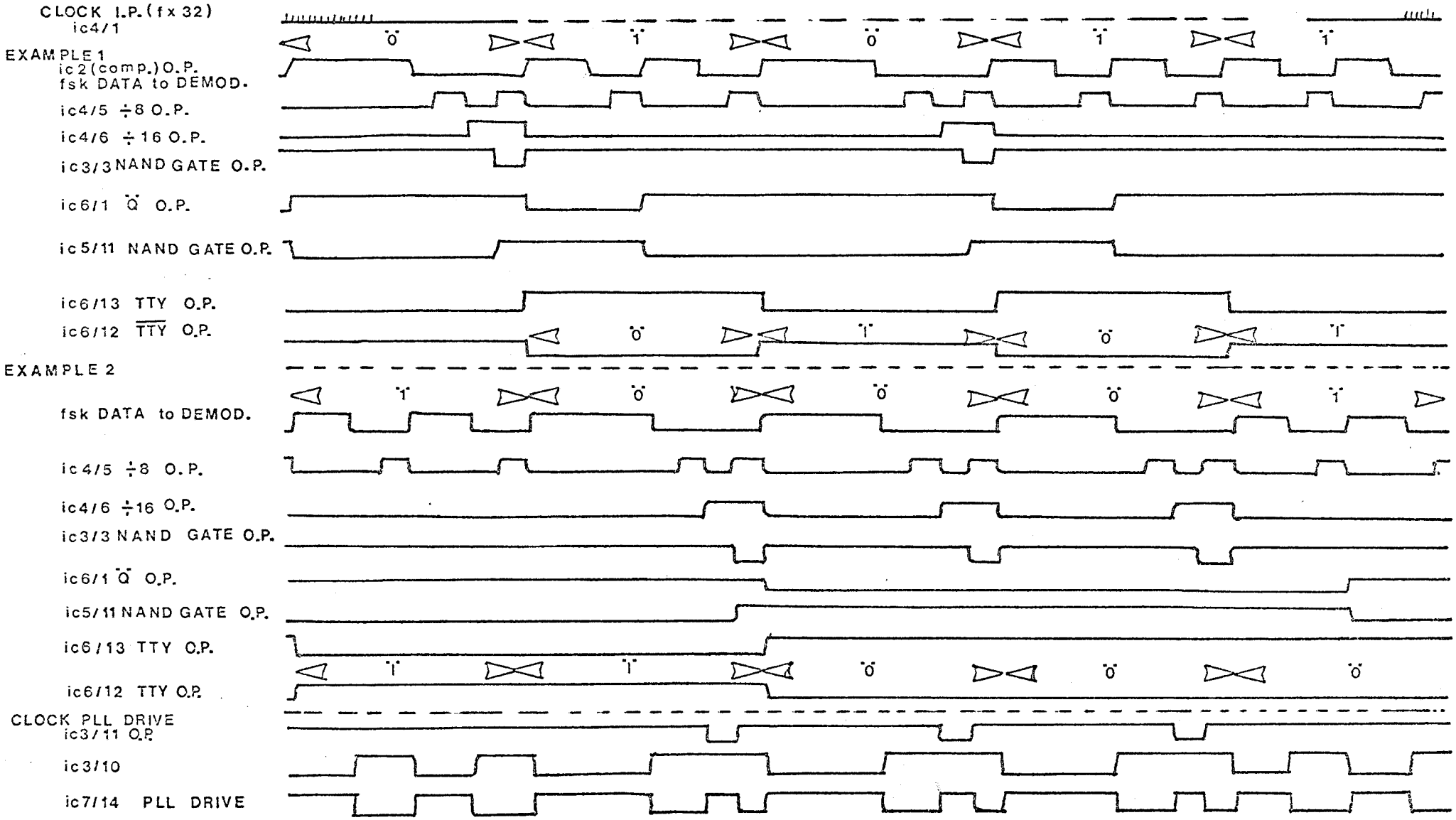


Fig. 3 DEMODULATOR WAVEFORMS

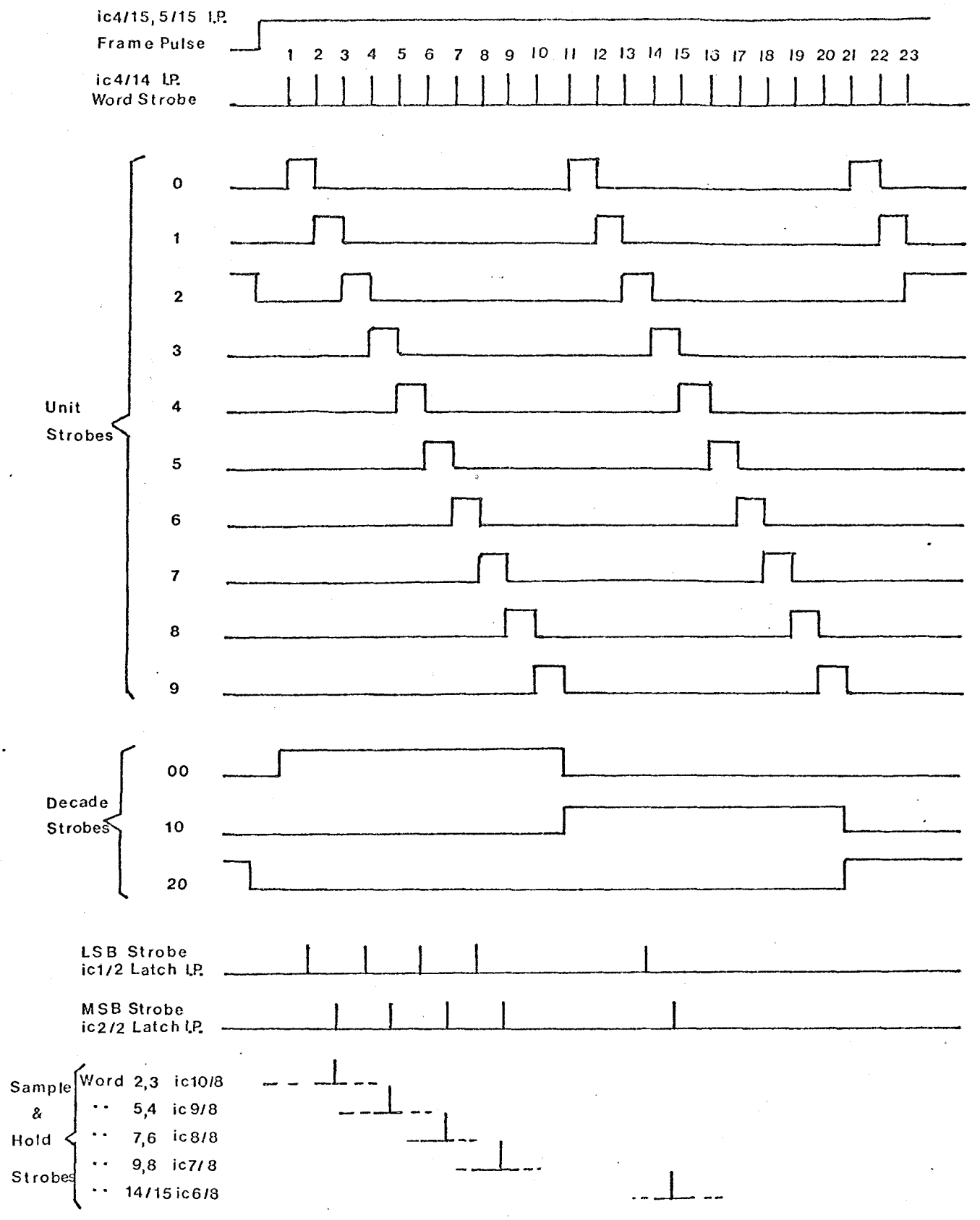


Fig. 4 BINARY D.A.C. WAVEFORMS

F.S.K. DEMODULATOR DK1/1-CONNECTOR1

PIN NO.	DETAILS	CONNECT TO
1	(0V.) COMMON	3/2,13/10
2	FRAME SYNC. (+10V)	SK2/C,TP6 LED F.P.
3	FRAME SYNC.	RED TERM. B.P.
4	CLOCK *16 (+5V)	SK2/B,TP5 5/4
5	DATA 2 O/P (+10V)	BLUE B.P 5/5
6	FRAME SYNC. (+5V)	5/7
7	CLOCK *4	
8	CLOCK *8	YELL.B.P.
9	DATA 1 O/P(+/-10V)	SK2/A
10	+5V SUPPLY I/P	8/2

F.S.K. DEMODULATOR DK1/1-CONNECTOR 2

PIN NO.	DETAILS	CONNECT TO
1	DATA 3 O/P (+12V)	TP4,5/5
2		
3	_12V SUPPLY I/P	8/10
4	SIGNAL I/P COMMON	TP8,GRN.BP
5		
6		
7	F.S.K. SIGNAL I/P	LEVEL CONT. F.P.
8		
9	+12V SUPPLY I/P	8/3
10	PRE-AMP O/P	TP3,13/8

8 BIT DATA CHANNEL SELECT DK2/1-CONNECTOR 3

PIN TO	DETAILS	CONNECT TO
1	+5 VOLT I/P +1.e.d.SUP	8/2,F/P.
2	0 VOLT(COM)	1/1,11/2
3	2*0 O/P	led F/P
4	2*1 O/P	"
5	2*2 O/P	"
6	2*3 o/p	"
7	2*4 O/P	"
8	2*5 O/P	"
9	2*6 O/P	"
10	2*7 O/P	"

8 BIT DATA CHANNEL SELECT DK2/1-CONNECTOR 4

PIN TO	DETAILS	CONNECT TO
1	CB1 PULSE TO COMP.	11/10
		SK3/10
2	2*0 BIN. DATA O/P	SK3/1
3	2*1 " " "	SK3/2
4	2*2 " " "	SK3/3
5	2*5 " " "	SK3/6
6	2*4 " " "	SK3/5
7	2*3 " " "	SK3/4
8	2*6 " " "	SK3/7
9	2*7 " " "	SK3/8
10	0V(COM) TO COMP.	SK3/11

8 BIT DATA CHANNEL SELECT DK2/1-CONNECTOR 5

PIN TO	DETAILS	CONNECT TO
1	WORDSTROBE "0" O/P	F/P SWT.
2	" "10" O/P	" "
3	" "20" O/P	" "
4	CLOCK I/P*16(+5V)	1/4
5	TTY DATA I/P(+12V)	1/5
6	WORDSTROBE "30" O/P	F/P SWT.
7	FRAME SYNC I/P (+12V)	1/6,11/8
8	FRAME SYNC O/P (+5V)	n.c.
9	STROBE SWT."10s" O/P	F/P
10	" " "UNITS" O/P	F/P

8 BIT DATA CHANNEL SELECT DK2/1-CONNECTOR 6

PIN TO	DETAILS	CONNECT TO
1	2*0 BIN. O/P TO D.A.C.	10/8
2	2*1 " " " "	10/7
3	2*2 " " " "	10/6
4	2*3 " " " "	10/5
5	2*4 " " " "	10/1
6	2*5 " " " "	10/2
7	2*6 " " " "	10/3
8	2*7 " " " "	10/4
9		
10		

8 BIT DATA CHANNEL SELECT DK2/1-CONNECTOR 7

PIN TO	DETAILS	CONNECT TO
1	WORDSTROBE "2" O/P	F/P
2	" "7" "	F/P
3	" "3" "	F/P
4	" "8" "	F/P
5	" "4" "	F/P
6	" "9" "	F/P
7	" "5" "	F/P
8	" "1" "	F/P
9	" "0" "	F/P
10	" "6" "	F/P

D.C. POWER SUPPLIES. DK5-CONNECTOR 8

PIN TO	DETAILS	CONNECT TO
1	+ve.UNREG. I/P	+ve. RECT.O/P
2	+ve.5Volts O/P	3/1,1/10,9/7
3	+ve.12Volts O/P	2/9,+12V.led.
4	+ve.15Volts O/P	9/3
5	0Volts UNREG.	RECT.UNIT
6	0Volts(com) O/P	11/4,12V.led
7	-ve.15Volts O/P	9/5
8	-ve.5Volts O/P	n.c.
9	-ve.UNREG. I/P	-ve.RECT.O/P
10	-ve.12Volts O/P	2/3,-12V.led.

BINARY D.A.C.+5 O/Ps DK3/1-CONNECTOR 9

PIN TO	DETAILS	CONNECT TO
1	n.c.	
2	PRESSURE ANAL. O/P	SK6/1,TP7
3	+15Volt. I/P	8/4
4	PART.CHLS. ANAL. O/P	SK6/2
5	-15Volt. I/P	8/7
6	PART.CHL1 ANAL. O/P	SK6/3
7	+5Volts.I/P	8/2
8	TRANMISS. ANAL. O/P	SK6/4
9	0V(COM) ANAL. O/Ps.	SK6/9
10	TEMP. ANAL. O/P	SK6/5

BINARY D.A.C.+5 O/Ps DK3/1-CONNECTOR 10

PIN TO	DETAILS	CONNECT TO
1	2*4 BIN DATA I/P	6/5
2	2*5 " " "	6/6
3	2*6 " " "	6/7
4	2*7 " " "	6/8
5	2*3 " " "	6/4
6	2*2 " " "	6/3
7	2*1 " " "	6/2
8	2*0 " " "	6/1
9	n.c.	
10	n.c.	

BINARY D.A.C.+5 O/Ps DK3/1-CONNECTOR 11

PIN TO	DETAILS	CONNECT TO
1	n.c.	
2	0 Volts(COM.)	11/4,3/2
3	n.c.	
4	0 Volts(COM.)	11/2,8/6
5	n.c.	
6	n.c.	
7	n.c.	
8	FRAME SYNC I/P	5/7
9	n.c.	
10	WORDPULSE I/P	4/1

DATA TRANSFORMER UNIT DK6-CONNECTOR 12

PIN TO	DETAILS	CONNECT TO
1	SEA CABLE SIGNAL	SK1 core
2	SEA CABLE SCREEN	SK1
3	TAPE RECORDER SIG.O/P	SK5/C
4	TAPE RECORDER SIG.O/P	SK5/D
5	T1 O/P TO F/P SWT.	SWT1a
6	T1 O/P TO F/P SWT.	SWT1b
7	T3 O/P TO F/P SWT.	SWT1a
8	T3 O/P TO F/P SWT.	SWT1b
9	T2 O/P TO TAPE REC.	SK5/A
10	T2 O/P TO TAPE REC.	SK5/B

DATA TRANSFORMER UNIT DK6-CONNECTOR 13

PIN TO	DETAILS	CONNECT TO
1	n.c.	
2	n.c.	
3	AMP. O/P TO VOL. CONT	F/P
4	n.c.	
5	n.c.	
6	n.c.	
7	n.c.	
8	AUDIO I/P	2/10
9	n.c.	
10	0Volts(COM)	1/1

BACK PANEL
OUTPUT DATA TO F.I.D.O. DECK UNIT
TERMINALS

COLOUR	DETAILS AMPLITUDE	INTERNAL CONNECTION
GREEN	COMMON 0V	2/4 SKT.2/F
BLUE	T.T.Y. DATA +10V.	1/5
YELLOW	CLOCK*8 +5V.	1/8
RED	FRAME SYNC. +10V.	1/3

BACK PANEL
SEA CABLE INPUT
SOCKET1

PIN No.	DETAILS	CONNECT TO
INNER	F.S.K.DATA	CON12/1
OUTER	SEA EARTH	CON12/2

BACK PANEL
SERIAL DATA OUTPUT
SOCKET 2

PIN NO.	DETAILS AMPLITUDE	INTERNAL CONNECTION
A	T.T.Y. DATA +/- 10V.	1/9
B	*16 CLOCK +5.7V.	1/4
C	FRAME SYNC. +10V.	1/2
D	NOT USED	
E	" "	
F	COMMON 0V.	2/4

BACK PANEL
PARALLEL DATA OUTPUT
PLUG 3

PIN NO.	DETAILS	LEVEL	INTERNAL CONNECTION
1	BIT0	+5V.	4/2
2	BIT1	+5V.	4/3
3	BIT2	+5V	4/4
4	BIT3	+5V.	4/7
5	BIT4	+5V.	4/6
6	BIT5	+5V.	4/5
7	BIT6	+5V.	4/8
8	BIT7	+5V.	4/9
9	NOT USED		
10	CB1	+5V.	4/1
11	COMMON	0V.	4/10
12/15	NOT USED		

BACK PANEL
TAPE RECORDER INPUT/OUTPUT SIGNAL
SOCKET 5

PIN NO.	DETAILS	INTERNAL CONNECTION
A	SEA CABLE SIG-	12/9
B	NAL INPUT.	12/10
C	REPLAYED	12/3
D	TAPE SIGNAL	12/4
E/L	NOT USED	
M	COMMON(0V.)	SKT.2/F

FRONT PANEL (F/P)

TEST POINTS

T.P. No.	DETAILS	CONNECT TO
1	I/P SIGNAL	LEVEL CONT.F/P
2	PRE-AMP I/P SIG.	LEVEL CONT.O/P
3	PRE-AMP O/P SIG.	2/10
4	TTY DATA O/P	2/1
5	CLOCK*16 O/P	1/4
6	FRAME PULSE	1/2
7	CHL.1 D.A.C. O/P	9/2
8	0Volts(COM)	2/4

DWP'S DM9.

PRINT TRIMMING LINE

INSTITUTE OF OCEANOGRAPHIC SCIENCES

PRE-AMP

F.S.K. - DEMODULATOR

P.L.L. CLOCK GEN.

FRAME SYNC PULSE GEN

Note:- IC1 - UA741 8 PIN DIL.
IC2 - AM311 8 PIN DIL
IC3, IC5 CD4011BE - 14 PIN DIL
IC4, IC8 CD4520BE 16 PIN DIL
IC6 CD4013BE 14 PIN DIL
IC7 CD4046BE 16 PIN DIL
IC9, IC10 CD4015BE 16 PIN DIL
IC11, 12 SN75188 14 PIN DIL
D1 - D5 IN4148

TITLE						CIRCUIT No.
INSTITUTE OF OCEANOGRAPHIC SCIENCES	D.W.P.S. [F.I.D.O.] F.S.K. DEMODULATOR DK1		1	Nov 1982		DWPS DM9
			2	Apr 1983		
			3	11/6/1984		
			4	7/4/1984		SHEET No.
		AMENDMENT	ISSUE	DATE	AMENDMENT	ISSUE DATE

I.O.S. FORM No. 107 (1/75)

PAPER SIZE A3

LANK SIZE-360mm x 610mm

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
R1	RESISTOR.	22Kᴀ	0·4W	METAL FILM MR25	R.S. COMPONENTS	148-815	
R2	-"-	390Kᴀ	"	-"-	-"-	149-127	
R3	-"-	100Kᴀ	"	-"-	-"-	148-972	
R4	-"-	4·7Kᴀ	"	-"-	-"-	148-663	
R5	-"-	2·7Kᴀ	"	-"-	-"-	148-607	
R6	-"-	2·7Kᴀ	"	-"-	-"-	148-607	
R7	-"-	100Kᴀ	"	-"-	-"-	148-972	
R8	-"-	10Kᴀ	"	-"-	-"-	148-736	
R9	-"-	100ᴀ	"	-"-	-"-	148-269	
R10							USED ON ISSUE 2 ONLY
R11							-"-
R12	-"-	100Kᴀ	"	-"-	-"-	148-972	
R13	-"-	100Kᴀ	"	-"-	-"-	148-972	
R14	-"-	2·7Kᴀ	"	-"-	-"-	148-607	
R15							USED ON ISSUE 1 ONLY.
R16	-"-	33Kᴀ	"	-"-	-"-	148-859	
C1	CAPACITOR	100 PF	100V.	CERAMIC WSR/81252.			
C2	-"-	0·068 μF		METALLISED POLYESTER.	FARNELL	WIMA MKS2.	RM 5MM
C3	-"-	100 μF	16V	ELECTROLYTIC DUBLIER CEB - FARNELL CEB SERIES		100-814	
C4	-"-	100 μF	16V	-"-	-"-	-"-	
C5	-"-	100 μF	16V	-"-	-"-	-"-	
C6	-"-	100 μF	16V	-"-	-"-	-"-	
C7	-"-	0·47 μF		METALLISED POLYESTER.	FARNELL	WIMA MKS2.	RM 5MM.

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

D.W.P.S. [FIDO] F.S.K. DEMODULATOR

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S. DWPS D119/2

COMPILED BY T.J.P.S DATE 10/11/83 SHEET No. 1 OF 2

ISSUED FOR ORDER No. FOR UNITS

I.O.S. FORM No. 105 (1/76)
PRINT TRIMMING LINE
297 x 363mm
WORKING DRAWING 0705 82

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
IC1	INTEGRATED CIRCUIT	μA 741 CP		OP. AMP 8 PIN D.I.L	R.S COMPONENTS.	305-31	
IC2	— " —	LM 311 N		COMP. 8 PIN D.I.L.	— " —	308-843	
IC3	— " —	CD 4011 BE		CMOS GATE 14 PIN DIL.	— " —	306-544	
IC4	— " —	CD 4520 BE		CMOS DIV. 16 PIN DIL	— " —	309-802	
IC5	— " —	CD 4011 BE		CMOS GATE 14 PIN DIL	— " —	306-544	
IC6	— " —	CD 4013 BE		DUAL CMOS D TYPE FF 14 PIN DIL	— " —	306-550	
IC7	— " —	CD 4096 BE		R.P.L. CMOS 16 PIN DIL	— " —	306-645	
IC8	— " —	CD 4520 BE		CMOS DIV 16 PIN DIL	— " —	309-802	
IC9	— " —	CD 4015 BE		DUAL 4 BIT SHIFT REG CMOS 16 PIN DIL	— " —	306-572	
IC10	— " —	CD 4015 BE		— " —	— " —	306-572	
IC11	— " —	SN 75188 N		LINE DRIVER 14 PIN DIL	— " —	309-587	
IC12	— " —	— " —		— " —	— " —	— " —	
D1-D25	DIODE	IN 4148		SILICON SWITCHING	— " —	271-606	
S1	SWITCH			S.P.D.T VERTICAL	— " —	334-224	
S2	"			— " —	— " —	— " —	
CON 1	PCB CONNECTOR	10 PIN PCB MOUNTING - MOLEX			TYCO KK - FARNELL	143-523	MOLEX REF 22-27-2101
CON 2	— " —			"		143-523	AMP (CONNECTOR 22-01-2105
IC	HOLDER. (IC1, IC2)			8 PIN DILE Low Profile	VERO	19-2176B	
—	" — (IC3, IC5, IC6, IC11, IC12)			14 PIN DIL Extra Low Profile	VERO	19-2177H	
—	" — (IC4, IC7, IC8, IC9, IC10)			16 PIN DIL Extra Low Profile	VERO	19-2178C	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

D.W.P.S [FIDO] F.S.K. DEMODULATOR

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S. DWPS DM9/1

COMPILED BY T.J.C. DATE 15/11/83 SHEET No. 2 OF 2

ISSUED FOR ORDER No. FOR UNITS

I.O.S. FORM No. 105/1/75

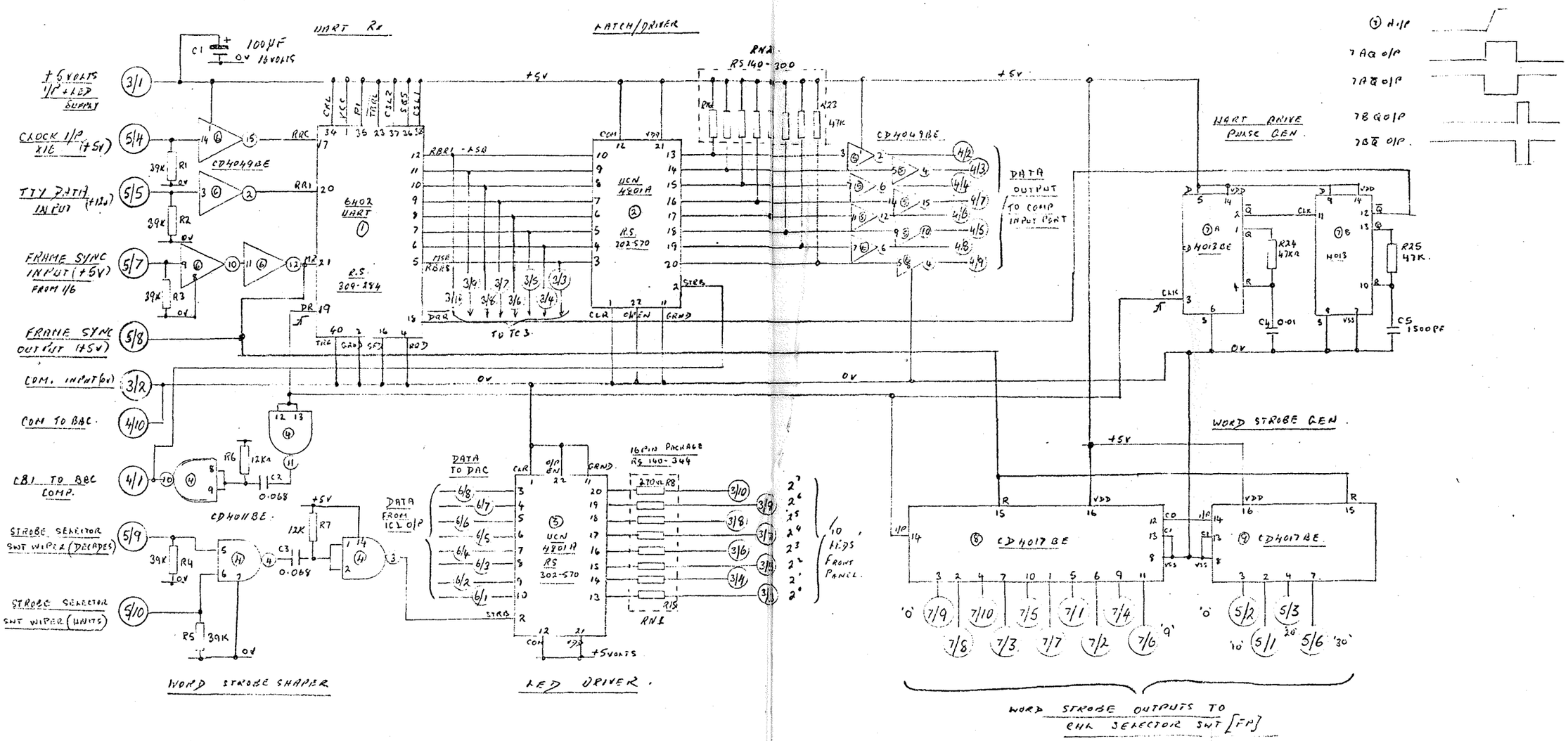
PRINT TRACING LINE

297 x 363 mm

WORKING SHEETLINE 0705.82

PRINT TRIMMING LINE

INSTITUTE OF OCEANOGRAPHIC SCIENCES



		1	Nov 1976				CIRCUIT No. DWPS DI410 10
Connector Pin Numbering	NIL	2	March 1976				
							SHEET No.
AMENDMENT	ISSUE	DATE	AMENDMENT	ISSUE	DATE		

TITLE D.W.P.S

8 BIT DATA CHL. SELECT

DK2/1

DECK UNIT

INSTITUTE OF OCEANOGRAPHIC SCIENCES

T.J.P.G.

Woking Dyeline 0423/82

I.O.S. FORM No. 107 (1/75)

PRINT TRIMMING LINE

BLANK SIZE - 360mm x 594mm

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
R1	RESISTOR	39KΩ	0·4W	METAL FILM MR25	R.S. COMPONENTS	148-871	
R2	- " -	- " -	- " -	- " -	- " -	- " -	
R3	- " -	- " -	- " -	- " -	- " -	- " -	
R4	- " -	- " -	- " -	- " -	- " -	- " -	
R5	- " -	- " -	- " -	- " -	- " -	- " -	
R6	- " -	12KΩ	- " -	- " -	- " -	148-758	
R7	- " -	- " -	- " -	- " -	- " -	- " -	
R8-R15	RESISTANCE MODULE	270Ω		DISCRETE CARBON FILM RESISTOR [8 RESISTOR]	- " -	140-344	16 PIN DIL.
R16-R23	- " -	47KΩ		8 COMMON RES. SIL.	- " -	140-300	
R24	RESISTOR	47KΩ	0·4W	METAL FILM MR25	- " -	148-893	
R25	- " -	47KΩ	- " -	- " -	- " -	- " -	
C1	CAPACITOR.	100μF	16VOLT	ELECTROLYTIC. DUBILIER	CEA FARNELL. CEB SERIES.	100-814	
C2	- " -	0·068μF	63V	POLYESTER WIMA MKS2	FARNELL.		
C3	- " -	0·068μF	"	- " -	- " -		
C4	- " -	0·01μF	"	POLYESTER WIMA	- " -		
C5	- " -	1500PF	"	"	"		
IC1	INTEGRATED CIRCUIT	6402		UART	R.S. COMPONENTS.	309-284	
IC2	- " -	UCN4801A		LATCH-DRIVER	- " -	302-570	SPRAGUE MANUFACTURE
IC3	- " -	"		- " -	- " -	302-570	- " -
IC4	- " -	CD4011BE		QUAD NAND GATE-CMOS	- " -	306-544	
IC5	- " -	CD4049BE		HEX INV. - CMOS	- " -	306-667	
IC6	- " -	"		- " -	- " -	306-667	
IC7	- " -	CD4013BE		DUAL D F/F CMOS	"	306-550	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

D.W.P.S 8 BIT DATA CHL SELECT DK2/1

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S. DWG'S DM10/1

COMPILED BY T.J.C. DATE NOV 11/83 SHEET No. 1 OF 2

ISSUED FOR ORDER No. FOR UNITS

I.O.S. FORM No. 105 (1/76)

PRINT TRIMMING LINE

297 x 363mm

WORKING DRAWING SIZE A2

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
IC8	INTEGRATED CIRCUIT	CD4017BE		DECADE DECODER	R.S. COMPONENTS		
IC9	— " —	"		— " —	— " —		
CON 3	CONNECTOR	10WAY		MOLEX PCB MOUNTING			MATING
CON 4	"	"		TYPE KK	FARNELL	143-523	FREE SOCKET
CON 5	"	"		MOLEX REF	22-27-2101		REF 22-01-2105
CON 6	"	"					
CON 7	"	"					
I.C. HOLDER [IC1]				40PIN D.I.L.	EXPRESS KONTAKT VERO	19-2184F	
I.C HOLDER [IC2, IC3]				22 PIN DIL	— " — VERO	19-2181K	
I.C HOLDER [IC4, IC7]				14 PIN DIL	— " — VERO	19-2177H	
I.C. HOLDER [IC5, IC6, IC8, IC9]				16 PIN DIL	— " — VERO	19-2178C	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

D.W.P.S. 8 BIT PATH CHR. SELECT DK2/1

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S. DWPS DH10/2

COMPILED BY T.J.P.C. DATE 11/11/83 SHEET No 2 OF 2.

ISSUED FOR ORDER No. FOR UNITS

I.O.S. FORM No. 105 (1/75)

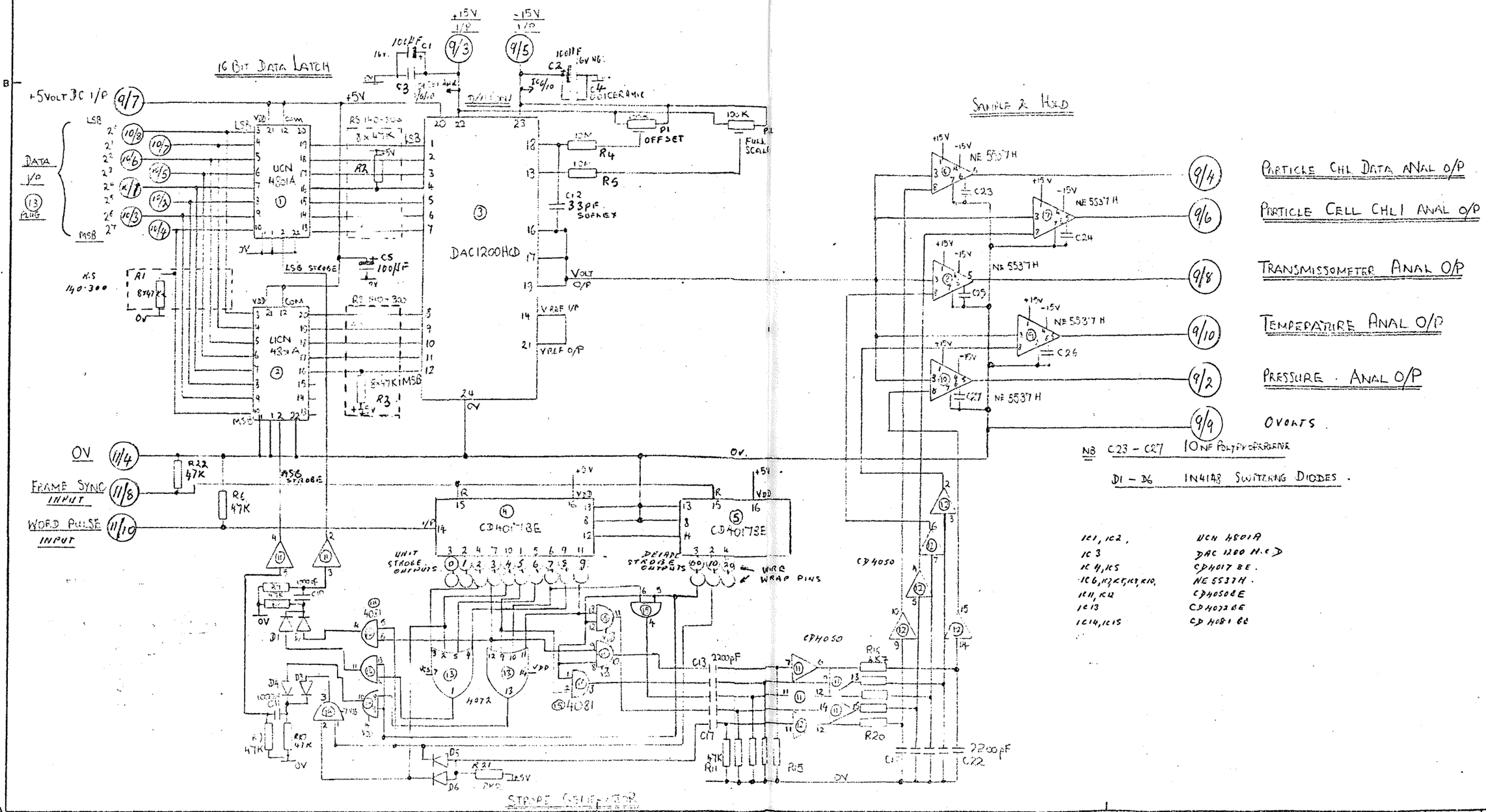
PRINT TRIMMING LINE

297 x 363mm

DWPS
DM11

PRINT TRIMMING LINE

INSTITUTE OF OCEANOGRAPHIC SCIENCES



NB C23 – C27 10NF POLYPROPYLENE

D1 – D6 IN4148 SWITCHING DIODES.

IC1, IC2,	UCN 4801A
IC 3	DAC 1200 H.C.D
IC 4, IC5	CD4017 BE.
IC6, IC7, IC8, IC9, IC10,	NE 5537H.
IC11, IC12	CD4050BE
IC13	CD4072BE
IC14, IC15	CD 4081 BE

INSTITUTE OF OCEANOGRAPHIC SCIENCES

TITLE D.W.P.S
DECK UNIT
BINARY DAC +5 OUTPUTS
DK3/1

ISSUE	DATE	AMENDMENT	ISSUE	DATE
1	JUNE'83			
2	9/6/83			
3	A - 7/8 SSG.			
4	4/10/83			
5	1/12/83			

CIRCUIT DWPS DM11 SHEET No.

I.O.S. FORM No. 107

PRINT TRIMMING LINE

BLANK SIZE - 360mm x 594mm

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
R1	RESISTANCE MODULE	8 X 47KΩ		8 COMMONED RESISTORS SIL	R.S COMPONENTS	140-300	
R2	-"-	-"-		-"-	-"-	-"-	
R3	-"-	-"-		-"-	-"-	-"-	
R4	RESISTOR	10MΩ	0.5W	CHARCOAL FILM CFR80	-"-	133-330	
R5	"	"	"	-"-	-"-	"	
R6	"	47KΩ	0.4W	METAL FILM MR25	-"-	148-893	
R7	"	"	"	-"-	-"-	-"-	
R8	"	"	"	-"-	-"-	-"-	
R9	"	"	"	-"-	-"-	-"-	
R10	"	"	"	-"-	-"-	-"-	
R11	"	"	"	-"-	-"-	-"-	
R12	"	"	"	-"-	-"-	-"-	
R13	"	"	"	-"-	-"-	-"-	
R14	"	"	"	-"-	-"-	-"-	
R15	"	"	"	-"-	-"-	-"-	
R16	"	4.7KΩ	"	-"-	-"-	148-663	
R17	"	"	"	-"-	-"-	-"-	
R18	"	"	"	-"-	-"-	-"-	
R19	"	"	"	-"-	-"-	-"-	
R20	"	"	"	-"-	-"-	-"-	
R21	"	8.2KΩ	"	-"-	-"-	148-714	
R22	"	47KΩ	"	-"-	-"-	148-893	
P1	TRIMMER	100KΩ	0.5W	25TURN CERMET POT	-"-	186-558	
P2	"	"	"	-"-	-"-	-"-	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

DWPS [FIDO] BINARY D.H.C. WITH 5 OUTPUTS

INSTITUTE OF OCEANOGRAPHIC SCIENCES DK3/1

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S. /DWPS DH11/1

COMPILED BY TJ'C, DATE 14/11/83 | SHEET No. 1 OF 3

ISSUED FOR ORDER No. FOR UNITS

I.O.S. FORM No. 105 (1 75)

PRINT TRIMMING LINE

297 x 363 mm

I.O.S. FORM No. 105 (1/75)

PRINT TRIMMING LINE

297 x 353 mm

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
C1	CAPACITOR	100μF.	16VOLT	ELECTROLYTIC RADIAL CEG SERIES	FARNELL	100 - 814	
C2	- " -	- " -	"	- " -	- " -	- " -	
C3	- " -	0·01 μF	100V	CERAMIC	STC	81237/XR7/0·01/±10%	
C4	"	0·01μF	100V	"	STC	"	
C5	"	100μF	10V	TANTALUM BEAD	RS COMPONENTS.	102 - 746	
C6/C9	REMOVED - ISSUE NO 4 -						USED WITH VERSION 1-2-3. WHEN MICROWAVE IS INSTALLED
C10	CAPACITOR	1000PF	100V	CERAMIC	STC	81237/XR7/0·001/±10%	
C11	"	1000PF	100V	CERAMIC	STC	- " -	
C12	"	33PF	160V	POLYSTYRENE TYPE EP9	SUPREX		
C13-C22	"	2200PF	100V	CERAMIC	STC	81237/XR7/0·0022/±10%	
C23-C27	"	0·01μF	63V	POLYPROPYLENE. WIMA FKP2	FARNELL	143 - 703.	
IC1	INTEGRATED CIRCUIT	UCN4801A		LATCH-DRIVER	R.S COMPONENTS	302 - 570	SPRAGUE [MANUFACTURE]
IC2	- " -	"		"	"	"	"
IC3	"	DAC1200HCD		BINARY DAC. 12BIT.	FARNELL	DAC1200HCD	NAT S.C
IC4	"	CD4017BE		CMOS DECADE	R.S COMPONENTS	306 - 588	
IC5	"	"		"	"	- " -	
IC6 - IC10	"	NE5537H		SAMPLE & HOLD	FARNELL	NE5537H	8 PIN TO-99
IC11	"	CD4050BE		CMOS BUFFER HEX.	R.S. COMPONENTS	306 - 673	
IC12	"	"		"	"	- " -	
IC13	"	CD4072BE		CMOS DUAL 4 I/P OR	"	309 - 694	
IC14	"	CD4081BE		CMOS QUAD 2 I/P AND	"	308 - 405	
IC15	"	"		"	"	- " -	
D1 - D6	DIODE	IN4148		SI. SWITCHING DIODE	"	271 - 606	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

D.W.R.S [FIDO] BINARY DAC WITH SCOPUTS.

INSTITUTE OF OCEANOGRAPHIC SCIENCES DR3/1.

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S. / DWRS DR1/2

COMPILED BY DATE SHEET No. 2 OF 3.

ISSUED FOR ORDER No. FOR UNITS

I.O.S. FORM No. 105 (1/75)

PRINT TRIMMING LINE

297 x 363 mm

CIRCUIT DIAGRAM SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	RATING	GRADE	TYPE	TRADE OR SUPPLIERS NAME	REFERENCE No.	
CON 9	CONNECTOR	10WAY		MOLEX PCB MOUNTING			
CON 10	"	"		TYPE KK	FARNELL	143-523	MATING FREE SOCKET
CON 11	"	"		MOLEX	REF 22-27-2101		REF 22-01-2105
IC HOLDER [IC1, IC2]				22PIN DIL EXTRA LOW PROFILE	VERO	19-2181K	
— " — [IC 3]				24 PIN — " —	VERO	19-2182E	
— " — [IC 4, IC5, IC11, IC12]				16 PIN — " —	VERO	19-2178C	
— " — [IC6, IC7, IC 8, IC9, IC 10]				8PIN (TO99) PINS ON 0.1" GRID	FARNELL	H23-2013	

REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE	REMARKS	ISSUE	DATE

DWPS [FIDO] BINARY DRC WITH 5 OUTPUTS DR3/1.

INSTITUTE OF OCEANOGRAPHIC SCIENCES

ELECTRONICS COMPONENTS FOR DRG. No. I.O.S. / DWPS DH11/3

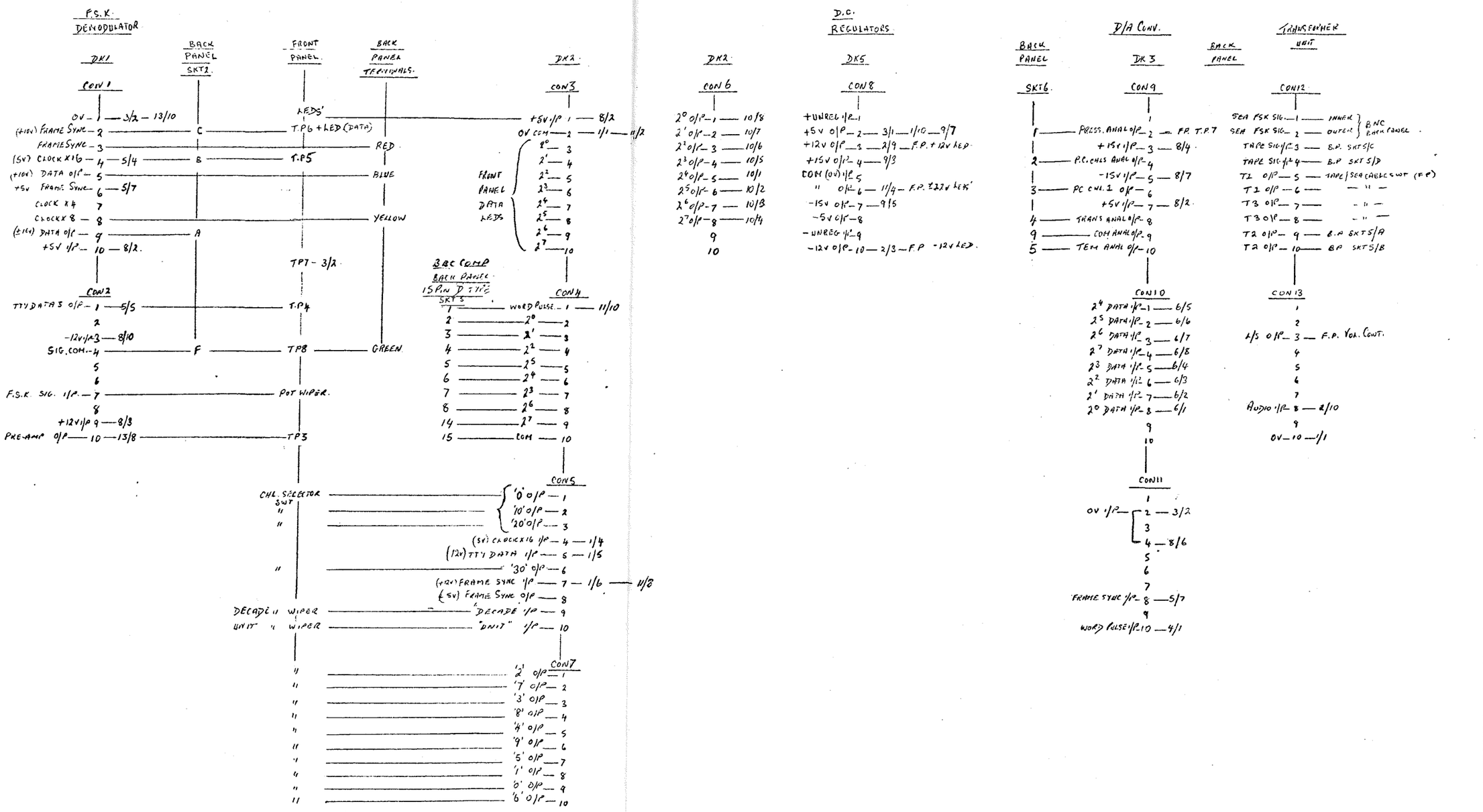
COMPILED BY T.J.A.C. DATE | SHEET No 3 OF 3

ISSUED FOR ORDER No. FOR UNITS

WORKING DYELINE 07.05.82

PRINT TRIMMING LINE

INSTITUTE OF OCEANOGRAPHIC SCIENCES



INSTITUTE OF OCEANOGRAPHIC SCIENCES	TITLE D.W.I.P.S. F.S.K. DEMODULATOR DECK UNIT INTER-CONNECTION DIAGRAM T.J.P.	First technical issue.	1	20-3-84			CIRCUIT DW DU 15
							SHEET No.
		AMENDMENT	ISSUE	DATE	AMENDMENT	ISSUE	DATE

Wokring Dyaline 0893/82

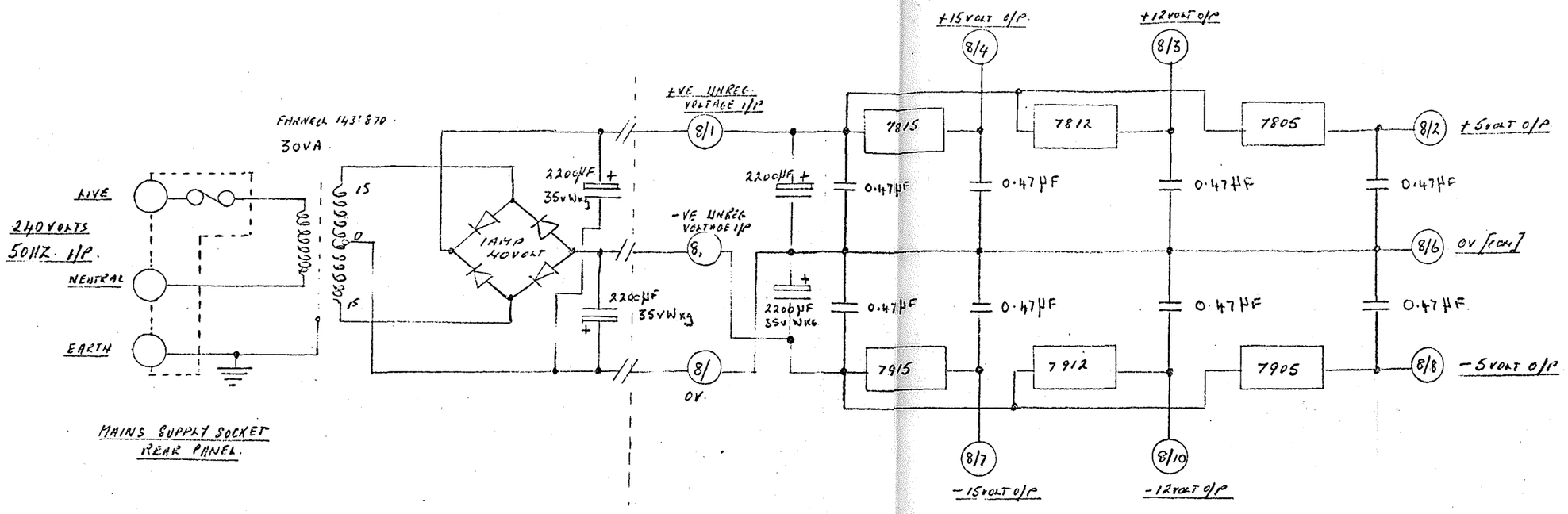
PRINT TRIMMING LINE

I.O.S. FORM No. 107 (1)

BLANK SIZE - 360mm x 594mm

PRINT TRIMMING LINE

INSTITUTE OF OCEANOGRAPHIC SCIENCES



MAINS SUPPLY SOCKET
REAR PANEL.

UNREGULATED DC SUPPLY P.C.B.

D.C. REGULATING P.C.B. DK5.

B

A

INSTITUTE OF OCEANOGRAPHIC SCIENCES	TITLE D.W.P.S. F.S.K. DEMODULATOR DECK UNIT D.C. SUPPLY SYSTEM. T.J.K.	FRENCH UNIT ISSUE	1	16-4-84				CIRCUIT No. D.W.P.S. D.17,16.
								SHEET No.
		AMENDMENT	ISSUE	DATE	AMENDMENT	ISSUE	DATE	

Ag Drawing 0823/92

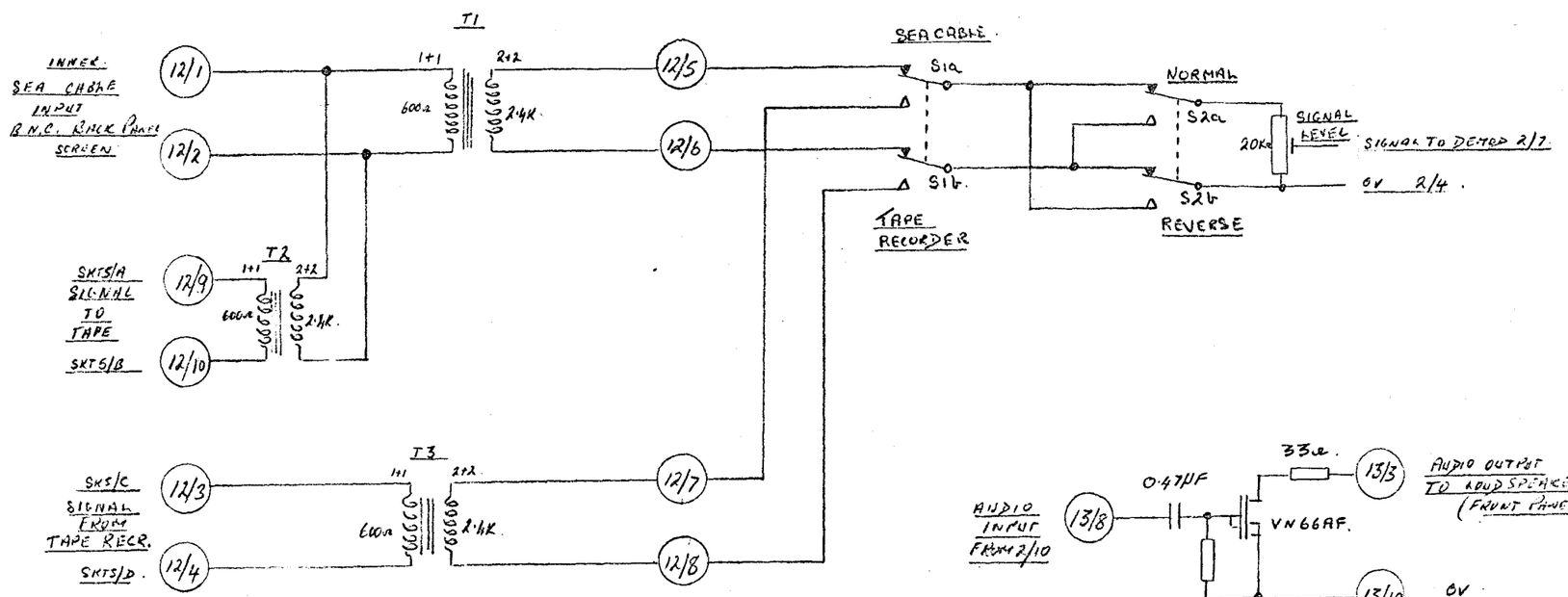
360mm x 594mm

PRINT TRIMMING LINE

I.O.S. FORM No. 107 (1/75)

PRINT TRIMMING LINE

INSTITUTE OF OCEANOGRAPHIC SCIENCES



Note :-

1. S1 & S2 MOUNTED ON FRONT PANEL.
2. T1, T2, T3, AVAILABLE FROM RS COMPONENTS REF. No 217-797

PRINTED CIRCUIT P.C.B DK6

LOUD SPEAKER OUTPUT

INSTITUTE OF OCEANOGRAPHIC SCIENCES	TITLE D.W.P.S F.S.K DEMODULATOR DECK UNIT DATA TRANSCEIVER UNIT DK6							CIRCUIT No. DWPS DM17
		FRENCH ISSUE	1	17-4-84				SHEET No.
		AMENDMENT	ISSUE	DATE	AMENDMENT	ISSUE	DATE	

Working Drawing 0893/82

PRINT TRIMMING LINE

I.O.S. FORM No. 107 (1/75)

BLANK SIZE - 360mm x 594mm