INTERNAL DOCUMENT 226.

I.O.S.

AN ACOUSTIC DOPPLER CURRENT METER

by

J L WHELLOCK

Internal Document No 226

NATURAL ENVIRONMENT RESEARCH COUNCIL

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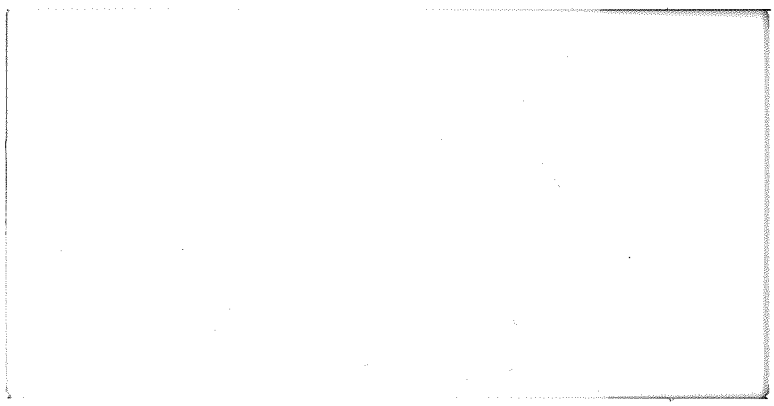

AN ACOUSTIC DOPPLER

CURRENT METER

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This report was prepared as part of a project for a Higher Technician Education Council Certificate in electronics completed at the Somerset College of Art and Technology.

Institute of Oceanographic Sciences
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ABSTRACT

The aim of this project was to design and construct a quadrature phase detector to be used in an acoustic doppler current meter being developed by the Institute of Oceanographic Sciences. The instrument will be used to measure the velocity of water flow close to the surface of the seabed.

The original circuit designs were produced by the United Hospital, Bristol where a similar system is being developed to measure the velocity of the blood flow through the blood vessels.

This system is constructed from discrete components, and is therefore difficult to build and use reliably. The aim was to replace them with designs based on integrated circuits.

INTRODUCTION

This report concentrates on one particular part of the acoustic doppler system but an outline is given in the first section of why it is needed and how it works. The rest of the report is given over to the theories of the processor circuit and the technical details of how it works. A series of circuits were built and tested and these results are also included.

At present, the processor board is made from discrete components, several of which must be measured and matched and the circuit has to be tuned to the correct frequency. Originally it was intended to evaluate the performance of a series of communications integrated circuits produced by Plessey. However, soon after the project had been set a new integrated circuit was released by Analog Devices, the AD539. This is a wideband dual channel multiplier/divider which appeared to satisfy the requirements. Using the preliminary data available circuits were built in order to compare them with the circuit already being used.

Using the results obtained it is hoped that a circuit may now be designed to replace the present circuit and be included in the instrument.

1.1 THE NEED FOR AN ACOUSTIC CURRENT METER

An important aspect of the research carried out at the Institute of Oceanographic Sciences involves the movement of sediments along the seabed. This is a very important subject as it includes the movement of sandbanks in estuaries and rivers, the accumulation of silt and sand in harbours, erosion of beaches etc.

In order to predict the movement of sediment in different areas over various lengths of time it is necessary to build up data on movement in particular sites. This is carried out in field work using various instruments each measuring a different component. A typical instrument rig would carry up to ten impellor type current meters, at various heights above the bed to give a velocity profile, impact sensors to record the number of sand particles moving in suspension, and a system which pumps samples up from the seabed collecting the sand which is in suspension.

All of these instruments create a bulky piece of equipment which in itself can cause turbulence and affect the readings that are made. They also lead to many different data channels which have to be logged and the analysis of the data is very lengthy.

Using acoustic instruments means that they can be placed away from the area being investigated and so cannot alter the natural effects that are taking place in the surrounding environment. The acoustic doppler current meter will measure the doppler shift that takes place when an acoustic beam is reflected back by sediment particles in suspension. This will give the velocity of the particles and by taking samples at different points along the axis of the acoustic beam, a velocity profile will be built up.

This technique could be a major step in helping to replace the many separate instruments used at the present time. It will also be able to measure sand movement on the surface of the seabed, which at the moment is only able to be judged by filming using underwater cameras and recording on video tape. Obviously this is not a satisfactory technique and only gives qualitative results.

1.2 THE DOPPLER EFFECT

A method used by the IOS(T) to measure the velocity of sand movement is based on the doppler effect. This is most easily explained as the change in pitch that occurs when the distance between the sound and the listener is changing at an appreciable rate. It is often experienced as the change in the note of a car horn being sounded as the car is being driven past the listener.

In practice the IOS(T) doppler current meter uses an acoustic frequency of 2MHz (to be changed to 5MHz). This is transmitted as a short pulse which is reflected back by the moving sand particles in the form of an echo. When a moving target, such as the sand particles, intercepts acoustic pulses from a stationary transducer, the echo reflected back shows two doppler effects. One is the shift in frequency when the receiver is moving with respect to the sound source, and the other occurs when the target, ie the echo, is moving with respect to the receiver.

In the IOS(T) doppler current meter the same transducer acts as both the transmitter and receiver so the doppler shift encountered is due to the moving target. This can be explained mathematically as follows.
Let the frequency transmitted by the transducer be f_0 (the carrier frequency) then the frequency reaching the target moving at a velocity V is f_1 and:

$$\frac{f_1}{f_0} = \frac{c + V}{c}$$

where c = velocity of sound in water

The target reflects an echo which is received by the transducer as f_2, therefore:

$$\frac{f_2}{f_1} = \frac{c}{c - V}$$

These two equations may be combined to give:

$$\frac{f_2}{f_0} = \frac{c + V}{c - V}$$

The total shift in frequency, known as target doppler is the difference between the frequency that is transmitted and the frequency that is received:

$$f_2 - f_0 = \frac{2Vf_0}{c}$$

This doppler shift is usually known as f_D:

$$f_D = \frac{2Vf_0}{c}$$

This equation assumes that the transducer is mounted at 90° to the flow axis, however in practise it will be mounted at an angle θ as shown in figure 1 below:

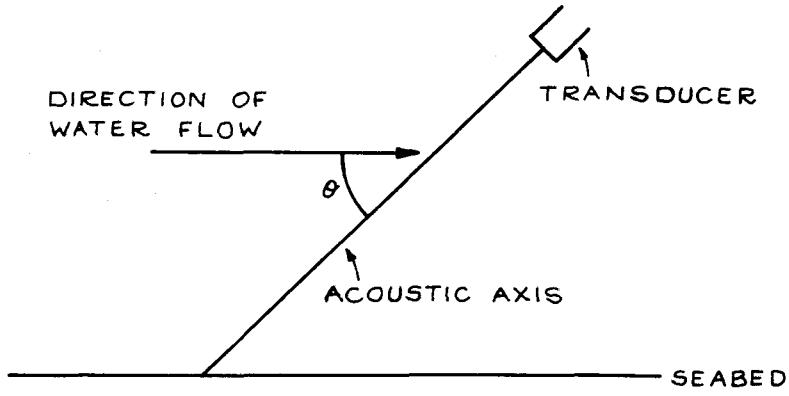


Figure 1. THE POSITION OF THE TRANSDUCER

To allow for this the final equation becomes:

$$f_D = \frac{2Vf_0}{c} \cos \theta$$

1.3 VELOCITY RESOLUTION

Velocity resolution is determined by the shape of the doppler power spectrum. The ideal spectrum would be a single pulse at frequency f_D. However in a practical system there are several factors which may broaden this ideal. These include flow gradients, angular beamwidth and finite transit time effects.

The effects of the beamwidth angle can be minimised by designing a transducer with a very narrow beamwidth. However the effects of the transit time can limit the time available for processing. The best doppler resolution that may be obtained is given by

$$\Delta f_D = \frac{1}{T_t}$$

where T_t = transit time

However this does not take into account the velocity gradients that may occur in the volume of water in the active part of the acoustic beam. This can cause an increase in the spectrum width which is greater than the limitation due to the transit time.

1.4 BASIC DESCRIPTION OF THE DOPPLER SYSTEM

The parts making up the doppler system have been broken down and shown in block diagram form in figure 3. In order to understand how the instrument works the action of each part is briefly described below and the waveforms present are shown in figure 4.

The Master Oscillator

This provides an accurate 2MHz square wave output. The output frequency may be tuned so that it can be matched to the individual transducer being used. It also provides the basic frequency for the transmission gate, the sample pulse and the quadrature generator. This ensures that the various pulses around the circuit are all linked in phase.

The Transmitter

This consists of a transmission gate generator which derives a suitable output pulse to switch on the transmitter and to blank the receiver from 'seeing' the transmitted pulse, see figure 2 below. The transmission pulse is then amplified to a level which can drive the transducer.

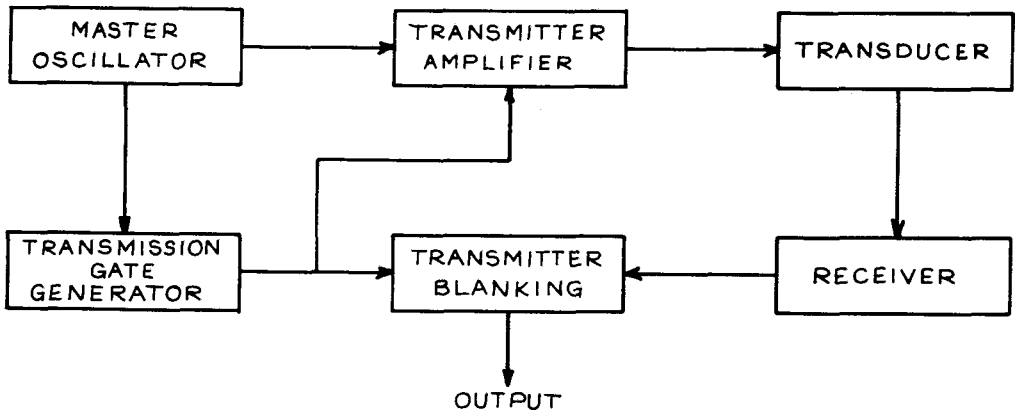


Figure 2

The Transducer

A piezo electric ceramic crystal transducer is used in the doppler. Its resonant frequency is 2 MHz and it has a very narrow beamwidth.

The Receiver

The receiver is basically an amplifier which boosts the signal coming from the transducer to a suitable level to drive to following processing stages. It is blanked by the transmission gate to prevent the transmitted signal getting through.

Quadrature Generator

This takes the 2MHz signal from the oscillator and introduces a 90° phase shift. This results in two signals in quadrature which are used to give the two channels in the processor. This means that the instrument can detect whether the sand particles are moving towards or away from the acoustic axis.

The Processor Board

This is described in more detail in the next section but basically it takes the signal from the receiver which contains the doppler frequency and transmitter frequency and separates them to output the doppler frequency f_D.

The Sample and Hold Circuit

This circuit determines the point along the length of the beam at which the velocity is sampled. At present only one point may be sampled but it is hoped to increase this so that up to say ten points may be sampled along the beam in order to produce a velocity profile.

This output is filtered and put through a phase locked loop to give the final output. The doppler frequency can then be displayed on a spectrum analyser or recorded on a data logger.

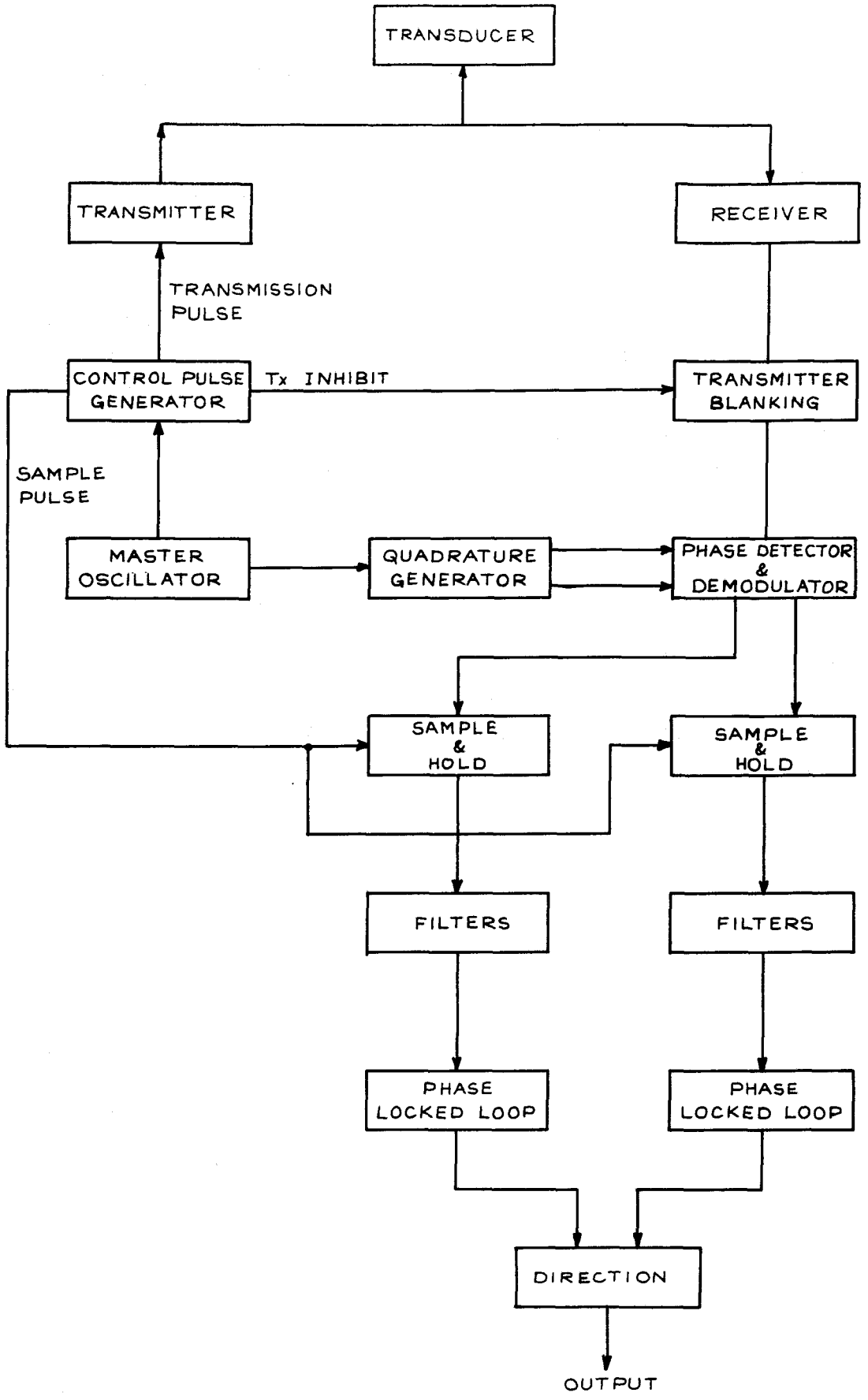


Figure 3. BLOCK DIAGRAM OF THE DOPPLER

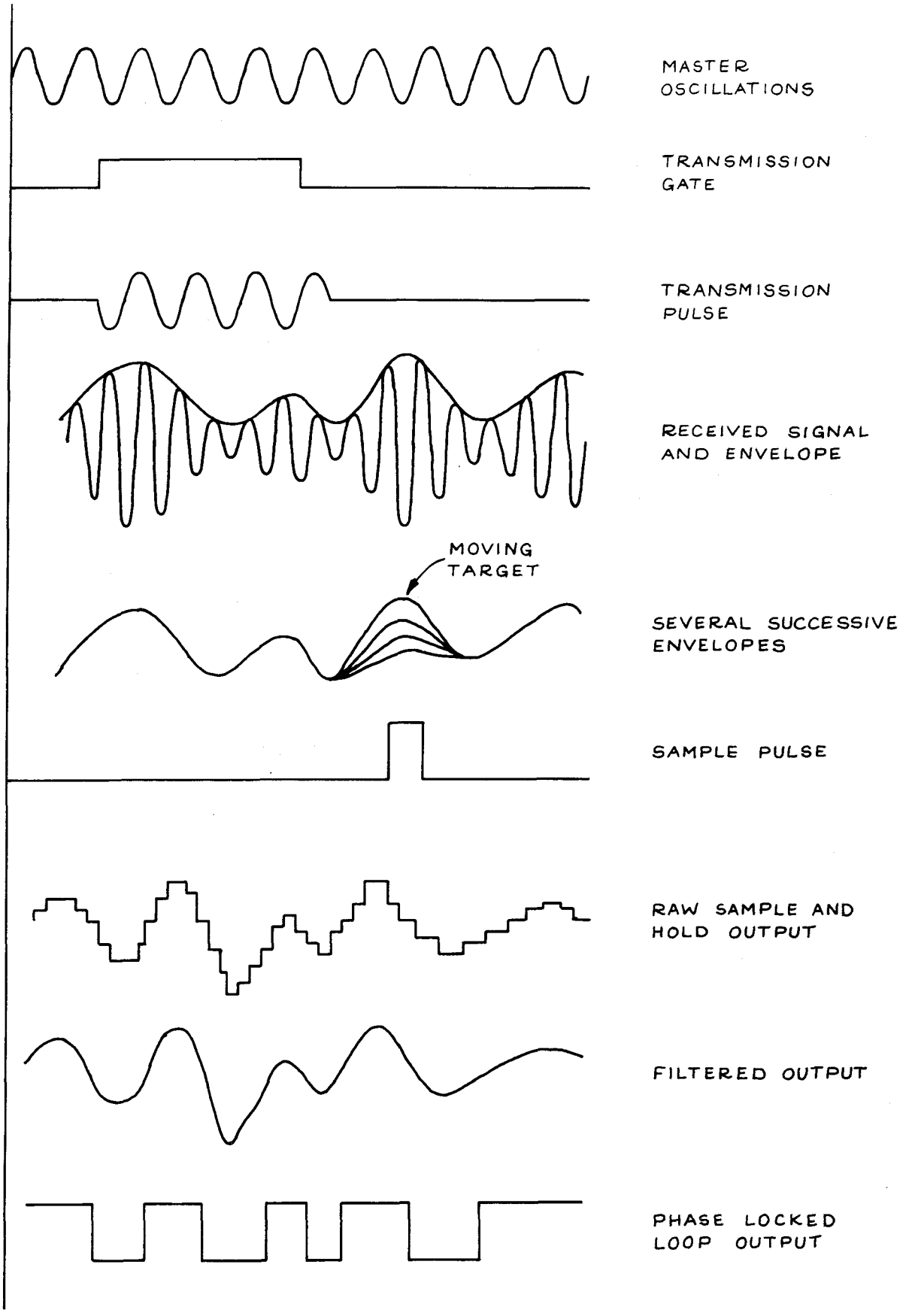


Figure 4. DOPPLER WAVEFORMS

2.1 THE DOPPLER PROCESSOR BOARD

In section 1.4 the doppler processor was described as separating the doppler frequency from the mixture of frequencies making up the signal received from the transducer. In order to understand how this is accomplished it is necessary to give a brief outline of amplitude modulation. The theory of amplitude modulation is the basis upon which the processor works.

2.2 THE PRINCIPLE OF MODULATION

Modulation is a process by which a high frequency carrier wave is altered according to a modulator frequency such as a voice. It is done so that the modulating frequency is put into a form which may be transmitted over long distances eg radio. There are four basic methods of modulation:

i. Pulse Modulation - the carrier frequency is switched on and off according to a code.

ii. Amplitude Modulation - the amplitude of the carrier wave is varied by the modulating signal.

iii. Frequency Modulation - the frequency of the carrier is varied by the frequency of the modulator.

iv. Phase Modulation - where the phase of the carrier is varied by the modulator.

2.3 AMPLITUDE MODULATION

In any type of modulation there is a basic carrier wave, usually a sine wave, which is modulated according to the information (modulating) signal.

The equation for a sinusoidal carrier wave may be written as:

$$v_c = A \cos (w_c t + \theta)$$

where v_c is the instantaneous carrier voltage

In amplitude modulation the frequency w_c is constant while the amplitude A is varied. This gives rise to the following waveforms:

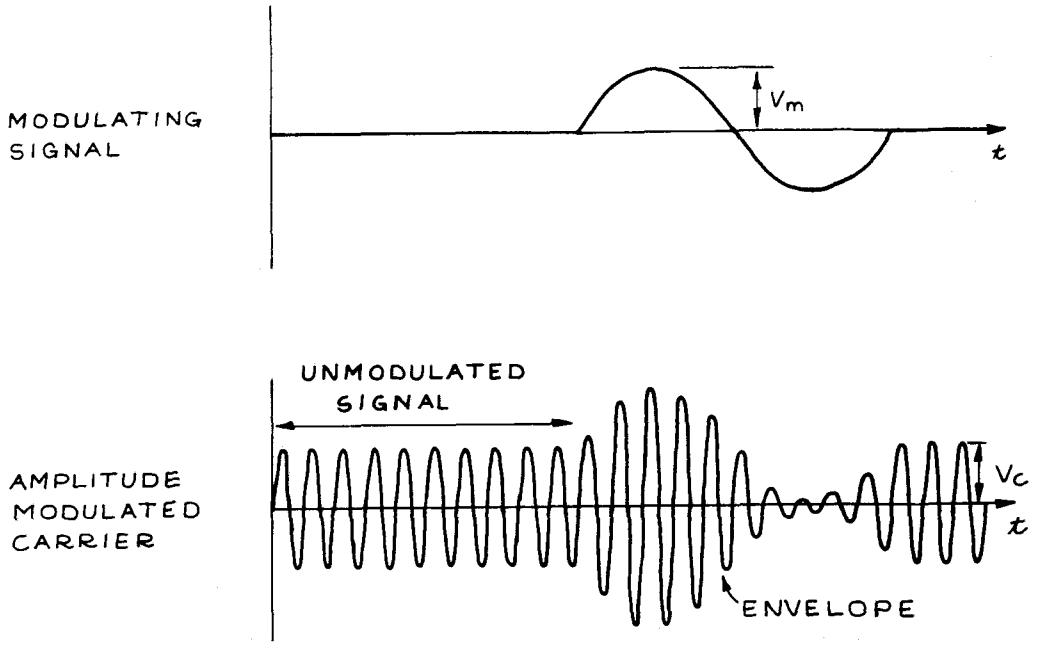


Figure 5. AMPLITUDE MODULATION WAVEFORMS

If the modulating signal is also sinusoidal, as above, then:

$v_m = Vm \cos w_m t$ where vm = instantaneous voltage
Vm = maximum voltage

If the amplitude of the carrier is varied by this signal then:

$$A = Vc + Vm \cos w_m t$$

$$A = Vc \left(1 + \frac{Vm}{Vc} \cos w_m t\right)$$

The ratio of Vm/Vc is known as the modulation factor, m_a and should not exceed 1. ie the modulating signal should always be smaller than the carrier.

This gives us the instantaneous voltage for the modulated carrier wave as:

$$v = Vc(1 + m_a \cos w_m t) \cos w_c t$$

When multiplied out it should be noted that the result includes the product of the two signals:

$$v = V_c \cos w_c t + m_a V_c \cos w_m t . \cos w_c t$$

By trigonometric identity the product of two cosines may be simplified:

ie $\cos A . \cos B = \frac{1}{2}[\cos(A + B) - \cos(A - B)]$

Therefore the complete equation will become:

$$v = V_c \cos w_c t + \frac{m_a V_c}{2} \cos(w_m + w_c)t - \frac{m a V_c}{2} \cos(w_c - w_m)t$$

This equation reveals how the amplitude modulated wave is not made up of one frequency but in fact contains three. These are the original carrier frequency, the sum of the carrier and modulating frequencies and the difference between the carrier and modulator.

The sum and difference frequencies are known as the upper and lower side frequencies respectively. When the modulator is made up of a complex waveform containing many frequencies then a group of side frequencies will be produced. These are then called sidebands.

A diagram showing the frequency spectrum obtained when a carrier is modulated by a group of frequencies is shown in figure 6.

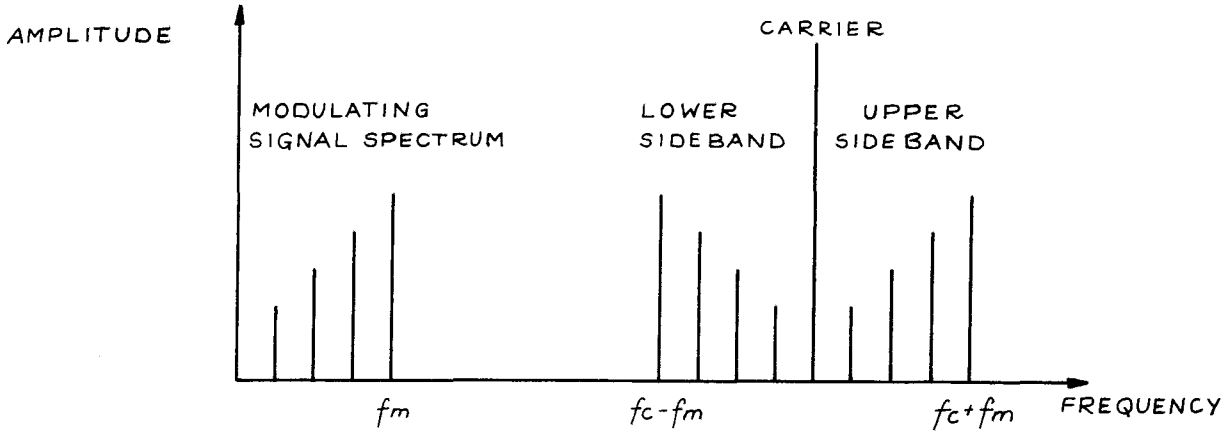


Figure 6. FREQUENCY SPECTRUM OF AMPLITUDE MODULATION

One important point to note from this frequency spectrum is the way in which the bandwidth of the amplitude modulated signal is doubled compared with the original signal bandwidth. This large bandwidth can be a problem in radio transmitting as the radio spectrum is very crowded. This has led to techniques such as single sideband transmission (SSB) where only one of the sidebands is transmitted as they both hold the same information.

2.4 APPLICATION OF AM TO THE DOPPLER PROCESSOR

The Doppler processor board is divided into two channels, one in quadrature with the other. This is in order to establish the direction in which the sand particles are moving. They could be moving towards the acoustic beam axis or away from it.

Each of these channels works in exactly the same way the only difference being the 90° phase shift in the carrier waveform.

The part of the board which processes the signal is basically an AM modulator. It uses the original 2MHz signal from the master oscillator as the carrier, and then modulates it with the signal being received from the transducer.

The signal being received by the transducer is made up of the 2MHz signal which was transmitted and the doppler frequency f_D. This frequency changes according to the velocity of the flow, but it is always a very low frequency compared with the transmitted pulse. This results in the received signal being very close in frequency to the original frequency.

Therefore when the receiver signal is used to modulate a carrier frequency of 2MHz the sidebands that are produced will be made up of the doppler frequency. This is more easily understood by considering the frequency spectrum which results when a frequency close to the carrier is used as the modulator:

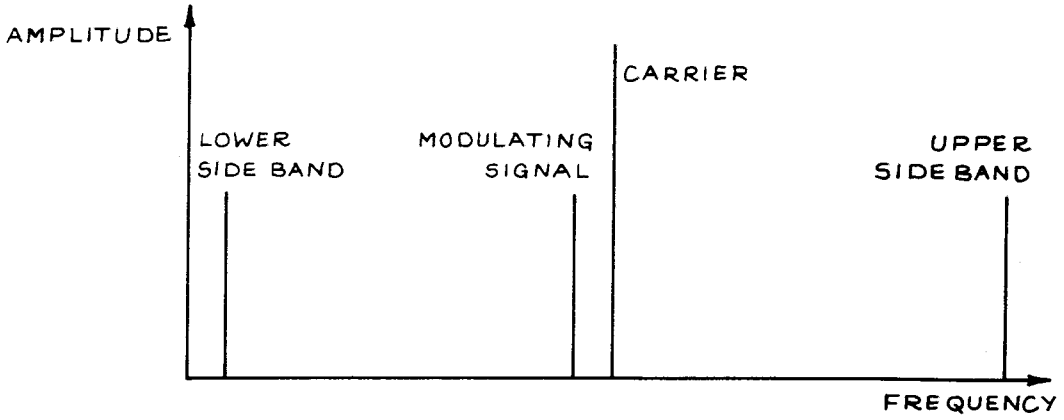


Figure 7. FREQUENCY SPECTRUM WITM Fm CLOSE TO Fc

The important thing to note from this frequency spectrum is the way that the two sidebands have been separated from the carrier frequency. It is using this method that the doppler frequency is separated from the transmitted frequency.

Consider the modulating frequency made up of the carrier and doppler frequencies:

$$f_m = f_c - f_D$$

This results in the two sidebands becoming:

$$\text{L.S.B.} = fc - fm$$

$$= fc - (fc - fD) = fD$$

$$\text{U.S.B.} = fc + fm$$

$$= fc + (fc - fD) = 2fc - fD$$

Thus, the lower sideband is made up of just the doppler frequency. As this frequency is extremely low compared with the other frequencies that are present it is a simple matter of filtering the signal to leave just the doppler frequency.

Once the doppler frequency has been obtained it can be displayed on an oscilloscope or spectrum analyser, and measured using a frequency counter. The raw signal is fed through a phase-locked loop to "maintain" the doppler frequency, which "drops out" between the echos received from individual sand particles, in order that the signals can be counted digitally and recorded.

The circuit used to carry out this process is made up of a balanced modulator and tuned circuits which will be described in the next section along with the practical tests that have been carried out in order to replace this circuit.

3.1 THE SINGLE CHANNEL PROCESSOR

As each channel of the processor board has an identical circuit it is easier to consider the circuit of just one channel.

Before describing the practical work carried out for this project a more detailed description will be given of the present circuit and the reasons why it needs to be changed.

The circuit diagram for the single channel circuit is shown below

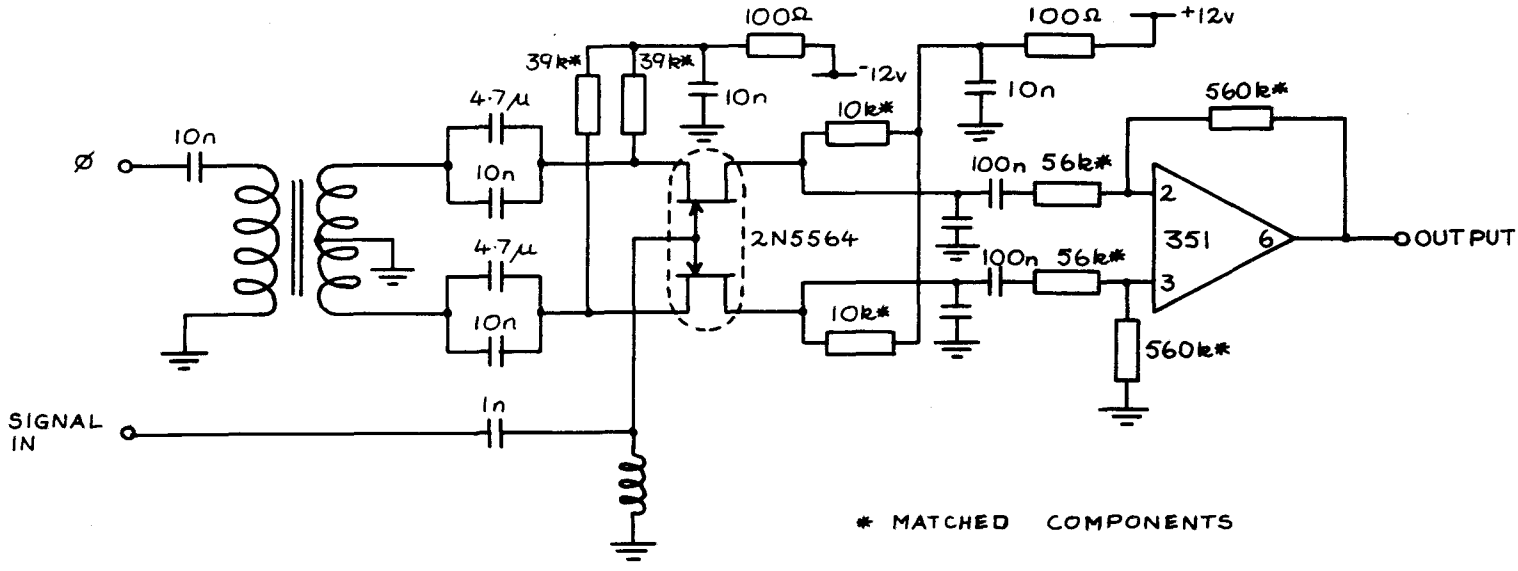


Figure 8. SINGLE CHANNEL PROCESSOR

This is basically a balanced modulator the operation of which is based upon the non-linear characteristic of the field-effect transistor. The output current of the FET can be expressed as:

$$i = a_1v + a_2v^2 + a_3v^3 + ----$$

This current is controlled by the voltages that are present at the gate and across the drain and source of the FET. In this case the gate voltage is the modulating frequency and the source/drain voltage is due to the carrier frequency.

The carrier signal is put through a centre tap transformer so that the carrier voltages at the two FET's are in antiphase. This results in the voltages controlling the two FET's becoming:

$$\text{Controlling } T_1 = Vm \sin w_m t + Vc \sin w_c t$$

$$\text{Controlling } T_2 = Vm \sin w_m t - Vc \sin w_c t$$

Therefore the output currents of each transistor will be:

$$i_1 = a_1Vm \sin w_m t + a_1Vc \sin w_c t + a_2V^2m \sin^2 w_m t + 2a_2Vm\,Vc \sin w_m t \sin w_c t + a_2V^2c \sin^2 w_c t + ----$$

and

$$i_2 = a_1Vm \sin w_m t - a_1Vc \sin w_c t + a_2V^2m \sin^2 w_m t - 2a_2Vm\,Vc \sin w_m t \sin w_c t + a_2V^2c \sin^2 w_c t + ----$$

These two signals are then passed through a differential amplifier which will output the difference between these two signals. It is also designed so that it will amplify them by a factor of ten. The output thus becomes:

$$Vo = 2 \times 10(a_1Vm \sin w_m t + 2a_2Vm\,Vc \sin w_m t \sin w_c t + ----)$$

The second part of the equation is the product of two sine waves which has been explained previously to give the two sidebands of amplitude modulation. The lower sideband which is the one required will be separated using a low pass filter. This filtering will also remove any of the harmonics of the carrier wave which could be generated by the higher orders of the FET characteristics.

3.2 DISADVANTAGES OF USING DISCRETE COMPONENTS

Although the single channel processor as described above is fairly straightforward in the way it works in theory, it is not quite so simple in practise.

The values of several of the components have to be calculated to tune them to the frequency being used. This can cause a problem where inductors are

involved, especially in the case of the transformer which has to be wound by hand.

It is also extremely important that the two field effect transistors are matched in order to ensure a balanced output. This is why a single chip with two matched transistors has been chosen to replace the two separate transistors in the original circuit.

Several resistor values also have to be matched, again to keep a balanced system. This can be very time consuming as the resistors must be measured on a bridge until two are found with equal values.

A printed circuit board has been designed for this circuit which does help to make it easier to build once the components are ready. However the PCB had to be designed very carefully because of the number of different connections between the separate components.

All of this makes the production of the circuit very lengthy and it is not very easy to test and use.

3.3 USING THE AD539

The AD539 is a single integrated chip which maybe used as a dual channel multiplier or divider. In section 2.3 it was noted that the output required is a product of two signals in order to separate the sidebands and carrier. Therefore in order to investigate the operation of the AD539 a wideband single channel multiplier was built using the manufacturers circuit details. This was again designed on a printed circuit board to overcome any difficulties that mght be caused by using high frequencies. A photograph of this board is shown in figure 10 and should be compared with the size and complexity of the discrete component board in figure 11. The circuit diagram is shown below:

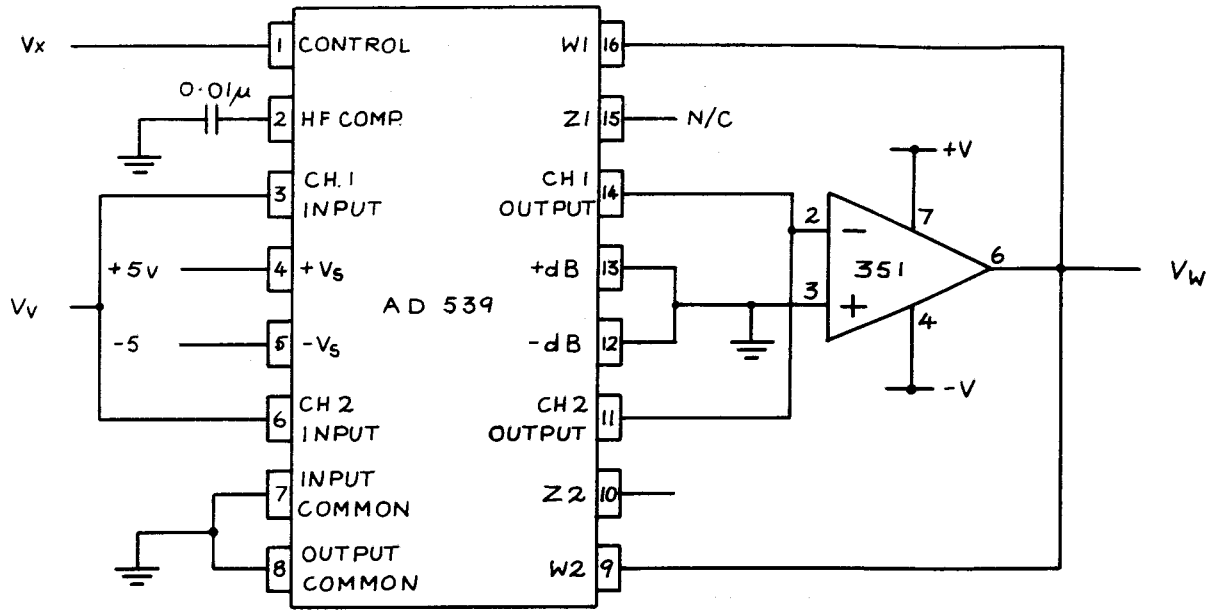


Figure 9. WIDE BAND SINGLE-CHANNEL MULTIPLIER

Although the AD539 is a dual channel device the two signal channels maybe connected in parallel to give a single channel multiplier which is simpler to investigate.

The output of the device is quoted in the data as being:

$$Vw = -Vx.Vv$$

Vx is the control signal which will be used as the carrier wave in this application, while Vv will be the modulating signal. This will result in the output becoming:

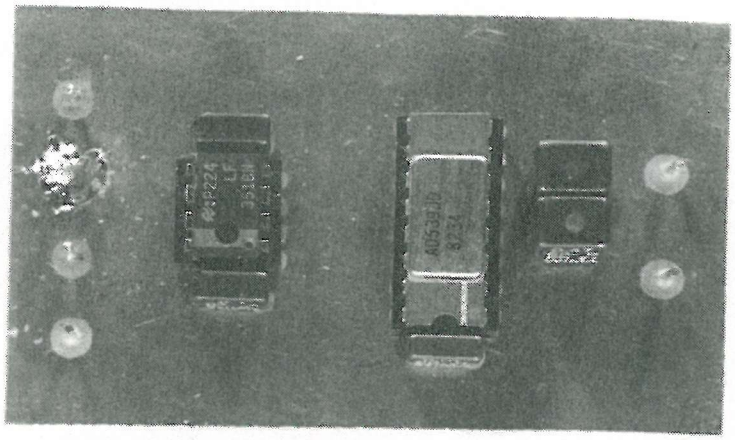
$$Vw = -(Vc \cos w_c t)\ (Vm \cos w_m t)$$

$$= -Vc\ Vm(\cos w_c t.\cos w_m t)$$

$$= \frac{-Vc\ Vm}{2}\ [\cos(w_c + w_m)t - \cos(w_c - w_m)t]$$

This equation is made up of just the lower and upper sidebands without the carrier. In order to establish whether this is the output of the circuit, it is necessary to test it.

Figure 10. INTEGRATED CIRCUIT MULTIPLIER



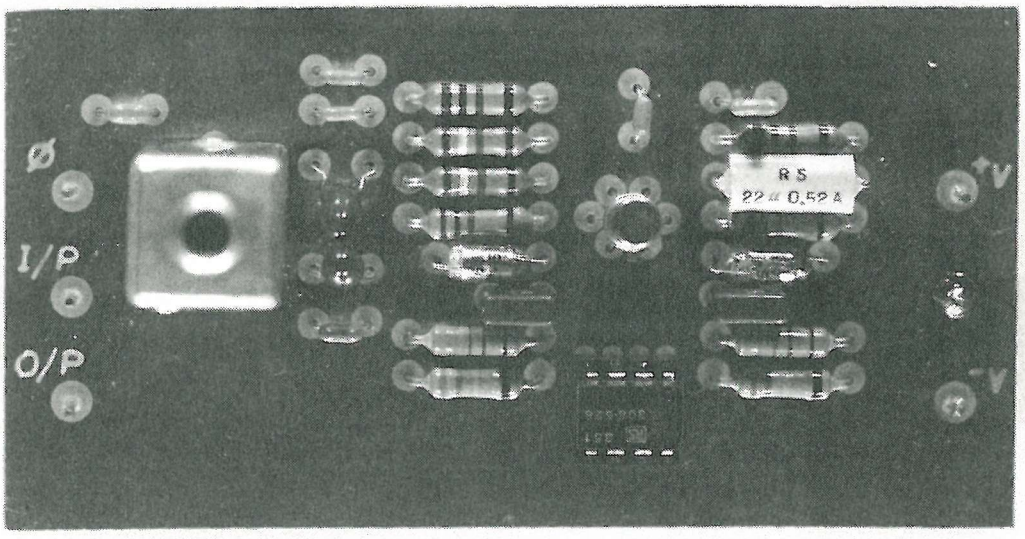


Figure 11. DISCRETE COMPONENT CIRCUIT

3.4 TESTING THE SINGLE CHANNEL MULTIPLIER

The equipment needed to test the circuit is shown below and in figure 13

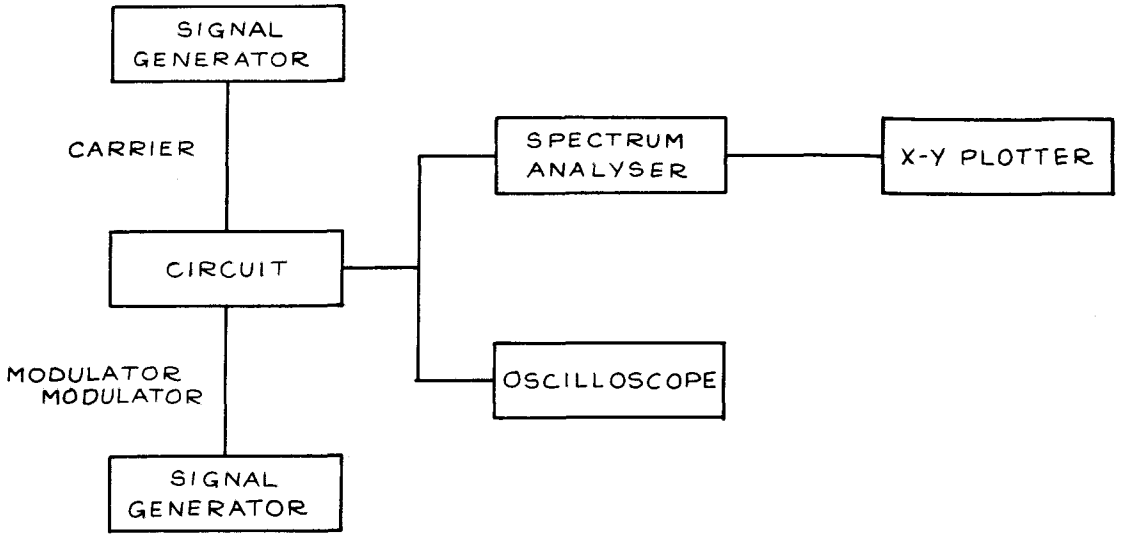


Figure 12. TEST EQUIPMENT

The carrier frequency and modulating signal are provided by two signal generators. The output of the circuit is displayed on an oscilloscope and its frequency response is displayed on a spectrum analyser. The spectrum analyser gives a suitable output for plotting on an X-Y plotter.

The spectrum analyser used can display a maximum frequency of only 50 kHz so for the purpose of this test a carrier frequency of 25 kHz was chosen. This was to ensure that both of the sidebands could be displayed. In order to separate the two sidebands, the frequency of the modulating signal was chosen to be close to the carrier frequency. This is also what would happen in the acoustic doppler as explained in section 2.4.

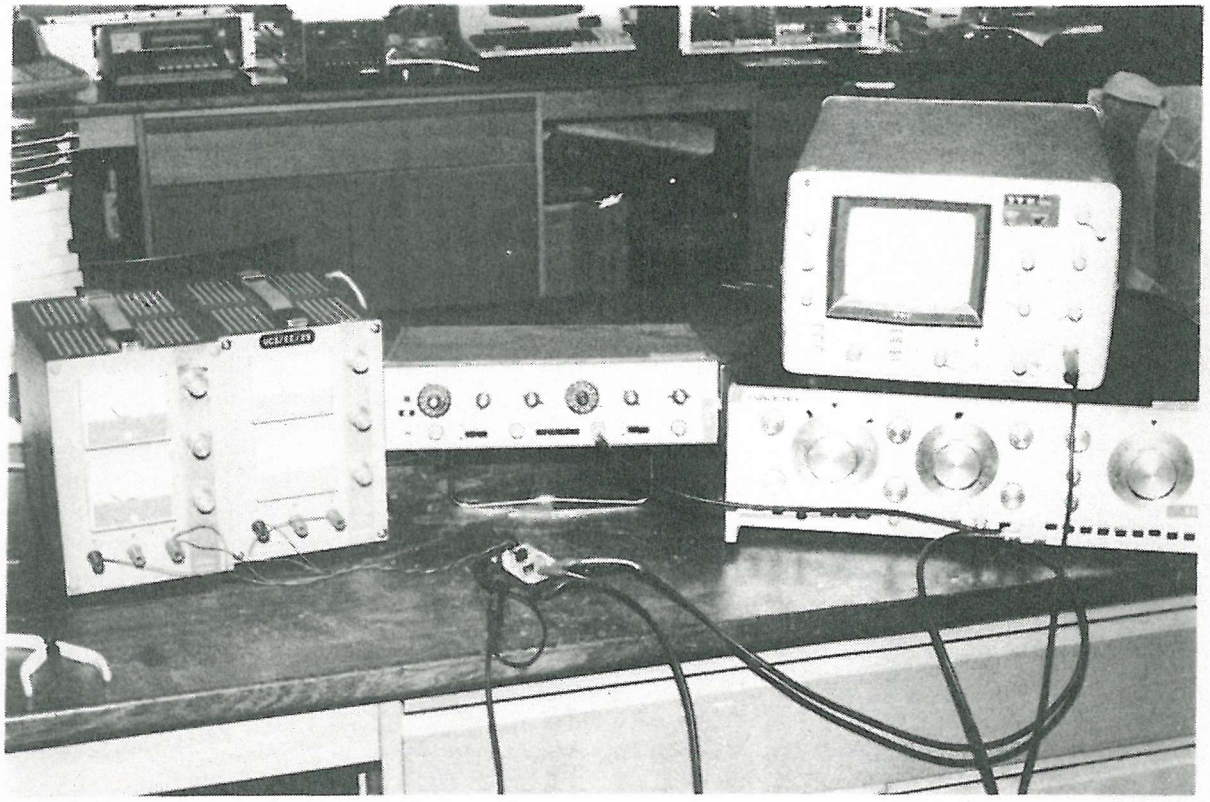


Figure 13. TEST EQUIPMENT

Results

An example of the type of output obtained from this circuit has been plotted and is shown in figure 14. The upper and lower sidebands are clearly displayed but it is evident that the modulating frequency and carrier frequency have also broken through. This should not be a problem in this application as in practise the carrier and modulating signal will be at approximately 2 MHz and can be filtered out. If a low pass filter is used to filter the output then only the lower sideband will get through, see figure 15.

From these results it would appear that this simple circuit would give very similar results to the discrete component circuit. In order to verify this the two circuits must be compared under the same conditions.

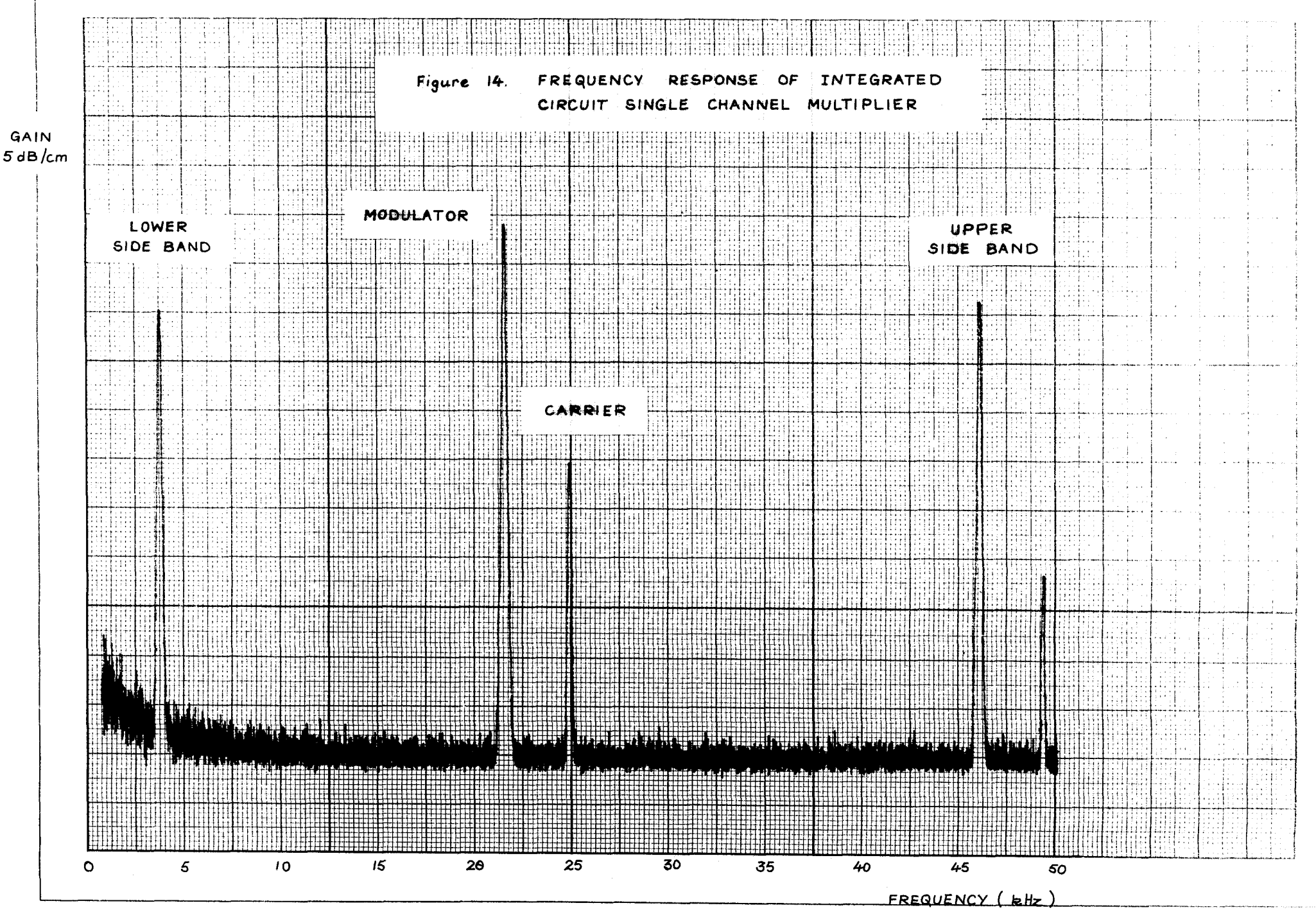


Figure 14. FREQUENCY RESPONSE OF INTEGRATED CIRCUIT SINGLE CHANNEL MULTIPLIER
GAIN
5 dB/cm
LOWER
SIDE BAND
MODULATOR
CARRIER
UPPER
SIDE BAND
0
5
10
15
20
25
30
35
40
45
50
FREQUENCY (kHz)

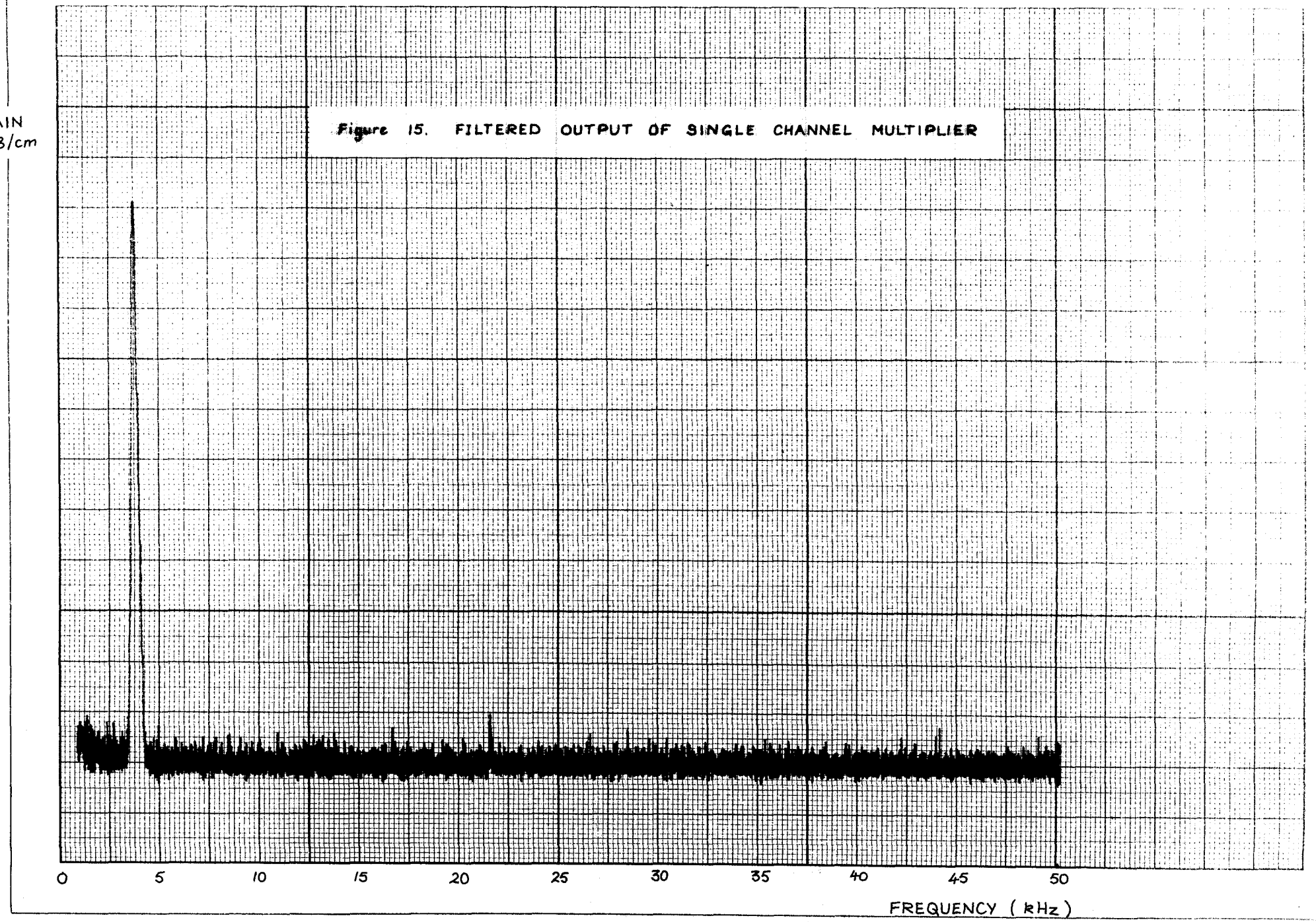


Figure 15. FILTERED OUTPUT OF SINGLE CHANNEL MULTIPLIER

3.5 COMPARISON OF THE TWO CIRCUITS

As the discrete component circuit is tuned to a specific frequency (in this case 5 MHz) it therefore dictates the frequency that can be used as the carrier in this comparison.

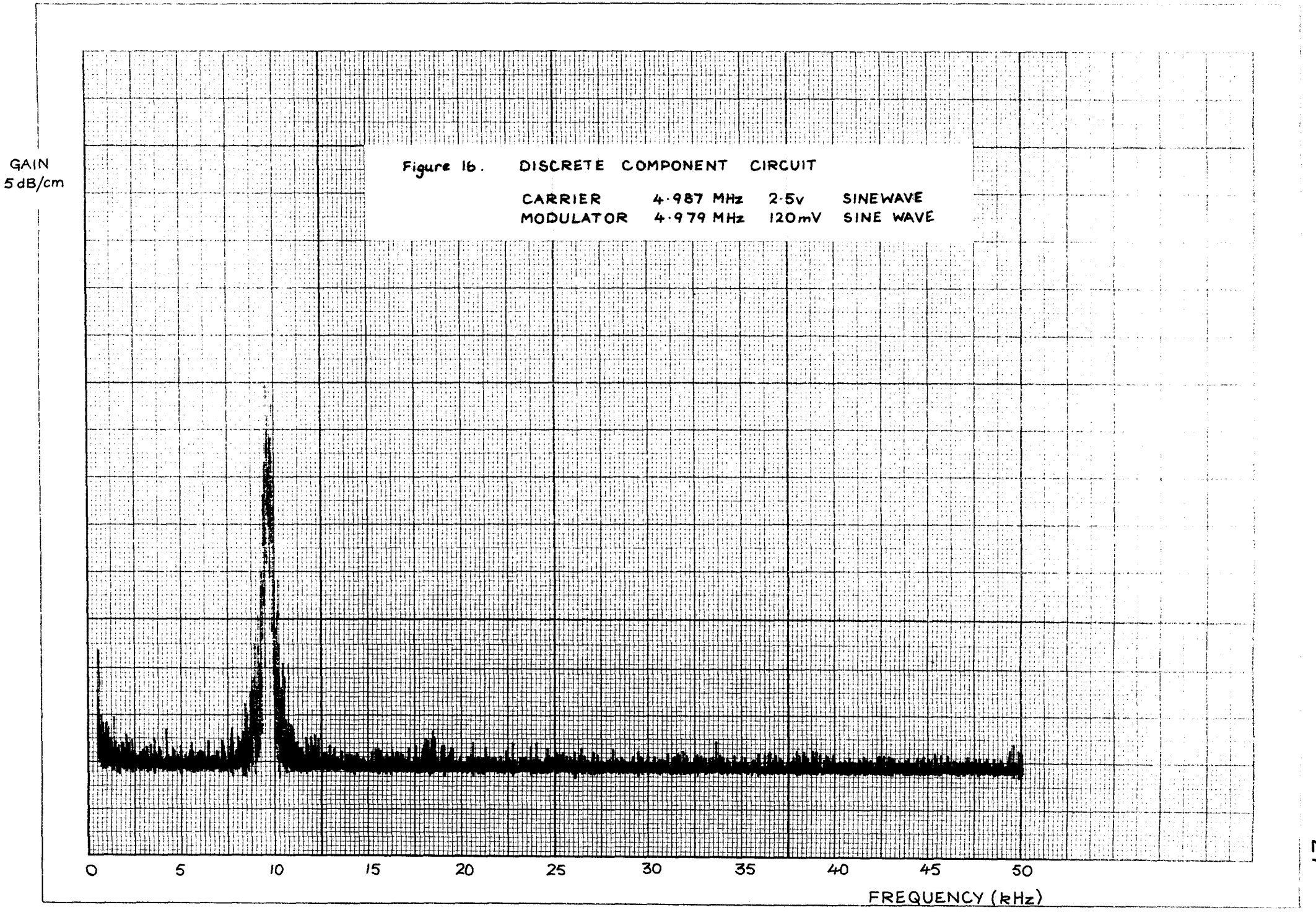
However, as the spectrum analyser can only work up to a frequency of 50 kHz the whole of the frequency spectrum cannot be displayed. To overcome this the modulating frequency is set to be less than 50 kHz so that the lower sideband can be seen. In this experiment then only the lower sidebands of the two circuits may be compared. As this is the portion of the signal that is important this is not a problem.

Using the equipment as described previously the two circuits were set up using the same carrier signal. It soon became obvious that the AD539 circuit needed a larger modulating signal in order to drive it and that the discrete component circuit would be overdriven by the same size signal. This is probably due to the amplification in the discrete component circuit caused by the differential amplifier. Therefore in this comparison, although the frequencies of the modulator and carrier are equal, the amplitude of the modulator was attenuated by 20 dB's before being input to the discrete component circuit.

Results

Plots taken from the two circuits are shown on the following pages. Figures 16 and 17 show the outputs of the two circuits when used with a sinusoidal carrier, while figures 18 and 19 show the outputs with a square wave carrier. In practise the carrier will be square wave generated from the master oscillator circuit.

The two traces from the sinusoidal carrier input are very similar giving a good comparison. The two square wave traces also give a good comparison taking into account the frequency drift of both of the signal generators and the rather poor signal shape they give at high frequencies.


GAIN
5 dB/cm
Figure 16. DISCRETE COMPONENT CIRCUIT
CARRIER 4·987 MHz 2·5v SINEWAVE
MODULATOR 4·979 MHz 120mV SINE WAVE
0
5
10
15
20
25
30
35
40
45
50
FREQUENCY (kHz)

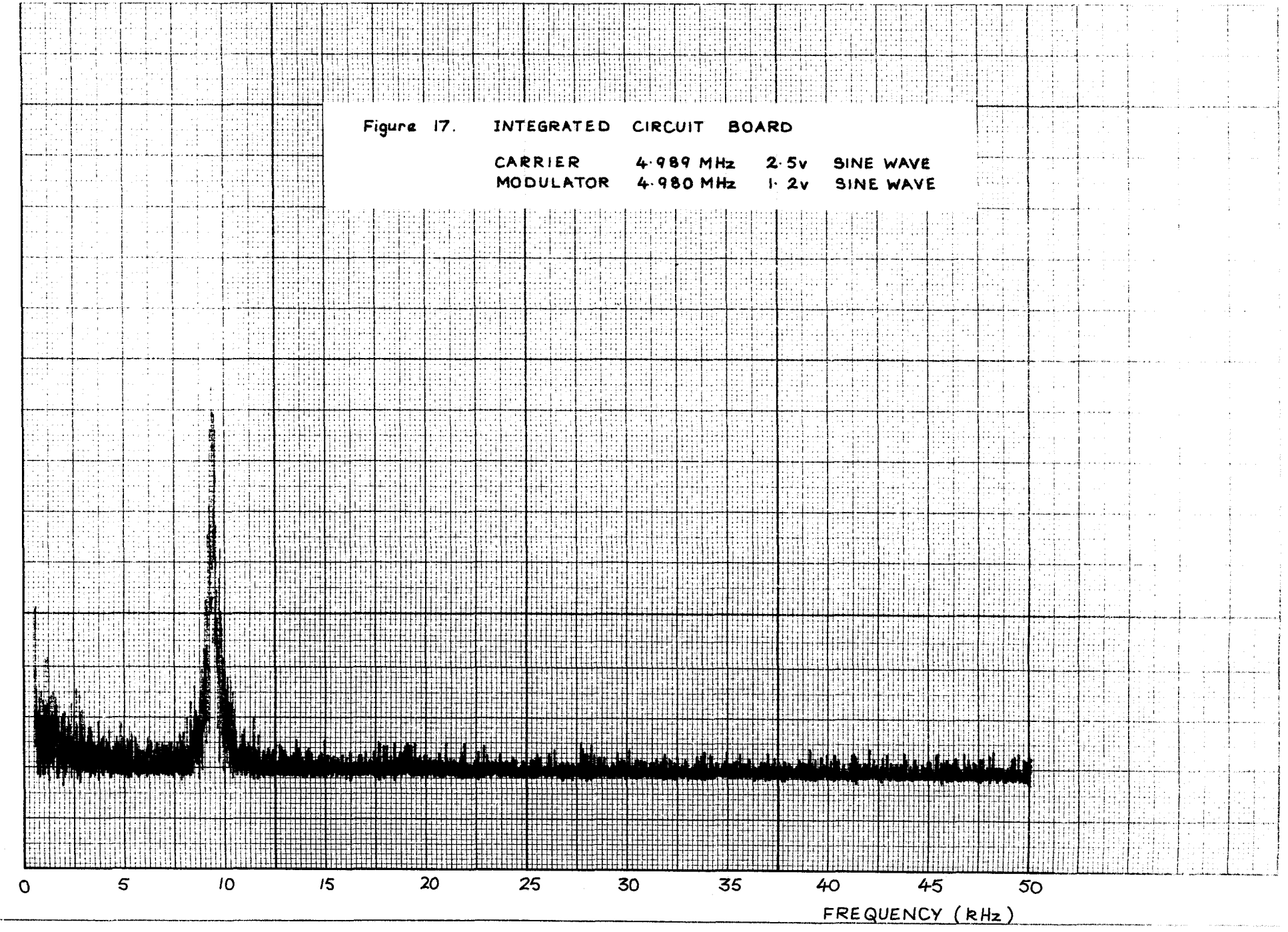
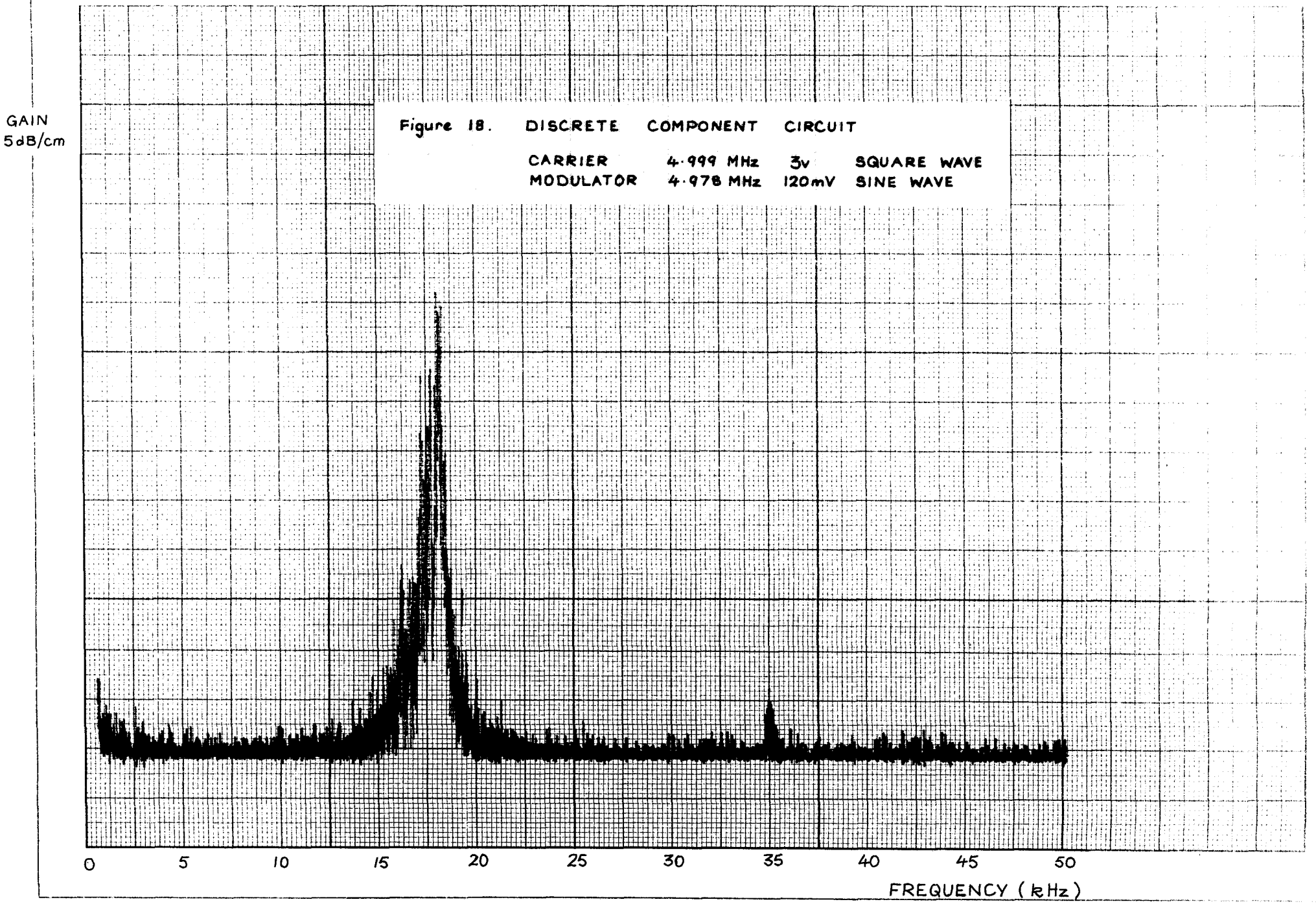
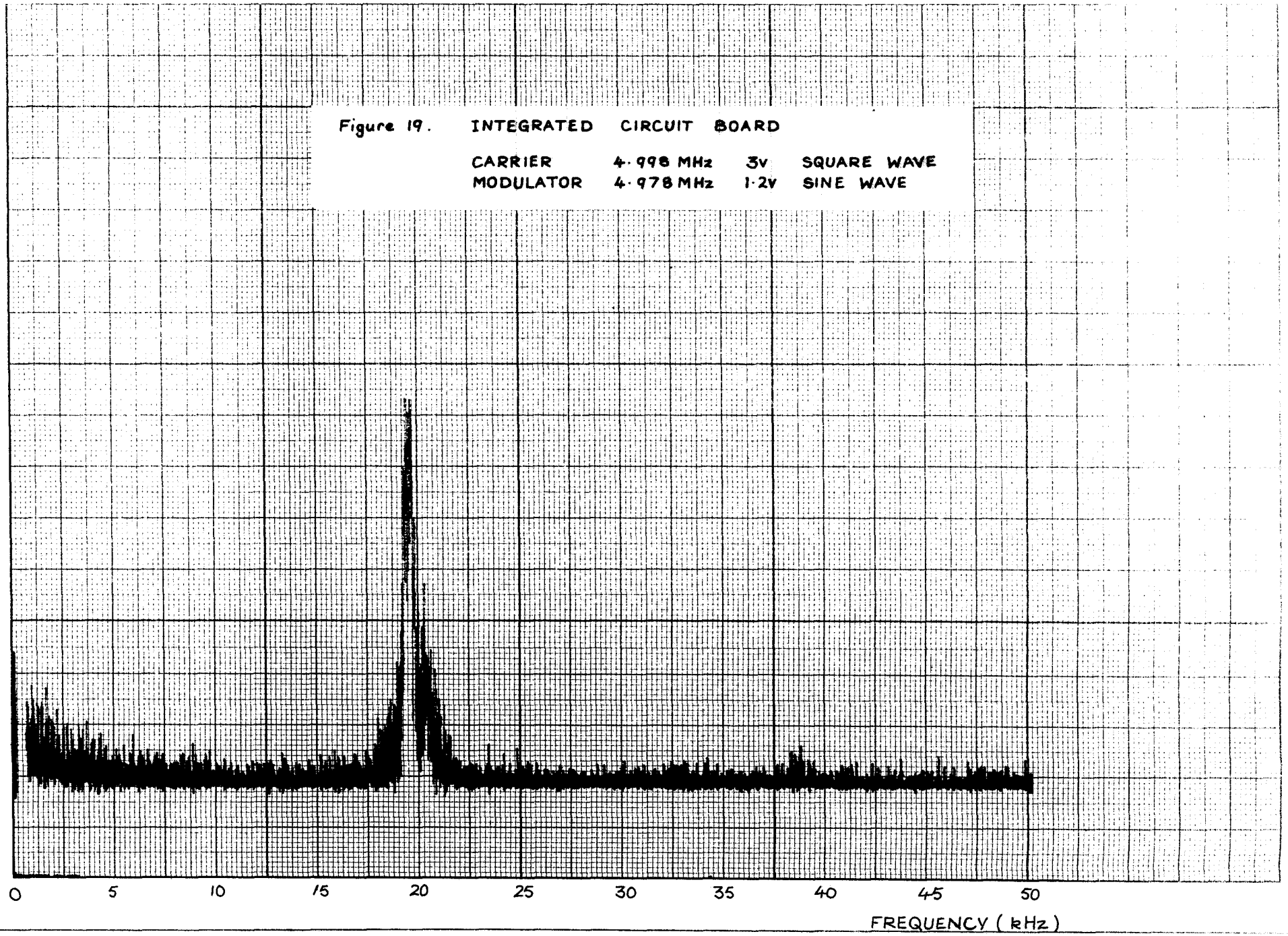


Figure 17. INTEGRATED CIRCUIT BOARD

CARRIER	4·989 MHz	2·5v	SINE WAVE
MODULATOR	4·980 MHz	1·2v	SINE WAVE


GAIN
5dB/cm
Figure 18. DISCRETE COMPONENT CIRCUIT
CARRIER 4·999 MHz 3v SQUARE WAVE
MODULATOR 4·978 MHz 120mV SINE WAVE
0
5
10
15
20
25
30
35
40
45
50
FREQUENCY (kHz)


GAIN
5dB/cm
Figure 19. INTEGRATED CIRCUIT BOARD
CARRIER 4·998 MHz 3v SQUARE WAVE
MODULATOR 4·978 MHz 1·2v SINE WAVE
0
5
10
15
20
25
30
35
40
45
50
FREQUENCY (kHz)

3.6 THE DUAL CHANNEL PROCESSOR

This is made up of two identical single channel circuits, the complete circuit diagram is shown overleaf in figure 20. The circuit also includes the transmitter blanking circuit and the sample and hold circuit as briefly described in 1.4. It is from this circuit that the single channel circuit was made in order to carry out the comparison tests.

Although the AD539 is a dual-channel device closer inspection of the manufacturers data reveals that it works by modulating one carrier signal with two different input signals. In the acoustic doppler there are two carrier signals in quadrature which have to be modulated by one input signal. Therefore instead of being able to use just one integrated circuit for both channels, two will be needed, each in a single channel configuration. There is also the important fact that the receiver signal will have to be further amplified in order to give a sufficient input level to the device.

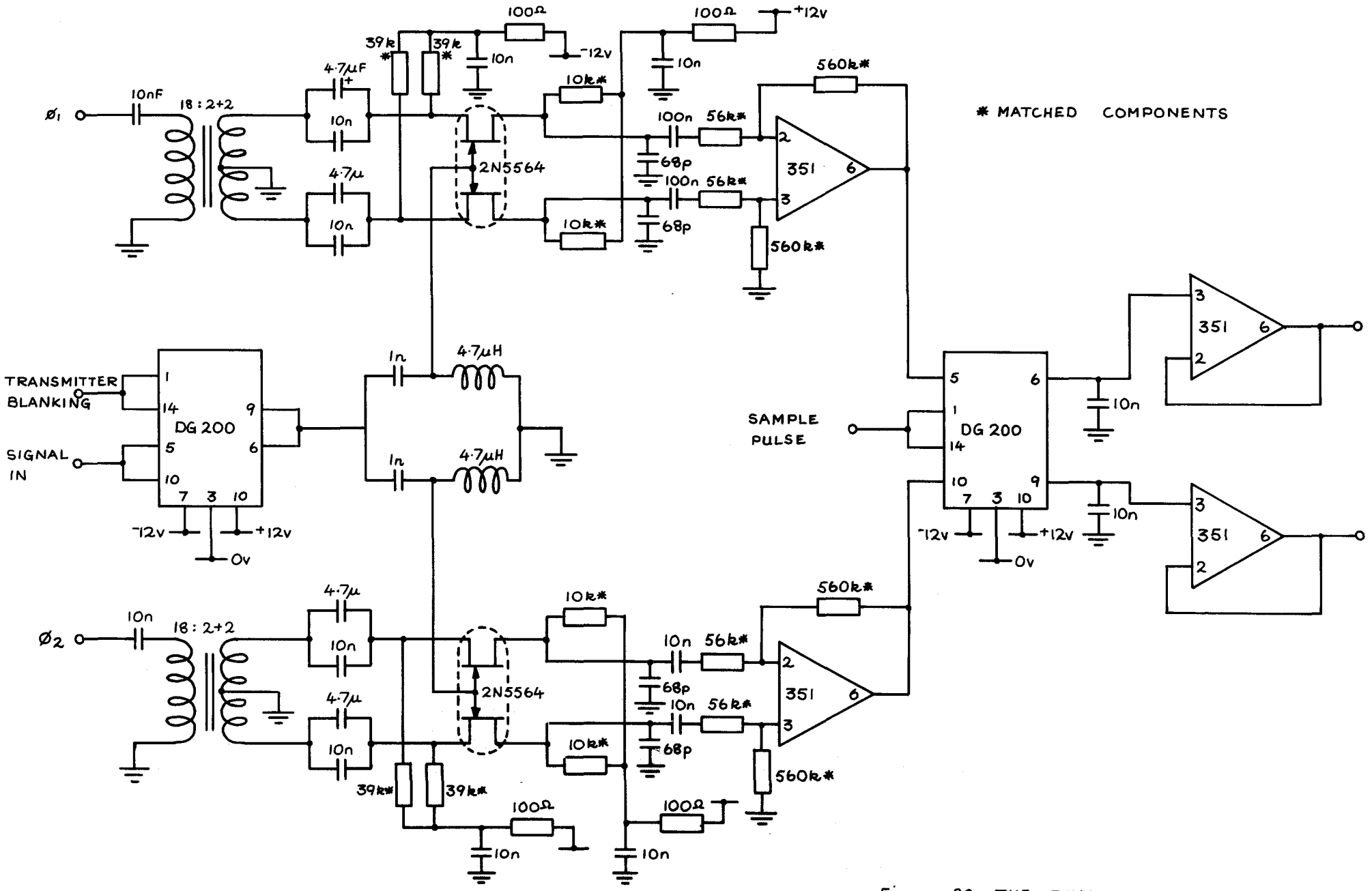


Figure 20. THE DUAL CHANNEL PROCESSOR

3.7 TESTING THE COMPLETE DOPPLER CURRENT METER

All the circuits which make up the complete instrument have been mounted in die-cast aluminium cases which are earthed. Eventually they will be redesigned to fit inside an underwater housing, but they are easier to work on in their present form. A photograph of the circuits set up in their cases is shown below:

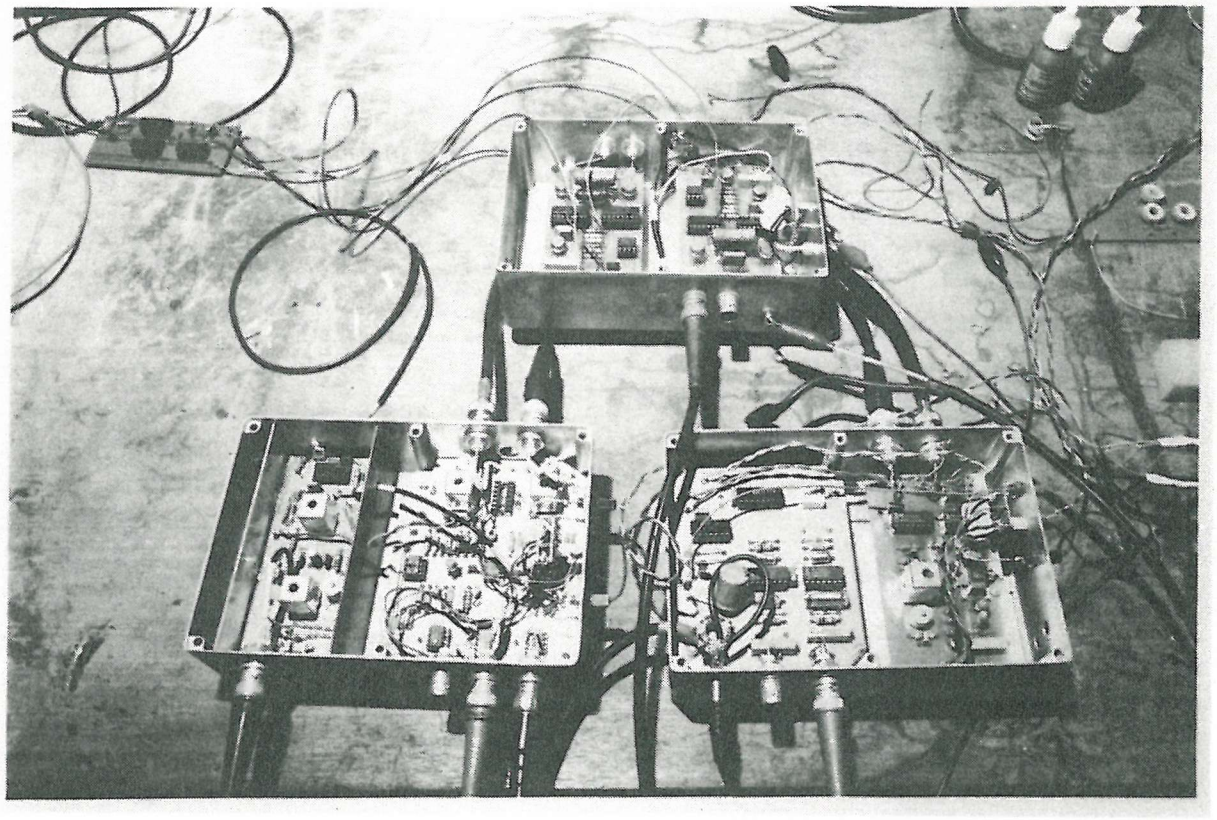


Figure 20: THE COMPLETE DOPPLER SYSTEM

The response of these circuits is tested by mounting the transducer in a flume with a circulating flow of water (see overleaf). Polystyrene granules are placed in the water as they are neutrally buoyant particles which will act as targets for the Doppler. The water is pumped around the flume by a propellor and the flow velocity is adjustable.

The outputs of the circuits may be displayed on an oscilloscope and the Doppler frequency is measured on a frequency counter. The change in the Doppler frequency can be seen easily when the velocity of the water flow

is altered. The frequency drops steadily when the pump is switched off and the water is left to slow down and stop.

This sort of test procedure has been invaluable in developing the instrument as it would be extremely difficult to simulate the waveforms which are produced by the transducer being in the water flow.

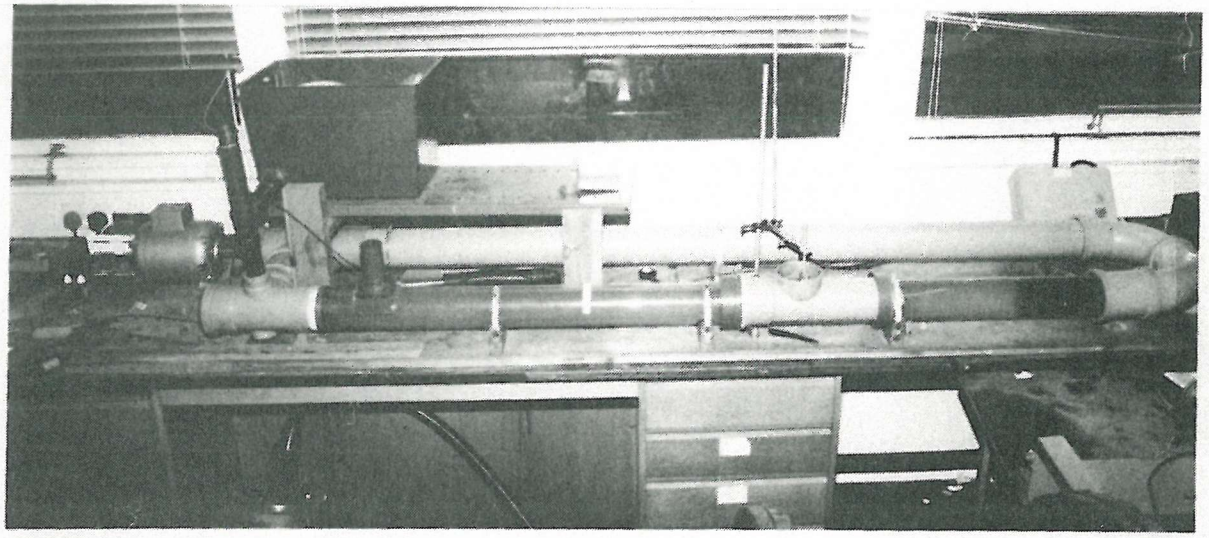


Figure 21: THE TESTING TANK

CONCLUSIONS

Throughout this project the aim has been to develop a dual channel circuit to replace the processor board based on discrete components. Although this has not been completed, enough information has been gained about the AD539 integrated circuit to realise that it could fairly easily be used in a circuit similar to the one tested.

The results of the comparison tests show that the integrated circuit will need a higher level of input signal, therefore the gain of the receiver will need to be improved. It is probable that his would be done anyway, including a swept gain system.

The frequency that the system uses has now been increased from 2 MHz to 5 MHz to give increased acousting scattering. This causes a major problem in re-designing the tuned circuits but will mean no changes using the integrated circuit as there are no frequency dependent components. This is obviously a great advantage over using discrete components and hopefully a new circuit will soon be in use.

REFERENCES

UNDERWATER ACOUSTICS - Leon W Camp

SENSORS FOR THE MEASUREMENT OF THE TRANSPORT OF SAND AS BEDLOAD - A P Salkield (Institute of Oceanographic Sciences Report No 73, 1978)

INFORMATION TRANSMISSION, MODULATION AND NOISE - Misha Schwartz

ELECTRONIC FUNDAMENTALS AND APPLICATIONS - John D Ryder

PRINTED CIRCUITS HANDBOOK - Clyde F Coombs

TRANSDUCERS FOR BIOMEDICAL MEASUREMENTS: PRINCIPLES AND APPLICATIONS - Richard S C Cobbold

ACKNOWLEDGEMENTS

I wish to express my appreciation for the help and advice provided by my colleagues at the Institute of Oceanographic Sciences and lecturers at the Somerset College of Art and Technology. In particular I would like to thank Dr A P Salkield of IOS.

APPENDIX 1

MAKING PRINTING CIRCUIT BOARDS

An important part of this project has been the design and production of suitable printed circuit boards (PCB's). When high frequencies and low signal levels are involved the layout of a PCB can be critical.

Low signal levels are extremely susceptable to noise and interference, therefore large ground planes are used and all power supplies are carefully decoupled with capacitors and transient suppressors (radio frequency chokes, RFC).

Problems can also arise due to stray capacitance between parallel conductors at high frequencies. It is therefore important to make sure that all conductors are as short as possible.

The stages in producing a circuit board are given below:

i) Designing the Artwork

The design of the PCB is made on drafting film using printed transfers and drafting tapes of suitable dimensions.

The size of the finished board is marked out and the positions of components are estimated to make sure that connections are short and do not cross. When there are large numbers of connections to be made it is advisable to sketch alternative layouts on graph paper before transferring the best design onto the final layout.

All of the boards for the doppler are double-sided with the top surface being used as a large ground plane. To achieve this there must be a small area around each connection free from copper. A mask to do this is made by placing a pad on each connection and then reversing this photographically.

ii) Transferring the Mask to Film

Although this is done commercially by using large, expensive reproduction cameras it can also be achieved with good accuracy and quality using a contact print method which is very simple.

In the dark room a piece of auto-positive film is placed on a clean glass plate. (Negative film for the top ground plane.) The drafting film mask is then positioned on top of the film and covered by another piece of plate glass. The film is then exposed through the mask for 4 minutes. After this the light is turned off and the film is taken out and developed. It is then fixed and dried ready to be used.

A separate mask is made for the top and bottom surface and these have to be put together matching all of the registers. They are stuck together to form an envelope.

iii) Preparing the Board

The type of board that is used is fibreglass which has been coated with a layer of copper and then a layer of etch resistant material is applied on the top. This material, although resistant to etching chemicals, is sensitive to ultra-voilet light.

A piece of the board is placed inside the mask envelope and each side is exposed to a concentrated source of ultra-violet light for three minutes. The board is then developed which removes the etch resist in the areas which were exposed.

The board is placed in an etching tank containing a concentrated acid solution which etches away the exposed copper leaving just the required conductors. Once etched the board is cleaned with acetone to remove the etch-resist and placed in a tinning tank. The copper is tinned so that it is easier to solder.

The finished board needs to be cut to size and drilled ready to be built.

The masks which were used to make the printed circuit boards for this project were photocopied and are included in this appendix.

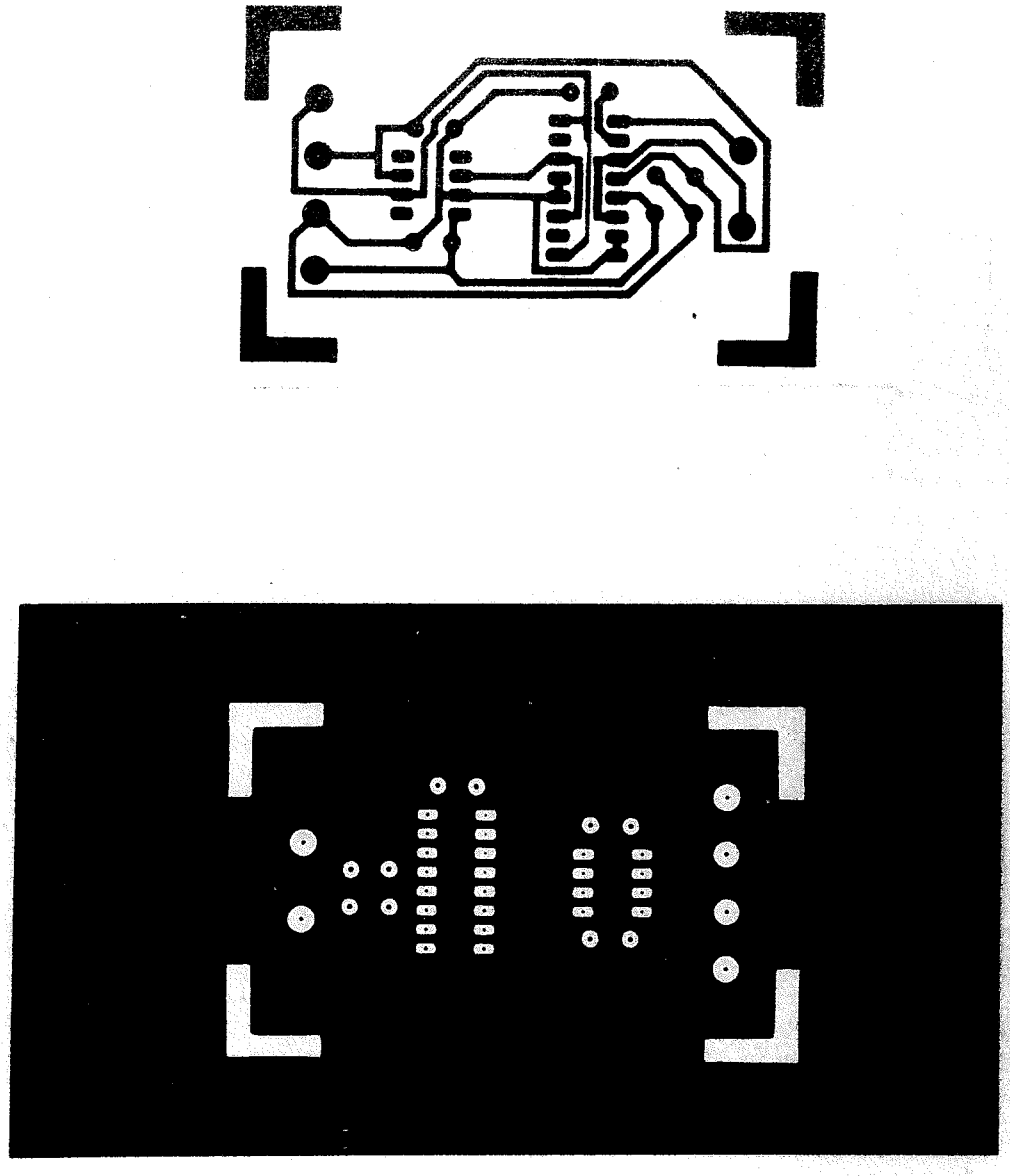


Figure 22. PCB MASK FOR THE INTEGRATED CIRCUIT WIDE BAND MULTIPLIER

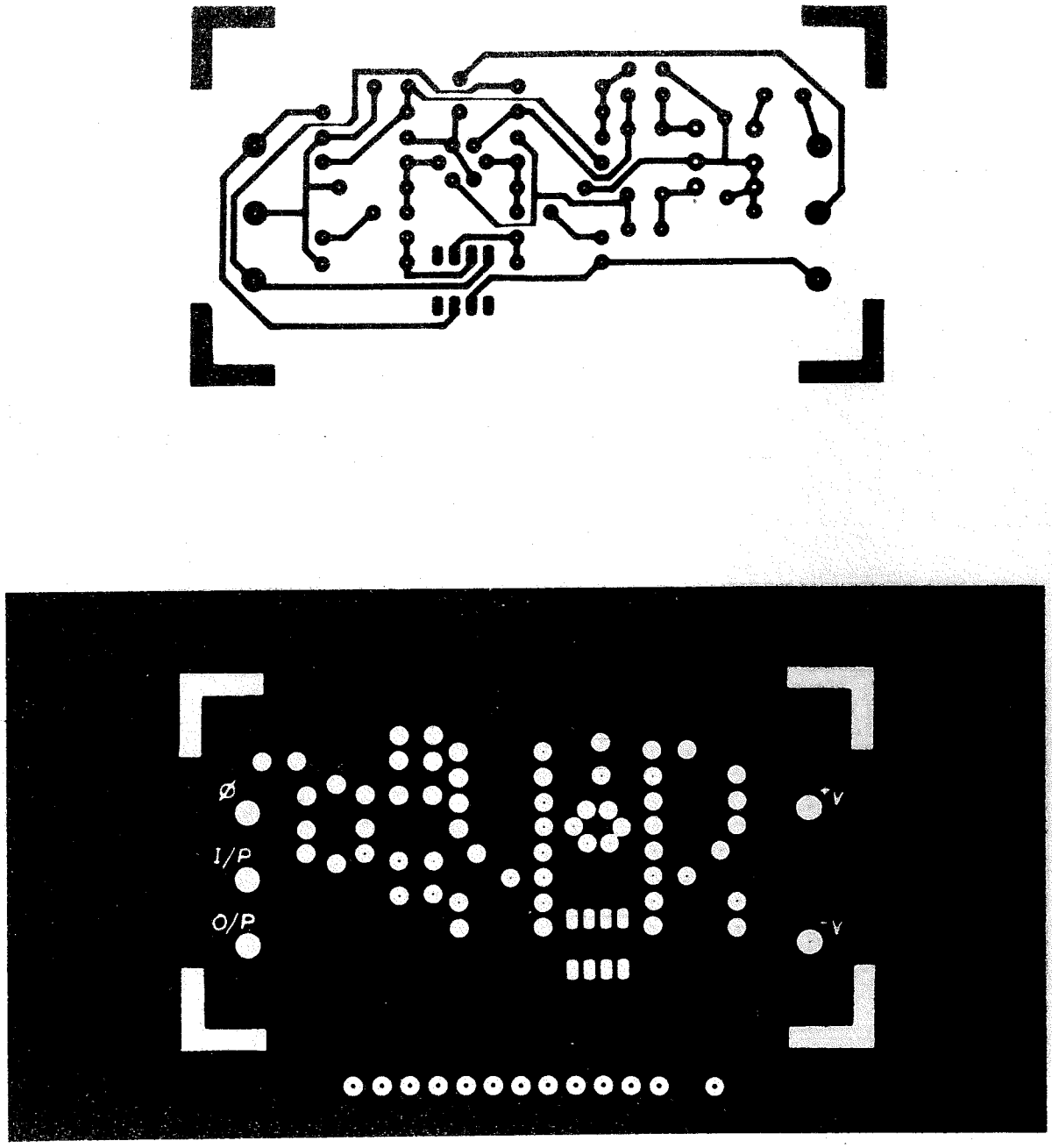


Figure 23. PCB MASK FOR THE DISCRETE COMPONENT CIRCUIT

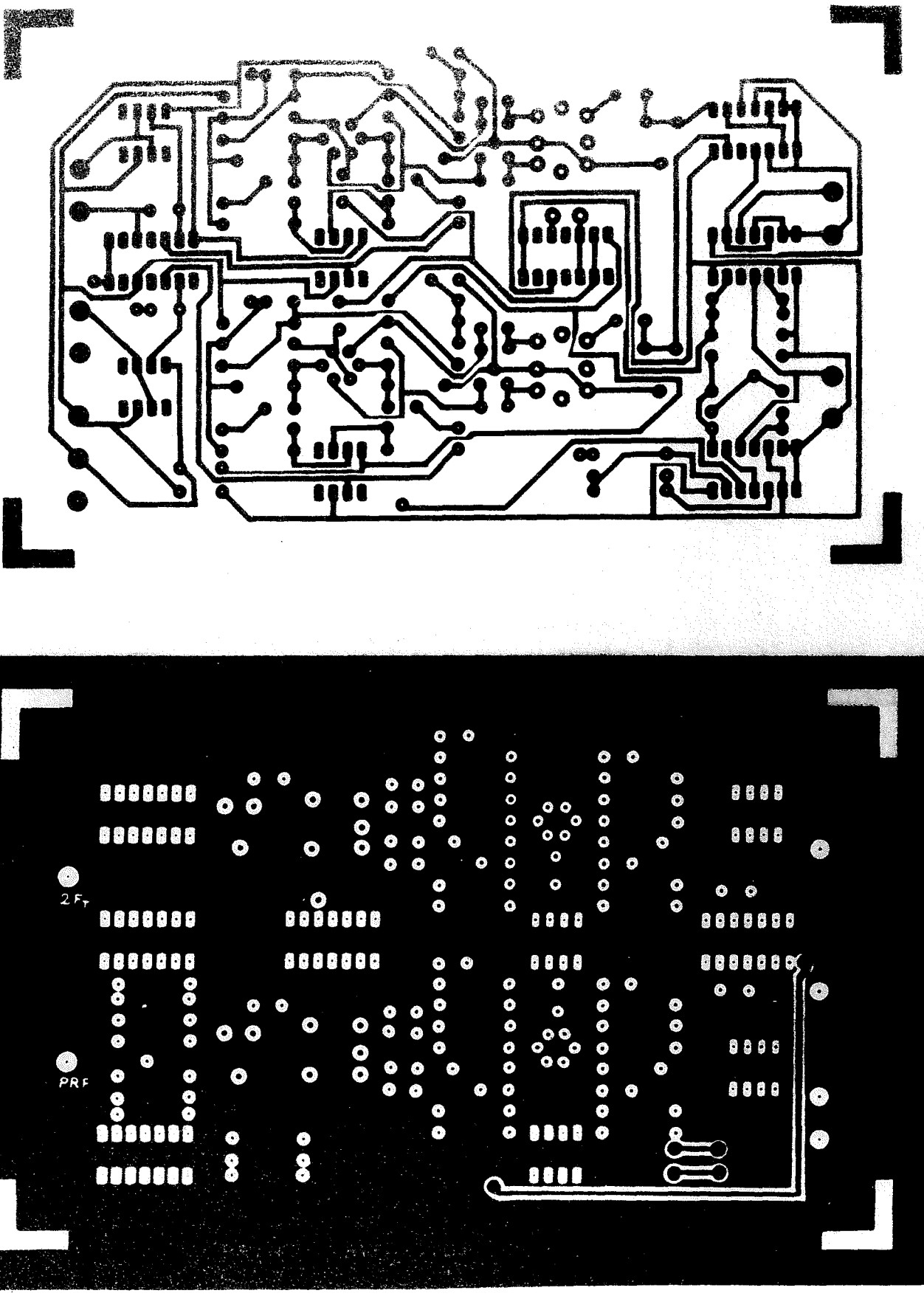


Figure 24. PCB MASK FOR THE DUAL CHANNEL DISCRETE COMPONENT CIRCUIT

APPENDIX 2

ANALOG DEVICES

Wideband Dual-Channel Log/Lin Multiplier/Divider

PRELIMINARY

AD539

FEATURES
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Two Quadrant Multiplier/Divider
Linear Control BW of 5MHz
Fully-Calibrated Multiplier/Divider
Wide-Range (>100dB Log Mode)

APPLICATIONS
Precise AGC and VCA Systems
Video Switching and Effects
Wide-Range VCOs and VCFs
High-Speed Analog Division
Logarithmic Gain/Loss Control
Square-Law Gain/Loss Control

PRODUCT DESCRIPTION

The AD539 is a low distortion analog multiplier with two wide band signal channels controlled by a common input for either linear or logarithmic gain control. It provides excellent ac characteristics up to and beyond video frequencies. The device has good static accuracy in computation applications; laser-trimming eliminates all offsets and a stable internal voltage reference determines scaling.

The 60MHz signal bandwidth of each current-mode output is relatively insensitive to gain. Low-impedance loads are needed for maximum bandwidth. This restricts output voltage to a few hundred millivolts. Using a suitable external op amp lowers the bandwidth to 15MHz but achieves the advantages of accurate signal multiplication and large output voltage.

The two channels may be used independently, with very low cross talk between channels, or in parallel, to double the output current. A differential configuration reduces distortion. Connecting the two channels in series achieves a gain/loss range of over 100dB with a square-law control characteristic.

The AD539 can be configured as a dual- or single-channel analog divider for wide band AGC applications and for voltage-controlled filters and oscillators.

Power dissipation is only 133mW with the recommended ±5 volt supplies. The AD539 is available in three versions with different accuracies and operating temperature ranges; the "J" and "K" are specified 0 to +70°C operation; the "S" is guaranteed over the military range of −55°C to +125°C. All versions are packaged in a 16-pin DIP.

OPERATIONAL DETAILS

The linear gain-control input (pin 1) accepts a voltage V_X of zero to +3V full scale (FS) relative to input common (pin 7). This input presents a purely resistive load of 500Ω (or a FS current input of 6mA). To stabilize the internal control amplifier a grounded compensation capacitor is required at pin 2. Its value determines the small-signal bandwidth and slew-time of the control system and to some extent the HF distortion and cross talk of the signal channels. Using the minimum recommended capacitance of 3000pF the bandwidth is typically 5MHz at $V_X = +1.5V$ (mid-scale). In the linear control mode the "dB" (logarithmic) inputs (pins 12 and 13) should be shorted and connected to a fixed bias (usually ground).

The "dB" inputs provide logarithmic control over a very large attenuation range for signal processing applications. The loss function is not exactly logarithmic, but at large attenuation the scaling is asymptotic to 3mV/dB at 25°C; it is not temperature stable. In this mode the linear control input will usually be grounded, but these inputs can be combined to achieve special control characteristics.

The signal inputs V_{Y1} and V_{Y2} (pins 3 and 6) accept ±2 volt full scale inputs and present an input impedance of about 400kΩ shunted by 3pF. Distortion at an input voltage of 1.5V rms and at full gain ($V_X = +3V$) is typically 0.04%. Phase stability over the signal window at the color sub-carrier frequency of 3.579MHz is within ±0.2° for $V_Y = -1V$ to +1V.

The outputs (pins 14 and 11) deliver a short-circuit current of nominally ±1mA FS and ±2.75mA peak, from a source resistance of 1.2kΩ. An external op amp connected as a current to voltage converter increases accuracy and provides larger output voltages. Two internal 6kΩ feedback resistors per channel allow for 1 volt scaling ($V_W = V_X \cdot V_Y$) or 2 volt scaling $\left(V_W = \frac{V_X \cdot V_Y}{2}\right)$.

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/842-1717 Mid-West 312/653-5000 Texas 214/231-5094

SPECIFICATIONS (typical @ $T_A = 25°C$, $V_S = \pm 5V$, unless otherwise specified)

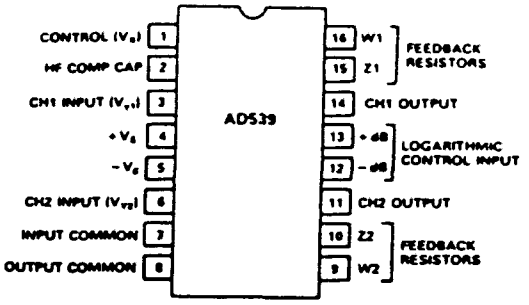
Parameter	Conditions	AD539JD	AD539KD	AD539SD
SIGNAL-CHANNEL DYNAMICS				
Minimal Configuration (Figure 1)				
Bandwidth, −3dB	$R_L = 50\Omega$	60MHz (30MHz min)	•	•
Maximum Output	$+0.1V < V_X < +3V$, V_Y ac = 1V rms	−10dBm	•	•
Feedthrough	$V_X = 0$, V_Y ac = 1.5V rms, f = 1MHz	−75dBm	•	•
	f = 20MHz	−55dBm	•	•
Phase Stability	f = 3.58MHz, $V_X = +3V$, V_Y ac = 100mV			
	$-1V < V_Y dc < +1V$	±0.2°	•	•
	$-2V < V_Y dc < +2V$	±0.5°		
Group Delay	$V_X = +3V$, V_Y ac = 1V rms, f = 1MHz	2ns	•	•
Standard Dual-Channel Multiplier (Figure 2)				
Bandwidth, −3dB	$+0.1V < V_X < +3V$, V_Y ac = 1V rms,	5MHz	•	•
Maximum Output	$V_X = +3V$, V_Y ac = 1.5V rms	4.5V rms	•	•
Feedthrough	$V_X = 0$, V_Y ac = 1.5V rms, f < 100kHz	<1mV rms	•	•
Crosstalk (CH1 to CH2)	V_{Y1} = 1V rms, $V_{Y2} = 0$			
	$V_X = +3V$, f < 100kHz	−40dB	•	•
THD + Noise	f = 10kHz			
	$V_X = +1V$, V_Y ac = 1V rms	0.02%	•	•
	$V_X = +3V$, V_Y ac = 1V rms	0.04%	•	•
Wide Band Single-Channel Multiplier (Figure 3)				
Bandwidth, −3dB	$+0.1V < V_X < +3V$, V_Y ac = 1V rms	15MHz	•	•
Maximum Output Feedthrough	$V_X = +3V$, V_Y ac = 1.5V rms	2.25V rms	•	•
	$V_X = 0$, V_Y ac = 1.5V rms, f = 3MHz	TBF, mV rms	•	•
CONTROL CHANNEL DYNAMICS				
(Figure 3)	C_C = 3300pF			
Bandwidth, −3dB	$V_X dc = +1.5V$, V_X ac = 100mV rms	5MHz	•	•
SIGNAL INPUTS, V_{Y1} & V_{Y2} (Pins 3 & 6)				
Nominal Full-Scale Input		±2V	•	•
Operational Range, Degraded Performance	$-V_S > 7.5V$	±4.2V min	±4.2V min	±4.2V min
Input Resistance		400kΩ	•	•
Bias Current		10μA (30μA max)	• (20μA max)	•
Offset Voltage		5mV (20mV max)	5mV (10mV max)	•
Stability Over Temperature (T_{MIN} to T_{MAX})		TBFmV	•	•
Power Supply Sensitivity		TBFmV/V	•	•
LINEAR CONTROL INPUT, V_X (Pin 1)				
Nominal Full-Scale Input		+3.0V	•	•
Operational Range, Degraded Performance		+3.2V min	•	•
Input Resistance[1]		500Ω	•	•
Offset Voltage		1mV (4mV max)	1mV (2mV max)	•
Stability Over Temperature (T_{MIN} to T_{MAX})		TBFmV	•	TBFmV max
Power Supply Sensitivity		TBFmV/V	•	•
Decibel Gain	(Figure 2)	$20\log_{10}(V_X)$	•	•
Absolute Gain Error	$V_X = 0.1V$ to $+3.0V$	0.1dB (0.5dB max)	0.1dB (0.2dB max)	•
LOGARITHMIC CONTROL INPUTS (Pins 12 & 13)[2]				
Asymptotic Sensitivity		0.33dB/mV	•	•
Temperature Sensitivity		0.03dB/°C	•	•
CURRENT OUTPUTS (Pins 11 & 14)[1]				
Full-Scale Output Current	$V_X = 5V$, $V_Y = \pm 2V$	±1mA	•	•
Peak Output Current	$V_X = \pm 3.4V$, $V_Y = \pm 5V$	±2.8mA (±2mA min)	±2mA min	±2mA min
Output Offset Current	$V_X = 0$, $V_Y = 0$	0.2μA (2μA max)	•	•
Output Resistance		1.2kΩ	•	•
Scaling Resistors	Z1, W1 to CH1 Output	6kΩ	•	•
	Z2, W2 to CH2 Output	6kΩ	•	•
VOLTAGE OUTPUTS, V_{W1} & V_{W2}[3]	(Figure 2)			
Multiplier Transfer Function,				
Either Channel		$V_W = +V_X \cdot V_Y / V_Q$	•	•
Multiplier Scaling Voltage, V_Q		1.00V	•	•
Accuracy		0.5% (2% max)	0.5% (1% max)	•
Temperature Sensitivity (T_{MIN} to T_{MAX})		TBFppm/°C	•	•
Power Supply Sensitivity		TBF%/V	•	•
Total Multiplication Error	$V_X <= +3V$, $-2V < V_Y < 2V$	0.6% FSR (2.5% max)	0.6% FSR (1.5% max)	•
Control Feedthrough	$V_X = 0$ to $+3V$, $V_Y = 0$	15mV (60mV max)	15mV (30mV max)	•
POWER SUPPLIES				
Operational Range		±4.5V to ±16.5V	•	•
Current Consumption[4]	$+V_S$	8.5mA	•	•
	$-V_S$	18.5mA	•	•
PRICES				
(1–24)				
(25–99)				
(100+)				

NOTES
[1]Resistance value and absolute current outputs subject to 20% tolerance.
[2]Read Application Note for explanation of decibel scaling sensitivity.
[3]Spec assumes the external op-amp is trimmed for negligible input offset.
[4]Specifications same as AD539JD.
Specification subject to change without notice.

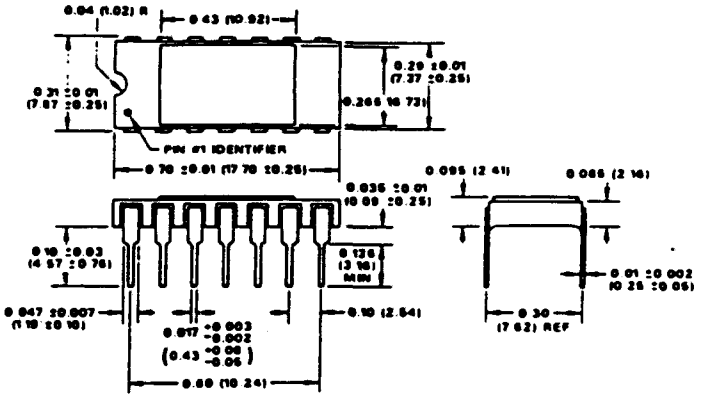
PRELIMINARY

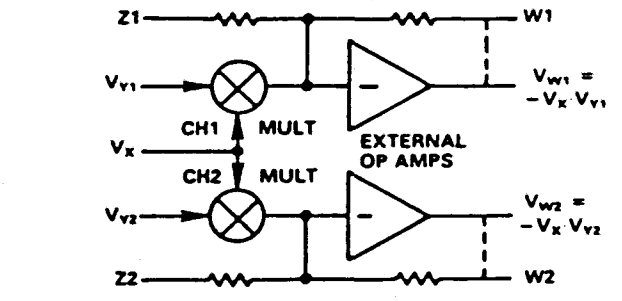
PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm)



TO-116





AD539 Basic Functional Scheme

CIRCUIT DESCRIPTION

Figure 1 is a simplified schematic of the AD539. Transistors Q1-Q6 were designed for low distortion, high bandwidth and low signal feedthrough. The band-gap reference produces a stable reference current of 1.375mA. This current flows entirely in Q1 when the control input (V_X, on pin 1) is zero. As the control input is raised, a proportion of I_{REF} flows in Q2. At full scale control voltage (V_X = +3V) about 0.87 I_{REF} (1.2mA) is steered into Q2 due to the 1:3 emitter area ratio of Q1/Q2. The other controlled cascode pairs (Q4/Q3 and Q5/Q6) split their emitter currents in the same proportion.

The dc bias current of pairs Q4/Q3 and Q5/Q6 is 2 I_{REF} (2.75mA). At full scale signal voltage (V_Y = ±2V) the transconductance stages produce a signal current of ±1.15mA. Thus, when both V_X and V_Y are at their full-scale values, the collector current of either Q3 or Q6 contains a bias component of 0.87 × 2.75mA, or 2.4mA, and a signal component of 0.87 × ±1.15mA, or ±1mA. The bias component is absorbed by the 1.25k resistors, also connected to V_X. The signal components are available for direct use into external load resistors (in which case, scaling is not precise) or can be forced into either or both of the 6kΩ feedback resistors associated with each channel by the use of an external op amp. In the latter case, scaling is accurate, since it involves only the *ratio* of thin-film resistors and the reference *voltage* generated by the trimmed band-gap circuit.

The dB inputs may be used to add or subtract a voltage into the control system. Because of basic properties of bipolar transistors, this voltage will alter the proportion of signal delivered to the output according to an approximately logarithmic function, becoming more exactly logarithmic as the attenuation is increased (pin 13 more negative than @ pin 12) with an asymptotic scale of 3mV/dB. Note that the bias system is only balanced when the dB nodes are at the same potential; consequently, the logarithmic node results in a variable dc level at the outputs unless a single-channel differential configuration is used (see Figure 8a).

GENERAL PRECAUTIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high-quality ground plane should be used with the device either soldered directly into the board, or mounted in a low-profile socket. Pins 12 and 13 (unless required for logarithmic control) should be

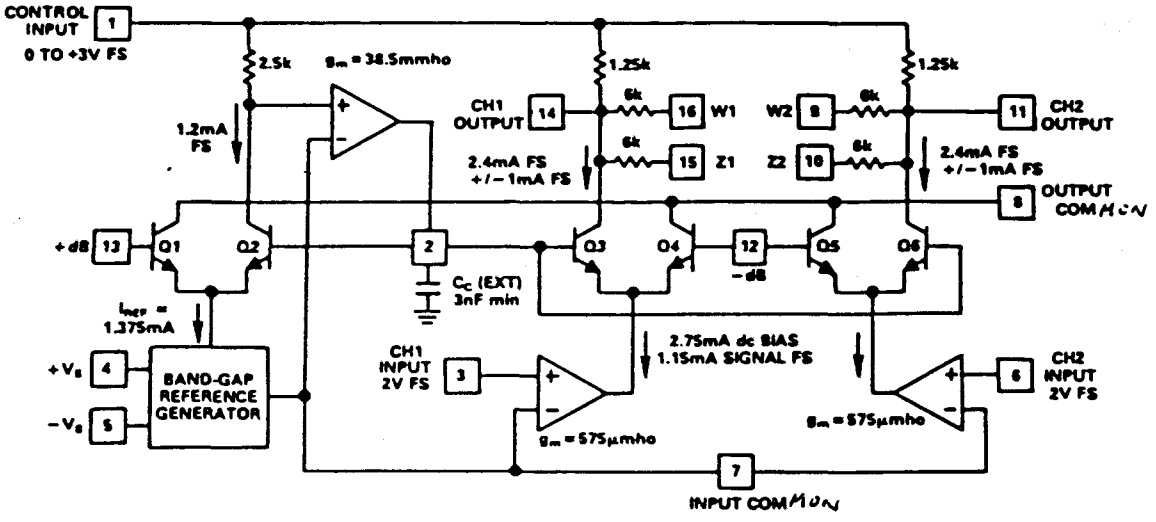


Figure 1. Simplified Schematic of AD539 Multiplier

connected directly to ground; even very small residual voltages between these two pins can adversely affect performance. Power supply decoupling ceramic capacitors of 0.47μF should be connected from pins 4 and 5 to the ground plane. In applications using external high speed op amps, their supplies should be separately decoupled, and appropriate compensation capacitors used. (In the figures, these capacitors are omitted for clarity.)

The control amplifier compensation capacitor at pin 2 should also be connected directly to the ground plane. Unless maximum control bandwidth is esssential, this capacitor should be as large as possible, to minimize distortion and cross talk at high frequencies and to improve the phase response. The control bandwidth scales inversely with this capacitance. For example, using a 0.01μF capacitor, bandwidth is typically 2MHz at $V_X = 1.7V$; with 0.1μF it is reduced to 200kHz. Little benefit accrues for compensation capacitors above 0.1μF. The control bandwidth is also a function of V_X, decreasing as V_X approaches its limiting values of 0 and +3.2V.

V_X should not be outside of this operational range. The ac gain is zero for $V_X < 0$, but there remains a feedforward path (see Figure 1) to the output causing control feedthrough. Above $V_X = +3.2V$, the ac gain does not increase beyond its maximum value, but once again the excess control bias appears as an unwanted output. Apart from the anomalous output behavior in these forbidden regions, the control system will also require considerable time to recover from such overload.

The power supplies to the AD539 can be as low as ±4.5V and as high as ±16.5V. The maximum allowable value of the signal inputs, V_{Y1} and V_{Y2}, is approximately 0.5V above $+V_S$; the minimum value is 2.5V below $-V_S$. To accommodate peak signal input of ±5V requires $V_S = +4.5V$ min, $V_S = -7.5V$ min. While there is no advantage in raising supplies above these values, it may often be convenient to use the same supplies for the op amps. The AD539 is able to tolerate the excess voltage with only a slight effect on accuracy. Dissipation at ±16.5V is about 450mW, so some form of heat-sink is advisable with high supply voltages.

LINEAR MULTIPLIER MODES

Standard Dual-Channel Multiplier

Figure 2 shows the connections for a fully-calibrated two-channel multiplier. Each channel generates an output

$$V_W = -V_X \cdot V_Y$$

where inputs and output are in volts. At the nominal full-scale inputs $V_X = +3V$ and $V_Y = \pm 2V$ the full-scale output is ±6V. The peak guaranteed output ($V_X = +3.2V$, $V_Y = \pm 4.2V$) is ±13.4V assuming that suitable supplies are used for the op amps.

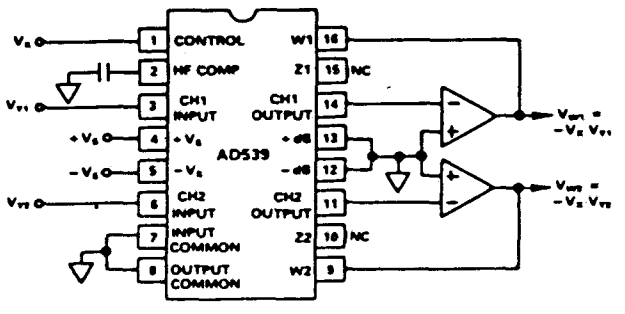


Figure 2. Standard Dual-Channel Multiplier. The Type of Op Amps, Their Supply Voltages and Any Additional HF Compensation Depends on Application Requirements

Viewed as a voltage controlled amplifier, this configuration provides a gain of

$$G = 20\log_{10}(V_X)$$

or slightly over 10dB at $V_X = +3.2V$, 0dB at $V_X = +1V$, −20dB at $V_X = +0.1V$, and so on. At small values of V_X, the control offset voltage will degrade accuracy of attenuation. For example, a 1mV offset will cause the attenuation at $V_X = 10mV$ to range from −40.9dB to −39.2dB. Figure 3 shows the guaranteed gain error boundaries for all configurations using the internal applications resistors.

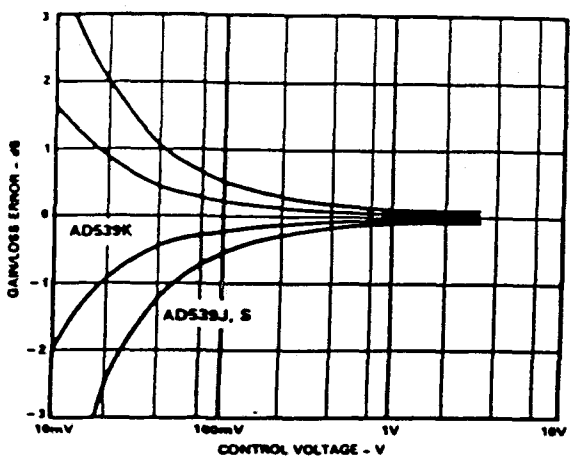


Figure 3. Maximum ac Gain Error Boundaries

Figure 4 shows the frequency response using AD509 op amps with no external compensation added, a 0.01μF compensation capacitor on the AD539, $V_Y = 1V$ rms and $V_S = \pm 12V$. The −3dB bandwidth is over 5MHz for $0.01V \le V_X \le 3.16V$. The curve at $V_X = 0$ shows the HF feedthrough at nominally zero gain.

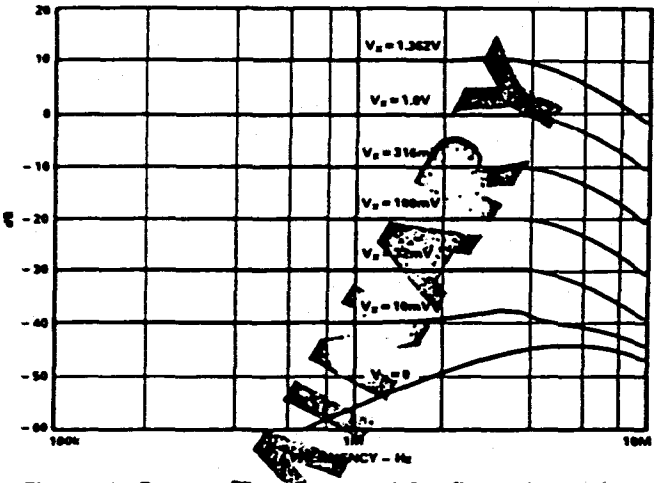


Figure 4. Response, Standard Configuration Using AD509 Output Op Amp

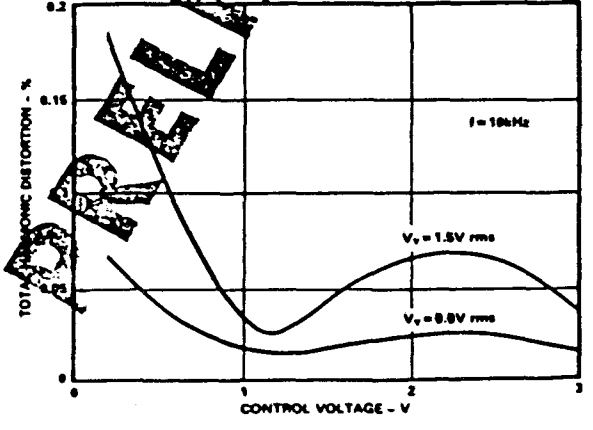


Figure 5. Total Harmonic Distortion vs. Control Voltage

Distortion is a function of the signal level (V_Y), the control voltage (V_X) and frequency. Figure 5 shows typical results at 10kHz as a function of V_X.

The "Z" and "W" pins provide essentially identical 6kΩ resistors for gain-setting purposes. In this case, the "Z" pins may be used as additional calibrated summing inputs, where

$$V_W = -(V_X \cdot V_Y + V_Z)$$

Using just the "W" pins as shown, the closed-loop gain of the op-amps is 5; when both "Z" and "W" pins are used it is 10. If desired, both resistors may be paralleled for feedback purposes to provide 2V scaling, that is

$$V_W = -V_X \cdot V_Y/2$$

With op-amps having provision for external HF compensation and a high unity-gain bandwidth (e.g. the AD518) this configuration can offer higher bandwidth at the expense of gain (4dB max) and output (±7.5V max).

APPLICATIONS

Wide Band Single-Channel Multiplier

Connecting both signal channels in parallel increases the full scale output current to ±2mA by reducing the feedback resistance to 3kΩ. Bandwidth is greater than 12MHz in this configuration with the ADLH0032 output op amp. High frequency compensation for the ADLH0032 and supply decoupling are omitted in Figure 6a for clarity. Choose the amplifier compensation capacitor to optimize the HF response for the specific application.

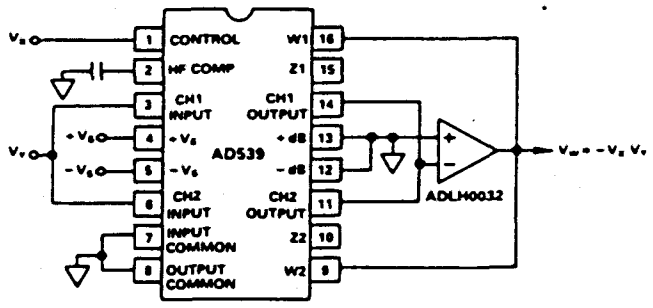


Figure 6a. Wide Band Single-Channel Multiplier

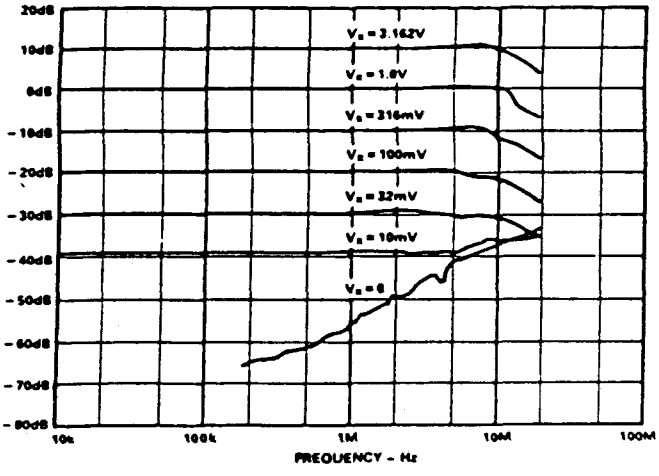


Figure 6b. Wide Band Single-Channel Gain vs. Frequency

In some applications it may be desirable to reduce the feedback and resistance further by shunting Z1 and Z2 with W1 and W2 resulting in a scaling voltage of 2 volts and a feedback resistance

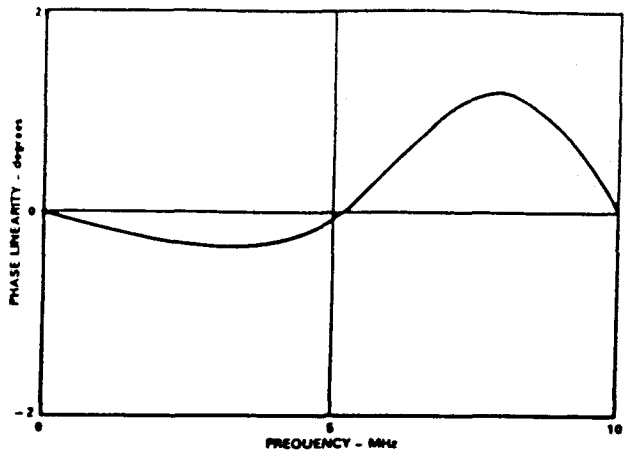


Figure 6c. Wide Band Single-Channel Multiplier Phase Linearity

of only 1.5kΩ. The peak output is reduced to ±6.7 volts. Bandwidth increases slightly to over 15MHz.

Minimal Single-Channel Multiplier

The maximum bandwidth is achieved using low-value (50Ω – 100Ω) load resistors at the signal outputs. Figure 7a shows the minimal configuration. Both channels operate in parallel, and the effective scaling voltage is approximately 60V for $R_L = 50\Omega$, 40V for $R_L = 75\Omega$ and 30V for $R_L = 100\Omega$. Figure 7b shows the HF gain response for $R_L = 50\Omega$ for $V_Y = 1.5V$ rms and control voltages from 10mV to 3.162V. Using $R_L = 75\Omega$, the peak load power is approximately 0dBm.

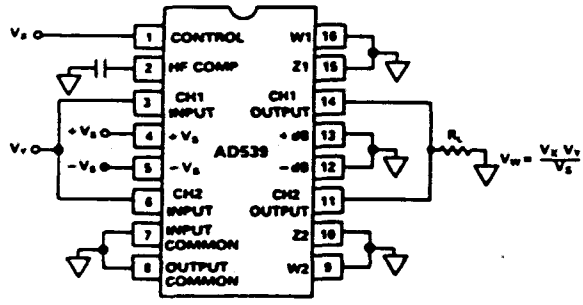


Figure 7a. Minimal Single-Channel Multiplier

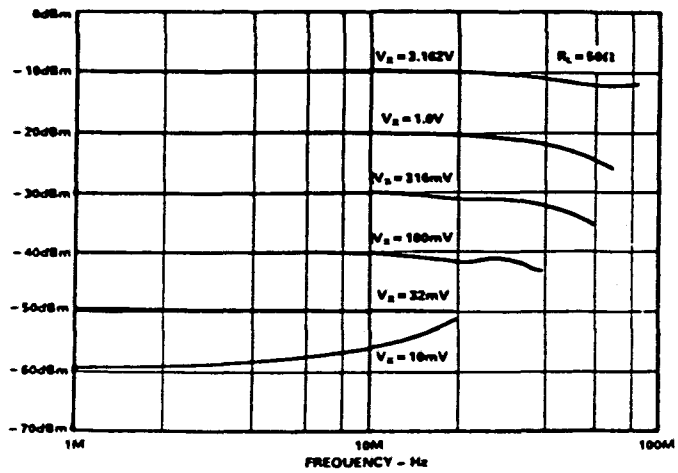


Figure 7b. HF Response in Minimal Configuration

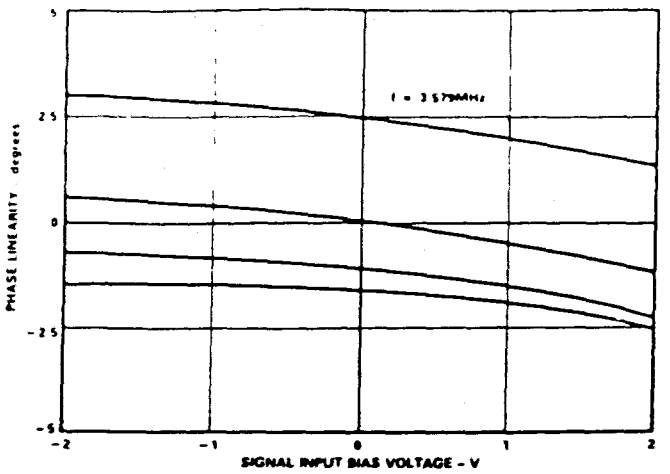


Figure 7c. Phase Stability Vs. Signal Voltage

The phase stability versus signal voltage at the color sub-carrier frequency of 3.579MHz is shown in Figure 7c. This is often called "differential phase linearity." The phase-stability for the AD539 is specified for the minimal configuration because even high quality op amps cause some degradation. Over the full specified signal window of $V_Y = \pm 2V$, at FS gain ($V_X = +3V$), the phase varies only $\pm 0.5°$. For reduced signal ranges, for example, $V_Y = -1V$ to 0, the phase variation can be as small as $\pm 0.1°$. At lower values of control voltage the phase stability worsens; however, in video switching applications a decrease in phase stability is tolerable, since the output is also greatly attenuated.

Differential-Mode Multiplier

The differential-mode multiplier configuration converts a differential signal to single-sided form, thus rejecting a common-mode signal at the input. This configuration, as shown in Figure 8a, behaves as a wide band instrumentation amplifier with voltage controlled gain.

Resistors R1 and R2, in this differential-mode, reduce multiplier distortion to a minimum level. Figure 8b shows typical results with an ADLH0032 op amp for wide bandwidth. Note the improvement in distortion compared to the standard configuration (Figure 5).

Connecting Z1 and Z2 to the control input reduces the risk of saturation at high signal levels by increasing the bias voltage at the outputs. Omit resistors R1 and R2 in applications that require protection from output saturation.

The differential-mode configuration also reduces transient feedthrough in the control channel. A spurious response can occur with the AD539 wired in the standard configuration because the fast rising control input reaches the output (via the 1.25kΩ resistors, Figure 1) before the signal input (that must wait for the control amplifier to settle). This effect is shown in Figure 8c with one channel of the AD539 driving a 50Ω load. Figure 8d shows the improvement using a differential oscilloscope on both outputs, each terminated in 50Ω, with only channel 1 receiving an input.

Cascaded Channels

The two signal channels of the AD539 can be cascaded to achieve a wide gain/loss range with a square-law control characteristic. Figure 9a shows typical connections and Figure 9b is the HF response. The maximum gain is now 20dB, maximum loss with reasonably well-controlled accuracy is 80dB. Bandwidth from −40dB to +20dB is approximately 5MHz.

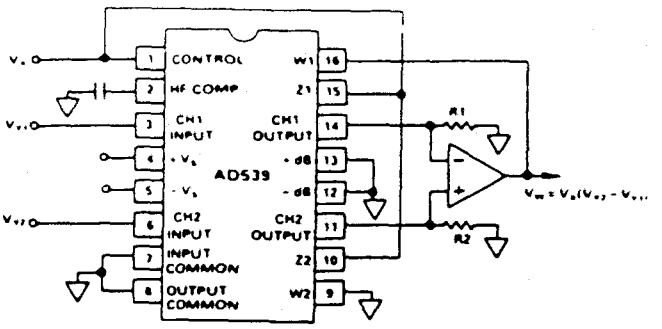


Figure 8a. Differential-Mode Multiplier

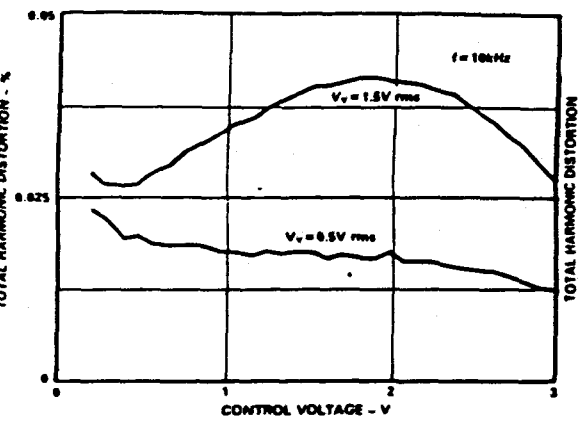


Figure 8b. Differential Distortion Characteristics

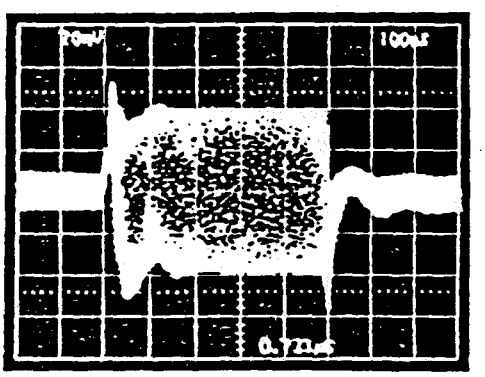


Figure 8c. Transient Feedthrough for Standard Configuration

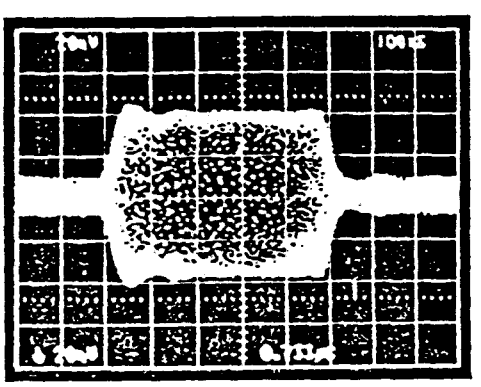


Figure 8d. Transient Feedthrough for Differential-Mode Configuration

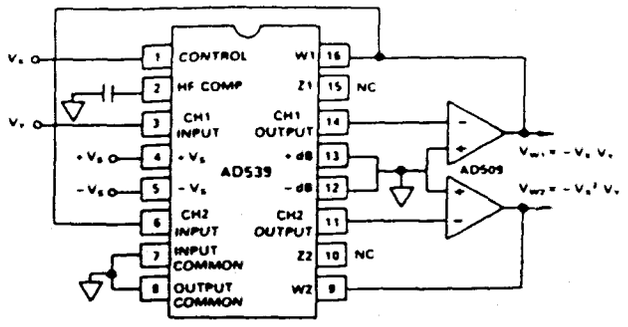


Figure 9a. Square-Law, Voltage-Controlled Amplifier

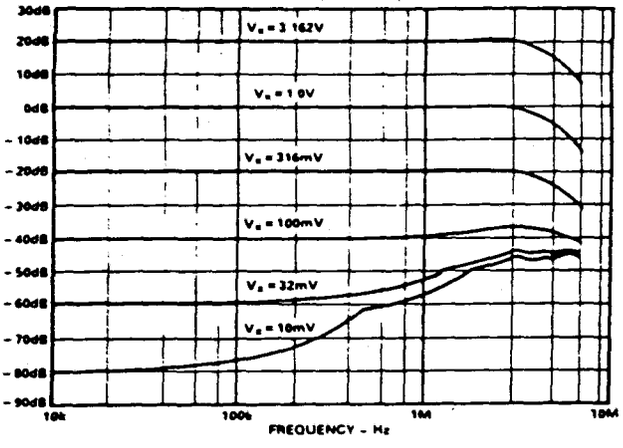


Figure 9b. HF Response of Square-Law, Voltage-Controlled Amplifier

Linear Division

The AD539 provides excellent operation as a two-quadrant analog divider in wide band applications, with the advantage of dual-channel operation. Figure 10 shows the standard connections for division with a 1V scaling voltage. The maximum input (V_W) can be a high as ±13.4V, but the output is limited by the V_Y signal range of the AD539 to ±2V FS, ±4.2V pk. This limitation can be overcome using attenuators between the op amp output and the AD539 inputs.

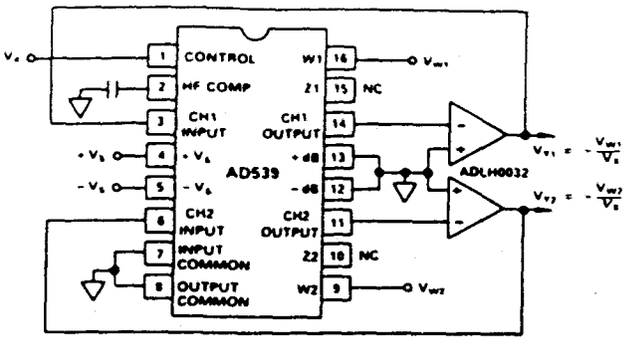


Figure 10. Standard Dual-Channel Divider

Figure 11 shows the control input attenuated, resulting in an overall scaling voltage of 10V. Bandwidth of this scheme using AD507 op amps is typically 7.5MHz for V_X = +10V, 1.5MHz for V_X = +1V and 125kHz with V_X = 100mV (gain of 100). This compares very favorably with the AD535 divider which has a bandwidth of 10kHz for a denominator input of 100mV.

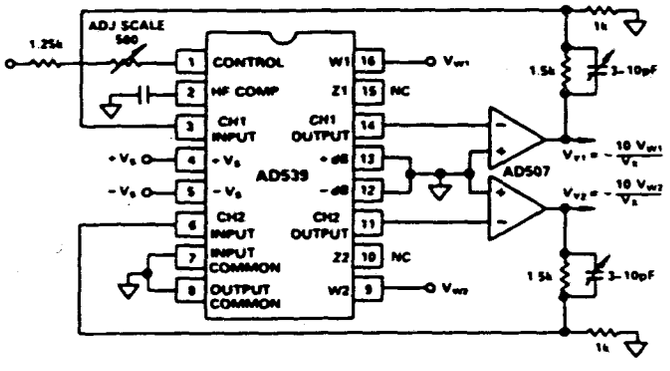


Figure 11. Dual-Channel Divider with 10V Scaling

FURTHER APPLICATIONS

Many more applications, including an extensive discussion of the logarithmic gain modes, will be found in the application note "Application of the AD539 Wide Band Multiplier". High speed applications using very fast output op amps are also discussed in this application note.