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AN AUTOMATIC ZERO-LEVEL SETTING CIRCUIT

A part of the electronic model
for tides and storm surges

S. Ishiguro

1982

NATURAL ENVIRONMENT RESEARCH COUNCIL

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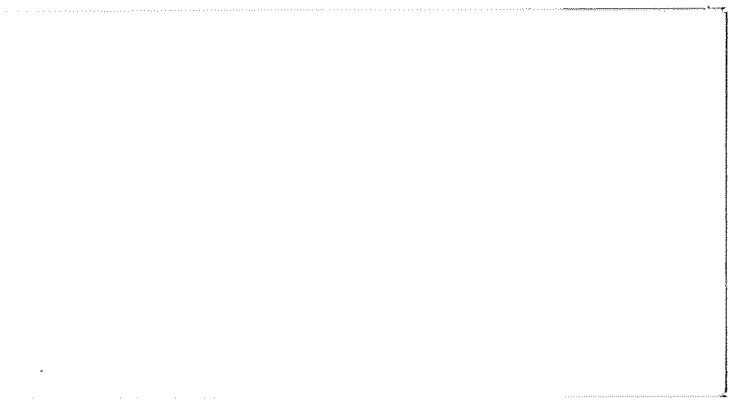

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CONTENTS

ABSTRACT

A circuit which separates an arbitrary-waveform voltage from an arbitrary dc level has been described. This circuit contributed significantly to reducing the time of processing the data of responses of sea level to external forces. The circuit will have general applications.

1. INTRODUCTION

'Electronic Model' is a system of simulating tides and storm surges for oceanography. Operation of the system includes obtaining a response (e.g. sea level) to an external force (e.g. the stress of a wind on the sea surface). In the main computing network of the system, the response is represented by an analogue voltage which is superimposed on a dc voltage. Due to an instrumental reason, the dc voltage varies from grid to grid in the network. Therefore, the zero-level of the response has to be determined individually. This paper describes a circuit which determines the zero level automatically. This increases the efficiency of operation when a large number of responses are processed.

2. PRINCIPLE

Fig. 1 shows the principle of the operation which satisfies the conditions described in the introduction. A shows a response voltage, e(t), superimposed on an arbitrary dc voltage, E_a. T_o is a period from the start of the operation to the start of the external force. The response is obviously zero during T_o. E_a can be sampled in this period, and held until the operation is completed, as shown in B. The response shown in C can be obtained by subtracting B from A.

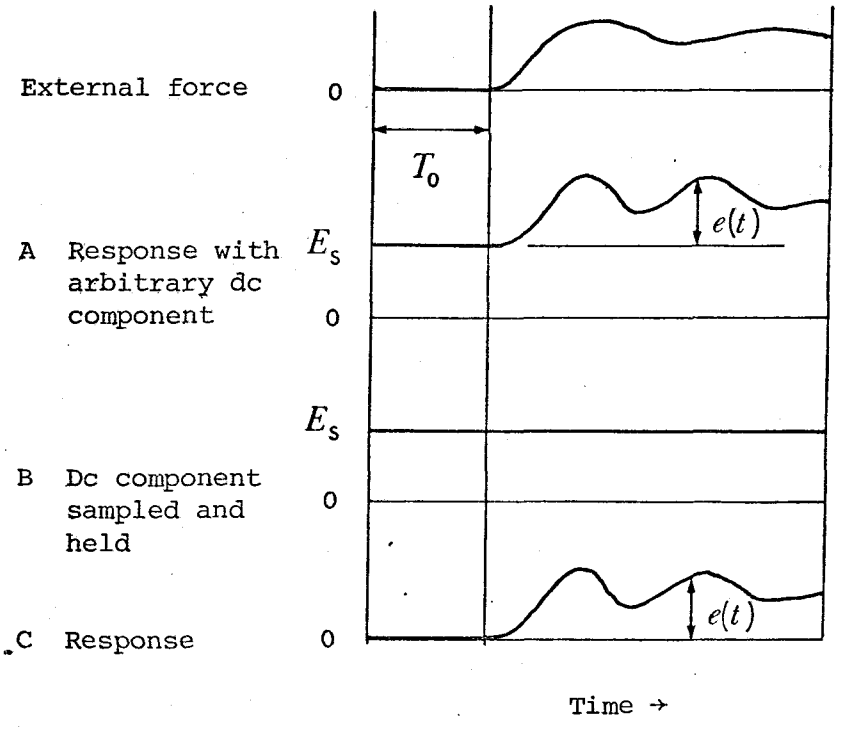


Fig. 1 Principle of operation

3. DESIGN OF THE CIRCUIT

The circuit is described here in two parts:

3.1 Main circuit

Fig. 2 shows circuit BD50 which has been based on the principle described in Chapter 1. 741(1) is a voltage follower to which a voltage representing a 'response with a dc component' (A in Fig. 1) enters. This output is divided into two parts. The first part enters into a sample-and-hold circuit, LF398. This voltage is sampled only when its pin 8 is logically high (+5V), and held for a short period. C1 is the holding capacitor. VR2 is for adjusting a dc offset. C2 and VR1 are for adjusting an ac offset, and require a voltage having a reversed polarity to that of the logic voltage supplied to pin 8.

The second part of the output of 741(1), A, and the output of LF398, B, enter the 741(2) so that its output, C, is equal to A - B. C is scaled by a step-potentiometer and an output amplifier, 741S.

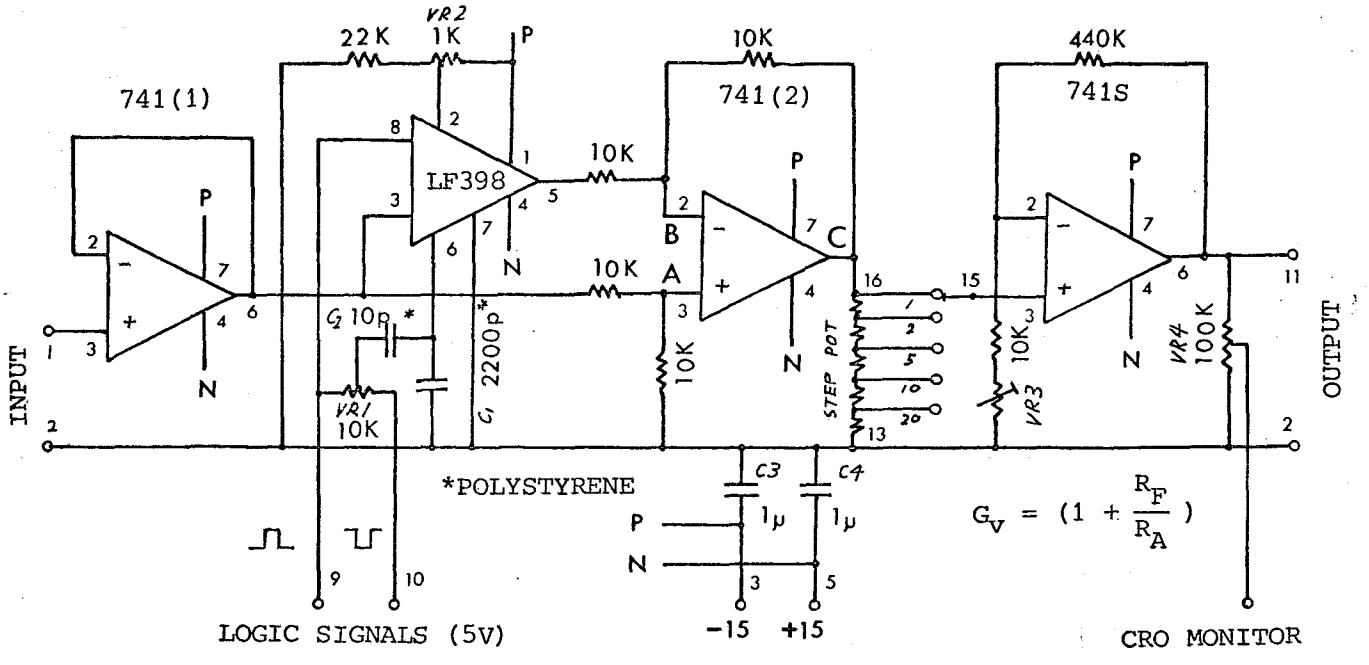


Fig. 2 Main circuit BD50 based on the principle shown in Fig. 1.

3.2 Timing circuit

Although the pulse width of T_o (see Fig. 1) is not critical, it is important that the end of the period T_o is exactly the same as the start of a voltage representing an 'external force'.

Fig. 3 shows a scheme to satisfy this condition. The 'input memory' stores a waveform representing an 'external force', with an undisturbed period, T_s. The timing circuit, which is controlled by a clock, generates two types of pulse:

P_1 : Pulses to read the whole contents of the input memory, including the undisturbed period.

P_2 : A single pulse having the width of T_o which ends at the end of T_s.

The voltage representing the 'external force' is read from the memory by P_1, and this is fed into the 'main computation network'. The 'response' to this external force is measured by BD50 to which P_2 is supplied.

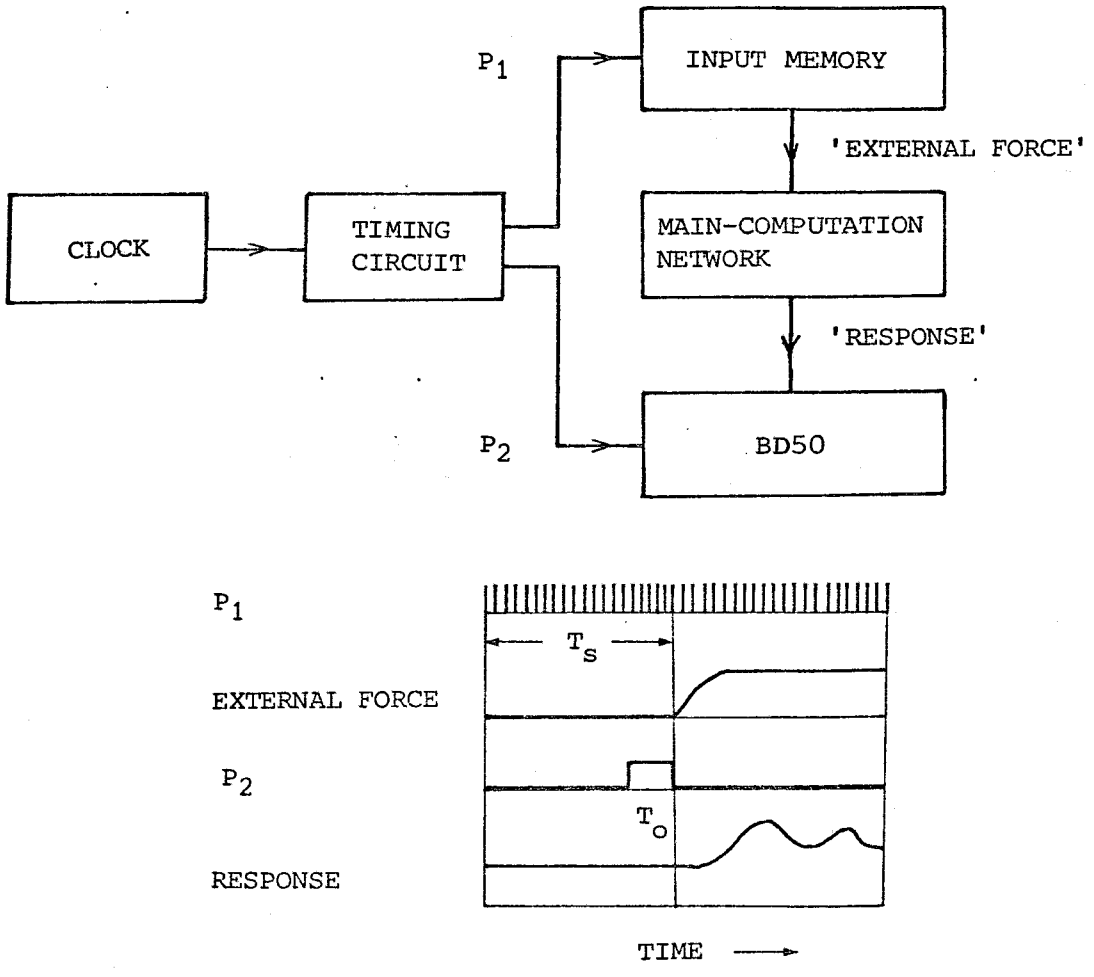


Fig. 3 Scheme of the timing circuit for generating T_o

Fig. 4 shows an example of an actual circuit based on the scheme shown in Fig. 3. The counters, 93(3) and 93(4) are built on board M1 of the input memory. The outputs from E and F are fed into terminals 9 and 10 of BD50 respectively, and G into BD22 for synchronizing the start of an operation.

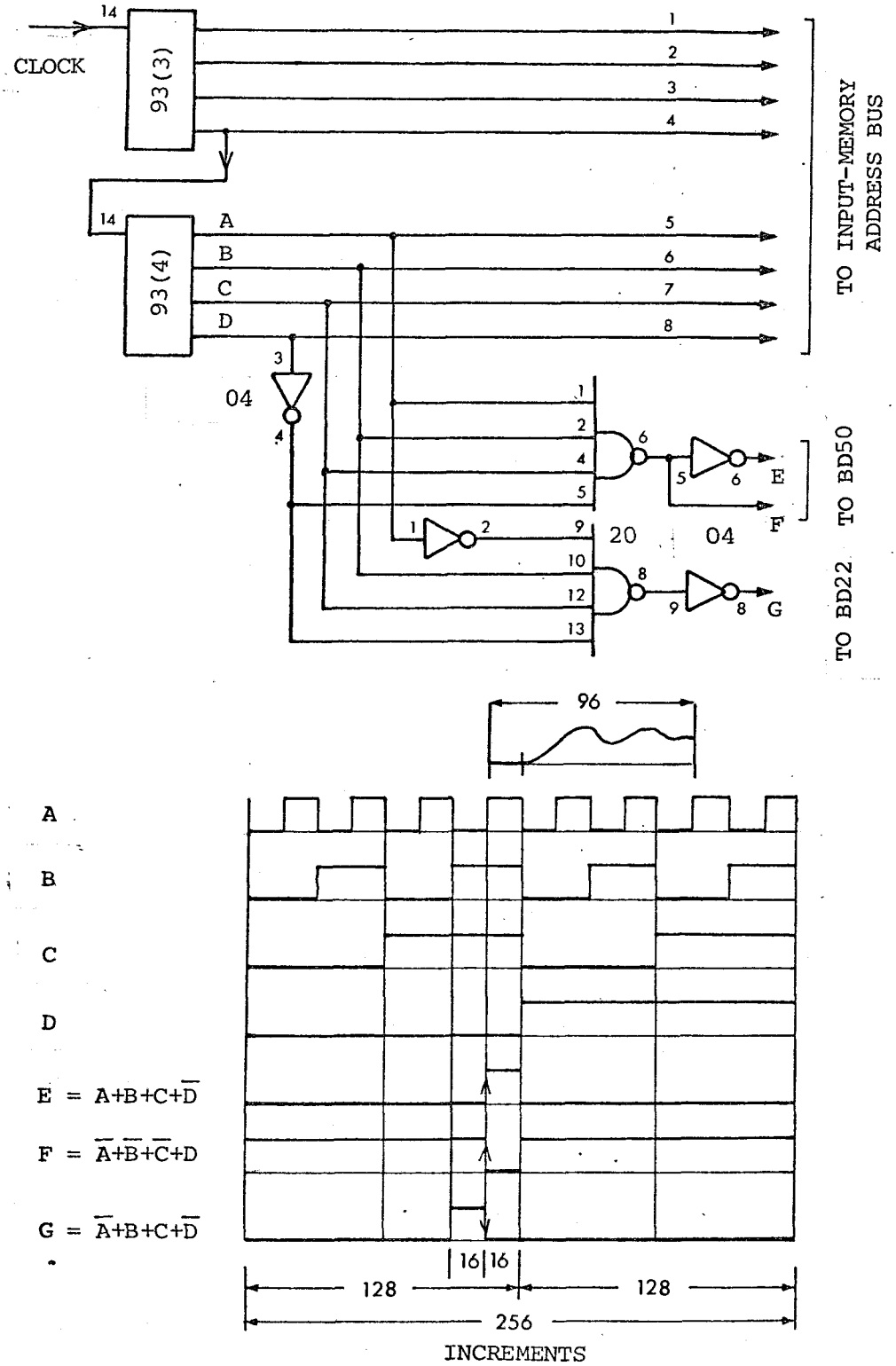


Fig. 4 Example of an actual timing circuit based on the scheme shown in Fig. 3, and its timing diagram.

4. PHYSICAL ARRANGEMENT

Fig. 5 shows the physical arrangement of circuit board BD50 with the step-potentiometer (gain control), and related connectors. BD50 is contained in a small metal case (5 × 7 × 10 cm^2), fixed on the side of the main computation-network cabinet. This case, the control cabinet and input memory are connected by three cables. The timing circuit is contained in the input memory. The power (+15V and -15V, 150 mA max.) for BD50 is supplied from the control cabinet.

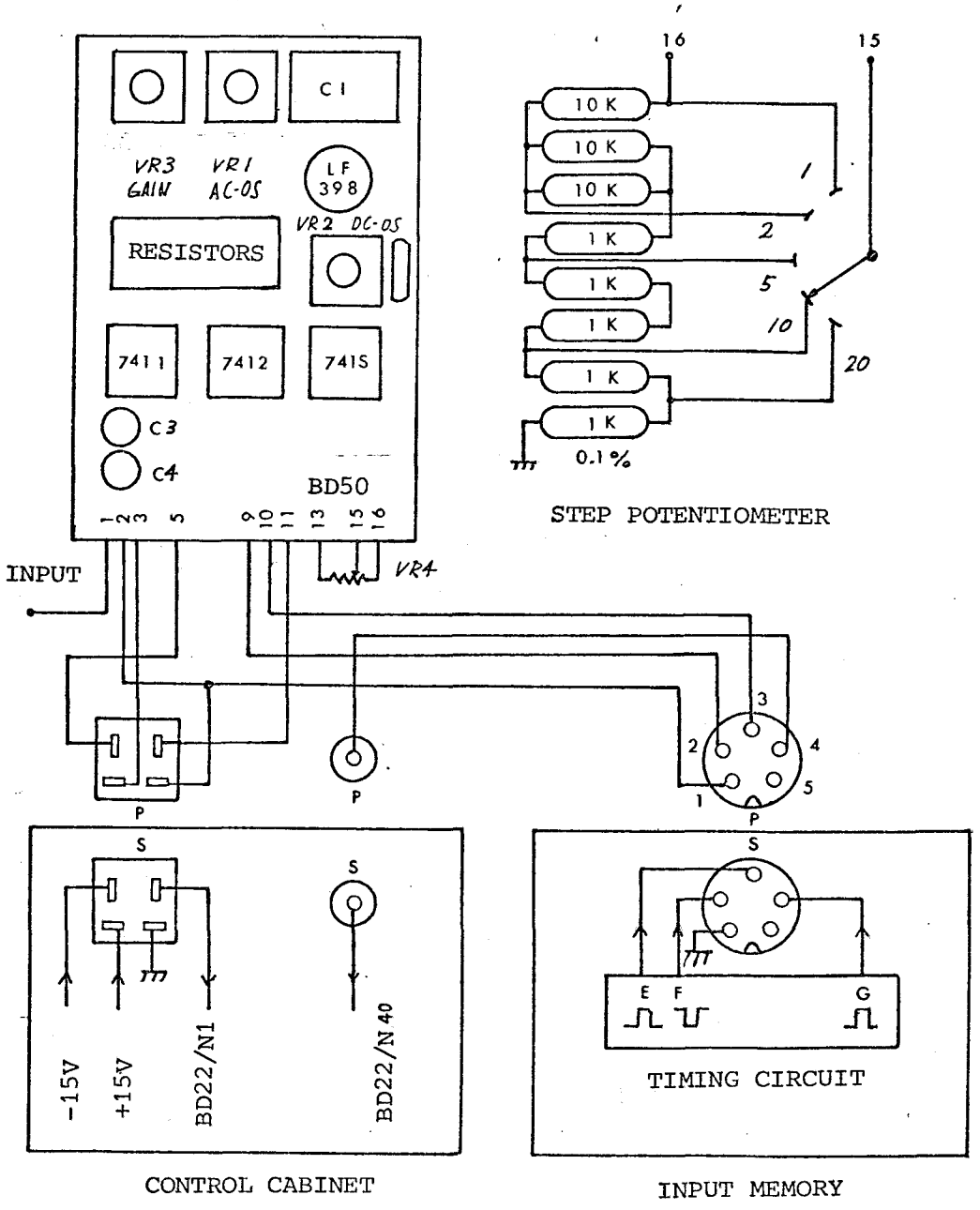


Fig. 5 Physical arrangement of BD50 and related circuits.

5. CALIBRATION OF THE CIRCUIT

The voltage gain of circuit BD50 is adjusted by VR3 (see Fig. 2), after the dc offset and ac offset of LF398 have been adjusted by VR3 and VR2 respectively. For the calibration of the voltage gain, a circuit shown in Fig. 6 was used.

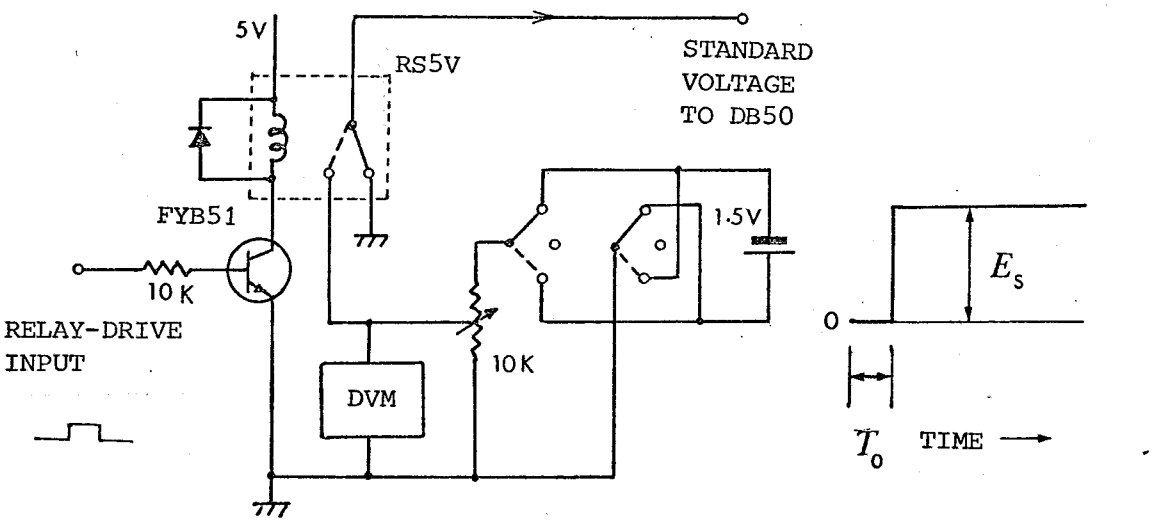


Fig. 6 Calibration circuit for BD50, and its standard waveform.

This calibration circuit generates a standard step-voltage E_s with a zero-volt period of T_o, as shown in Fig. 6. The value of E_s can be chosen between +1.5V and -1.5V, and the voltage can be read by a dc range of a digital voltmeter with a 4.5-digit accuracy. In order to obtain T_o, the logic pulse fed into terminal 9 of BD50 (see Fig. 2) should also be fed into the relay-drive input of the calibration circuit.

With the calibration circuit, the output of BD50 should be digitized by the ADC on BD22. Its digital output should be read by an appropriate instrument. Then the gain control VR3 should be adjusted to obtain the following conditions:

Input (mV)	Output (digits)
-127	254
0	127
+127	0

At gain control position 1, and BIPolar mode of the ADC.

Fig. 7 shows the relationship of the input and output, with gain control position 1, and BIPolar and MONopolar modes. Table 1 shows the relationships between the positions of the gain control and the ratio of the input and output values. Fig. 8 and Fig. 9 shows examples of actual calibrations.

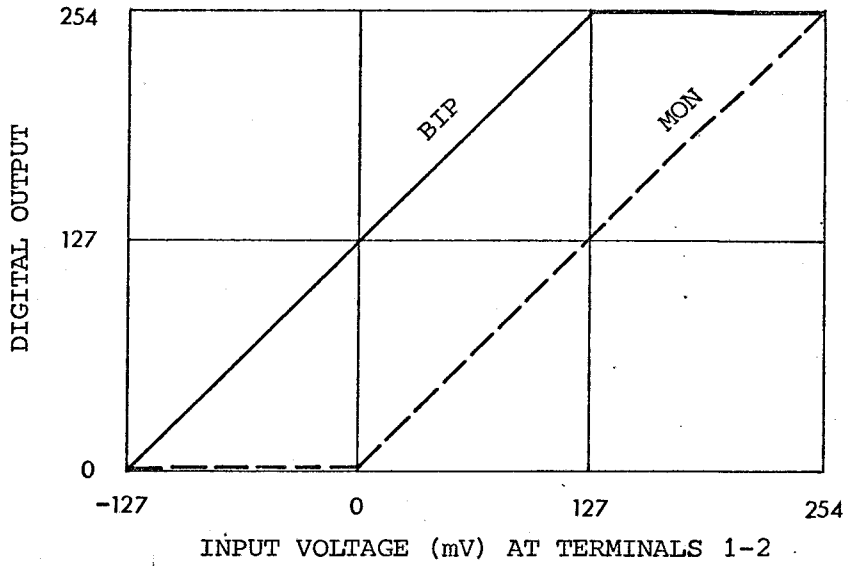


Fig. 7 Relationships between the input and output of circuit BD50 with a digitizer, in BIPolar and MONopolar modes, and the gain control position 1.

Table 1 Relationships between the input and output of circuit BD50 with a digitizer, in each position of the gain control.

Gain control position	Sensitivity
1	1mV/digit
2	1mV/ 2 digits
5	1mV/ 5 digits
10	1mV/10 digits
20	1mV/20 digits

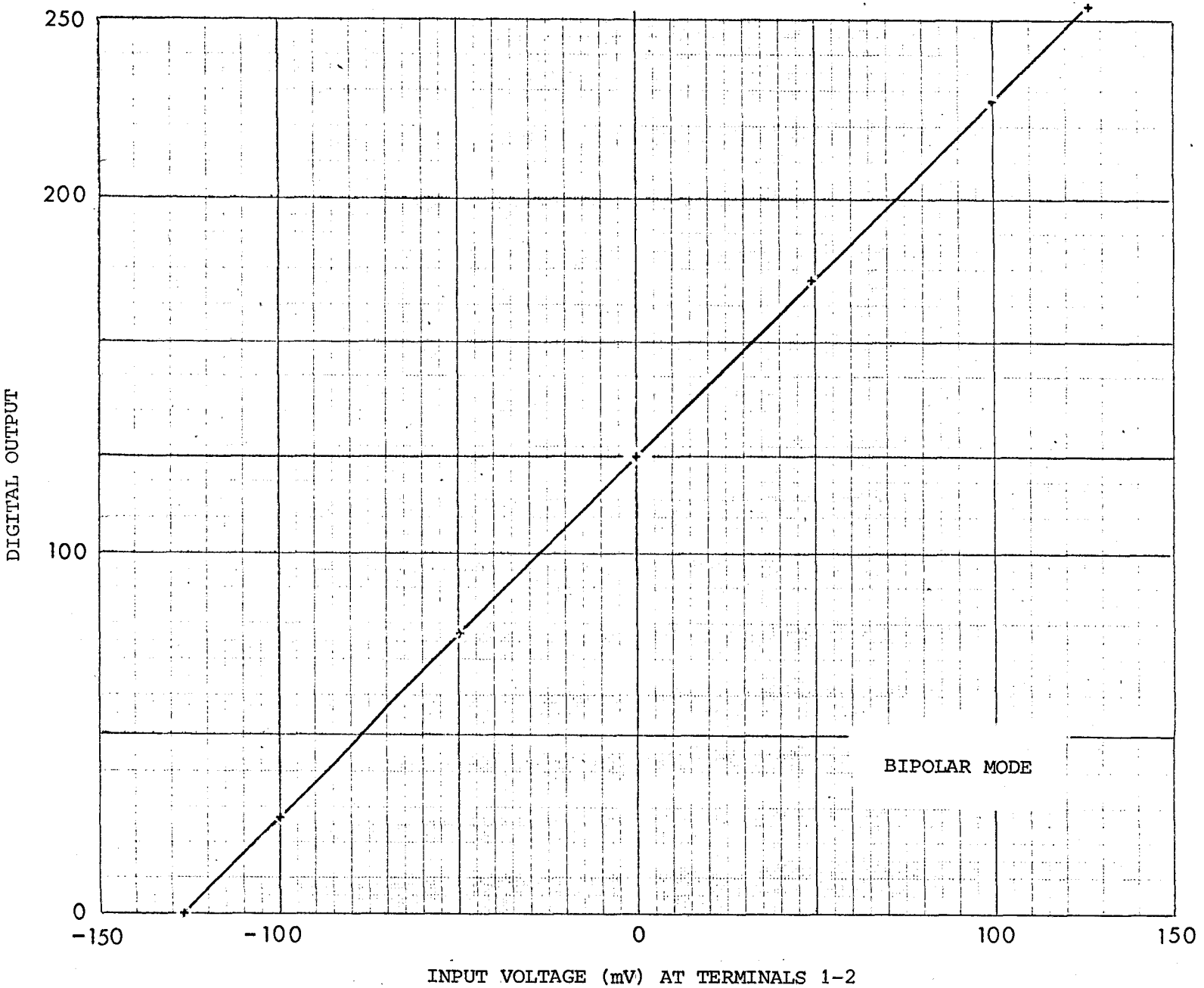
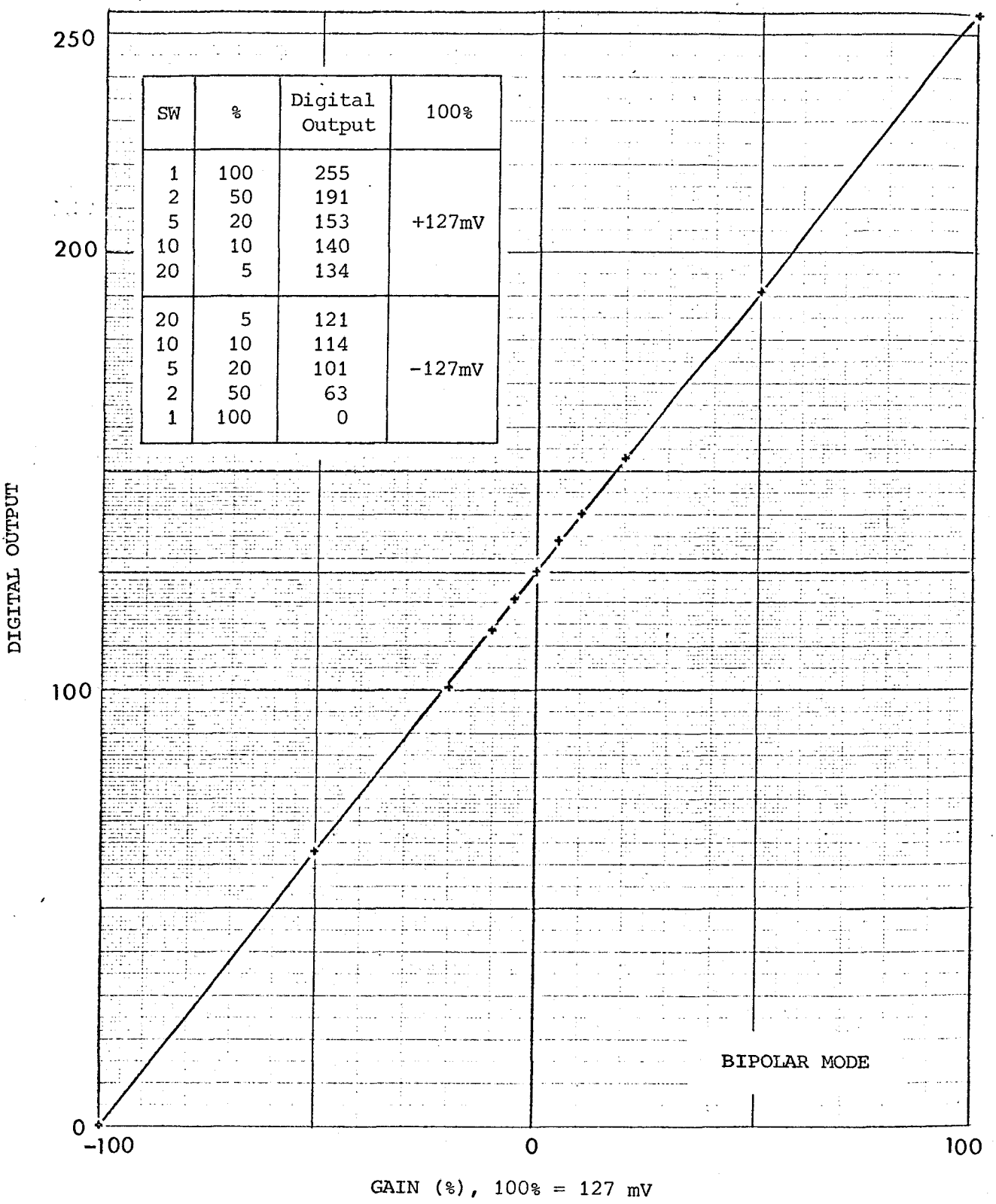


Fig. 8 Example of calibration of circuit BD50 showing its input and output.



SW	%	Digital Output	100%
1	100	255	
2	50	191	
5	20	153	+127mV
10	10	140	
20	5	134	
20	5	121	
10	10	114	
5	20	101	-127mV
2	50	63	
1	100	0	

Fig. 9 Example of calibration of circuit BD50, with different positions of the gain control.

6. CONCLUSIONS

In order to obtain information of sea-level responses to wind fields and atmospheric pressure fields, large amounts of data expressing the responses have to be processed. The circuit described in this paper contributed significantly to reducing the processing time of operations.

The circuit will have general applications.

A part of circuit BD22 has been modified to combine BD50. The modification has been described in a separate paper, together with its modifications for other requirements.