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INTERNAL DOCUMENT 184

I.O.S.

I.O.S. F.S.K. DEMODULATOR

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NATURAL ENVIRONMENT RESEARCH COUNCIL

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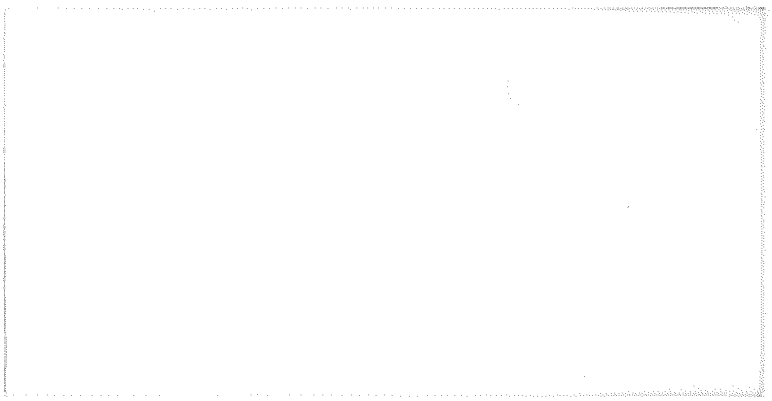

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1983

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I.O.S. F.S.K. DEMODULATOR

1. INTRODUCTION

This report describes an instrument whose purpose is to demodulate an F.S.K. data transmission, used, for example, by the Neil Brown and the I.O.S. D.W.P.S. (Deep Water Particle Sampler) systems. It was felt that there could be other potential users and that this system could provide an economical solution.

The equipment presently used within I.O.S. are expensive (up to £25,000) commercially manufactured units used with the C.T.D. systems. Primarily because of their expense, they are few in number and are constantly required for operational use. These units incorporate multiple channel 6 digit readouts, 12 bit D/A convertors and various other functions which although possibly necessary for an operational capability would not be a necessity for other applications such as maintenance and calibration. In the laboratory the D.W.P.S. system requires an F.S.K. demodulator for bench testing and maintenance as well as calibrating the particle cell system. There are also times when back-up data tapes need to be replayed either for data checking or into computing systems.

All the above requirements could be accommodated with a basic demodulator unit that would output the data in TTY format; generate clock pulses and produce a frame synchronising pulse.

The instrument described here satisfies the above requirements and has an additional feature of being able to display selected binary 8 bit data words.

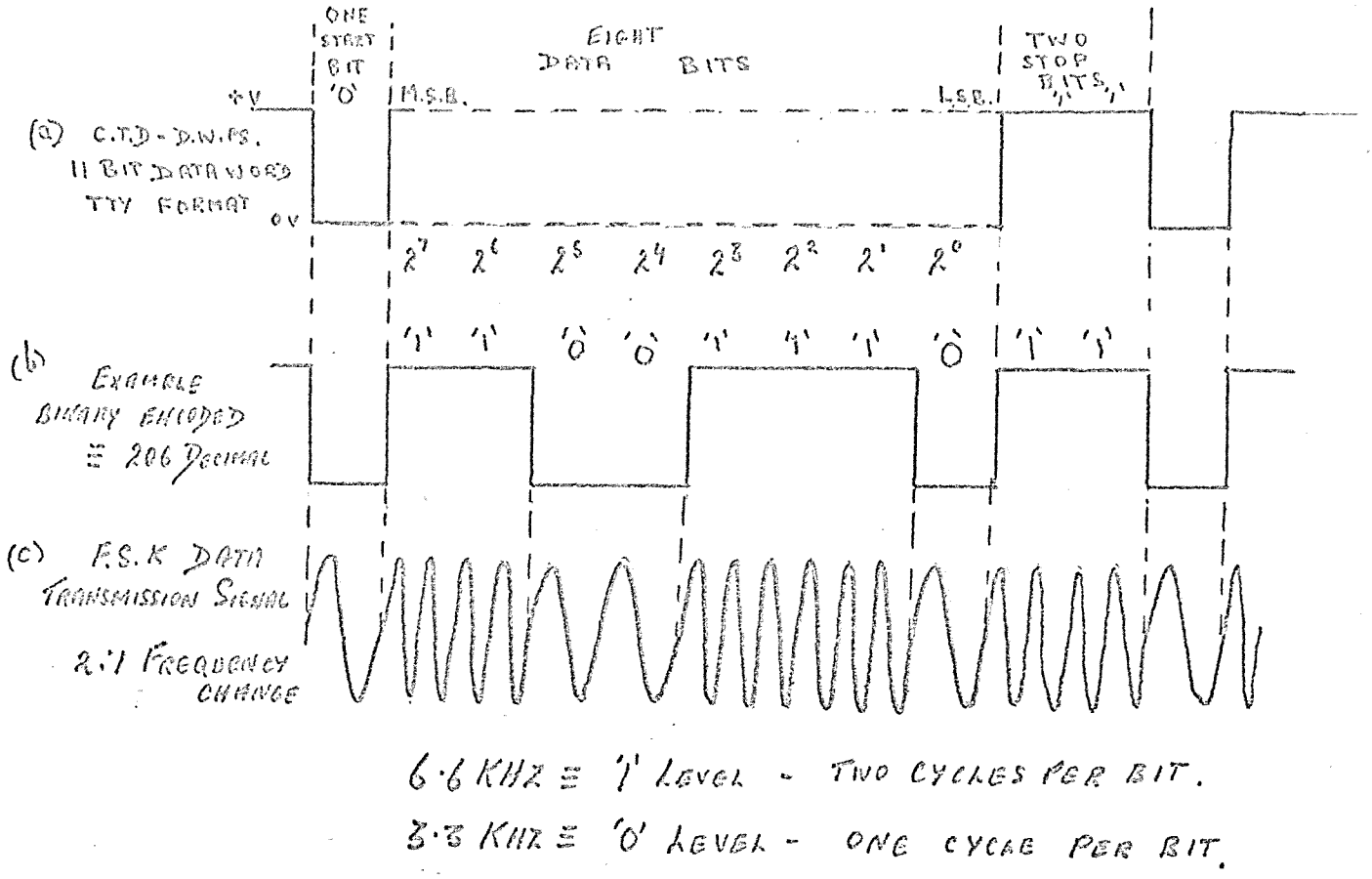


Figure 1. Serial Data and F.S.K. Modulated Waveforms

2. CIRCUIT DESCRIPTION

Fig. 1(a) illustrates the format of the TTY 8 bit data words generated by the underwater unit. These words are binary coded and figure 1(b) shows the binary equivalent of 206 decimal encoded, while waveform 1(c) shows the data on the transmission line after passing through the frequency shift keying (F.S.K.) modulating system.

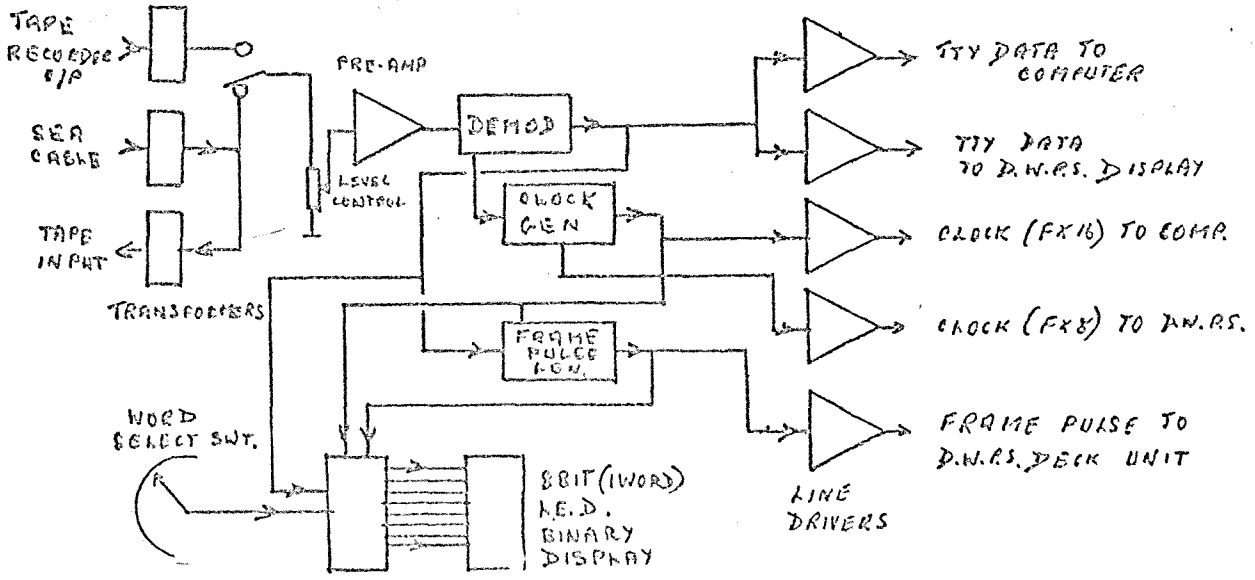


Figure 2. Block Schematic Deck Unit

With reference to Figure 2 and to the detailed circuit diagrams, the system operates as follows. The F.S.K. data is coupled to the level control at the input of the pre-amplifier (I.C.1) via a line transformer from either the tape recorder or sea cable. For explanatory purposes the C.T.D. F.S.K. modulating frequencies are used in this description i.e. $3\frac{1}{3}$ kHz (low level) and $6\frac{2}{3}$ kHz (high level). The data source is selected by a switch on the front panel. The nominal signal amplitude at the input is ±0.75 volt and inspection of the signal shows attenuation of the high frequency component due to cable capacity effects. The feedback resistor is shunted with a diode network which produces ±1.6 volt pulses of equal amplitude for high and low frequencies. The pre-amp input is also connected to a +6 volt d.c. source which results in the data output biased about this level. This output is connected to one input of a voltage comparator (I.C.2) while the second input is connected to the +6 volt d.c. bias voltage. Optimum adjustment of the input level setting control sets the effective threshold level of the comparator producing a noise free square wave data stream.

The 311 comparator (I.C.2) output is connected via inverters to the demodulator and clock generator circuits. The demodulator consists of a dual binary up counter (I.C.4, CD4520BE), a dual D type flip flop (I.C.6, CD4013BE). For ease of explanation the demodulator waveform diagram is shown in Figure 3.

The F.S.K. signal is applied to the reset input of the binary up counter (I.C.4) holding this I.C. off until the signal changes to a low state. When the next pulse changes to a low level the clock pulses (derived from the clock pulse generator at pin 1 (I.C.4) are divided down. Clock pulse frequency is 32 × bit rate i.e. 106 kHz. When the low frequency ($3\frac{1}{3}$ kHz) component is present on the F.S.K. signal there will be pulses at both Q3 (÷8) and Q4 (÷16) outputs of I.C.4. With a high frequency input only Q3 will produce an output. The Q3 and Q4 outputs are taken to the inputs of a NAND gate (I.C.3) the output of which is fed back to the enable input of I.C.4. The NAND gate output will hold off I.C.4 when a pulse has been generated at I.C.4 Q4 output. When the I/P signal to I.C.4 changes from a low level to a high level, I.C.4 will be reset. The output of the NAND (I.C.3, pin 3) is also connected to the 'D' input of a D type flip flop (I.C.6A) with the F.S.K. signal connected to the clock input (pin 3). The output is coupled to

one input of a dual NAND gate (I.C.5, pin 12) which has the second input (pin 13) connected to the output of the first gate (I.C.3, pin 3). The output of this second gate (I.C.5, pin 11) is used as the 'D' input of the second flip flop (I.C.6B). The input data signal is connected to the clock input of this I.C. and the 'Q' outputs are the demodulated TTY data. These outputs are taken via normal/reverse switches and line drivers (I.C.11, I.C.12) to the computer interface unit and to the FIDO deck unit. Note the phase change when comparing the F.S.K. data input and the demodulated output data.

The clock pulse generator consists of a phase lock loop (PLL) operational amplifier (I.C.7) and a binary up counter (I.C.8). The free running output frequency of the PLL is approximately 100 kHz while with a $3\frac{1}{3}$ kHz bit rate signal it will be locked in at 106 kHz (32 × bit rate) and in double time, when using the tape recorder replaying at twice recording speed, at 212 kHz. The input to the PLL (I.C.7) is taken from the output of two gates in the demodulator section. These gates (I.C.5 and I.C.3) break up the input signal to enhance the higher frequency of the signal so reducing any tendency for the PLL to swing off its locked on state when the data contain a series of 0s (low frequency). The 106 kHz O/P is used in the demodulator (I.C.4, pin 1), the 53 kHz, the 16 × bit rate frequency to the computer via line drivers, the 26.5 kHz O/P (8 × bit rate frequency) to the FIDO deck unit and 3.3 kHz (bit rate) to the frame pulse unit. The lock in range of the PLL covers bit rate frequencies of approximately 2 to 8 kHz and can with a small modification cover a larger band.

The frame pulse unit consists of two dual four stage static shift registers (I.C.9,10), a 12 diode AND gate and an inverter (I.C.5). The shift registers are connected in series, the input being the TTY data from the F.S.K. demodulator. The input and the first eleven consecutive outputs are coupled by diodes to form an AND gate which only produces a positive level output twelve bits after the last word in the frame is completed (when the data is at a '1' level). The output will then return to zero at the start bit ('0' level) of the frame. The pulse is inverted and the rising positive edge becomes the start of the frame synchronising pulse. The pulse is coupled via line drivers to the FIDO deck unit.

The circuit diagram for displaying selected 8 bit words on 8 LEDs is shown in Figure 5. The UART (I.C.1) removes the start and stop bits

from the TTY data and the octal latch driver (I.C.2) is connected to the LEDs. To select a particular word the frame synchronising pulse is used to reset the UART and two 4017 counters (I.C.4, I.C.5). The 'data ready' (DR) pulses, generated by the UART at the end of each data word entry, are counted and the output strobes at each stage are connected to two 10 digit switches on the front panel, one switch for the 'units', the other for 'decades'. The wipers of the two switches are connected via a NAND gate and inverter to the strobe I/P of the LED latch driver (I.C.2). When a strobe pulse is applied to pin 2, I.C.2, the data present at the input ports are latched into the output.

The circuit diagram of Figure 6 shows the arrangement of the conventional d.c. power supply p.c.b. Transformers T_1, T_2 and T_3 are the data line matching transformers for interfacing the deck unit, the tape recorder and the underwater unit and cable. A miniature loudspeaker is driven off the data line to give audible data indication.

The complete unit is packaged in a 19" rack mounting Verovip drawer unit 2U (88.9 mm) high. All the connections into the unit are via the back panel and the front panel arrangement is shown in Figure 7.

3. OPERATIONAL RESULTS

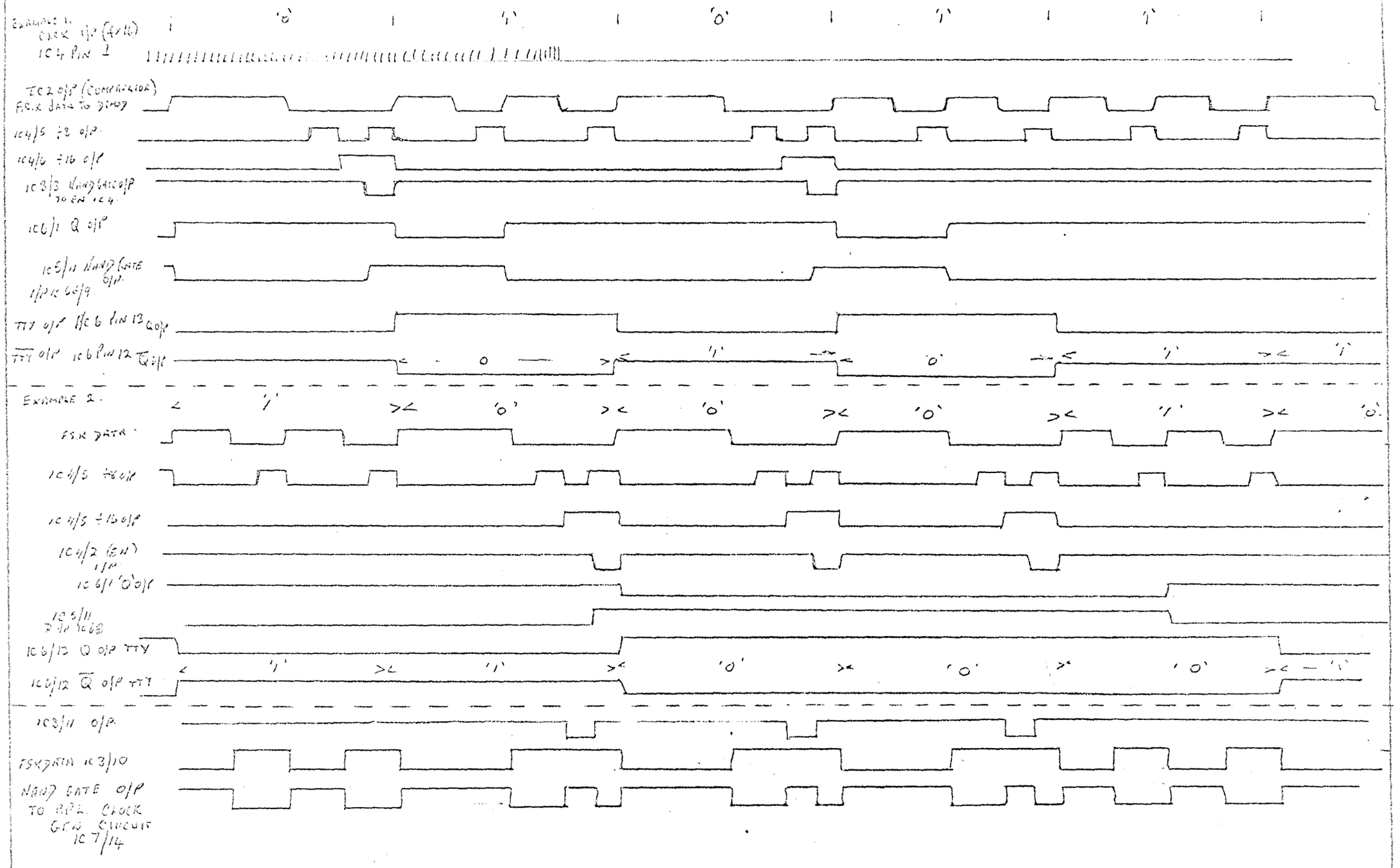
The prototype unit was used extensively during a 4 week cruise in April 1983 providing data to the ship's computer system and to the back-up tape recorder. The initial adjustment of the level control was found to be satisfactory for C.T.D. and F.I.D.O. transmissions and the capability of the unit to lock on to the transmission easily, readily and quickly, not only saved time but gave confidence in the system. Another advantage lay in the time saved by being able to replay tapes at twice the recorded speed, a feature that the present C.T.D. system does not permit.

4. DEVELOPMENTS

At the present time the unit is being interfaced to a PET Micro for displaying particle data with the D.W.P.S. This will assist in real time data assessment and during calibration.

5. ACKNOWLEDGEMENTS

Thanks are due to R. Pascal of the Applied Physics Group for his work in preparing the prototype and to K.G. Birch for his work on the software programming for interfacing with the PET.



D.W.P.S. [FIDO] F.S.K DEMODULATOR - DECK UNIT.

F.S.K DEMODULATOR WAVEFORMS.

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REVISED	DRAWN BY TJPG DATE MAY 1983 SHEET No. FIG 3
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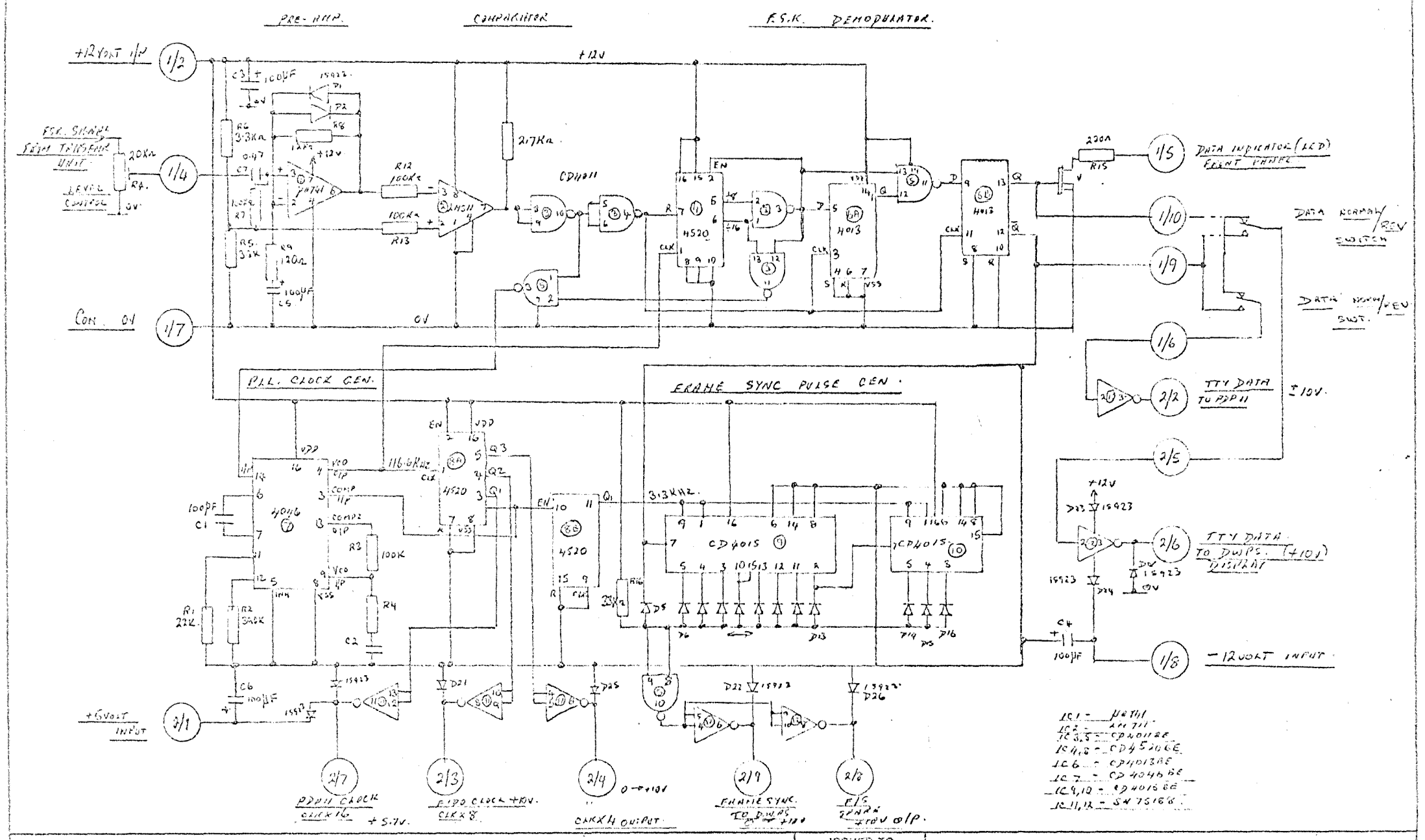

D.W.P.S. [FIDO]. F.S.K. DEMODULATOR - DECK UNIT.

PRE-AMP - DEMODULATOR - CLOCK GEN - FRAME SYNC GEN.

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ISSUED TO

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DRAWING No. I.O.S./

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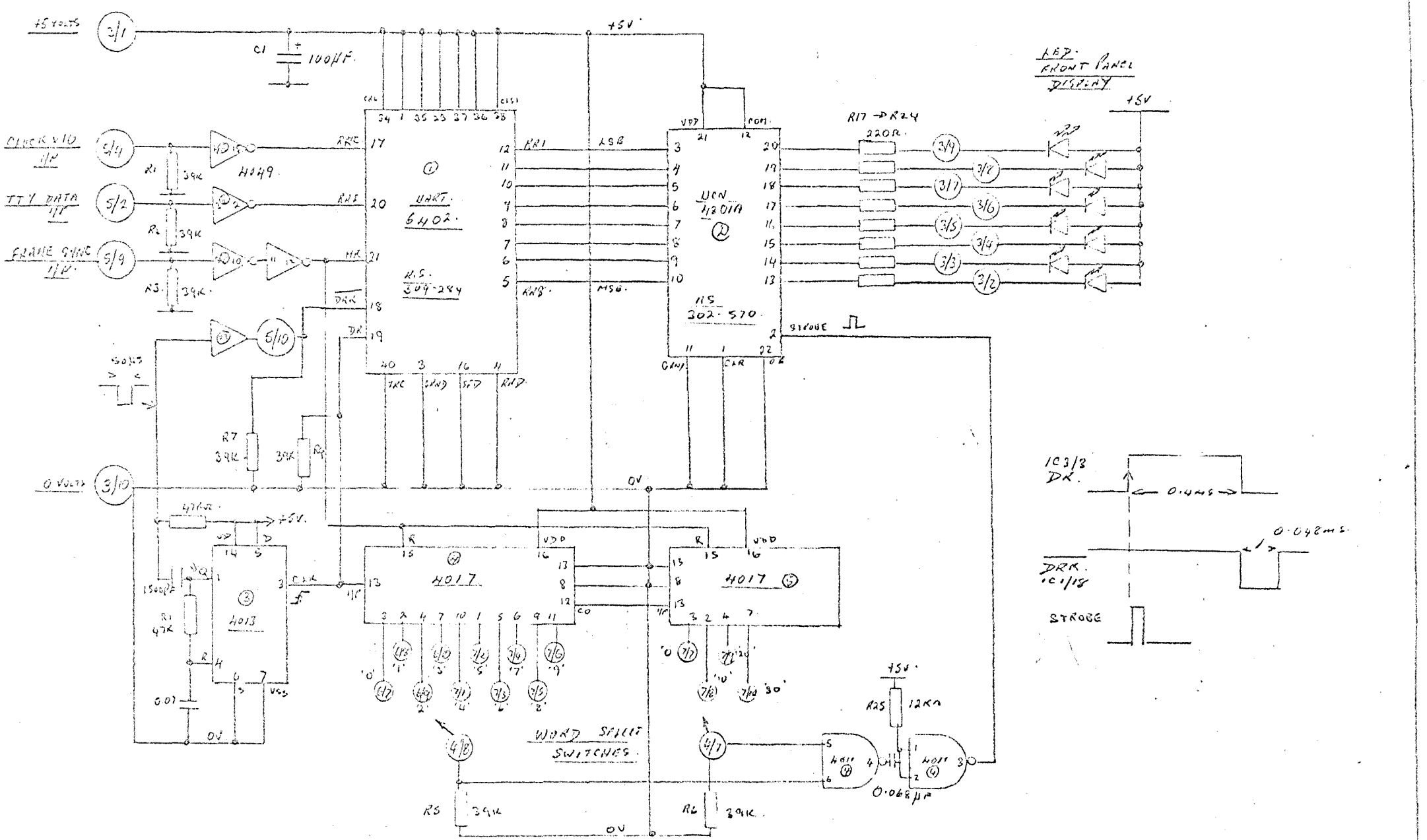

D.W.P.S. [FIDO] F.S.K. DEMODULATOR. - DECK UNIT.

DATA WORD [BINARY] DISPLAY CIRCUIT

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ISSUED TO	DRAWING No. I.O.S./
REVISED	DRAWN BY T.J.P.G. DATE MAY 83 SHEET No. FIG 5.
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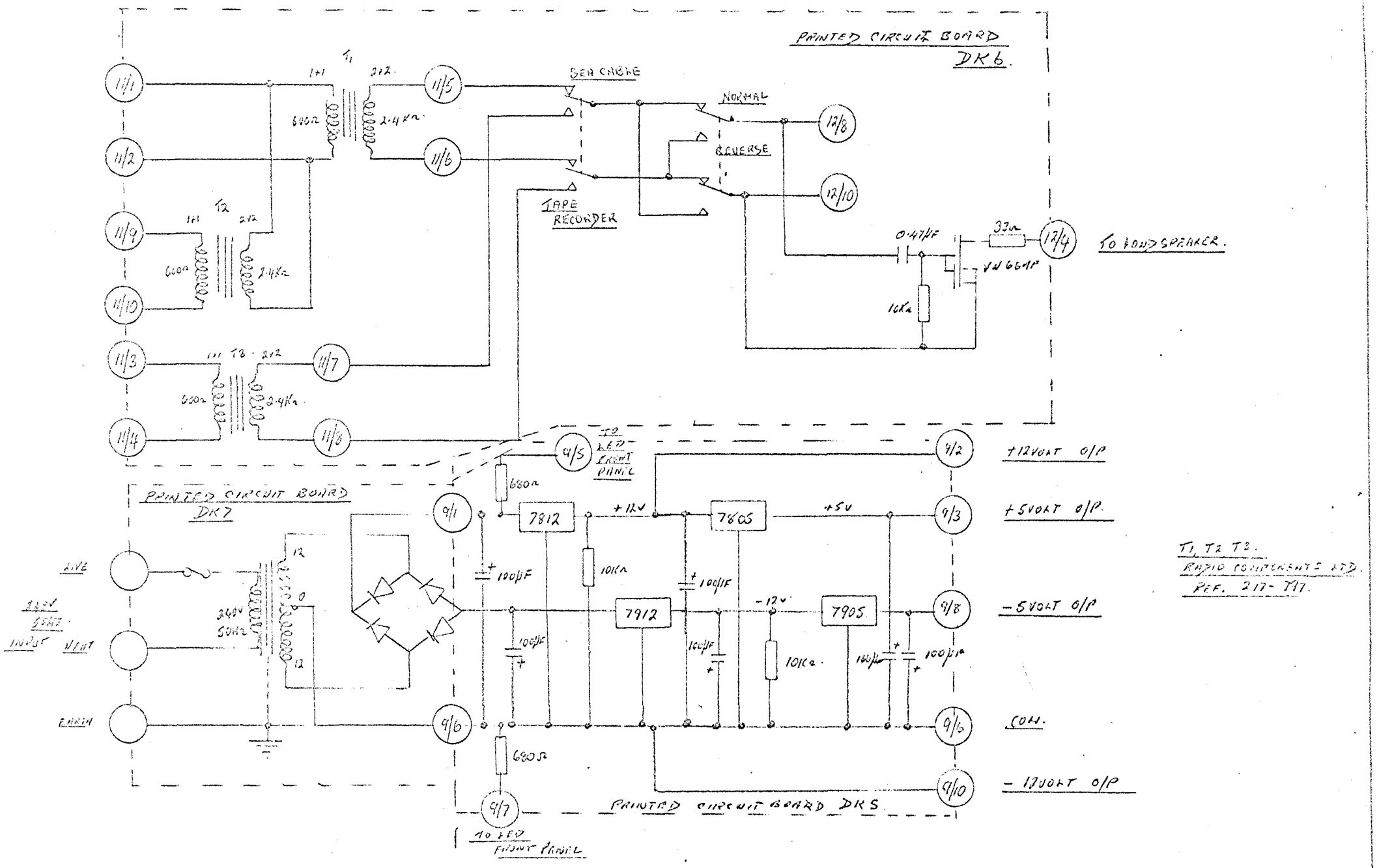

D.W.R.S. [FIDO]. F.S.K. DEMODULATOR. - DECK UNIT

DATH TRANSFORMER CIRCUIT.

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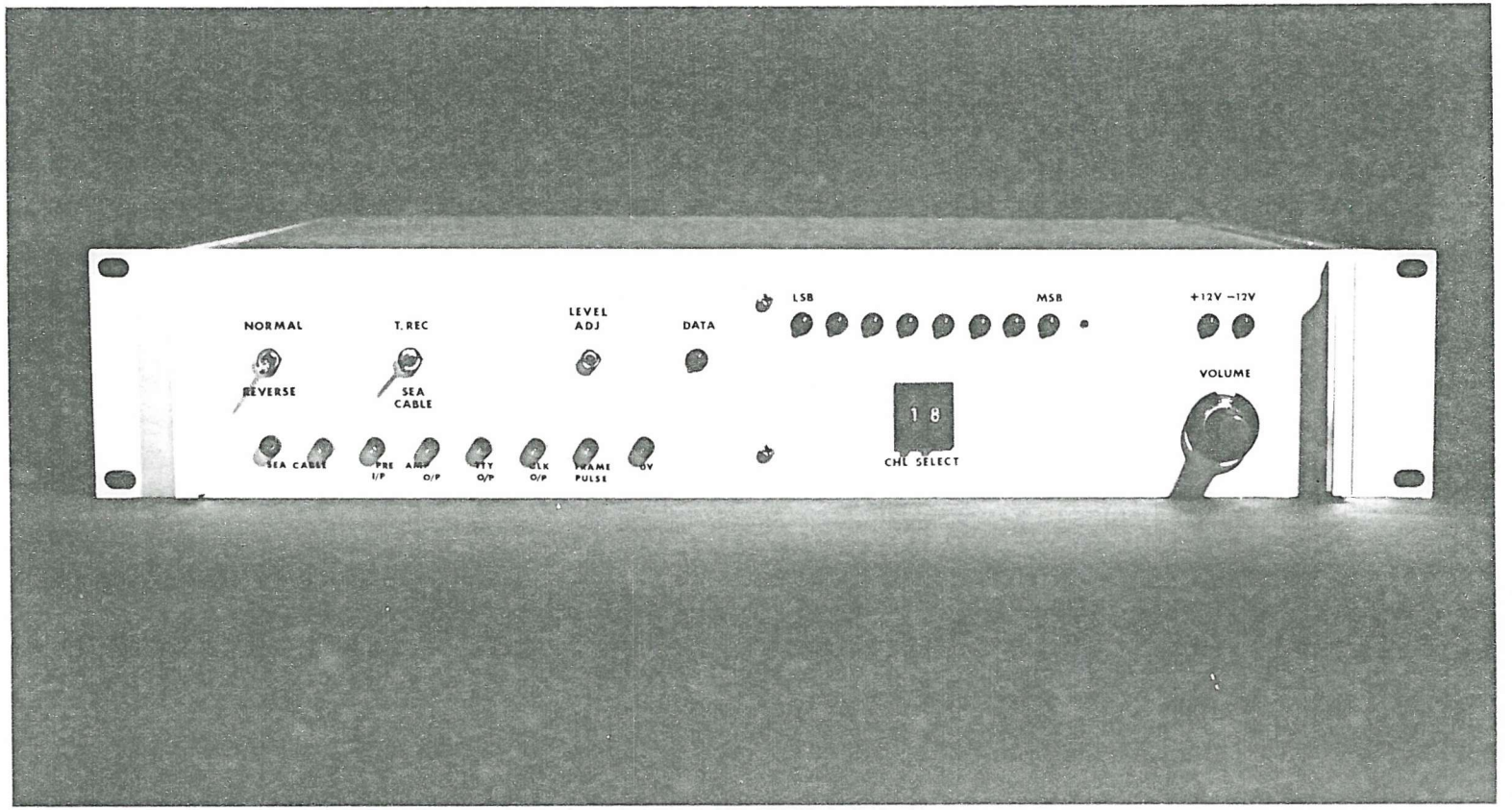

FIG. 7. F.S.K. DEMODULATOR - FRONT PANEL LAYOUT