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INTERNAL DOCUMENT
60

Input memory

A part of the electronic model for tides and storm surges

S. Ishiguro

January 1977

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Input memory

A part of the electronic model for tides and storm surges

S. Ishiguro

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Contents

29 diagrams and 13 tables

Abstract

As an essential part of the electronic model for tides and storm surges, a semiconductor memory having 6-bit 28K words has been designed. This has a single channel 8-bit parallel-word digital input (6 bits for data, and 2 bits for control), and 140 channels of analogue-current output each of which can drive up to 5 opto-electronic couplers in series (700 in all) without being affected by the load conditions. The order of words fed into the input is re-arranged internally, so that 140 sets of different series of data are available from the output simultaneously, in either the form of F(t)s or F'(s)t, depending on a control setting. The same output but in digital form is also available, although terminals are not provided externally. The writing and reading speed can be arbitrary, from zero to about 1 million words per second, depending on the external instruments. The same memory is utilized, when it is not used for its original purpose, for part of the numerical map plotter which is built into the model system.

1. Introduction

An electronic model by which tides and storm surges in an arbitrary shallow sea can be simulated has been developed (see a separate paper). Input data representing external forces, such as wind stress, atmospheric pressure, tide-generating force, are fed into the model system in a digital form. A memory for storing these input data within the model system is called, in this paper, the 'input memory'. It has been developed specially for this purpose, since several special features are required. The same memory is utilized for the numerical map plotting, also within the system, for economy. Fig. 1 shows the position of the memory in the model system, greatly simplified.

The choice of type of memory and its circuit configuration was made early in 1972 to make the cost-performance optimum. The rapid advance of electronic components and their availability have made this choice less good, but the same design has been used up to today. The committee who examined the author's proposed plan of the model gave their comments for the input memory, but the author could not accept them (see Appendix 6).

This paper has been written to give enough information for servicing and operating the apparatus, as well as that on the design.

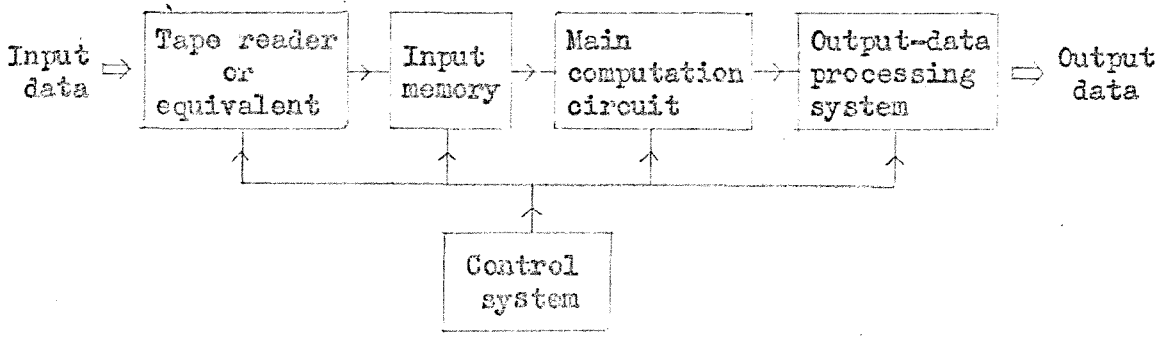

Fig. 1 Position of the input memory within the model system (greatly simplified).

2. Basic requirements

The input memory has been prepared to store the input data and to feed the stored data into the main computation circuit, satisfying the following basic conditions:

(1) Input data are available at various speeds and intervals from different sources, e.g. a key board, tape reader, data line, while the main computation circuit requires an exact data-feeding speed specified by K_t*.

(2) Most input data are available in digital form, while the main computation circuit requires analogue voltages or currents specified by K_e or K_i*.

(3) Most input data are available in the form of $F(x,y)$ or $F(t)_{x,y}$, and are transmitted in series, while the main computation circuit requires the form of $F(t)_{x,y}$ only and totally in parallel.

(4) The whole computation is completed rapidly (typically within 10 ms) by the main computation circuit, and a large amount of output data (typically 10^5 to 10^6 words) appears simultaneously, while most recorders in the output-data processing system cannot cope with this speed. An efficient arrangement is to repeat the complete computation, by using the input memory, as often as required so that the output data are recorded in turn.

(5) The electronic output of the input memory should be matched with the light-emitting diodes of opto-electronic couplers used for the external-force input of each grid card**.

(6) The memory should have a capacity of at least 168K bits (70 stations, 2 components, 200 time-increments, 6-bit word).

(7) The memory is utilized for re-arranging the output data in the form of maps, by using an electronic circuit, RD4, and an alpha-numerical printer (see Ref. 3).

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* K_t, K_e and K_i are constants on which all the parameters of an electronic model are based.

** By combining a number of such cards, the hydrodynamic system of an arbitrary sea can be modelled.

3. Writing, reading and programme

Input data are given in series in the form of $F(x,y)_t$ or $F(t)_{x,y}$, with 140 sets of (x,y) and 200 increments of t, i.e. 48K of 6-bit words in all. The memory is divided into 140 sections each of which has one output channel.

Two different writing modes have been prepared:

Writing mode 1 — For input data in the form of $F(x,y)_t$. Each word belonging to t = n is stored in Address n of each of 40 channels, where n = 1 to 200.

Writing mode 2 — For the input data in the form of $F(t)_{x,y}$. All the words belonging to x,y = m are stored in Address 1 to 200 of channel m, where m = 1 to 140.

Reading of the stored data in all the channels is carried out simultaneously, and in synchronization referred to t, i.e. always 200 time-increments in one reading cycle. Three reading modes, each of which has different intervals of reading cycles:

Reading mode 0 — No intervals.

Reading mode 1 — With intervals, each of which is equivalent to reading time for 200 words.

Reading mode 3 — With intervals, each of which is equivalent to a reading time of 600 words.

Because of high operating speed, manual control of the apparatus is possible only for 'selection of writing mode', 'selection of reading mode', 'start' and 'erase of memory'. The rest of the actions inside the apparatus are controlled by programmed codes which are fed into its 7th and 8th input channels simultaneously with input data which are fed into the 1st to 6th input channels. Five different actions are represented by four different 2-bit binary codes, as shown in Table 1.

Table 1 2-bit binary codes to be fed into the 7th and 8th channels for controlling the input memory.

Code	Function
00	(Before 10 is fed) Reading, continue (After 10 has been fed) Writing, continue
10	Start reading
01	Stop writing, and start reading
11	Omit the word (in the same row) from writing

4. Outline of the circuit

Fig. 2 shows the block diagram (greatly simplified) of the input memory. The input data are read by the tape reader, and the final output is obtained in the form of multi-channel infra-red light beams which are fed into the photo transistors in the main computation network.

The tape reader is operated in a continuous mode (500 ch/s), and the output signal of the optical sensor facing the tape feeding holes (FH) is used for the writing clock. The tape driving motor start is controlled manually, through SW-M4 and the motor control circuit, but the tape motor stop is controlled by a code at the end of the tape. The tape driving motor is also stopped, for protection of the tape, by the same motor-control circuit, through the tape-speed detection circuit, when the tape speed is lowered by any external force (e.g. jamming of the tape). The output of the tape reader (six data channels and two control signal channels) is stored by the temporary memory in order to adjust the access timing of the following circuits.

The output of the temporary memory is permanently connected to all channels of the SSR (168K bit static memory), but storing the data in appropriate cells of the memory is determined by 140 channels of 'K signals' which are generated by the time-controlled demultiplexer.

When writing into the SSRs is completed, the code at the end of the tape is fed into the write/read control circuit, so that this generates 'REC signal' by which the SSR is changed to a reading mode. At the same time, the time-controlled demultiplexer, to which 'c signal' and three other signals from the write/read control circuit are fed, changes the K signals for an appropriate reading mode.

Each channel of SSR output (140 channels in all) is converted simultaneously into an analogue voltage by a DAC, and the voltage is converted again into a current by a VCC. The current is fed into LEDs in each channel which are connected in series (5 units maximum per channel, 700 units maximum in all). The current in each channel is sampled by a low resistance (10 ohms) and fed back to the VCC so that the current is independent of the load. The current is biased, through SW-M5, for linear operation of the LEDs. The voltage across the sampling resistance of each channel can be monitored through the output monitoring terminals.

SW-M1 selects writing mode 1 or 2. SW-M2 selects reading mode 0, 1 or 3. SW-M3 selects the period of the reading clock, T, T/2, or T/3, where T is the period of the clock supplied from an external source (normally 100 s, and synchronised with the clock of the output-data processing system). Each of these switches are combined with frequency divider (1), (2) or (3). Figs. 3 to 5 show the timing diagrams of the writing and reading modes.

DAC: Digital-to-analogue converter, VCC: Voltage-to-current converter,
SSR: Static shift register.

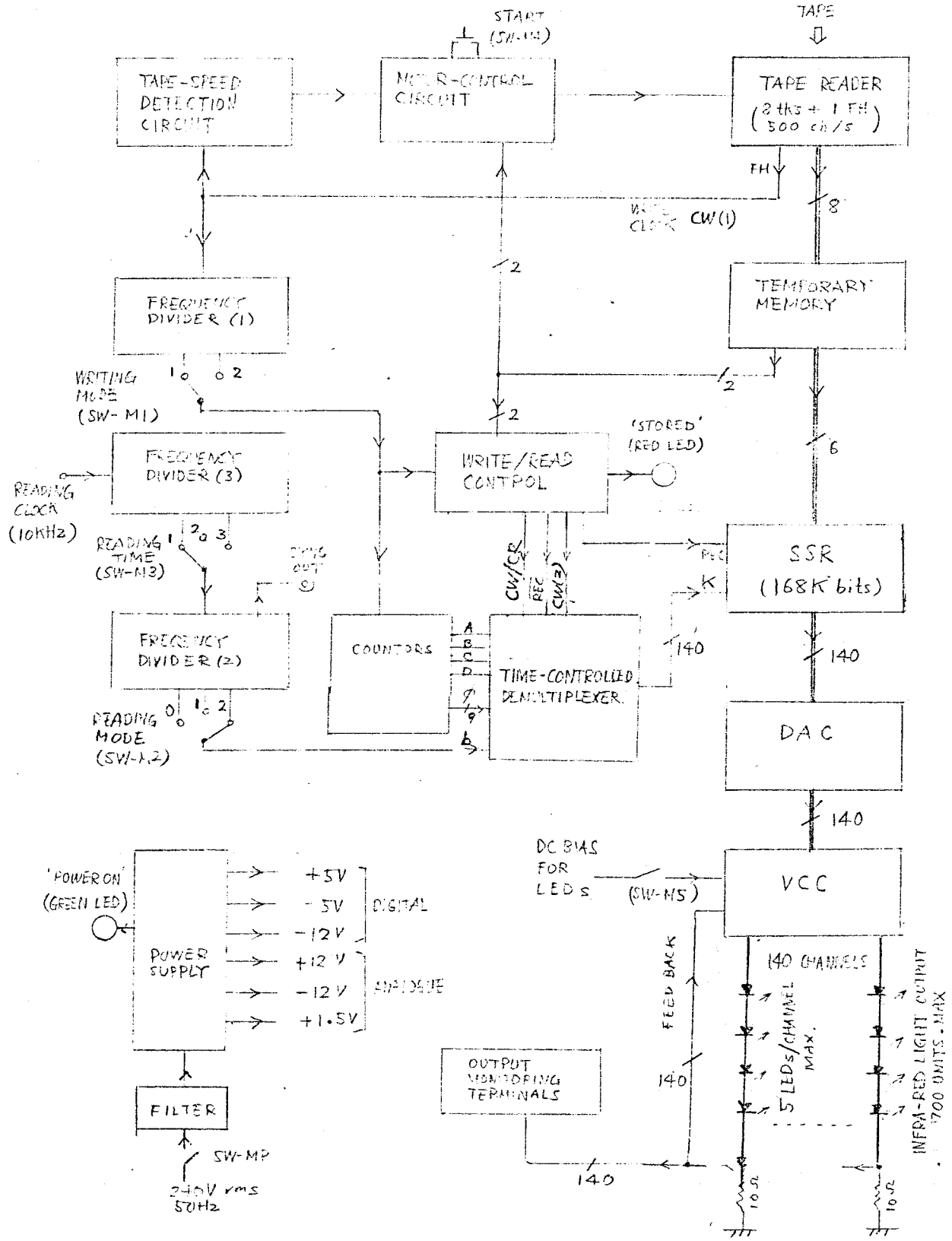


Fig. 2 Block diagram of the input memory.

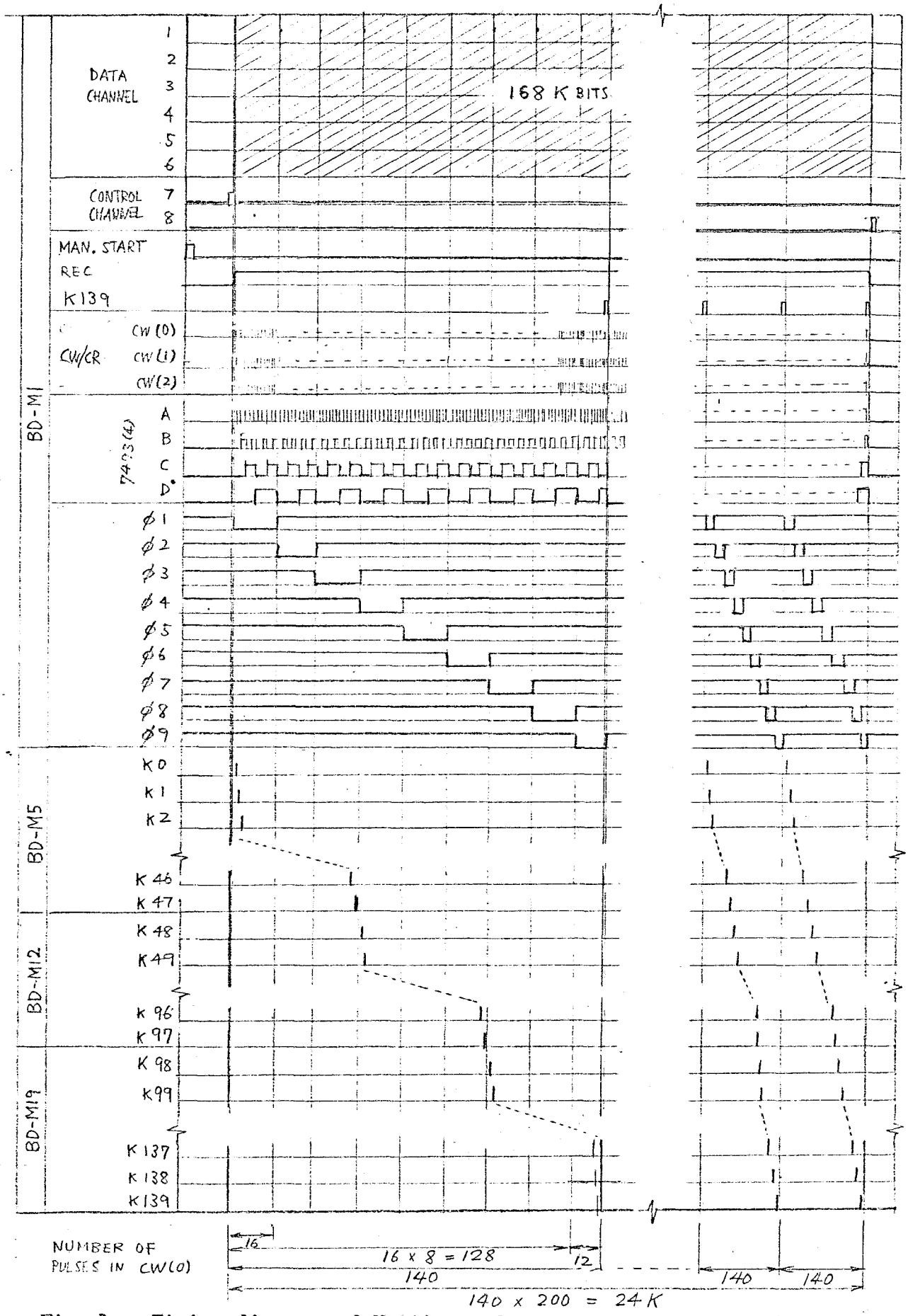


Fig. 3 Timing diagram of Writing mode 1.

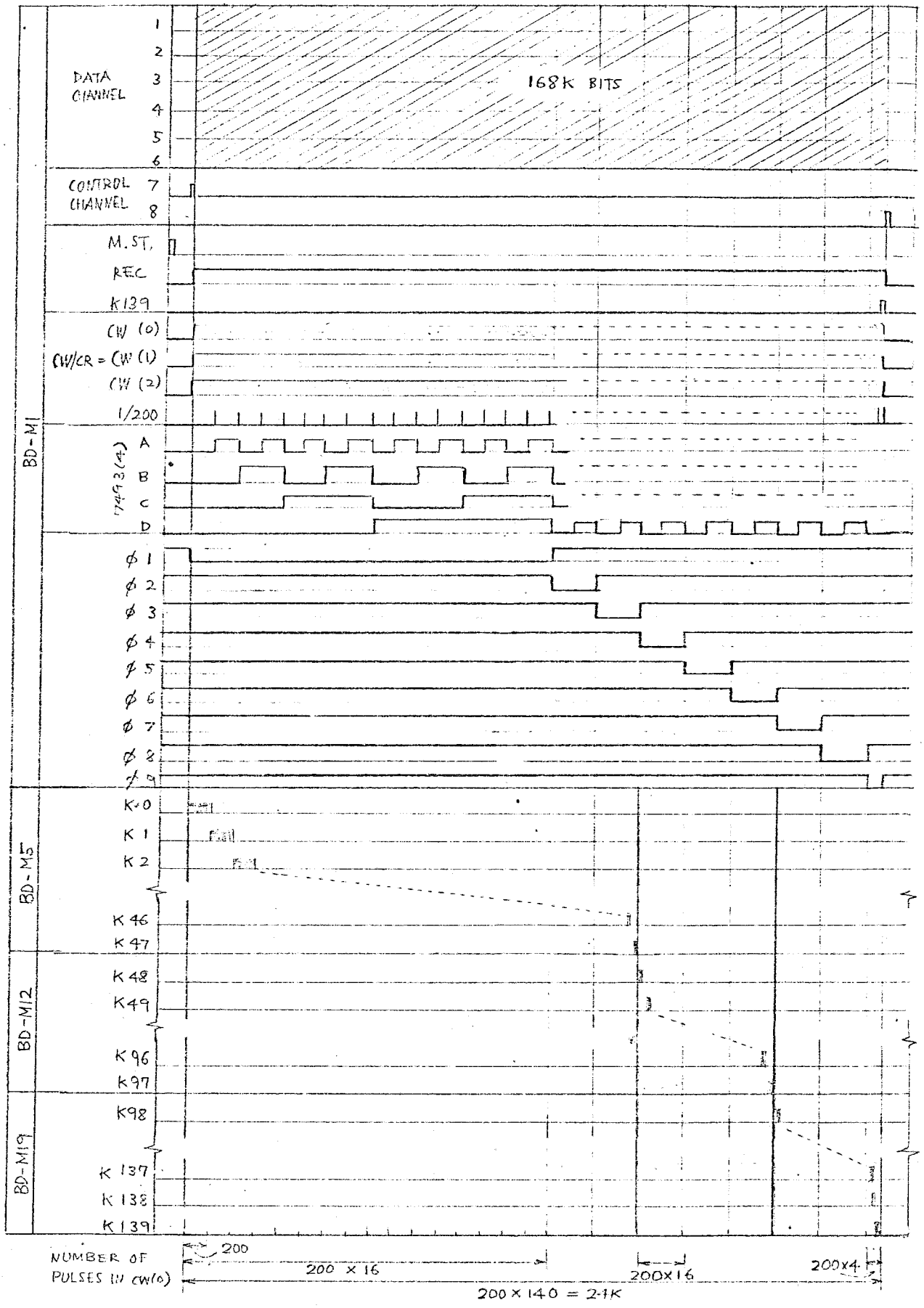


Fig. 4 Timing diagram of Writing mode 2.

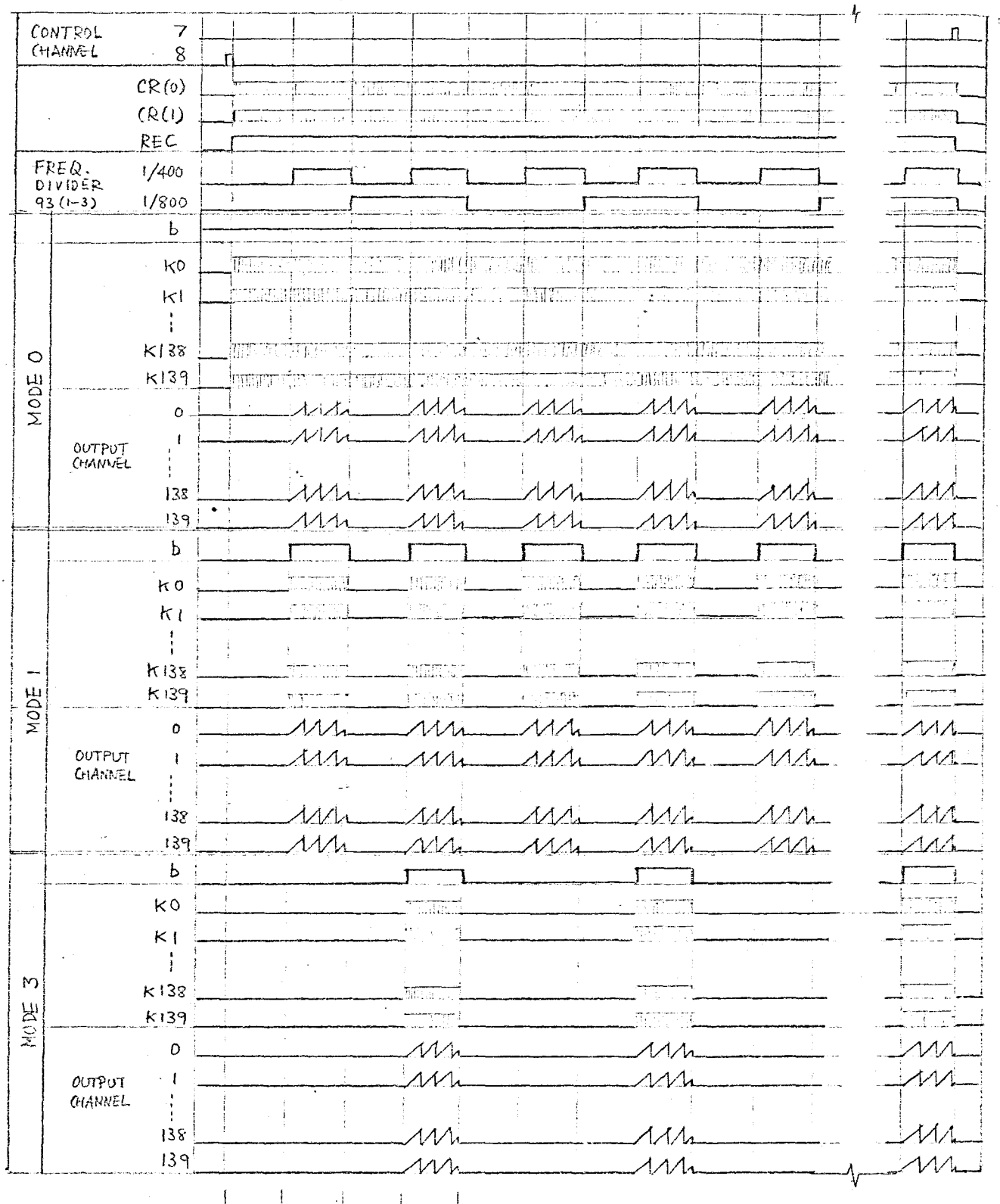


Fig.5 Timing diagram of Reading modes 0, 1 and 3.

5. Circuit descriptions

Figs. 7 to 10 show the circuit diagrams of the input memory, and Fig. 11 shows timing diagrams of some parts of the memory.

Tape reader and its interface (Fig. 6)

An optically-sensing punched-tape reader (500 channels maximum) is used. The tape is driven by a dc motor with a capstan (tape-feeding holes are not used for the originally intended purpose) and a solenoid-operated clutch. Each of the motor and clutch is driven by a transistor circuit. A train of pulse signals (one pulse per word) is obtained from an opto-electronic sensor faced on the tape-feeding hole (FH), other than those on the normal 8 tracks, and this is used for the writing clock. Fig. 6 shows the circuit diagram of the interface (the board containing this circuit is mounted inside the tape reader case).

74/5 (in Fig. 7) generates an 'ON signal' for the motor and clutch driving circuits, when SW-M4 is manually operated. The 74 generates an 'OFF signal' when its Pin 2 goes to a high state, through 32(3)/6. This occurs either when the tape-end signal (through Pin 4) or the 'tape slow-down signal' (through Pin 5) is fed. The latter is generated by the circuit including 122, when the period of FH signal becomes less than the predetermined value τ = 150 ms approximately (CR on 122/11).

Each word (8 bit) from the tape reader is stored in 75(1), and 75(2) until the next word is fed. The stored word is divided into two parts: tracks 1 to 6 for data channels which are connected directly to the SSR, and tracks 7 and 8 which are connected to the control circuit.

Write/read control circuit (Fig. 7)

74/8 is the main part of the write/read control circuit. This turns to a writing mode, when track 7 of the tape input is activated; and turns to a reading mode, when track 8 of the tape input is activated.

When this unit is in a writing mode, the writing clock, CW, enters from FH to the SSR, through 32(2)/4, 08(2)/4, 32(2)/12, 04/9, 121(1)/6 and to BD-M5, BD-M12 and BD-M19. In this mode, the reading clock is inhibited by 08(2)/1. At the same time, the writing clock is fed to terminal of BD-M5 etc. through pulse shaper 121(2), 32(3)/13, 08(2)/10, 04/5 and to temporary memory 75(1)/4; and through 08(1)/1 to frequency divider 93(1)/14; and to tape-speed detector 122/3.

When this unit is in a reading mode, the writing clock, CR, enters frequency divider 93(6)/14 first. After the pulse period is selected by SW-M3, the pulses are fed into BD-M5 etc., through 08(2)/2, 32(2)/13, 04/9; and to counter 93(1)/11 through the same circuit.

When the whole system is switched on at the start of operations, 74/8 is reset by 13/8. At the start of each new writing cycle 74/8 is also reset by 75(2)/14.

Indication of ICs: for example, 121(1)/6 shows Type 74121, 1st IC-package, Pin No. 6. A particular unit in a multiple-unit-package is represented by just one of the pin numbers belonging to the unit.

Write-prohibiting circuit (Fig. 7)

When both tracks 7 and 8 of the tape reader are activated at the same time by a control code '11' (see Table 1), the writing clock is inhibited by 32(2)/11. In this state, only the tape reader and the temporary memory work normally, and the rest of the circuits including the SSR stay in the previous state; i.e. the word with code '11' is not stored.

Frequency dividers (Fig. 7)

Type 93 units have been used for all the frequency dividers. Frequency dividers (1) and (2) in Fig. 2 are combined in the actual circuit as shown in Fig. 7. 93(1) and 93(2) make a 1/100 divider, 93(3) makes 1/2, 1/4 and 1/8 dividers, and the combined circuits make 1/200, 1/400 and 1/800 dividers. The combined circuit of these and 08(1) with SW-M2 make the clock required for reading mode 0, 1 or 2.

Time-controlled demultiplexer and counters (Fig. 8)

'K signal' (see Fig. 2) for writing mode 1 or 2 is made up by combining two counters 93(4) and 93(5), a BCD decimal decoder 42, nine 4-16 line decoders 154(1) to 154(9), three 4-input NOR gates 40(1) to 40(3), and 140 AND gates 08(1) to 08(36). Among several possible arrangements, this combination has been used by taking account of the fan-out capability and the cost of the units.

In writing modes 1 and 2, all the counters and frequency dividers are reset at the start of each operation, by the signal from track 7 of the tape to 32(2)/10.

In writing mode 1, all the counters and one of the frequency dividers, 93(3), are reset when every 400 words are entered into the SSR, in addition to the start of the operation, by signals from 154(9)/14 to 32(2)/9; i.e. 200 resets per operation.

SSR, DAC and VCC (Fig. 9)

Fig. 9 shows the combined circuit of the SSR, DAC and VCC. 140 channels are identical. The first stage of each channel consists of three packages of 2511A (dual-type, 6 units in all; see Appendix for details). This type has a tri-state output for each unit which is controlled by digital signals fed into Pins 3 and 12, but these are kept permanently high by pull-up resistors in this design. Therefore, each unit is controlled only by 'K signal' (Pin 8) and 'REC signal' (Pin 1). A particular 'K signal' is fed into the 6 units in each channel in parallel. The ERC signal is fed into all the units in the system (840 units, or 480 pins) in parallel.

A 6-bit DAC, type MC1406, is used for a DAC in each channel, with the reference voltage of +2V (Pin 12). Pin 13 which is prepared for a temperature compensation resistor is earthed directly without a resistor. The output voltage is converted by a fixed resistor (220), and the voltage is fed into the following stage.

The VCC in each channel consists of half 747C. The input is divided into two branches: a 24K resistor for the signal input, and a 330K resistor, which is connected to +15V through SW-M5, for biasing LEDs in each channel. If the system is used for other purposes which do not require bias currents, SW-M5 should be switched off. The circuit has been designed to produce the output current of

Signal	4.0 mA maximum
Bias	8.0 mA constant

The output current is sampled by the 10Ω resistor, and this voltage is fed back to the input, so that the output current is independent from the load conditions, unless the load exceeds a certain value which is limited by the 747C and its power supply voltages.

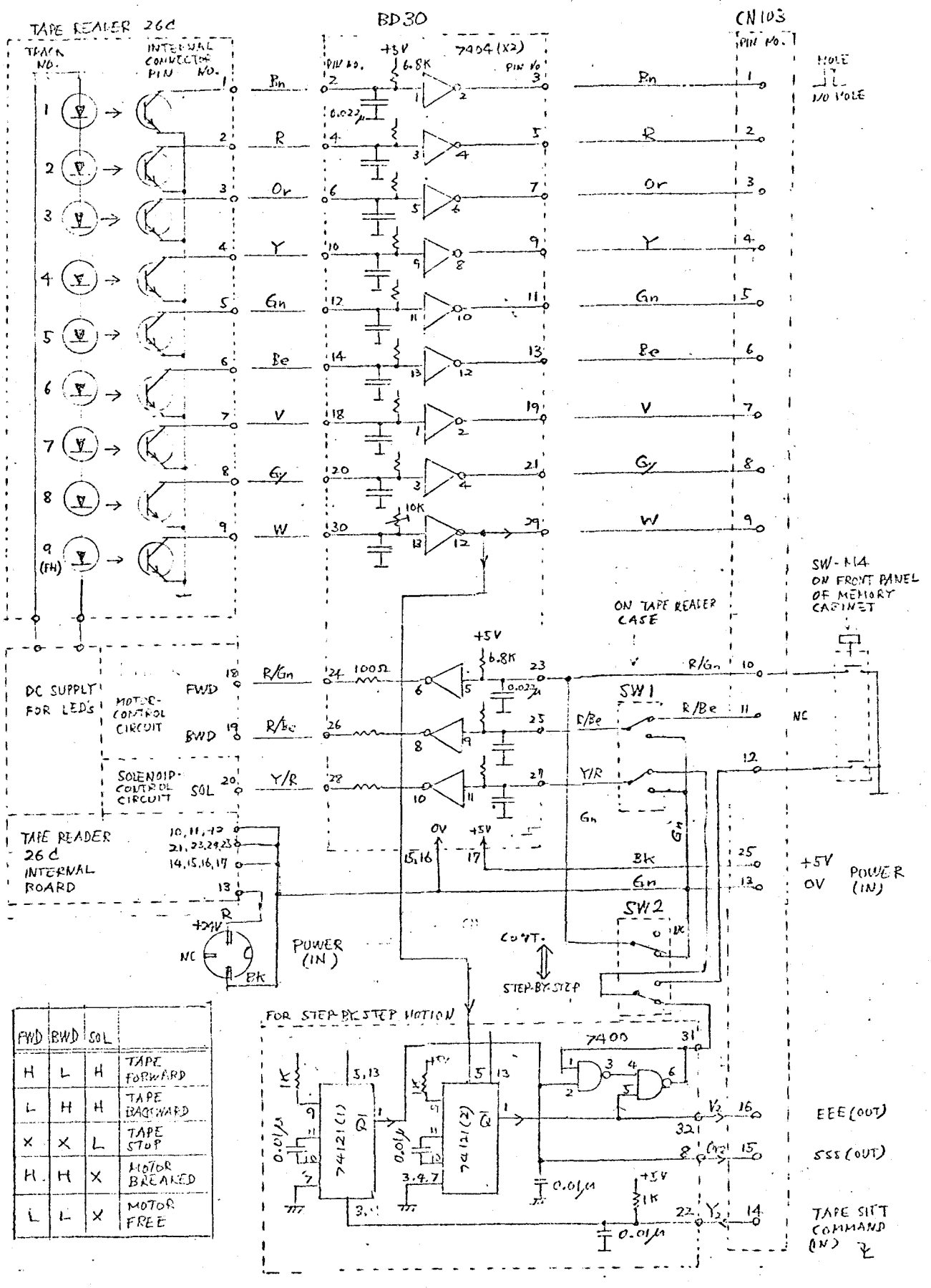
Note The output terminals of this circuit should not be kept open. Otherwise, high frequency oscillations will be generated, since the amplifier will be in an open-loop state. The terminals can be short-circuited, if not used.

Power supply (Fig. 10)

Fig. 10 shows the block diagram of the power supply for the input memory. Six different supply voltages, +5V, -5V, and -12V for the analogue circuits, and +12V, -12V, and +1.5V for the digital circuits, are required, other than +24V for the tape-driving motor, which is shared with the main control unit and contained in its cabinet.

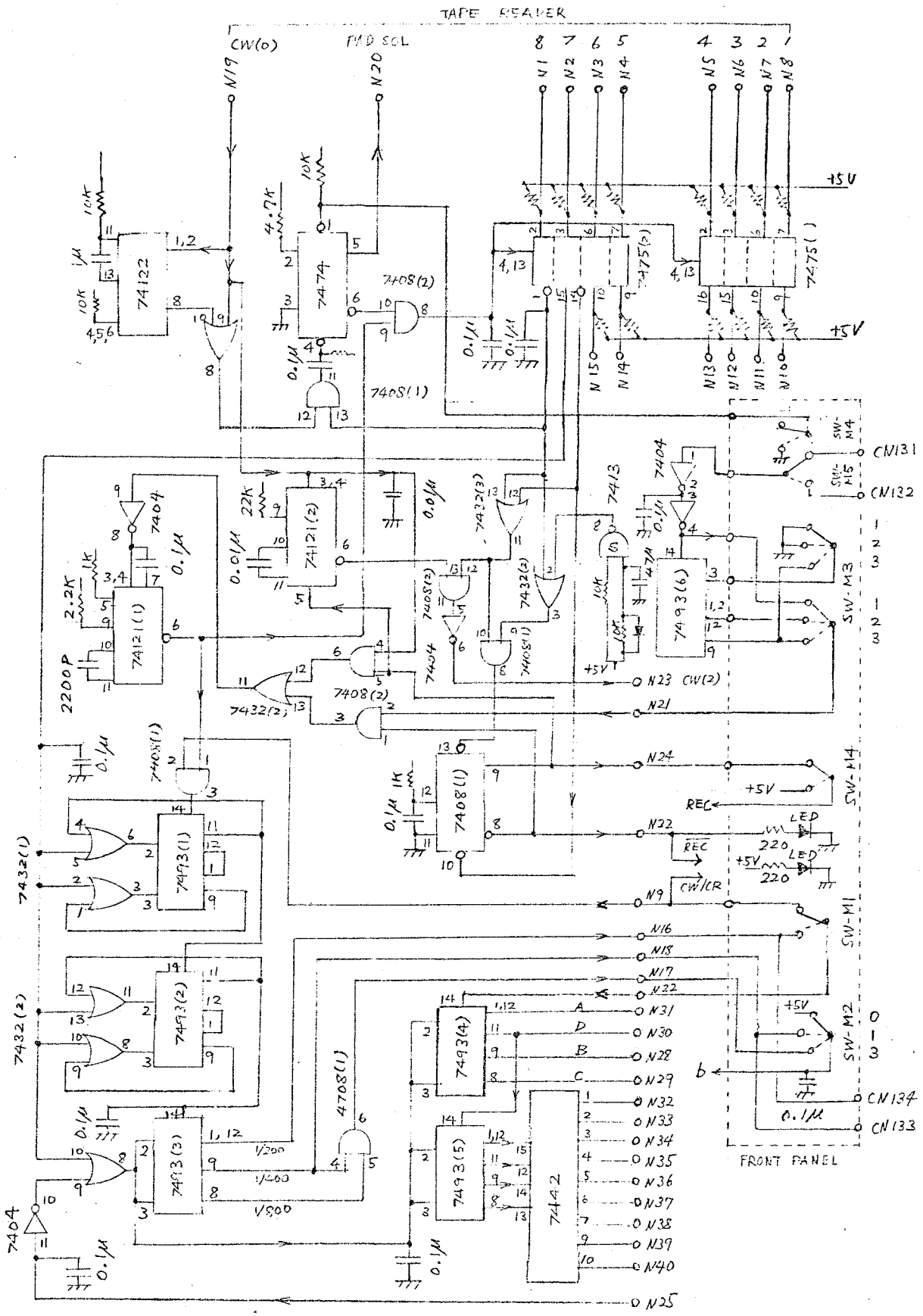
All the supply units, except for +1.5V which has been assembled for the purpose, have been chosen from standard products, with minor modifications. The choice was made in 1973 mainly for economical reasons, by sacrificing the physical compactness and electrical efficiency. (If these factors are problems, the power supply can be replaced, for example, by a switching regulator type). The maximum current required for each voltage is shown also in Fig. 10.

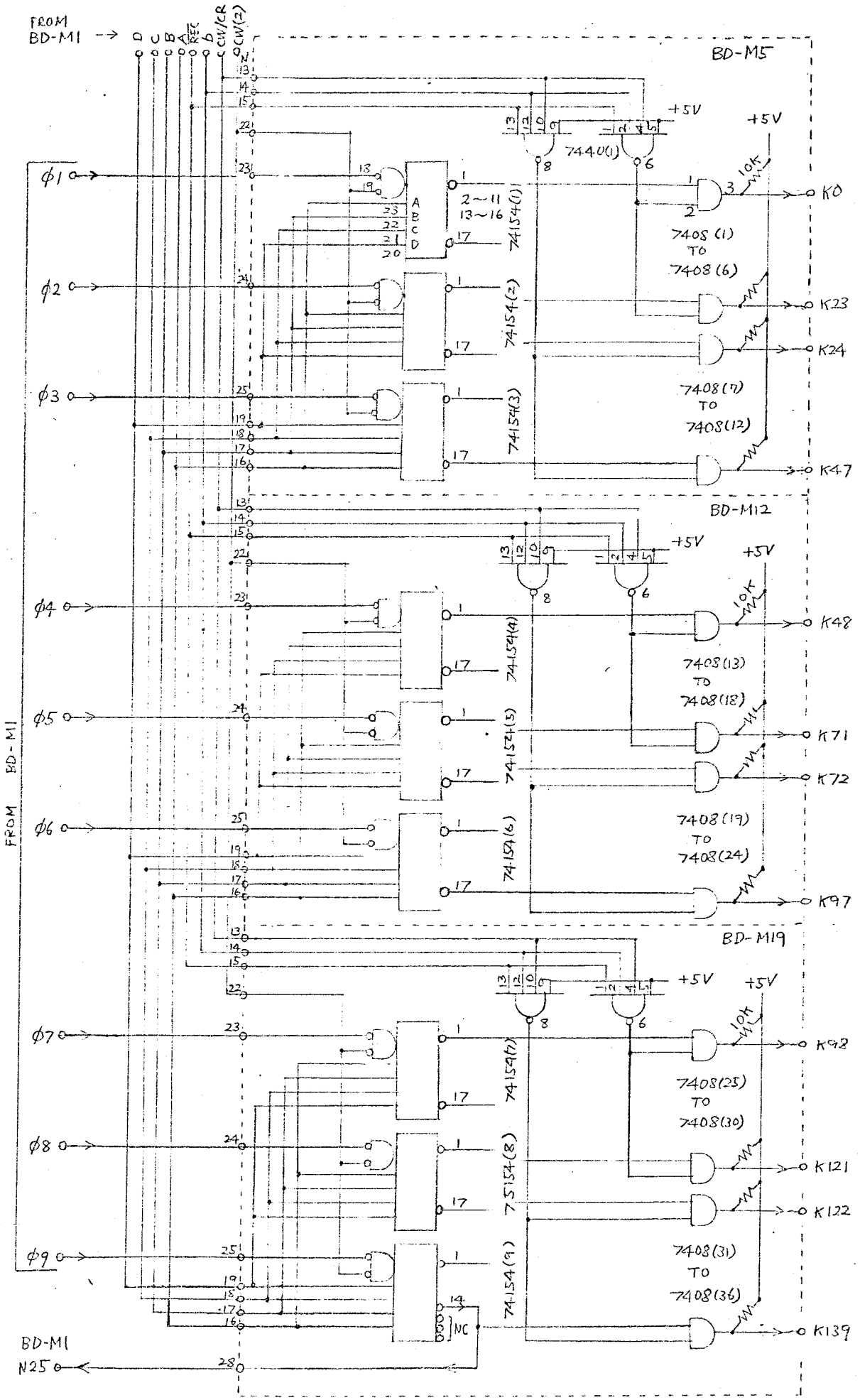
It is required to separate the input memory cabinet and the power supply cabinet by up to 2 m, for the arrangement of the control table. This imposes the need for each supply unit to have a four-line arrangement with the remote voltage-sensing. The sensing points are in the connector near to the memory cabinet, CN130. This arrangement can avoid the voltage rises of each power source when the connector is disconnected from the memory. Instead, a relatively large capacitor (or capacitors) is required to terminate each voltage-sensing point, in order to compensate for the inductance of the lead wires. Otherwise, high-frequency oscillations will be generated. In order to ensure adequate compensation, small capacitors had to be added to some supply lines inside the memory cabinet, at physically different points which were determined experimentally.



FWD	RWD	SOL	
H	L	H	TAPE FORWARD
L	H	H	TAPE BACKWARD
X	X	L	TAPE STOP
H	H	X	MOTOR BREAKED
L	L	X	MOTOR FREE

Fig. 6 Circuit diagram of the interface between the tape reader and input circuit.


TAPE REAVER
CW(0)
FWD SOL
N19
N20
8 7 6 5
4 3 2 1
N1 N2 N3 N4
N5 N6 N7 N8
+5V
74122
7474
7408(2)
7408(1)
7475( )
N15 N14 N13 N12 N11 N10
SW-M4
SW-M5
CN131
CN132
SW-M3
7404
7413
7493(6)
7421(1)
7421(2)
7432(2)
7408(1)
N23 CW(2)
N21
SW-M4
N24
REC
LED
220
N22
CW/CR
N9
SW-M1
N16
N18
N17
N22
SW-M2
CN134
CN133
FRONT PANEL
7493(1)
7493(2)
7493(3)
7493(4)
7493(5)
7442
N31
N30
N28
N29
N32
N33
N34
N35
N36
N37
N38
N39
N40
N25
0.1μ
0.01μ
2200P
22K
10K
4.7K
1K
1/200
1/400
1/800


FROM BD-M1
D
C
B
A
REC
CW/CR
CW(2)
BD-M5
BD-M12
BD-M19
+5V
7440(1)
10K
φ1
φ2
φ3
φ4
φ5
φ6
φ7
φ8
φ9
2~11
13~16
74154(1)
74154(2)
74154(3)
74154(4)
74154(5)
74159(6)
74159(7)
74154(8)
74154(9)
7408 (1) TO 7408 (6)
7408 (7) TO 7408(12)
7408(13) TO 7408(18)
7408(19) TO 7408(24)
7408(25) TO 7408(30)
7408(31) TO 7408(36)
K0
K23
K24
K47
K48
K71
K72
K97
K98
K121
K122
K139
NC
FROM BD-M1
BD-M1
N25

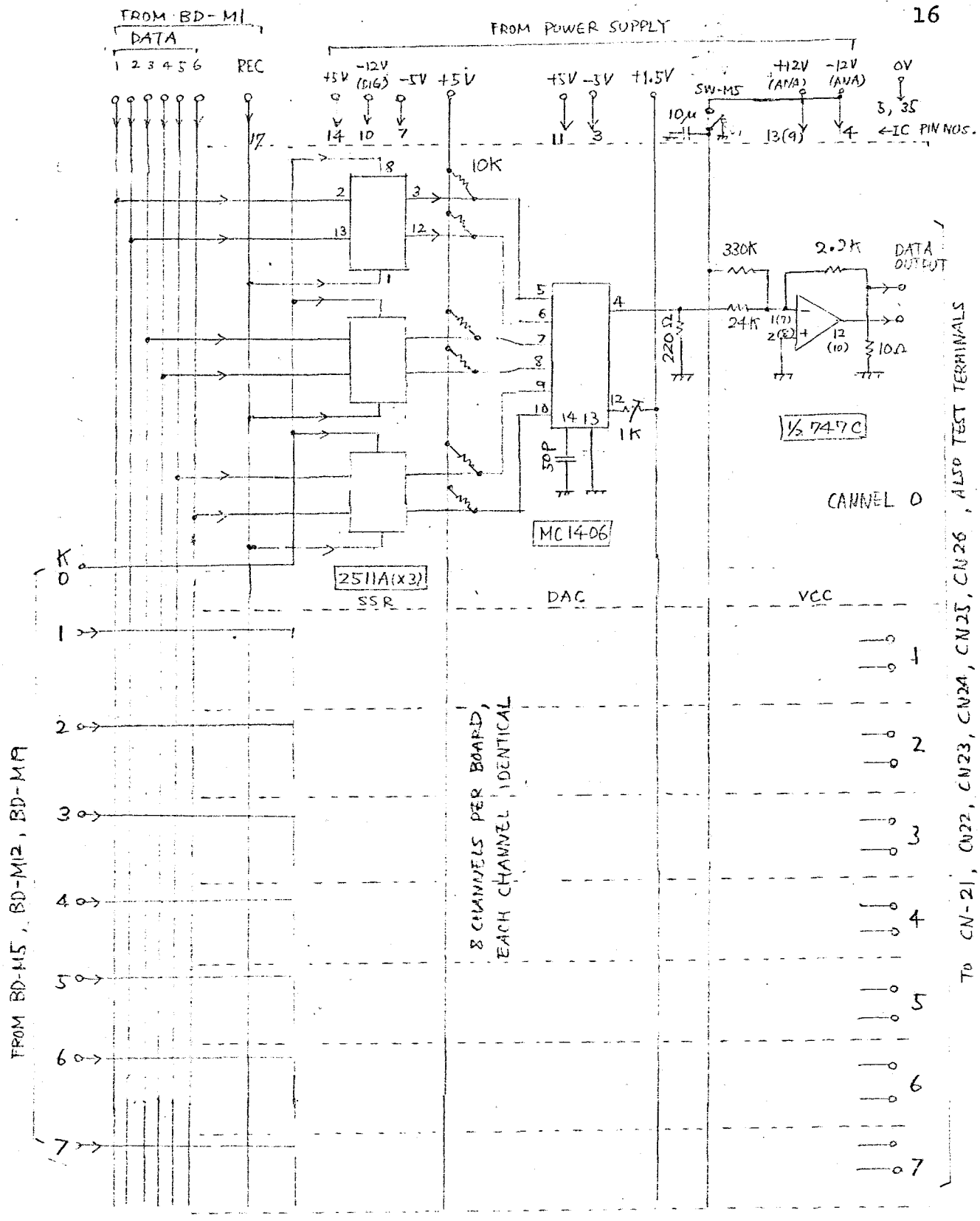
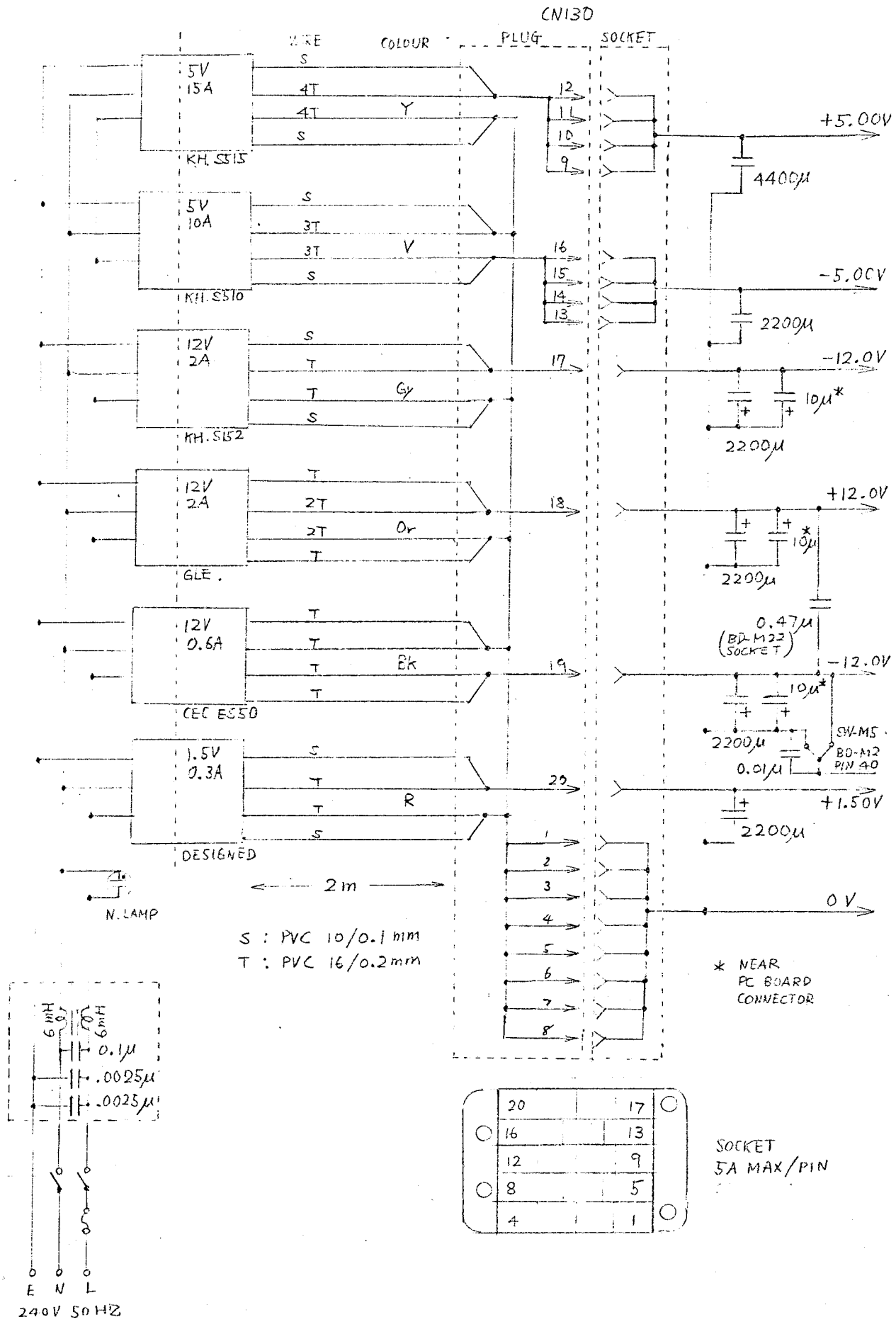
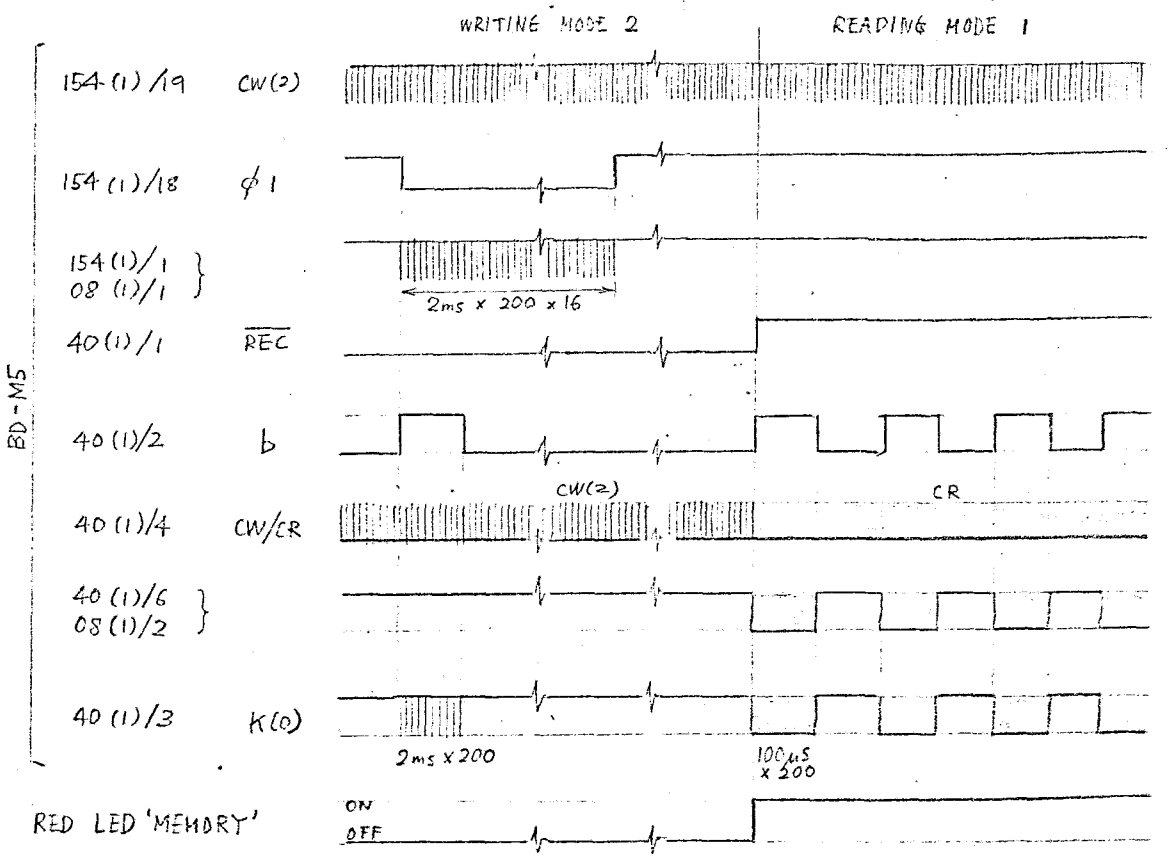


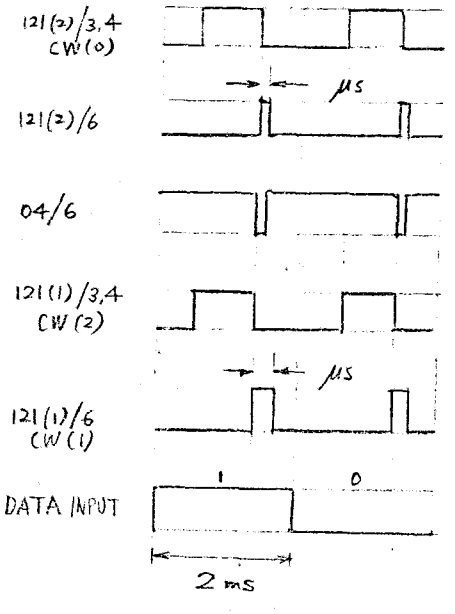
Fig. 9 Circuit diagram of BD-M2 to BD-M4, BD-M6 to BD-M11, BD-M13 to BD-M18, and BD-M20 to BD-M22 (18 boards are identical).


CN13D
WIRE
COLOUR
PLUG
SOCKET
5V 15A
KH. S515
5V 10A
KH. S510
12V 2A
KH. S512
12V 2A
GLE.
12V 0.6A
CEC ES50
1.5V 0.3A
DESIGNED
N. LAMP
2m
S : PVC 10/0.1 mm
T : PVC 16/0.2mm
+5.00V
4400μ
-5.00V
2200μ
-12.0V
10μ*
2200μ
+12.0V
10μ*
2200μ
0.47μ
(BD-M22 SOCKET)
-12.0V
10μ*
2200μ
SW-M5
BD-M2 PIN 40
0.01μ
+1.50V
2200μ
0 V
* NEAR PC BOARD CONNECTOR
0.1μ
.0025μ
.0025μ
E N L
240V 50HZ
20 17
16 13
12 9
8 5
4 1
SOCKET
5A MAX/PIN

TRANSIENT FROM WRITING MODE 2 TO READING MODE 1

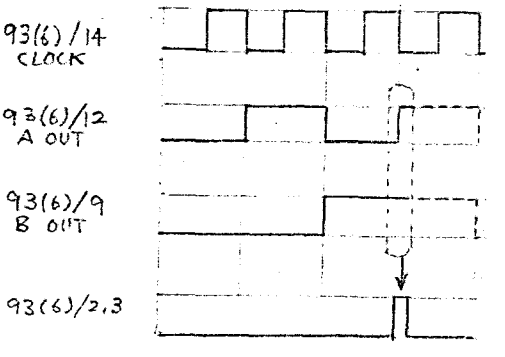


PULSE SHAPERS AND DATA INPUT



FREQUENCY DIVIDER FOR READING CLOCK

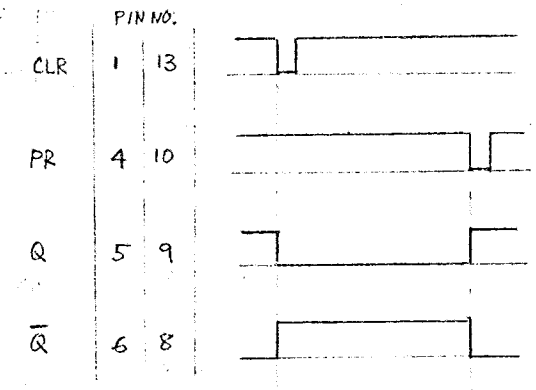
CW-M3, POSITION 3 ONLY SHOWN.



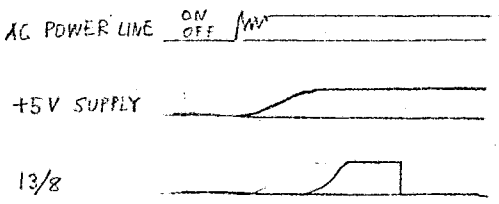
R1 93(6)/2	R2 93(6)/3	
0	X	COUNT
X	0	
1	1	RESET

Fig. 11 Timing diagrams of some parts of the input memory.

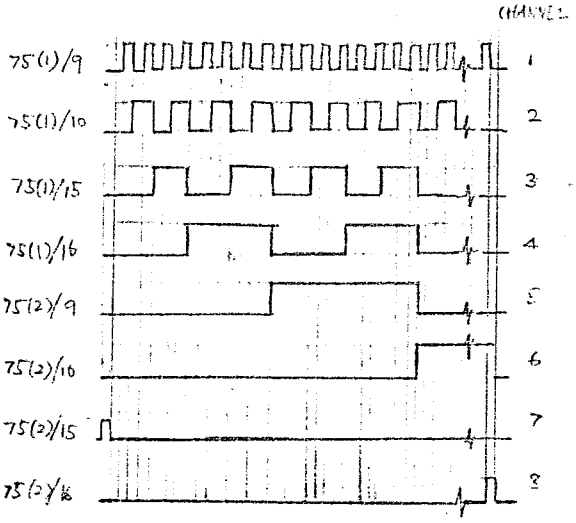
7474 (EACH UNIT)



INITIAL RESET

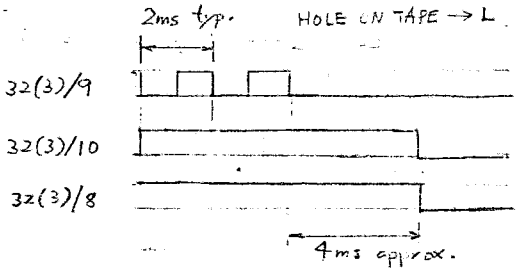


TEMPRARY MEMORY OUTPUT

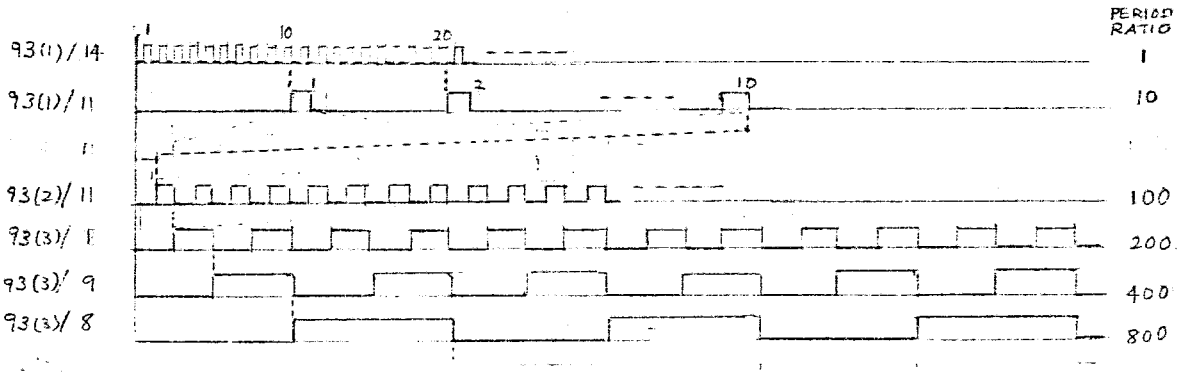


WHEN TEST TAPE M-1 IS USED

MOTOR-SPEED DETECTION



FREQUENCY DIVIDER



COUNTER

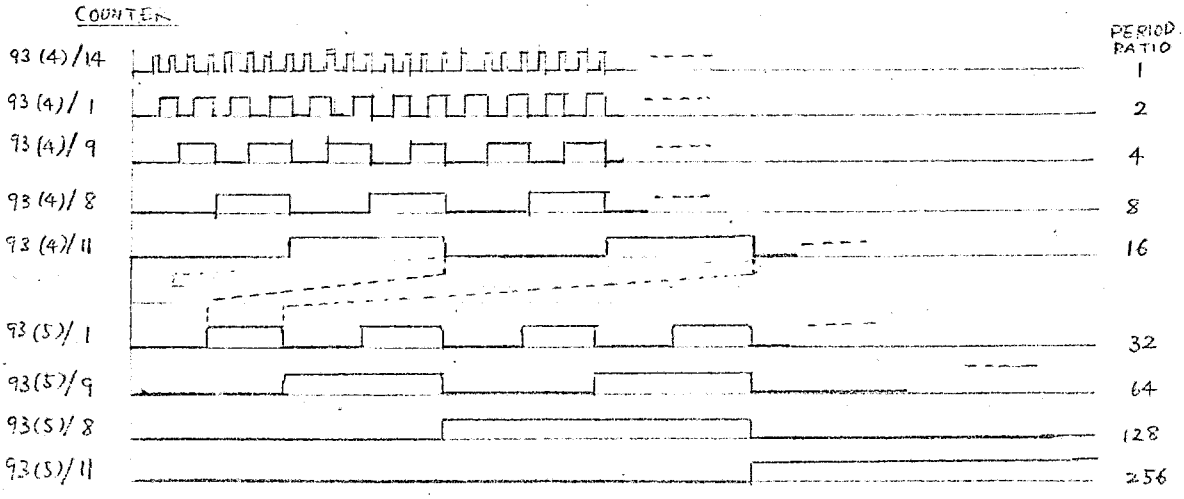


Fig. 11 (continued)

6. Physical design

The input memory is physically divided into three parts: the memory cabinet, power supply unit, and tape reader.

Memory cabinet

Fig. 13 shows the construction of the memory cabinet. Its details are shown in Appendix 2 (Figs. 14 to 21).

Fig. 29 (Appendix 4) shows a part of the front panel on which the controls and indicators are arranged. Fig. 14 shows the front inner-chassis and Fig. 15 shows its circuit diagram.

The front inner-chassis consists of

SW-M1	Writing mode selection
SW-M2	Reading mode selection
SW-M3	Reading period selection
SW-M4	Writing status
LED (Green)	Power on
LED (Red)	Data stored
Output monitoring terminals	

The output monitoring terminals are utilized, when the memory is used for plotting numerical maps, for selecting the sampling time of the maps (see Ref. 3).

Fig. 16 shows the rear view of the PC-board frame on which 22 edge connectors and six 50-pin connectors for the output are arranged. These are divided into three identical groups, except for a board, MD-M1, which has different construction. These wiring connections are shown in Appendix 2.

Fig. 17 shows the rear inner-chassis which contains connectors

CN103	From the tape reader
CN130	From the power supply
CN131	From the internal clock, CR-A
CN132	From an external clock, CR-B
CN133	To a CRO (1/200 of the clock)
CN134	To the numerical map plotter, through BD4
SW-M5	Clock selection, A or B
SW-M6	Bias current for opto-electronic couplers
Power supply voltage checking terminals	

This chassis also contains internally seven 22000 μF capacitors by which high-frequency oscillations associated with the long leads of the power supplies can be suppressed (their physical positions within the chassis are critical).

Fig. 18 shows the rear panel on which a fan (8 cm^2, 9-13 litres per second) is fixed, and the six output cable connectors are secured.

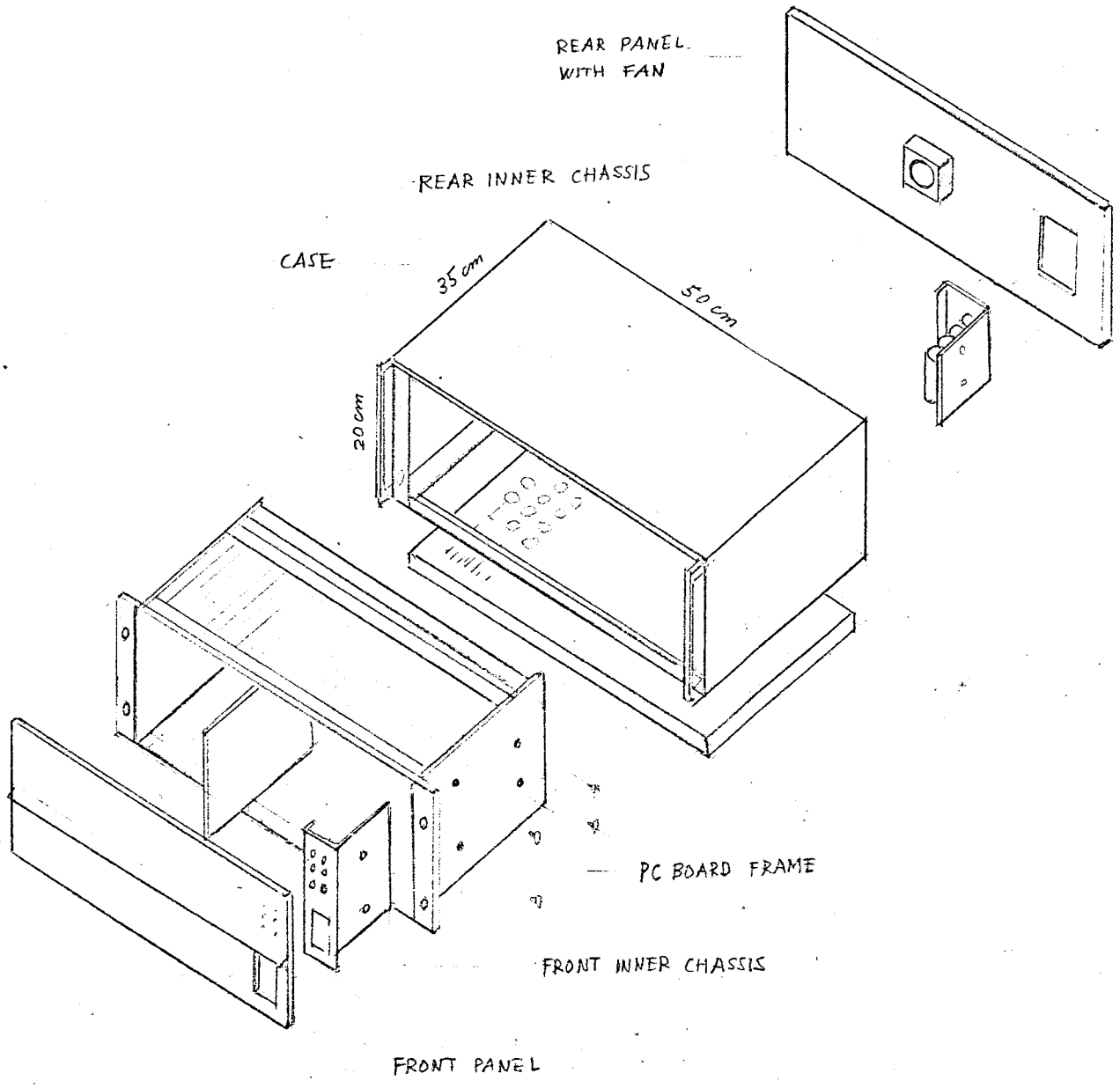


Fig. 12 Physical construction of the memory cabinet.
(see Appendix 1 for details)

Printed circuit boards

22 printed circuit boards which have three different constructions but all of uniform width (16 cm) are used.

BD-M1	Main part of the control circuit
BD-M5, BD-M12, BD-M19	Demultiplexers (three boards are identical)
BD-M2 to BD-M4 BD-M6 to BD-M11 BD-M13 to BD-M18 BD-M20 to BD-M22	SSRs, DACs, CCVs (18 boards are identical)

Figs. 19a, 19b, 19c, 20a, 20b and 21 show the physical designs of these printed circuit boards.

Power supply unit

All the power supplies for the input memory are contained in the control table, and cooled by a fan (12 cm^2, 50 litres per second). This unit and the memory cabinet are connected by a cable (2 m approx.).

7. Performance

Table 2 shows a summary of performance of the input memory. Fig. 13 shows an example of overall linearity from the digital input of the input memory to the analogue output of a floating circuit, though its opto-electronic coupler.

The temperature of the hottest components (integrated circuit packages of Type 2511A on BD-M2 etc., particularly those near the centre part of the cabinet) become higher than room temperature by about 22°C, with the fan in operation.

8. Conclusions

A semicondictor-circuit memory which satisfies particular requirements (a single channel digital input, 140 channel parallel output each of which has different time series of data in analogue and digital forms, with current driving facilities for up to 700 opto-electronic couplers, and internal facilities for converting the order of data) for the electronic model for tides and storm surges has been designed and constructed successfully.

This is an essential part of the model, and contributes to simplifying and speeding up the whole model operation. The cost of the memory (see Appendix 6 and Ref. 1) has been considered to be very reasonable in respect to its advantages.

Table 2 Summary of performance of the input memory

Input	Form of data	Mode 1: $F(t)_{x,y}$, or Mode 2: $F(x,y)_t$.
	Code — Data	Digital, parallel 6-bit 8421 code, 6 bits/word, one word/data.
	Code — Control	Digital, parallel 2-bit code. See Table 1.
	Channel	Parallel 8-bit single.
	Writing speed	0 to 2×10^5 words/s, including random intervals, depending on an external data, e.g. Speed of data reader (words/s) — Writing time for 28K w. 500 — 56 s 100,000 — 0.28 s
	Terminals	TTL logic.
Storage	Capacity	6-bit x 200 time-increments x 140 channels = 168K bits.
	Max. period	As long as power supply is continued.
Output	Form of data	Continuous $F(t)_{x,y}$
	Type	Analogue current, signal (2 mA pk-pk max.) + dc bias (10 mA), for driving LEDs (infra-red).
	Reading speed	0 to 10^6 words (equivalent)/s
	Repetition	All channels can be read in parallel, in synchronization and repetition, with intervals of zero (Mode 0), T (Mode 1) or 2T (Mode 2); where T is a duration of 200 words equivalent.
	Terminals	Current output (independent of external impedance) output impedance less than 10 for DC to 10 kHz.
Control	Programmed	Start, stop of writing and reading, and omission of wrong words etc.
	Manual	Selection of 2 writing modes, 3 reading modes, and the period of the reading clock.
Accuracy	Amplitude	Relative accuracy: max error $\pm$0.7% of full scale.
	Frequency	DC to 10 kHz (-3 db to 1 kHz)
Linearity		Better than 1% of full scale.
Stability	Temperature	Typically 0.002% per °C for DAC (0 to 40°C)
	Power line	1% against $\pm$10% input change
Power requirement		240V rms, 50 Hz, 250 W max.

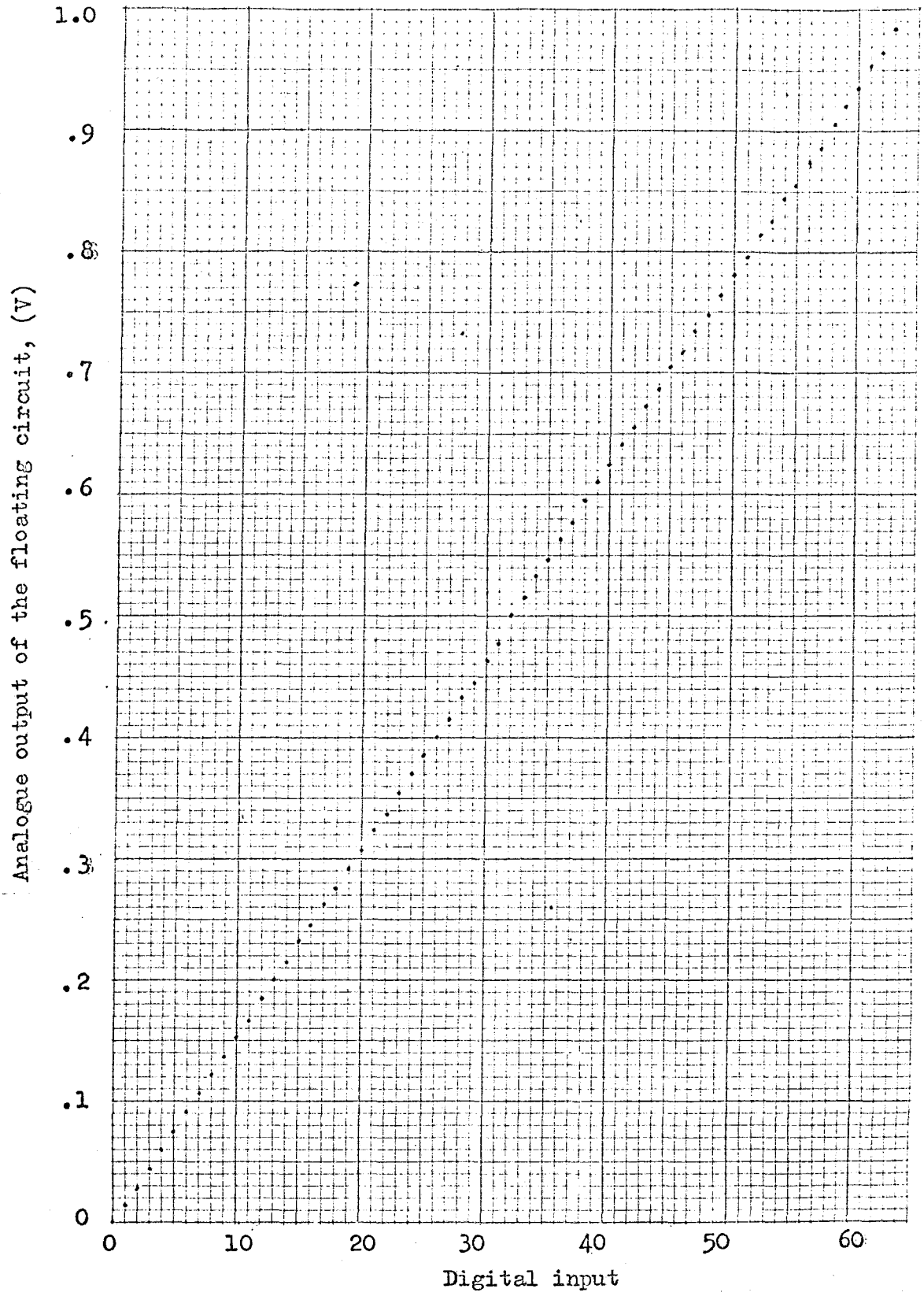


Fig. 13 Overall linearity from the digital input of the input memory to the analogue output of a floating circuit, through its opto-electronic coupler.
(The analogue output voltage was measured by a DVM having an accuracy of ± 0.1%).

Acknowledgement

The author would like to thank Mr J. Smithers for his considerable contributions in making the prototype of this memory, and adjusting and testing the actual memory.

References

(1) Ishiguro, S. (1972)
New electronic sea model,
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(2) Ishiguro, S. and Smithers, J. (1973)
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Numerical map plotter,
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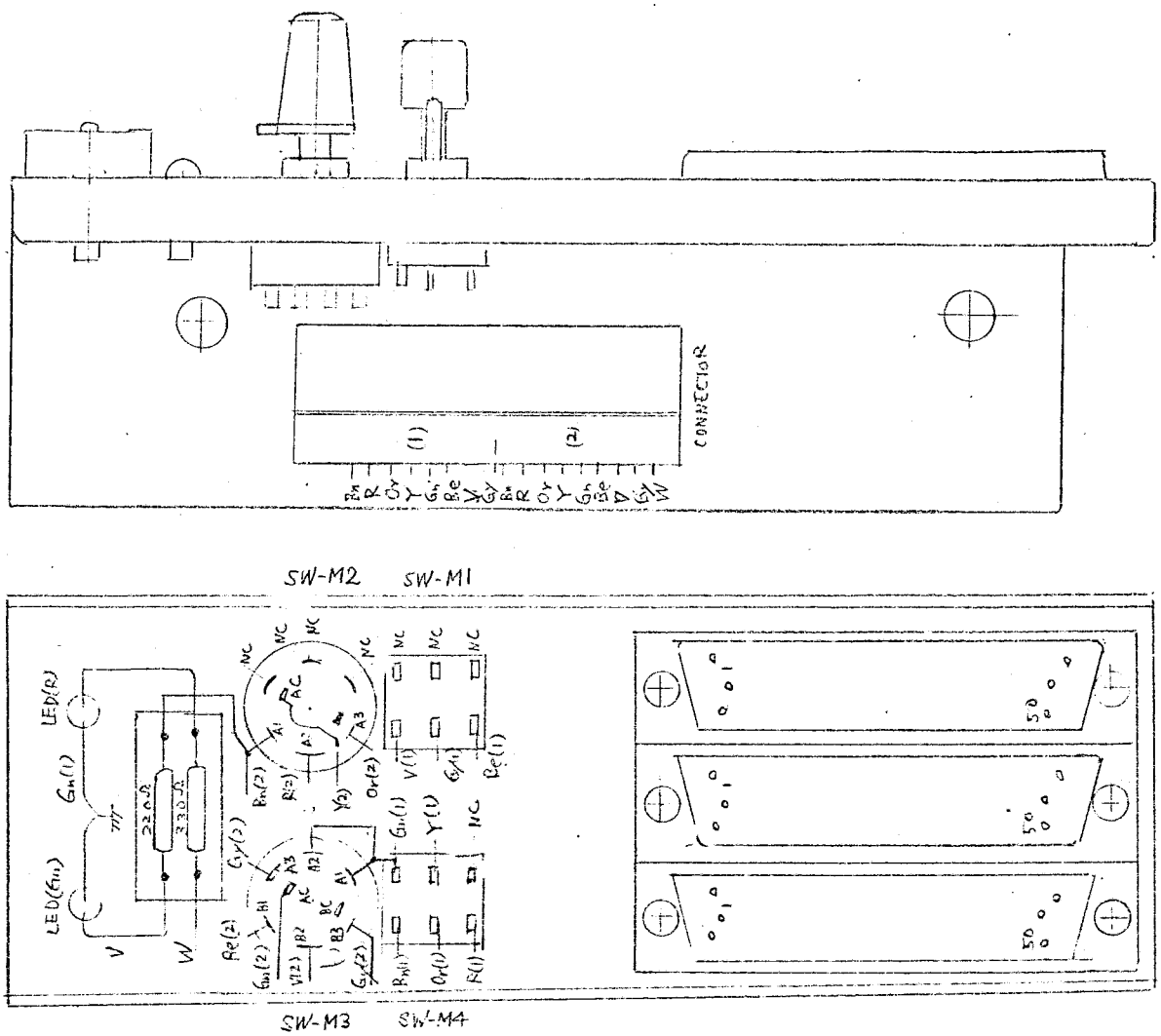


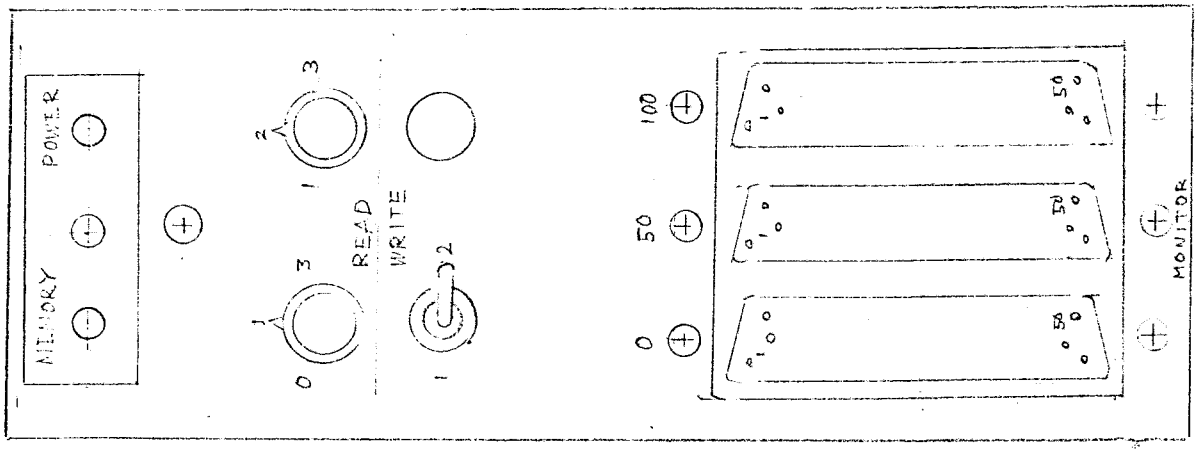


Fig. 14 Front inner-chassis (full scale)

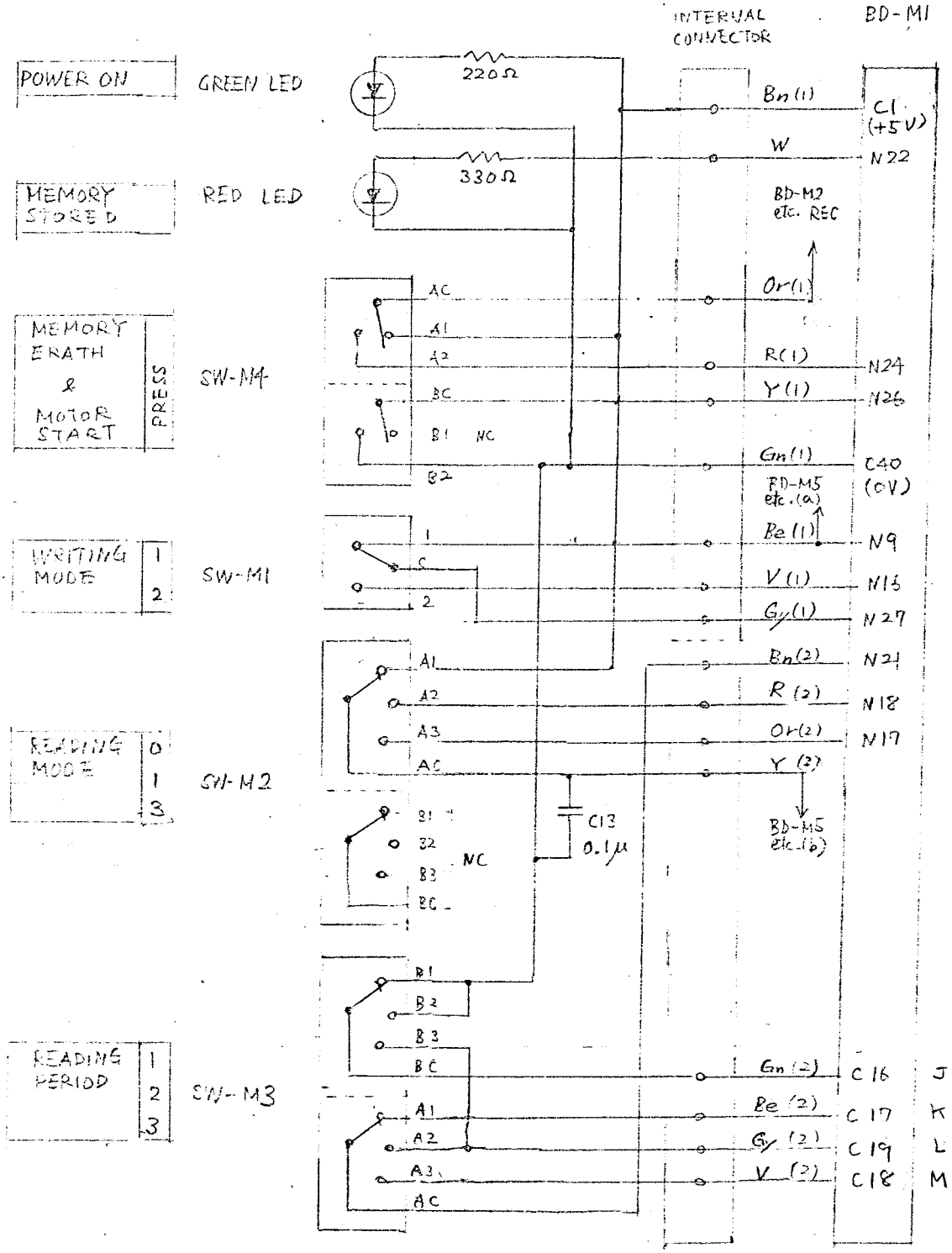
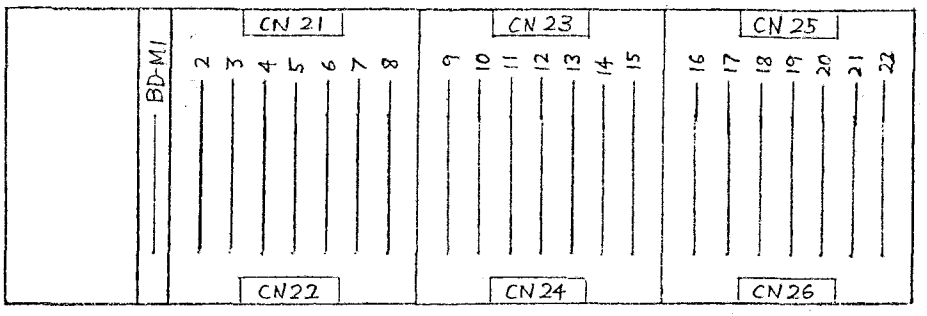


Fig. 15 Circuit diagram of the front inner-chassis



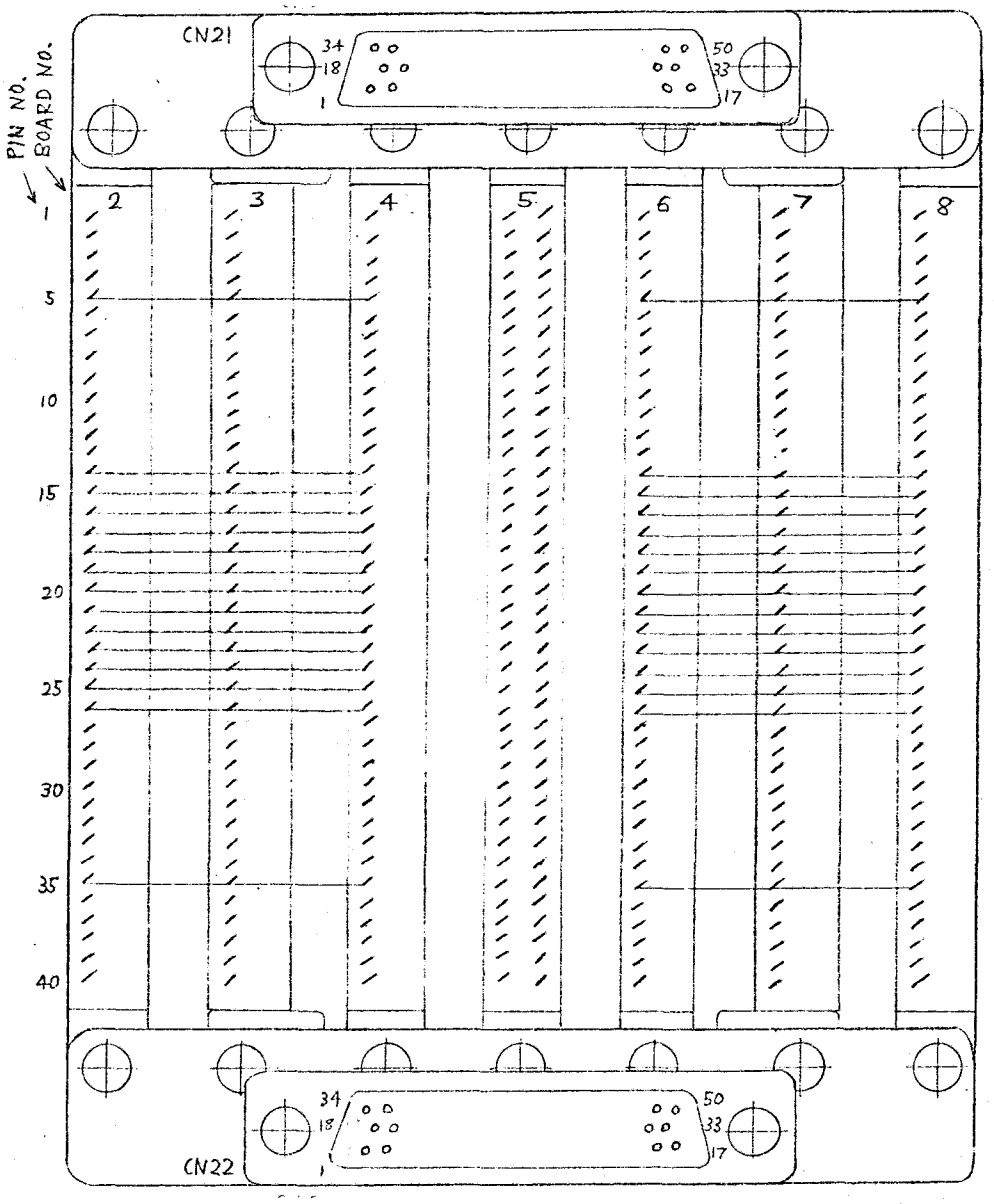


Fig. 16 (a) Rear view of the PC-board frame with the output connectors (schematic, arbitrary scale)
(b) Detailes of the first section of the frame containing BD-M2 to BD-M8 (full scale). The three sections are identical.

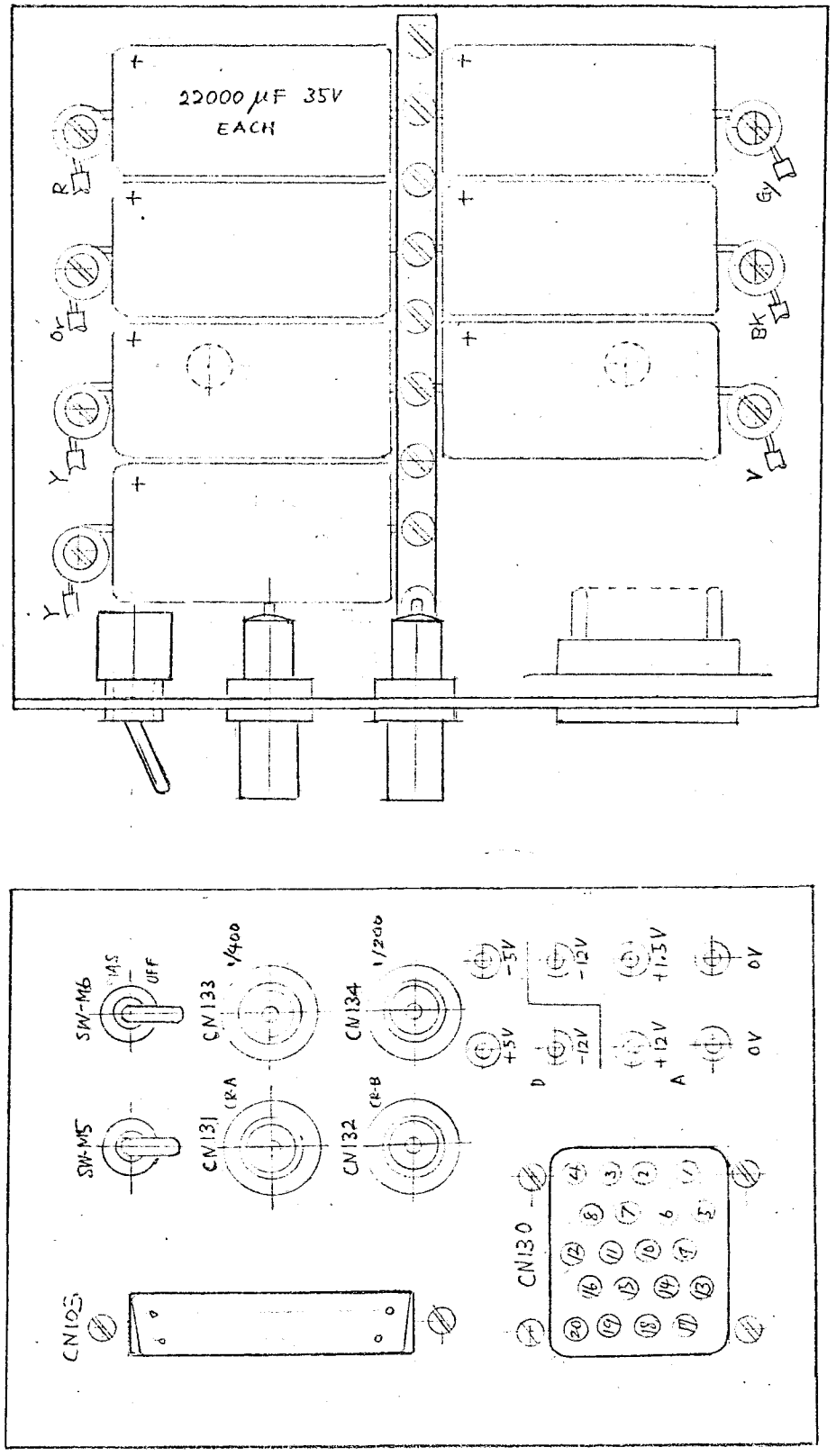


Fig. 17 Rear inner-chassis (full scale). See Fig. 10 for the circuit.

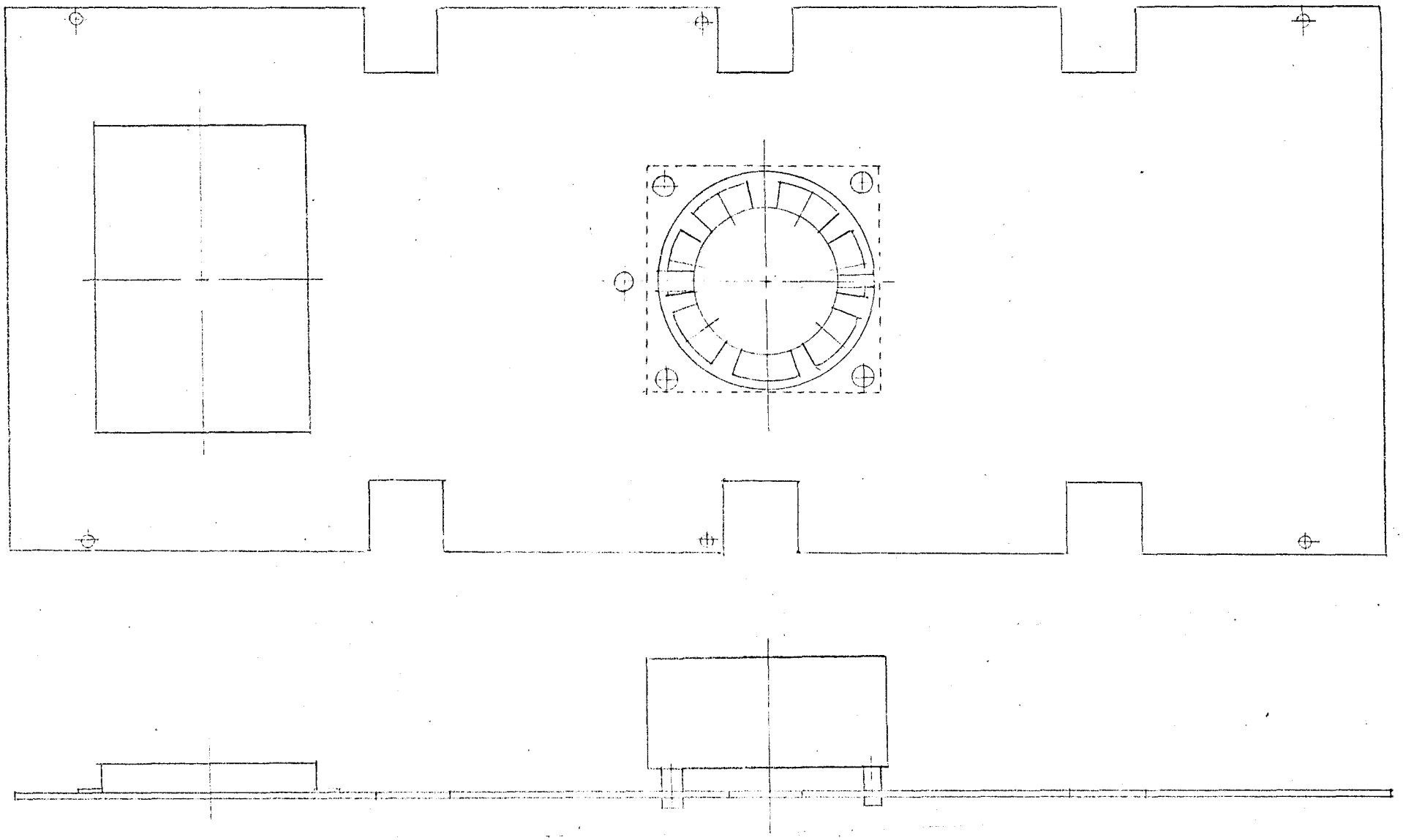


Fig. 18 Rear panel with a fan (scale $\frac{1}{2}$).

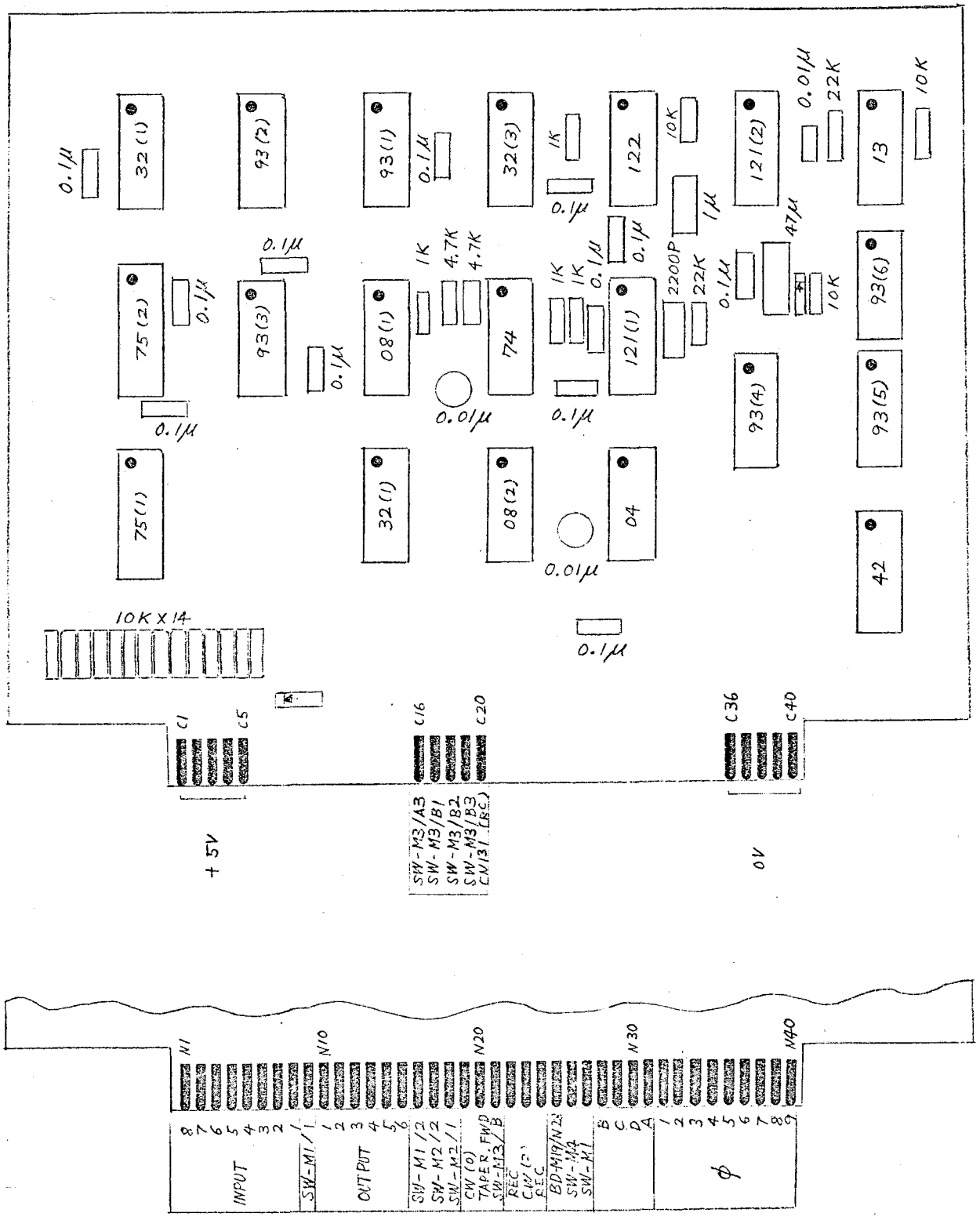


Fig. 19 Control circuit board.

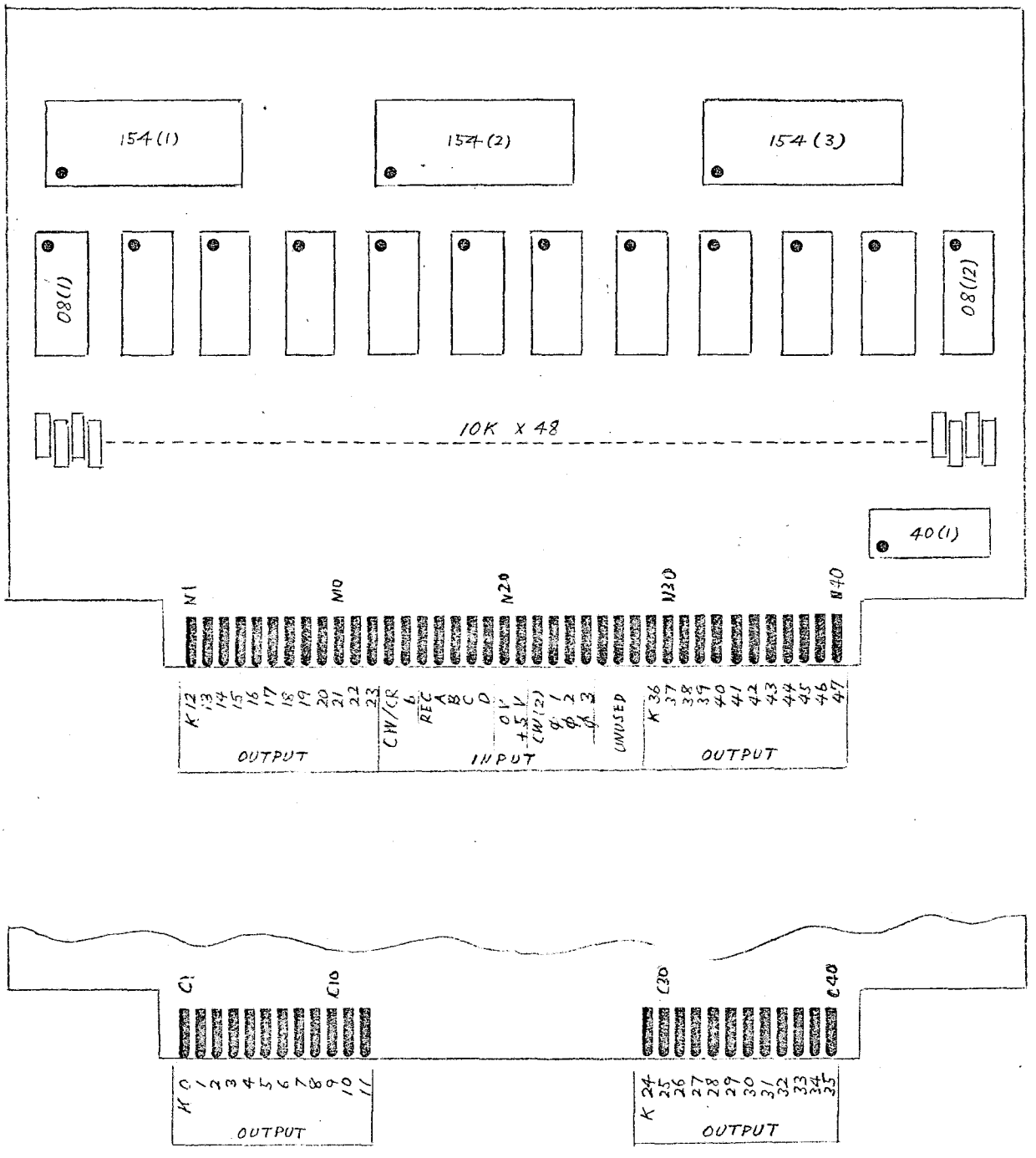


Fig. 20 Sub-control circuit board (3 boards identical).

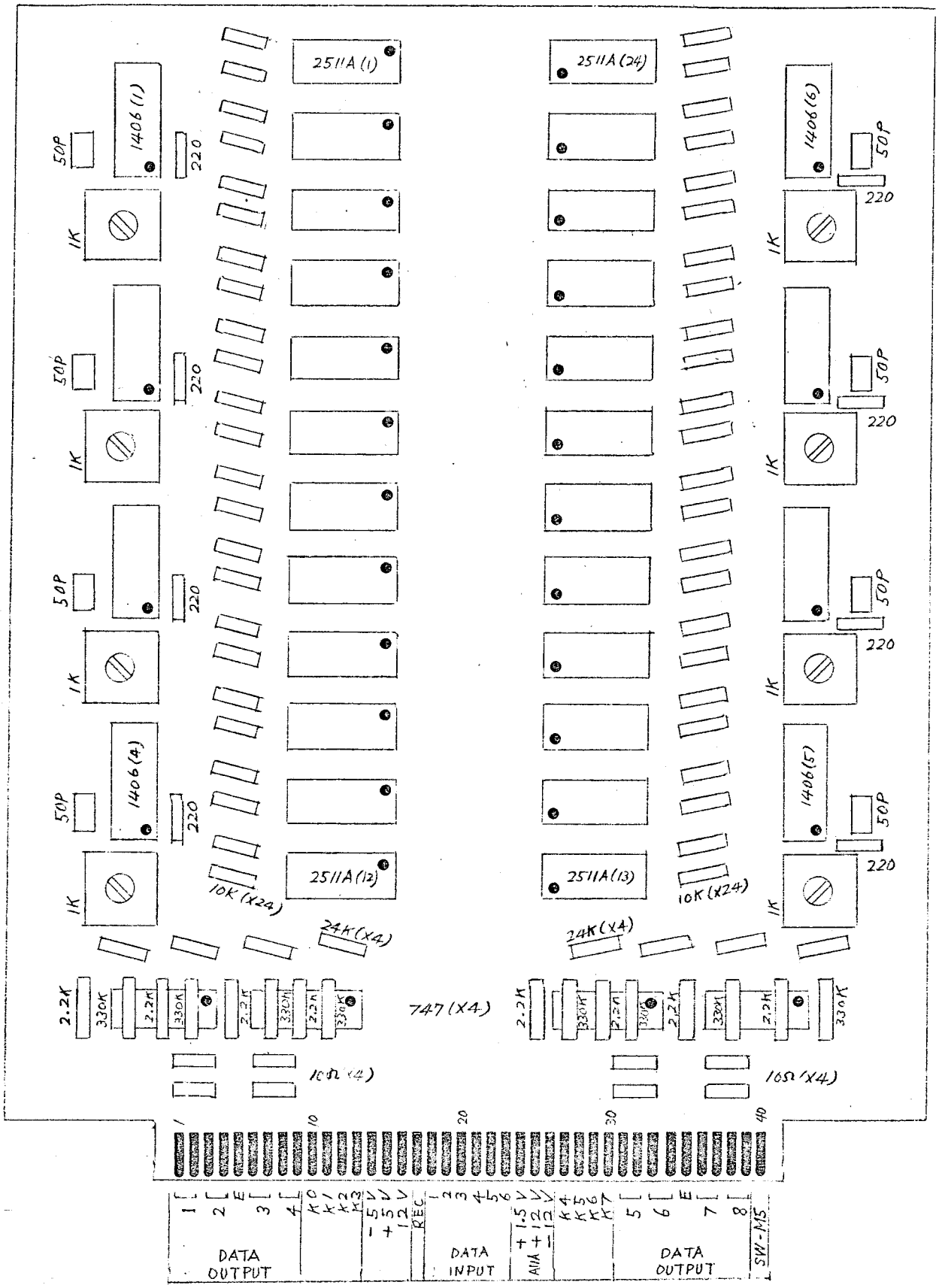


Fig. 21 Memory board (18 boards identical).

Appendix 2 Tables for internal connections

All the connections are permanent. These tables are necessary only for the construction of the instrument or its servicing.

Table 3 Connection between CN130 and circuit boards

Voltage	0V	+5V	-5V	-12V	+15V	-15V	+2V
CN130 Pin No.	1-8	9-12	13-16	17	18	19	20
Pin No. ↘							
BD-M1	c36-40	c1-5	-	-	-	-	-
BD-M2	35	15	14	17	26	25	24
BD-M3	35	15	14	17	26	25	24
BD-M4	35	15	14	17	26	25	24
BD-M5	c20	c21	-	-	-	-	-
BD-M6	35	15	14	17	26	25	24
BD-M7	35	15	14	17	26	25	24
BD-M8	35	15	14	17	26	25	24
BD-M9	35	15	14	17	26	25	24
BD-M10	35	15	14	17	26	25	24
BD-M11	35	15	14	17	26	25	24
BD-M12	c20	c21	-	-	-	-	-
BD-M13	35	15	14	17	26	25	24
BD-M14	35	15	14	17	26	25	24
BD-M15	35	15	14	17	26	25	24
BD-M16	35	15	14	17	26	25	24
BD-M17	35	15	14	17	26	25	24
BD-M18	35	15	14	17	26	25	24
BD-M19	c20	c21	-	-	-	-	-
BD-M20	35	15	14	16	26	25	24
BD-M21	35	15	14	16	26	25	24
BD-M22	35	15	14	16	26	25	24

For example, CN130 Pin Nos. 9 to 12 have the voltage of +5V, and connected to BD-M1 Component-side Pin Nos. 1 to 5. CN130 Pin 17 has the voltage of -12V, and connected to BD-M2 Non-component side Pin No. 17.

Table 4 Connection between BD-M1 and other parts

Function	BD-M1 Pin No.	Part connected	
Input 8	1	CN103/8	W
7	2	7	V
6	3	6	Be
5	4	5	Gn
4	5	4	Y
3	6	3	Or
2	7	2	R
1	8	1	Bn
CW/CR	9	SW-M1/1	Be(1)
Output 1	10	Pin 18	
2	11	Pin 19	
3	12	Pin 20	
4	13	Pin 21	
5	14	Pin 22	
6	15	Pin 23	
	16	SW-M1/2	V(1)
R Mode 2	17	SW-M2/A2	Or(2)
R Mode 3	18	SW-M2/A1	R(2)
FH	19	CN103/9	
FWD, SOL	20	CN103/10, CN103/12	
	21	SW-M3/B	Bn(2)
$\overline{\text{REC}}$	22	Pin 15	Or/Bn
(CW2) ϕW	23	Pin 22	Gy/Be
REC	24	Pin 17	
Reset	25	BD-M19/74154(9) Pin 14	Gy
Start	26	SW-M4	Y(1)
	27	SW-M1/C	Gy(1)
B	28	Pin 17	W/R
C	29	Pin 18	W/Or
D	30	Pin 19	W/Gy
A	31	Pin 16	W/Gn
ϕ1	32	BD-M5/23	Bn
ϕ2	33	BD-M5/24	R
ϕ3	34	BD-M5/25	Or
ϕ4	35	BD-M12/23	Y
ϕ5	36	BD-M12/24	Gn
ϕ6	37	BD-M12/25	Be
ϕ7	38	BD-M18/23	V
ϕ8	39	BD-M18/24	Gy
ϕ9	40	BD-M18/25	W
*	c1-c5	+5V	
	c16	SW-M3/A3	Gn(2)
	c17	SW-M3/B1	Be(2)
	c18	SW-M3/B2	V(2)
	c19	SW-M3/B3	Gy(2)
	c20		W/Bn

in each of BD-M2 to BD-M4, BD-M6 to BD-M11, BD-M13 to BD-M18, BD-M20 to BD-M22

in each of BD-M5, BD-M12, BD-M19

* c: Pin on the component side of the board.

Table 5 Connection between BD-M5, BD-M12 or BD-M19 and other connectors

Colour	BD-M5 pin No.		BD-M12 pin No.		BD-M19 pin No.		
Bn	1	M2/10	1	M9/10	1	M16/10	Non-component side
R	2	11	2	11	2	11	
Or	3	12	3	12	3	12	
Y	4	13	4	13	4	13	
Bn	5	M3/10	5	M10/10	5	M17/10	
R	6	11	6	11	6	11	
Or	7	12	7	12	7	12	
Y	8	13	8	13	8	13	
Bn	9	M4/10	9	M11/10	9	M18/10	
R	10	11	10	11	10	11	
Or	11	12	11	12	11	12	
Y	12	13	12	13	12	13	
Bn	29	M2/27	29	M9/27	29	M16/27	
R	30	28	30	28	30	28	
Or	31	29	31	29	31	29	
Y	32	30	32	30	32	30	
Bn	33	M3/27	33	M10/27	33	M17/27	
R	34	28	34	28	34	28	
Or	35	29	35	29	35	29	
Y	36	30	36	30	36	30	
Bn	37	M4/27	37	M11/27	37	M18/27	
R	38	28	38	28	38	28	
Or	39	29	39	29	39	29	
Y	40	30	40	30	40	30	
Bn	1	M6/10	1	M13/10	1	M20/10	Component side
R	2	11	2	11	2	11	
Or	3	12	3	12	3	12	
Y	4	13	4	13	4	13	
Bn	5	M7/10	5	M14/10	5	M21/10	
R	6	11	6	11	6	11	
Or	7	12	7	12	7	12	
Y	8	13	8	13	8	13	
Bn	9	M8/10	9	M15/10	9	M22/10	
R	10	11	10	11	10	11	
Or	11	12	11	12	11	12	
Y	12	13	12	13	12	13	
Bn	29	M6/27	29	M13/27	29	M20/27	
R	30	28	30	28	30	28	
Or	31	29	31	29	31	29	
Y	32	30	32	30	32	30	
Bn	33	M7/27	33	M14/27	33	M21/27	
R	34	28	34	28	34	28	
Or	35	29	35	29	35	29	
Y	36	30	36	30	36	30	
Bn	37	M8/27	37	M15/27	37	M22/27	
R	38	28	38	28	38	28	
Or	39	29	39	29	39	29	
Y	40	30	40	30	40	30	

For example, BD-M5 Pin No. 1 is connected to BD-M2 Pin No. 10 by the Brown wire.

Table 6 Connection between the output terminals and each of BD-M2 to BD-M4, BD-M6 to BD-M11, BD-M13 to BD-M18, and BD-M20 to BD-M22.

	Pin No	CN21	CN22	CN23	CN24	CN25	CN26
Bn	1	M2/1	M2/31	M9/1	M9/31	M16/1	M16/31
R	2	2	32	2	32	2	32
Or	3	3	33	3	33	3	33
Y	4	4	34	4	34	4	34
Gn	5	6	36	6	36	6	36
Be	6	7	37	7	37	7	37
V	7	8	38	8	38	8	38
Gy	8	9	39	9	39	9	39
Bn	10	M6/1	M6/31	M13/1	M13/31	M20/1	M20/31
R	11	2	32	2	32	2	32
Or	12	3	33	3	33	3	33
Y	13	4	34	4	34	4	34
Gn	14	6	36	6	36	6	36
Be	15	7	37	7	37	7	37
V	16	8	38	8	38	8	38
Gy	17	9	39	9	39	9	39
Bn	18	M3/1	M3/31	M10/1	M10/31	M17/1	M17/31
R	19	2	32	2	32	2	32
Or	20	3	33	3	33	3	33
Y	21	4	34	4	34	4	34
Gn	22	6	36	6	36	6	36
Be	23	7	37	7	37	7	37
V	24	8	38	8	38	8	38
Gy	25	9	39	9	39	9	39
Bn	26	M7/1	M7/31	M14/1	M14/31	M21/1	M21/31
R	27	2	32	2	32	2	32
Or	28	3	33	3	33	3	33
Y	29	4	34	4	34	4	34
Gn	30	6	36	6	36	6	36
Be	31	7	37	7	37	7	37
V	32	8	38	8	38	8	38
Gy	33	9	39	9	39	9	39
Bn	34	M4/1	M4/31	M11/1	M11/31	M18/1	M18/31
R	35	2	32	2	32	2	32
Or	36	3	33	3	33	3	33
Y	37	4	34	4	34	4	34
Gn	38	6	36	6	36	6	36
Be	39	7	37	7	37	7	37
V	40	8	38	8	38	8	38
Gy	41	9	39	9	39	9	39
Bn	43	M8/1	M8/31	M15/1	M15/31	M22/1	M20/31
R	44	2	32	2	32	2	32
Or	45	3	33	3	33	3	33
Y	46	4	34	4	34	4	34
Gn	47	6	36	6	36	6	36
Be	48	7	37	7	37	7	37
V	49	8	38	8	38	8	38
Gy	50	9	39	9	39	9	39

For example, CN21 Pin No. 1 is connected to BD-M2 Pin No. 1, by Brown wire.

Table 7 Conection between Tape reader 26C and the input memory through CN103

Function	BD30 Pin No.	Cable (Gy)	CN103 Pin No.	Memory internal
Data channel 1	3	Bn	1	Bn
2	5	R	2	R
3	7	Or	3	Or
4	9	Y	4	Y
5	11	Gn	5	Gn
6	13	Be	6	Be
Control channel 7	19	V	7	V
8	21	Gy	8	Gy
FH (Tape feed hole)	29	W	9	W
FWD (Tape forward)	23	R/Gn	10	Y/R *
BWD (Tape backward)	25	R/Be	11	R/Be
SOL (Clutch solenoid)	27	Y/Be	12	Y/R *
Common (OV)	15-16	Gn(D)+Pk	13	W(T)
+5V	17	Bk	25	Y
Screen	10-12, 21-25	-		

* Connected

Table 8 Conection between Tape reader 26C and the contol cabinet

Function	Tape-reader internal connector Pir No.	Cable (W)	CN16 Pin No.
Motor drive, +24V	13	R	L
Common, OV	14-17	Bk	N
Screen	10-12, 21-25	-	-

Table 9 Connection between BD30 and the internal connector of Tape reader 26C

Function	Tape reader internal connector Pin No.	Cable (Pink)	BD30 Pin No.
Data track 1	1	Bn	2
2	2	R	4
3	3	Or	6
4	4	Y	10
5	5	Gn	12
6	6	Be	14
Control track 7	7	V	18
8	8	Gy	20
FH	9	W	30
FWD	18	R/Gn	24
BWD	19	R/Be	26
SOL	20	Y/R	28
Common (OV)	10-12, 21-25	Gn	14-15

Table 10 Memory channel No., Output channel No., and Monitoring terminal No.

1 The memory is written automatically in the order of Memory channel No.

2 The Memory channel No. is indicated at the end of each peir of wires inside the main network cabinet.

3 Each Monitoring terminal is connected to the first pin of each Output channel, and the same wire colour is used.

4 Pin Nos. 9 and 42 of each Output terminal are not used.

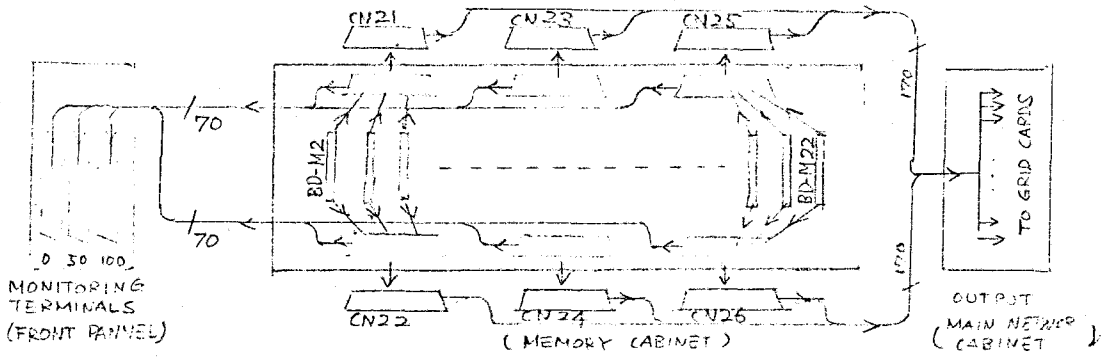


Fig. 22 Key diagram for tables

Memory channel No.	Output terminal: Pin No.	Wire colour	Connector	Circuit board No.	Monitoring terminal No.
0	1-2	Bn-R	CN21	BD-M2	(100) 40
1	3-4	Or-Y			(0) 1
2	5-6	Gn-Be			2
3	7-8	V -Gy			3
4	18-19	Bn-R		BD-M3	4
5	20-21	Or-Y			5
6	22-23	Gn-Be			6
7	24-25	V -Gy			7
8	34-35	Bn-R		BD-M4	8
9	36-37	Or-Y			9
10	38-39	Gn-Be			10
11	40-41	V -Gy			11
12	10-11	Bk-Bn		BD-M6	12
13	12-13	R - Or			13
14	14-15	Y -Gn			14
15	16-17	Bn-R			15
16	26-27	W -Bk		BD-M7	16
17	28-29	Bn-R			17
18	30-31	Or-Y			18
19	32-33	Gn-Or			19
20	43-44	Bk-Bn		BD-M8	20
21	45-46	R -Or			21
22	47-48	Y -Gn			22
23	49-50	Y -Gn			23

Memory channel No.	Output terminal			Circuit board No.	Monitoring terminal No.
	Pin No.	Wire colour	Connector		
24	10-11	Bk-Bn	CN22	BD-M6	(0) 24
25	12-13	R - Or			25
26	14-15	Y -Gn			26
27	16-17	Bn-R			27
28	26-27	W -Bn		BD-M7	28
29	28-29	Bn-R			29
30	30-31	Or-Y			30
31	32-33	Gn-Or			31
32	43-44	Bk-Bn		BD-M8	32
33	45-46	R -Or			33
34	47-48	Y -Gn			34
35	49-50	Y -Gn			35
36	1-2	Bn-R		BD-M2	36
37	3-4	Or-Y			37
38	5-6	Gn-Be			38
39	7-8	V -Gy			39
40	18-19	Bn-R		BD-M3	40
41	20-21	Or-Y			41
42	22-23	Gn-Be			42
43	24-25	V -Gy			43
44	34-35	Bn-R		BD-M4	44
45	36-37	Or-Y			45
46	38-39	Gn-Be			46
47	40-41	V -Gy			47
48	1-2	Bn-R	CN23	BD-M9	48
49	3-4	Or-Y			49
50	5-6	Gn-Be			50
51	7-8	V -Gy			(50) 1
52	18-19	Bn-R		BD-M10	2
53	20-21	Or-Y			3
54	22-23	Gn-Be			4
55	24-25	V -Gy			5
56	34-35	Bn-R		BD-M11	6
57	36-37	Or-Y			7
58	38-39	Gn-Be			8
59	40-41	V -Gy			9
60	10-11	Bk-Bn		BD-M13	10
61	12-13	R - Or			11
62	14-15	Y -Gn			12
63	16-17	Bn-R			13
64	26-27	W -Bk		BD-M14	14
65	28-29	Bn-R			15
66	30-31	Or-Y			16
67	32-33	Gn-Or			17
68	43-41	Bk-Bn		DB-M15	18
69	45-46	R -Or			19
70	47-48	Y -Gn			20
71	49-50	Y -Gn			21

Memory channel No.	Output terminal			Circuit board No.	Monitoring terminal No.
	Pin No.	Wire colour	Connector		
72	10-11	Bk-Bn	CN24	BD-M13	(50) 22
73	12-13	R -Or			23
74	14-15	Y -Gn			24
75	16-17	Bn-R			25
76	26-27	W -Bk		BD-M14	26
77	28-29	Bn-R			27
78	30-31	Or-Y			28
79	32-33	Gn-Or			29
80	43-44	Bk-Bn		BD-M15	30
81	45-46	R -Or			31
82	47-48	Y -Gn			32
83	49-50	Y -Gn			33
84	1-2	Bn-R		BD-M9	34
85	3-4	Or-Y			35
86	5-6	Gn-Be			36
87	7-8	V -Gy			37
88	18-19	Bn-R		BD-M10	38
89	20-21	Or-Y			39
90	22-23	Gn-Be			40
91	24-25	V -Gy			41
92	34-35	Bn-R		BD-M11	42
93	36-37	Or-Y			43
94	38-39	Gn-Be			44
95	40-41	V -Gy			45
96	1-2	Bn-R	CN25	BD-M16	46
97	3-4	Or-Y			47
98	5-6	Gn-Be			48
99	7-8	V -Gy			49
100	18-19	Bn-R		BD-M17	50
101	20-21	Or-Y			(100) 1
102	22-23	Gn-Be			2
103	24-25	V -Gy			3
104	34-35	Bn-R		BD-M18	4
105	36-37	Or-Y			5
106	38-39	Gn-Be			6
107	40-41	V -Gy			7
108	10-11	Bk-Bn		BD-M20	8
109	12-13	R -Or			9
110	14-15	Y -Gn			10
111	16-17	Bn-R			11
112	26-27	W -Bk		BD-M21	12
113	28-29	Bn-R			13
114	30-31	Or-Y			14
115	32-33	Gn-Or			15
116	43-44	Bk-Bn		BD-M22	16
117	45-46	R -Or			17
118	47-48	Y -Gn			18
119	49-50	Y -Gn			19

Memory channel No.	Output terminal Pin. No.	Wire colour	Connector	Circuit board No.	Monitering terminal No.
120	10-11	Bk-Bn	CN26	BD-M20	(100) 20
121	12-13	R -Or			21
122	14-15	Y -Gn			22
123	16-17	Bn-R			23
124	26-27	W -Bk		BD-M21	24
125	28-29	Bn-R			25
126	30-31	Or-Y			26
127	32-33	Gn-Or			27
128	43-44	Bk-Bn		BD-M22	28
129	45-46	R -Or			29
130	47-48	Y -Gn			30
131	49-50	Y -Gn			31
132	1-2	Bn-R		BD-M16	32
133	3-4	Or-Y			33
134	5-6	Gn-Be			34
135	7-8	V -Gy			35
136	18-19	Bn-R		BD-M17	36
137	20-21	Or-Y			37
138	22-23	Gn-Be			38
139	24-25	V -Gy			39
-	34-41	Not used			

Function		Monitoring terminal No.
Tape reader output, channel	1	(100) 41
	2	42
	3	43
	4	44
	5	45
	6	46
	7	47
	8	48
Writing clock	(W)	49
Reading clock	(Bk)	50

Note Signals can be observed at the monitoring terminals, only when the output terminals are connected to the loads, or short-circuited.

Appendix 3 Initial adjustments and tests

The initial adjustments and tests of the input memory are necessary only when it is built or some of its components (mainly those in its analogue circuits) are replaced.

Note Each circuit board can be pulled out by applying a simple extraction tool to the hole on the board (near the edge opposite to the connector).

Without connecting BD-M19 to the proper connector, the whole system will not work. BD-M5 and BD-M12 are interchangeable for testing purposes. BD-M2 and other identical boards are also interchangeable for testing purposes. BD-M1 should never be connected to connectors other than the designed one.

Adjustment procedure

(1) Check each power supply voltage at the plug of NC130, before this is connected to the memory.

(2) Connect CN21 through CN26 to the memory. A pair of terminals on the other end of each channel in these connectors should be connected to a proper load (e.g. LED input terminals on a grid card), or should be short-circuited, in order to avoid high-frequency oscillations.

(3) Check again each power supply voltage at the monitoring terminals on the memory. Re-adjust if necessary.

(4) Apply test tape M1 (specified by Fig. A2a) for writing mode 1. Check the output waveform of each channel, at the test terminal on the memory. Confirm that all the bits are stored (some distortions on the waveforms can be ignored in this test). If satisfactory, apply test tape M2 (specified by Fig. A2b) for writing mode 2. Repeat the checking.

(5) Adjust each potentiometer on BD-M2, and on the similar boards, so that the output current of each channel is 4.00 mA pk-pk. Also check the linearity. Details of this procedure are given on the following page.

Note The current can be checked by measuring the voltage at each monitoring terminal on the memory with an accuracy better than $\pm 2\%$ (the accuracy of the 10Ω resistor). A better measuring accuracy can be obtained by measuring the voltage across a known resistor (say 100Ω $\pm 0.1\%$) which is connected temporarily to the pair of terminals at the other end of cable of CN21 etc. with the differential input of a CRO.

Checking of the logic circuits

The logic circuits need no adjustments. However, waveforms at various points of the circuit are shown in Fig. 11 for test purposes.

Details of adjustments of the potentiometers on BD-M2 etc.

(a) Insert only BD-M1, MD-M5, BD-M12 and BD-M19 into the input memory frame, and keep them in an operating state.

(b) Insert each of the rest of the boards in turn, one at a time, into No. 6 rail (the rail for BD-M6) of the frame. This position in the frame has maximum space for adjusting the board.

(c) Switch off SW-M5 (on the rear panel) so that no dc bias voltage is fed.

(d) Feed test tape TM-3 (specified in Fig. 24) through tape reader 26C. The feeding must be repeated for each board under test.

(e) Connect Monitor terminal (on the front panel) No. 12, 13, 14, 15, 24, 25, 26 or 27 to a CRO, depending on the potentiometer to be adjusted. It is recommended to use the 10 mV/cm dc range of the CRO, after the sensitivity of this range is calibrated by 40 mV pk-pk signal with the accuracy of ±1%.

(f) Turn each potentiometer so that maximum resistance is obtained (see Fig. 25). The output on the CRO will show slightly less than 40 mV pk-pk.

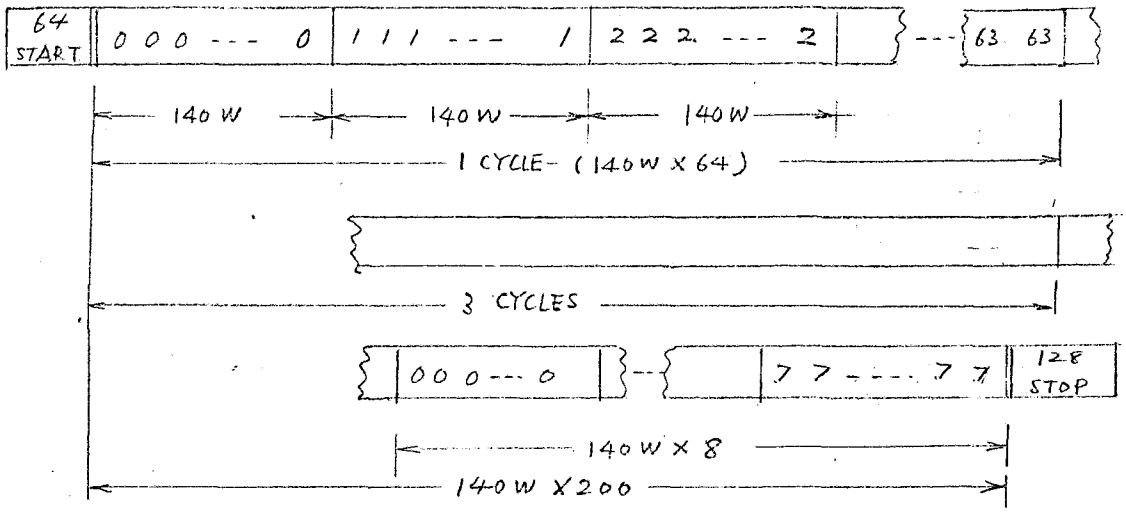
(g) Turn the potentiometer gradually (in reverse direction for first turn) so that the output voltage becomes exactly 40 mV pk-pk. Use two flat parts in the output voltage waveform (46-100 and 101-136 in Fig. 24).

Note If the potentiometer is turned to reduce the resistance further, the output voltage will reduce again, after it has reached maximum. Consequently there is the second wiper-position by which a 40 mV pk-pk output can be obtained. The second position must not be used.

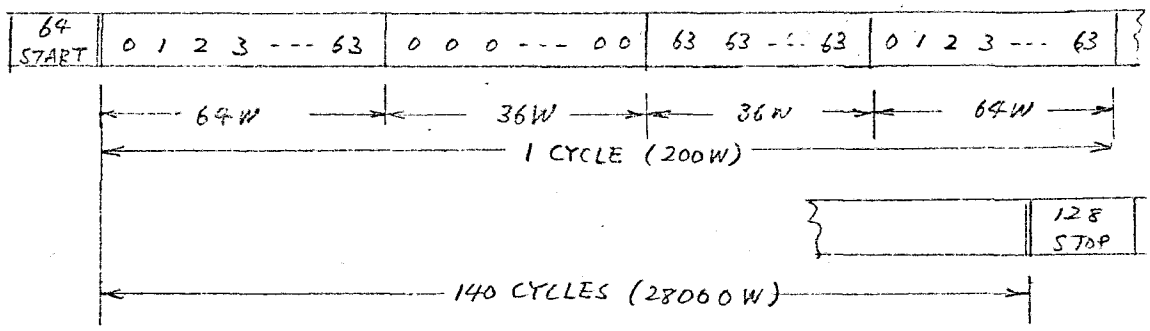
(h) The linearity of each circuit should be checked by parts of the output waveform (0-63 or 136-200 in Fig. 24).

(i) The position of the whole output waveform on the CRO will vary slightly from circuit to circuit, and the vertical control of the CRO has to be adjusted if the waveform is required to be in the same position. This is due to different offset voltages of 747s used for VCCs. These offset voltages do not affect the real operations, since the dc component of each opto-electronic coupler is cut by a coupling capacitor inside each grid card.

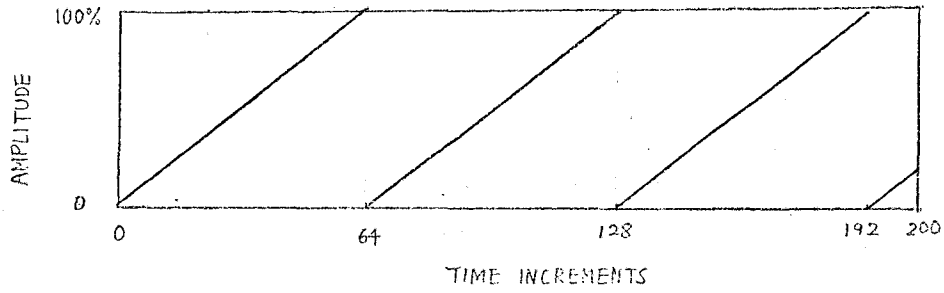
Note The position of the potentiometers on each circuit board, with their channel numbers and card numbers are shown in Fig. 26.



(a) Test tape TM-1 for Writing mode 1

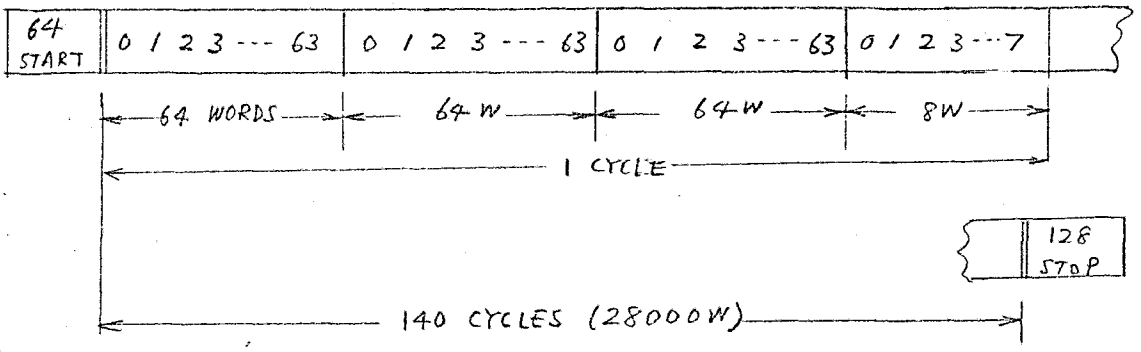


(b) Test tape TM-2 for Writing mode 2



(c) Analogue output waveform of each channel (common for Writing modes 1 and 2)

Fig. 23 Test tapes for the input memory. Binary numbers are indicated by decimal numbers.



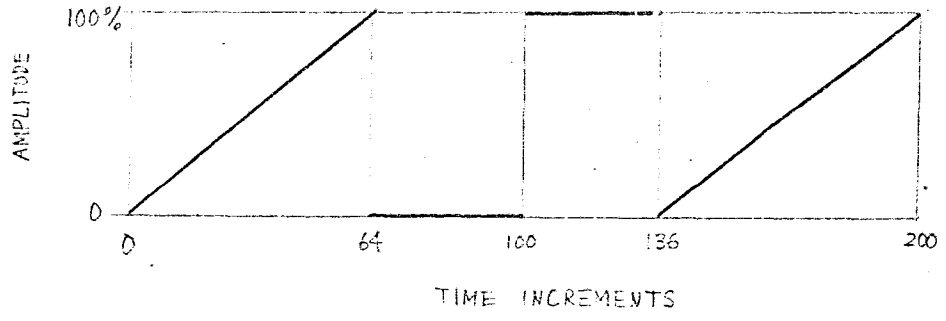


Fig. 24 Test tape, TM-3, for the amplitude calibration of the input memory. Binary numbers are indicated by decimal numbers.

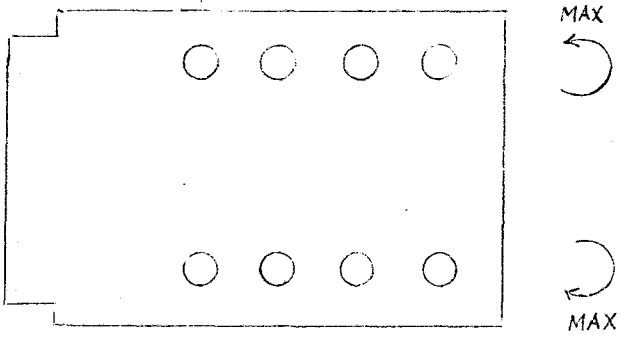
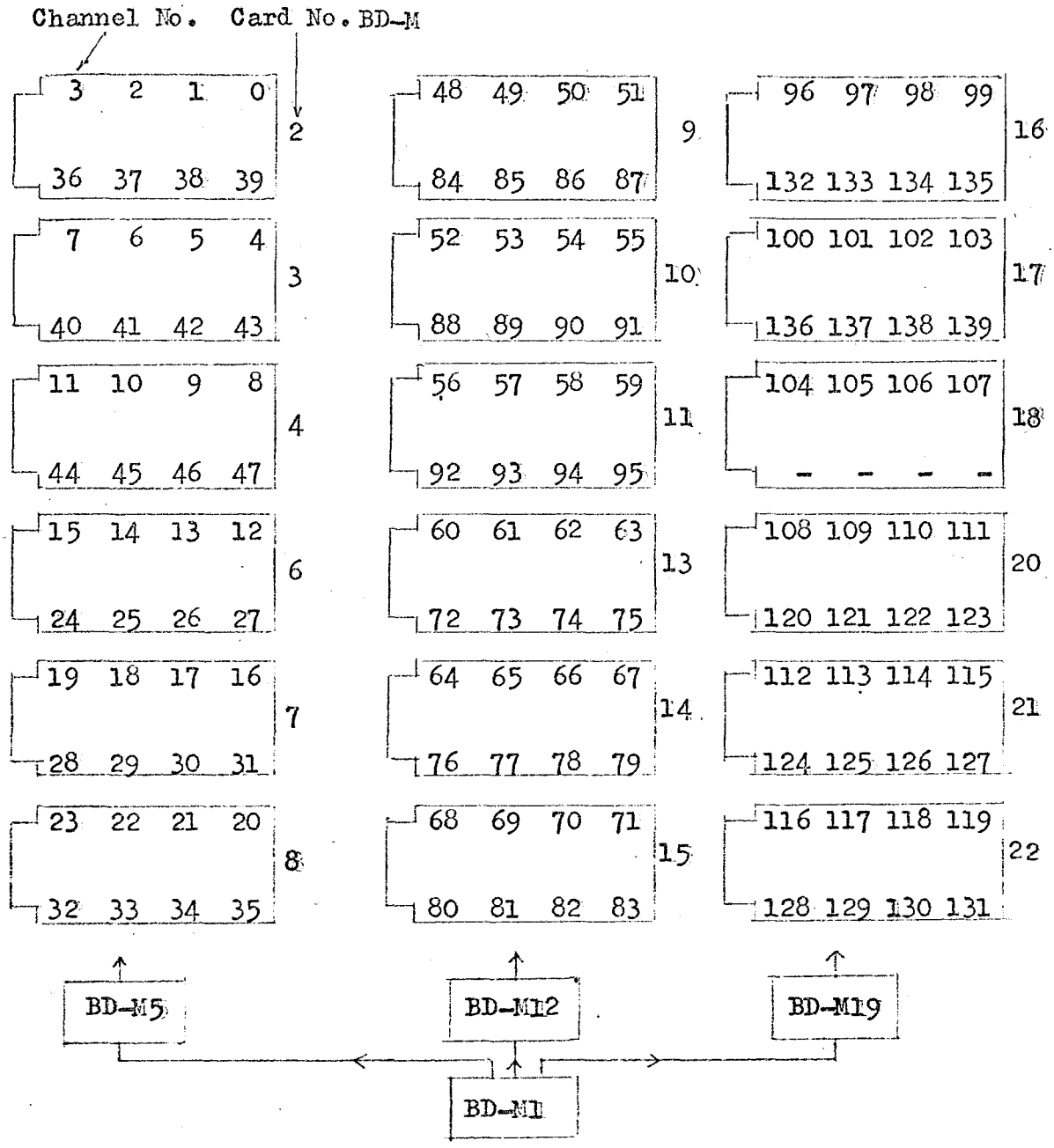


Fig. 25 Directions of turning potentiometers on BD-M2 etc.



Note The input memory is written in the order of the channel number.

Fig. 26 Approximate position of the components for each channel on BD-M1 to BD-M22 (component-side view)

Appendix 4 Operating instructions

1. Connection of the cables

Do not switch on the power supply until all the connections have been completed.

Table 11 Connections between the input memory cabinet and other parts.

Connector No.* on memory cabinet	Part to be connected
CN130	From the power supply for the input memory
CN103	From tape reader, model 26C
CN131	From the output memory
CN132	From an appropriate oscillator for a clock
CN133	To the synch. input of a CRO for monitoring
CN134	To CN (on the rear panel of the control cabinet)
CN21 to CN26	To the main computation cabinet
Fan	From a 240V AC line, through the power supply

*Numbers are marked on actual components.

2. Checking of the power supply voltages

Although the power supply voltages are stabilised, check them occasionally on the test terminals as shown in Fig. 27.

Each voltage should be within 1% of the nominal value.

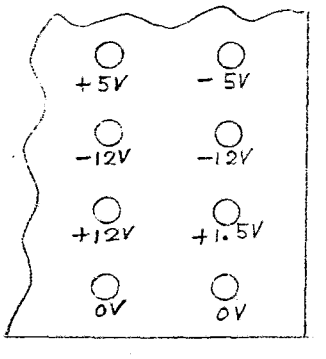


Fig. 27 Power-supply voltage checking terminals on the rear panel

3. Control of the tape reader, 26C

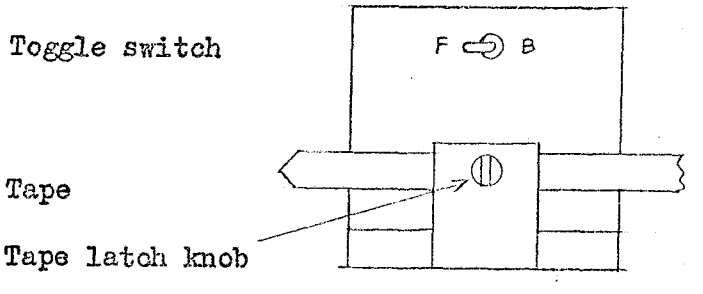


Fig. 28 Tape reader, 26C

The tape reader has only two controls: a tape latch knob and toggle switch.

(1) Tape latch knob

When the line marked on the knob is in a position across the tape, the tape can be inserted or taken out.

When the line marked on the knob is in a position along the tape, the tape is ready to run.

(2) Toggle switch

Forward run The switch should be in F-side normally, and the tape is ready to run forward in this position. Press the red button* (on the front panel of the input memory) to start running the tape.

Normal stop Tape stops automatically when a punched hole on the 7th track is read by the tape reader.

Automatic emergency stop If the speed of the tape is reduced by an external force (e.g. jamming of the tape), the tape stops automatically for protection. This is not supplied to the backward running of the tape.

Manual emergency stop Turn the toggle switch to B-side and back to F-side as quickly as possible. This can be applied to both forward and backward runnings.

Re-start for forward run after an emergency stop Press the red button*.

Backward run Turn the switch to B-side. The tape will not stop automatically. Turn the switch to F-side to stop the tape.

*When the red button is pressed, data stored in the memory are cleared automatically.

4. Control of the input memory

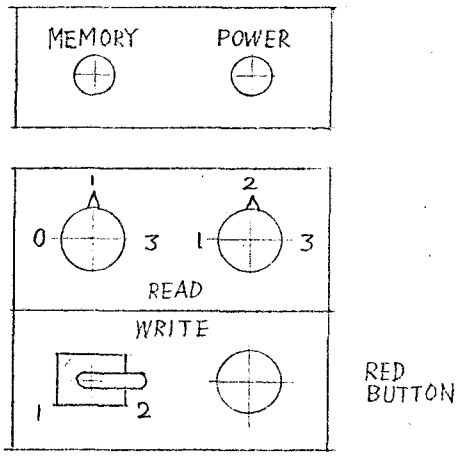


Fig. 29 Controls and indicators on the front panel of the input memory.

There are four controls and two indicators on the front panel of the input memory cabinet, as shown in Fig. 29.

Knob 0-1-3 When this knob is set in 0, the stored data in the memory are read (and fed into the computation circuit) continuously repeatedly without intervals.

When this knob is set in 1, the stored data are read repeatedly with intervals each of which is equivalent to the period of 200 time-increments.

When this knob is set in 3, the stored data are read repeatedly with intervals each of which is equivalent to 200 x 3 time-increments.

The choice of the positions of the knob depends on the type of model.

Knob 1-2-3 When this knob is set in 1, 2 or 3, the period of reading the memory (and the rate of feeding the data into the computation circuit) takes 1, 2 or 3 times the period of the reading clock (which is fed from terminal CN131 or CN132 on the rear panel of the input memory).

For example, if the reading clock is set to the period of 0.1 ms, and the knob is set in 1, 2 or 3, each time increment of the data stored in the memory will be read at the rate of 0.1 ms, 0.2 ms or 0.3 ms which corresponds to 1 h, 2 hs or 3 hs in real time.

Toggle switch 1-2 If a given input tape is made in writing mode 1, set the switch to 1. If a given input tape is made in writing mode 2, set the switch to 2.

Red Button The red button should be pressed, after all other controls are set.

When this is pressed, a tape on the tape reader starts to run, and the data on the tape are stored into the memory. When the tape comes to its end, the tape reader stops automatically, and the stored data are fed into the computation circuit also automatically.

There are two controls, which are not frequently operated, on the rear panel of the input memory cabinet (see Fig. 17).

Toggle switch SW-M5 Normally set this switch to A so that the clock within the model system enters into the memory through terminal CN131.

Set the switch to B, only when external clock (which should be fed through connector CN132) is used.

Toggle switch SW-M6 Normally set this switch to BIAS so that all the output currents fed from the memory to opto-electronic couplers in the main computation circuit are biased by 0.8 mA.

Set the switch to OFF, only when the memory is applied to numerical-map plotting.

Appendix 5 Design Notes

(1) The manufacturing deviation (given by the data sheet) for the clock-input and data-input voltages of Type 2511A (CMOS memory) are shown in Table 12. The manufacturing deviation of the output voltages of TTL units is shown in Table 13.

Table 12 Manufacturing deviation of input voltage of Type 2511A

L state	Min. Max.	-5V +1.05V
H state	Min. Max.	+3.2V +5.3V

Table 13 Manufacturing deviation of output voltage of TTL units

L state	Max. Typ.	+0.4V +0.22V
H state	Min. Typ.	+2.4V +3.3V

In order to combine these two types, the following considerations have been made:-

(a) A pull-up resistor is added between each output terminal of the TTL and the +5V supply line. Approximately +5V is obtained at the output of most TTL units by using a 10K resistor. For a few exceptional units, lower values than 10K are required to achieve +5V.

(b) Although +5.3V is required, according to the above table, for the maximum H state input voltage of 2511A, in practice all the units used have been operated by +5.0V satisfactorily.

(c) It has been found that a few products of 7408 have an L state output voltage greater than specified value (0.4V). These had to be extracted.

(2) In order to control 140 AND-gates (35 packages of 7408) in series, 6 buffered NAND-gates (3 packages of 7440) each of which has maximum fan-out of 30 have been used for BD-M5, BD-M12 and BD-M19 (each NAND gate is loaded by 24 units, except for 22 units in the last group).

(3) The power supply terminals (0V and +5V) on BD-M1 are shunted by a reversed polarity diode, in order to protect the circuit from accidental contact with the -12V supply line.

(4) The input terminal 74/4 which is connected to 08(1)/11 through a 1K resistor is pulled up to +5V level by a 10K preset resistor at the joint of the 1K resistor. The preset resistor should be adjusted

so that the input to 74/1 can control this flip-flop when 08(1)/11 is in an H state, and cannot control when 08(1)/11 is in an L state. Note 08(1)/11 is normally in an H state, but changed into an L state only when either 75(2)/1 or 32(3)/8 is activated.

(5) The capacitor (0.1 μF) connected to 121(2)/6 is necessary to ensure that its output is triggered by the rear edge of each input pulse fed into 121(2)/3,4. Without this capacitor, the output is triggered by both the front and rear edges, and each word in the input data is stored in two sets of memory cells in duplicate. This will result in the output waveform as shown in Fig. 1(a).

(6) The capacitor (0.1 μF) connected between 121(1)/3,4 and 121(1)/7 (which is a part of the earth line) is necessary to prevent the improper entry of the reading clock (10 kHz) during the writing mode. The lengths of the capacitor leads should be minimised, and its earthing point should be 121(1)/7 itself. The improper entry of the reading clock will disturb the demultiplexing action, and the output waveform will be as shown in Fig. 1(b).

(7) The capacitor (0.1 μF) connected between 04/2 and earth is to filter out noises mixed in the reading clock which is derived from a 1 MHz oscillator.

Appendix 6 Committee's comments

The author made a proposal of the model system, including two different designs of the input memory (which was called 'input system' at that time). The committee who examined it in 1972 commented as follows:

Cost of the input memory

The author estimated that the cost of the input memory (when either design was applied) was approximately £2,000 for its components and assembly, based on his design, actual price lists (for components) and the contractors' quotations (for assembly) at that time.

The committee estimated £75,000 at least for the components and assembly.

Since the cost of the input memory is a substantial proportion of the total cost of the whole model, this difference is significant in evaluating the whole scheme.

It has been proved, after the memory was actually constructed in 1973, that the cost was £2,000.

Coupling method

In both the proposed design of the input memory, the author used opto-electronic coupling extensively, which he thought essential for the required electronic conditions, reliability and low cost.

The committee advised the author that opto-electronic coupling was not reliable, according to their experience, and recommended the use of transformer coupling instead.

The author could not accept this because:

(1) In the computation circuit of the model system, there are electromotive forces in both the primary and secondary sides of the coupling, and the signal must be transmitted only from the primary to the secondary. An opto-electronic coupling is ideal for this purpose, while a transformer alone cannot realise this condition absolutely.

(2) A transformer by which an analogue signal having a wide frequency range can be transformed with a computer-grade accuracy would be very expensive, in addition to a large physical size and weight which would make the whole system large and expensive. Note that such couplings are required in the same number as that of grids (say 600).

(3) In the author's opinion, the reliability of opto-electronic coupling is as high as for other semiconductor products and that it was a well established technique even in 1972, and is now one of the standard techniques in electronics.

(4) The author has tested all the opto-electronic couplers which he wanted to use, 660 units in all, under far severer conditions than commercial tests, including their temperature characteristics. Only 7 units were to be unsatisfactory, most of which still satisfy the commercial test standards.

(5) It has been proved, after the actual construction of the memory, that the opto-electronic couplings have been successfully working up to date.