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MK V CTD/Level 'A' Interface

J Smithers

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INSTITUTE OF OCEANOGRAPHIC SCIENCES
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ABSTRACT

This report describes the format of data transmitted by the MK IIIb and MK V CTD systems (Conductivity, Temperature and Depth probes).

The differences between the two and the problems of transferring data from the CTD Deck units to the RVS Level 'A' shipborne computing systems are described.

The design and circuit descriptions of an interface to overcome the problems is given.

KEYWORDS

FRAME SYNC
LEVEL 'A'
MK IIIb CTD
MK V CTD

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CONTENTS.

DIAGRAMS/COMPONENT SCHEDULE

MKV CTD DECK UNIT/LEVEL 'A' INTERFACE

1. Introduction.

During the many years that IOSDL have been using Neil Brown CTD systems, a number of changes have been made to the way in which data are logged during cruises. The original CTD systems used an analogue tape recorder to log the undemodulated data transmitted up the sea-cable from the underwater unit. This data was then replayed in real time back at the Institute, and transferred to a HP2100 computer for processing.

The first improvement made, was to log data directly from the CTD deck unit and process it on a ship borne IBM 1800 system. Ship borne computing gradually improved over the years with more powerful machines being used until the present day Level 'A','B' and 'C' system was adopted. At the same time the CTD deck units were also upgraded allowing a direct serial data link to the Level 'A' without the need for intermediate electronics.

This system has now been used successfully for many cruises until the purchase by IOSDL of a new MKV CTD. This instrument differs slightly in it's data format from the MKIIIb CTDs in use. Although the differences are small they pose a problem in the way in which the Level 'A' can acquire the data as will be shown.

2. General Description.

The data transmitted by the MKIIIb CTDs, consists of a number of words depending upon the particular instrument, grouped together to form a data frame sent in a repeating format, at either 8 or 16 data frames/second. The data words are transmitted from the CTD deck unit at 9600 Baud and have 1 start bit, 8 data bits, 2 stop bits and no parity. The 8 data bits are in binary format with 2 data words allocated for some variables to obtain the necessary resolution. As far as the Level 'A' is concerned. one of the most important of these data words is the first or FRAME SYNC word. This alternates between binary 11110000 and 00001111 every data frame, (decimal 15 or 240 or hex &F0 and &0F). The Level 'A' software looks for this FRAME SYNC, and knowing that its inverse should occur after a set number of words, can consequently lock onto and correctly identify a data frame.

When the MKV CTD was developed by Neil Brown Instrument Systems Ltd. this format was changed. The basic layout of a data frame is similar to that of the MKIIIb but with no FRAME SYNC word. The data

when transmitted at 9600 Baud, consists of 20 words, each of approximately 1 millisecond duration, occurring every 1 millisecond, and with a 19 millisecond gap at the end of each data frame.

2.1 The Problem.

Using a PC running a DOS single user operating system to log and display the CTD data presents no problems as the acquisition software has complete control over the environment in which it is working. The prime object of this software is to log the data and then perform other tasks in the time available before the next incoming data word triggers the logging process.

The new MKII Level 'A' uses a multi-user, multi-tasking operating system (OS9). The operating system divides the time into a number of slices and allows each program a slice at a time. Each slice consists of a number of tick intervals, which in the MKII Level 'A' is 1/100th of a second. The software clock is also updated with ticks at 100 /second. Whilst this gives a sub second resolution of 10 milliseconds, the accuracy is 0 to +30 milliseconds. The situation is further complicated by the fact that the part of the program which reads the incoming data is also being switched in and out of its execution state. It is therefore not possible to guarantee that the program can correctly identify between which bytes of data the gap occurred. (Thanks to Martin Beney, RVS Barry for an explanation of the problem.).

2.2 The Solution.

To solve the problem it was decided to design and build a piece of hardware that would take the serial data stream from the CTD deck unit, detect the inter frame gap, and insert a FRAME SYNC word alternating between &F0/&0F in this gap. The resultant data could then be detected and correctly identified by the MKII Level 'A' in a similar way to the MKIIIb CTDs.

3. Circuit Description.

The circuit to add the frame sync pulses to the MKV CTD data stream turns out to be fairly simple. The RS232 data from the CTD deck unit is received by IC1 , a MAX232 Line Driver/Receiver chip. This device converts the RS232 levels to an inverted unipolar +5V level.

The output from the line receiver is inverted by IC8a , a CD4049 connected by wire links from test point pins TP4-TP5 and TP6-TP7. The inclusion of links to enable the invertor to be connected or not, is merely for circuit versatility. If this invertor needs to be taken out of circuit, at any time, then it's input

should be grounded by connecting TP3-TP4 and joining TP5-TP6. The output of IC8a drives the RETRIGGER input of IC2, a CD4047 monostable.

Capacitor C6 and resistor R2 control the pulse length from the Q and Q/ outputs of this device. If the time constant of the R/C network is set long enough, then the monostable is retriggered before its Q output can go low. This produces a pulse whose length is greater than the group of CTD data pulses, but goes low for a period before the next data frame, or conversely the Q/ output goes high during the inter frame gap. The Q/ output of IC2 clocks IC3b, a CD4013 dual D type flip-flop on its positive going transition. The Q and Q/ outputs of this flip-flop each drive four of the eight parallel inputs of IC4, a 6402 UART. This produces the &F0 and &0F (240/15) frame sync words required. The D input of IC3b is driven by IC3b, Q/ output. The Q and Q/ outputs of IC3b therefore alternate to produce the sync words for each MKV data frame.

The output from IC2 also drives the second half of the IC3a whose output pulse length is controlled by R1/C5, to provide a positive transition from its Q/ output, delayed with reference to the end of the data pulse group.

A low level from this output loads the data present on the UART transmitter buffer inputs into it's transmitter buffer register. A low to high transition then loads the transmitter register and sends the serial frame sync word on its transmitter register output.

The baud rate clock is generated by IC5 a 4702 chip, 2.456MHZ crystal, R3 and C7 and is hard wired for 9600 Baud. The UART is configured to transmit a serial word of 1 start bit, 8 data bits and 2 stop bits with no parity. The serial frame sync word generated is timed by the IC2 and IC3a, to occur after the 20 data words transmitted by the MKV CTD and during the 19 millisec inter frame gap between data groups. IC7a, a CD4001, inverts the output from the UART and OR'S this and the positive going data from IC8a. The inverted output of IC7b drives IC6, a second MAX232 chip. The four 1uF capacitors associated with the MAX232 device enable an on-chip $\pm$ 10 volt supply to be derived from the +5V source, providing RS232 output voltage levels. The MAX232 inverts the signal present on it's input, ensuring the proper polarity to drive the CTD/PS2 Computer COM1 input. Provision is again made to invert the data direction if necessary by removing the wire links from test points TP10-TP11 and TP8-TP9. The input of IC8b is normally grounded by connection of test points TP8-TP9 when not in use. IC9 is a commercial encapsulated 240V AC/+5V DC power supply. All unused gates and invertors on IC7 and IC8 have their inputs grounded. The 25 way 'D' type connectors on the back of the interface unit provide input to, and output from the unit. Both input and output are provided on plug and socket type connectors for versatility. The small front panel button provides a Master Reset pulse, should the UART lock up for any reason.

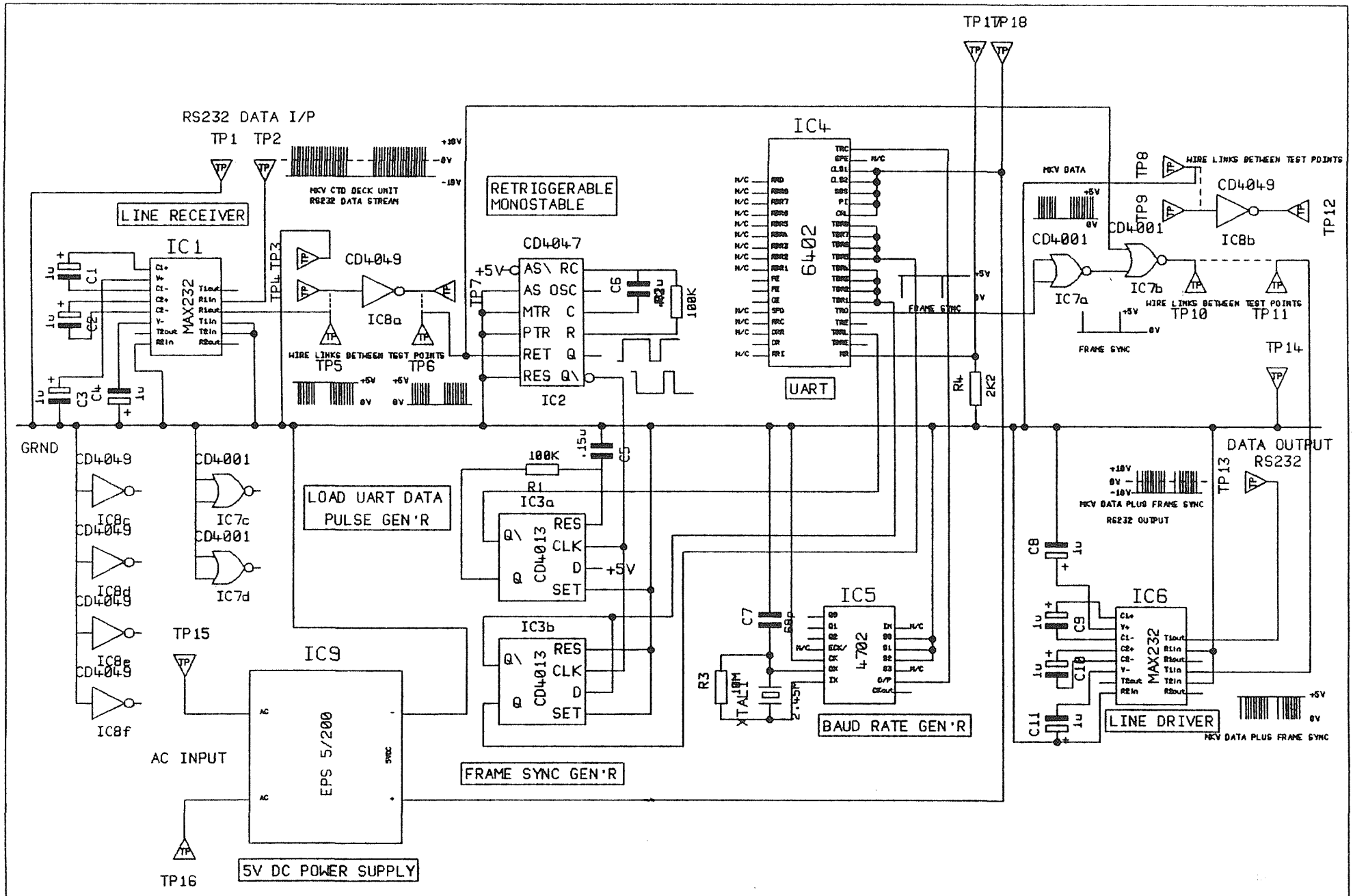

FIG 1. MKV CTD DATA INTERFACE

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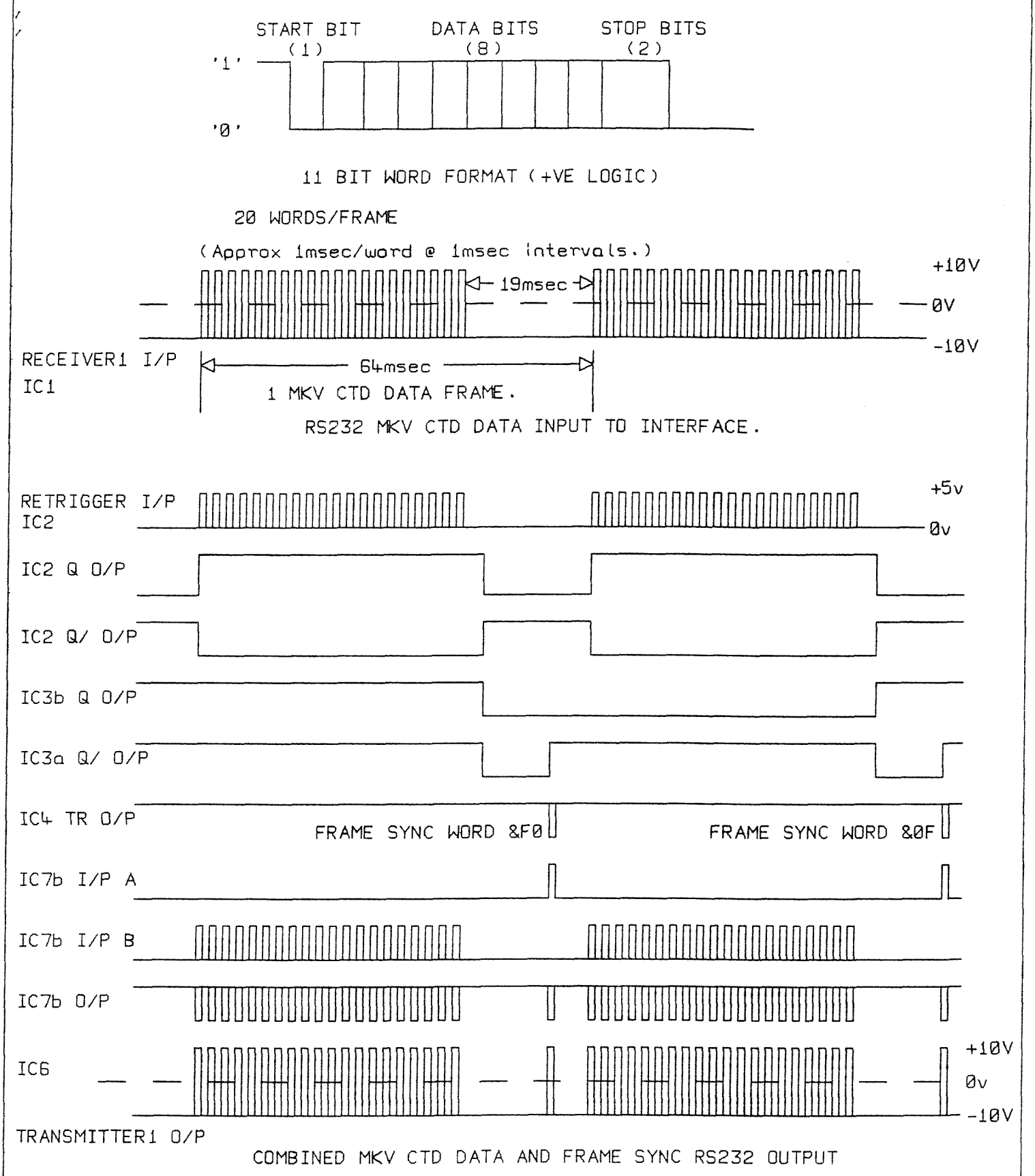

FIG 2. MKV CTD INTERFACE WAVEFORMS.	DRAWN	J.SMITHERS
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CCT DIA SYMBOL	ELECTRONIC COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	VALUE	RATING	TYPE	SUPPLIERS NAME	REF No.	
R1	RESISTOR	100K	0.4W	MET FILM MR25	IOSDL STORES		ANY EQUIVALENT
R2	RESISTOR	100K	0.4W	MET FILM MR25	IOSDL STORES		"
R3	RESISTOR	10M		THICK FILM	RS COMPS	158-159	"
R4	RESISTOR	2K2	0.4W	MET FILM MR25	IOSDL STORES		"
C1	CAPACITOR	1uF	100V	ELECTROLYTIC	IOSDL STORES		"
C2	CAPACITOR	1uF	100V	ELECTROLYTIC	IOSDL STORES		"
C3	CAPACITOR	1uF	100V	ELECTROLYTIC	IOSDL STORES		"
C4	CAPACITOR	1uF	100V	ELECTROLYTIC	IOSDL STORES		"
C5	CAPACITOR	0.15uF	63V	POLYESTER	IOSDL STORES		"
C6	CAPACITOR	0.02uF	63V	POLYESTER	IOSDL STORES		"
C7	CAPACITOR	68pF	160V	SILVER MICA	IOSDL STORES		"
C8	CAPACITOR	1uF	100V	ELECTROLYTIC	IOSDL STORES		"
C9	CAPACITOR	1uF	100V	ELECTROLYTIC	IOSDL STORES		"
C10	CAPACITOR	1uF	100V	ELECTROLYTIC	IOSDL STORES		"
C11	CAPACITOR	1uF	100V	ELECTROLYTIC	IOSDL STORES		"
IC1	INT CIRCUIT	MAX232		LINE REC/DRV	FARNELL	MAX232N	"
IC2	INT CIRCUIT	CD4047		MONOSTABLE	IOSDL STORES		"
IC3	INT CIRCUIT	CD4013		D FLIP-FLOP	IOSDL STORES		"
IC4	INT CIRCUIT	6402		UART	FARNELL	CDP6402CE	"
IC5	INT CIRCUIT	4702		BAUD GEN'R	FARNELL	HD 347029	"
IC6	INT CIRCUIT	MAX232		LINE REC/DRV	FARNELL	MAX232N	"
IC7	INT CIRCUIT	CD4001		QUAD 2IP NOR	IOSDL STORES		"
IC8	INT CIRCUIT	CD4049		HEX INVERTOR	IOSDL STORES		"

MKV CTD DATA INTERFACE

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DRAWN	J.SMITHERS	DATE	13-11-92
ISSUE	1	SHEET	1 OF 2

CCT DIA SYMBOL	ELECTRONIC COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	VALUE	RATING	TYPE	SUPPLIERS NAME	REF No.	
IC9	INT CIRCUIT			240VAC-5VDC	FARNELL	EPS5/200	ENCAPSULATED PSU
XTAL1	CRYSTAL	2.45MHZ		HC33/U	RS COMPS	303-359	ANY EQUIVALENT
TP1-TP18	TERMINAL PIN			VERO 18-0222D	IOSDL STORES		"
F1	FUSE HOLDER	250mA	240VAC	PANEL MTG	RS COMPS	412-021	"
SW1	SWITCH	2A	240VAC	MSP106D SPDT	RS COMPS	339-241	"
SW2	SWITCH	100mA	30VDC	SUB-MIN N/O	RS COMPS	336-731	MOMENTARY PUSH
CASE	ENCLOSURE				RS COMPS	501-468	ANY EQUIVALENT
SKT1	SOCKET			25 WAY D TYPE	FARNELL	150-814	"
SKT2	PLUG			25 WAY D TYPE	FARNELL	150-810	"
SKT3	SOCKET			25 WAY D TYPE	FARNELL	150-814	"
SKT4	PLUG			25 WAY D TYPE	FARNELL	150-810	"
SOCKETS	SOCKET IC			14 PIN	IOSDL STORES		"
SOCKETS	SOCKET IC			16 PIN	IOSDL STORES		"
SOCKETS	SOCKET IC			40 PIN	IOSDL STORES		"

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