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N E W I N P U T M E M O R Y

A part of the electronic model
for tides and storm surges

S. Ishiguro

1979

NATURAL ENVIRONMENT RESEARCH COUNCIL
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CONTENTS

ABSTRACT

In the electronic model for tides and storm surges, input data representing meteorological conditions (e.g. atmospheric-pressure field and wind field) for a certain period is stored in the memory first. Then the data is fed into each grid of the model simultaneously, with the electronic smoothing of time-increments in the data. Unlike a conventional numerical model, the whole dynamic computation is carried out without step-by-step procedures so that the differential (not difference) equations are solved.

This paper describes an electronic memory system for such a purpose. The main part of the system consists of N-channel MOS RAMs in large-scale integrated circuits, with DACs at the last stage, and control circuits. The system has a single 8-bit parallel input, and 144 channels of analogue opto-electronic outputs each of which can produce different functions simultaneously.

The input data can take either the form of $F_1(t)_{x,y}$ or $F_2(x,y)_t$, but the outputs are always in the form of $F_o(t)_{x,y}$; where x and y represent a position in the sea and t represents time. The conversion of the forms is carried out by the control circuits during the input-data feeding.

The system has enough capacity to handle the 100 km meteorological grids covering the seas around the British Isles, and to feed the meteorological input into the 'sea grids' several of which are contained in each meteorological grid. The system can store the hourly input data for 10 days which is sufficient for most storm surge analyses. The full data feeding takes about one minute with an optical tape-reader. The output data can be repeatedly produced with a typical period of 10 milli seconds which is enough to solve all the equations.

The system can also produce tidal components for the model, and has also been designed to be usable as a random access memory for conventional digital data having about 36K addresses.

The system is contained in a cabinet of 50 × 35 × 22 cm^3, with a power supply cabinet having the same dimensions. The AC power supply input requires about 156W.

This paper has been written to describe the design and performance of the input memory system, and also as a guide to its operation and servicing.

1. INTRODUCTION

The 'electronic model for tides and storm surges' (Ref. 1) contains an 'input memory'. This is a system by which a set of input data (e.g. atmospheric pressure data) is stored before it is fed into the main computation circuit in the model. Fig. 1 shows the position of the input memory in the model.

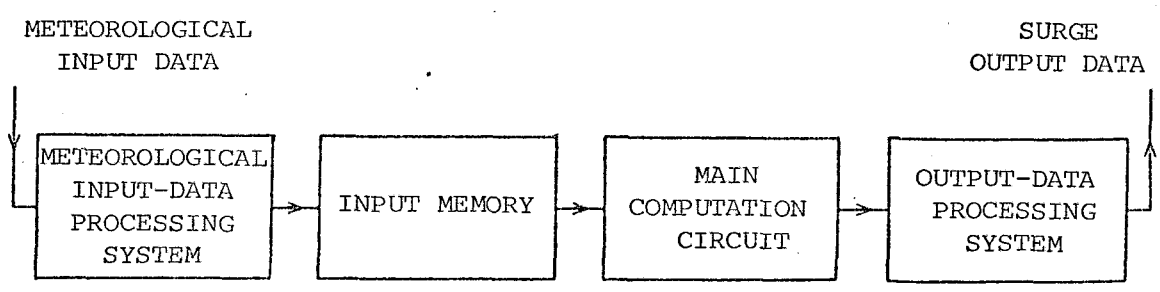


Fig. 1 Input memory in the electronic model for tides and storm surges (a greatly simplified illustration).

The main requirements for the input memory are:-

1. To store a set of input data (about 200K bits in a digital form) for a certain period (say 10 milli seconds minimum, and 1 hour maximum);

2. To generate a set of simultaneous analogue current outputs (different waveforms in say 140 channels to drive up to 600 optoelectronic couplers); and

3. To rearrange the input data into a suitable form for the model, in a minimum time (ideally during the input-data feeding).

The most particular requirement, compared with a conventional memory, is 2, while 1 and 3 are not unusual. It is more economical, therefore, to construct a memory for the required conditions rather than to modify a standard memory.

In an earlier design, an optoelectronic-mechanical system was used for the input memory. Since 1972, a totally electronic system had been used successfully (Ref. 2), until an accident near the end of 1978 (a high voltage line touched the power supply line of the memory). On this occasion, it was decided to redesign the input memory using more up-to-date components and techniques, although the alterations to its interface circuits and physical construction were minimized. This paper describes the design and performance of the new input memory. A guide to its operation and servicing is also included.

Table 1 shows a comparison of the new and previous input memories. The main improvements to the new input memory are the increase of resolution in a waveform representation; the increase of store capacity; and the capability of a random data treatment (the memory can now be used as a general purpose data store within the system). The power supply for the new input memory has also been improved electronically and physically, with a more elaborate circuit protection facility.

The true cost of the new input memory is lower than the previous memory, considering the value of money. This is due to the use of large-scale integrated circuits which are mass-produced for micro-processors.

Table 1 Main improvements of the new memory over the previous memory.

		New memory	Previous memory
Resolution (bits/value)		8	6
Time increments (per channel)		256	200
Total memory bits		295K	168K
Digital output terminals		Data bus	Not available
General-purpose data-handling capability		Random and sequential	Sequential only
Memory type		N-channel MOS LSI RAM	CMOS SSR
Waveform monitor output		2V pk-pk	200mV pk-pk
Main clock		Internal, 10 MHz	External, 10 kHz
Power supply	For digital	+5V	+5V, -5V, -12V
	For analogue	+12V, -12V	+12V, -12V, -1.5V
	Regulator	Switching type & linear type	Linear type
	Cooling	Natural convection	Motor fans
	Total AC input power	165W	250W
	Case dimensions	50 × 35 × 22 cm^3	50 × 70 × 22 cm^3
Circuit protections		a High dc-voltage shut down (100ns) b 240V ac-line shut down (50ms) c Audible alarm d Power-supply protections	Power-supply protections only

2. FUNDAMENTAL DESIGN

2.1 Data rearrangements

Fig. 2 shows the timing diagram of the main data rearrangements. Data can be processed in five different modes:-

Sequential write mode 1
Sequential write mode 2
Sequential read mode 0
Sequential read mode 1
Random write/read mode

Sequential write mode 1 has been prepared to write the following set of data.

$$x_o(t_o),\quad x_1(t_o),\quad x_2(t_o) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad x_{143}(t_o) \quad ;$$

$$x_o(t_1),\quad x_1(t_1),\quad x_2(t_1) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad x_{143}(t_1) \quad ;$$

$$\vdots \qquad \vdots \qquad \vdots \qquad\qquad\qquad\qquad \vdots$$

$$x_o(t_{255}),\ x_1(t_{255}),\ x_2(t_{255}) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad x_{143}(t_{255}).$$

where $x_n(t_m)$ represents a value for station x_n and at time t_m. The data is fed into the system in this order, but all the values related to x_n are written in channel n of the memory, keeping the order of t_m within each section.

Sequential write mode 2 has been prepared to write the following set of data.

$$x_o(t_o),\quad x_o(t_1),\quad x_o(t_2) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad x_o\ (t_{255});$$

$$x_1(t_o),\quad x_1(t_1),\quad x_1(t_2) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad x_1\ (t_{255});$$

$$\vdots \qquad \vdots \qquad \vdots \qquad\qquad\qquad\qquad \vdots$$

$$x_{143}(t_o),\ x_{143}(t_1),\ x_{143}(t_2) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad x_{143}(t_{255}).$$

where $x_n(t_m)$ has the same definition as in the previous example. The data is fed into the system in this order, and all the data related to x_n is written in channel n of the memory, keeping the order within each set.

Note: When the writing has been completed, the written data by modes 1 and 2 become the same in the memory.
The actual data is a vector quantity, and the other component $y_n(t_m)$ is treated in the same way as above examples.

Sequential read mode 0 has been prepared to read the data written in all the channels of the memory simultaneously, keeping synchronized so that all the values related to t_m are read at the same time. Values within each channel are read in the order of t_0, t_1, t_2 .... t_{255}. The reading is automatically cycled without a break.

Sequential read mode 1 is similar to mode 0, but with intervals having a period equivalent to 256 increments.

Random write/read mode is a conventional arrangement. Each value of data is written in a particular address which is specified by an address code. The written data is read by giving the appropriate address code.

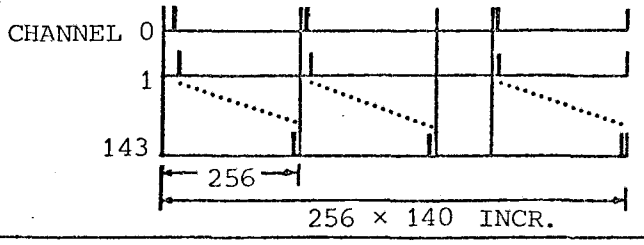
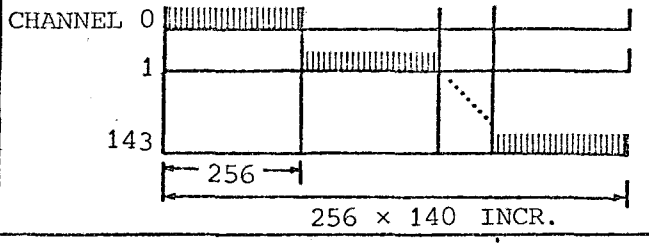
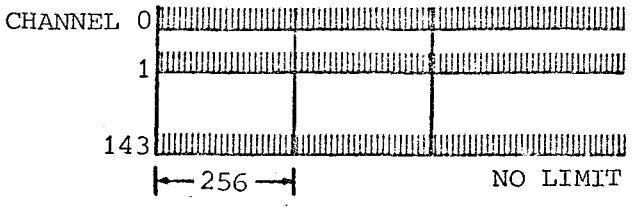
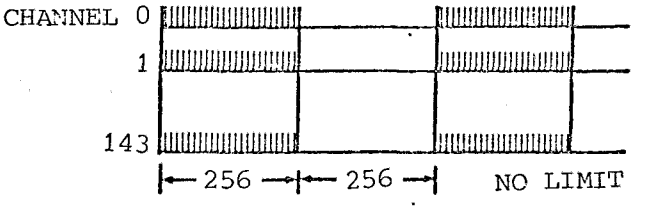
MODE		INPUT	OUTPUT
WRITE MODE 1		DIGITAL 8-BIT 36.6K WORDS	ANALOGUE CURRENT THROUGH DACs
WRITE MODE 2			
READ MODE 0			
READ MODE 1			
RANDOM WRITE/READ MODE	259K BITS	8-BIT DATA, 15-BIT ADDRESS	8-BIT DATA

Fig. 2 Five modes of data rearrangement by the input memory.

2.2 System structure

Fig. 3 shows the fundamental structure of the input memory system. This consists of:-

Memory units (144 channel identical),
Address bus and data bus with switching circuits,
Sequential-code generator,
Data/address separator, and
Control circuit with a clock.

The input to the system is always digital (bit-parallel and word-serial), but the output of the system is digital (the same form as the input) and analogue (simultaneous reading of all the channels).

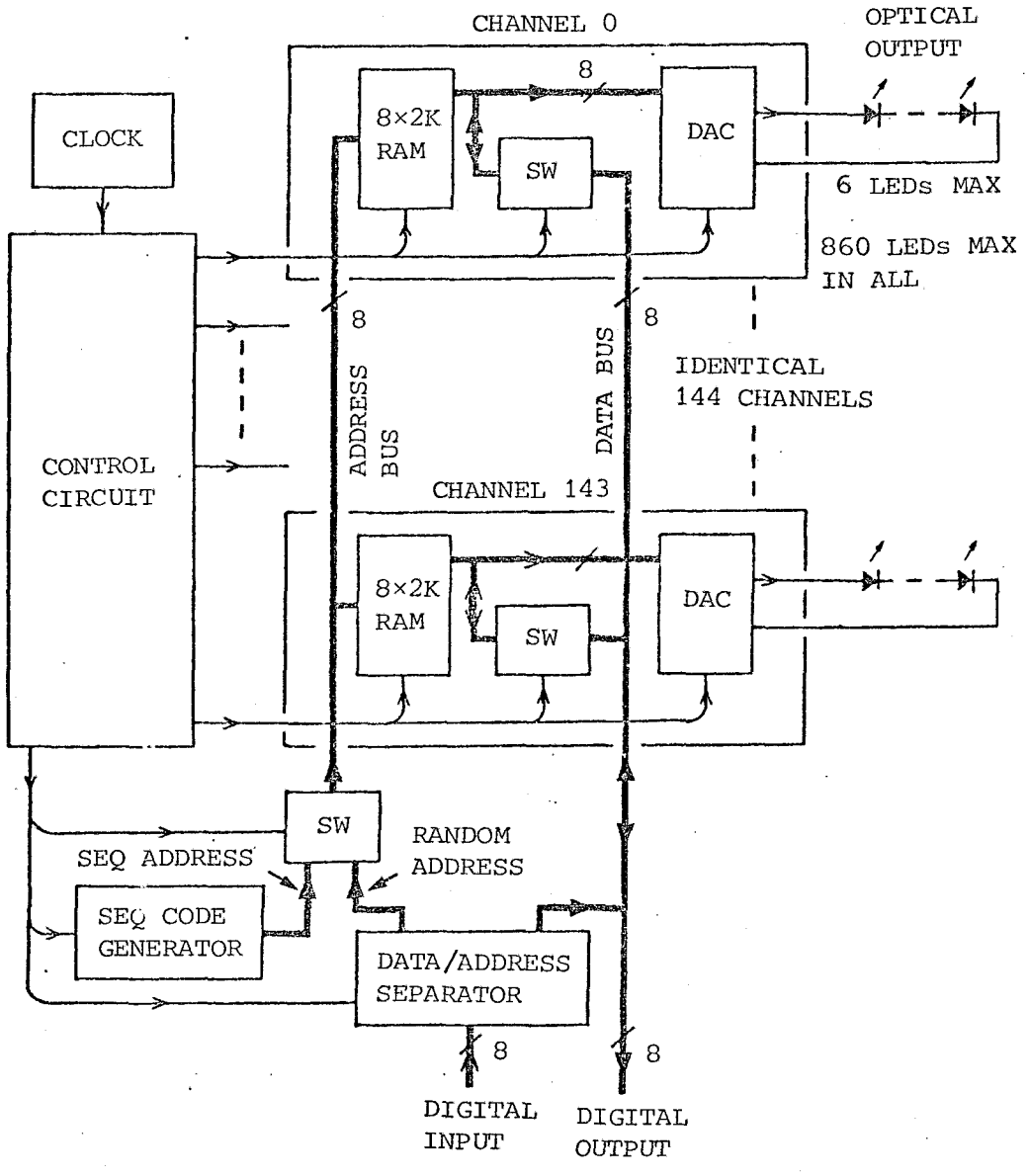


Fig. 3 Fundamental structure of the input memory system.

A set of data and their addresses, if any, are fed into the same input terminals of the system. If an input is random, with addresses, the data and addresses are separated by the data/address separator, and fed into the data bus and address bus respectively. If an input is sequential, without addresses, the data is fed directly (by-passing the data/address separator) into the data bus. In this case, their addresses are internally generated by the address generator following the order of arrival of each value in the data, and fed into the address bus.

Each memory channel consists of a 2K × 8 RAM, a set of switches and a DAC. In a write mode, the switches are closed so that the input data is fed into both the RAM and DAC. The address codes enter into all the RAMs in the system simultaneously. However, the control circuit works so that only one address accepts an input value at a time. Since all the DACs are connected to the data bus in a write mode, the input data can be monitored in an analogue form through the DACs.

In a read mode, all switches in the memory channel are opened so that the written data in each RAM can only be fed into each DAC (note, the data written in each DAC is different). Each DAC drives up to 6 units of LEDs contained in optoelectronic couplers.

2.3 Fundamental circuit arrangements for the 5 modes

The system works in five different modes of operation (listed in 2.1) according to the control circuit. The fundamental circuit arrangement for each mode is shown in Figs. 4 to 7*. Throughout these figures, essential control circuits only are shown for simplicity.

Each RAM chip has a chip-enable terminal ($\overline{CE}$) and read/write control terminal (R/W), other than data terminals and address terminals. The five different modes of operation can be obtained by using different combinations of $\overline{CE}$ and R/W, with respect to timing and chips concerned (280 units in all).

The start and end of any write mode is programmed by special codes on an input tape, and any read mode follows automatically, immediately after the completion of a write operation. The choice of one of the write modes, and the choice of one of the read modes, are carried out manually by selecting the control switches.

The write clock, in any write mode, enters from an external system (e.g. a tape reader) and is synchronized with a data entry. The read clock, in any sequential mode, is generated by an internal clock. The read clock in a random mode can be chosen either from an external or internal source.

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*Common symbols are used for ICs in Figs. 4 to 7 and Fig. 10 (the circuit diagram in chapter 3). For example, 93(3) indicates IC type 7493, and package no. 3 within the same type. If only one type of IC is used in the system, package no. is omitted. Also 93(3)/7 indicates pin no. 7 in the same package.

Sequential write mode 1 (Fig. 4)

Three code generators are used in this mode.

The 1st code generator consists of 93(3). This is driven directly by the write clock, and generates 16 different 4-bit codes sequentially (one code per clock pulse). This output is fed into channel selectors 154(1) to 154(9) so that one channel of each selector is selected at a time. Only one channel throughout all the 154s can be selected, when the CE terminal of a particular 154 is activated at the same time.

The 2nd code generator consists of 93(4). This is driven by the 16th code output of 93(3), and generates 9 different 4-bit codes sequentially (one code per 16 clock pulses). This output is fed into another channel selector, 42, so that one channel of this selector is activated at a time. The combined effect of the 1st and 2nd code generators activates only one output terminal throughout all the 154s (144 terminals in all).

The 3rd code generator consists of 93(1) and 93(2). This is driven by the 141th output of the 154s, and generates 256 different 8-bit codes sequentially (one code per 140 clock pulses). This output is fed into the address bus to which all the RAMs are connected (140 sets in all). The combined effect of this output and the output of the 154s selects only one address throughout all the RAMs at a time, and this is activated by a clock pulse through a delay circuit and the R/W terminal.

The 11th output of 42 is used for driving 93(1) and 93(2), and for resetting 93(3) and 93(4).

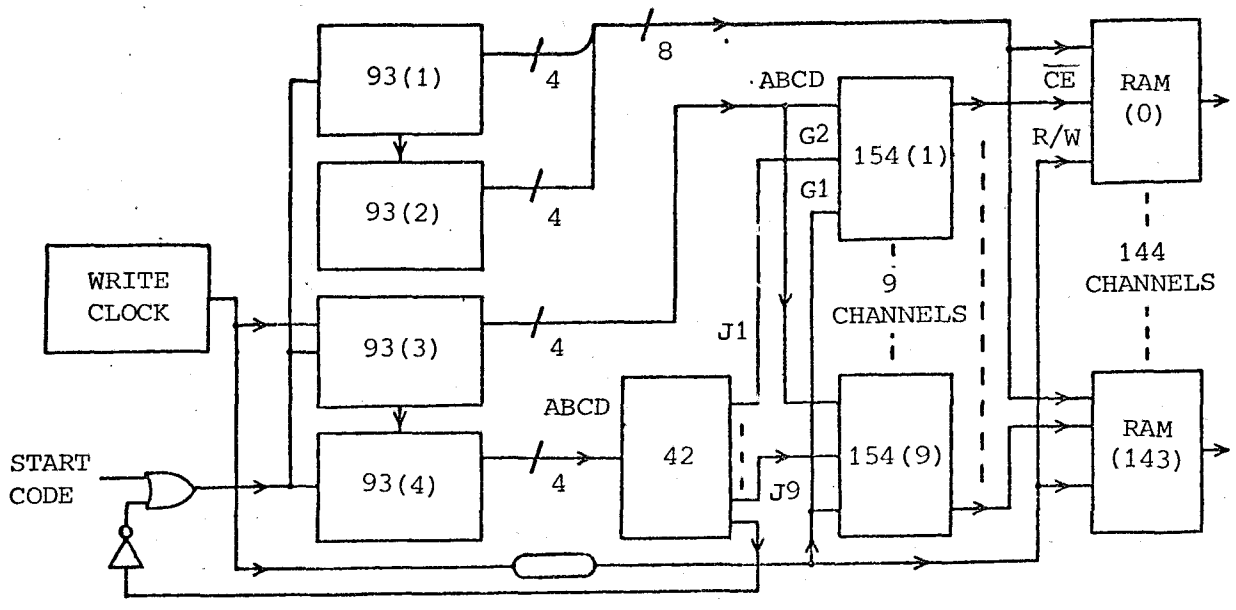


Fig. 4 Sequential write mode 1.

Sequential write mode 2 (Fig. 5)

Again three code generators are used in this mode, but in a different combination from the write mode 1.

The 1st code generator consists of 93(1) and 93(2). This is driven directly by the write clock, and generates 256 different 8-bit codes (one code per clock pulse). This output is fed into the address bus of the RAMs so that one address of each RAM is selected at a time. Only one address throughout the RAM can be selected, when the CE terminal of a particular RAM is activated.

The 2nd code generator consists of 93(3). This is driven by the 256th code of the 1st code generator, and generates 16 different 4-bit codes (one code per 256 clock pulses). This output is fed into channel selectors 154(1) to 154(9) so that one of 16 channels in each 154 is selected at a time. Only one channel throughout all the 154s can be selected, when the CE terminal of a particular 154 is activated.

The 3rd code convertor consists of 93(4). This is driven by the 16th code output of 93(3), and generates 9 different 4-bit codes (one code per 4096 clock pulses). This output is fed into 154(1) to 154(9) so that one of the 154s is selected at a time. The combined effect of 1st, 2nd and 3rd code generators selects only one address throughout all the RAMs at a time, and this address is activated by a clock pulse through the delay circuit and the R/W terminal.

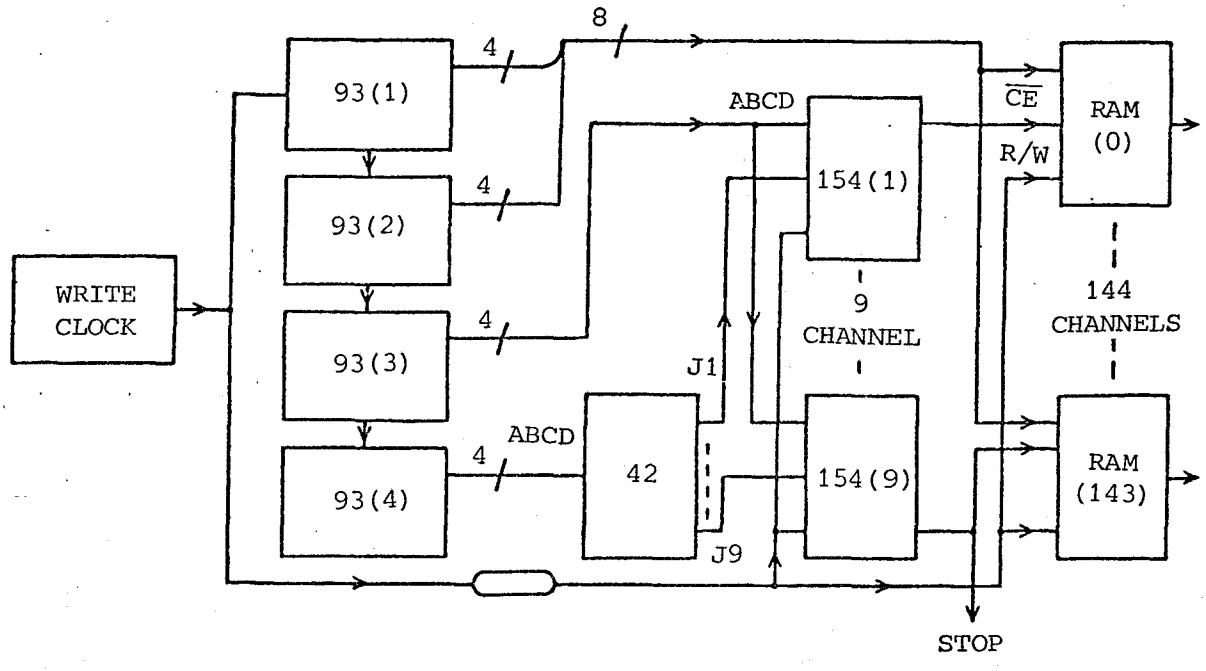


Fig. 5 Sequential write mode 2.

Sequential read modes 0 and 1 (Fig. 6)

Once data is written, by either sequential write mode 1 or 2, there is no difference in the order of written data in the memory. Therefore, any sequential read mode can be applied to read the memory written by either sequential write mode 1 or 2.

For sequential read mode 0, one code generator, consisting of 93(1) and 93(2), is used. This is driven by the read clock, through a gate which can be ignored in this mode, and generates 256 different 8-bit codes (one code per clock pulse). The output of the code generator is fed into the data bus to which all the RAMs are connected so that they are read simultaneously, data written in each set of RAM (256 words) being read sequentially. The reading data is cycled without a break until it is stopped externally.

For sequential read mode 1, two code generators are used. The first code generator consists of 93(1) and 93(2). This works in the same way as that in sequential read mode 0, except the gate is activated in this mode. The second code generator consists of 93(3), 93(4) and 93(5). This is driven directly by the write clock, and generates one-bit code (or an on-or-off code), its on-period and off-period being equal to the period of 256 clock pulses. This output is fed into the above-mentioned gate, so that the reading data is cycled at intervals until the cycling is stopped externally.

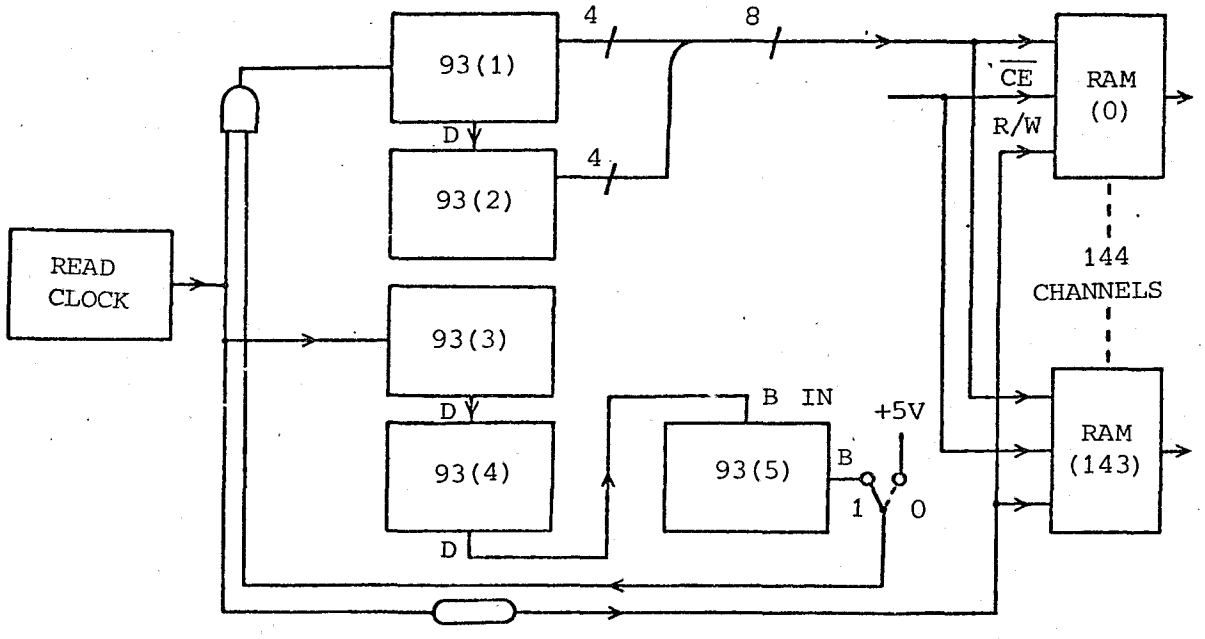


Fig. 6 Sequential read modes 0 and 1.

Random write/read mode (Fig. 7)

An input for the random read mode of this system must have the format shown in Fig. 7 at the input terminal of the system. This particular format is used for other parts within the model, and simplifies its hardware. If arbitrary input is given, this must be converted into the specified format before it is fed into the memory system.

Three registers with a timing circuit are used for converting this bit-parallel word-serial form into bit-parallel word-parallel form.

The 1st register, consisting of 75(1) and 75(2), is used for holding address A1 (8-bit word). This output is fed into the addresses of all the RAMs through the data bus. Only one address throughout all the RAMs can be selected at a time, if a particular RAM is activated through its CE terminal.

The 2nd register, consisting of 75(3) and 75(4), is used for holding address A2 (another 8-bit word). The output of this register is divided into two parts: 4 least-significant bits and 4 most-significant bits. The 1st part is fed into selector 154(1) to 154(9) in parallel so that a particular terminal within each 154 is selected. Only one particular terminal throughout all the 154s can be selected at a time, when a particular 154 is activated through its CE terminal. The 2nd part of the register output is fed into another selector, 42, so that one of its 9 channels, which are connected to 154(1) to 154(9), is selected. The combined effect of the 1st and 2nd registers selects only one address throughout all the RAMs at a time.

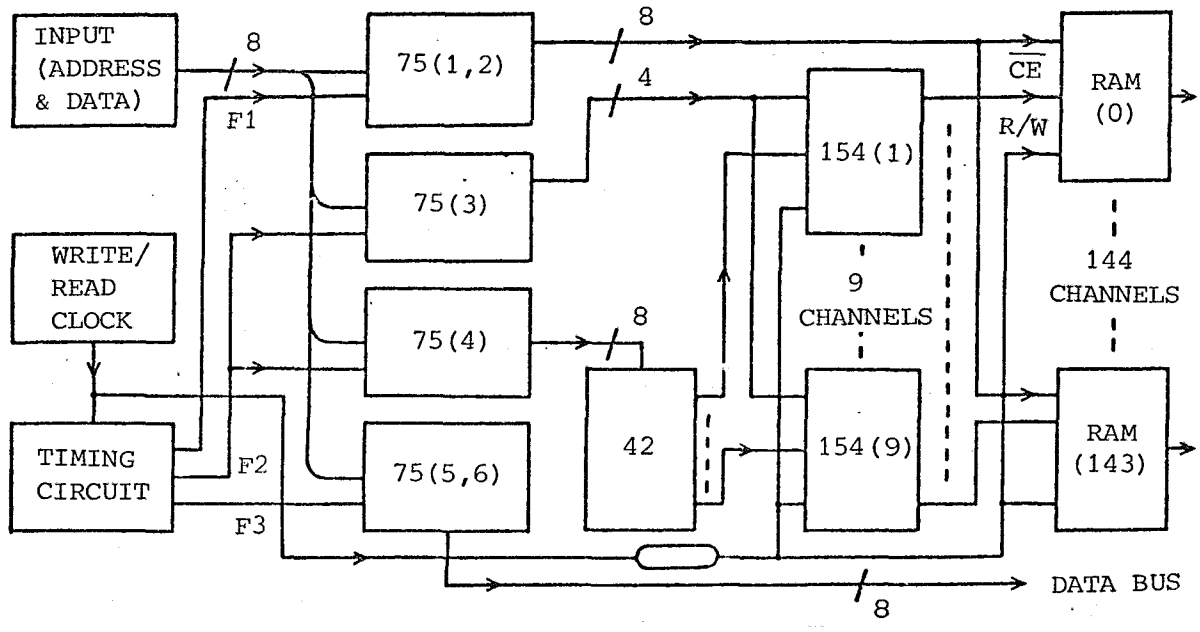


Fig. 7 Random write/read mode.

The 3rd register, consisting of 75(5) and 75(6), is used for holding data D (8-bit word). This output is fed into all the RAMs through the data bus. Since only one address throughout all the RAMs is already selected, the data is written into this address by activating this address through its CE terminal.

The operation of the random read mode is carried out in a similar way to its write mode. A set of address codes, A1 and A2, from which the data should be read, is fed into the system through its input terminal so that a particular address is selected. The written data in this address is read through the data bus by activating the RAMs.

Section (n-1)	Section n				Section (n+1)
	Address		Data	Space	
	A1	A2	D	-	

Fig. 8 Format of input for the random write/read mode.
One section corresponds to 4 clock pulses,
each sub-section corresponds to one clock pulse.
Each sub-section consists of a parallel 8-bit code.

2.4 Choice of a memory type

The following conditions are required for the type of RAMs in this application:-

1. The whole memory can be divided into sections of (8-bit X n m addresses) each of which can be controlled separately, where n > 140 and m > 200;

2. The leakage currents of all the input terminals of the memories should be small;

3. The number of control terminals per section should be small;

4. The number of different power supply voltages and the total power dissipation should be small; and

5. The total cost should be small.

Requirement 2 is due to a large number of terminals connected to a single data bus which is driven by a small number of output circuits. Requirements 3 and 4 are due to the use of a large number of components. Requirement 5 is obviously due to a limited budget.

AM9112 (AM Device), Intel 2112A, Signetics 2112 and TMS4043 (Texas Instruments) can meet the range of requirements. They are essentially the same type as a 256-word by 4-bit random access memory element using N-channel MOS devices integrated on a monolithic array. It has only two control terminals, other than address and data terminals, and is operated by a single +5V power supply requiring 150 mW. The input leakage currents of these devices, however, differ between manufacturers, AM9112 and Intel 2112A being considerably less than others. Taking into account the availability in this country at the time of designing, therefore, AM9112 has been chosen. At the time of purchase, the price of this device was £1.50 each (+300 quantity).

2.5 Choice of a type of DAC and output circuit

The analogue output of the input memory is required to drive up to 6 LEDs (forward current approximately mA each) in series with the maximum current of 12 mA (8 mA dc bias +4 mA pk-pk signal). The physical size of a DAC in this application should be small due to the limited space on the circuit board. The cost of each DAC should be small, because this is the most expensive single component in the system and 144 units of them have to be used. For these reasons, only monolithic type 8-bit DACs were considered. For example,

AD7523	(AD Device)	£1.71 (100+ price)
MC1408L	(Motorola)	2.17
DAC-08CQ	(PMI)	2.26
NE5007N	(Signetics)	2.40
ZN425E	(Ferranti)	3.50

Since the output current required exceeds the maximum current of any of these DACs, it is necessary to add a current amplifier, and to use power supply voltages other than +5V. The combination of NE5007N and 741 (an OP amplifier) has been chosen, taking into account the best availability. Note AD7523 requires an external component which makes the highest total cost in these examples.

NE5007N has negative and positive output-current terminals which can be chosen for the purpose. The polarity of the bias current can also be chosen, when it is added to the signal current through the input of the 741. These make four different combinations as shown in Fig. 9. By considering the format of the programme (described in a separate paper), the circuit shown in the 2nd column of Fig. 9 has been chosen.

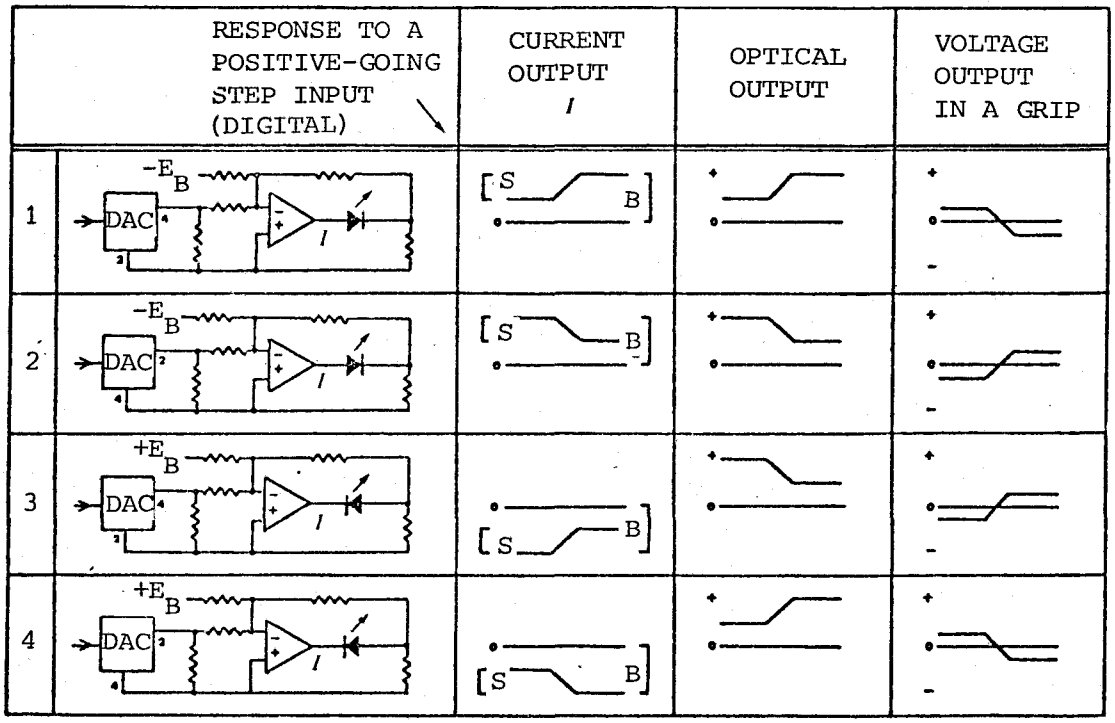


Fig. 9 Possible combinations of the output-circuit configurations.
B : Bias S : Signal

3. CIRCUIT DESCRIPTION

Fig. 10 shows the circuit diagram of the input memory, except its power supply. This circuit includes the five circuits shown in Figs. 4, 5, 6 and 7, and other peripheral circuits. The peripheral circuits are as follows:-

Switches

The five different modes of operation are obtained by using several manual and automatic switches which are controlled by the former. The manual switches are:-

Sequential-or-random switch,
Write mode switch (1 or 2),
Read-period selection switch (1, 2 or 3), and
Start switch.

The first switch is on the rear panel, and the rest of the switches are on the front panel.

The automatic switches consist of 20 sets of 1-pole 2-way logic switches, contained in five IC packages, 157(1) to 157(5), and eight sets of on-off switches contained in 4016(1) and 4016(2). The first 16 sets are used for switching between sequential and random modes. The last 4 sets of 2-way switches and all the on-off switches are used for switching between write and read modes.

Clock

The clock consists of a crystal (10 MHz ± 10 ppm) and two units of 04(3) (in a linear operation with two 1K feed-back resistors). The frequency is reduced by 90(1) to 90(4) and 93(4) and 93(6) to nf, nf/2 and nf/3, where n can be chosen (by an internal semi-fixed switch) to be 1 MHz, 100 kHz or 10 kHz. The final choice of the frequency is carried out by the read-period selector switch.

Tape-control circuit

This circuit consists of 121(3), 2/3 of 00, 30, 1/2 of 04(2), 121(2) and 1/2 of 93(5). The timing diagram for this circuit is shown in Table 10.

When switch START is activated manually, 121(3) generates a pulse. This sets the FF, consisting of 00, to a state which starts an external tape-reader. 121(3) also generates another pulse at the same time, and this pulse sets the output of 93(5) low. The start code (1111 1111) on the tape is then decoded by 30, and enters into 93(5) through 121(1). This sets the output of 93(5) high. When the tape-reading has been completed, the end code (again 1111 1111) on the tape is detected by 30. This enters into 93(5) and sets its output low. At the same time, 121(2)/6 generates a reset signal, RST, and this enters into 00/13 just before the output of 93(5) is lowered. The signal from the 00/11 resets the FF so that the tape-reader is stopped. When the whole system is switched on for the first time, a pulse is generated at 04(2)/10, and this resets the whole control circuit.

Write/Read signal generator

Several parts of the memory control circuit require a set of voltages by which the write or read mode of the whole system is indicated. This signal is generated by 93(5) (low in a write mode and high in a read mode), and is shown as CSW in Fig. 10. The complementary signal to this signal is also generated by 04(1)/8,9, and is shown as $\overline{\text{CSW}}$ in Fig. 10. The state of $\overline{\text{CSW}}$ is indicated by a red LED on the front panel; e.g. an ON state of this LED indicates that the whole system is in a read mode.

R/W-terminal control signal

Each RAM requires a signal to control its R/W terminal. This signal should be high in a read mode, and low for about 100 ns after every one words has entered into the memory. Such a signal is generated by passing the write clock through a pulse delay circuit, 04(1)/1,2,3,4. This signal is shown as R/W in Fig. 10.

$\overline{\text{CE}}$-terminal control signal

Each RAM also requires a signal to control its $\overline{\text{CE}}$ terminal. This signal should be high normally, and should be low only after each address code has entered into a RAM until just before it is removed. The actual low period of the signal differs between the write and read mode, because the period of the write and read clock are different. Such a signal is obtained at the input terminal of each 08 in circuit board M5, M12 and M19 (140 terminals in all).

This signal is generated by the write or read clock separately, and the signal is passed through a pulse-width control circuit, 121(1), and a pulse-delay circuit, 04(1)/1,2,3,4. After this, the signal passes through different circuits, depending on the write or read mode. In a write mode, the signal passes through 32/4,6; and a selected channel of 154(1) to 154(9); and enters into the input terminal of a selected 08 on boards M5, M12 and M19. In a read mode, the signal passes through 32/1,3; one of 04(1)/5,6, 04(1)/11,10 or 04(1)/13,12; also all the 04s on board M5, M12 or M19; and enters into the input terminal of all the 08s on boards M5, M12 or M19. After 04(1)s, the circuit is divided into three groups, because of their 'fan-out' capability.

Read-pulse width control circuit

When a set of words written in a RAM is read continuously, there are inherent intervals between the adjacent words. When such a set of words is converted into an analogue voltage (or current) by an ADC, its output also contains the intervals other than the converted values of useful signal. In order to overcome this, each interval must be adjusted to be very small compared with the period of each useful signal voltage. This adjustment is carried out by a potentiometer (100K) connected to 121(1)/9.

Register-timing circuit

Three groups of registers, 75(1) to 75(6), shown in Fig. 7, require three pulses, F1, F2 and F3, which have different widths and timings. These pulses are generated by 93(7), 2/4 of 04(2), and 3/4 of 08. When all the registers have completed the registration of address and data, another pulse is required to execute a write or read of the data into the address. This pulse is taken from 08/3, and passed through another pulse-delay circuit, 04(2)/1,2 and 04(2)/3,4, a pulse shaper, 121(4), and fed into the same circuits as for a sequential mode.

Memory, DAC and output circuit

The system has 140 channels of analogue current output each of which drives up to 6 LEDs (824 in all). All the channels are identical, and one of them is shown on the right hand side of Fig. 8. One channel consists of two RAM packages, 9112(1) and 9112(2), two IC packages of switching circuit, 4066(1) and 4066(2), a DAC, 5007, and a current output circuit, 741.

The address terminals of the RAMs are permanently connected to the address bus (8 channels). The data terminals (input and output common, also 8 channels) of the RAMs are permanently connected to the input terminals (8 channels) of the DACs. The data terminals of the RAMs are also connected to the data bus through the switching circuits only when the system is in a sequential write mode, or in a random write and read modes. This arrangement is necessary for a simultaneous reading of RAMs, in a sequential mode, each of which store different data.

The reference voltage (terminal 15) of each DAC is taken from the +12V supply line through a 50K potentiometer by which the full scale of the output is set.

The output current (at terminal 4) of the DAC is proportional to its digital input, the maximum current being mA. The final current output required to drive up to 6 LEDs in series is

8 mA (bias current) + 4 mA pk-pk (signal)

The bias current is necessary to operate each LED in a linear range. In order to satisfy these conditions, a 741 is inserted between each DAC and a set of LEDs. The output signal current of the DAC is converted once into a signal voltage by a 1K resistor. Then a constant voltage of -12V is added to the signal voltage through a 30K resistor, which is connected to the inverted input terminal of the 741. The output current of the 741 is sampled by a 100Ω resistor as a voltage, and this is fed back to the inverted input of the 741. In this way, the output current becomes independent of the load (from a short circuit to 6 LEDs). The details of the design of this part of the circuit are described in Appendix .

The DACs and output circuits are operated by a ±12V power supply for driving up to 6 LEDs, while the rest of the system is operated by a single +5V power supply.

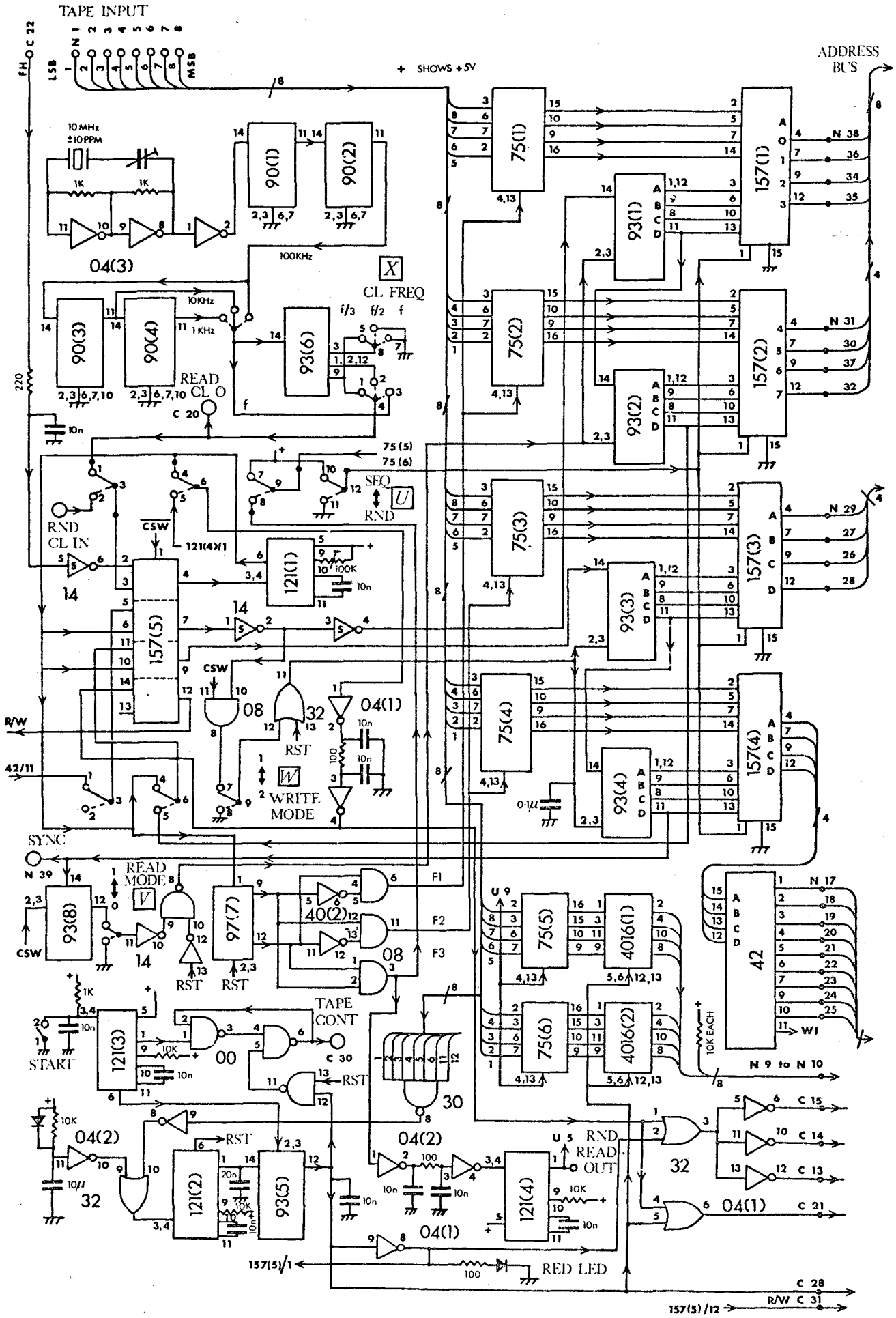


Fig. 10 Circuit diagram of the input memory.
(Continued to the next page).

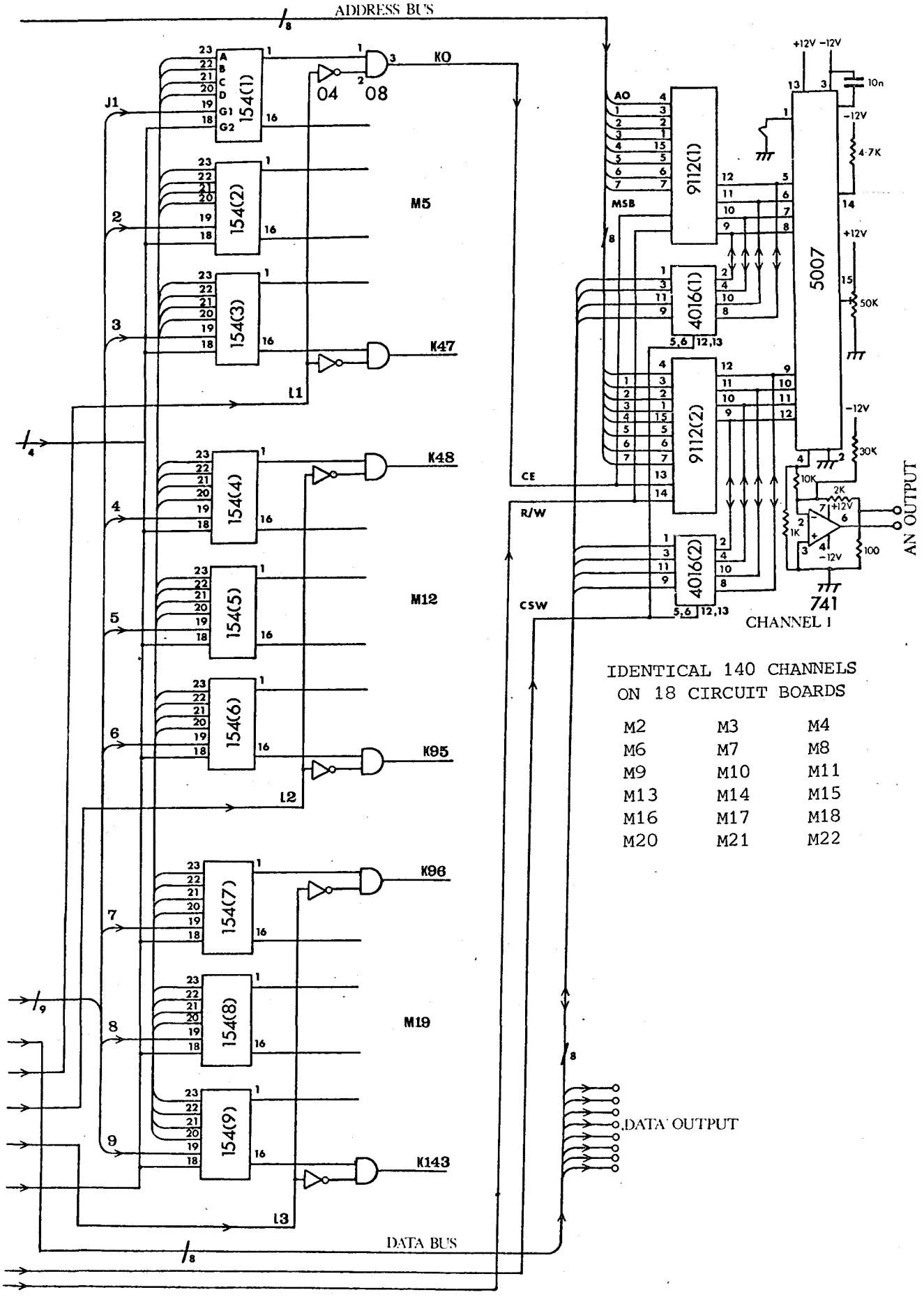


Fig. 10 (Continued from the previous page).

Read modes control circuit

This circuit selects read mode 0 or 1, the former being a repeated reading of the memory without intervals, and the latter with intervals of 256 words. The circuit consists of 93(8), 14/10,11 and 08/8,9. 93(3) and 93(4) are also used as a pulse counter in the reading modes.

The read clock enters in parallel into the address-code generator, 93(1) and 93(2); and the pulse counter, 93(3) and 93(4). The reset signal, which is generated only at the start of reading, enters into the two circuits simultaneously, so that they work in complete synchronization. Note the reset signal, RST, enters into the 93(1) and 93(2) through 14/13; and into the 93(3) and 93(4) through 32/12.

In read mode 0, 93(3) and 93(4) have no effect on reading, although they are working and pulses (pulse width 256 words, intervals also 256 words) are obtained at 93(8)/12. Note switch 'V' cuts off the output of 93(8)/12. Consequently, the reading of the memory continues without intervals.

In read mode 2, where switch 'V' connects 93(8)/12 to 14/11, the pulses enters into the 93(1)/2,3 and 93(2)/2,3 so that they are interrupted periodically (both the active and rest periods of 256 words). See Table 12 for the timing diagram.

Protection circuits

The data bus is linked with other circuits by 4016s (8 channels in the control circuit board, and 560 channels in the memory boards). In a sequential read mode, all the 4016s are in an off state, and each channel of the data bus is electrically floating with a very high resistance. In order to avoid the electro-static charge of this line, each line is connected to +5V line through a 10K resistor as shown near 4016(1).

Noise filtering circuits

The power supply terminals of each of 93s and 121s are shunted by 0.1μ capacitor within each package.

Other than the above usual method of noise filtering, the following two circuits are important in this particular control board:-
A 0.1μ capacitor by-passing the terminals 93(3)/2,3 and 93(4)2,3 to earth: without this capacitor, the address code in write modes will be disturbed, resulting in a periodical noise in the final output waveform.

A 0.1μ capacitor with 200Ω resistor by-passing the input from C22 to earth: without this filter, a similar effect to the above will appear.

4. POWER SUPPLY AND PROTECTION CIRCUITS

In order to drive the input memory, three regulated dc-voltages are required as shown in Table 2. Three different types of power supply units (all standard products) are employed as shown in Table 3. The memory cabinet and power supply cabinet are separate, connected only by a cable (about 30 cm long) with a 20-pin connector. Beyond the connector, an independent conductor is used for each circuit board. Each voltage is monitored at the connector, and fed back to the voltage sensing terminals of each power supply, except for the +12V unit which does not have sensing terminals.

The main memory units withstand between -0.5V and +7.0V, while the DAC units withstand between -18V and +18V. Therefore, protection against an accidental supply-line voltage rise is required. The accident which is most likely to occur is that the -12V or +12V line makes contact with the +5V line within the system. Another accident, which is less likely to occur, is the 240V ac-line contacting any of the dc lines.

In order to minimize the risk of such an accident, most of the -12V or +12V line terminals are surrounded by conductors which are connected to the ground line.

As a further protection, the circuit shown in Fig. 12a has been added to the power supply. This circuit works as follows:-

Accidental contact of the +12V line to the +5V line

The voltage on the +5V terminal is constantly monitored through the voltage sensor of the circuit (shown in Fig. 12a), and this is compared to the reference voltage of 6.2V (fixed by a zener diode). If the sensor voltage becomes higher than the reference voltage, comparator 319(1) generates a positive-going voltage which activates thyristor 106S5(1). Then the +12V line is shunted by the thyristor, within 80 nano seconds. At the same time, comparator 319(2) also generates a positive-going voltage and activates thyristor 106S(2). This thyristor activates a latch relay by which the 240V ac-line for the whole system is cut off within about 50 milli seconds.

Since 319(2) and 106S(2) have to be operated after the regulated +12V power output is shut down, they are driven by an unregulated voltage (+17V to +20V) which is available within the same power supply unit even after the shut down.

The latch relay has been designed for the purpose, by using a standard micro switch and a solenoid. Fig. 13 shows its construction, and Fig. 14 shows its operation. Once the relay is activated by the primary voltage, the secondary circuit is opened, and stays in an open state independent of the primary voltage after the first activation. The relay can be reset only by manual operation, after the cause of the accident has been rectified.

Accidental contact of the -12V line to the +5V line

The +5V line is kept in a regulated condition, even when the -12V line contacts it, except for an instantaneous voltage drop (not below 0V). During an accidental contact, about 150 mA of current flows into the -12V supply terminal.

The protection circuits have been tested successfully with the actual full load.

Table 2 DC power requirement

Circuit board	Number of boards	Typical current per board			Unit
		+5V	-12V	+12V	
M1	1	480	-	-	mA
M5, M12, M19	3	350	-	-	mA
M2 to M22 except the above 4 boards	18	500	72	155	mA
Total current		10530	1296	2790	mA
Total power		52.7	15.5	33.5	W

The power requirement for the +12V line depends on its load; the value shown is the maximum. The total power of the three voltages is 101.5 W.

Table 3 Power supply units used

Nominal voltage		+5	-12	+12	V
Maximum current		20	2	3	A
Make		Gould	Gresham	Countant	-
Model		MG5-20	GXL-12/2	HC12-3.0	-
Regulation method		Switching	Linear	Linear	-
Input	Voltage	115 to 240	100 to 250	105 to 240	V
	Frequency	45 to 440	45 to 450	50 to 60	Hz
Output	Line regul. ±10% change	±0.1	±0.01	±0.05	%
	Load regul. Zero to full	±0.1	±0.04	±0.1	%
	Temp. coeff.	±0.01	±0.02	±0.03	%/°C
	Impedance @ 100 kHz	100	250	250	mΩ
	Noise @ bandwidth	50 30	2.0 1	3.0 20	mV pp MHz
Protection	Over voltage	120 to 130	No	No	% FS
	Over load	110	110	110 to 250	% FS
Operating temperature		-10 to +70	-15 to +50	0 to +50	°C
Power efficiency		70	50	55	%
Case dimensions		164×105×88	204×108×87	143×114×63	mm^3
Weight		2.0	2.3	1.8	Kgr

All the figures are based on manufacturers' specifications.

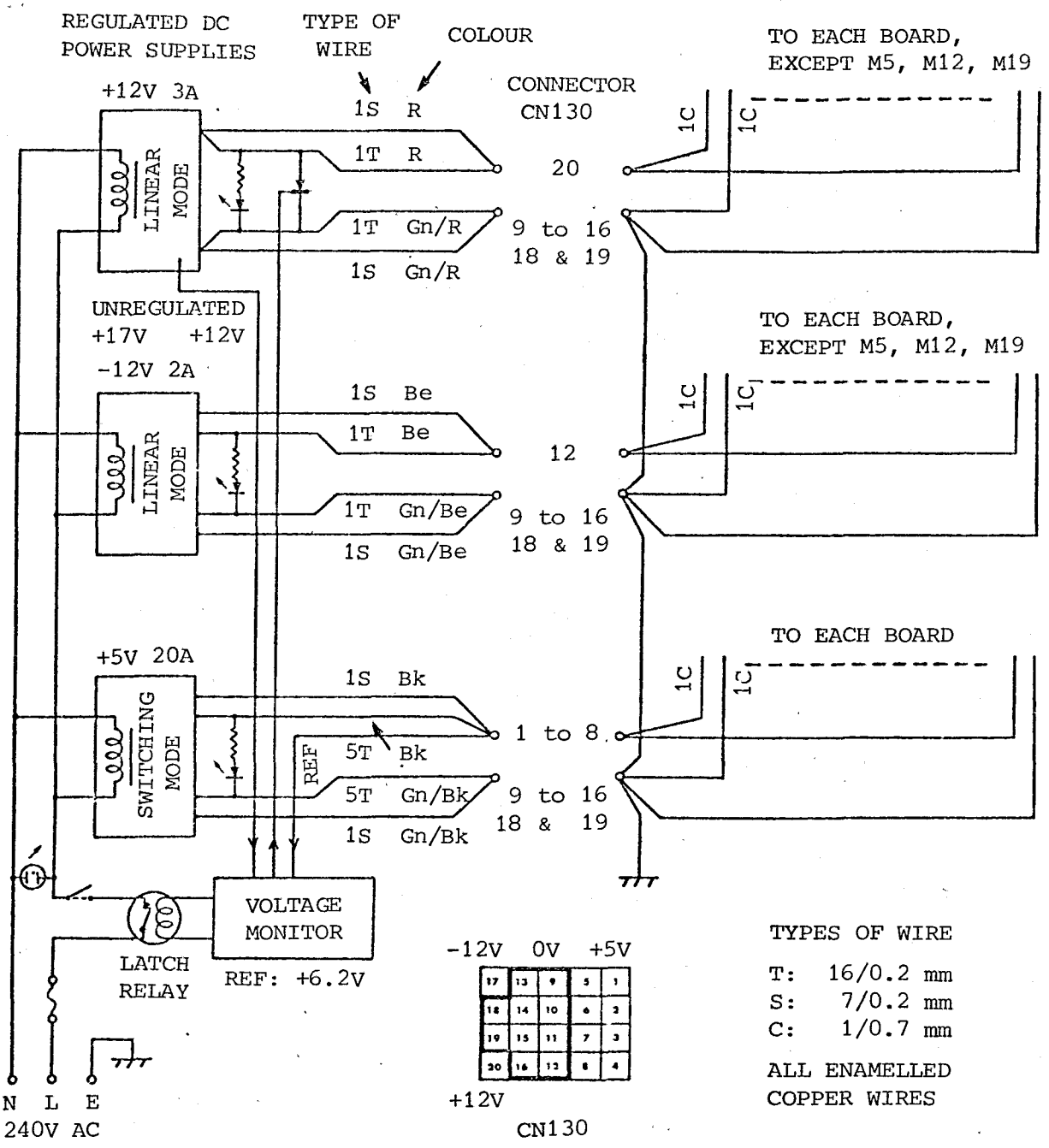


Fig. 11 Circuit diagram of the power supply unit.

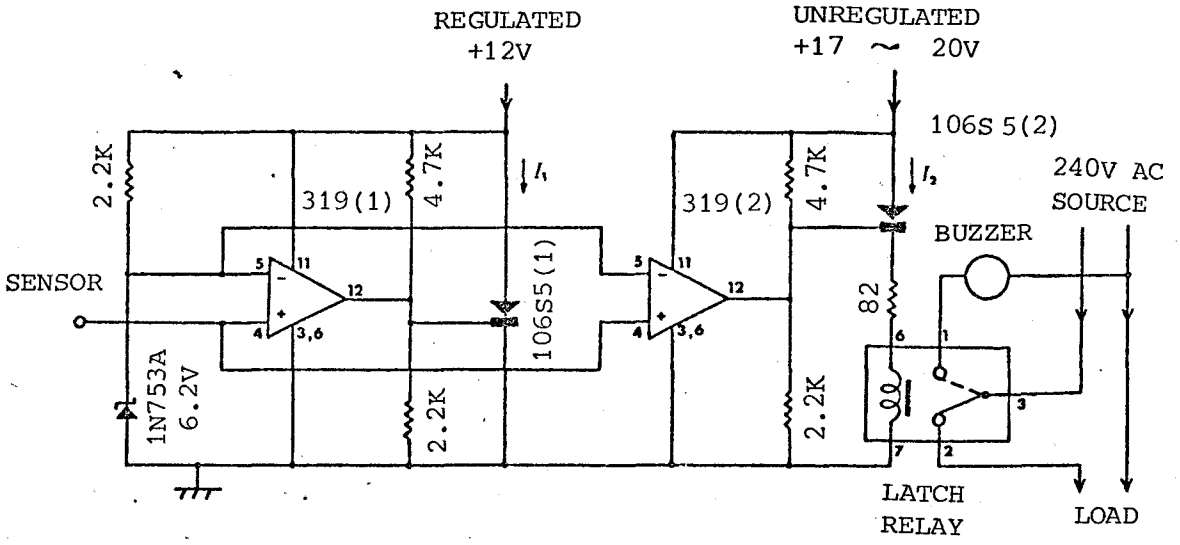


Fig. 12a Voltage monitor and protection circuit.
I_1 = 1.8A after 106S5(1) has been activated by the instantaneous rise (>6.2V) of the sensor voltage.
I_1 = 10A, if the sensor voltage is kept >6.2V.
I_2 = 75mA after 106S(2) has been activated by the same sensor, either instantaneously or continuously.

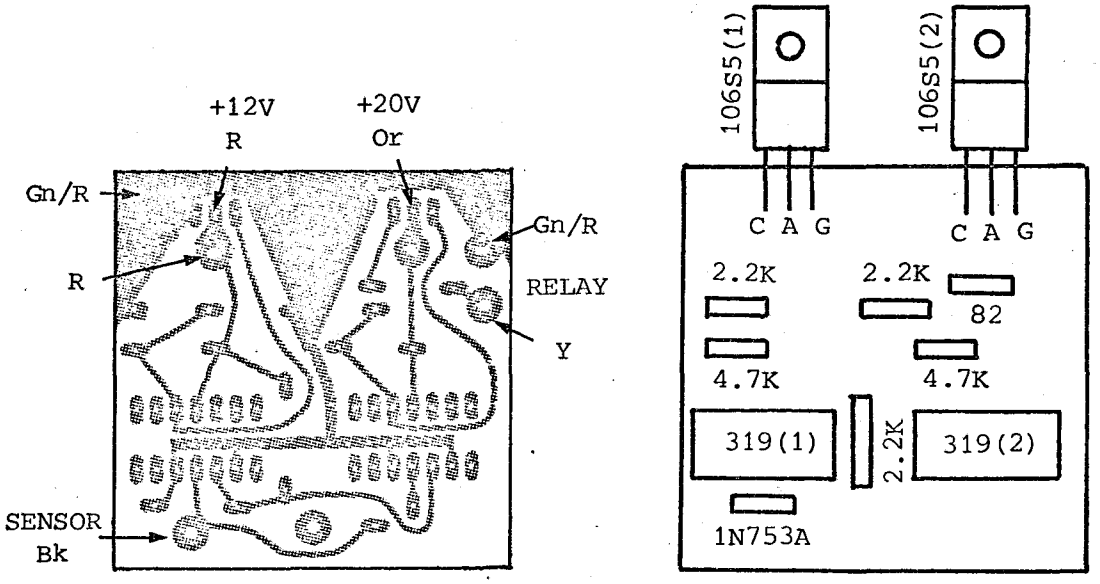


Fig. 12b Component arrangement of the board shown in Fig. 12a.

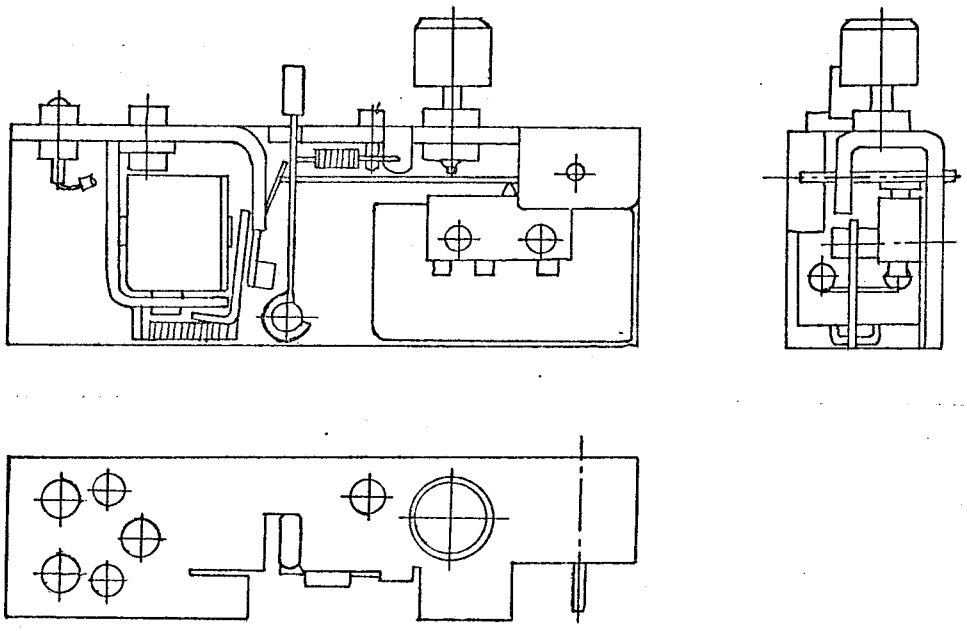


Fig. 13 Construction of the latch relay (full scale). The actual unit is contained in a transparent case with an 8-pin connector.

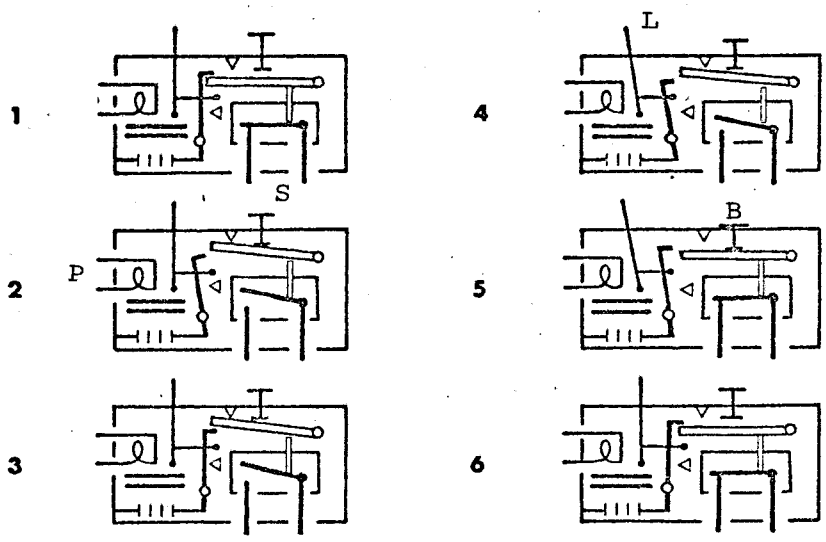


Fig. 14 Action of the latch relay shown in Fig. 13.
1 Normally the secondary circuit, S, is closed.
2 If the primary circuit, P, is energized, S is opened.
3 For resetting, press the lever, L.
4 Press the button, B, and
5 Release L.

5. PHYSICAL CONSTRUCTION

The previous input memory was linked with external systems through mode then 300 terminals which are connected internally to 22 printed-circuit board connectors. These parts, including a board frame and outer cabinet, have been reused for the new input memory in order to save work. In other words, the physical dimensions and terminal arrangements of all the new circuit boards have been designed to be the same as the previous ones, except for the control circuit board, M1. This has made the component density on each new board very high, and even the use of multiple flat cable on a board was necessary. This has also made the order of actual channels on each circuit board appear odd.

The input memory system has been divided physically into two parts: a main memory cabinet and a power supply cabinet, as shown in Fig. 15.

Memory cabinet

This consists of:-

Control circuit board, M1, with a front control panel;

Output monitor terminals;

3 sub control-circuit boards, M5, M12 and M19;

18 memory circuit boards, M2 to M4, M6 to M11, M13 to M18, M20 to M22;

Rear panel with a switch and connectors;

6 sets of multiple connector for output;

Board frame with connectors and wirings; and

Cabinet case with its front and rear covers.

Fig. 16 shows the three types of circuit board, 22 boards in all. Figs. 17 to 23, and Tables 4 to 6 show their details. Tables 5 to 8 show connections of terminals in the memory cabinet.

Circuit board M1, which requires more frequent and complex examinations than other boards, has long flexible wires between its edge-connections and the cabinet, so that the board can be examined in a working state outside the cabinet.

The rest of the boards have to be disconnected from their edge connectors for detailed examinations. Note, the 18 memory boards (M2 to M22) can be examined with the memory test unit (chapter 6.1). The three boards (M5, M12 and M19) have enough spaces for examination in a working state, when the memory boards are extracted from the cabinet.

A method of extracting the memory boards with a simple tool is shown in Appendix 5.

Power supply cabinet

This cabinet contains the three power-supply units, voltage monitoring circuit, and protection circuits with its reset switches.

Fig. 15 Memory cabinet (top) and power supply cabinet (bottom).

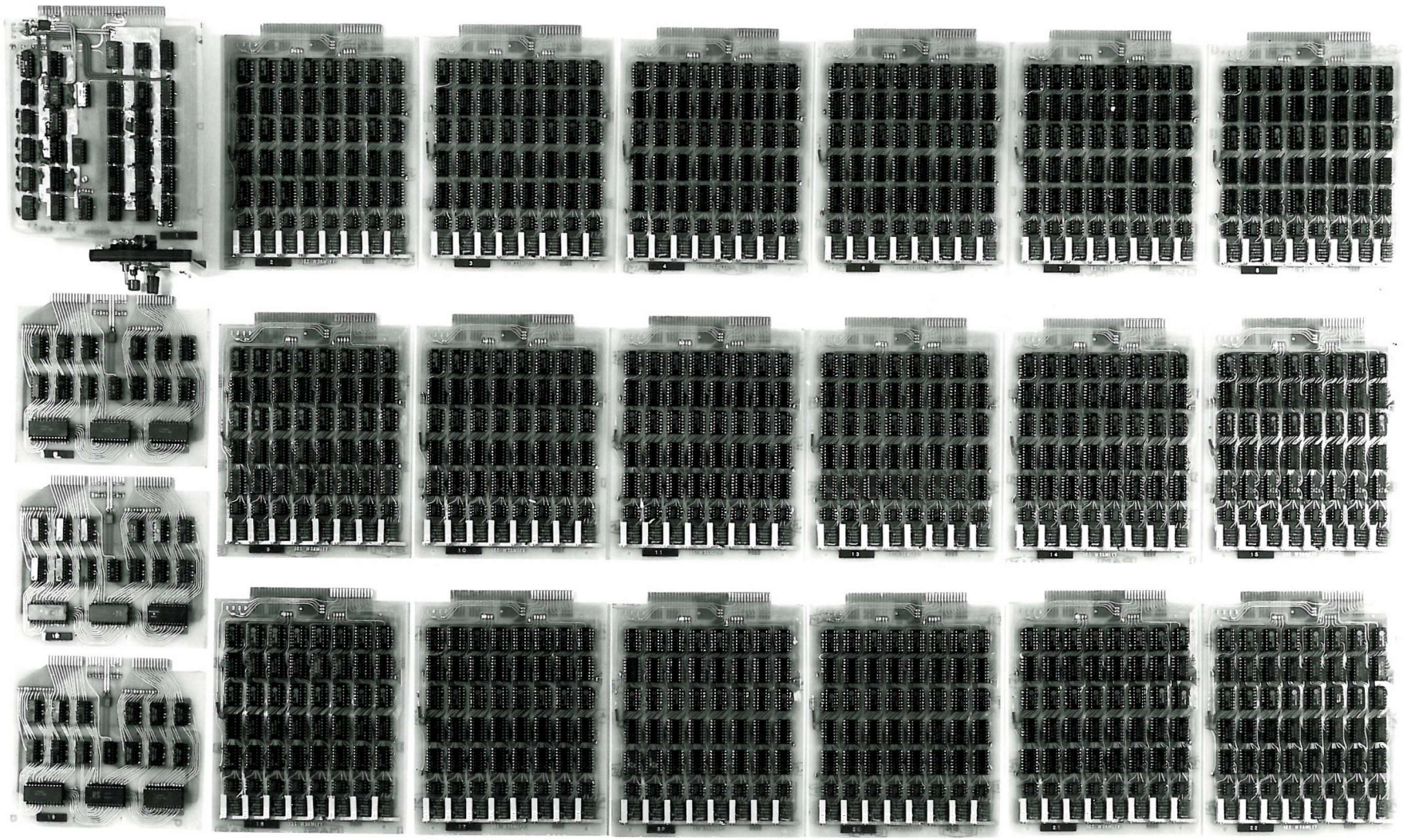


Fig. 16 The circuit boards contained in the memory cabinet.
Control circuit board, M1 (top left); three sub-control boards,
M5, M12, M19 (bottom left); and 18 memory boards, M2 to M22.

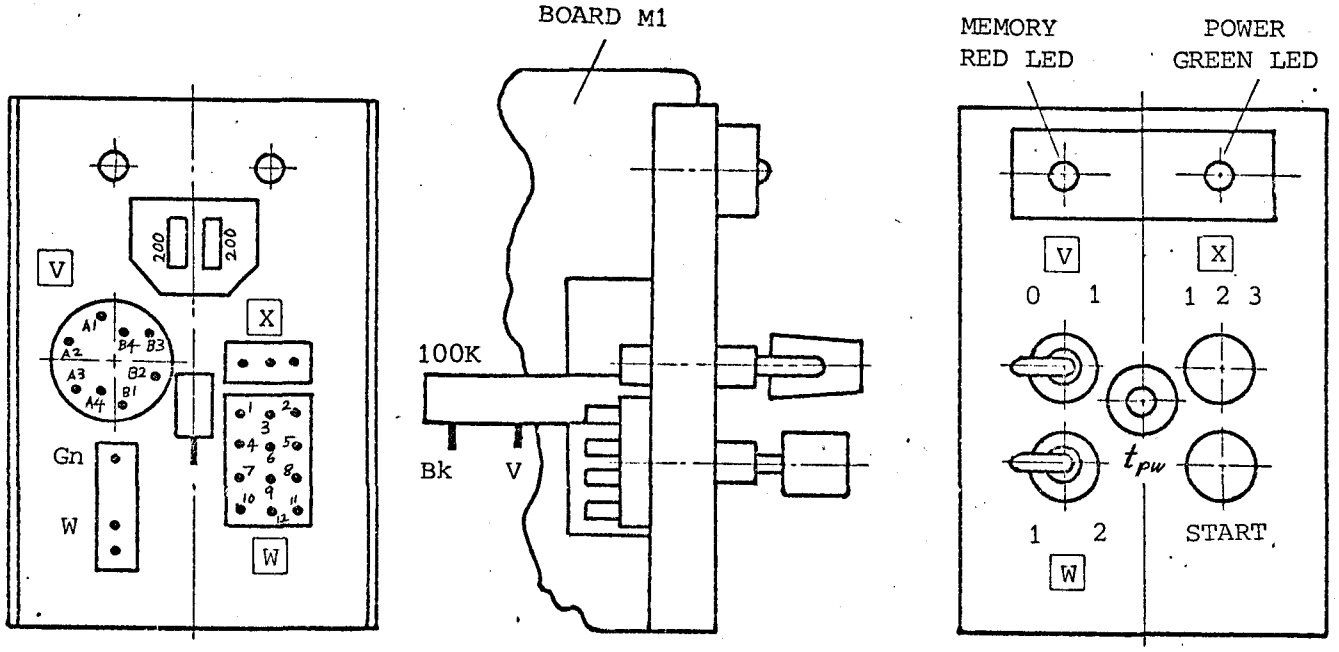


Fig. 17 Front panel of the memory cabinet.

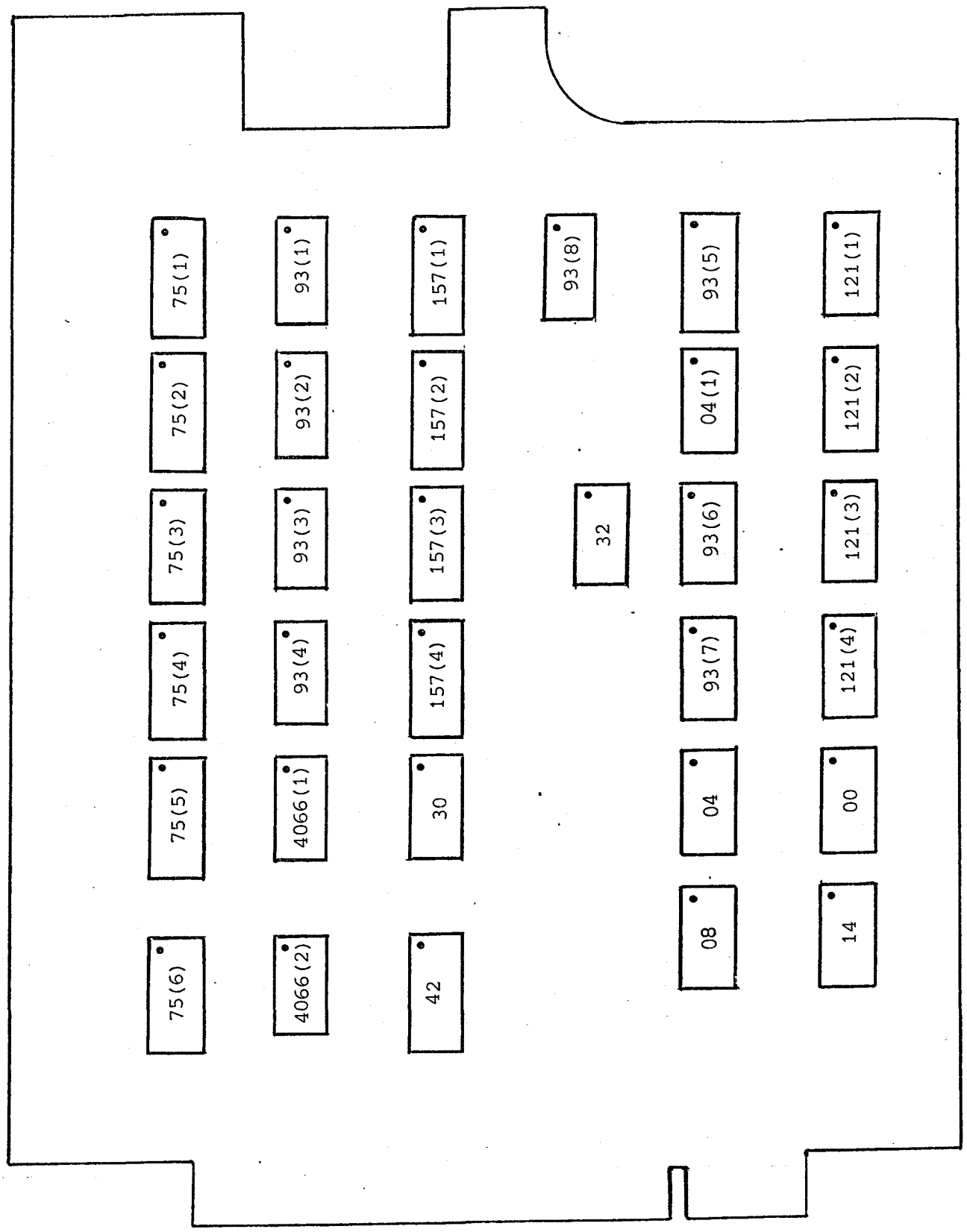


Fig. 18a Control circuit board, M1.
(Component side).

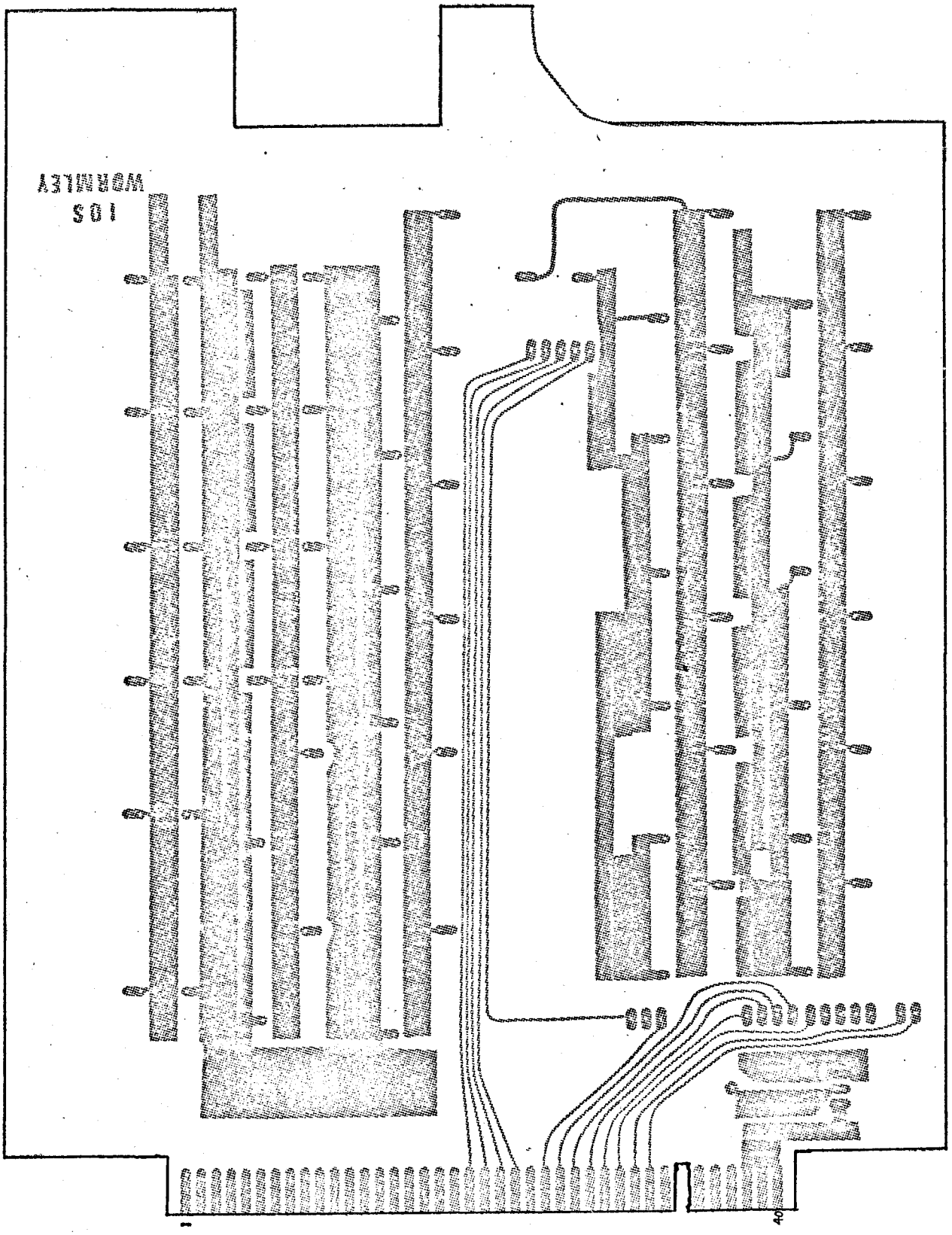


Fig. 18b Control circuit board, M1.
(Conductors on the component side).

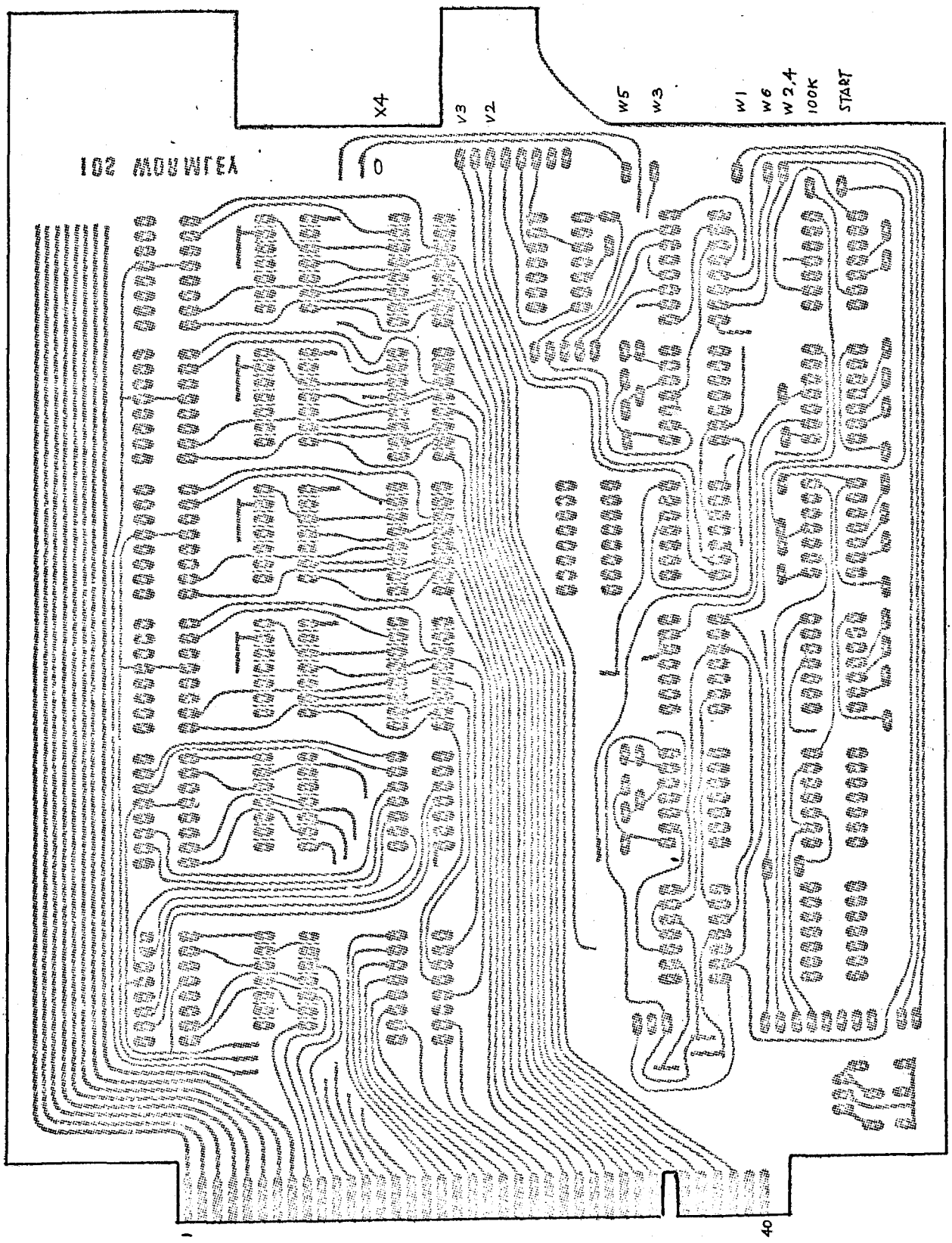


Fig. 18c Control circuit board, M1.
(X-ray view of the non-component side).

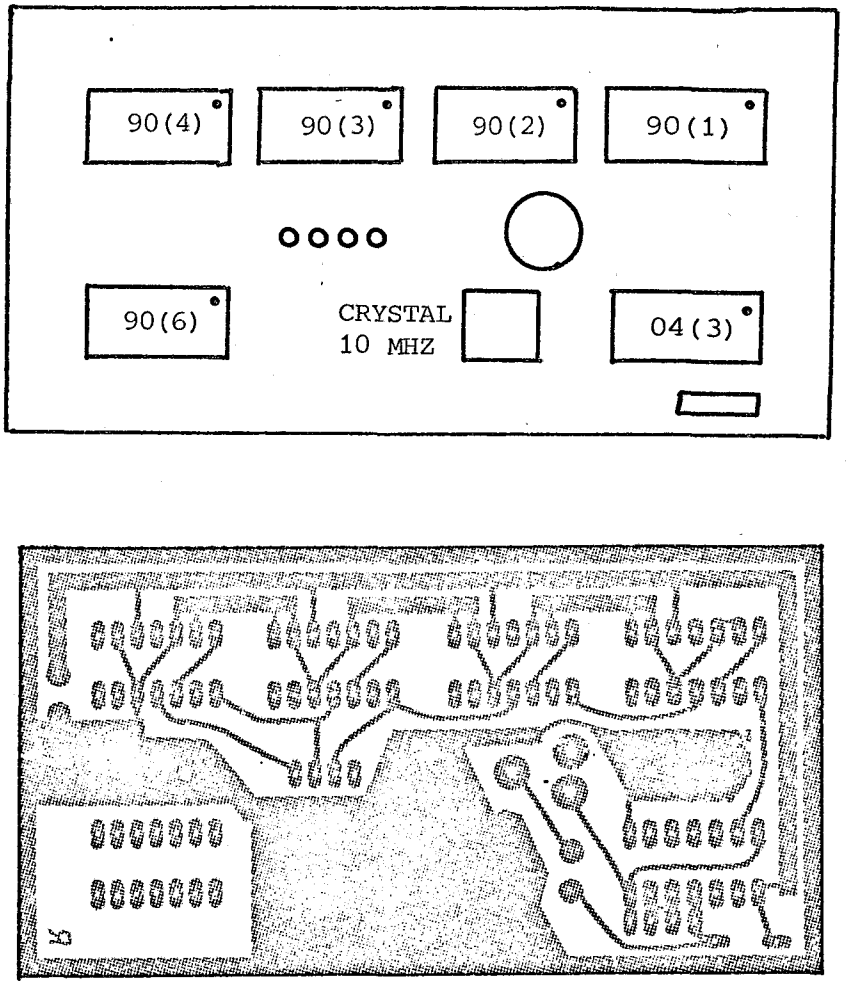


Fig. 18d Additional board to the control circuit board, M1. Component side (top), and the X-ray view of the non-component side (bottom).

Table 4 Connections of the control circuit board, M1.

Board M1 pin No.		Connected to	
N 1	Bn	CN103/1	Tape Out 1
N 2	R	/2	2
N 3	Or	/3	3
N 4	Y	/4	4
N 5	Gn	/5	5
N 6	Be	/6	6
N 7	V	/7	7
N 8	Gy	/8	8
N 9	Bn	CN103/14	Data Bus 1
N10	R	/15	2
N11	Or	/16	3
N12	Y	/17	4
N13	Gn	/18	5
N14	Be	/19	6
N15	V	/20	7
N16	Gy	/21	8
N17	Bn	M 5 /23	J1
N18	R	/24	J2
N19	Or	/25	J3
N20	Y	M12 /23	Select. J4
N21	Gn	/24	J5
N22	Be	/25	J6
N23	V	M19 /23	J7
N24	Gy	/24	J8
N25	W	/25	J9
N26	Bk	/18	C
N27	Gy	M5 /17	Select. B
N28	W	M12 /19	D
N29	V	M19 /16	A
N30	V	/7	A5
N31	Be	/6	A4
N32	Gy	/8	A7
N33	-	Slot	Address Bus -
N34	Or	18bds/3	A2
N35	R	/4	A3
N36	Y	/2	A1
N37	Bn	/5	A6
N38	Gn	/1	A0
N39	Or/Be	M1/V4	SYNC Q (RP)
N40	-		

Board M1 pin No.		Connected to
C13	Or/Gn	M19/N27 L3
C14	Or/Bn	M12/N27 L2
C15	Or/R	M5/N27 L1
C16	Bn	M1/U1 (RP)
C17	-	
C18	W	M1/U12 (RP)
C19	Gy	M1/U9 (RP)
C20	Or/Bk	SEQ R CLK O (RP)
C21	Gy/Be	M5,M12,M19/22 'P'
C22	W	CN103/9 W-CL
C23	Or	M1/U3 (RP)
C24	Be	M1/U6 (RP)
C25	V	M1/U8 (RP)
C26	Y/R	RWD R CLK O (RP)
C27	W/Bk	Not used
C28	R/Bk	C9 of all 18 bds
C29	Y	M1/U4 (RP)
C30	W/Or	CN103/10, 12
C31	W/Gn	C11 of all 18 bds
C33	-	Slot
C34	Gn/Bk	Common (OV)
C35		
C36		
C37		
C38		
C39	Bk	+5V supply
C40		

(RP) : Rear panel
R-CL : Read clock
18bds: 18 boards, M2 to M4, M6 to M11, M13 to M18, M20 to M22.
C : Component side
N : Non-component side

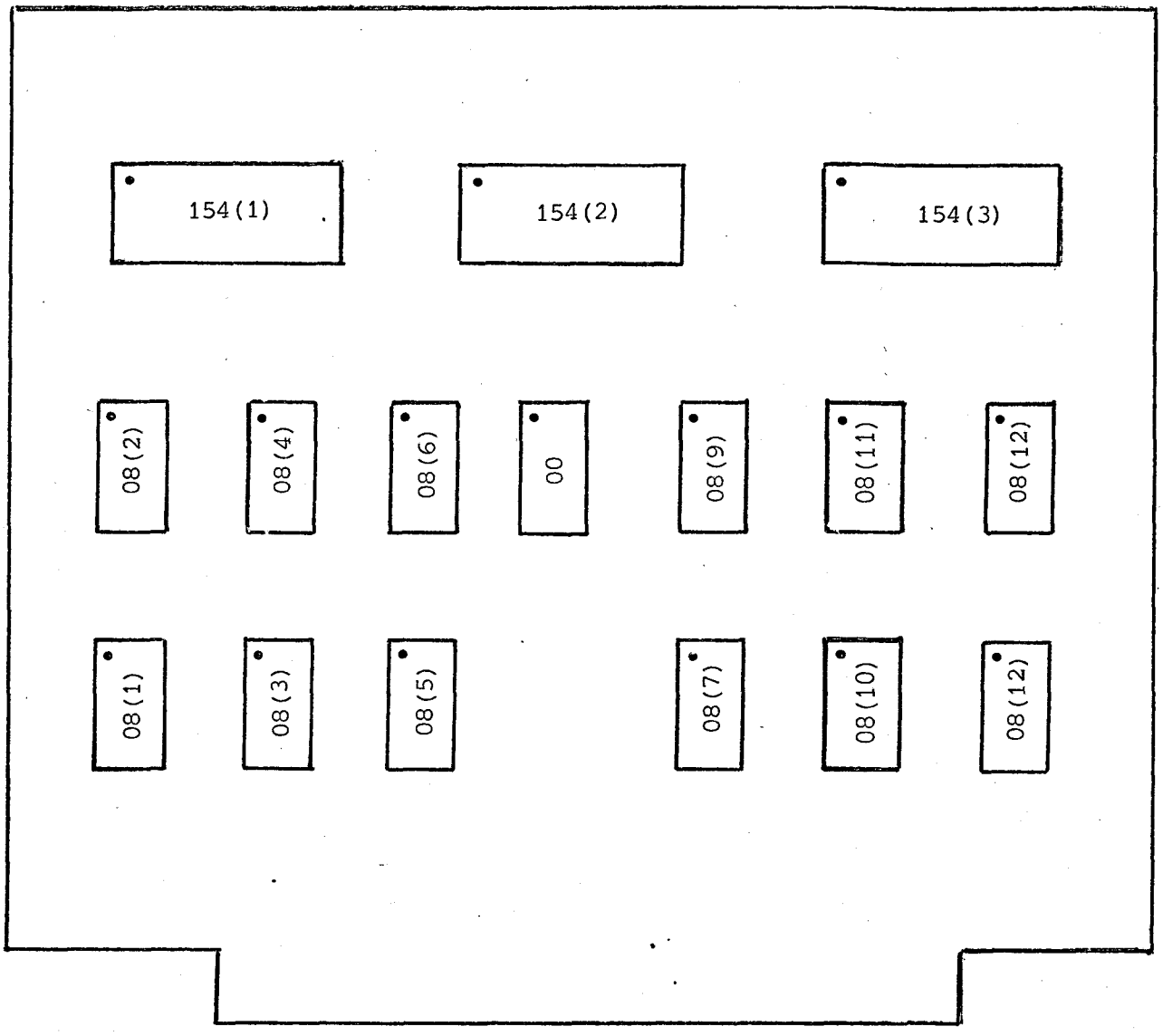


Fig. 19a Sub-control circuit board, M5, M12 or M19. (Component side).

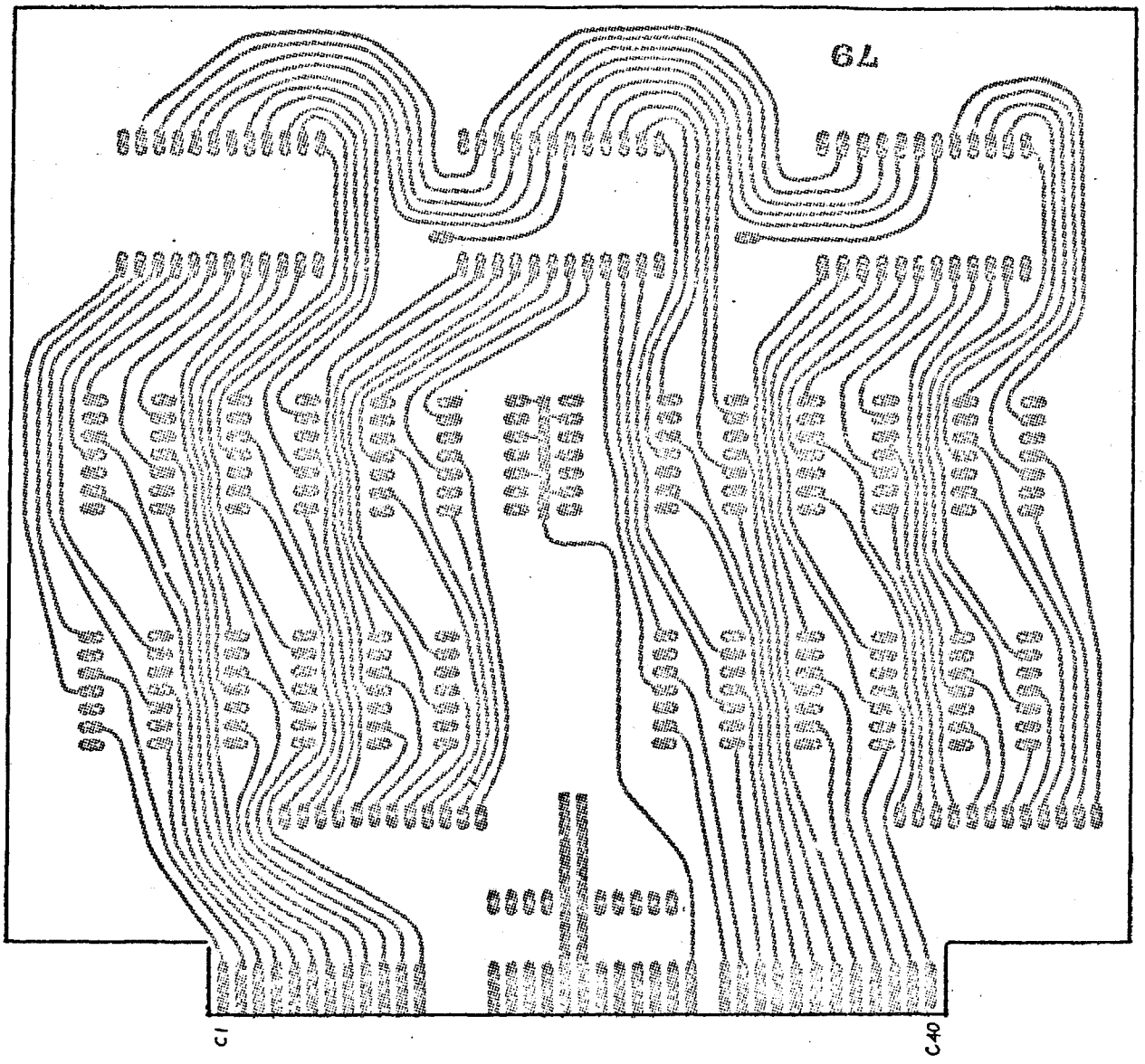


Fig. 19b Sub-control circuit board, M5, M12 or M19.
(Conductors on the component side).

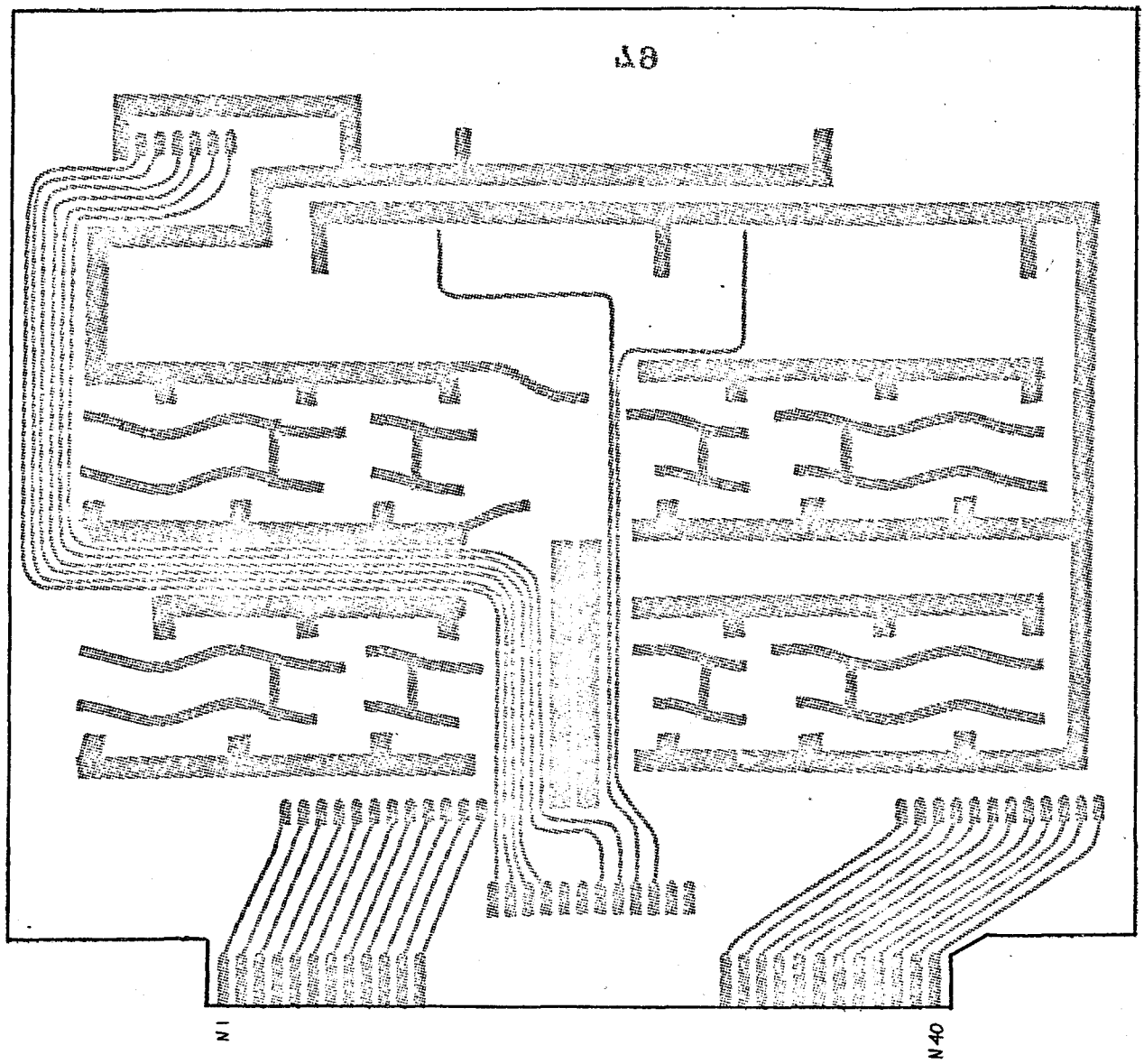


Fig. 19c Sub-control circuit board, M5, M12 or M19. (Non-component side).

Table 5 Connections of boards, M5, M12 and M19.

M5	Connection	
C 1	M2/C10	K 0
C 2	C11	K 1
C 3	C12	K 2
C 4	C13	K 3
C 5	M3/C10	K 4
C 6	C11	K 5
C 7	C12	K 6
C 8	C13	K 7
C 9	M4/C10	K 8
C10	C11	K 9
C11	C12	K10
C12	C13	K11
C16	M1/N29	A
C17	N27	B
C18	N26	C
C19	N28	D
C20	CN130/1	+5V
C21	9	0V
C22	M1/C21	P
C23	N7	J1
C24	N18	J2
C25	N19	J3
C26	-	-
C27	M1/C15	L1
C29	M2/C27	K24
C30	C28	K25
C31	C29	K26
C32	C30	K27
C33	M3/C27	K28
C34	C28	K29
C35	C29	K30
C36	C30	K31
C37	M4/C27	K32
C38	C28	K33
C39	C29	K34
C40	C30	K35
N 1	M6/C10	K12
N 2	C11	K13
N 3	C12	K14
N 4	C13	K15
N 5	M7/C10	K16
N 6	C11	K17
N 7	C12	K18
N 8	C13	K19
N 9	M8/C10	K20
N10	C11	K21
N11	C12	K22
N12	C13	K23
N29	M6/C27	K36
N30	C28	K37
N31	C29	K38
N32	C30	K39
N33	M7/C27	K40
N34	C28	K41
N35	C29	K42
N36	C30	K43
N37	M8/C27	K44
N38	C28	K45
N39	C29	K46
N40	C30	K47

M12	Connection	
C 1	M9/C10	K48
C 2	C11	K49
C 3	C12	K50
C 4	C13	K51
C 5	M10/C10	K52
C 6	C11	K53
C 7	C12	K54
C 8	C13	K55
C 9	M11/C10	K56
C10	C11	K57
C11	C12	K58
C12	C13	K59
C16	M1/N29	A
C17	N27	B
C18	N26	C
C19	N28	D
C20	CN130/1	+5V
C21	9	0V
C22	M1/C21	P
C23	N20	J4
C24	N21	J5
C25	N22	J6
C26	-	-
C27	M1/C14	L2
C29	M9/C27	K72
C30	C28	K73
C31	C29	K74
C32	C30	K75
C33	M10/C27	K76
C34	C28	K77
C35	C29	K78
C36	C30	K79
C27	M11/C27	K80
C38	C28	K81
C39	C29	K82
C40	C30	K83
N 1	M13/C10	K60
N 2	C11	K61
N 3	C12	K62
N 4	C13	K63
N 5	M14/C10	K64
N 6	C11	K65
N 7	C12	K66
N 8	C13	K67
N 9	M15/C10	K68
N10	C11	K69
N11	C12	K70
N12	C13	K71
N29	M13/C27	K84
N30	C28	K85
N31	C29	K86
N32	C30	K87
N33	M14/C27	K88
N34	C28	K89
N35	C29	K90
N36	C30	K91
N37	M15/C27	K92
N38	C28	K93
N39	C29	K94
N40	C30	K95

M19	Connection	
C 1	M16/C10	K 96
C 2	C11	K 97
C 3	C12	K 98
C 4	C13	K 99
C 5	M17/C10	K100
C 6	C11	K101
C 7	C12	K102
C 8	C13	K103
C 9	M18/C10	K104
C10	C11	K105
C11	C12	K106
C12	C13	K107
C16	M1/N29	A
C17	N27	B
C18	N26	C
C19	N18	D
C20	CN130/1	+5V
C21	9	0V
C22	M1/C21	P
C23	N23	J7
C24	N24	J8
C25	N25	J9
C26	-	-
C27	M1/C13	L3
C29	M16/C27	K120
C30	C28	K121
C31	C29	K122
C32	C30	K123
C33	M17/C27	K124
C34	C28	K125
C35	C29	K126
C36	C30	K127
C37	M18/C27	K128
C38	C28	K129
C39	C29	K130
C40	C30	K131
N 1	M20/C10	K108
N 2	C11	K109
N 3	C12	K110
N 4	C13	K111
N 5	M21/C10	K112
N 6	C11	K113
N 7	C12	K114
N 8	C13	K115
N 9	M22/C10	K116
N10	C11	K117
N11	C12	K118
N12	C13	K119
N29	M20/C27	K132
N30	C28	K133
N31	C29	K134
N32	C30	K135
N33	M21/C27	K136
N34	C28	K137
N35	C29	K138
N36	C30	K139
N37	M22/C27	-
N38	C28	-
N39	C29	-
N40	C30	-

C : Component side N : Non-component side

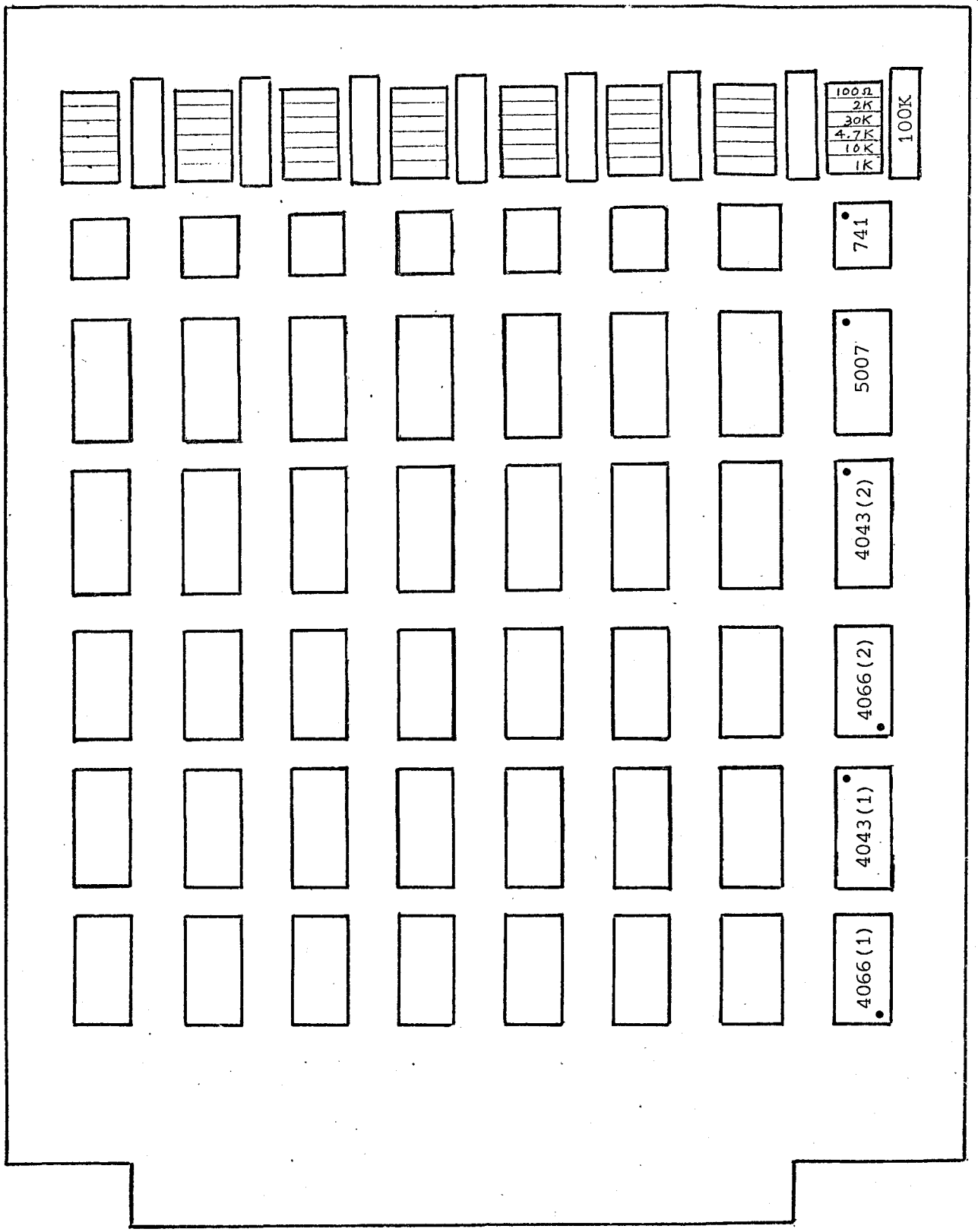


Fig. 20a Memory board, M2 to M22; 18 boards identical. (Component side).

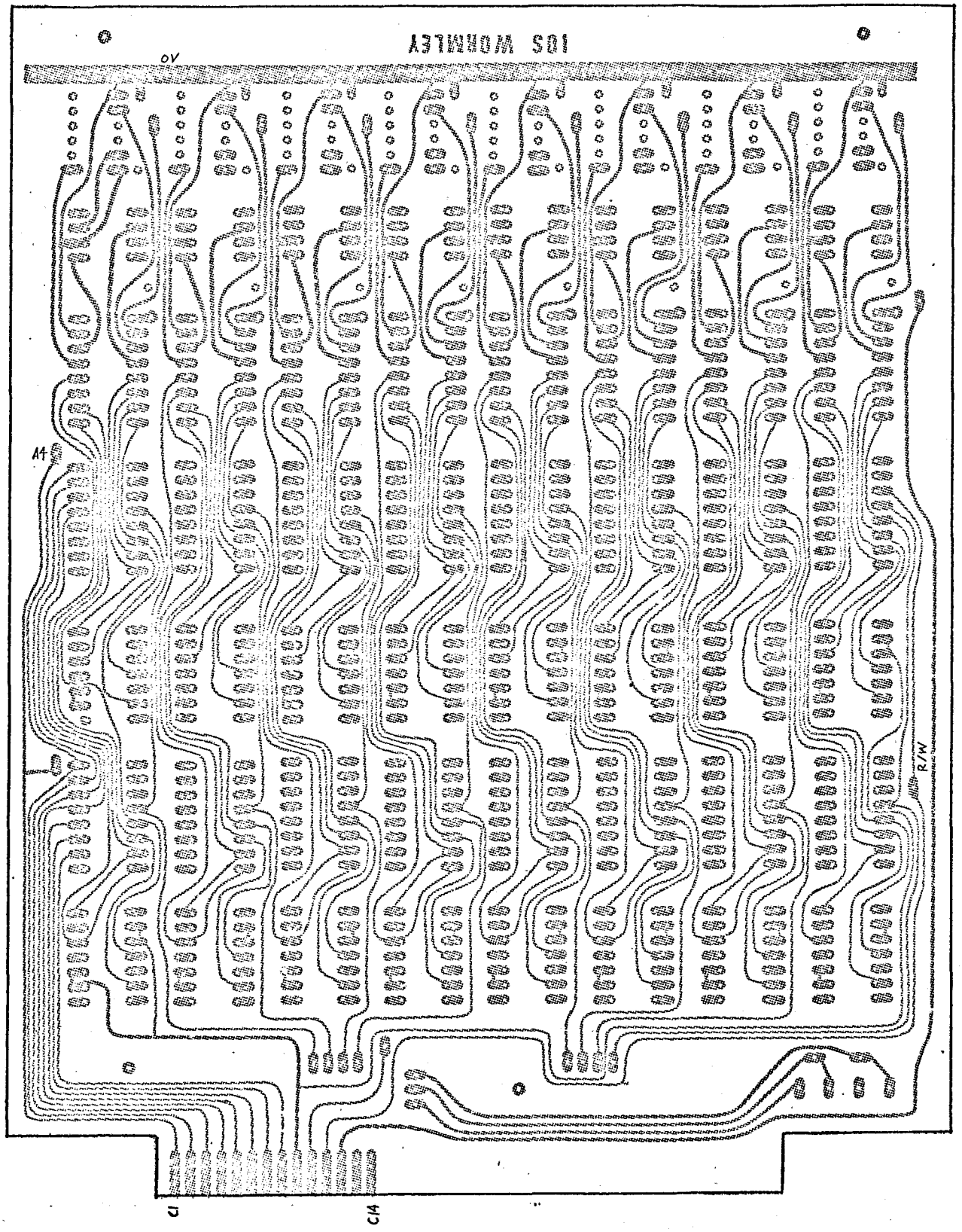


Fig. 20b Memory board, M2 to M22; 18 boards identical. (Conductors on the component side).

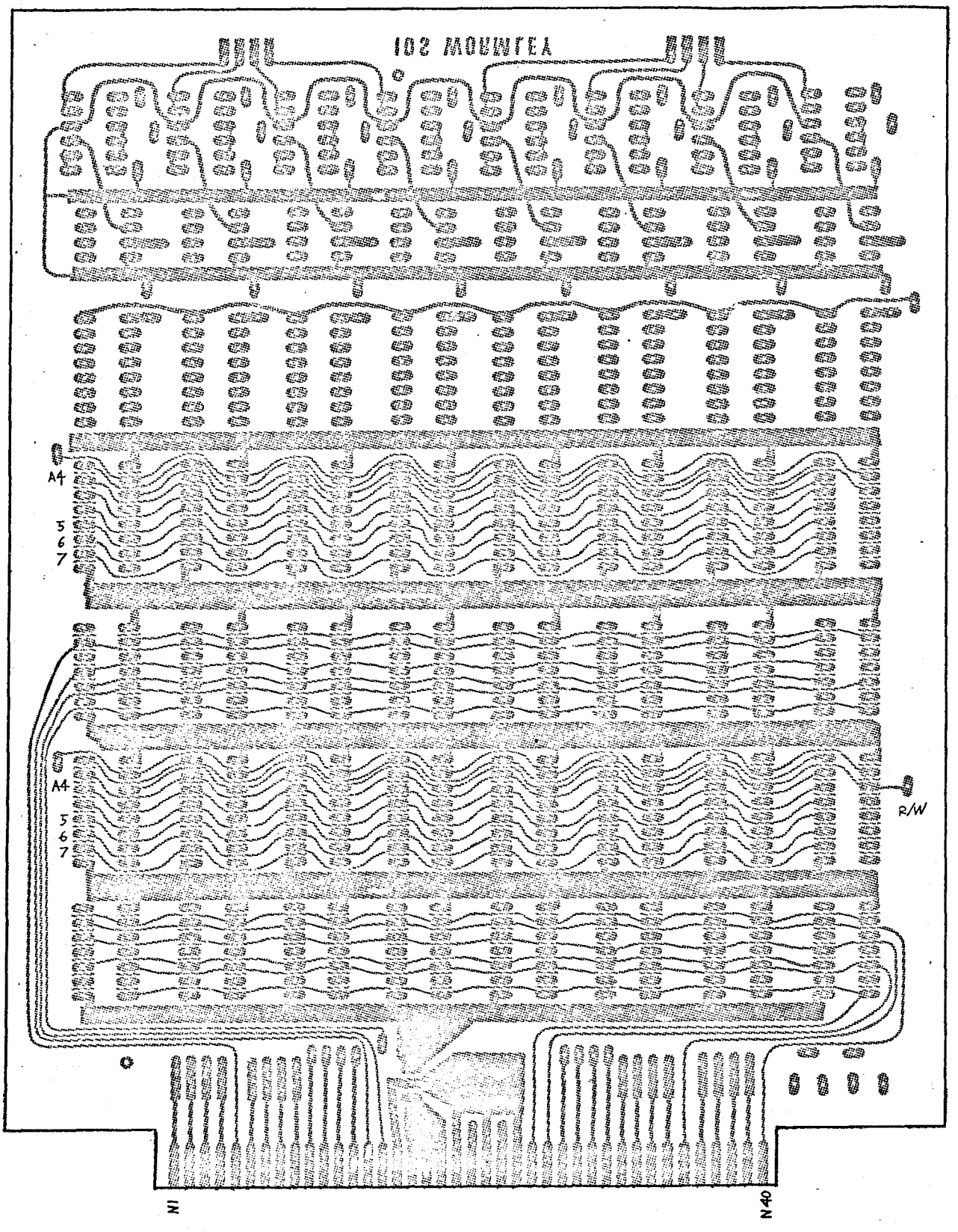


Fig. 20c Memory board, M2 to M22; 18 boards identical. (Non-component side).

Table 6 Connections of the 18 memory boards.

One of the 18 boards, pin No.	Connection	Function
N1 N2 N3 N4		Output
N5	D8 (LSB)	Data Bus
N6 N7 N8 N9		Output
N10 N11 N12 N13	K1 K2 K3 K4	Selector
N14 N15	D7 D5	Data Bus
N16	CN130/9	OV
N17 N18 N19	CN130/1	+5V
N20 N21 N22 N23 N24	CN130/9 CN130/17 CN130/9 CN130/20 CN130/9	OV -12V OV +12V OV
N25 N26	D4 D3	Data Bus
N27 N28 N29 N30	K5 K6 K7 K8	Selector
N31 N32 N33 N34		Output
N35	D1	Data Bus
N36 N37 N38 N39		Output
N40	D2	Data Bus
C1 C2 C3 C4 C5 C6 C7 C8	A4 A3 A2 A1 A0 A5 A6 A7	Address Bus
C9	M1/C28	SW
C10	D6	Data Bus
C11 C12	M1/C31 CN130/9	R/W OV VTH

The 18 board, M2, M3, M4, M6, M7, M8, M9, M10, M11, M13, M14, M15, M16, M17, M18, M20, M21 and M22 are identical.

A pin No. whose function only is shown in this table can be determined by other tables:-

Output ..... Table 8

Selector ..... Table 5

Data Bus ..... Table 4, 7

Address Bus ..... Table 4

Table 7 Connections of the rear panel.

CN103 (socket) From Tape-reader

CN103 pin No		Connetion
1	Bn	Tape out 1
2	R	2
3	Or	3
4	Y	4
5	Gn	5
6	Be	6
7	V	7
8	Gy	8
9	W	BD30/29 FH
10	R/Gn	BD30/23 TFW
11	R/Be	/25 TBW
12	Y/Be	/27 Clutch
13		Common
14	Bn	Data Bus 1
15	R	2
16	Or	3
17	Y	4
18	Gn	5
19	Be	6
20	V	7
21	Gy	8
22 23 24 25	Not used	

4 co-ax connectors

		Connection
SEQ R-CL	Or/Bk	M1/C20
SYNC OUT	Or/Be	M1/N38
RND CIK	R	M1/U2
PRINT OUT	Y/R	M1/C26

CN130 (socket) From Power supply

Pin No		Connection
1 to 8	Bk	+5V
9 to 16 18, 19	Gn	OV
17	Be	-12V
20	R	+12V

CN133 (socket) To Test unit

Pin No		Connection	
1	Y	M1/C20	R-CIK
2	Bk	CN133/1	+5V
3	Gn	/9	OV
4	Be	/17	-12V
5	R	/20	+12V

SEQ/RND switch

Switch pin No		Connection
1	Bn	M1/C17
2	R	(RP) RND Clock
3	Or	M1/C23
4	Y	M1/C29
5	Gn	M1/C26
6	Be	M1/C24
7, 10	Bk	CN130/1 +5V
8	V	M1/C25
9	Gy	M1/C19
11	Gn/Bk	CN130/9 OV
12	W	M1/C18

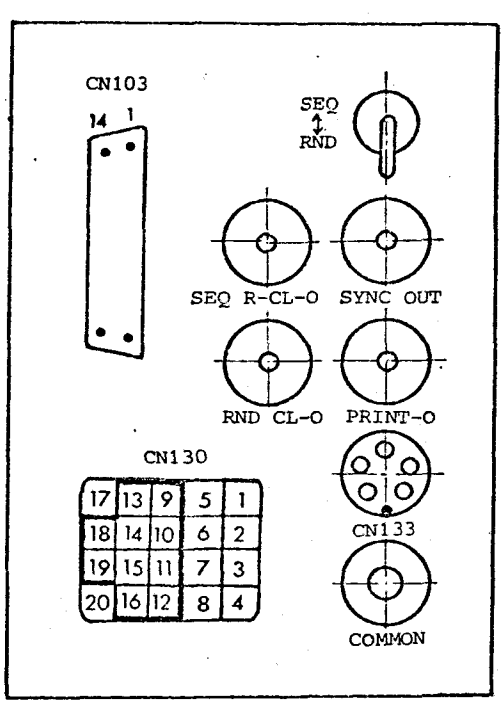


Fig. 21 Rear panel.

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	M1	← BOARD NO.
116	112	108		104	100	96	68	64	60		56	52	48	20	16	12		8	4	0		
117	113	109		105	101	97	69	65	61		57	53	49	21	17	13		9	5	1		
118	114	110		106	102	98	70	66	62		58	54	50	10	18	14		10	6	2		
119	115	111		107	103	99	71	67	63		59	55	51	11	19	15		11	7	3		← CHANNEL NO.
128	124	120		140	136	132	80	71	72		92	88	84	32	28	24		44	40	36		
129	125	121		141	137	133	81	77	73		93	89	85	33	29	25		45	41	37		
130	126	122		142	138	134	82	78	74		94	90	86	34	30	26		46	42	38		
131	127	123		143	139	135	83	79	75		95	91	87	35	31	27		47	43	39		

MONITOR GROUP NO. + PIN NO. = CHANNEL NO.

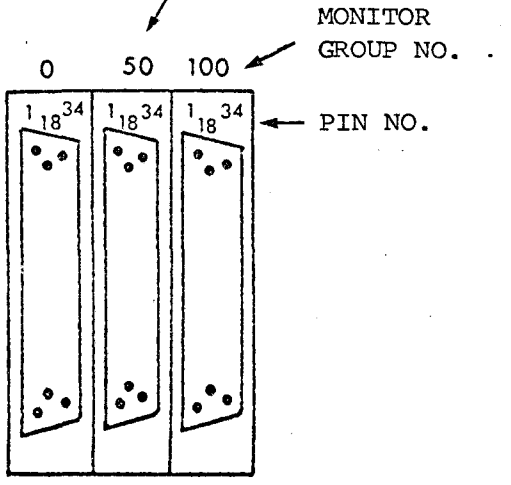


Fig. 22 Position of each channel, shown by the channel number, seen on the front of the memory cabinet without the cover (top); and the output monitor terminals (bottom).

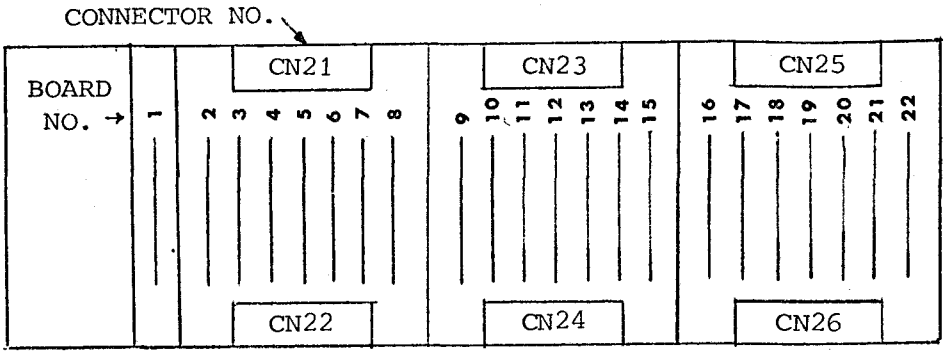


Fig. 23a Rear view of the memory cabinet showing the positions of all the boards and output connectors, CN21 to CN24.

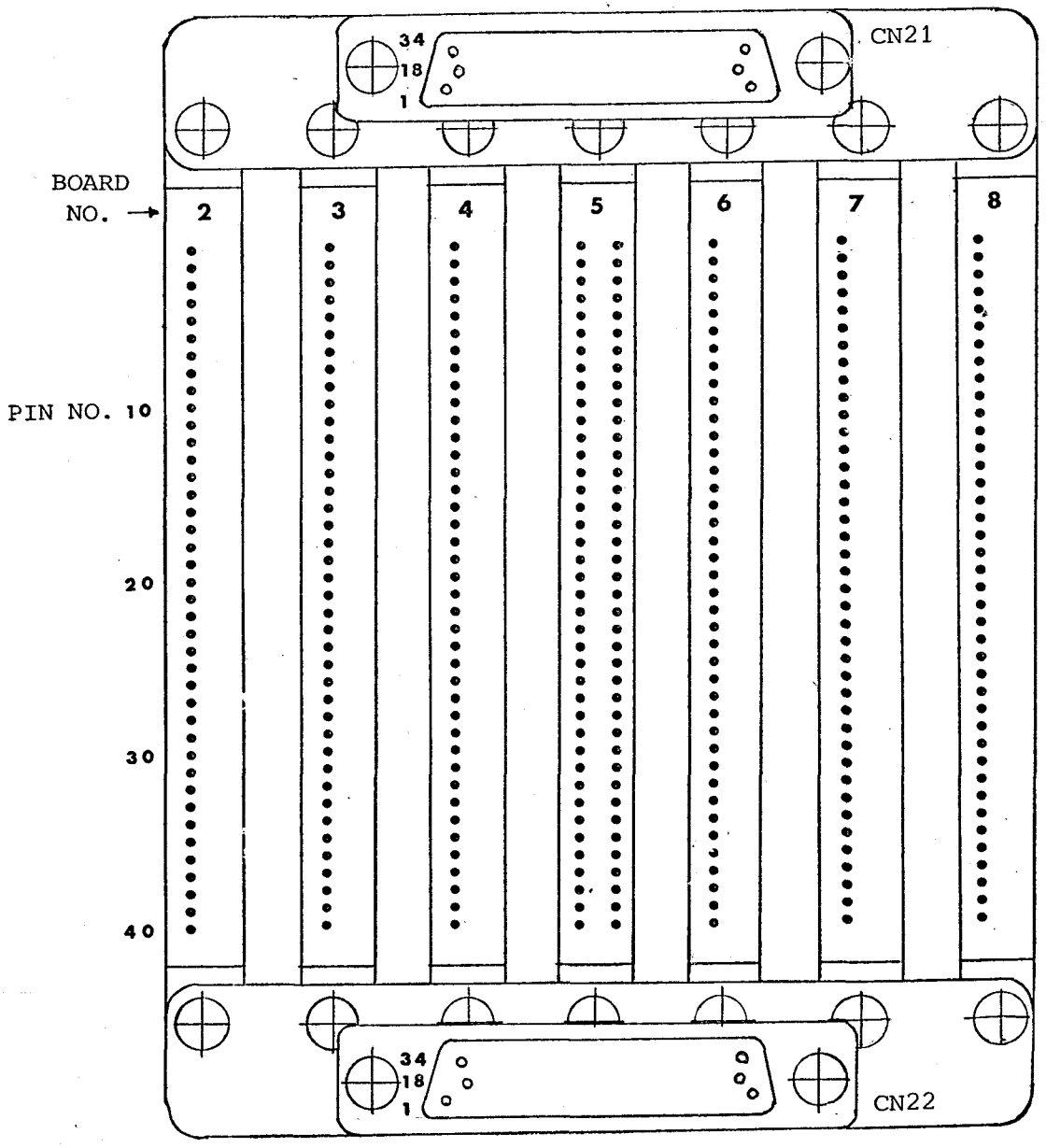


Fig. 23b Details of one third of Fig. 23a showing the pin numbers of connectors (full scale).

Table 8 Relationships between the memory channel numbers, board pins, output connections, and monitor pin numbers.

Memory channel	From board	To connector	Connector wire colour	Monitor pin No.
0	M2/C1-2	CN21/1-2	Bn-R	(100) 40
1	C3-4	3-4	Or-Y	(0) 1
2	C6-7	5-6	Gn-Be	2
3	C8-9	7-8	V-Gy	3
4	M3/C1-2	18-19	Bn-R	4
5	C3-4	20-21	Or-Y	5
6	C6-7	22-23	Gn-Be	6
7	C8-9	24-25	V-Gy	7
8	M4/C1-2	34-35	Bn-R	8
9	C3-4	36-37	Or-Y	9
10	C6-7	38-39	Gn-Be	10
11	C8-9	40-41	V-Gy	11
12	M6/C1-2	10-11	Bk-Bn	12
13	C3-4	12-13	R-Or	13
14	C6-7	14-15	Y-Gn	14
15	C8-9	16-17	Bn-R	15
16	M7/C1-2	26-27	W-Bk	16
17	C3-4	28-29	Bn-R	17
18	C6-7	30-31	Or-Y	18
19	C8-9	32-33	Gn-Or	19
20	M8/C1-2	43-44	Bk-Bn	20
21	C3-4	45-46	R-Or	21
22	C6-7	47-48	Y-Gn	22
23	C8-9	49-50	Y-Gn	23
24	M6/C31-32	CN22/10-11	Bk-Bn	24
25	C33-34	12-13	R-Or	25
26	C36-37	14-15	Y-Gn	26
27	C38-39	16-17	Bn-R	27
28	M7/C31-32	26-27	W-Bk	28
29	C33-34	28-29	Bn-R	29
30	C36-37	30-31	Or-Y	30
31	C38-39	32-33	Gn-Or	31
32	M8/C31-32	43-44	Bk-Bn	32
33	C33-34	45-46	R-Or	33
34	C36-37	47-48	Y-Gn	34
35	C38-39	49-50	Y-Gn	35
36	M2/C31-32	1-2	Bn-R	36
37	C33-34	3-4	Or-Y	37
38	C36-37	5-6	Gn-Be	38
39	C38-39	7-8	V-Gy	39
40	M3/C31-32	18-19	Bn-R	40
41	C33-34	20-21	Or-Y	41
42	C36-37	22-23	Gn-Be	42
43	C38-39	24-25	V-Gy	43
44	M4/C31-32	34-35	Bn-R	44
45	C33-34	36-37	Or-Y	45
46	C36-37	38-39	Gn-Be	46
47	C38-39	40-41	V-Gy	47

Memory channel No.	From board	To connector	Connector wire colour	Monitor pin No.
48	M9/C1-2	CN23/1-2	Bn-R	(0) 48
49	C3-4	3-4	Or-Y	49
50	C6-7	5-6	Gn-Be	50
51	C8-9	7-8	V-Gy	(50) 1
52	M10/C1-2	18-19	Bn-R	2
53	C3-4	20-21	Or-Y	3
54	C6-7	22-23	Gn-Be	4
55	C8-9	24-25	V-Gy	5
56	M11/C1-2	34-35	Bn-R	6
57	C3-4	36-37	Or-Y	7
58	C6-7	38-39	Gn-Be	8
59	C8-9	40-41	V-Gy	9
60	M13/C1-2	10-11	Bk-Bn	10
61	C3-4	12-13	R-Or	11
62	C6-7	14-15	Y-Gn	12
63	C8-9	16-17	Bn-R	13
64	M14/C1-2	26-27	W-Bk	14
65	C3-4	28-29	Bn-R	15
66	C6-7	30-31	Or-Y	16
67	C7-8	32-33	Gn-Or	17
68	M15/C1-2	43-44	Bk-Bn	18
69	C3-4	45-46	R-Or	19
70	C7-7	47-48	Y-Gn	20
71	C8-9	49-50	Y-Gn	21
72	M13/C31-32	CN24/10-11	Bk-Bn	22
73	C33-34	12-13	R-Or	23
74	C36-37	15-16	Y-Gn	24
75	C38-39	16-17	Bn-R	25
76	M14/C31-32	26-27	W-Bk	26
77	C33-34	28-29	Bn-R	27
78	C36-37	30-31	Or-Y	28
79	C38-39	32-33	Gn-Or	29
80	M15/C31-32	43-44	Bk-Bn	30
81	C33-34	45-46	R-Or	31
82	C36-37	47-48	Y-Gn	32
83	C38-39	49-50	Y-Gn	33
84	M9/C31-32	1-2	Bn-R	34
85	C33-34	3-4	Or-Y	35
86	C36-37	5-6	Gn-Be	36
87	C38-39	7-8	V-Gy	37
88	M10/C31-32	18-19	Bn-R	38
89	C33-34	20-21	Or-Y	39
90	C36-37	22-23	Gn-Be	40
91	C38-39	24-25	V-Gy	41
92	M11/C31-32	34-35	Bn-R	42
93	C33-34	36-37	Or-Y	43
94	C36-37	38-39	Gn-Be	44
95	C38-39	40-41	V-Gy	45

Memory channel No.	From board	To connector	Connector wire colour	Monitor pin No.
96	M16/C1-2	CN25/1-2	Bn-R	(50) 46
97	C3-4	3-4	Or-Y	47
98	C6-7	5-6	Gn-Be	48
99	C8-9	7-8	V-Gy	49
100	M17/C1-2	18-19	Bn-R	50
101	C3-4	20-21	Or-Y	(100) 1
102	C6-8	22-23	Gn-Be	2
103	C8-9	24-25	V-Gy	3
104	M18/C1-2	34-35	Bn-R	4
105	C3-4	36-37	Or-Y	5
106	C6-7	38-39	Gn-Be	6
107	C8-9	40-41	V-Gy	7
108	M20/C1-2	10-11	Bk-Bn	8
109	C3-4	12-13	R-Or	9
110	C6-7	14-15	Y-Gn	10
111	C8-9	16-17	Bn-R	11
112	M21/C1-2	26-27	W-Bk	12
113	C3-4	28-29	Bn-R	13
114	C6-7	30-31	Or-Y	14
115	C8-9	32-33	Gn-Or	15
116	M22/C1-2	43-44	Bk-Bn	16
117	C3-4	45-46	R-Or	17
118	C6-7	47-48	Y-Gn	18
119	C8-9	49-50	Y-Gn	19
120	M20/C31-32	CN26/10-11	Bk-Bn	20
121	C33-34	12-13	R-Or	21
122	C36-37	14-15	Y-Gn	22
123	C38-39	16-17	Bn-R	23
124	M21/C31-32	26-27	W-Bk	24
125	C33-34	28-29	Bn-R	25
126	C36-37	30-31	Or-Y	26
127	C38-39	32-33	Gn-Or	27
128	M22/C31-32	43-44	Bk-Bn	28
129	C33-34	45-46	R-Or	29
130	C36-37	47-48	Y-Gn	30
131	C49-50	49-50	Y-Gn	31
132	M16/C31-32	1-2	Bn-R	32
133	C33-34	3-4	Or-Y	33
134	C36-37	5-6	Gn-Be	34
135	C38-39	7-8	V-Gy	35
136	M17/C31-32	18-19	Bn-R	36
137	C33-34	20-21	Or-Y	37
138	C36-37	22-23	Gn-Be	38
139	C38-39	24-25	V-Gy	39
140	M18/C31-32	34-35	Bn-R	40
141	C33-34	36-37	Or-Y	41
142	C36-37	38-39	Gn-Be	42
143	C38-39	40-41	V-Gy	43

Bn: Brown R: Red Or: Orange Y: Yellow Gn: Green
Be: Blue V: Violet Gy: Grey W: White Bk: Black
M: Memory board C: Component-side of a board

This table should be read, for example, as:-
Memory channel No. 137 (a group of wires) comes from memory board M17, Pins 33 and 34; and goes to connector CN26, Pins 20 and 21. The colours of the wires are Orange and Yellow. This channel output can be monitored through Monitor Group 100, Pin 37.

6. TESTS AND ADJUSTMENTS

Since the input memory system has about 286K bits of memory cells, these have to be tested in an efficient way. A test method developed for this particular memory system is described in this chapter.

The tests are carried out in the following four stages:-

1. Test of each memory board;

2. Test of the whole system in sequential write mode 2;

3. Test of the whole system in sequential write mode 1; and

4. Test of the whole system in the random write/read mode.

For each stage of the test, a special test tape is required. Only when 1 is successful, can 2 be successful. Only when 2 is successful, can 3 be successful, and so on. It is recommended, therefore, that the tests be carried out in this order. For 1, a test unit has been designed. For 2, 3 and 4, no special equipment is required, other than a conventional CRO and printer (or tape-punch) which are parts of the model system.

If 1 is successful, but 2, 3 or 4 is not successful, this shows that a fault (or faults) lies in the control circuit (M1, M5, M12, M19) or wirings in the memory cabinet. A guide to finding possible faults can be found in 7.4.

6.1 Memory test unit

Fig. 24 shows the memory test unit by which each memory board (M2, M3, M4, M6, M7, M8, M9, M10, M11, M13, M14, M15, M16, M17, M18, M20, M21 or M22) can be tested separately. The test unit has a circuit based on the same principle as that used for the control circuit in the memory cabinet, but with a much simpler construction. The test unit can be operated independently from the memory cabinet, providing it is connected to the cabinet through connector CN133 (power supply and clock), and to the tape-reader through connector CN103 (data input and tape-reader control signals).

By using this test unit, with a test tape, all the 8 channels of memory on each board can be tested simultaneously. The output of each channel can be observed on a CRO, a normal state of operation being shown by a straight sloped line.

Fig. 25 shows the circuit diagram of the test unit. This consists of a tape-control circuit, write/read circuit, and address-code generator.

Tape-control circuit When a manual start switch is activated, a pulse (constant width) is generated by 121(3). This pulse holds the output of FF (00/1 to 6) low, and starts the motor of the tape-reader. When the tape-reader runs, a start code on the tape, '255', is detected by an 8-input NAND gate, 30. This pulse enters 93(3) through 121(2), but this is ignored by the former since 93(3) responds to every two input pulses. When the tape comes to the end, the end signal, also '255', is again generated by 30, and again enters 93(3). This time, 30 activates another pulse to raise the output of the FF, so that the tape stops.

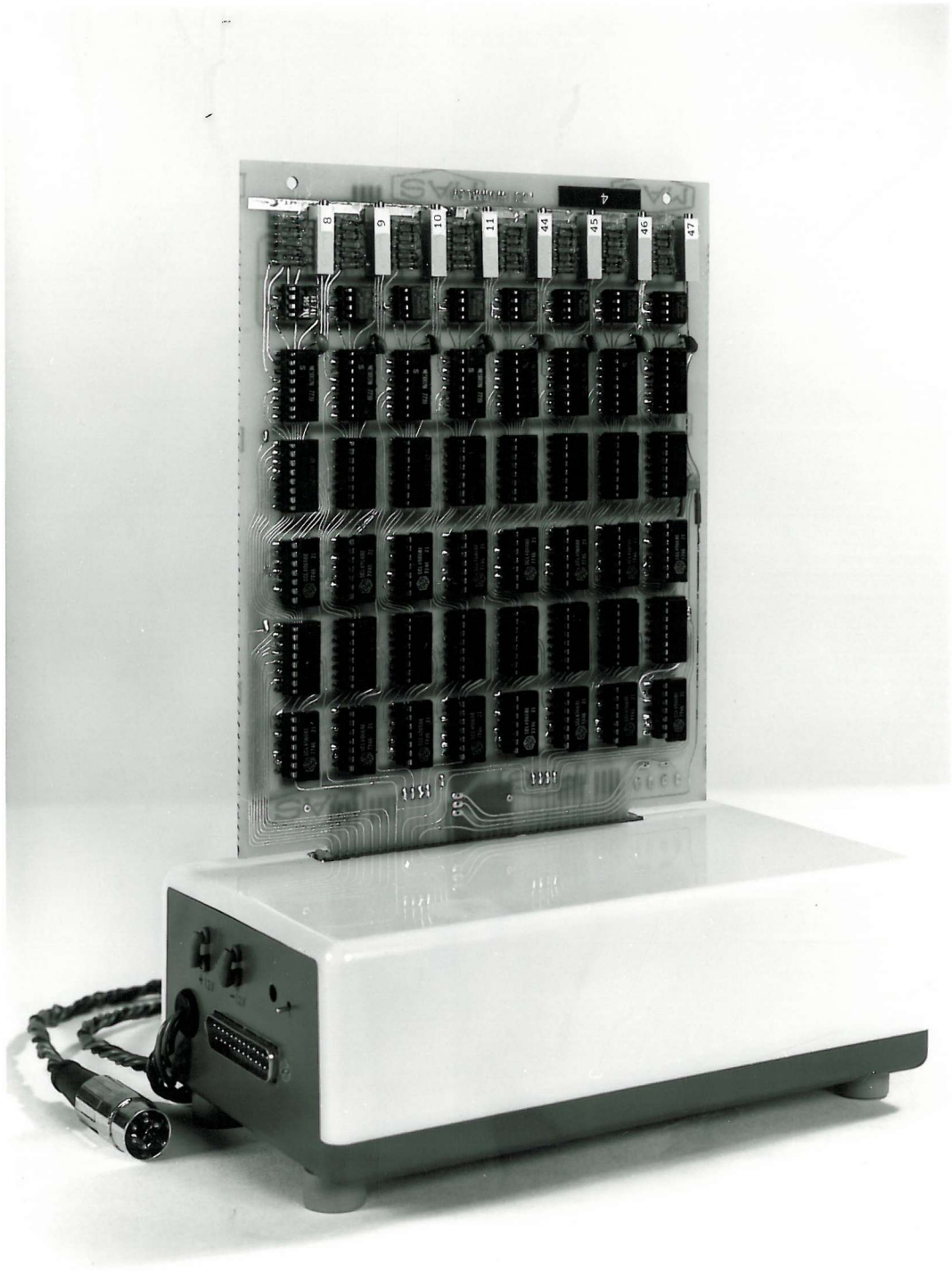


Fig. 24 Memory test unit with a memory board under test.

Write/read signal circuit The output of 93(3) is lowered only for a period between the above two '255' signals. This output voltage controls switch 51 by which a write clock or read clock is selected. Also an inverted output of 93(3) is fed into the board under test, and this controls the electronic switches on the board. The write or read clock passed through 51 is used, after shaping by 121(1), or read clock passed through 51 is used, after shaping by 121(1), for the address code generator. The same pulses are delayed by a delay circuit, 04/1 to 6, and these pulses are used for the CE (chip enable) signal.

Address-code generator This consists of two binary-code ICs, 93(1) and 93(2). The positive-going pulse output of 121(2) is used to reset the address-code generator, so that the start of the binary code is synchronized with the start of the tape codes.

Fig. 26 shows the circuit board of the test unit. Table 9 shows the connections within the test unit.

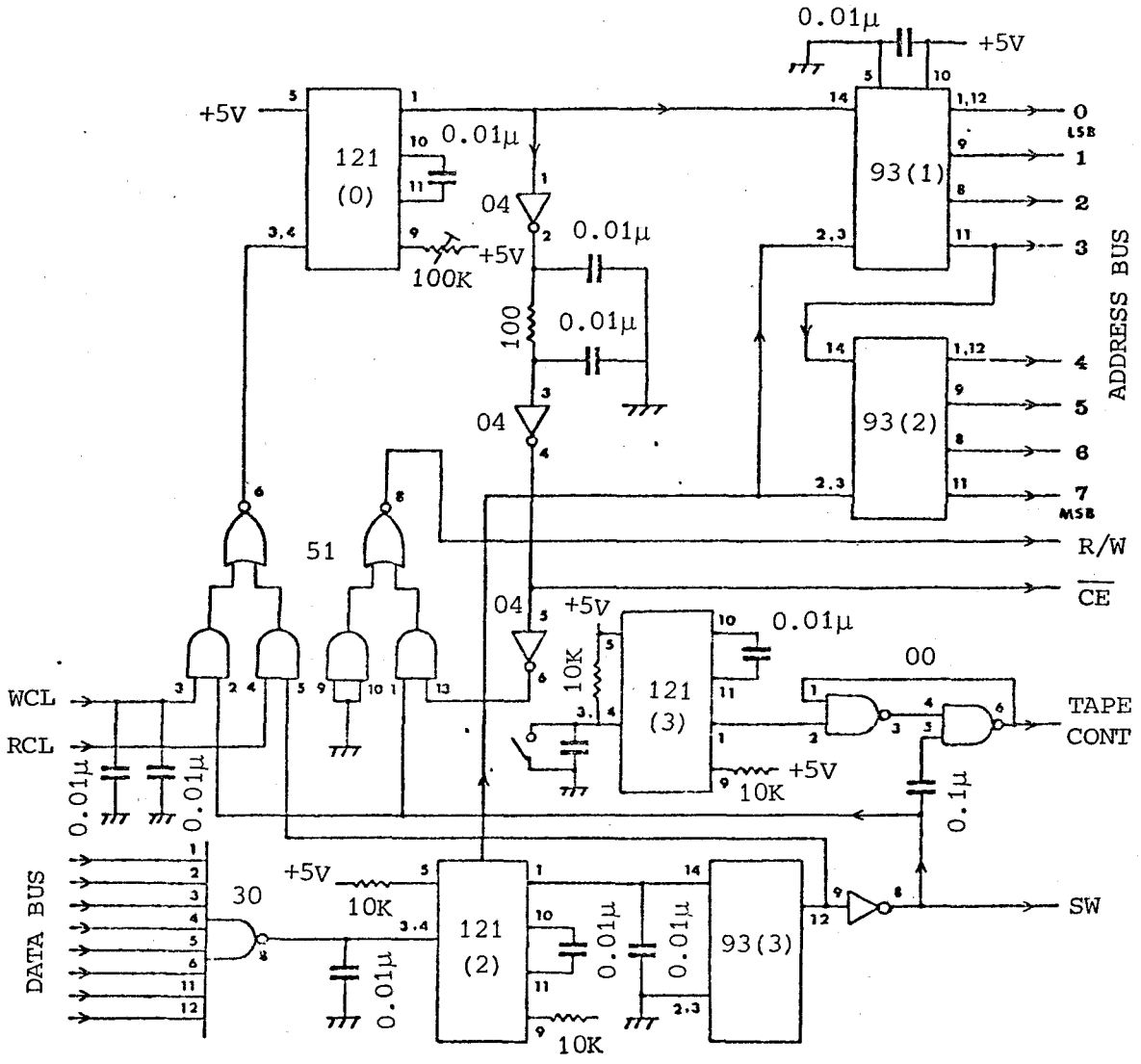


Fig. 25 Circuit diagram of the memory test unit.

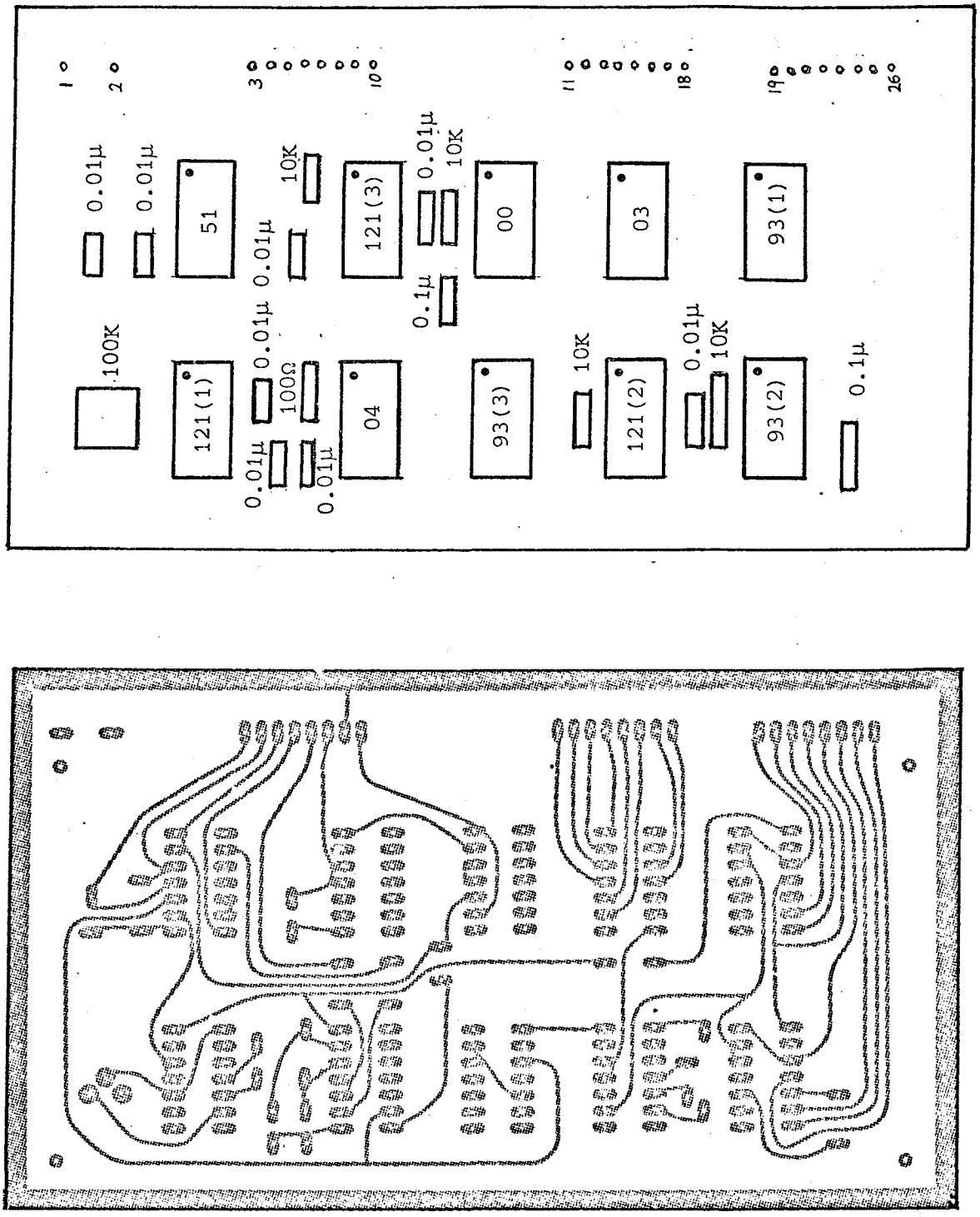


Fig. 26 Circuit board of the memory test unit.
Top: Component side. Bottom: Non-component side.

Table 9 Connections of the memory test unit.

Test-unit circuit board pin No.	Wire colour	Connection	Function
1	Gn	CN133/3	OV
2	Bk	CN133/2	+5V
3	W/Or	CN133/1	R-CLK
4	W	CN103/9	W-CLK
5	W	CNT/C9	SW
6	Bk	CNT/C11	R/W
7	W/Or	CNT/C10 C11 C12 C13 C27 C28 C29 C30	CE
8	V	Micro SW	
9	Gn	Micro SW	Start
10	Or/R	CN103/10 12	Tape-control
11	Gy	CN103/1 & CNT/N35	Data 1
12	V	2 N40	2
13	Be	3 N26	3
14	Gn	4 N25	4
15	Y	5 N27	5
16	Or	6 N28	6
17	R	7 N29	7
18	Bn	8 N30	8
19	R	CNT/C5	Addr. 0
20	Bn	C4	1
21	Or	C3	2
22	Y	C2	3
23	Gn	C1	4
24	Be	C6	5
25	V	C7	6
26	Gy	C8	7

Connector CNT pin No.	Wire colour	Connection	Function
N16 N17	Gn	CN133/3	OV
N18 N19	Bk	CN133/2	+10V
N20	Gn	CN133/3	OV
N21	R	CN133/5	+12V*
N22	Gn	CN133/3	OV
N23	Be	CN133/4	-12V*
N24	Gn	CN133/3	OV

*Through the current-mesuring terminals.

6.2 Test tapes

Five different test tapes are required for testing all the modes of the input memory system. Although 8-track punched tapes are used in these examples, other types of tapes can be used, providing they have the same formats as the examples and a suitable tape-reader is used.

The natural binary code is used for the actual test tapes. However, for simplicity, decimal figures are used to describe the formats of the tapes in this chapter. For example, binary '11111111' is represented by decimal '255'.

Test tape TEMB2

255	0, 1, 2, 3, ... 254	255
Start		End

Total 257 words

This tape is used for testing each memory board separately. The tape should be formed in an endless loop, with a space of about 100 words. This tape can be run in either direction.

Test tape TWM1

255	0, 254	1, 253	2, 252	....	254, 0	255
Start	72 times	72 times	72 times		72 times	End

Total 36722 words

This tape is used for testing the whole system in write mode 1. The margins are the same as above.

Test tape TWM2

255	0, 1, 2, 3, ... 254	255
Start	144 times	End

Total 36722 words

This tape is used for testing the whole memory system in sequential write mode 2. Appropriate margins should be added before the 'Start' and after the 'End'.

Test tape TRNDW

255	1, 1, 1, 0	1, 2, 2, 0	. . .	1, 254, 254, 0	
Start	2, 1, 1, 0	2, 2, 2, 0	. . .	2, 254, 254, 0	
	3, 1, 1, 0	3, 2, 2, 0	. . .	3, 254, 254, 0	
	.....	.....		.....	
	144, 1, 1, 0	144, 2, 2, 0	. . .	144, 254, 254, 0	255
	A_1 A_2 D -	A_1 A_2 D -		A_1 A_2 D -	End

Total 146882 words

This tape is used for testing the whole memory system in the random write mode. All the figures (words) from the 'Start' to 'End' should be punched continuously on a single tape. The figures in row A1 represent 'group-addresses' (from 1 to 144), and those in row A2 'addresses' in each set of memory packages (from 1 to 254). The figures in row D represent data (from 1 to 254). The row (-) represents spaces. The margins of the tape are the same as for TWM1.

Test tape TRNDR

The format of this tape is the same as test tape TRNDW, but all the figures in row D are zero. This tape is used for reading the whole memory which is written by test tape TRNDW.

6.3 Test of each memory board

This test is applicable only to each of the memory boards, M2, M3, M4, M7, M8, M9, M11, M13, M14, M15, M16, M17, M18, M20, M21 and M22. The test should be carried out by using the memory test unit (chapter 6.2) so that the rest of the system is not involved.

Before connecting a memory board to any active circuit, confirm the following resistances:-

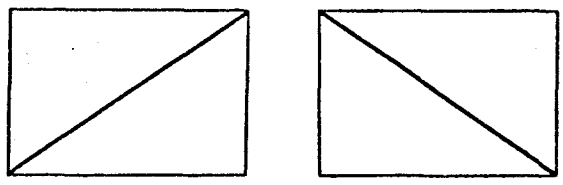
+5V supply line	approx.
-12V supply line	approx.
+12V supply line	approx.

where each value is referred to a resistance between each supply line on a memory board and its common line. Also each resistance value shown is for a case where a resistance-measuring current flows from the common line to each supply line. Note, the value is directional due to semiconductor circuits.

Test each memory board by using the memory test unit with test tape TEMB2. All 8 channels of each memory board will be written simultaneously. The output of each channel can be observed, through its 5007/4, using a CRO.

After the perfect operation of all the channels is confirmed by running test tape TEMB2 in a certain direction, reconfirm all the channels by running the tape in the other direction. In this way, all the bits of the memory can be examined. Note, bits in two series of natural binary code, 1 through 254, and 254 through 1, are reciprocal.

The correct waveform should be as shown in Fig. 27a or Fig. 27b, depending on the direction of running the test tape. If only a few particular values in a particular channel deviate from the straight slope line of a waveform, as shown in Fig. , this suggests a faulty memory IC. In this case, the replacement of the IC is the only solution. See Appendix 4 and 'Abnormal waveforms' in chapter 6.4, for other types of fault.



a b

Fig. 27 Normal waveforms

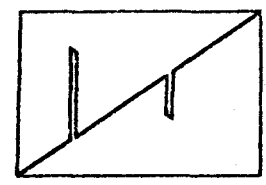


Fig. 28 Waveform suggesting a faulty memory.

6.4 Test of the system through the analogue waveforms

After the performance of each memory board has been confirmed by the previous test (6.3), a performance of the whole system (which is totally digital) in all the sequential modes can be confirmed rapidly by observing the analogue waveforms on a CRO from a DAC which is built in each channel of the memory. Each waveform is available from two different terminals:-

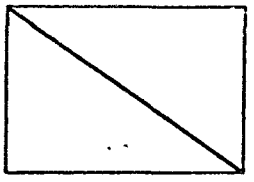
A Pin 4 of each DAC (5007) with the maximum voltage of 0.4V, and

B Monitor terminal on the front panel with the maximum voltage of 0.04V in a reverse polarity to A.

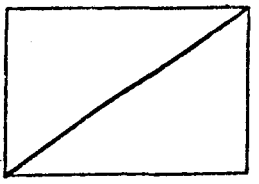
Note, B is available only when the outputs of the channels (CN21 to CN26 in the rear of the memory cabinet) are connected to their loads (LEDs in the main computation circuit, or external resistors of zero to about 1K ohms).

Normal waveforms

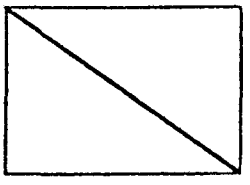
Fig. 29 shows normal waveforms at A when the two test tapes are used. Note, if a test tape is run in a reverse direction, the slope in each figure will be reversed. However, it is not necessary to test the memory by running the test tapes in two directions, if the memory has already been tested by test tape TEMB2 in two directions.



Channels 0, 2, 4 ... 254
with test tape TWM1



Channels 1, 3, 5 ... 253
with test tape TWM1

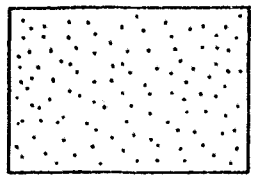


Any channel with
test tape TWM2

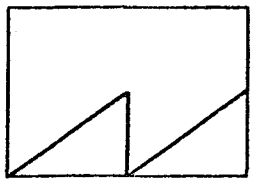
Fig. 29 Normal waveforms of ADC outputs with test tapes.

Abnormal waveforms

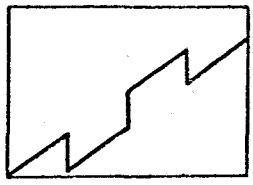
If the waveforms of the outputs of the system are not as shown in Fig. 29, there is a fault (or faults) in the system. Fig. 30 shows some examples of abnormal waveforms, with suggestions of possible faulty operations.



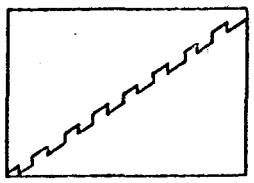
(1) No input data enters into the memory, although the read operation is normally carried out. Note, when the memory system is switched on for the first time, without input data, this waveform will be seen. There is no fault in this case.



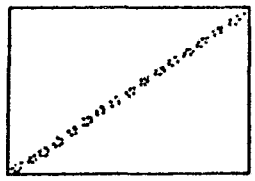
(2) The MSB line in a channel is cut off.



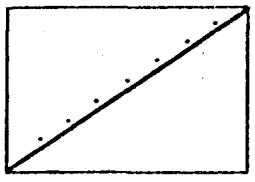
(3) The 2nd-SB line in a channel is cut off.



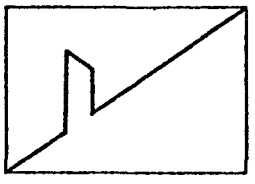
(4) The 6th-SB line in a channel is cut off. Note, a fault in a line other than these examples can easily be determined.



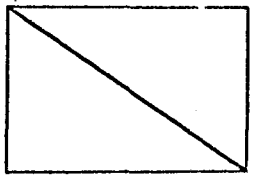
(5) Two lines which carry different-bit signals are crossed, e.g. the 7th-bit line and the 8th-bit line.



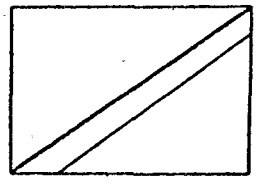
(6) This possible fault can occur only in write mode 1. Noise appears only one side of the slope. This suggests that the address-code generator is disturbed by a regular noise. The noise possibly enters from the driving terminal or reset terminals of the generator, due to a faulty noise filter.



(7) This is a similar case to the above, but caused by very occasional irregular noise, due again to a faulty filter.



(8) In write mode 1, if the slope is reversed (compared with the expected slope) and some random noise is observed at the same time, terminals of an IC on board M5, M12 or M19 are possibly opened. The noise and signal from the adjacent channel which has a reversed slope are picked up.



(9) A thin image of a slope appearing beside the proper slope suggests that the switch-control terminals of 4016 (high input impedance) are opened, and switching is carried out by an improper signal.

Fig. 30 Abnormal waveforms.

6.5 Test of digital circuits in sequential modes

If the test described in chapter 6.4 is satisfactory, this proves the perfect performance of all the digital circuits in the system, except for a few circuits which are solely used for the random read/write mode. In this case, no further test is required for the digital circuits for sequential modes.

If the test of each memory board (chapter 4.3) is satisfactory, but the test of the whole system (chapter 4.4) is not satisfactory, then a fault (or faults) is suspected in the digital circuits of the system. See 'Abnormal waveforms' in chapter 4.4 and 'Guide to fault finding' in Appendix 4, for determining the type of fault and the location of the faulty circuit. Then compare the observed waveform against the correct waveforms shown in Tables 10 through 14.

Table 10 Waveforms in the tape-control circuit and CSW-signal generator in control circuit board M1.

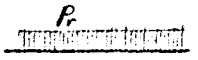
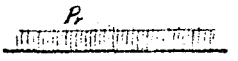
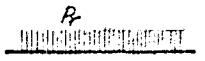
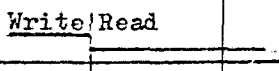
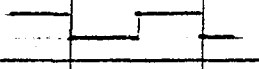
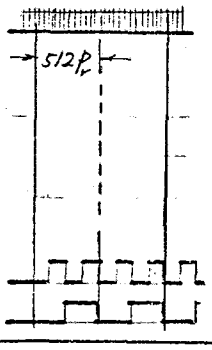
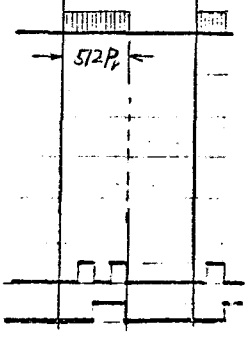
Function	Board pin No	IC pin No	Waveforms
Manual START			Arbitary
		121(3)/5 00/1	
		121(3)/6	
		00/6	
START code on tape		30/8	Tape margin before 'START' code
		121(2)/1 93(5)/14	
Reset signal RST		121(2)/6	
CSW	C28	93(5)/12	
		00/11	
$\overline{\text{CSW}}$		04(1)/8	
Write clock	C22	157(5)/2	
Read clock	C20	157(5)/3	
L1 L2 L3	C15 C14 C13	04(1)/6 /10 /12	
P	C21	32/6	

Table 11 Waveforms in control circuit board M1 in sequential write and read modes.

Function	Board Pin No	IC pin No	Write mode 1	Write mode 2	Read mode 0
Write clock		14/6 157(5)/2			X
Pulse-width control		121(1)/6 08/10 157(5)/11 157(5)/9	P_w t_{pw}	P_w t_{pw}	X
		93(1)/14 93(3)/14			P_r t_{pw}
A	N29	93(1)/1	157(1)/4		
B	N27	9	7		
C	N18	8	9		
D	N19	11	10		
		93(2)/1	157(2)/4		
		9	7		
		8	9		
		11	12		
		93(3)/1	157(3)/4		
		9	7		
		8	9		
		10	12		
		93(4) 1 / 9 / 8 / 11	157(4) 4 / 7 / 9 / 12	42 15 / 14 / 13 / 12	
			$280P_w$ $280^8 P_w$	$2P_w$ $2^{16} P_w$	$2P_r$ $512P_r$
			$2P_w$		$2P_r$ $512P_r$
J1	N17	42/1			
2	N18	2			
3	N19	3			
4	N20	4			
5	N21	5			
6	N22	6			
7	N23	7			
8	N24	8			
9	N25	9	$36P_w$	$512P_w$	X
L1 L2 L3	C15 C14 C13	04(1)/6 10 13	L Always	L Always	$2P_r$
P	C21	32/6	$2P_w$	$2P_w$	H Always

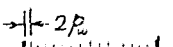
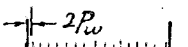
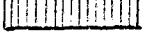
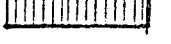
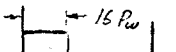
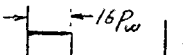
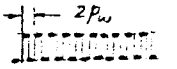
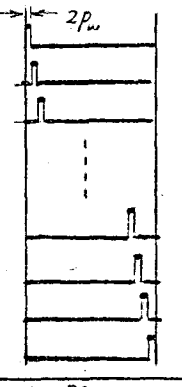
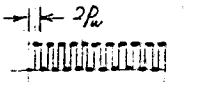
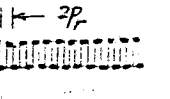
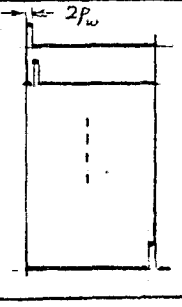
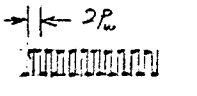
P_w : Write-clock period. P_r : Read-clock period. X : Irrelevant.
t_{pw} : Controlled pulse width.

Table 12 Waveforms in control circuit board M1 in sequential read modes 0 and 1.

Function	Board Pin No	IC pin No		Read mode 0	Read mode 1
Read clock	C20	157(5)/3			
Controlled pulse of clock		121(1)/6 157(5)/10 93(3)/14			
SYNC out	N39	93(4)/11		X	
CSW		93(8)/2,3		X	Write/Read 
		93(8)/12		X	
		14/11		L Always	
		93(1)/2,3 93(2)/2,3		L Always	
Address code	N38	93(1) 1	157(1) 4		
	N36	9	7		
	N34	8	9		
	N35	11	11		
	N31	93(2) 1	157(2) 4		
	N30	9	7		
	N37	8	9		
	N32	11	11		

P_r : Read-clock period. X : Irrelevant.

Table 13 Waveforms in sub-control circuit board M5 in sequential write and read modes. (M12 and M19 are identical to M5).

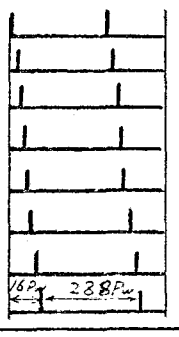
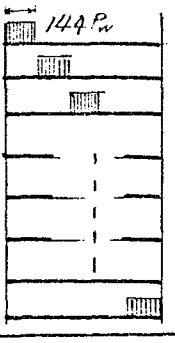
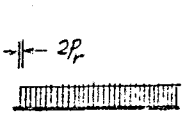
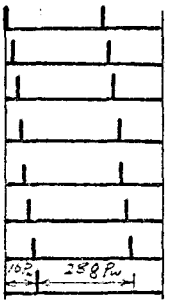
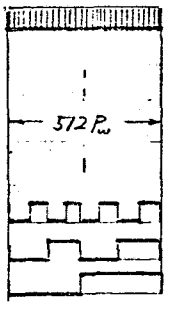
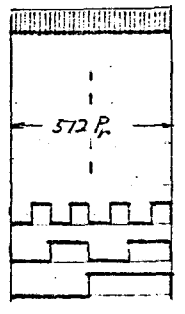
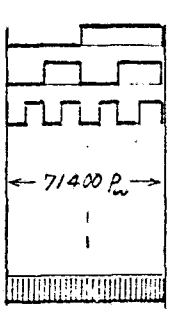
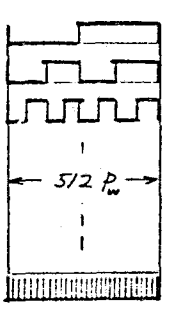
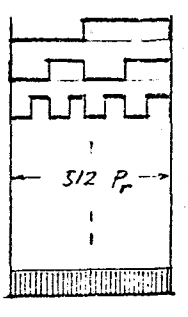
Function	Board Pin No	IC pin No	Write mode 1	Write mode 2	Read mode 0
A	N16	154(1)/23 154(2)/23 154(3)/23			X
B	N17	154(1)/22 154(2)/22 154(3)/22			X
C	N18	154(1)/21 154(2)/21 154(3)/21			X
D	N19	154(1)/20 154(2)/20 154(3)/20			X
P	N22	154(1)/18 154(2)/18 154(3)/18			H Always
* J1	N23	154(1)/19			X
J2	N24	154(2)/19			
J3	N25	154(3)/19			
L1	N27	04/1,3,5 9,11,13		H Always	
* K1	N1	08(1)/6			
K2	N2	3			
K3	N3	8			
K45	C37	08(12)/6		All the channels	All the channels
K46	C38	3			
K47	C39	8			
K48	C40	11			
Lines within the board		154(1)/1 2 154(2)/1 154(3)/1 17		 All the channels	H Always

P_w : Write-clock period. P_r : Read-clock period. X : Irrelevant.

* For board M12: J4 to J6; K48 to K95 should be applied.
For board M19: J7 to J9; K95 to K139 should be applied.

** All the waveforms are independent of test tapes.

Table 14 Waveforms in each memory board in sequential write/read modes.

Function	Board Pin No	IC pin No		Write mode 1 Tape TWM1	Write mode 2 Tape TWM2	Read mode 0
R/W	C11	9112(1)/14 & 9112(2)/14 in 8 channels				H Always
CSW	C9	4016/5,6,12,13; 4016/5,6,12,13 in 8 channels		H Always	H Always	L Always
K0	N10	9112(1)/13 9112(2)/13 in each of these channels	Ch 1			 In all the channels
K1	N11		2			
K2	N12		3			
K3	N13		4			
K4	N24		5			
K5	N28		6			
K6	N29		7			
K7	N30		8			
Data bus 1	N35	4016(2)/1	in all the 8 channels	As in tape TWM1	As in tape TWM2	X
Data bus 2	N40	9				
Data bus 3	N26	4				
Data bus 4	N25	3				
Data bus 5	N15	4016(1)/3				
Data bus 6	C10	1				
Data bus 7	N14	9				
Data bus 8	N5	11				
Address bus 0	C5	9112(1) 4	9112(2) 4			
Address bus 1	C4	3	3			
Address bus 2	C3	2	2			
Address bus 3	C2	1	1			
Address bus 4	C1	15	15			
Address bus 5	C6	5	5			
Address bus 6	C7	6	6			
Address bus 7	C8	7	7			
Lines within board 1	Not connected	4016(2) 10	9112(2) 9	5007 5	In each channel			
Lines within board 2		8	10	6				
Lines within board 3		4	11	7				
Lines within board 4		2	12	8				
Lines within board 5		4016(1) 4	9112(1) 12	9				
Lines within board 6		2	11	10				
Lines within board 7		10	10	11				
Lines within board 8		8	9	12				

P_w : Write-clock period. P_r : Read-clock period. X : Irrelevant.

18 boards, M2, M3, ... M22 are identical.

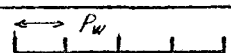
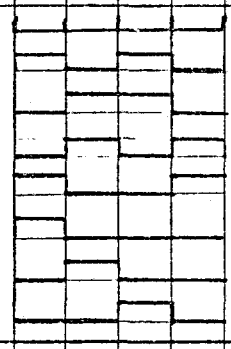
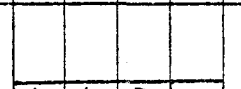
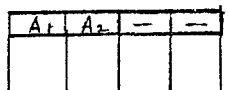
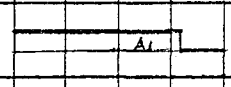
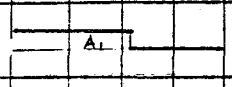
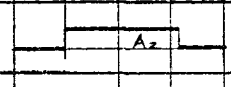
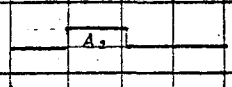
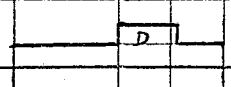
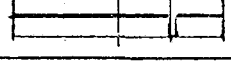
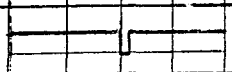
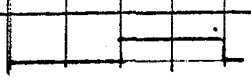
6.6 Test of the random write/read mode

Keeping all the circuit boards in a normal operating state in the memory cabinet, apply test tape TRNDW for writing the test data. Then apply test tape TRNDR for reading it. The output should be printed in a digital form. The correct output should be as follows:-

1, 2, 3, 4 ..... 254 (repeated in 144 sets)

If the output does not agree with this, a fault (or faults) will be in the circuits which are solely used for the random mode. Compare the observed waveforms in the circuits against the correct waveforms shown in Table 15.

Table 15 Waveforms in control circuit board M1 in the random write/read mode.

Function	Board Pin No	IC pin No	Write	Read
Write clock		14/5		
Input		93(7)/1		The same as in 'write', but period = P_r
A		93(7)/12		
B		93(7)/12		
Sampling code $\overline{A}$		04(2)/12		
$\overline{B}$		04(2)/6		
F1		08/6		
F2		08/10		
F3		08/11		
Input data from tape	N1 to N8	75(1)/3,6,7,2 75(2)/ " 75(3)/ " 75(4)/ " 75(5)/ " 75(6)/ "		
Sampling		75(1)/15,10,9,16 75(2)/ "		
		75(3)/15,10,9,16 75(4)/ "		
		75(5)/15,10,9,16 75(6)/ "		
Delayed & shaped F3	C26	121(4)/1		
RND read clock		157(5)/3	X	
Output data	N9 to N16	Data bus	X	

P_w : Write-clock period. P_r : Read-clock period. X : Irrelevant.

Waveforms for other parts of the circuit are not shown, since they dependon addresses given in a random mode.

The movement of the tape in a random read mode depends on a related external system.

6.7 Adjustments

The digital circuits in the input memory system do not require any adjustment, if they work properly. The analogue parts of the system require three types of adjustments only when the system is built for the first time or overhauled.

(1) Power supply voltages

The three power supply voltages should be adjusted to

+12.0V ± 1%

-12.0V ± 1%

+5.0V ± 2%

(2) Pulse width of the reading clock

Apply test tape TWM2, and observe the output waveforms of any memory channel through the monitor terminal (on the front panel of the memory cabinet) by a CRO. Generally two lines will be seen on the CRO, one being sloped, and the other one a horizontal line. Adjust the potentiometer, PULSE WIDTH (on the front panel), so that the horizontal line on the CRO cannot be seen, or very thin compared with the sloped line.

Note, the above two lines are part of a single voltage, as shown in Fig. 31, which is a train of pulses. The pulse width, t_{pw}, depends on the read-clock rate. Since the same pulse-width control circuit is used for the write clock, its pulse width is also controlled at the same time. However, this does not affect the performance of the system.

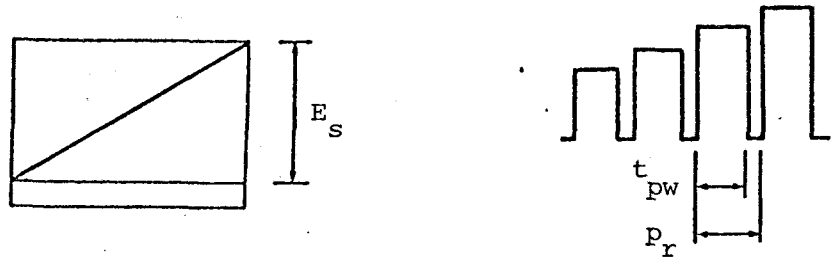


Fig. 31 Output waveform seen on a CRO (left) and its details (right).

(3) Full scale of each DAC

Each memory channel has a DAC by which a digital signal is finally converted into analogue current. This conversion scale should be adjusted individually.

Apply test tape TWM2, and observe the output waveform through the monitor terminal with a CRO whose sensitivity is calibrated to ±0.05%. Adjust a potentiometer in each channel (on the edge of each memory board) so that

$$E_s = 0.400V \pm 1\%$$

where E_s is the voltage corresponding to the height of the slope shown in Fig. 31.

Table 16 is a summary of the performance of the input memory system. Fig. 32 shows the constant-current characteristic of the analogue output of one of the memory channels. Fig. 33 shows an example of the output current of a memory channel which was derived from a digital input in write mode 2.

Table 16 Summary of performance of the input memory system

Input		Form of data	Sequential write mode 1: $F_1(t)_{x,y}$ Sequential write mode 2: $F_2(x,y)_t$ Random write/read mode, with addresses
		Data code	8-bit natural binary code, one word per data, from 0* to 254*
		Address code	8-bit natural binary code 000*-001* to 000*-254* 001*-001* to 001*-245* ... ... 143*-001* to 143*-254* (35560 addresses in all)
		Start/end codes	255*
		Channel	Single parallel 8-bit TTL
		Write speed	Arbitrary up to 100K words/s Typical sequential mode, 500 words/s
		Type	N-channel MOS large-scale ICs
Memory		Capacity	8 bits × 256 increments × 144 channels 294,912 bits in all
		Max store period	As long as the power supply is maintained
Output	Sequential	Form of data	Sequential mode 0: $F(t)_{x,y}$ repeat continuously Sequential mode 1: $F(x,y)_t$ repeat with intervals Simultaneous outputs in 144 channels
		Type	Analogue currents, signal (±2 mA) max) with a DC bias (8 mA) in each channel which can drive up to 5 optoelectronic couplers
		Read speed	Arbitrary up to 100K words/s (equivalent) Typically 1K words/s (equivalent)
	Random	Terminals	Floating current output, independent of external load up to 500Ω
		Read speed	Arbitrary up to 100K words/s
		Data code	8-bit words
		Terminal	Single channel 8-bit data bus, TTL logic
		Sync signal	TTL logic, between an external apparatus
Control		Programmed	Write start, Write end, and Read start
		Manual	Selection: Sequential or Random Write mode 1 or 2 Read mode 0 or 1 Read clock rates Adjustment: Read-clock pulse width Full scale of each analogue output

Accuracy	Resolution	0.4% of the full scale	
	Linearity	Better than 0.4%	
	Frequency range of analogue output	This is limited by the IC in each output; DC to 10 kHz (-3 dB) with 747C. The ADC in each channel, DC to 1.8 MHz.	
	Stability	FS temp. coeffic. of the DAC, 10 ppm/^{o}C Power-supply sensitivity of the DAC, $^{+0.0003}_{-0.002}$ % FS/%VS	
Temperature range	Operation	0 to +50^{o}C	Limited by the power supply units
	Storage	-55 to +85^{o}C	
Power requirement		240V, 50 Hz, 0.65A rms (156W)	
Protection		Voltage monitor for the +5V line High-voltage shut down (100 ns) 240V AC-line shut down (50 ms) Audible alarm Protection for each power unit	
Dimensions & Weight	Memory cabinet	50 × 35 × 22 (H) cm^3, 12.5 Kgr	
	Power cabinet	50 × 35 × 22 (H) cm^3, 14.0 Kgr	

*Natural binary code is represented by a decimal number for convenience.

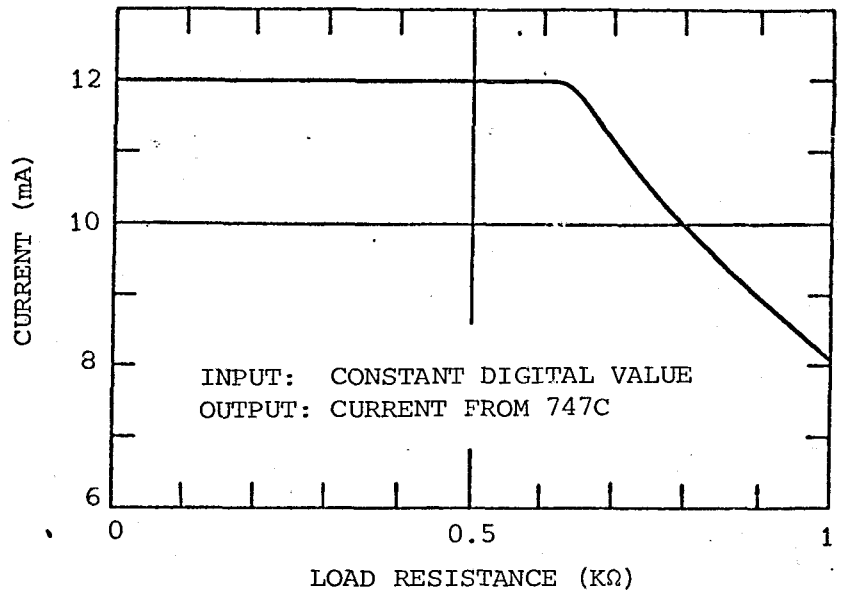


Fig. 32 Constant-current characteristic of the analogue output of a memory channel.

This characteristic shows that the output current is independent of its load up to about 0.6 KΩ which is equivalent to about 5 optoelectronic couplers.

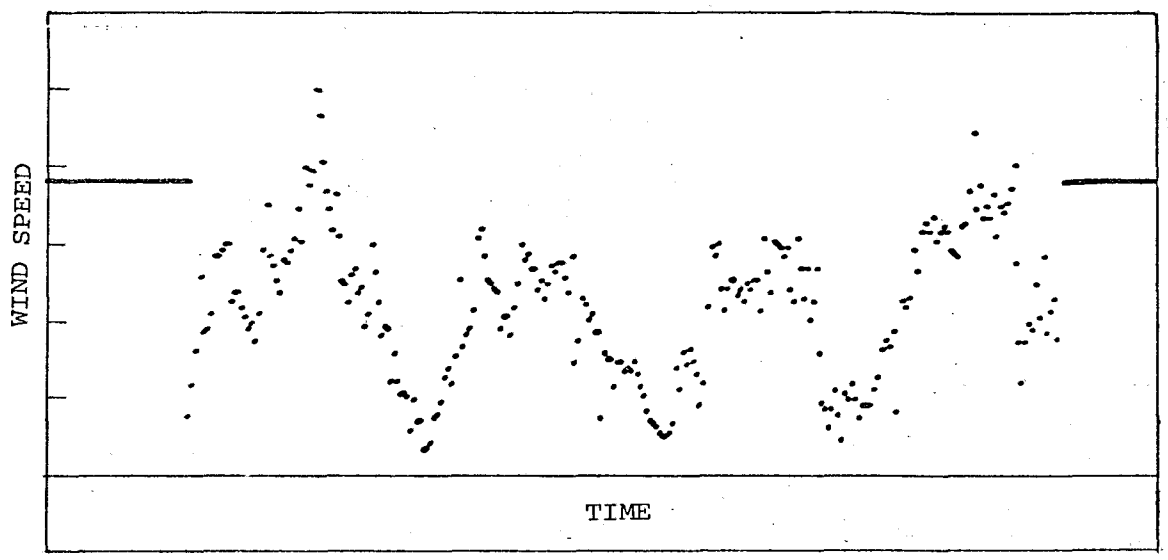


Fig. 33 Example of the wind variation with time, reproduced by the input memory system.
Input: Digital data of hourly-mean wind speed for 10 days.
Output: Analogue current through an optoelectronic coupler driven by one of the channels of the system.
Intervals = 100μS.

8. CONCLUSIONS

A new electronic memory system has been developed by which the electronic model for tides and storm surges can more efficiently be operated with a higher accuracy and longer successive period than the previous memory. The new system can also be used as a general purpose random access memory for handling data relating to the project.

ACKNOWLEDGEMENTS

This work is a part of the project commissioned by the Department of Industry and the Department of Energy. The author is grateful to Miss K. Reeves-Wilkin for her help with constructing and testing the memory system, and drawing diagrams in this paper.

REFERENCES

(1) Ishiguro, S. (1973) New Electronic Sea Model, IOS Internal Document, pp. 88.

(2) Ishiguro, S. (1977) Input Memory, IOS Internal Document, pp. 53.

Appendix 1 FORMATS OF INPUT TAPES

The input system has a set of input-data terminals into which any type of input signal can be fed, providing its format satisfies the specifications of the terminals. For simplicity, however, examples given in this appendix are only for punched tapes with a tape reader.

Sequential modes

An input-data tape for a sequential mode should have the following format:-

(1) The tape should have 8 tracks;

(2) A word (or a single value) in the input data should be represented by an 8-bit natural binary code, from 0 to 254 in decimal equivalent;

(3) '1' in the binary code should be represented in such a way that this produces a logic high signal at the input terminals of the system, and '0' in the reversed state;

(4) Both the start code and end code are represented by binary '1111 1111' (254 in decimal equivalent). The start code should be put on the tape immediately before the first word of the input data, and the end code immediately after the last word of the input data;

(5) All the 144 channels of the memory are read simultaneously with a synchronized timing. The order of reading words within each channel depends on the order in which they are written. There are two write modes:-

Write mode 1

Fig. A1 shows the relationship of the write words and read words. The input data should be written from the top-left to bottom-right continuously. Then the reading will be carried out from the top to bottom within each channel and all the channels simultaneously. The words in the 1st column of Fig. A1 (indicated by 1 to 254) will come out in this order from the output terminal of the 1st channel, the 2nd column from the 2nd channel, and so on.

Write mode 2

(6) Fig. A2 is similar to Fig. A1, but for write mode 2. The input data should be written again from the top-left to bottom-right continuously. Then the reading will be carried out from the left to right (indicated by 1 to 254) within each channel and all the channels simultaneously. The words in the 1st horizontal line in Fig. will come out in this order at the output terminal of the 1st channel, the 2nd line from the 2nd channel, and so on.

If the use of the full memory is not required, parts of the memory can be left blank. The relationship of write and read of 'blank word' is exactly the same as in (5). However, a certain code should be filled in this position, otherwise a previously written word, or a random noise, can remain in this position of the memory.

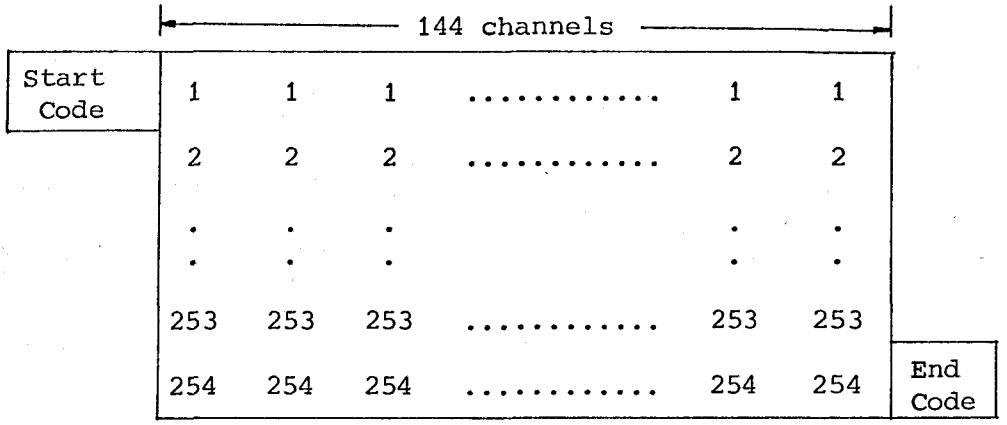


Fig. A1 Format for write mode 1

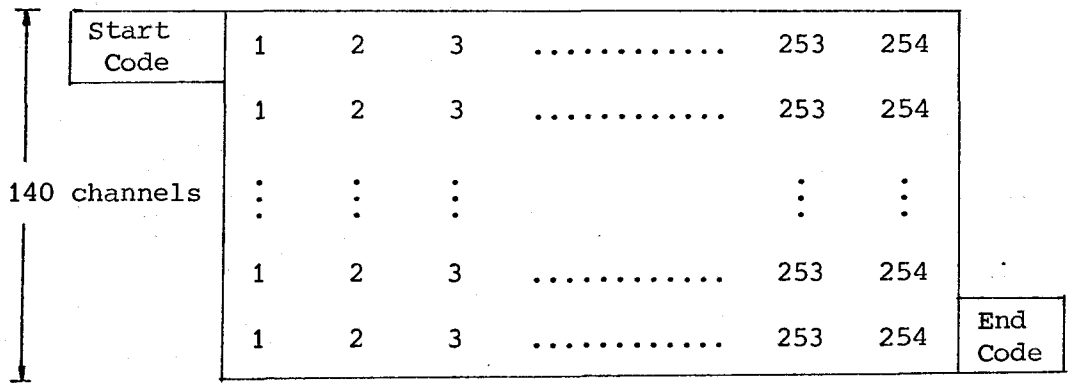


Fig. A2 Format for write mode 2

Note: The numbers in Figs. A1 and A2 show the order of simultaneous reading, and not input data.

Random mode

The formats (1) to (4) for the sequential modes can equally be applied to the random mode. In this mode, each word in the input data must be accompanied by an address into which the word is written. Fig. A3 shows the format of one section consisting of two words for (A1 and A2), data (D) and a space (-), where A1 is from 1 to 144, and A2 is from 1 to 254. The order of such sections in the input data does not have to be considered, because each section has an address. The maximum number of the sections is 36576. Note, address 0 and 255 are not used.

The formats by which data in a particular address is read is related to an external system (e.g. a printer). See instruction for each external system.

A_1	A_2	D	-

Fig. A3 Format for random write mode.

Appendix 2 SIMULATION OF A WRITE MODE

An actual write-mode operation can be completed in a short time (about one minute at the longest, with the optical tape-reader). This is, however, too short for checking various parts of the system in a write mode. In order to simulate a write mode operation for an adequate period for a test, the following procedure should be applied:-

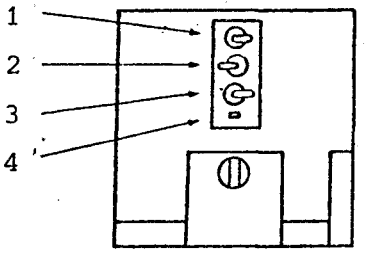
(1) Make a short tape in an endless loop which has no word.

(2) Interrupt all the light beams in the tape-reader head a few times by using a piece of paper, so that the system turns into a write mode (this is indicated by the red LED 'ON' on the front panel of the input memory cabinet).

(3) Apply the endless tape to the tape-reader. Set two of the switches on the tape-reader,

1 and 3 → Right side

2 and 4 → Irrelevant



Note, the read mode can be kept for any length of time without any special procedure.

Appendix 3 OPERATING INSTRUCTIONS

1. Preparation

Connect the following 6 connectors:-

CN130 (Memory cabinet)	- CN130 (Power-supply cabinet)
CN103 (Memory cabinet)	- CN103 (Tape-reader)
CN21 to CN22 (Memory cabinet)	- Main computation cabinet
Earth terminal (Memory cabinet)	- Earth terminal (Control cabinet)
Power line (Main cabinet)	- 240V AC line
CN11 (Tape-reader)	- CN11 (Control cabinet)

Switch on:-

Power switch (Control cabinet) ... Red light will be ON.
Power switch (Memory cabinet) ... 4 red lights will be ON.

If one of the 4 lights (possibly -12V indicator) does not come ON, try again after switching off for a few seconds.

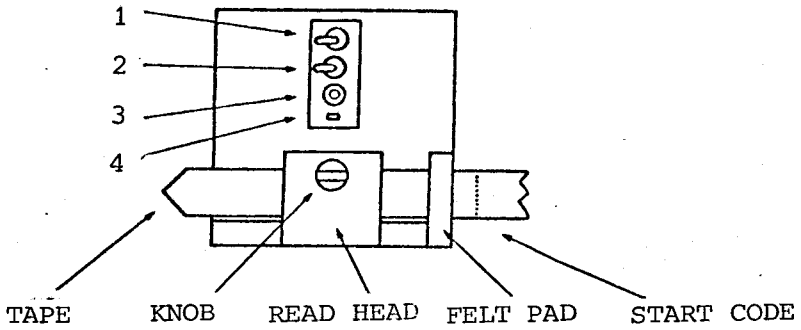
2. Selection of operating modes

Select the write mode and read mode required:-

Sequential or random mode switch	(on the rear panel)
Write mode 1 or 2 switch	(on the front panel)
Read mode 0 or 1 switch	(on the front panel)

3. Starting an input tape

A Tape-reader switches should be 1 → Left side, 3 → Neutral. 2 and 4 are irrelevant.

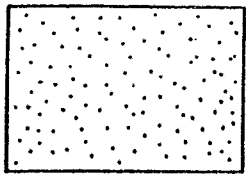


B The input tape should be wound onto a reel, and the reel should be supported by a holder, so that the tape can be pulled at a speed of about 1.3 m/s. Prepare a large box into which the tape is fed, unless an appropriate take-up reel is available.

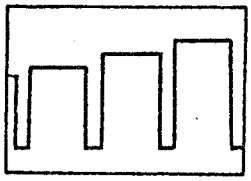
C Pass the tape through the felt pad and read head. Position the start code about 10 cm before the read head, and lock the knob.

D Press the red button on the memory cabinet. The tape will run until the end code passes through the read head. Then the tape will stop, and read mode will start automatically.

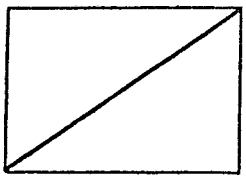
Note If the output of any memory channel is monitored by a CRO, the following patterns can be seen for a correct starting.



1 When the power switch is set to ON.



2 During a write mode.



3 After a write mode has been started.

4. Protection circuits

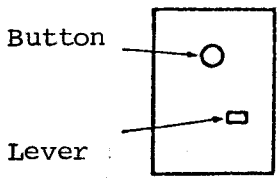
In order to protect the memory system from a high voltage, the +5V supply line of the memory is continuously monitored by an electronic circuit. If this voltage is changed accidentally, other dc power supply lines will be shut down within 100 ns. The 240V ac line will be cut off within 50 ms. Then a buzzer will be heard.

If this happens, disconnect the 240V connector from the ac power line, and eliminate the cause of the fault. The protection circuit (located at the rear of the power supply cabinet) can be reset in the following way:-

1 Press the lever downwards.

2 Press the button.

3 Then release the lever.



Note Each power supply unit (+5V, -12V or +12V) has its own protection circuit and a fuse. The 240V connector also has a fuse.

5. Random read mode

Since this operation is related to an external system, follow the instructions for each external system.

Appendix 4 GUIDE TO FAULT FINDING

Most parts of the input memory system are used for both the sequential and random modes, and only minor parts are used for the random mode only. The former can be tested rapidly by using sequential mode test tapes and observing the outputs on a CRO. The latter requires a checking with a numerical printer, but the circuits involve a few components.

If an abnormal waveform is found in a sequential mode test, most types of fault can be analysed by the waveforms shown in Fig. . Although the type of fault itself suggests the location of the faulty circuit, the following considerations also help to find the location.

(1) If a common type of fault is found throughout all the memory channels, the fault will be in the control circuit.

(2) If a common type of fault is found throughout a group of 6 memory boards (e.g. M2, M3, M4, M6, M7 and M8), and not in other groups, the fault will be one of the sub-control circuit boards related to this group (e.g. M5).

(3) If a fault is found in a single memory board only, the fault will be either the board itself or in a circuit of the relevant sub-control board.

(4) In the case of (1) to (3), the relevant board-connectors and wirings should be checked.

(5) If a fault is in a memory board, the faulty component can more easily be found by testing this board with the memory test unit.

(6) In most cases, a board which has a possible fault can be confirmed by replacing this with an identical board. Note, the 18 memory boards, M2, M3 ... M22 are identical; the 3 sub-control boards, M5, M12 and M19 are also identical. Similarly, an IC which has a possible fault can be confirmed by replacing this with an identical type of IC.

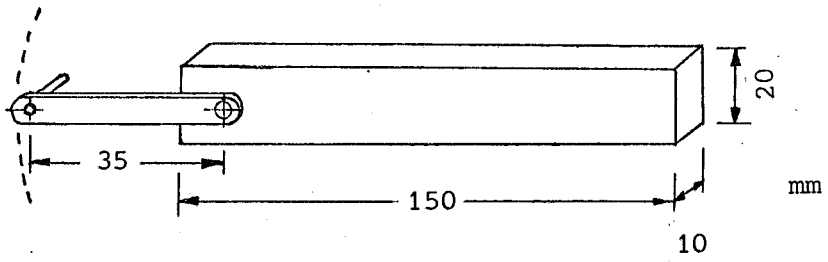
(7) Most faults, other than faulty ICs or wrong wiring, are dry-joints or short-circuits due to imperfect soldering.

(8) If test tape TEMB2 does not start in a test with the memory test unit, this suggests accidental contact (or contacts) in the data bus, address bus, R/W lines, CE lines or SW lines on the board.

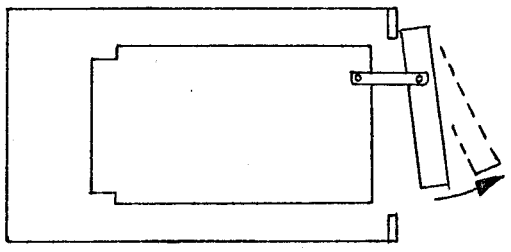
Appendix 5 EXTRACTING A CIRCUIT BOARD

A simple tool as shown in a has been prepared. Each memory board (M2, M3 etc) has two holes in its upper and lower parts. Use one of them for extracting the board with the tool, as shown in b or c. Each sub-control circuit board (M5, M12 or M19) has a hole for extracting it with the tool. Pull the board as shown in d.

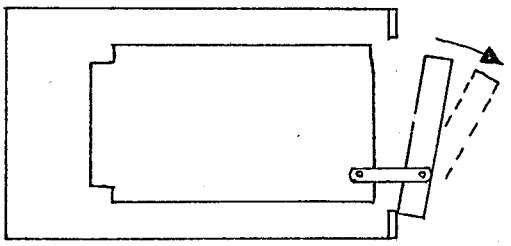
a



b



c



d