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INTERNAL DOCUMENT

85

OUTPUT MEMORY

A part of the electronic model
for tides and storm surges

S. Ishiguro
1980

NATURAL ENVIRONMENT RESEARCH COUNCIL

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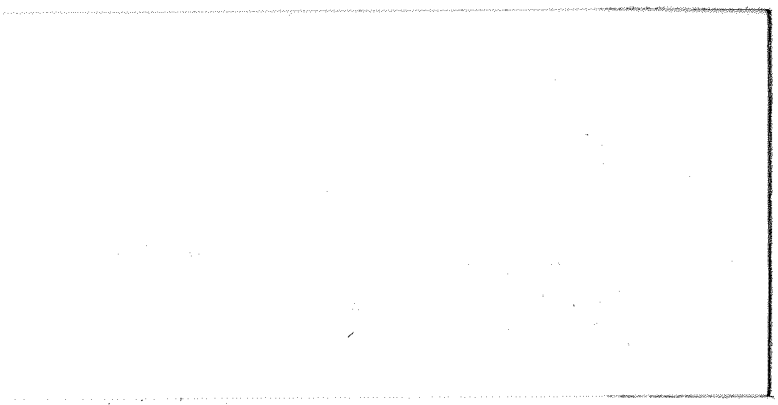

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O U T P U T M E M O R Y

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21 pages, 9 diagrams, 7 tables

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ABSTRACT

The output of each grid of the electronic model for tides and storm surges consists of three voltages which represent the water level, and the x and y components of water currents. Each voltage varies with time and contains data equivalent to typically 1K words/sec. This rate is too high for most peripheral instruments in the system. A circuit block which interfaces between the grid and the peripheral instruments has been developed for this purpose. The block consists of a programmable scaling circuit, DAC, memory, ADC and timing circuit, and has an 8-bit resolution with a storage capacity enough for a 10-day storm surge. The block is assembled on a single board (20 × 16 cm^2), and can be connected directly to the numerical printer, numerical-map printer, tape punch, XY recorder and vector printer in the model system.

1. INTRODUCTION

The electronic model for tides and storm surges contains its output data processing system which displays a set of output voltages from each grid of the model in usable forms; e.g. numerical tables, numerical maps, punched tapes, graphs and vector diagrams.

The speed of the data output from the grid is much faster than the maximum speeds of the peripheral display instruments. In order to adjust these speed differences, the data from the grid is first stored in a memory, then taken out at a speed matching each peripheral instrument. This memory is called 'Output Memory' in this system.

A 'Transient Recorder', the only standard product available at the time of the planning of the system, had been used for the output memory until 1978. However, this was the only part of the system which limited the resolution of data to 6 bits, after the 'Input Memory' (Ref. 1) had been changed from 6 bits to 8 bits.

Described in this paper is a circuit block designed to replace the previous 6-bit output memory with 8-bit. The new memory is based on a different principle, and has a larger capacity, better facilities, and a smaller physical size.

2. SCHEME OF THE SYSTEM

Fig. 1 shows the block diagram of the output memory.

A set of time varying voltages representing the x and y components of current (x, y), and water level (z) at each grid of the model is available simultaneously from the Main Computation Network (Ref. 4). These voltages are multiplexed by the multiplexer built in the network, so that a single set of voltages is selected at a time (typically 10 milli seconds for a 10-day storm surge). The selection is carried out automatically by a programmed circuit, or manually.

A set of selected voltages consists of three voltages: x, y and z. One of them is again selected by a multiplexer within the system. The finally selected voltage is scaled by a scale control which is programmed in relation to the selection of grids in the model.

The timing and duration of sampling a selected voltage is carried out by the Sample-time Control. The timing of the start of sampling can be decided either manually or automatically by the START switch. In an automatic operation, a trigger is given at the start of each computation through the clock in the Input Memory (Ref. 1). The duration of sampling is normally fixed to the period of 256 clock pulses (typically about 26 ms) although the clock rate can be changed.

A sampled voltage is digitized by an 8-bit ADC, so that a set of 256 words data is obtained. This is written into a random access memory. When the writing of the memory is completed, the memory turns into a reading mode automatically, and produces the 256-word data repeatedly with the rate of 10k words/s. This digital output can be recorded, if necessary, by a magnetic recorder. In a normal operation, this output is displayed on a CRO through the DAC(Y), with a synchronized time base produced by the DAC(X).

Since the above mentioned memory-reading rate is too high for an XY plotter and tape punch, another reading rate, 25 words/s, has been prepared. The change of the reading rate is carried out by a manual switch, 'WRITE-PLOT'. When this switch is turned to the PLOT position, the read rate is still 10k words/s, but when the START switch is pressed, the rate is changed into 25 words/s only for one set of reading (256 words), then automatically returns to the fast rate. During the slow reading, the outputs of the DAC(X) and DAC(Y) are fed into the XY plotter and tape punch, together with a signal for controlling the vertical movement of the XY plotter pen and a tape punch command signal.

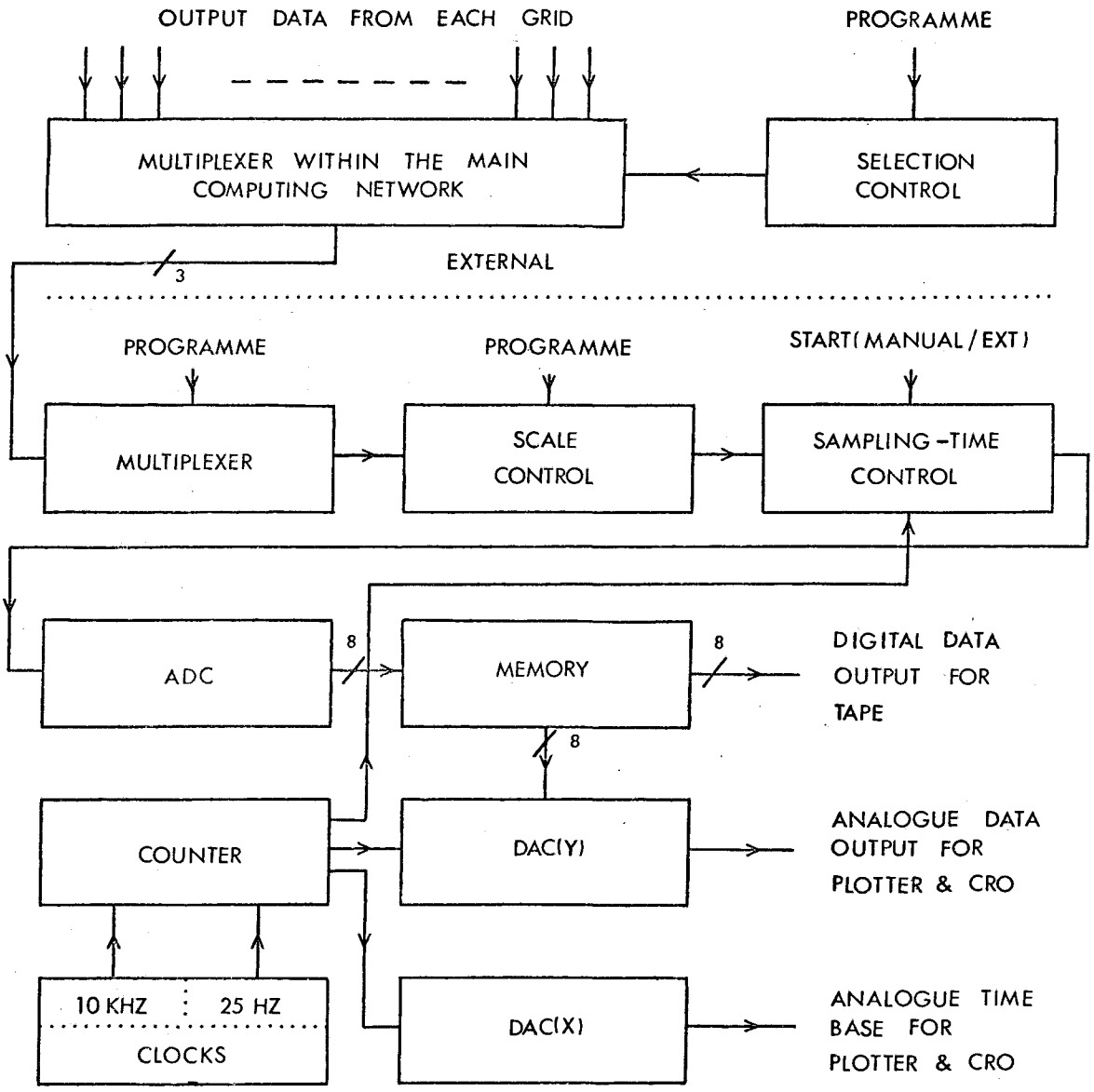


Fig. 1 Block diagram of the output memory, BD22.

3. CIRCUIT DESCRIPTIONS

Fig. 2 shows the circuit diagram of the output memory, and Fig. 3 shows its timing diagram.

Clocks

Two timers, 555(1) and 555(2), are used for the clocks of 10 kHz and 25 Hz respectively. An external clock input has been prepared for a more accurate clock rate in the input voltage sampling and for synchronization with the rest of the circuit in the model system. When the whole model is operated, the crystal clock in the Input Memory (Ref. 5) is used for the standard clock.

Normally the whole system is operated in a memory-read mode with the 10 kHz clock. Only when the WRITE-PLOT switch (SW1) is set to one of the positions, and START (SW2) or EXT TRIG is activated, the system turns into a memory-write mode or output-plot mode, both for a period of 256 clock pulses only. After this period, the system returns to a read mode automatically.

Read Mode

The 10 kHz clock generated by 555(1) enters into the chip-enable terminal ($\overline{CE}$) of the memory, 9112(1) and 9112(2), through 51/13, 51/4, 51/6 and 121(4)/6. The 121(4) is used for keeping the pulse width and shape constant independently from the type of clocks. During the read mode, the write/read terminals ($\overline{WR}$) of the memory are kept high, and the switching terminal (SW) of 4066(1) and 4066(6) are kept low, by 04/6.

The shaped 10 kHz clock pulses from 121(4)/1 enter into the binary code generator, 93(1) to 93(3), and its output (8-bit word) is fed into the address terminals of the memory. Therefore, the memory is read in the same order as its address numbers. The output from the 93(1) and 93(2) is converted into an analogue voltage by 2N425E(X) and 741(X) for the time base of a CRO display. The output of the memory is also converted into an analogue voltage by 2N425E(Y) and 741(Y) for the CRO display.

Write Mode

The system is turned into a write mode by setting SW1 to WRITE position and activating SW2 manually or EXT TRIG automatically. When this procedure is taken, 121(2) generates a pulse of 0.7 μs. This sets the flip flop, 00(1)/6, and lowers the input of 04/5 so that the data-ready signal ($\overline{DR}$) from AD570 passes through 51/6, and this enters into $\overline{CE}$ of the memory. At the same time, the switching terminal (SW) of 4066(1) and 4066(2) is activated so that the output of the ADC enters into the memory.

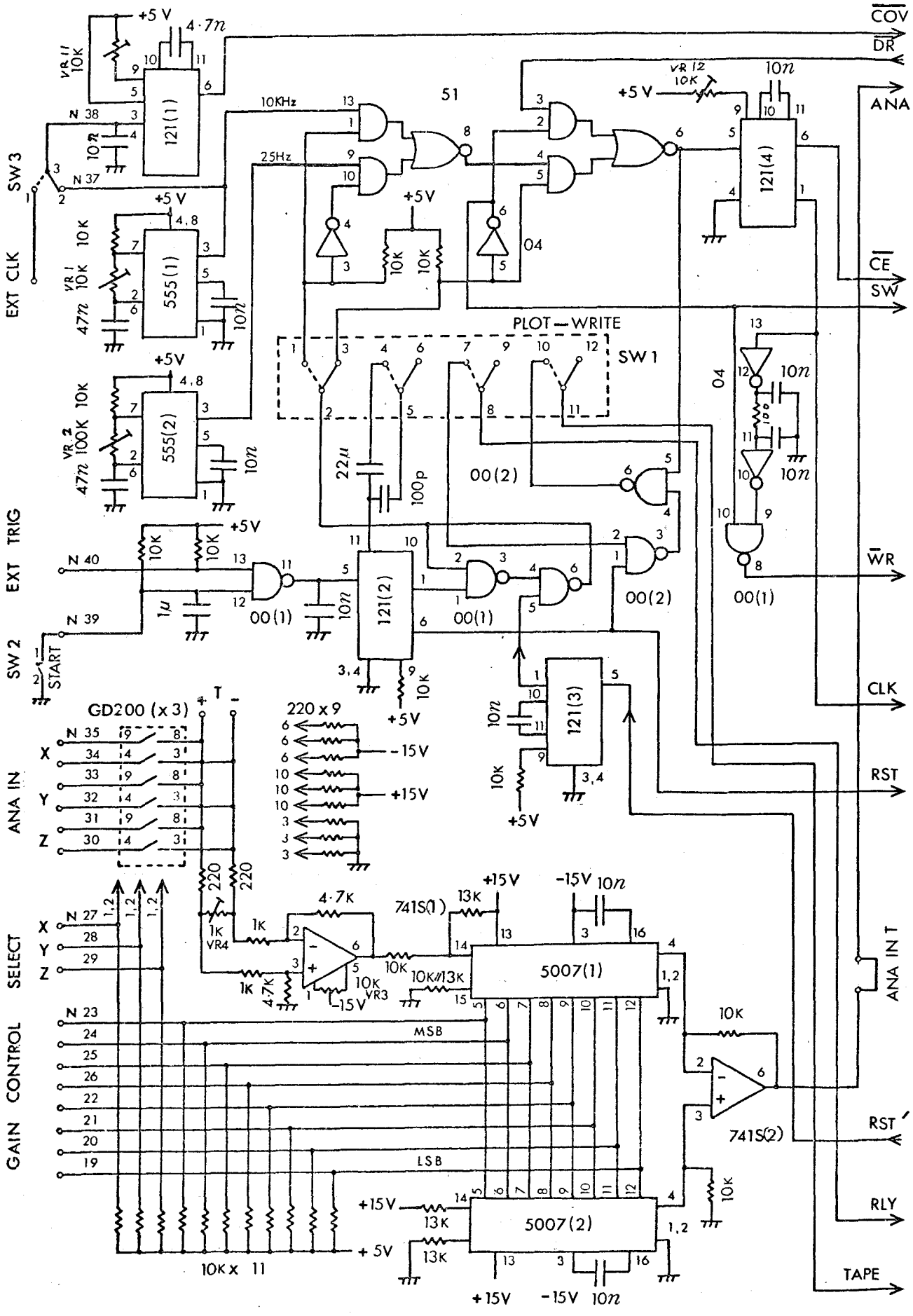
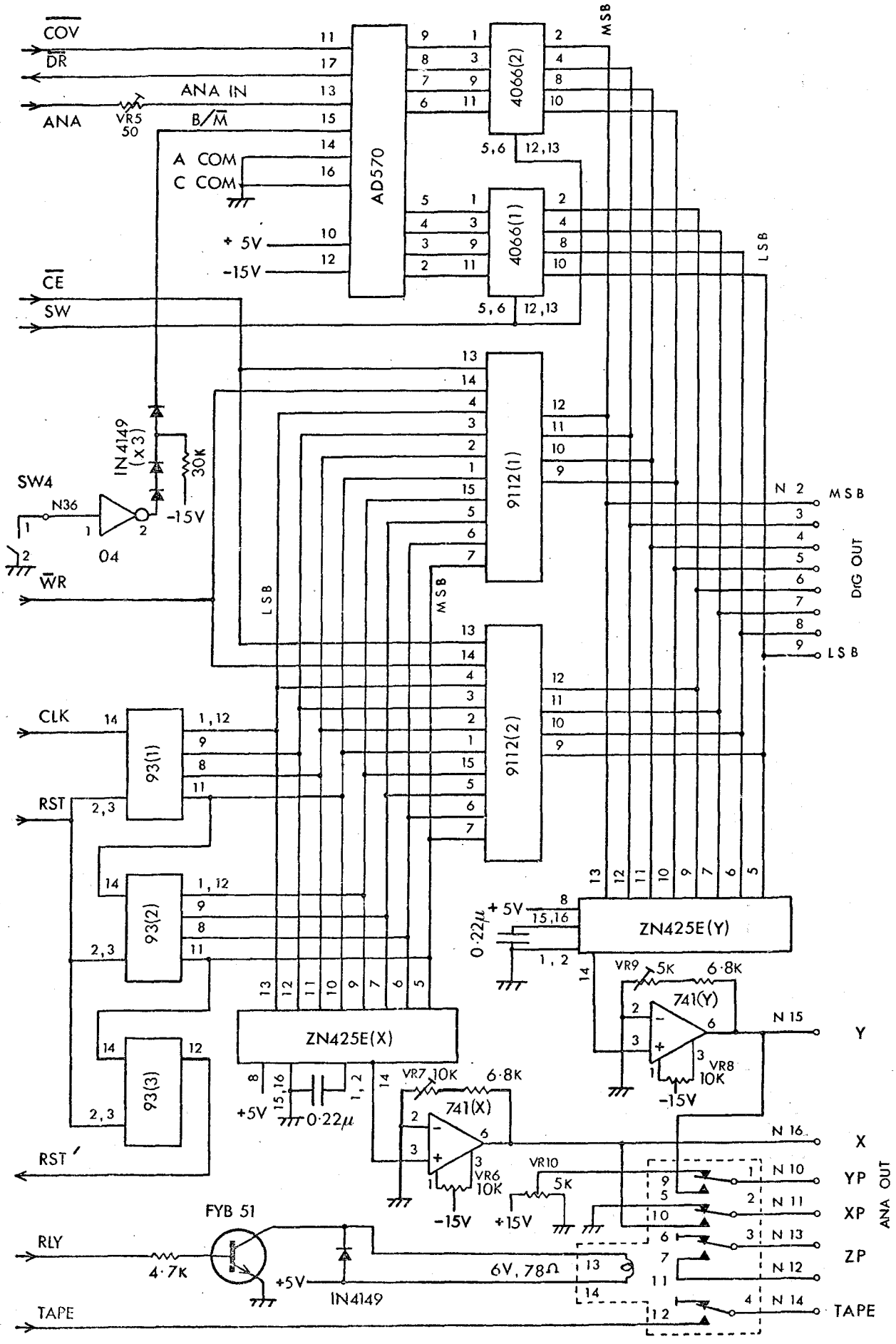


Fig. 2 Circuit diagram of the output memory, BD22.


COV
DR
ANA IN
ANA
VR5 50
B/M
A COM
C COM
+ 5V
-15V
AD570
4066(2)
4066(1)
MSB
LSB
CE
SW
IN4149 (x3)
30K
SW4
N36
04
WR
9112(1)
9112(2)
N 2
MSB
DrG OUT
LSB
CLK
RST
93(1)
93(2)
93(3)
RST'
ZN425E(Y)
ZN425E(X)
0·22µ
741(Y)
741(X)
VR9 5K
6·8K
VR7 10K
VR8 10K
VR6 10K
VR10 5K
N 15
Y
N 16
X
N 10
YP
N 11
XP
N 13
ZP
N 12
N 14
TAPE
ANA OUT
FYB 51
RLY
4·7K
IN4149
6V, 78Ω
TAPE

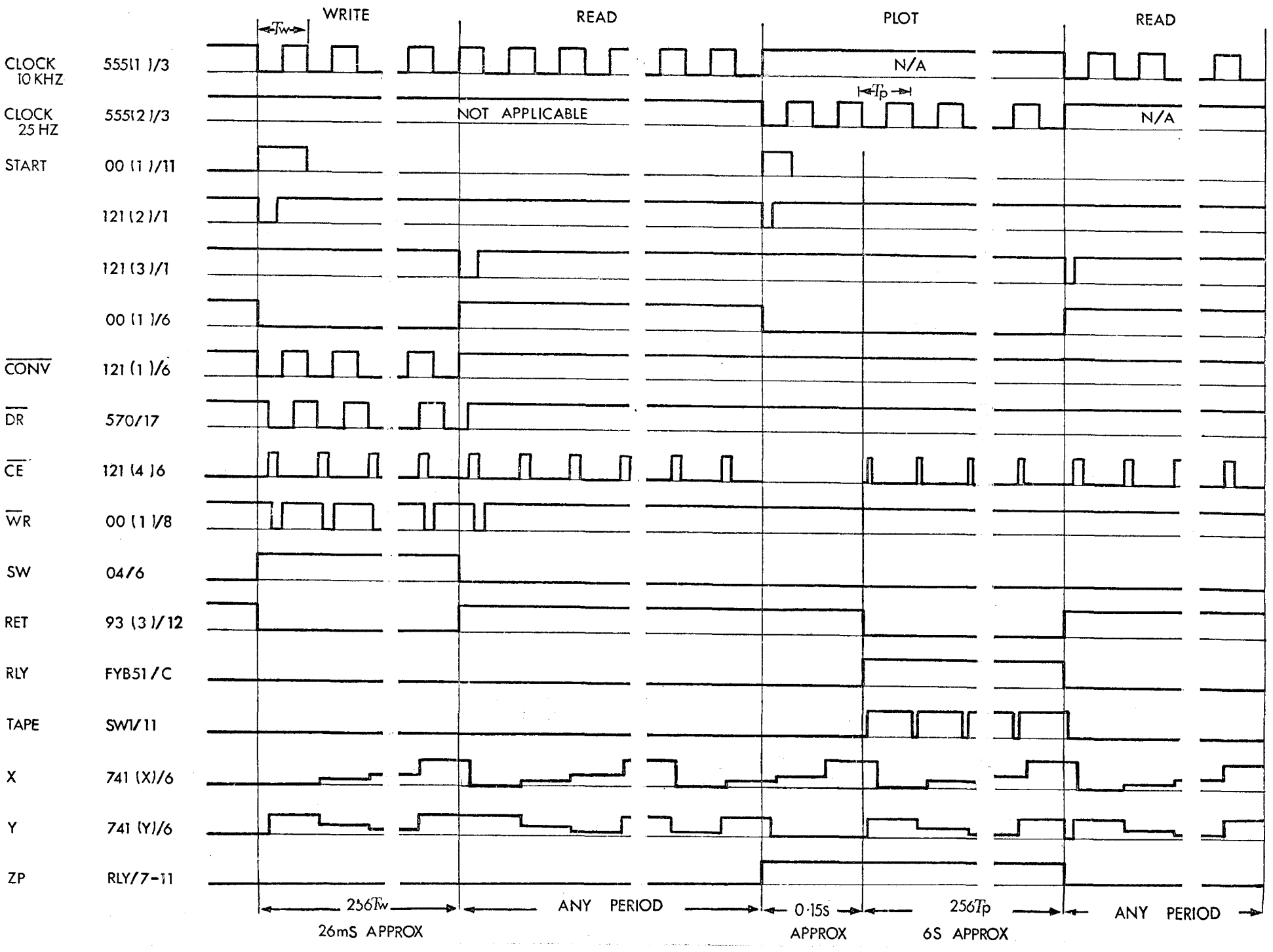


Fig. 3 Timing diagram of the output memory, BD22.

The output pulses of 121(4)/1, which are the shaped pulse form of $\overline{DR}$, enters into the binary code generator, 93(1) to 93(3). When 256 pulses have been entered, 93(3)312(RST') goes high, and resets the flip flop, 00(1)/6, through 121(3). Consequently, the analogue voltage fed into AD570/13 is digitized for a period which corresponds to 256 clock pulses (the 10 kHz internal clock or an external clock with any frequency).

During the write mode, both the outputs of the binary code generator and the memory are converted into analogue voltages as in the read mode, so that they can be monitored by a CRO.

Plot Mode

The write mode is applied for both the XY plotter and tape recorder (either a tape punch or a magnetic tape recorder), since both a digital-data output with a timing signal and an analogue-data output with an analogue time-base signal are available simultaneously. Because of the speed limitation of an XY plotter, the memory read rate of 25 words/s is used. This rate can be changed by adjusting the 10K VR connected to the 555(2) if necessary.

The plot mode is obtained by setting SW1 to PLOT, and activated by START (SW2) manually. When this is activated, 121(2) generates a pulse of about 0.15 sec which is determined by the 22μF capacitor connected to 121(2)/11. Therefore, the flip flop, 00(1)/6 is set by this pulse, about 0.15 sec after SW1 is activated. This delay is necessary for the movement of the XY plotter pen from the initial position to the start of a graph to be drawn. The initial position of the pen is determined by the data value written in the memory in the reset state, i.e. the data in its address No. 0. When SW2 is activated, the code generator is immediately reset. The flip flop, 00(1)/6 is also reset at the same time. Consequently, the data in the memory is read and plotted exactly in the same order as they were written.

The relay (in the bottom-right corner of Fig. 2) is activated through FYB51, only for the period which the 256 words in the memory are read, so that the analogue data output, analogue time-base and tape-recorder command signal (one pulse for each word) are fed into the XY plotter and the tape punch (or recorder).

Multiplexers

Two groups of multiplexers are used for selecting one set of data voltages from each grid of the model (three voltages from each grid; e.g. 1500 voltages in all from 500 grids). The first group of multiplexers is built in the Main Computation Cabinet (see Fig. 1 for the block diagram, and see Ref. 4 for their details). The second group of multiplexers is contained in this circuit, and used for selecting one of the three voltages (indicated by X, Y and Z at the board terminals N30 to N35 in Fig. 2). Three sets of CMOS analogue switches, CD200s, are used for the second multiplexers which are controlled by a set of digital signals, SELECT XYZ (board terminals N27 to N29).

Input-scale control

One of the voltages selected by the GD200s is passed through a balanced input amplifier, 741S(1), and fed into the scaling circuit. The scaling circuit consists of two identical multiplying type DACs, 5007(1), 5007(2), and an operational amplifier, 741S(2). The 5007(1) amplifies an input signal consisting of an AC on a certain DC level, with 256 different gains depending on an 8-bit digital code fed into its terminals 5 to 12. The gain control of 5007(1) affects the DC level, as well as the AC signal. To compensate for this disadvantage, the 5007(2) controls the gain of a DC voltage in the same proportion as the DC level change in 5007(1). Consequently, the balanced output of 741S(2) has a controlled amplitude of AC signal with a constant DC level. This voltage is fed into AD570/13.

The gain control signal consists of 256 binary words (0 to 265 in a decimal equivalent), and is fed into board terminals N19 to N23. Fig. 4 shows two types of gain control:'Programme tape input' (in a separate case) and a set of 8 manual switches (on the main control panel) together with three voltage selection switches, X, Y and Z. The former is used for a gain control which is synchronized with the selection of grids (see a separate paper for this necessity). The latter is used for individual control of gain.

The programme tape input is essentially a simple tape reader for a parallel 8-bit punched tape on which the control programme is recorded. The tape is driven by a step motor with synchronization of the scanning of grids of the model. The tape can also be moved continuously or step-by step, by controlling three switches, S, C and AUTO S-C.

Bipolar/Monopolar Control

The dynamic range of AD570 can be used more efficiently by selecting its operation mode, either bipolar or monopolar according to the input-data voltage. This selection is carried out by controlling the voltage at terminals 15 of AD570, through BIP-MON switch (SW2) and 04/2. SW2 is on the main control panel.

Power Supply

A power supply having +5V, +15V and -15V is required for this circuit. The power supply is shared with other circuits in the main control cabinet, but its lead wires are separated from other circuits at the voltage regulated terminals.

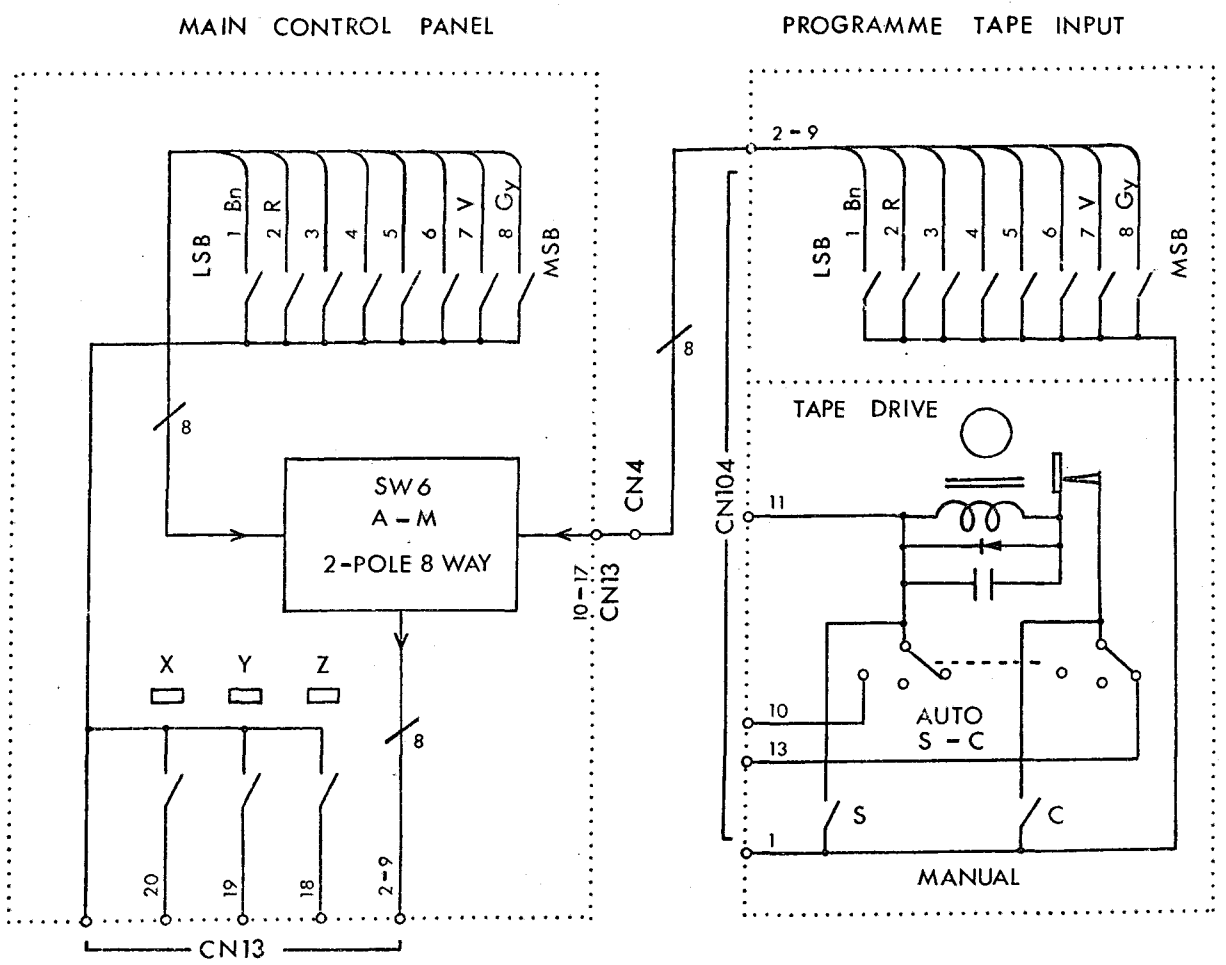


Fig. 4 Manual and programmed gain controls.

4. PHYSICAL ARRANGEMENT

Fig. 5 shows the board (BD22) on which the circuit shown in Fig. 2 is arranged. BD22 is contained in the main control cabinet. Table 1 shows the connections of edge-connector terminals of BD22 and other circuits.

Fig. 6 shows the physical arrangement of BD22, the main control board (parts which are related to BD22 only), XY plotter, CRO, tape punch and programme-tape input for the gain control, together with their connections. Tables 1 to 4 show the circuit connection related to BD22.

Fig. 7 shows the actual apparatus of the programme-tape input for the gain control. This includes a tape driving system, and it is contained in a noise-suppressing box (200 × 205 × 140 mm^3).

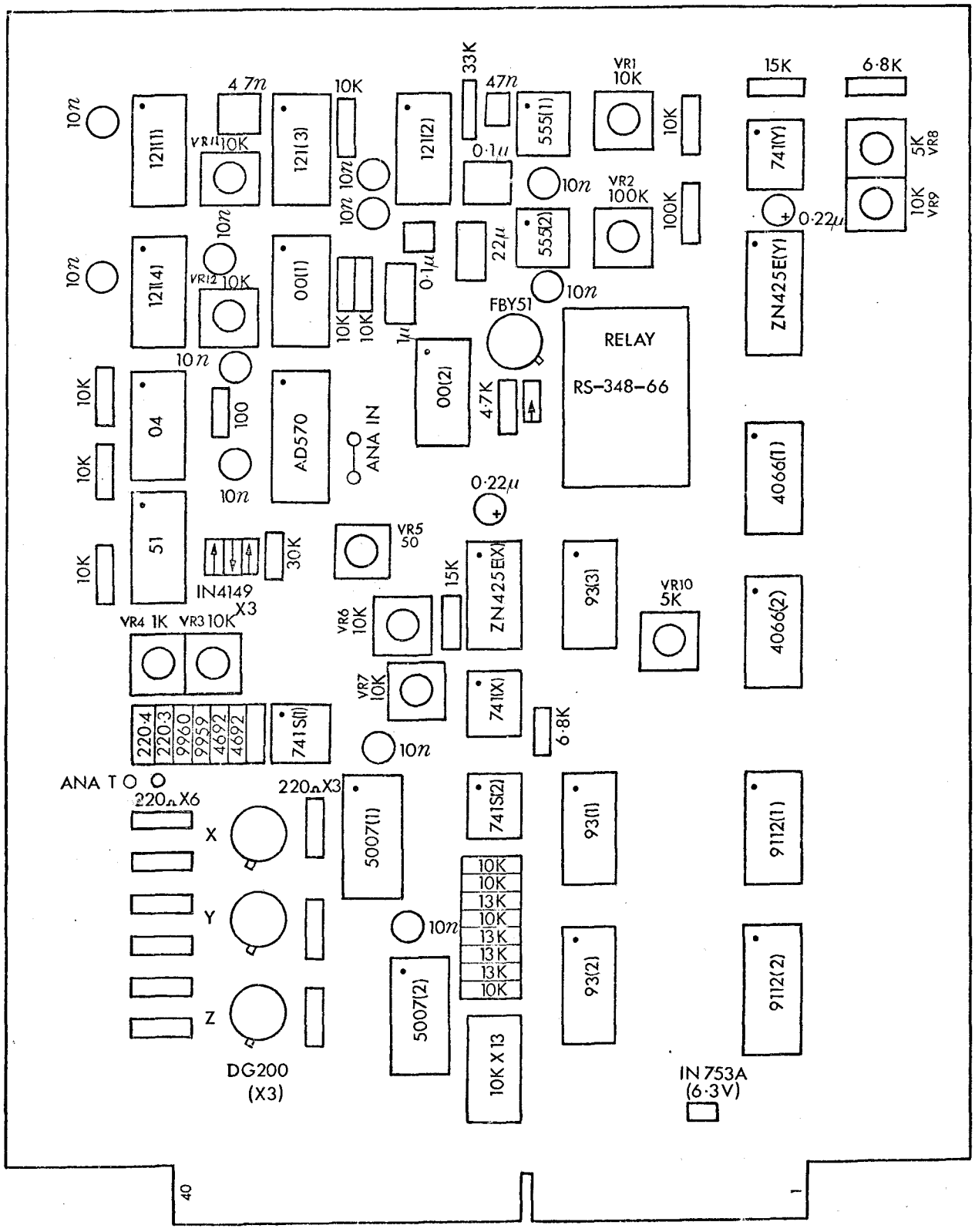


Fig. 5 Component arrangement of BD22.

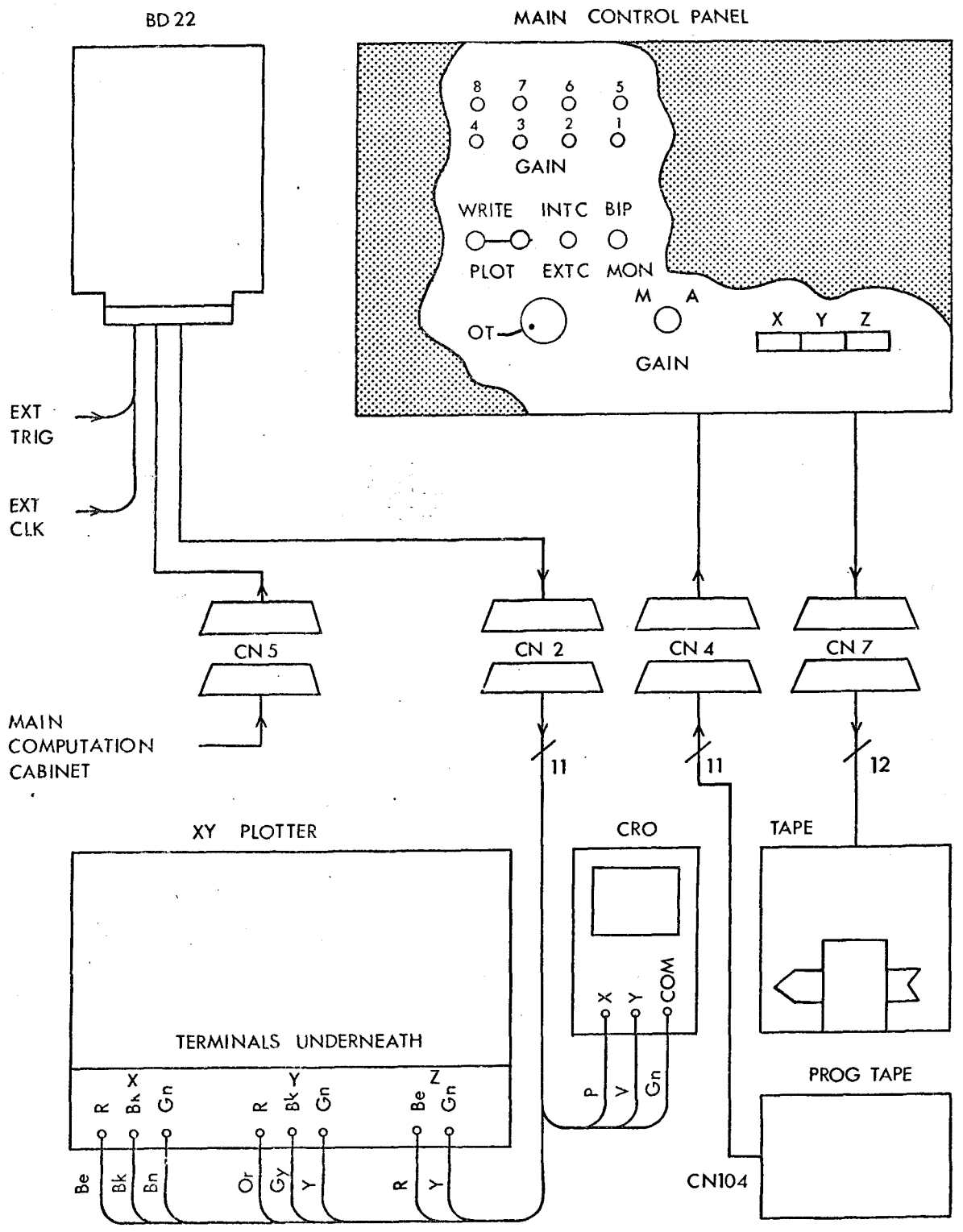


Fig. 6 Physical arrangement of BD22 and its related parts.

Table 1. Connection of BD22 Output Memory

Pin No N1	W	CN15/9	SW1/11 W-PLOT
2	Gy	13/27	8 MSB
3	V	25	7
4	Be	CN14/20	6
5	Gn	19	DIG OUT 5
6	Y	18	4
7	Or	17	3
8	R	16	2
9	Bn	15	1 LSB
10	Bn	CN2/1	XP
11	R	2	ANA XP'
12	Or	3	OUT ZP
13	Y	4	ZP'
14	Gy/R	BD11/2	TAPE COM'D
15	Be	CN2/5	X
16	V	6	Y
17-18	-		
19	Bn	CN13/2	1 LSB
20	R	3	2
21	Or	4	3
22	Y	5	GAIN 4
23	Gy	9	CONT 8 MSB
24	V	8	7
25	Be	7	6
26	Gn	6	5
27	W/R	CN13/18	X
28	W/Be	19	SELEC Y
29	W/Gn	20	Z
30	Bn	CN5/6	R X
31	R	7	Bk X'
32	Or	8	R Y
33	Y	9	Bk Y' ANA IN
34	Gn	10	R Z
35	Be	11	Bk Z'
35	Gn	CN15/26	BIP-MON
37	Y	27	EXT-INT C
38	Or	28	"
39	R	10	START
40	Bn	REAR PAN	EXT TRIG
C1	Bn	CN15/1	
C2	R	2	
3	Or	3	
4	Y	4	W-PLOT SW
5	Gn	5	
6	Be	6	
7	V	7	
8	Gy	8	
9-11	Gn	Common	
12	Bk	5V	
13-14	-		
15	R	15V	
16	Gn	Common	
17	Be	-15V	

Table 2. Connection of CN2

Pin No			
1	Bn	BD22/N10	PX
2	R	11	PY
3	Or	12	PLT PZ
4	Y	13	PZ'
5	Be	15	CRO X
6	V	16	Y
7-13	-		
14	Gn	Common	

Table 3. Connection of CN4

Pin No			
1	Gn	Common	
2	Bn	CN13/10	1 LSB
3	R	11	2
4	Or	12	3
5	Y	13	4
6	Gn	TAPE 14	5
7	Be	IN 15	6
8	V	16	7
9	Gy	17	8 MSB
10	Y	CN5/4	3055 COL
11	Bn	24V	
12	Gn	Common	
13-25			

Table 4. Connection of CN5

Pin No			
1	R	24V	
2	Gn	Common	
3	Gy	BD10/4	
4	Y	CN4/10	3055 COL
5	-		
6	Bn	BD22/30	R X
7	R	31	Bk X'
8	Or	32	R Y
9	Y	33	Bk Y'
10	Gn	34	R Z
11	Be	35	Bk Z'
12-21	-		
22	Gy/Be	-15V	Be
23	Gn	Common	Y
24	Gy/R	15V	V
25	-		

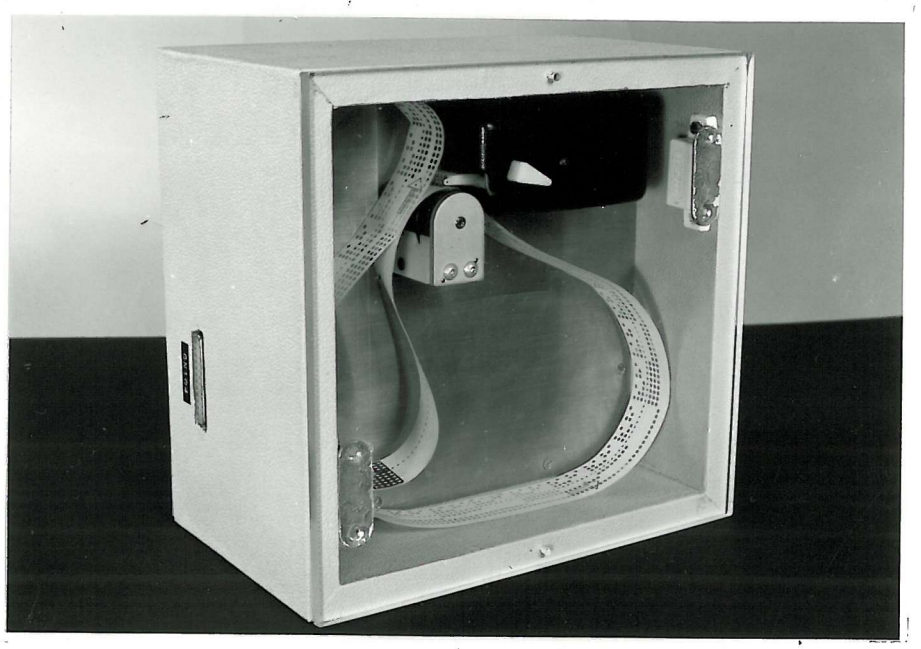


Fig. 7 Programme tape input for the gain control.

5. ADJUSTMENTS AND TESTS

Most parts of the BD22 are digital circuits, and no adjustments are required. The timing diagram shown in Fig. 3 will help to confirm the normal performance of this digital circuit.

However, some adjustments are required for setting the clock rates, and the input and output scalings which are mainly related to the external conditions. The parts which should be adjusted are listed in Table 5. Normally no frequent adjustments are required.

Table 5 Adjustments of BD22.

Parts to adjust	Function
VR1	Clock rate for WRITE (& READ) and CRO display, 10 kHz.
VR2	Clock rate for PLOT, 25 Hz.
VR3	Zero set of the input amplifier.
VR4	Full scale of the input amplifier.
VR5	Full scale of the ADC.
VR6	Zero set of the X axis (time base) of the output.
VR7	Full scale of the X axis of the output.
VR8	Zero set of the Y axis (data) of the output.
VR9	Full scale of the Y axis of the output.
VR10	Off-set of the Y axis of the output.

See Fig. 5 for the positions of VRs on the circuit board.

Clock rates

Two clock rates, 10 kHz and 25 Hz, should be adjusted to the nominal value approximately. (An accurate rate is required only for the sampling time control, and the crystal-controlled clock contained in the Input Memory is used for this purpose).

ADC

Table 6 shows the designed relationship between the analogue input (at the test terminals, ANA IN T) and digital output. By feeding a specified input voltage, adjust VR5 to obtain the corresponding digital value.

Table 6 Analogue-digital relationship at AD570 terminals

Mode	Analogue input (V)	Digital output	
		Binary	Dec. equiv.
Monopolar	0.000	0000 0000	0
	9.999	1111 1111	255
Bipolar	-5.000	0000 0000	0
	0.000	1000 0000	127
	+4.999	1111 1111	255

Each LSB = 9.766 mV

Input scaling

Make a short circuit of test terminals +T-, and set the digital gain control of the input scaling circuit to maximum (1111 1111). Then adjust VR3 to obtain a zero output voltage at test terminals ANA IN T.

By setting the digital gain control of the input scaling circuit to maximum (1111 1111), and by applying an appropriate DC voltage, E_m, to test terminals +T-, adjust VR4 so that the output voltage at ANA IN T becomes 9.999V (for the monopolar mode). The value of E_m is specified separately according to a model parameter.

After the above-mentioned tests have been completed, check other relationships shown in Table 6. Typical full scale errors will be ±2LSB or ±0.2%. A better accuracy can be obtained by adjusting VR5 more precisely.

Output scaling

The adjustments of the output scaling are related to the external instrument used, mainly an XY plotter. (Adjustments for a monitor CRO is less critical). Usually an XY plotter has its own scale controls including multipliers. Adjustments of VR6 to VR10 should be carried out for a selected scale of the XY plotter, and after that, usual scale controls should be carried out by using the controls within the plotter.

6. OPERATION PROCEDURES

BD22 has been built in the main control cabinet, and can be controlled by its control panel. Fig. 6 shows external instruments which should be operated with BD22. An XY plotter should be used which has a reasonably high writing speed (e.g. 120 cm/s for the Y axis, 80 cm/s for the X axis), a large acceleration capability (e.g. 3 m/s for the Y axis, 2 m/s for the X axis), and a fast response in the up-and-down motion of the pen. A CRO should be used in an XY scanning mode. Note, the XY plotter and the tape punch can be operated simultaneously.

The operating procedures are as follows:-

1 Connect the instruments as shown in Fig. 6.

2 Set the main control knob on the control panel to TO.

3 Select a bipolar or monopolar mode by switch BIP or MON.

4 Select the type of input data, the x or y component of the water current, or the water level, by pressing the push button switch X-Y-Z* on the control panel.

5 Select the gain control, manual or automatic, by GAIN M or A.

(a) If the gain is controlled manually, use switches GAIN 1 to 6, where 1 corresponds to LSB, and 8 to MSB.

(b) If the gain is controlled automatically, use the PROG TAPE unit, with an appropriate control tape. The movement of the tape can be controlled by operating three switches on the case of the unit, as well as a synchronized motion with the scanning of grids in the model.

6 Select the data sampling clock, either the internal (approximately 10 kHz for an experiment) or external (an exact frequency for a real operation), by setting INT C or EXT C. Normally the crystal clock in the Input Memory is used for a real operation. The input terminal for this clock is on the rear panel of the cabinet.

7 Usually the WRITE-PLOT switch (a change-over switch with a red push-button switch) should be set to WRITE. In this position, the circuit is still in a read mode. Only when the red push button or EXT TRIG terminal (on the rear panel) is activated, the circuit turns into a write mode. Then after a period of 256 clock pulses, the circuit returns automatically to the read mode (of the newly written data) which is displayed on the CRO. Use the EXT TRIG for an accurate start of the sampling.

8 For plotting the newly written data using the XY plotter and/or tape punch, set the WRITE-PLOT switch to PLOT. In this position the circuit is still in a read mode. When the XY plotter and/or tape reader are ready, press the red push button switch so that the plotting is carried out. After the 256 words are plotted, the circuit returns automatically to the read mode of the same words.

9 In order to monitor newly processed data, press the red button as many times as required with the WRITE-PLOT switch in WRITE position. Every time the red button is pressed, the monitoring data is refreshed by sampling 256 increments of the write clock pulses.

* These X, Y, Z are not related to the symbols used for the XY plotter.

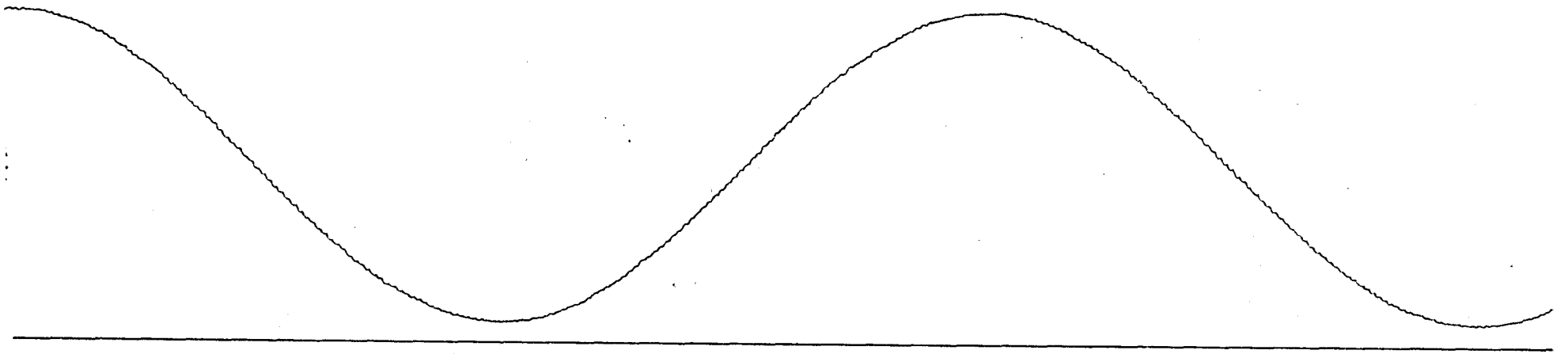
7. PERFORMANCE

Table 7 shows a summary of the performance of the output memory. Figs. 8 and 9 show examples of graphical and numerical outputs of the output memory.

Table 7 Performance of the output memory, BD22

Frequency range of analogue input	Required for tide/ surge analyses		DC to 10 kHz
	Input amplifier		DC to 200 kHz
	ADC		DC to 400 kHz
Amplitude range of input at ANA X, Y, Z	Monopolar		0 to +10mV
	Bipolar		-5mV to +5mV
Multiplexers	Internal		3-channel selection by binary codes
	External (in the Main Comp. Cabinet)		1500 channels by the grid selector
Data sampling clock	Internal		10 kHz approx.
	External (in the Input Memory)		Any frequency up to 200 kHz
Plotting clock	For an XY plotter/tape punch		25 Hz approx.
Analogue output	Data		0 to 2.5V
	Time base	For a CRO	0 to 2.5V 25.6ms repetition
		For an XY plotter	Single sweep with 0.15s delay*
Digital output	8-bit parallel binary, 256 words, single pulse traces, at the rate of 25 words/s approx. Synchronization signal for each word		
Input gain control	256 steps between zero and maximum Programmed: Tape reader with a programme tape, and synchronized with the grid selector Manual: 8 switches for binary code		
Analogue input resistance	1KΩ**		
Resolution	8-bit		
Relative accuracy	±1/2 LSB @ 25°C		
Temperature range	0 to 70°C		
Gain temp. coeffic.	176 ppm/°C		
Power requirement	+5V (350mA), +15V (8mA), -15V(14mA)		
Physical	29 ICs on a single board of 16 × 20 cm²		

* For settling the plotter pen at the start of each trace.
**Designed to match the multiplexers.



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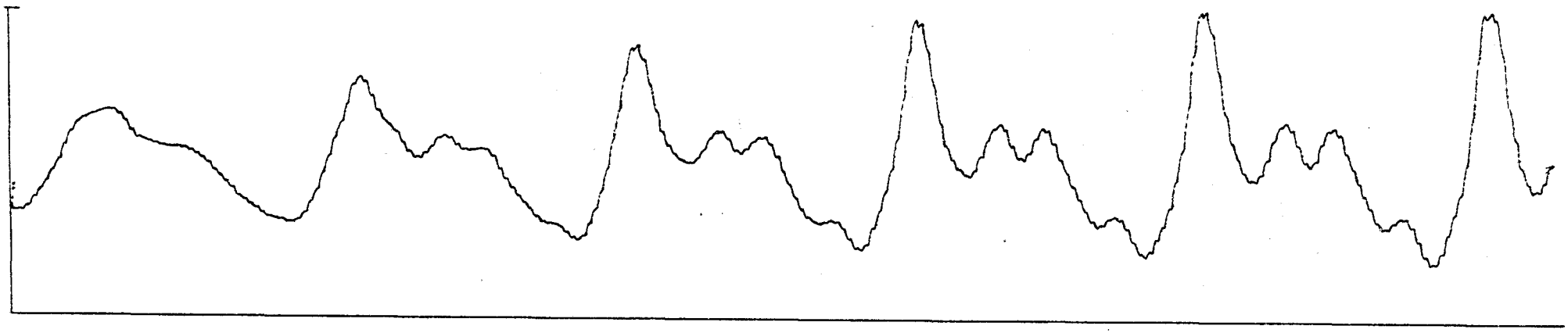
000 000 000 000 000[253 253 253 253 252 252 251 249 248 246 245 243 241 239 236
234 231 228 225 222 218 215 211 208 204 200 195 191 187 182 178 173 169 164 160
156 149 144 140 134 130 125 120 115 110 105 100 095 090 085 081 076 072 067 063
059 054 050 047 043 039 036 032 029 026 023 020 018 015 013 011 009 008 006 005
004 003 002 002 001 001 001 001 000 000 000 000 000 000 001 001 002 003 004 005
006 008 009 011 013 015 017 019
022 025 028 031 034 037 041 045 049 053 057 061 065 069 074 078 083 087 092 097
102 107 111 116 121 126 131 136 141 145 151 156 161 165 170 175 179 184 188 191
197 201 205 209 212 216 219 223 226 229 232 235 237 239 242 244 245 247 249 250
251 252 253 253 253 253 253 253 253 252 251 250 249 248 246 244 242 240 238 235
232 230 227 224 220 217 213 210 206 202 198 194 189 185 180 176 171 167 162 157
152 147 142 137 132 128 122 118 113 108 103 098 093 088 084 079 074 070 065 061
057 053 049 045 041 038 034 031 028 025 022 019 017 014 012 010 009 007 006 004
003 003 002 001 001 001 001 002 002 003 004 005 006 008 009 011 013 015 018 021]
```

Fig. 8 Example of graphical and numerical outputs from the output memory. Sinusoidal waveform, sampled at 10K increments/sec.



222	220	220	222	222	222	222	220	220	222	220	[208	208	202	199	196	193	192	191	193
154	162	166	168	170	172	173	172	168	162	154	149	147	145	143	142	141	141	141	146
138	135	132	128	122	117	112	107	101	097	093	090	085	083	082	081	079	079	082	080
097	107	121	135	149	163	178	193	200	195	184	172	154	150	153	145	138	133	133	137
143	152	152	149	144	142	139	140	141	140	134	126	115	108	102	096	092	084	089	079
078	076	071	067	065	069	079	091	105	125	149	175	223	223	226	214	194	172	155	144
137	132	129	129	134	141	150	156	156	149	140	137	141	147	154	151	145	139	124	111
102	092	085	081	079	081	083	081	076	067	060	058	053	077	091	107	125	151	187	223
247	244	220	192	164	145	134	125	121	119	125	136	149	159	164	158	145	135	133	139
151	158	158	147	134	124	112	102	092	083	078	082	085	087	084	077	056	055	053	058
068	079	095	117	143	183	223	255	255	235	202	172	149	135	124	117	117	123	135	151
153	156	150	147	133	128	134	148	159	162	156	141	128	116	106	096	084	078	078	080
087	097	080	068	056	048	049	059	074	090	107	133	173	223	255	255	250	215	178	152
138	116	109	112	118	133]	088	020	000	000	000	000	000	000	000	000	000	000	000	000

Fig. 9 Example of graphical and numerical outputs from the output memory. Arbitrary waveform, sampled at 10K increments/sec.

8. CONCLUSION

The output data processing system for the electronic model previously contained an instrument (a standard product, 'Transient Recorder') by which the data was stored temporarily and its processing speed adjusted for the peripheral instruments of the system. This was the only part in the system, which limited the resolution of data to 6 bits. This has now been replaced by an 8-bit resolution circuit block designed for the purpose. This block has a larger storage capacity (2.5 times) and smaller physical size (a single board), and a programmable scaling control. The block can be connected directly to the recording instruments in the system, while the previous instrument required some interfaces.

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