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The IOSDL Seasoar Pressure Digital to Analogue Converter

T J P Gwilliam & J Smithers

1990

Natural Environment Research Council

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ABSTRACT

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DIAGRAMS/COMPONENT SCHEDULE

THE I.O.S.D.L. SEASOAR PRESSURE DIGITAL TO ANALOGUE CONVERTER.

1. INTRODUCTION.

The Seasoar system is a towed oceanographic instrumentation package for use in the top 400 metres of the ocean. At IOSDL a Neil Brown Mk.3 conductivity,temperature and depth (CTD) unit is used as the prime sensor package for data collection and transmission to the shipboard equipment. With the pressure signal from the underwater CTD sensor system as the feedback element in a servo loop, the depth of the underwater vehicle can be controlled in a manual or in a fully automatic mode.

Over the past year the original deck units have been replaced by the more modern 1401 units. These units are designed for interfacing with microprocessors and other digitally operated equipment and regretfully unlike their predecessors do not provide an analogue output of the sensor data. With the IOSDL Seasoar controller requiring just such an analogue pressure signal, and no commercial unit available, it was therefore found necessary to design a circuit.

This report describes a circuit that will generate these pressure and temperature analogue signals from the CTD serial data stream. The temperature signal was included at little extra cost for possible experimental use in the future for controlling the Seasoar in a temperature following mode.

2. GENERAL DESCRIPTION.

This section provides a less detailed description of the circuit for those readers wishing only to have a general understanding. For ease of explanation reference is made to the block schematic of fig.1a, fig.1b and the block schematic of fig 2.

2.1 INPUT SIGNAL FORMAT.

The signal at the input from the CTD 1401 deck unit is a RS232 serial digital data stream operating at 9600 baud. The IOSDL serial data from the Seasoar CTD is made up of repeated "frames" of 18 words, with each frame containing the sampled information from the CTD underwater unit. For each parameter measured, the position of the data word within the frame is fixed, thus word 1 is the synchronising word, words 2 and 3 contain the pressure data, words 4 and 5 the temperature data, words 6 and 7 the conductivity data. The frames of data are repeated at the sampling or frame rate of eight frames a second. Each word consists of one start bit, eight data bits and two stop bits which explains why conductivity, temperature and depth measurements each require two words to convey the 16 bits of information.

Fig.1a illustrates this word format while fig.1b show the arrangement of the words within the frame.

2.2 CIRCUIT OPERATION.

The RS232 signal from the 1401 deck unit is applied to the pulse shaper and inverter where it is processed to produce two identical output signals. The switches, S1 and S2, provide a means of changing the polarity of the signals to the correct logic levels for the following stages.

The serial data from switch 1 is connected to the serial to parallel converter where the start bit and two stop bits are removed from each 11 bit word. The resultant eight data bits are then transposed to the output of the convertor in a parallel format for connection to the twelve bit digital to analogue converter (DAC).

The data output from switch 2 is used by the frame pulse generator to produce a synchronising pulse that resets the circuit on the completion of the last word in the frame and restarts the sequence at the start pulse of word one in each frame. Study of the word format of fig.1(a) show that every 11 bit word must contain at least one bit at zero level, the start bit, and the frame pulse generator uses a 12 input AND gate to detect the finish of the last word in the frame and the start of word 1 in the next. To allow for variation in the time interval between words a pulse is also used in the AND gate to preclude any false pulse generation. As visual confirmation that the circuit is working satisfactorily the frame pulse is used to drive a flashing indicator at the data frame rate.

Both the pressure and temperature information utilise two 8 bit words to convey the range and resolution required by the scientists. For Seasoar control 12 bit resolution, equivalent to a pressure of 0.16 dbars over a range of 550 metres, is quite sufficient.

Using pulses generated in the serial to parallel converter a set of strobes are produced in the word strobe circuit to sample the pressure and temperature data words in the digital to analogue convertor (DAC). Using it's own internal reference voltage the unit converts the 12 bit binary data, latched into it by the strobes, into a analogue voltage. After conversion this voltage is latched into the sample and hold devices by a further set of strobes produced by the strobe generator.

The analogue voltage is held constant at the output of the sample and hold circuits until the next frame when the conversion will be repeated and the analogue voltage updated.

3. CIRCUIT DESCRIPTION.

Using the basic waveforms of fig.1a and fig.1b plus the full circuit diagram of fig.4 the following is a more detailed explanation of the circuit operation.

The bipolar RS232 data signal is converted to a unipolar waveform using the pulse shaper circuit of IC1a and the inverter of IC1b. The two 0/+5volt outputs from this circuit are each connected to polarity switches to correct for the signal polarity selected in the underwater unit. The output of switch 1 is connected to the serial to parallel converter IC2. This device is a 6402 universal asynchronous receiver transmitter, UART, hard wired for a 11 bit word having 8 data bits, 1 start bit and 2 stop bits. The data received status flag pulse, DR, goes to a high level when a data word has been correctly transferred to the receiver buffer register. This positive going level change is utilised in three ways, the first to clock a decade counter, IC9, for word strobe generation, the second to reset the frame pulse generator circuit and finally to generate a pulse to clear the DR status flag thereby permitting the next word character to be received. This latter pulse is produced using the two cascaded one shot monostables of IC5, CD4013, which provide a delay of the active output edge, to pin 18 of the UART, on the DR pulse of approximately 0.4 milleseconds. The delay allows adequate time for the parallel information at the UART output to be latched into the DAC.

As mentioned in the last paragraph, the DR pulse is also used as the reset signal in the frame pulse circuit. The frame pulse is used as the master reset pulse to synchronise the action of the unit to the start pulse of word 1 in each frame. To generate this pulse the digital data from switch 2 and the pulse shaping circuit is clocked into a 12 stage shift register. Here the output from each stage is connected to a diode of a 13 input AND gate (D1-D12,D18). Inspection of fig1a show that each 11 bit word must contain at least one bit at level '0'. Therefore it is only 12 clock bits after the last word in the frame that the AND gate output can go positive. After amplification and inversion by IC1d and IC1d this frame pulse resets the word strobe counters, IC9 and IC10, and the UART, IC2. The AND gate output will remain positive and holding the circuit in a reset state until the start pulse of the first word of the next frame. Diode 17 will become forward biassed and the AND gate output will go low which after amplification and inversion by IC1c will provide the positive going edge to clock the monostable IC16. The inverted output will go low and being connected to the AND gate input via diode d18 will hold the AND gate output low for the duration of the 'on' time of IC16. The pulse width is controlled by the values of C21 and the variable resister VR2 which is adjusted to provide a pulse length approximately the length of time taken up by the data words in the frame. At the end of this pulse the AND gate will then produce a pulse on completion of 12 consecutive high level bits after the last word and the cycle is repeated. Without the pulse from IC16 to hold the AND gate off it would be possible to produce a spurious reset pulse during the period when data words are being received. This could occur with a data word containing a sufficient number of high level bits plus the interword time, which is always at a high level, is of sufficient length to equal the 12 bits of the AND gate.

For timing purposes a crystal controlled baud rate generator, IC4, is used to produce clock pulses at 153.6Khz. i.e. 16 times the baud rate.

The word strobe section of the circuit uses two cascaded decade counters, IC9 and IC10, to count the DR flag pulses and provide discrete word pulses at each counter stage output. The counters are reset to the start of word 1 by the frame pulse therefore word 1 strobe will always be on the 1 output of the counter and the pressure strobes on 2 and 3 outputs, temperature on 4 and 5 etc. Note also that word strobes in excess of 10 will not only use the same outputs as the unit strobes but provide a discrete output in the decade counter IC10.

Using a 2 input OR gate, unit strobes 2 and 4 are combined to form one input of a 2 input AND gate IC11a. The second input of this device is connected to the 0 output of the decade word counter IC10. This ensures that the logical outputs from the AND gate are only the unit word strobes 2 and 4, which are the least significant words (LSW) of the pressure and temperature respectively, and will not include those strobes from words 12 and 14. The LSW strobes are differentiated using R10 and C5 and the positive going pulses amplified and inverted by IC12a to give a 5 volt negative going leading edge pulse of approximately 47 microseconds in duration. These pulses are then connected to the A0 input of the DAC IC3 to latch the four most significant bits of the LSW of pressure and temperature data to the four least significant bits of the DAC input buffer.

The strobes to latch the MSW of pressure and temperature into the DAC are derived in an identical manner using the diodes D15 and D16 for the OR gate, IC11b for the AND gate, R11 and C6 for the differentiation and IC12b for the amplification and inversion.

The A3 input of the DAC shifts the 12 bit parallel data into the main latch and initiates the conversion sequence to produce the analogue output. The configuration of the DAC is set up to provide a 0 to +10 volt unipolar output using the internal 10.00 volt zener as the reference voltage source. Gain adjustment is fairly straight forward by setting the 12 input bits to a logical 1 and adjusting the output voltage to 9.9976 volts with potentiometer VR1.

The output from the DAC contains both the pressure and temperature signals and to separate these a further set of strobes are produced. Both sample pulses are produced using similar circuitry , the only difference being the signal sources. For the pressure circuit the input is the pressure MSW pulse A3 from IC9 and for the temperature it is the temperature MSW pulse A5 also from IC9. The pressure strobe is generated using the AND gate IC11c to select word strobe 3, the differentiation circuit R12 and C7, the amplifier and inverter IC12c, the integration circuit R14 and C9 and finally the inverter amplifier IC12c. The resulting active sampling edge occurs approximately 90 microseconds after the DAC has completed the conversion. This strobe is then used by the sample and hold integrated circuit IC13 to sample the pressure analogue signal at the output of the DAC. The pressure analogue signal voltage is then held by the sample and hold integrated circuit until the completion of the next pressure word in the next frame when it will again be updated. As mentioned earlier, the temperature sample and hold pulse is similarly produced but this time using IC11d, IC12d, IC12f associated components and the sample and hold circuit of IC14.

4. DEPLOYMENT.

This unit has already given satisfactory operational service using the 1401 deck units to provide the depth signal for the IOSDL Seasoar control system.

TJPG'SSDAC'
9/1/91

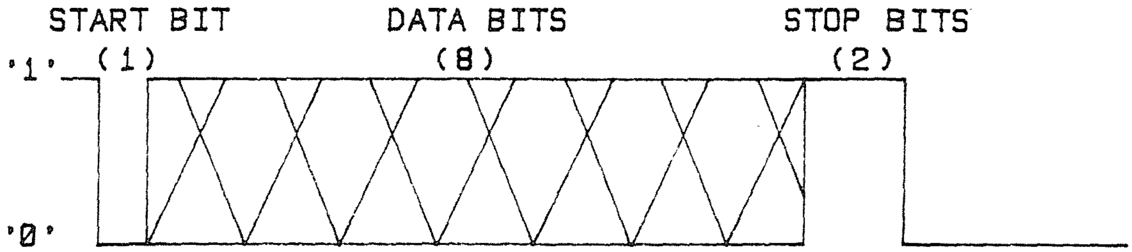

FIG 1A. 11 BIT WORD FORMAT (+VE LOGIC).

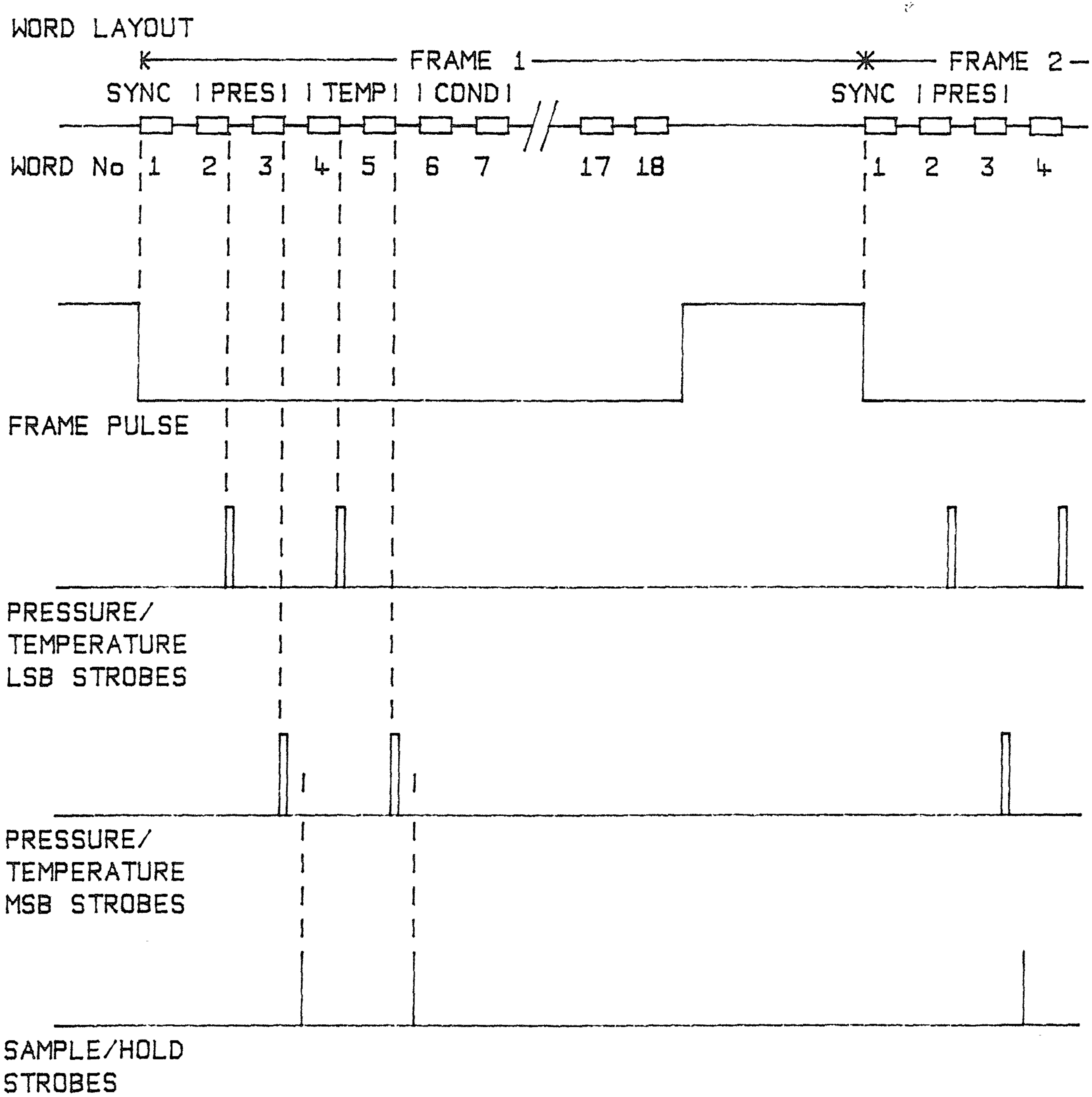

FIG.	1B.	CIRCUIT WAVEFORMS	DRAWN	J.SMITHERS
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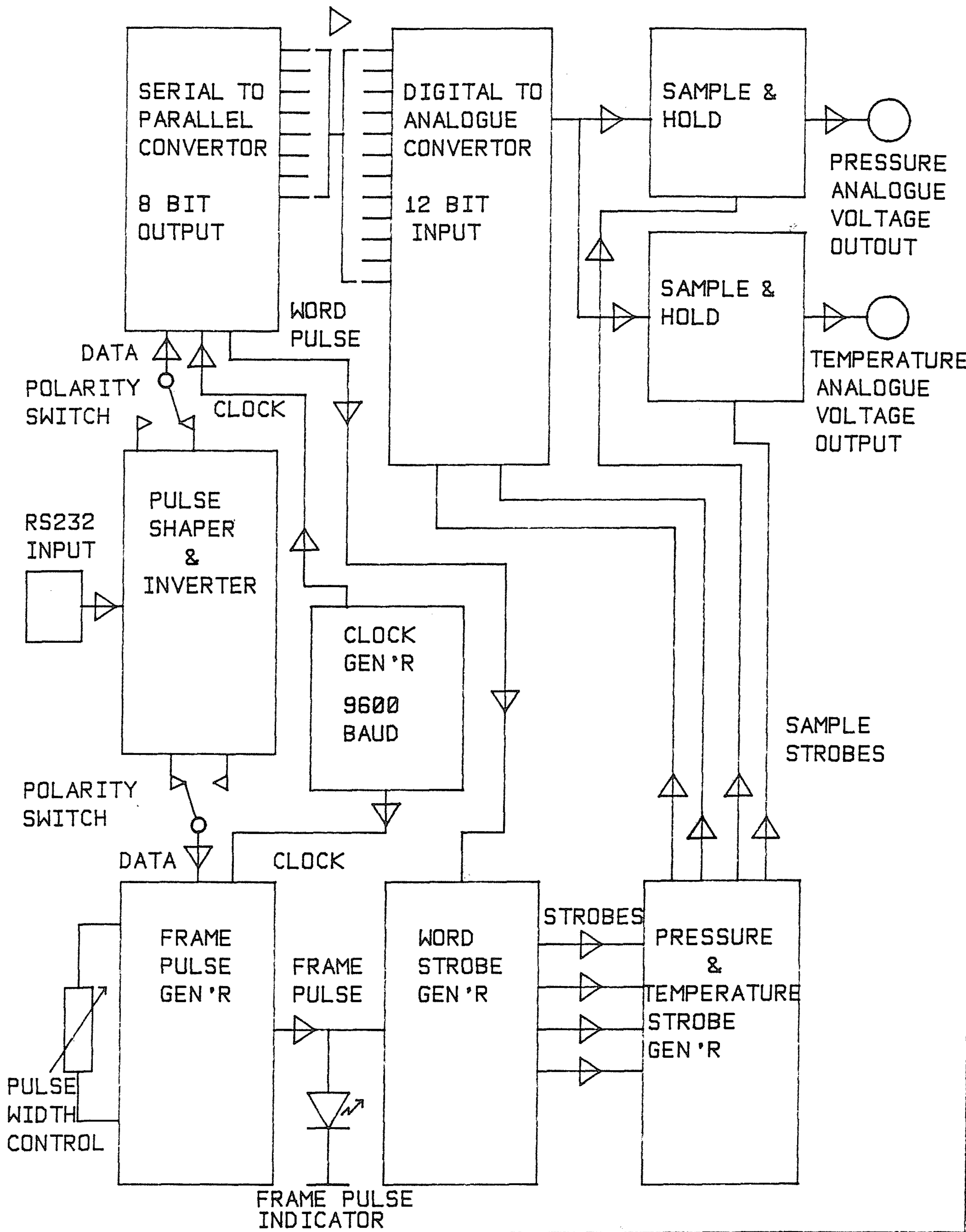

FIG.	2.	BLOCK SCHEMATIC SEASOAR PRESSURE DAC.	DRAWN	J.SMITHERS
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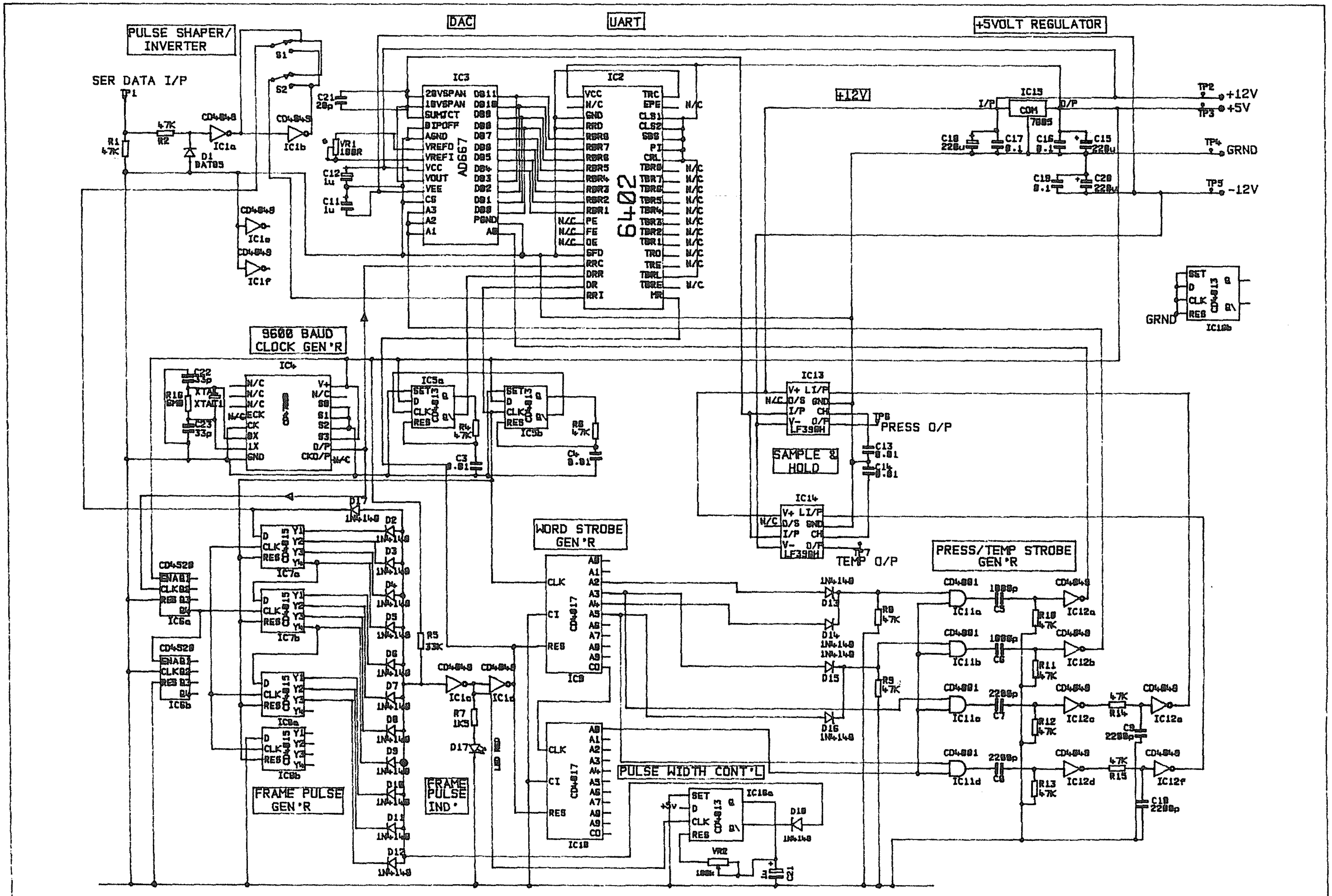

DRAWN	J.SMITHERS
DATE	07-01-91

SEASOAR BOARDS PRESSURE/TEMPERATURE D/A

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CCT DIA SYMBOL	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES & REMARKS
	NAME	VALUE	RATING	TYPE	SUPPLIERS NAME	REF No.	
R1	RESISTOR	47K	0.4W	METAL FILM MR25	IOSDL STORES		
R2	' '	47K	' '	' '	' '		
R3	–	–	–	–	–	–	M&D NOT USED
R4	RESISTOR	47K	0.4W	METAL FILM MR25	IOSDL STORES		
R5	' '	33K	' '	' '	' '		
R6	' '	47K	' '	' '	' '		
R7	' '	1K5	' '	' '	' '		
R8	' '	47K	' '	' '	' '		
R9	' '	47K	' '	' '	' '		
R10	' '	47K	' '	' '	' '		
R11	' '	47K	' '	' '	' '		
R12	' '	47K	' '	' '	' '		
R13	' '	47K	' '	' '	' '		
R14	' '	47K	' '	' '	' '		
R15	' '	47K	' '	' '	' '		

SEASOAR BOARD 5 PRESSURE/TEMPERATURE D/A.

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COMPILED DRAWN	P.GWILLIAM J.SMITHERS	DATE	03-01-91
ISSUE	1	SHEET	1 OF 5

CCT DIA SYMBOL	ELECTRONICS COMPONENT DESCRIPTION NAME	VALUE	RATING	TYPE	IDENTIFICATION SUPPLIERS NAME	REF No.	ALTERNATIVES & REMARKS
C1/C2	CAPACITOR						M&D NOT USED
C3	' '	.01uF		POLYESTER	IOSDL STORES		
C4	' '	.01uF		POLYESTER	' '		
C5	' '	1nF		CERAMIC	STC/IOSDL STORES		
C6	' '	1nF		CERAMIC	' '		
C7	' '	2.2nF		CERAMIC	' '		
C8	' '	2.2nF		CERAMIC	' '		
C9	' '	2.2nF		CERAMIC	' '		
C10	' '	2.2nF		CERAMIC	' '		
C11	' '	1uF		ELECTRO'	IOSDL STORES		
C12	' '	1uF		ELECTRO'	' '		
C13	' '	.01uF		POLYESTER	' '		
C14	' '	.01uF		POLYESTER	' '		
C15	' '	220uF		ELECTRO'	' '		
C16	' '	0.1uF		CERAMIC	STC/IOSDL STORES		

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CCT DIA SYMBOL	ELECTRONICS COMPONENT DESCRIPTION NAME	VALUE	RATING	TYPE	IDENTIFICATION SUPPLIERS NAME	REF No.	ALTERNATIVES & REMARKS
C17	CAPACITOR	0.1uF		CERAMIC	IOSDL STORES		
C18	' '	220uF		ELECTRO'	' '		
C19	' '	0.1uF		CERAMIC	' '		
C20	' '	220uF		ELECTRO'	' '		
C21	' '	20pF		SIL MICA	' '		
C22	' '	1uF		ELECTRO'	' '		
VR1	POT'R	100R		PCB PRESET	' '		
VR2	POT'R	100K		PCB PRESET	' '		
IC1	INTEGRATED CIRCUIT	CD4049B		16 PIN DIL	IOSDL STORES		6 STAGE INV CMOS
IC2	' '	6402		40 PIN DIL	RS COMPS	309-284	UART
IC3	' '	AD667JN		28 PIN DIL	RS COMPS	632-972	12 BIT DAC
IC4	' '	4702B		16 PIN DIL	RS COMPS	305-517	BAUD RATE GEN'R
IC5	' '	4013B		14 PIN DIL	IOSDL STORES		DUAL 4 STAGE SR

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CCT DIA	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES
SYMBOL	NAME	VALUE	RATING	TYPE	SUPPLIERS NAME	REF No.	& REMARKS
IC6	INTEGRATED CIRCUIT	CD4520B		16 PIN DIL	IOSDL STORES		DUAL BIN COUNTER
IC7	ʼʼ	CD4015B		16 PIN DIL	ʼʼ		DUAL 4 STAGE SR
IC8	ʼʼ	CD4015B		16 PIN DIL	ʼʼ		DUAL 4 STAGE SR
IC9	ʼʼ	CD4017B		16 PIN DIL	ʼʼ		DECADE COUNTER
IC10	ʼʼ	CD4017B		16 PIN DIL	ʼʼ		DECADE COUNTER
IC11	ʼʼ	CD4081B		14 PIN DIL	ʼʼ		QUAD AND GATE
IC12	ʼʼ	CD4049B		16 PIN DIL	ʼʼ		6 STAGE INV CMOS
IC13	ʼʼ	LF398H		TO99 8PIN	RS COMPS	307-086	SAMPLE/HOLD AMP
IC14	ʼʼ	LF398H		TO99 8PIN	RS COMPS	307-086	SAMPLE/HOLD AMP
IC15	ʼʼ	7805		T220 3PIN	IOSDL STORES		+5V REGULATOR
IC16	ʼʼ	CD4013B		14 PIN DIL	ʼʼ		DUAL D TYPE FF
D1	DIODE	BAT85		SIL SIGNAL	RS COMPS	300-975	SCHOTTKY BARRIER DIODE
D2-D16 D18	DIODE	1N4148		SILICON GP	IOSDL STORES		
D17	LED	2mA		RED 3mm	RS COMPS	588-386	MIN LOW CURRENT LED

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CCT DIA	ELECTRONICS COMPONENT DESCRIPTION				IDENTIFICATION		ALTERNATIVES
SYMBOL	NAME	VALUE	RATING	TYPE	SUPPLIERS NAME	REF No.	& REMARKS
S1	SWITCH			SPDT VERT PCB	RS COMPS	334-224	PCB MOUNTING
S2	SWITCH			,,	RS COMPS	334-224	PCB MOUNTING

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