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UNIVERSITY OF SOUTHAMPTON

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PNP POLYSILICON EMITTER BIPOLAR TRANSISTORS

by

Ian R.C. Post

A thesis submitted for the degree of
Doctor of Philosophy

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ABSTRACT

FACULTY OF ENGINEERING AND APPLIED SCIENCE

DEPARTMENT OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

PNP Polysilicon Emitter Bipolar Transistors

by Ian R.C. Post

This thesis reports on an experimental and theoretical investigation of *pnp* polysilicon emitter bipolar transistors. The fabrication of transistors with shallow emitter junctions (<0.05μm) is described. Measurements of base current and emitter resistance are then made on devices both with and without a deliberately grown interfacial oxide layer at the polysilicon/silicon interface.

A simple electrical method of measuring the emitter/base junction depth in shallow bipolar devices is presented, based on the measured base sheet resistance with and without an emitter diffusion. Good agreement is achieved with analytical techniques, such as SIMS and spreading resistance, for deep emitter junctions (>0.1μm). However, the electrical method shows itself to be more accurate for shallow emitter junctions (<0.05μm). This method is a valuable characterisation tool, because it is only in shallow emitter devices that the full effect of the polysilicon/silicon interface on the base current is observed.

Investigations of boron diffusion in polysilicon and single-crystal silicon are undertaken, in an effort to characterise the necessary anneals required to produce shallow emitter junction *pnp* devices. It is shown that the enhancement of boron diffusivity in polysilicon, over that in single-crystal silicon, is only a factor of 50–220. This makes the attainment of shallow emitter *pnp* devices (<0.05μm) considerably more difficult than for typical arsenic doped *npn* devices, where the enhancement of diffusivity is typically 10^4. Further problems are also described, such as boron precipitation in the as-implanted peak, which limits the maximum boron concentration in the polysilicon to $1–2x10^{20}$ cm^{-3}, and a low solid solubility, which limits the maximum electrically active boron concentration in the emitter to around $1–2x10^{19}$ cm^{-3}.

Using the shallow emitter *pnp* devices described above, the role of a deliberately grown interfacial oxide layer on the base current and emitter resistance is studied. Effective oxide barrier heights are extracted for these devices, which yield asymmetrical values of 0.31±0.02 eV for holes and either 0.68±0.08 eV or 0.44±0.06 eV for electrons, depending on which band-gap narrowing model is used ('DAS' or 'Popp'). This same procedure is also carried out for *npn* devices with identical interfacial oxide treatments, which also yield asymmetrical values of >0.72 eV for holes and 0.40±0.01 eV for electrons. The barrier heights obtained from *pnp* transistors are therefore inconsistent with those obtained from *npn* transistors. A new heterojunction tunnelling model is proposed for the polysilicon emitter, in which the interfacial 'oxide' layer is treated as a wide band-gap semiconductor. Using this model, the inconsistency in the measured barrier heights, and their asymmetry, can both be fully explained. Band-bending due to segregated dopant at the interface is central to this explanation.

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Ian Post,
Southampton University,
13th January 1992.

To My Parents, Raymond and Dorothy Post

Table of Contents

Abstract ... i
Acknowledgements ... ii
Table of contents ... iii

Chapter 1 – Introduction ... 1
References ... 5

Chapter 2 – Polysilicon Emitters for Bipolar Transistors: A Review and Re-Evaluation of Theory and Experiment ... 7
2.1 Introduction ... 7
2.2 Review of current gain theories for polysilicon emitter transistors ... 7
2.3 Theory ... 12
2.3.1 Base current of a shallow emitter bipolar transistor ... 12
a) Metal contacted emitters ... 13
b) Polysilicon emitters ... 14
2.3.2 Recombination velocity model for polysilicon emitter bipolar transistors ... 15
a) Oxide tunnelling model ... 16
b) Pseudo-grain boundary mobility model ... 17
c) Segregation model ... 18
2.3.3 Extended emitter model ... 19
2.3.4 Parameter values and minority carrier hole models in heavily doped n–type silicon ... 19
2.4 Experimental results ... 20
2.4.1 Devices with interfacial oxides ... 20
a) Effect of an interface anneal ... 20
b) Temperature dependence of current gain ... 22
c) Emitter resistance ... 23
2.4.2 Devices without an interfacial oxide layer ... 26
a) Segregation of dopant to the interface ... 26
b) Hydrogen passivation ... 34
c) Polysilicon thinning ... 36
d) Temperature dependence of current gain ... 37
e) Effect of an interface anneal ... 39
2.5 Modelling a discontinuous interfacial oxide layer ... 40
2.6 Conclusions ... 42
References ... 44

Chapter 3 – Electrical Method for Measuring the Emitter Depth of Shallow Bipolar Transistors 47
3.1 Introduction 47
3.2 Theory 48
3.3 Accuracy 50
3.4 Experimental procedure 51
3.5 Results and Discussion 52
3.5.1 Emitter junction depth 52
3.5.2 Modelling of collector currents 56
3.6 Conclusions 60
References 61

Chapter 4 – Investigation of Boron Diffusion in Polysilicon and its Application to the Design of *pnp* Polysilicon Emitter Bipolar Transistors with Shallow Emitter Junctions 63
4.1 Introduction 63
4.2 Experimental procedure 64
4.3 Results 65
4.3.1 SIMS results 65
4.3.2 Spreading resistance results 68
4.3.3 Electrical results 70
4.4 Discussion 73
4.5 Conclusions 82
References 83

Chapter 5 – Analysis of the Role of the Interfacial Oxide in *pnp* and *npn* Polysilicon Emitter Transistors 86
5.1 Introduction 86
5.2 Experimental procedure 86
5.3 Theory 87
5.3.1 Effective recombination velocity and heavy doping parameters 87
5.3.2 Tunnelling currents and resistances 89
5.4 Electrical results 91
5.4.1 Base current 91
5.4.2 Emitter resistance 92
5.5 Discussion 95
5.5.1 Extraction of oxide barrier heights 95

5.5.2 A heterojunction tunnelling model 99
5.6 Conclusions 108
References 109

Chapter 6 – Conclusions and Further Work 112

Appendices 115

Appendix 1 Derivation of T_{block} expressions 115
Appendix 2 Standard *pnp* processing details 120
Appendix 3 Electrical measurements set-up 127
Appendix 4 Mask set details 129
Appendix 5 HQUPETS input files for generating barrier band diagrams 131
Appendix 6 Published papers resulting from the work in this thesis 133
Appendix 7 List of Symbols 134

'Errors using inadequate data are much less than those using no data at all'

Charles Babbage 1792–1871.

Chapter 1

Introduction

As the lateral dimensions of BiCMOS devices and circuits are scaled, the power supply voltage must also be similarly scaled in order to limit short-channel effects in the MOS transistors [1]. In conventional BiCMOS driver circuits this lowering of the supply voltage results in a large increase in gate delay [2], [3]. To combat this effect the use of vertical *pnp* transistors has recently been reported in so called complimentary BiCMOS driver circuits (CBiCMOS) [4], [5], which present a significant performance improvement over conventional BiCMOS circuits. This has lately fuelled interest in high performance vertical *pnp* polysilicon emitter bipolar transistors.

Lu *et al.* [6] and Warnock *et al.* [7] have recently reported the use of boron doped polysilicon for use as the emitters of bipolar transistors. Devices were produced without any deliberately grown oxide at the interface, and the polysilicon was doped by ion-implantation. This was followed by a furnace anneal at temperatures below 900°C, which was intended to uniformly dope the polysilicon and diffuse boron into the single-crystal silicon to produce shallow emitter junctions (~0.03–0.05μm). Modelling of the collector current of the resultant devices revealed that the band-gap narrowing and minority carrier mobility data of del Alamo *et al.* [8] provided a good fit to the measured collector current. The interfacial region of the polysilicon/silicon interface was characterised by a recombination velocity of 1.4×10^5 cm s^{-1} for minority carriers, and an emitter resistance of around 300 $\Omega\mu m^2$ for the majority carriers.

The vertical *pnp* polysilicon emitter transistors as analysed by Lu *et al.* [6] and Warnock *et al.* [7] have subsequently been employed in high-speed self-aligned processes [9]–[12] for use in complimentary bipolar circuits. Devices were produced with basewidths of 0.08μm, and a combination of furnace anneals at 800°C followed by rapid thermal anneals were used to produce shallow emitter depths of 0.02μm. Impressive high-frequency results were obtained for these *pnp* devices, namely a cut-off frequency, f_t of 27 GHz, a maximum oscillation frequency, f_{max} of 27 GHz, NTL gate delays of 36 ps, and ECL gate delays of 20 ps. This value of ECL gate delay was virtually the same as that obtained for a similar *npn* process. This somewhat surprising result can however, be explained by considering values of minority carrier mobility. At typical base doping concentrations of 10^{18} cm^{-3}, the minority carrier hole mobility is around 290 $cm^2V^{-1}s^{-1}$ [8], which is only marginally below the minority electron mobility value of 340 $cm^2V^{-1}s^{-1}$ [13]. This compares with a hole majority carrier mobility which is only half that of the majority carrier electron mobility for the same doping concentration. Moreover, the hole impact ionization rate is lower than that for electrons, which means that the collector doping in *pnp* devices can be raised above that for a corresponding *npn* device before junction break-down can compromise device performance. This increase in collector doping will suppress base push-out [14], enabling

the cut-off frequency to increase, which can be used to offset the reduced hole mobility. These results demonstrate that the intrinsic device limits for *pnp* transistors are quite comparable to those for corresponding *npn* devices.

As an alternative to doping the polysilicon by ion-implantation, Maritan and Tarr [15] have investigated the use of boron *in-situ* doped polysilicon. Devices were analysed with either a dip etch in HF prior to polysilicon deposition (designed to remove any oxide at the interface), or a chemical clean which was designed to grow a uniform oxide layer approximately 10–20Å thick. Firstly, 'true' polysilicon emitter transistors were studied which received no emitter anneal after polysilicon deposition, so that the emitter/base junction resided at the polysilicon/silicon interface. The resulting base current characteristics of these devices were very non-ideal, as well as both the collector and base currents saturating at low forward bias. However, the devices with a deliberately grown interfacial oxide layer exhibited a base current suppression by over a factor of 18 compared to the devices which received a dip etch in HF. This gain enhancement, was however, achieved at the expense of a large increase in emitter resistance, with the deliberately grown oxide layer producing a resistance of 2500 $\Omega\mu m^2$ compared to 800 $\Omega\mu m^2$ for devices without a deliberately grown interfacial layer.

Maritan and Tarr [15] also produced devices which received an anneal of 900°C for 30 minutes after polysilicon deposition. This anneal considerably improved the ideality of the base current and improved the high current handling capability, and reduced the emitter resistance to acceptable values of 100–200 $\Omega\mu m^2$ for devices either with or without an interfacial oxide layer. However, this improvement in device performance was at the expense of a large increase in emitter depth ($\geq$0.15μm), which resulted in the base current blocking of the devices with chemically grown interfacial oxide layers diminishing to a factor of 2.5 below that for the HF device. These results are also confirmed by Ratanaphanyarat *et al.* [16], who directly compared emitter layers either fabricated from boron *in-situ* doped polysilicon or from boron ion-implanted polysilicon, followed by an anneal at 850°C for 15 minutes in dry nitrogen. They found that the use of ion-implantation enabled a shallower emitter/base junction depth of 0.06μm to be produced, compared to a junction depth of 0.08μm for the *in-situ* doped layers.

Laser *et al.* [17] attempted to model the devices of Maritan and Tarr [15] with deliberately grown interfacial oxide layers by using the one-band oxide model [18]. This model follows from the theoretical work of O'Neill [19], who explained the asymmetry in hole and electron barrier heights (as derived from modelling *npn* polysilicon emitter transistors [20]) as being due to tunnelling via states which are derived from the conduction band-edge. The hole barrier height is therefore assumed to be larger than the electron barrier height by an amount equal to the silicon band-gap.

Laser *et al.* [17] were unable to model the emitter resistance of these devices using the one-band oxide model, and had to artificially reduce the oxide thickness (equivalent to reducing the hole barrier height) in order to do so. Similarly, the modelled value of base current was a factor of 3 larger than the experimentally measured value. These results clearly contradict with the one-band oxide model, suggesting that the hole and electron barrier heights as derived from *npn* polysilicon emitter transistors are not applicable to *pnp* polysilicon emitter transistors.

The above results indicate that excellent high-frequency performance can be produced from *pnp* polysilicon emitter transistors, although they highlight two important areas where more work is required. Firstly, there are considerable problems in fabricating devices with shallow emitter junctions. Generally, for arsenic doped polysilicon emitter transistors, a wide range of anneals can be used to fabricate reproducible shallow emitter junctions [21]. However, this is much more difficult in *pnp* polysilicon emitter transistors. Both Lu *et al.* [6] and Warnock *et al.* [7] had to resort to a complicated combination of low temperature furnace anneals (800–880°C) and rapid thermal anneal to produce shallow emitter junctions. Furthermore, the *in-situ* doped polysilicon emitter transistors of Maritan and Tarr [15] had emitter junction depths of 0.15μm, which are too deep to exploit the gain enhancements due to blocking at the polysilicon/silicon interface.

Secondly, there exists much doubt about the precise physical mechanisms which control the base current of *pnp* polysilicon emitter transistors, especially for those with deliberately grown interfacial oxide layers. In *npn* polysilicon emitter transistors hole barrier heights of 1.1 eV and electron barrier heights of 0.4 eV have been extracted from the measured values of base current and emitter resistance [20]. However, Laser *et al.* [17] have shown that by using these barrier heights, they were unable to simultaneously model the base current and emitter resistance of *pnp* polysilicon emitter transistors. The work in this thesis has therefore been undertaken to address mainly these two problems, and is organised as follows:

Chapter 2 contains a critical review of the theories presented in the literature to explain the current gain enhancement of *npn* polysilicon emitter transistors. From these theories a simple analytical form is chosen which is then applied to a selection of experimental data from the literature, in an effort to identify the dominant current gain mechanisms as a function of fabrication conditions.

Chapter 3 outlines a simple electrical method for measuring the vertical base/collector and emitter/base junction depths of bipolar transistors, which are important parameters in characterising the electrical performance of devices. The electrical method is then validated by modelling the collector current from a selection of *npn* and *pnp* transistors.

Chapter 4 investigates the diffusion properties of boron in polysilicon through the use of SIMS and SUPREM modelling, in an effort to characterise the necessary fabrication conditions to produce shallow emitter junctions.

Chapter 5 reports on the effects of a deliberately grown interfacial oxide layer on the base current and emitter resistance of *pnp* devices. Electron and hole barrier heights are extracted for these devices, and compared with barrier heights from *npn* devices with identical interfacial layer treatments. A methodology is then described to explain the experimental observations. Finally conclusions are drawn, and suggestions for further work made, in chapter 6.

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Chapter 2

Polysilicon Emitters for Bipolar Transistors: A Review and Re-Evaluation of Theory and Experiment

2.1 Introduction

In this chapter a critical review is presented of the theories proposed in the literature to explain the current gain enhancement of *npn* polysilicon emitter bipolar transistors. From these theories a simplified analytical formulation is chosen which models the blocking properties of the interface, including tunnelling through the interfacial oxide layer, reduced minority carrier mobility at the disordered interface, and the potential barrier created by segregated dopant, which can all give rise to an enhanced current gain. Also modelled are mechanisms which limit the extent of any gain enhancement, such as recombination in the single-crystal emitter, in the bulk polysilicon, and at the polysilicon/silicon interface. This model is then applied to a selection of experimental data in an effort to identify the dominant current gain mechanisms in polysilicon emitter transistors, as a function of a given set of fabrication conditions.

2.2 Review of current gain theories for polysilicon emitter transistors

The first reported use of polysilicon as an emitter contact to a bipolar transistor was by Takagi *et al.* [1] in 1972. The deposited polysilicon was *in-situ* doped, and was primarily used as a diffusion source for fabricating shallow emitter junctions. No mention was made of any gain enhancement of the transistors when compared to conventional metal contacted transistors.

Graul *et al.* [2] were the first to report a gain enhancement attributed directly to the inclusion of a polysilicon layer used to contact the emitter. They first deposited undoped polysilicon, which was then implanted with arsenic, followed by a high temperature drive-in. This was designed to uniformly dope the polysilicon, and also to diffuse arsenic into the single-crystal silicon to form a shallow emitter junction. The measured gain of the polysilicon emitter transistors were a factor of 5 larger than conventional metal contacted transistors. Moreover, the temperature dependence of the current gain was less sensitive to temperature for the polysilicon emitter transistors, than for the metal contacted transistors. Since the main source of a temperature dependence of current gain is the difference in band-gap narrowing between the emitter and base, Graul *et al.* [2] postulated that the temperature dependence was due to the band-gap narrowing in the polysilicon emitter being lower than that in the emitter of a conventional implanted transistor.

De Graaff and de Groot [3] fabricated conventional transistors up to and including the base fabrication. After the emitter windows were opened, a deliberately grown interfacial oxide layer of thickness between 20–60Å was grown. Phosphorus *in-situ* doped polysilicon was then deposited by LPCVD, followed by a high temperature

drive-in, which was used to activate the dopant in the polysilicon, and to form a shallow single-crystal emitter. Analysis of the base current showed that the incorporation of the interfacial oxide layer resulted in a suppression of the base current by a factor of around 10, although the base current became highly non-ideal. This reduction was explained by assuming that the injected minority carriers in the emitter are forced to tunnel through the interfacial oxide layer (see fig. 2.1), thereby impeding minority carrier flow. Similarly the majority carriers (which form the emitter current) also have to tunnel through the oxide (fig. 2.1), which can limit the maximum current carrying capability of the device. Furthermore, de Graaff and de Groot [3] estimated the tunnelling probability of holes to be 2–3 orders of magnitude lower than the tunnelling probability for electrons.

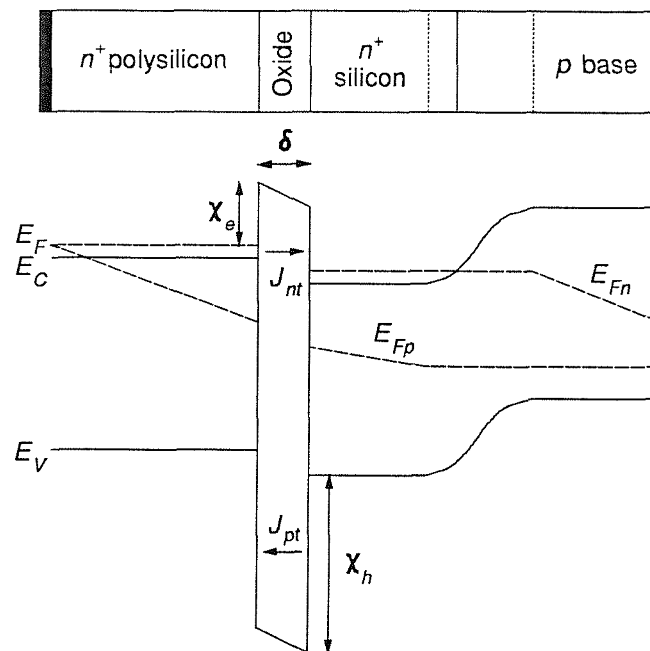

Fig. 2.1 Band diagram of the emitter/base structure of a polysilicon emitter transistor with an oxide layer at the polysilicon/silicon interface.

Ning and Isaac [4] fabricated transistors with conventional implanted emitters and then deposited arsenic *in-situ* doped polysilicon by LPCVD. They compared these transistors with conventional metal contacted devices, which ensured that any difference in base current could be attributed directly as a result of the emitter contact. The base current of the polysilicon contacted device was suppressed by a factor of 2 when compared to the metal contacted emitter. This increase in current gain was attributed to a lower minority carrier mobility in the polysilicon, when compared to single-crystal silicon. Solution of the current continuity and transport equations yields a minority carrier concentration which has a reduced gradient in the single-crystal emitter of the

polysilicon contacted device, compared to the metal contacted device (see fig. 2.2). Since the base current is directly proportional to the gradient of the minority carrier concentration at the edge of the emitter/base depletion region, the polysilicon contacted device will therefore have a reduced base current. This two-region model seems reasonable, if a little simplified, in that it would be expected that the amorphous nature of grain boundaries would enhance carrier scattering, and so the mobility in polysilicon, as a whole, would be less than single crystal silicon, doped to the same concentration.

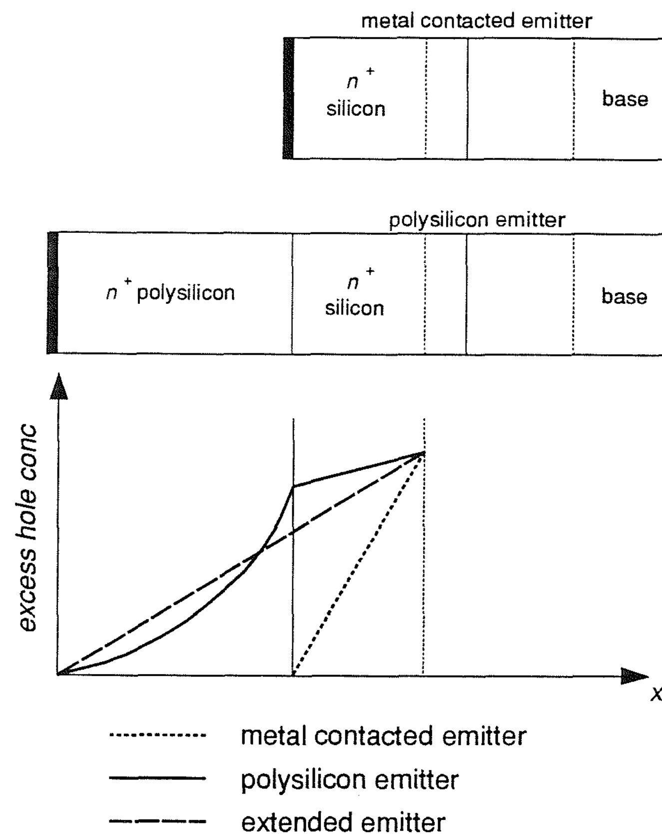

Fig. 2.2 Minority hole concentration in the emitter for a metal contacted emitter transistor, an extended emitter transistor, and a polysilicon emitter transistor.

Also shown in fig. 2.2 is the minority carrier distribution of an extended emitter device, in which the n^+ polysilicon is replaced by single-crystal silicon. This can arise in practice if complete epitaxial re-growth is induced during the emitter drive-in [5], [6]. It has many of the advantages of a polysilicon emitter, such as a shallow emitter/base junction, but the current gain is unaffected by the interface, and hence it behaves like a conventional bipolar transistor. For the purposes of this chapter this is a useful structure to consider, since a comparison of the gain of a polysilicon emitter, with that of an identical extended emitter, gives a measure of the gain enhancement or reduction resulting from the presence of the polysilicon/silicon interface.

Analysis of the microscopic structure of polysilicon reveals that it consists of crystalline regions (grains) separated by highly disordered amorphous regions (grain boundaries). Eltoukhy and Roulston [7], [8] have proposed theories which model the effects on minority carrier transport by individual grain boundaries. The grain boundaries are assumed to be infinitely thin, and characterised by a large concentration of interface states. The grain boundaries can affect minority carrier transport in two ways. Firstly, if the density of interface states are large enough ($>10^{14}$ cm^{-2}) then they will act as efficient recombination centres, and the model will predict no improvement in current gain over that for a metal contacted emitter. For low densities of interface states ($\leq 10^{12}$ cm^{-2}) recombination at the grain boundaries becomes negligible, and the minority carrier transport is dominated by scattering from the disordered region around the grain boundaries. This has the overall effect of lowering the minority carrier mobility in the polysilicon layer, and therefore reducing the base current. Eltoukhy and Roulston [7], [8] model the tunnelling through the interfacial layer in an analogous fashion to Stratton [9], and also analyse the effect that the interfacial layer has on the majority electron current by calculating the voltage drop across the interfacial oxide layer.

Yu *et al.* [10] have also proposed a unified tunnelling and transport model, and introduce the concept of an effective recombination velocity, which is a useful parameter for characterising the effects of various emitter contact technologies on the injected minority carrier concentration. The modelling of the grain boundaries is handled in a different way to that of Eltoukhy and Roulston [7], [8], in that they assume that the grain boundary has a finite thickness, in which the mobility of minority carriers is reduced, compared to that in the bulk of the grain. Recombination is assumed to occur only at the interface between the grain and grain boundary, but not actually in the grain boundary. Furthermore, recombination at the polysilicon/silicon interface is also modelled. Depending on whether the mobility degradation in the grain boundary, or the recombination at the grain/grain boundary interface dominates, the model will predict either a decrease or no improvement of base current, when compared to a device with a conventional metal contacted emitter.

An alternative explanation for the current gain enhancement in polysilicon emitter transistors has been proposed by Ng and Yang [11]–[13] to explain the observation that the current gain of polysilicon emitter transistors is dependent upon the amount of arsenic which segregates to the interface [14], [15]. Typically the concentration of arsenic at the polysilicon/silicon interface can be a factor of two or three larger than the concentration of arsenic in the bulk of the grains. Ng and Yang argued that if the segregated arsenic is electrically active then this could form a low-high-low barrier (see fig. 2.3). Typically the doping concentration changes so rapidly at the interface (greater than kT in a distance comparable to the mean free path) that the usual

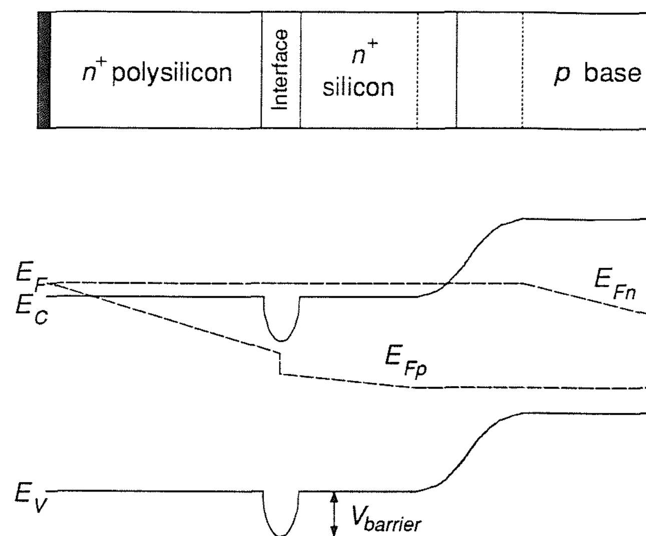

Fig. 2.3 Band-diagram of polysilicon emitter with electrically active dopant segregation barrier at the polysilicon/silicon interface.

drift-diffusion theory for carrier transport is no longer valid, and thermionic emission has to be invoked. The resulting model can therefore explain the increase of gain of a polysilicon emitter transistor with segregated arsenic at the interface, as well as the reduced temperature dependence of the current gain, although the model does not predict any increase in emitter resistance.

The main assumption of the thermionic emission theory is that the segregated arsenic remains electrically active, for which there has been no direct experimental evidence, although Wong *et al.* [16] have argued indirectly that the segregated arsenic could be electrically active. Furthermore, rigourous analysis of the theory by Wolstenholme [17] indicates that the base current is proportional to the ratio of the *effective* doping densities in the polysilicon and at the interface, which includes the effects of band-gap narrowing. Since effective doping concentration tends to saturate to a constant value as the electrically active doping concentration increases [18], then this implies that the segregation barrier will be smaller than predicted in [11]–[13]. The analysis in this chapter will use both the original theory as proposed by Ng and Yang [11]–[13] (i.e. with no band-gap narrowing), and the extended theory as developed by Wolstenholme [17] (i.e. including the effects of band-gap narrowing).

The model to be used in this chapter (and described in detail in the next section) follows from that of Yu *et al.* [10], extended to include the thermionic emission barrier due to dopant segregation [17]. TEM evidence of the polysilicon suggests that the layer consists of columnar grains, and so the polysilicon will be assumed to consist of only one crystalline grain.

2.3 Theory

2.3.1 Base current of a shallow emitter bipolar transistor

The injection and recombination of minority carriers in the emitter of a bipolar transistor play a crucial role in determining device behaviour. Of particular importance to the polysilicon contacted emitter transistor is the limiting effect on the current gain by recombination in the heavily doped single-crystal emitter. It is therefore important to evaluate and model these effects. It is easier to analyse the emitter of a bipolar transistor in terms of the effective recombination velocity, S_p at the emitter contact. This is defined as,

$$J_p(W_E) = qS_p p(W_E) \tag{2.1}$$

where $J_p(W_E)$ is the hole current density (for an *npn* device) at the emitter contact, and $p(W_E)$ is the excess hole concentration at the emitter contact. The numerical value of S_p can be used to define the recombination and blocking properties of the interface. For example, in a metal contacted emitter all the minority carriers are forced to recombine at the contact. Hence $p(W_E)$ is close to zero, and since $J_p(W_E)$ is finite, then S_p takes a large value (typically $\geq 10^6$ cm s^{-1}). If the metal contact is replaced by a thick interfacial oxide layer then $J_p(W_E) \rightarrow 0$ and so $S_p \approx 0$. For a typical polysilicon contact S_p will take an intermediate value between these two extremes.

For typical emitter depths <0.2μm and peak electrical emitter concentrations $\leq 10^{20}$ cm^{-3}, then an analytical expression can be derived [19] which expresses the base saturation current density, J_{BO} as a function of the emitter contact effective recombination velocity, S_p and the recombination parameters in the emitter,

$$J_{BO} = \frac{qn_{io}^2}{G_{eff}(W_E) + N_{Eeff}(W_E)/S_p}\left[1 + \int_0^{W_E} \frac{G_{eff}(W_E) - G_{eff}(x)}{\tau_p(x)N_{Eeff}(x)}dx + \frac{N_{Eeff}(W_E)}{S_p}\int_0^{W_E}\frac{dx}{\tau_p(x)N_{Eeff}(x)}\right] \tag{2.2}$$

where τ_p is the hole lifetime in the emitter, S_p is the effective recombination velocity at the emitter contact, and x=0 is defined as the edge of the emitter/base depletion region and $x=W_E$ is the position of the polysilicon/silicon interface. $G_{eff}(x)$ is the effective emitter Gummel number, and is defined as,

$$G_{eff}(x) = \int_0^x \frac{N_{Eeff}(x)}{D_p(x)} dx \tag{2.3}$$

$N_{Eeff}(x)$ is the '*effective*' doping concentration in the emitter and is used to model heavy doping effects. It is defined by,

$$N_{Eeff}(x) = N_E(x) \exp\left(\frac{-\Delta E_g^{app}(x)}{kT}\right) \tag{2.4}$$

where $N_E(x)$ is the electrically active doping profile in the emitter, and $\Delta E_g^{app}(x)$ is the '*apparent*' or '*device*' band-gap narrowing in the emitter.

The first term in equation 2.2 is identical to that obtained by Shibib *et al.* [20] for transparent emitters (i.e. no recombination in the bulk of the emitter). The last two terms in brackets model the effect on the base current by recombination in the bulk emitter, although, for the vast majority of devices analysed in this chapter, recombination in the bulk emitter is negligible. The only notable exception to this is for devices with thick interfacial oxide layers. The three terms in equation 2.2 are illustrated in fig. 2.4 as a function of S_p, where it can be seen that equation 2.2 can be simplified for certain specific emitter contact technologies, as discussed below. In order to calculate predicted values of base current to compare with reported experimental values in the literature, equation 2.2 is used together with measured emitter profiles, where available. In cases where the emitter profile is not given, a Gaussian profile is assumed in the single-crystal emitter, the Gaussian being constructed using estimates of the emitter/base junction depth and the doping concentration at the polysilicon/silicon interface.

a) Metal contacted emitters

As stated previously, metal contacted emitters are characterised by a large effective recombination velocity. In this case the last two terms in brackets from equation 2.2 can be ignored (see fig. 2.4). Also since $N_{Eeff}/S_p << G_{eff}(W_E)$ (S_p is large) then the base current of a shallow metal contacted emitter can be approximated to,

$$J_{BO} = \frac{q n_{io}^2}{\int_0^{W_E} N_{Eeff}(x)/D_p(x) dx} \qquad S_p \geq 10^6 \text{cm s}^{-1} \tag{2.5}$$

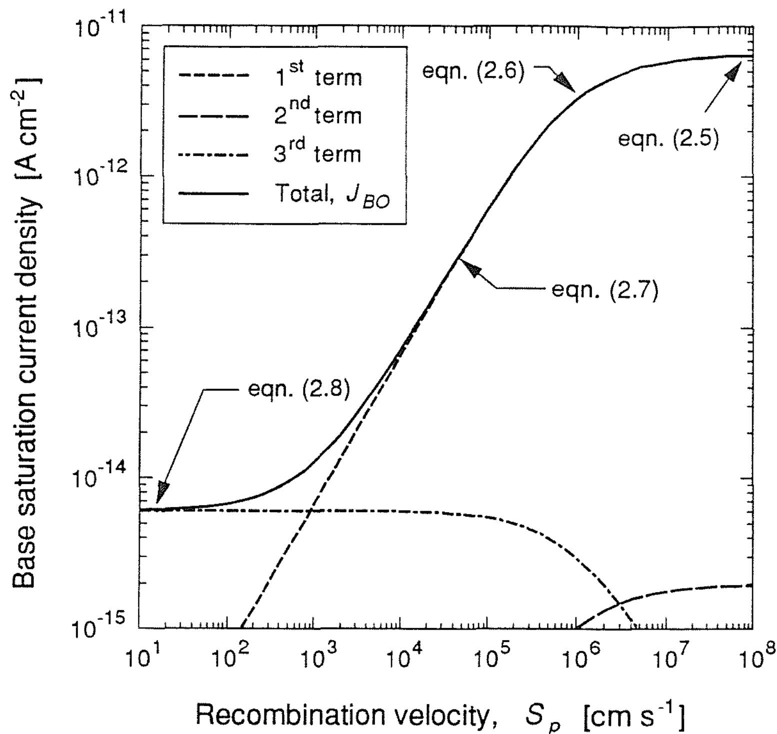

Fig. 2.4 Solution of equation 2.2 showing how the recombination velocity, S_p can be extracted from the measured base current, J_{BO}. Also shown are the simplifications that can be applied to equation 2.2 for certain ranges of S_p.

For this case recombination at the emitter contact is so large that the limiting factor is the supply of holes to the emitter contact. The base current is also proportional to the emitter depth, and so indicates that the base current will increase as the vertical dimensions of a metal contacted bipolar transistor are scaled.

b) Polysilicon emitters

If there is minimal blocking action of minority carriers at the polysilicon/silicon interface due to the 'break-up' of the interfacial layer, and/or a large density of recombination states exist at the interface, then typical values of effective recombination velocity, S_p are between 10^5 and 10^6 cm s^{-1}. In this case $N_{Eeff}/S_p \sim G_{eff}(W_E)$ and so equation 2.2 can be simplified to (see fig. 2.4),

$$J_{BO} = \frac{q n_{io}^2}{G_{eff}(W_E) + N_{Eeff}(W_E)/S_p} \qquad 10^5 < S_p < 10^6 \text{cm s}^{-1} \quad (2.6)$$

This is the intermediate case where the recombination at the contact is large enough so that again the supply of holes to the emitter contact is a limiting factor, although the effective recombination velocity is small enough to provide some blocking action.

If the interface provides some greater blocking action due to reduced grain boundary mobility and/or the presence of an interfacial oxide, then the polysilicon contact can be characterised by an intermediate value of effective recombination velocity. In this case $N_{Eeff}/S_p \gg G_{eff}(W_E)$ and so,

$$J_{BO} = \frac{q n_{io}^2 S_p}{N_{Eeff}(W_E)} \qquad 10^3 < S_p < 10^5 \text{cm s}^{-1} \quad (2.7)$$

The base current is still dominated by recombination at the emitter contact, but this time the dependence on emitter depth is lost (and hence the base current will remain constant as the emitter depth is scaled). In the extreme that S_p becomes very small (eg. for a device with a thick interfacial oxide layer) then the third term in brackets in equation 2.2 become prominent. In this limit equation 2.2 reduces to,

$$J_{BO} = \int_0^{W_E} \frac{q n_{io}^2}{L_p^2(x) N_{Eeff}(x)/D_p(x)} dx \qquad S_p \leq 10^2 \text{cm s}^{-1} (2.8)$$

The base current is now independent of the properties of the interface, and is completely dominated by recombination in the bulk of the emitter.

2.3.2 Recombination velocity model for polysilicon emitter bipolar transistors

The general model to be used in this study for a polysilicon emitter transistor is shown schematically in fig. 2.5. It is assumed that the polysilicon layer consists of only one crystalline grain separated from the monosilicon substrate by an interfacial

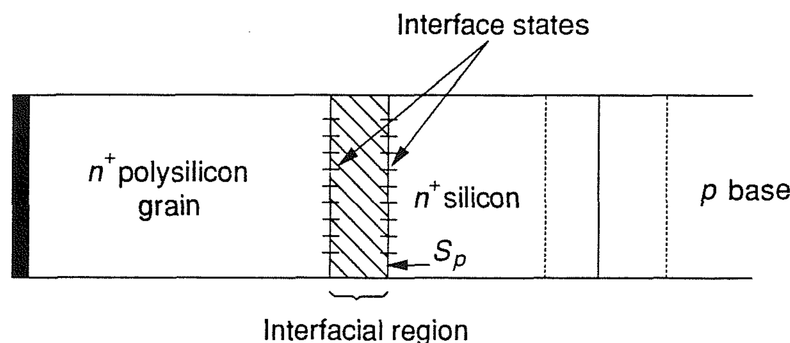

Fig. 2.5 Schematic diagram of a polysilicon emitter transistor.

region of finite thickness, which will be described in detail further on. A density of interface traps are also assumed to exist at the two interfaces between the interface region and the polysilicon grain and the monosilicon substrate.

The effective recombination velocity, S_p which characterises the polysilicon contact, can in general be expressed as [10],

$$S_p = S_I + \left[\frac{1}{T_{block}} + \frac{1}{S_I + S_g}\right]^{-1} \tag{2.9}$$

where S_I models the recombination of minority carriers via traps at the interface, and is given by,

$$S_I = \frac{1}{2} N_{it} c_p v_{th} \tag{2.10}$$

and N_{it} is the density of interface traps per unit area, c_p is the capture cross-section and v_{th} is the thermal velocity. The factor of 1/2 arises in equation 2.10, since it is assumed that the interface states are equally distributed between the left and right sides of the interface.

The parameter S_g describes the recombination of minority carriers in the bulk of the grain, and is given by [10],

$$S_g = a_g - \frac{b_g^2}{a_g + S_M} \tag{2.11}$$

where,

$$a_g = \frac{D_g}{L_g} \coth\left[\frac{W_p}{L_g}\right] \tag{2.12a}$$

$$b_g = \frac{D_g}{L_g} \operatorname{csch}\left[\frac{W_p}{L_g}\right] \tag{2.12b}$$

and D_g and L_g are the diffusivity and diffusion length of minority carriers in the grain respectively, S_M is the effective recombination velocity at the metal contact, and W_p is the polysilicon thickness.

Depending on the dominant carrier blocking mechanism, the value of T_{block} can take one of three values (see Appendix 1):

a) Oxide tunnelling model

If a deliberately grown interfacial oxide layer is present, then the dominating

blocking mechanism will be the tunnelling of minority carriers through the oxide. This model will be termed the *oxide tunnelling model*, in which the blocking recombination velocity, T_{block} can be expressed as [10],

$$T_{block} = T_{tun} = \frac{A_{hi}^{*}T^{2}}{qN_{v}} \cdot \frac{\exp(-b_{h})}{1 - c_{h}kT} \tag{2.13}$$

where,

$$b_{h} = \frac{4\pi\delta}{h}\sqrt{2m_{hi}^{*}\chi_{h}} \tag{2.14a}$$

$$c_{h} = \frac{2\pi\delta}{h}\sqrt{\frac{2m_{hi}^{*}}{\chi_{h}}} \tag{2.14b}$$

and χ_h is the barrier height to holes, m_{hi}^* is the effective mass of holes in the oxide, and δ is the oxide thickness. A_{hi}^* is the effective Richardson constant for holes in the oxide, and N_v is the effective density of states in the valence band, which are given by,

$$A_{hi}^{*} = \frac{4\pi q m_{hi}^{*}k^{2}}{h^{3}} \tag{2.15a}$$

$$N_{v} = 2\left[\frac{2\pi m_{v}^{*}kT}{h^{2}}\right]^{3/2} \tag{2.15b}$$

and m_v^* is the valence band effective density of states mass.

b) Pseudo-grain boundary mobility model

If no oxide is present at the interface, then the disordered nature of the interface can still block minority carrier injection. The interface can then be treated as a grain boundary of finite thickness, characterised by a reduction in carrier mobility. This model will be termed the *pseudo-grain boundary mobility model*, in which the blocking recombination velocity, T_{block} is given by,

$$T_{block} = T_{pgb} = \frac{kT}{q} \cdot \frac{\mu_{pgb}}{\Delta} \tag{2.16}$$

where Δ is the thickness of the pseudo-grain boundary, and μ_{pgb} is the minority carrier mobility in the pseudo-grain boundary. A value for Δ of 7Å [21] will be used throughout this chapter, which is consistent with the approximate thickness of a grain boundary in the bulk of the polysilicon. Typically, μ_{pgb} can be several orders of magnitude less than the hole mobility in single-crystal silicon [22]. It is also likely that the amorphous nature of the interface, and the presence of impurities, such as carbon, could result in an increase in band-gap, and so lead to the blocking of minority carriers. However, due to the large uncertainty of the precise physical properties of the interfacial region, this mechanism will not be considered in this chapter.

c) Segregation model

An alternative blocking mechanism has been proposed by Ng and Yang [11]–[13] for interfaces with no deliberately grown oxide. The model assumes that the segregated dopant at the interface is electrically active, and that the minority carriers are dominated by thermionic emission over this electrical barrier. This model will be termed the *segregation model*, in which the blocking recombination velocity, T_{block} is given by,

$$T_{block} = T_{th} = \frac{A_h^* T^2}{qN_v} \cdot \frac{N_E}{N_{Int}} \tag{2.17}$$

where N_E is the electrically active doping density in the emitter, and N_{Int} is the electrically active doping density of the segregated dopant at the interface, and N_v is the effective density states in the valence band. A_h^* is the effective Richardson constant for holes in silicon, which is expressed as,

$$A_h^* = \frac{4\pi q m_{hth}^* k^2}{h^3} \tag{2.18}$$

and m_{hth}^* is the effective mass of holes thermionically emitted over the segregation barrier. It has been pointed out by Wolstenholme [17] that the doping densities in equation 2.17 should strictly be effective doping densities, which include the effects of band-gap narrowing. For this mechanism to dominate the base current, the barrier created by the segregated dopant must be greater than about $2kT$. For a typical emitter doping concentration of 10^{20} cm^{-3}, this means that the segregated doping concentration must be greater than around $8\text{x}10^{20}$ cm^{-3} for the original Ng and Yang model [11]–[13], or greater than 10^{23}–10^{24} cm^{-3} for the extended model of Wolstenholme [17].

2.3.3 Extended emitter model

An important device structure that is useful for direct comparisons with the polysilicon emitter is that of the extended emitter. This device has the same emitter structure and doping profile as the polysilicon emitter device, but with no interface. In other words $T_{block}=\infty$ and $S_I=0$ in equation 2.9, so that $S_p=S_g$. The extended emitter can be used to clarify any blocking or recombination mechanisms at the interface. For example, if the base current of a polysilicon emitter is less than that of the identical extended emitter, then this is evidence of a blocking mechanism at the interface. Conversely, if the base current of the polysilicon emitter device is larger than that of an extended emitter device, then this is evidence of a recombination mechanism at the interface.

2.3.4 Parameter values and minority carrier hole models in heavily doped n-type silicon

Table 2.1 summarises the parameter values that will be used throughout this study, unless otherwise stated.

Parameter	Value	Reference
Hole effective mass in the interfacial oxide layer (m_{hi}^*)	$0.42m_o$	[8]
Hole effective mass for thermionic emission (m_{hte}^*)	$0.66m_o$	[23]
Valence band effective density of states mass (m_v^*)	$0.81m_o$	[24]
Interface trap capture cross-section x thermal velocity ($c_p v_{th}$)	$2x10^{-9}$ cm^3 s^{-1}	[25]
Grain boundary thickness (Δ)	7Å	[21]
Recombination velocity at metal contact (S_M)	10^6 cm s^{-1}	[10]

Table 2.1 Parameter values used in this study.

In order to obtain predictions of effective recombination velocity and base current from doping profiles, it is necessary to use empirically fitted values for the minority carrier recombination and transport parameters such as hole lifetime τ_p, hole mobility μ_p, and band-gap narrowing, ΔE_g^{app}. Values for these parameters, as a function of doping, will be taken from the work of del Alamo *et al.* [18],

$$\frac{1}{\tau_p} = (7.8\times10^{-13})N_E + (1.8\times10^{-31})N_E^2 \qquad \text{(s)} \quad (2.19a)$$

$$\mu_p = 130 + \frac{370}{1 + (N_E/8\times10^{17})^{1.25}} \qquad (\text{cm}^2\text{V}^{-1}\text{s}^{-1}) \quad (2.19b)$$

$$\Delta E_g^{app} = 18.7\times10^{-3}\ln\left(\frac{N_E}{7\times10^{17}}\right) \qquad \text{(eV)} \quad (2.19c)$$

Unfortunately, there is still much disagreement in the literature over the precise form equation 2.19 should take, mainly because minority carrier transport parameters are extremely difficult to measure. However, the parameter set above are consistent in that the measurements were performed simultaneously on the same silicon samples, and so these will be used throughout this chapter.

2.4 Experimental results

Over the past ten years or so, a considerable amount of experimental results on polysilicon emitter transistors have been published in the literature. In this section, approximately 8 or so key papers have been chosen which are representative of a broad cross-section of important experimental results. The results of these papers will be quoted in the form of raw experimental data (for example measured current densities and resistances etc.), and then any subsequent modeling will be performed using the simplified analytical equations outlined in section 2.3. This will allow a consistent comparison to be made between the predictions of the three blocking mechanisms and the reported experimental results.

2.4.1 Devices with interfacial oxides

a) Effect of an interface anneal

The analysis will begin by considering experimental results from devices with an interfacial oxide layer, which is generally grown using an oxidising chemical treatment. It has been well documented in the literature that such an interface treatment gives a significant improvement in the current gain. For example, Ashburn and Soerowirdjo [26] have shown that devices given an RCA clean prior to polysilicon deposition, had gains five times higher than those given an HF etch. A more detailed characterisation of the influence of the interfacial oxide on the current gain was carried out by Wolstenholme *et al.* [27]. In this experiment an interface anneal was carried out after polysilicon deposition, but prior to emitter implant, to thermally stress the interfacial

oxide. In this way, a range of interfacial oxide structures was obtained without significantly altering the emitter and base doping profiles. The results are shown in fig. 2.6 for devices given an RCA clean prior to polysilicon deposition. It is evident that a factor of 100 increase in base current is obtained as the temperature of the interface anneal is increased from 800 to 1100°C. These electrical results were correlated with high resolution TEM observations of the polysilicon/silicon interface which showed that an interfacial oxide was present, which broke up by increasing amounts as the interface anneal temperature was increased. For interface anneal temperatures of 900°C or below, the interfacial oxide was continuous and uniform, with a thickness of 14±2Å. In contrast, after an interface anneal at 950°C, a third of the interface had broken up, and the polysilicon had started to epitaxially align from the substrate, with these epitaxial regions extending typically 35Å into the polysilicon. An interface anneal at 1000°C lead to a further break-up of the interfacial oxide (70%, with epitaxial regions extending 40Å into the polysilicon), and an anneal at 1100°C produces an interface which consists entirely of oxide balls.

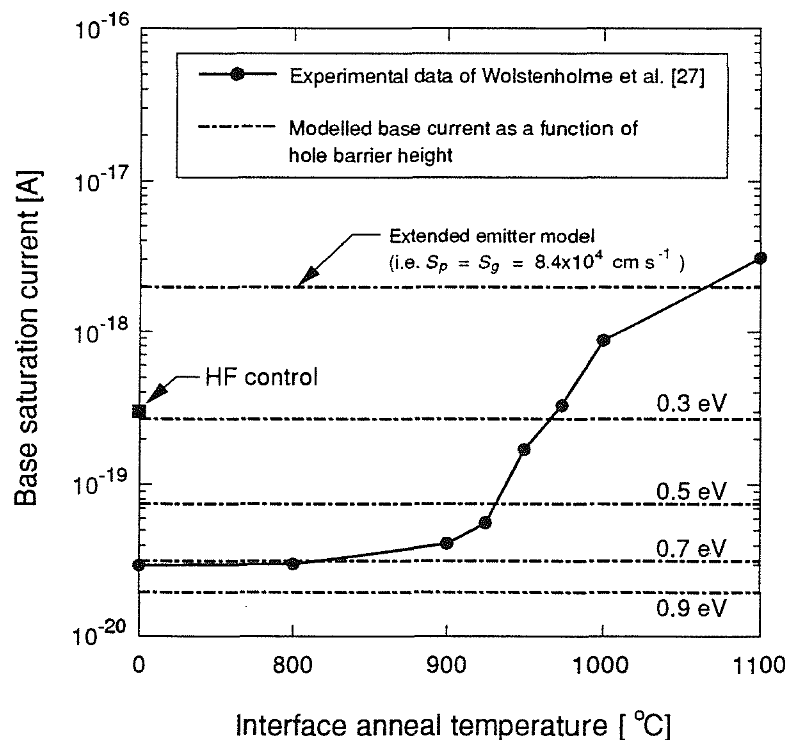

Fig. 2.6 Experimental data of Wolstenholme *et al.* [27] showing base saturation current as a function of interface anneal for devices with a deliberately grown interfacial oxide layer. The base current has been modelled by assuming that the dominant blocking mechanism is tunnelling through the interfacial oxide layer (i.e. *oxide tunnelling model* with δ=14Å, and S_I=0). Also shown is the modelled base current using the *extended emitter model* ($T_{block}=\infty$, and S_I=0).

Since interface anneals at 900°C and below produce a continuous interfacial oxide, it is possible to apply the *oxide tunnelling model* unambiguously to these results. Fig. 2.6 shows the modelled values of base current for different values of oxide barrier height, assuming that the devices are tunnelling-dominated (i.e. S_I=0 and T_{block}<<S_g). It is evident that these devices can be modelled by an oxide barrier height of 0.7 eV. It is probably more realistic to assume that some form of recombination via interface traps is also acting in parallel with the tunnelling, and if this is the case then the barrier height of 0.7 eV must increase in order that a fit to the measured base current is still obtained. An upper limit for the interface state density can be obtained by modeling the base current under the assumption that the device is dominated by recombination at the interface (i.e. $T_{block}\approx 0$). In this case, the control RCA device in fig. 2.6 can be modelled by an interface state density of 7.4×10^{11} cm^{-2}.

Also modelled in fig. 2.6 is the base current of an extended emitter device, in which no blocking or recombination at the interface is assumed to occur (i.e. $T_{block}=\infty$ and S_I=0). As can be seen, a reasonable fit to the 1100°C interface anneal device is achieved, which implies that the interface has no effect on the base current of this device. This conclusion is consistent with the TEM analysis, which showed that the interfacial oxide had completely 'balled-up', such that 97% of the interface was oxide-free. There was also a substantial amount of epitaxial re-growth of the polysilicon. These experimental results show that the interfacial oxide plays a dominant role in controlling the current gain of polysilicon emitter transistors with deliberately grown interfacial oxide layers. Recent work by Ronsheim *et al.* [28], using depth-resolved secondary ion mass spectroscopy, has quantified this process, and shown that there exists a direct correlation between the amount of oxygen at the interface (expressed as atoms/cm^2) and the base current of polysilicon emitter transistors.

Rutherford back scattering (RBS) analysis has been used by Wolstenholme [17] to investigate the distribution of arsenic at the interface for the devices reported in fig. 2.6. The results of this analysis are shown in fig. 2.7, and indicate that the concentration of arsenic at the polysilicon/silicon interface remains unchanged for interface anneals up to a temperature of 1000°C. This therefore completely rules out the *segregation model* as a possible mechanism for explaining the experimental results in fig. 2.6.

b) Temperature dependence of current gain

Further evidence supporting the *oxide tunnelling model* is obtained from measurements of the temperature dependence of the current gain. Several authors [2], [3], [26] have reported that polysilicon emitter transistors with a chemically grown interfacial oxide, have a gain which varies less strongly with temperature than observed

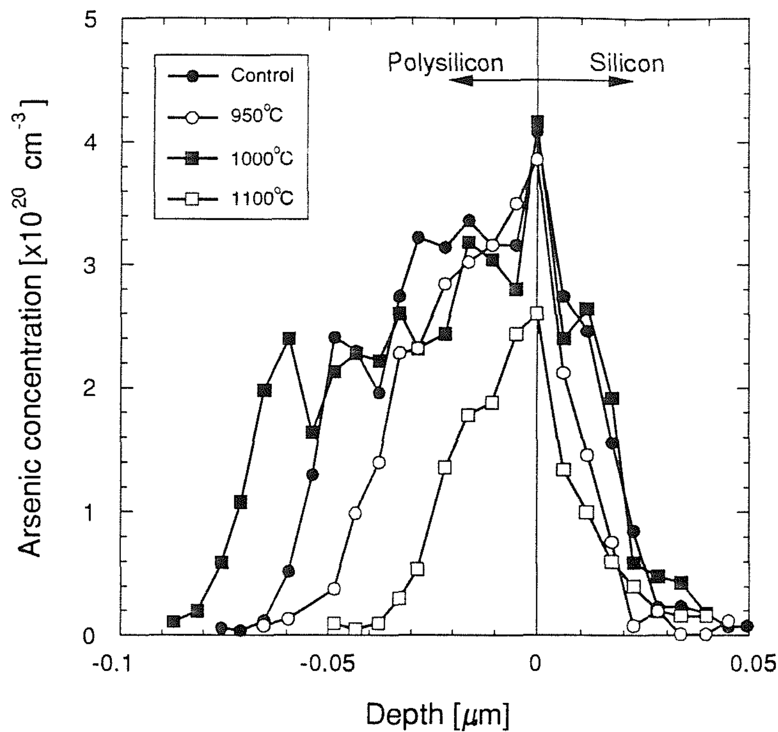

Fig. 2.7 Experimental data of Wolstenholme [17] showing Rutherford back scattering (RBS) arsenic profiles of the polysilicon/silicon interface for devices with a deliberately grown interfacial layer, subjected to various interface anneals.

for conventional metal contacted transistors. Fig. 2.8 shows the current gain as a function of inverse temperature from the work of Graul *et al.* [2], de Graaff and de Groot [3] and Ashburn and Soerowirdjo [26]. Also shown in fig. 2.8 is the temperature dependence of current gain for a conventional metal contacted transistor (whereby the temperature dependence of the current gain is determined by the difference in band-gap narrowing in the base and emitter). It can be seen, especially for temperatures above 300K (i.e. for $c_h kT \geq 0.2$ in equation 2.13), that the temperature dependence of current gain becomes less sensitive to temperature than conventional metal contacted transistors. In fact the results from de Graaff and de Groot [3] even show a negative temperature coefficient. Ashburn and Soerowirdjo [26] modelled the temperature dependence of gain, and showed that the *oxide tunnelling model* could explain the observed results for the whole temperature range in fig. 2.8.

c) Emitter resistance

The presence of a deliberately grown oxide layer at the polysilicon/silicon interface has been shown to block majority carrier flow, leading to an increase in emitter resistance [29]–[31]. This increased resistance can have serious consequences for circuit behaviour, most notably a reduction in output power, and also limitations on the output

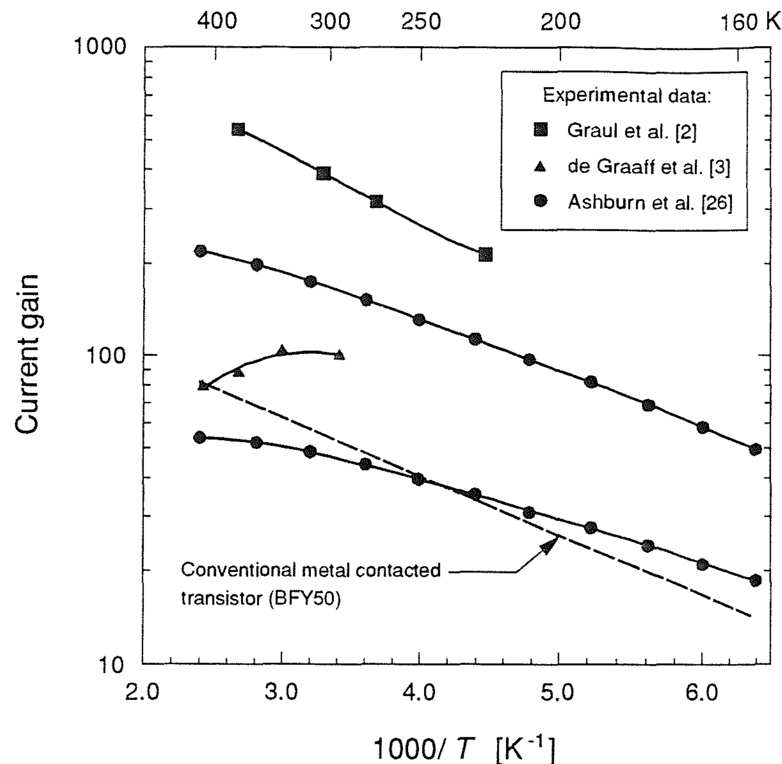

Fig. 2.8 Experimental data of Graul *et al.* [2], de Graaff and de Groot [3], and Ashburn and Soerowirdjo [26] showing current gain as a function of inverse temperature for devices with a deliberately grown interfacial oxide layer. Also shown is the temperature dependence of a conventional metal contacted bipolar transistors, whereby the temperature dependence is attributed to the difference in band-gap narrowing between the base and emitter.

voltage swing of switching circuits. Measurements of specific emitter interfacial resistivity for devices with deliberately grown interfacial oxide layers typically range from 200 to 500 $\Omega\mu m^2$ [29]–[31]. This compares with generally far lower values of 10 to 200 $\Omega\mu m^2$ [29], [31], [32] for devices without deliberately grown interfacial oxide layers. By applying the *oxide tunnelling model* to the devices with interfacial layers, and assuming an average oxide thickness of 14Å and an electrically active polysilicon doping level of 5×10^{19} cm^{-3}, implies a barrier height to electrons of around 0.3–0.4 eV (using the analytical expression for emitter resistance derived in [33]). Comparing this value with the barrier height for holes, which is around 0.7 eV (fig. 2.6), it can be clearly seen that there exists an asymmetry in oxide barrier heights for electrons and holes.

Wolstenholme *et al.* [31] have performed experiments on the 'balling-up' of the interfacial oxide from interface anneals, and then correlating this with measurements on emitter resistance, as shown in fig. 2.9. Also shown in fig. 2.9 is the base current data from fig. 2.6. Some important differences were observed when compared to the corresponding experiment used to study the effect of interface anneals on the base

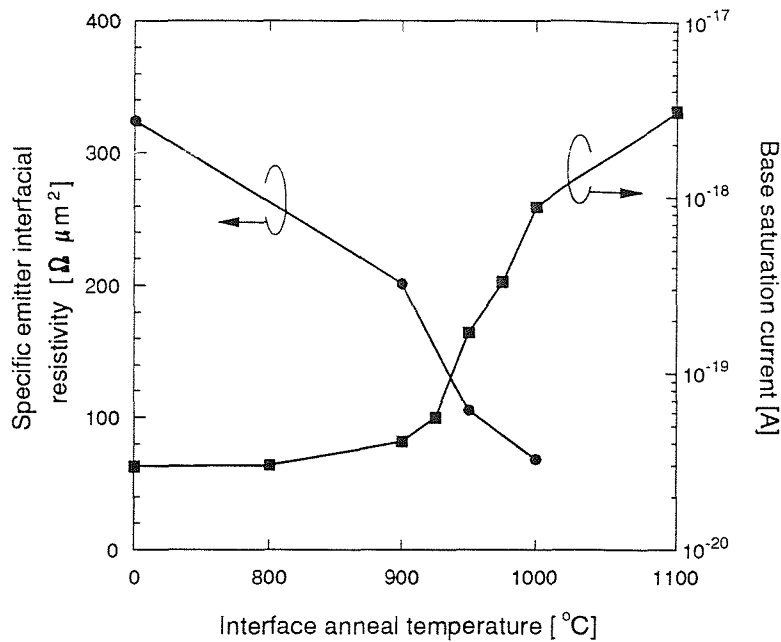

Fig. 2.9 Experimental data of Wolstenholme *et al.* [27], [31] showing the specific emitter resistivity and base saturation current as a function of interface anneal temperature for devices with a deliberately grown interfacial oxide layer.

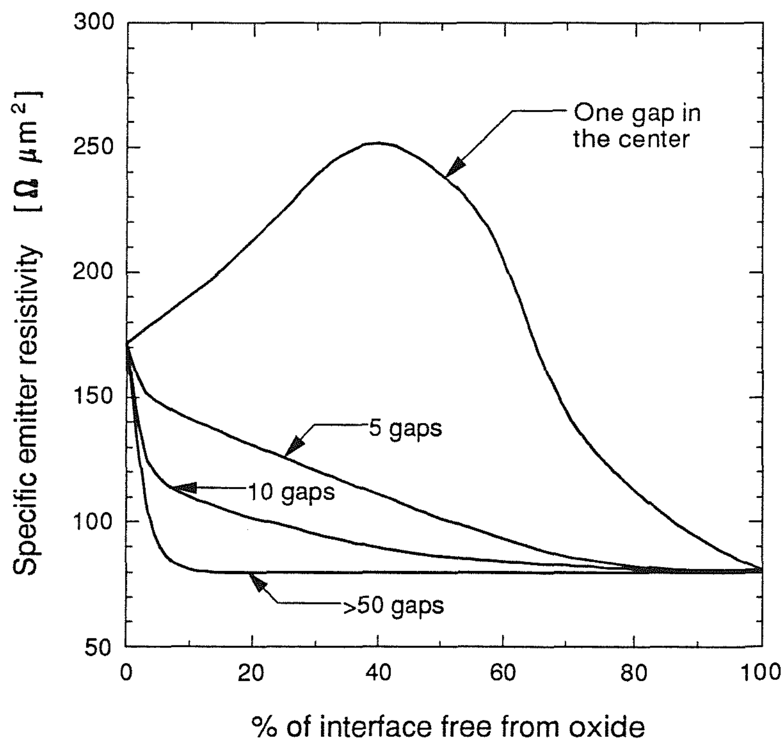

Fig. 2.10 Modelled specific emitter resistivity as a function of the percentage of the interface which is oxide-free for a device with a HF interfacial treatment, from the work of Hamel *et al.* [34]. It can be clearly seen that not only the amount of oxide, but its distribution along the interface will effect the emitter resistance.

current. Most notable was a substantial reduction in emitter resistance for the device given a 900°C interface anneal, compared to the control device, even though the TEM analysis showed that the interfacial layer for both devices was continuous and un-broken. Two-dimensional modeling by Hamel *et al.* [34], as shown in fig. 2.10, has recently shown that this result can be explained if a limited number of widely spaced small gaps in the oxide layer are produced in the 900°C interface anneal, even though nearly 99% of the oxide remains continuous (and so therefore these gaps would be difficult to observe by TEM). Since a large proportion of the interface remains intact, a reduction in base current is still obtained, as observed in fig. 2.9. These results show that an interface anneal is an important tool in adjusting the base current and emitter resistance of devices with deliberately grown interfacial oxide layers [35].

Measurement and modeling of the temperature dependence of emitter resistance, for devices with deliberately grown interfacial oxide layers, has been conducted by Yung *et al.* [36]. They found that the *oxide tunnelling model* could fit the observed temperature dependence, although the shape of the tunnelling barrier had to be changed from rectangular to triangular. Yung *et al.* [36] speculated that dopant pile-up at the interface was the physical cause of this change in barrier shape.

In summary, the *oxide tunnelling model* is successful in explaining the base current, emitter resistance, and the temperature dependence of these two quantities. Neither of the other two theories (*pseudo-grain boundary mobility model* and the *segregation model*) can explain both the reduction of base current and the increase in emitter resistance, as well as the temperature dependence of these quantities, for devices with interfacial oxide layers.

2.4.2 Devices without an interfacial oxide layer

For commercial applications, devices without a deliberately grown interfacial oxide layer are generally preferred because of the emitter resistance problem described above. However, it should be pointed out that an interfacial layer is invariably present at the polysilicon/silicon interface, even in devices given an HF etch prior to polysilicon deposition [27].

a) Segregation of dopant to the interface

Confirmation of the role of the interface in controlling the gain comes from the work of Neugroschel *et al.* [14], who have fabricated bi-layer polysilicon diodes by first depositing undoped polysilicon and then capping the device with *in-situ* arsenic doped polysilicon, as shown in fig. 2.11(a). Drive-in conditions were carefully chosen so that the amount of arsenic segregated to the polysilicon/silicon interface could be

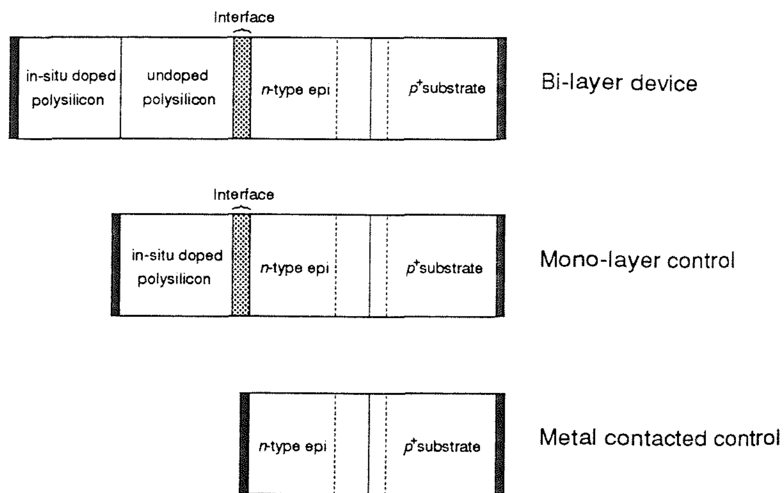

Fig. 2.11(a) Schematic diagram of a bi-layer device, mono-layer control device and metal contacted diodes as used by Neugroschel *et al.* [14].

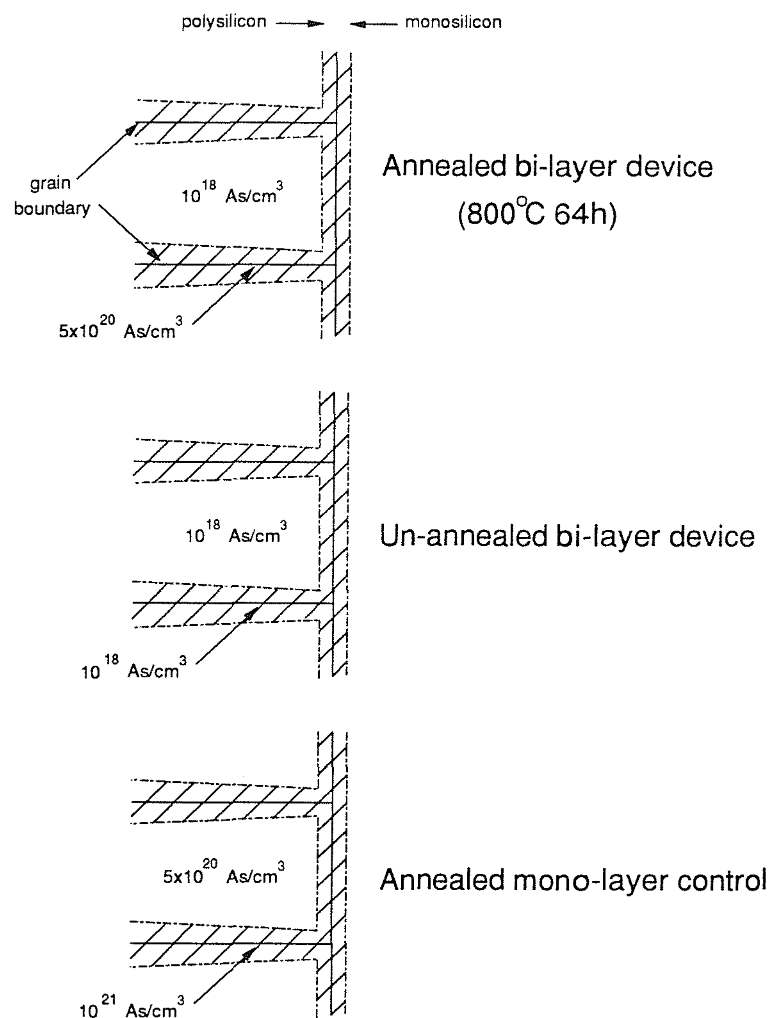

Fig. 2.11(b) Schematic diagram showing the arsenic concentration in the grains and grain boundaries of an annealed bi-layer device, an un-annealed bi-layer device and a mono-layer control as used by Neugroschel *et al.* [14].

varied. A long low temperature drive-in (eg. 64 hours at 800°C) was used to preferentially diffuse the arsenic along the grain boundaries, and dope the grain boundaries and interface to a concentration of around 5×10^{20} cm^{-3}. However, the temperature of the drive-in was not high enough to diffuse arsenic into the bulk of the grains [37], which remained at a low concentration of $\leq 10^{18}$ cm^{-3}. This device was then compared to both an un-annealed bi-layer device (with a low arsenic concentration of $\leq 10^{18}$ cm^{-3} in the grains and at the interface), and to a control device with a single *in-situ* doped polysilicon layer (with an arsenic concentration of $\sim 10^{21}$ cm^{-3} at the interface and around 5×10^{20} cm^{-3} in the grains). A schematic diagram showing the resulting doping concentrations in the polysilicon and at the interface for these three devices is shown in fig. 2.11(b).

Fig. 2.12 shows the current-voltage characteristics for the annealed and un-annealed bi-layer devices, and the single polysilicon layer control device. Also shown is the characteristic for a metal contacted control with no polysilicon layer. The diode current can be assumed to consist only of a hole current (i.e. base current) since the minority electron current injected into the p^+ substrate is small. If it is assumed that transport in the polysilicon layer dominates the hole current, then it would be expected that the current from both the annealed and un-annealed bi-layer devices would be the same, since they have near identical arsenic concentrations of $\leq 10^{18}$ cm^{-3} in the bulk of the

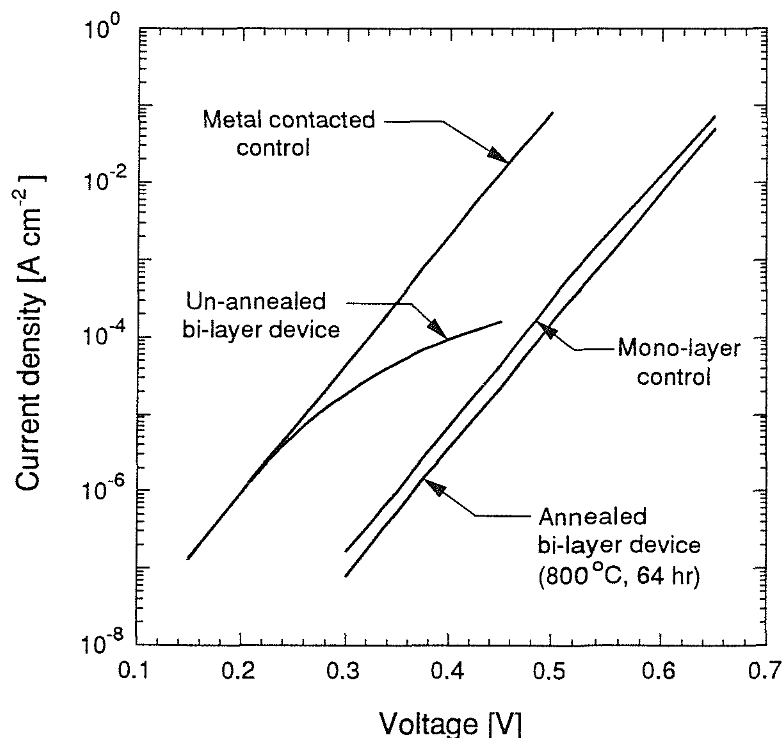

Fig. 2.12 Current-voltage characteristics of the diodes as analysed by Neugroschel *et al.* [14]. The devices shown are the metal contacted control, the single layer polysilicon control, and the annealed and un-annealed bi-layer devices.

grains. Also this value of current would be different to the mono-layer control device, which has a high arsenic concentration of 5×10^{20} cm^{-3} in the grains. This is not observed, and so it can be concluded that the properties of the bulk polysilicon do not contribute to the hole current. Furthermore, the current from the annealed bi-layer device is nearly identical to the mono-layer control, which have different doping concentrations in the bulk polysilicon, but have similar concentrations of arsenic at the polysilicon/silicon interface. It can thus be concluded that the *concentration* of arsenic at the polysilicon/silicon interface is important in controlling the hole current. In addition, the hole current from the metal contacted control is almost identical to that of devices with low arsenic concentrations at the interface, which implies the density of interface states is so large as to recombine all the minority holes at the interface. An interface state density of 6×10^{14} cm^{-2} can be calculated by using equation 2.10, assuming that the hole current is entirely dominated by recombination at the interface (i.e. $T_{block}=\infty$, and $S_I>>S_g$ so that $S_p=2S_I$ in equation 2.9).

For the devices with a high arsenic concentration at the interface, a dramatic reduction of hole current by a factor of 600 is obtained. Fitting this current to an effective recombination velocity, S_p, using equation 2.2 yields a value of 2.3×10^2 cm s^{-1}. Assuming that the hole current is again dominated by recombination at the interface, then an upper limit of 2×10^{11} cm^{-2} can be obtained for the interface state density. The increase of segregated arsenic from 10^{18} to 5×10^{20} cm^{-3} at the interface has thus reduced the interface state density by over a factor of 3000. It is probably more likely that a blocking mechanism makes up a substantial proportion of the hole current for high arsenic concentrations. Assuming that this blocking mechanism results from a reduction in minority carrier mobility at the interface (*pseudo-grain boundary mobility model*), and assuming that the disordered interfacial region is 7Å thick, then the minority carrier mobility, μ_{pgb} has to reduce to 7×10^{-4} cm^{2}V^{-1}s^{-1} (compared to the bulk silicon mobility of around 500 cm^{2}V^{-1}s^{-1} in the emitter) in order to model the effective recombination velocity. Alternatively, the *segregation model* can be used to fit the effective recombination velocity. SIMS analysis on the annealed bi-layer devices showed that the segregated arsenic at the interface was a factor of 10^4 larger than the arsenic in the emitter [14]. Assuming that the arsenic at the interface is electrically active, the barrier created could result in a blocking recombination velocity of 3×10^2 cm s^{-1}. This value is just marginally outside the constraints placed on the recombination velocity (i.e. $T_{block}\leq2.3\times10^2$ cm s^{-1}), and so it is plausible that this mechanism could provide the blocking action to injected holes. However, when band-gap narrowing is taken into account the segregated dopant can now only provide a blocking recombination velocity of 9×10^3 cm s^{-1}, which is well outside the constraints placed on the blocking recombination velocity.

The above results demonstrate the importance of recombination via states at the polysilicon/silicon interface, and also its relationship to the segregated arsenic concentration. Patton *et al.* [15] have also shown that recombination at the interface cannot be ignored, particularly when the doping concentration in the polysilicon is low. Fig. 2.13 shows the measured base current as a function of polysilicon doping level for various emitter drive-in conditions. Nearly all the devices have large base currents at low polysilicon doping levels ($3x10^{19}$ cm^{-3}), which fall to minimum values around $1-2x10^{20}$ cm^{-3} and then rise for increased doping levels up to $5x10^{20}$ cm^{-3}. Also shown in fig. 2.13 is the modelled base current from the extended emitter model (i.e. $T_{block}=\infty$ and $S_I=0$, so that $S_p=S_g$ in equation 2.9), which can qualitatively explain the increase in base current at high values of doping ($2-5x10^{20}$ cm^{-3}) by increased Auger recombination in the bulk polysilicon. However, the extended emitter model cannot explain either the sharp increase in base current at the low polysilicon doping levels of $3x10^{19}$ cm^{-3}, or the reduction in base current for the devices annealed at 900°C for

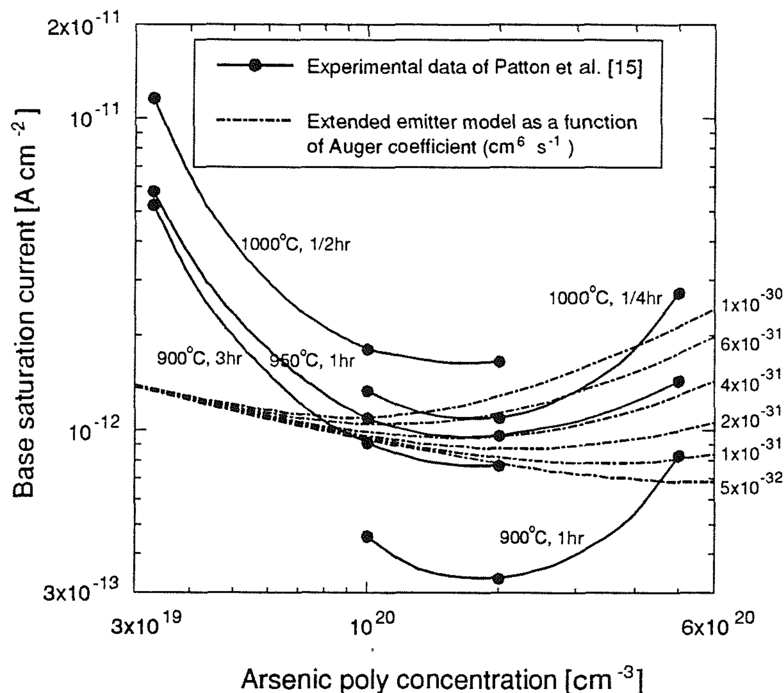

Fig. 2.13 Experimental data of Patton *et al.* [15] showing base saturation current as a function of arsenic concentration in the polysilicon for various emitter anneals. Also shown is the modelled base current as a function of Auger coefficient in the polysilicon, assuming that no blocking or recombination mechanisms exists at the interface (i.e. the *extended emitter model* with $T_{block}=\infty$, $S_I=0$). The polysilicon is assumed to be 40% electrically active and consisting of only one crystalline grain.

1 hour. It can therefore be concluded that a recombination mechanism is dominating at low polysilicon doping levels, whilst a blocking mechanism is dominating the 900°C 1 hour devices.

Fig. 2.14 shows the modelled values of base current as a function polysilicon doping for various interface state densities, assuming no blocking action at the interface (i.e. $T_{block}=\infty$, so that $S_p=2S_I+S_g$ from equation 2.9). The case for $N_{it}=0$ is that for the *extended emitter model* (i.e. $S_p=S_g$). The modeling clearly demonstrates that a constant value of interface state density cannot model the base current, especially at low arsenic concentrations.

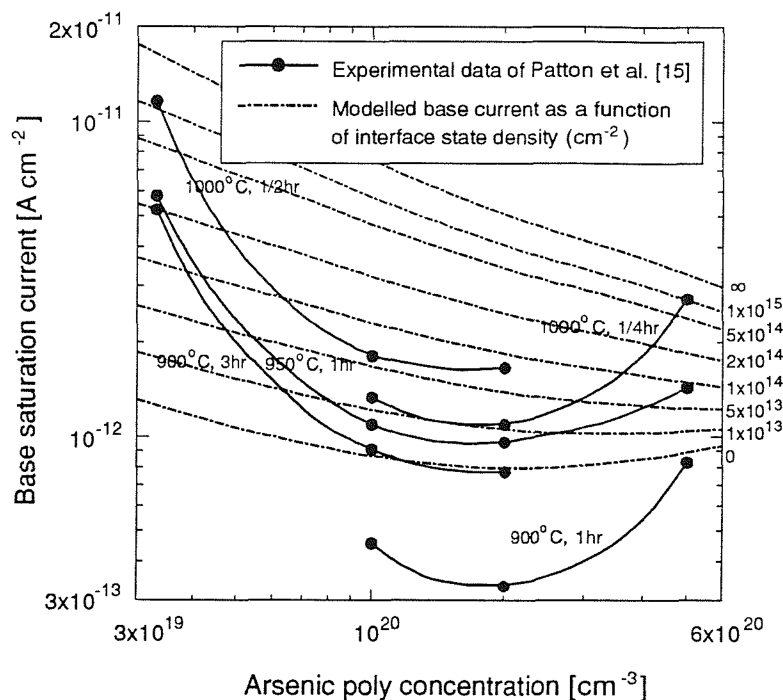

Fig. 2.14 Experimental data of Patton *et al.* [15]. Also shown is the modelled base current as a function of interface state density, assuming no blocking at the interface (i.e. $T_{block}=\infty$). The modelled base current for a metal contacted control is also shown (i.e. $N_{it}=\infty$).

Patton *et al.* [15] argued that the arsenic segregation could lower the trap density at the interface. Fig. 2.15 models the base current of the device annealed at 950°C for 1 hour, by the combined contribution of recombination via interface states (for interface state densities as a function of arsenic concentration) and minority carrier transport in the bulk polysilicon (assuming no blocking action at the interface, i.e. $T_{block}=\infty$). A reasonable fit to the measured base current can result, if it is assumed that the interface state density reduces from 2×10^{14} to 1.4×10^{13} cm^{-2}, as the arsenic concentration increases from 3×10^{19} to 2×10^{20} cm^{-3}. For higher arsenic concentrations, the interface state density

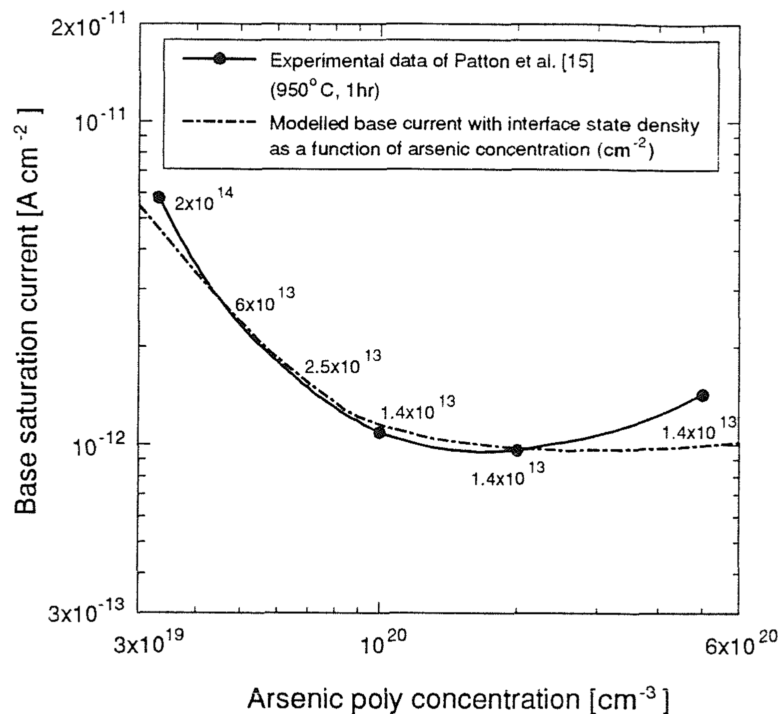

Fig. 2.15 Experimental data of Patton *et al.* [15] for an emitter anneal of 950°C for 1 hr. Also shown is the modelled base current as a function of interface state density, assuming that the interface state density varies with arsenic concentration in the polysilicon. No blocking action is assumed to occur at the interface (i.e. $T_{block}=\infty$).

is assumed to reduce to a constant density as the segregated arsenic saturates the interface states. The increase in base current at high arsenic concentrations ($\geq 2\times10^{20}$ cm^{-3}) is due to increased recombination in the bulk of the polysilicon.

Fig. 2.16 shows the fitted interface state density, as a function of polysilicon doping, for all the drive-in conditions in fig. 2.14. Also shown are the modelled results from Neugroschel *et al.* [14], who used low temperature drive-ins of 800°C, and the modelled results from Meister *et al.* [38] who used rapid thermal annealing at 1050°C. The most immediate trend visible is that of a dramatic reduction in interface state density for increases in arsenic concentration from 3×10^{19} to 10^{20} cm^{-3}. This behaviour can be explained by the passivation of the interface states due to segregation of arsenic to the interface. There is, however, a second trend in the results of fig. 2.16, which reveals that in most cases the largest interface state densities are obtained for the highest anneal temperatures. This result is nonetheless consistent with the findings of Mandurah *et al.* [39], who have studied the segregation of arsenic to the grain boundaries, as a function of anneal temperature. They found that as the anneal temperature is increased a greater proportion of the arsenic resides in the bulk of the grains, compared to the

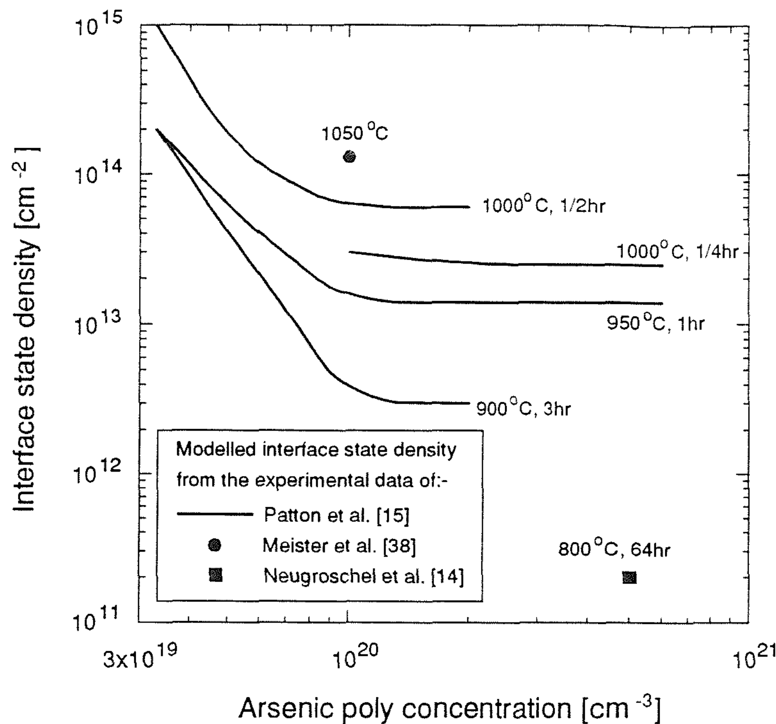

Fig. 2.16 Modelled interface state density as a function of arsenic concentration in the polysilicon, and polysilicon anneal, for devices with no deliberately grown interfacial oxide layers. Experimental data is from Patton *et al.* [15], Neugroschel *et al.* [14], and Meister *et al.* [38].

grain boundaries. Therefore, at these elevated temperatures, the passivation effect of the segregated arsenic at the interface is lost, and so the interface state density increases, which in turn increases the base current.

Turning now to the 900°C device annealed for 1 hour, the base current shows a reduction by a factor of 2.5 (for polysilicon doping concentrations of 1–2x10^{20} cm^{-3}) from the *extended emitter model* (fig. 2.13), which suggests that a blocking mechanism at the interface is controlling the base current. Fig. 2.17 shows the experimental data and the modelled base current, as a function of the effective recombination velocity, S_p. An effective recombination velocity of 2.7x10^4 cm s^{-1} can be fitted to the base current for polysilicon concentrations of 1-2x10^{20} cm^{-3}. Assuming that the effective recombination velocity is dominated by a blocking mechanism at the interface (i.e. S_I=0), then the *pseudo-grain boundary mobility model* can be used to model this fitted value of recombination velocity. This results in a minority hole interface mobility, μ_{pgb} of 0.1 $cm^2V^{-1}s^{-1}$, which is a reduction in hole mobility by a factor of 1500 compared with the mobility in the bulk emitter. Alternatively, the base current may be dominated by recombination via interface states, especially if the blocking recombination velocity

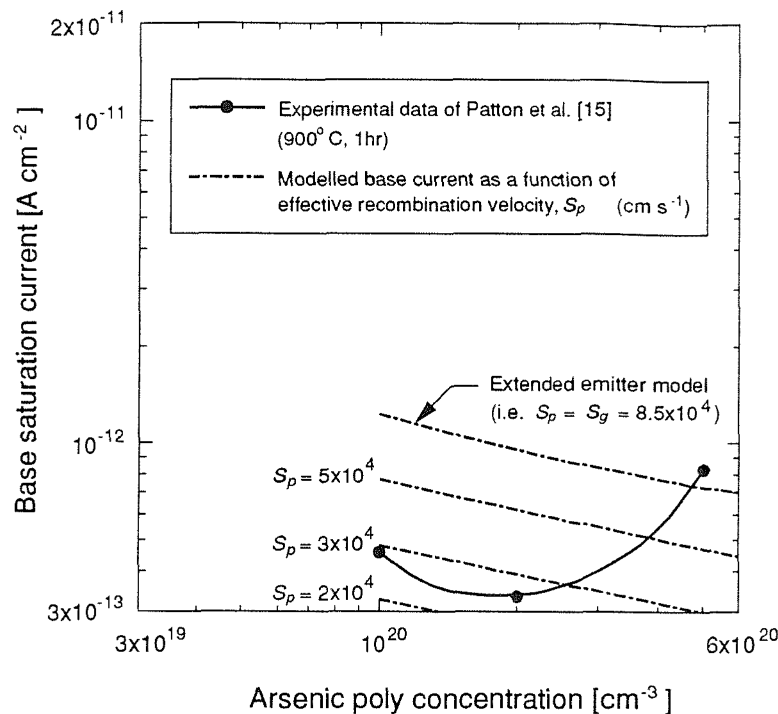

Fig. 2.17 Experimental data of Patton *et al.* [15] for an emitter anneal of 900°C for 1 hr. Also shown is the modelled base current as a function of the effective recombination velocity (S_p), and the modelled base current using the *extended emitter model* (i.e. with T_{block}=∞ and S_I=0). The polysilicon is assumed to be 10% electrically active.

is small. Assuming the base current is dominated by recombination at the interface (i.e. T_{block}≈0), then the fitted value of the effective recombination velocity would yield an upper limit to the interface state density of $1.3\text{x}10^{13}$ cm^{-2}.

The *segregation model* predicts a barrier to minority carriers of around $0.9kT$ (using the SIMS analysis in [15]) for the devices annealed at 1000°C, if the segregated arsenic at the interface is electrically active. Assuming a similar barrier exists for devices annealed at 900°C, then this barrier yields a recombination velocity of $7.5\text{x}10^4$ cm s^{-1} (no band-gap narrowing), or $8.1\text{x}10^4$ cm s^{-1} (with band-gap narrowing). These values of blocking recombination velocity therefore cannot account for the reduction in base current. For the highest arsenic concentration of $6\text{x}10^{20}$ cm^{-3}, no blocking action results, and the base current increases to that of an extended emitter device. It is plausible that this high concentration of arsenic could have caused the polysilicon to either partially or fully epitaxially re-align, and so emulate an extended emitter device.

b) Hydrogen passivation

Further confirmation of the importance of interface states has come from experiments on hydrogen passivation [15], [40]. For example, Patton *et al.* [15] implanted

hydrogen into polysilicon in an effort to passify the interface states. Fig. 2.18 shows that hydrogen passivation can reduce the base current by a factor of 3.5 for polysilicon doping levels of $3x10^{19}$ cm^{-3}. These changes in base current can be modelled by assuming that the hydrogen causes a reduction in interface state density. Fig. 2.18 shows the modelled base current, as a function of interface state density, for a polysilicon doping concentration of $3x10^{19}$ cm^{-3}, assuming that there is no blocking action at the interface (i.e. T_{block}=∞). The incorporation of the hydrogen has resulted in a drop in interface state density by a factor of 34 from $1.7x10^{14}$ cm^{-2} down to $5x10^{12}$ cm^{-2}.

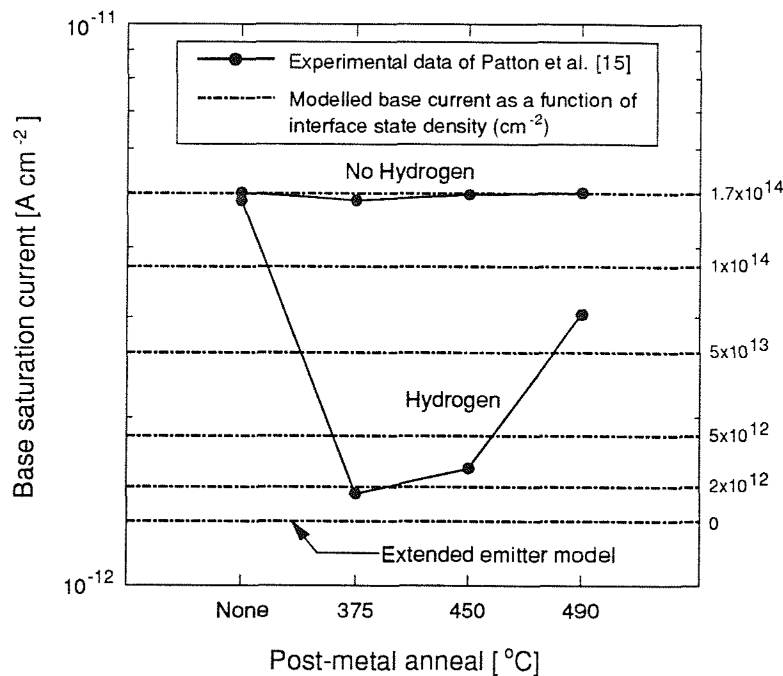

Fig. 2.18 Experimental data of Patton *et al.* [15] showing base saturation current as a function of post metal anneal after hydrogen passivation, for a polysilicon doping concentration of $3.3x10^{19}$ cm^{-3}, and an emitter anneal of 950°C for 1 hr. Also shown is the modelled base current as a function of interface state density assuming no blocking at the interface (i.e. T_{block}=∞).

It is clear from the modeling of these experiments that recombination at the polysilicon/silicon interface can dominate the base current, especially at low polysilicon doping concentrations. However, for practical polysilicon emitter devices, arsenic concentrations are chosen to be in the range $1–2x10^{20}$ cm^{-3}, with an emitter anneal of around 900°C for 1 hour, in order to form shallow emitter junctions. Therefore, from the modeling results in this section, recombination via interface states should not dominate for typical commercial devices.

c) Polysilicon thinning

The influence of the polysilicon layer on the current gain has been studied by several authors [15], [38] who made measurements on polysilicon emitter transistors in which the polysilicon layer has been thinned after emitter drive-in. The results of Meister *et al.* [38] are typical, and are shown in fig. 2.19. It can be seen that the base current remains constant down to a thickness of less than 10nm, which shows that the base current is dominated by the blocking/recombination properties of the polysilicon/silicon interface, even in devices without a deliberately grown interfacial oxide layer. Also shown in fig. 2.19 is the modelled base currents as a function of polysilicon thickness. Equation 2.2 was used to convert the modelled effective recombination velocity into a base current, and the emitter Gummel number was extracted from the metal contacted control. The device was first modelled by the *extended emitter model* (i.e. curve 1 with $T_{block}=\infty$ and $S_I=0$), and as can be clearly seen, it is impossible to model both the metal contacted control and the variation of base current with polysilicon thickness. Decreasing T_{block} to 5×10^5 cm s^{-1} (curve 2, with $S_I=0$) enables the base current of the metal contacted control and the polysilicon emitter

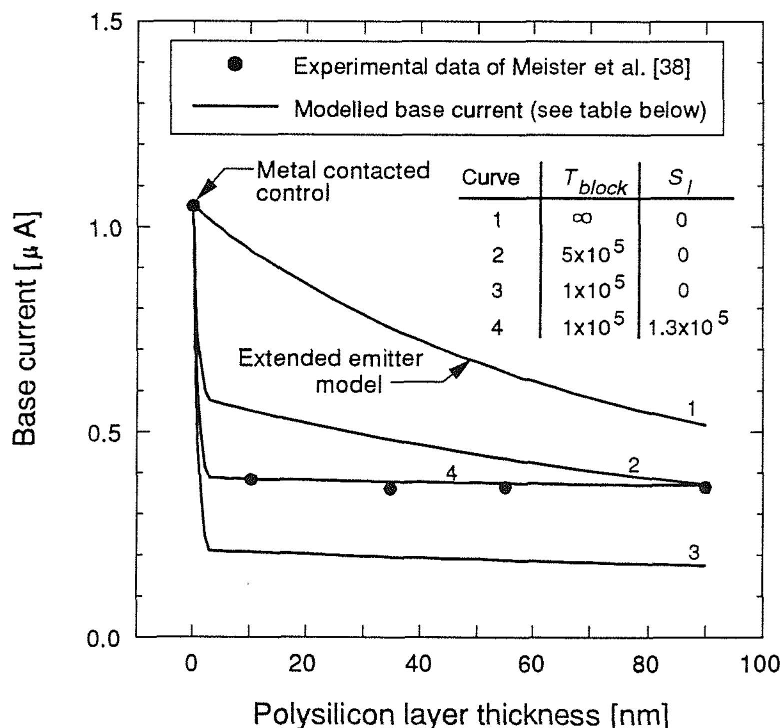

Fig. 2.19 Experimental data of Meister *et al.* [38] showing base current (V_{BE}=0.66V and A_{EW}=15.5X15.5μm^2) as a function of polysilicon thickness. Also shown is a metal contacted control with zero polysilicon thickness. The modelled base current is shown as a function of interface state density and blocking recombination velocity. Also shown is the modelled base current using the *extended emitter model* (i.e. $T_{block}=\infty$, $S_I=0$). S_M is taken to be equal to infinity.

device with an emitter thickness of 90nm to be both modelled. However, for polysilicon thickness between 0 and 90nm the model cannot be fitted to the base current. Further reductions in T_{block} to $1\text{x}10^5$ cm s^{-1} (curve 3), allows the constant base current with polysilicon thickness to be modelled, but at the expense of being unable to model the absolute value of base current. The only way to remedy this situation is for the interface state recombination velocity (S_I) to take values other than zero. Curve 4 in fig. 2.19 shows that an excellent fit to the experimental data can be made with $T_{block} \leq 10^5$ cm s^{-1}, and $S_I \geq 1.3\text{x}10^5$ cm s^{-1}, which corresponds to an interface state density which must be greater than $1.3\text{x}10^{14}$ cm^{-2}. This interface state density is rather high when compared with the values in fig. 2.18, although this can be explained by noting that the emitter drive-in temperature was 1050°C, which gives rise to a high interface state density.

d) Temperature dependence of current gain

The temperature dependence of the current gain for devices without a deliberately grown interfacial layer has been experimentally measured by Ashburn and Soerowirdjo [26] (figs. 2.20(a) and 2.20(b)). They found that the temperature sensitivity of the current gain was *greater* than that of conventional metal contacted transistors, especially at higher temperatures. This temperature dependence differs markedly to that of devices with deliberately grown interfacial oxide layers (i.e. dominated by tunnelling), which show a far *lower* temperature sensitivity at higher temperatures. Fig. 2.20(a) shows the experimental data of Ashburn and Soerowirdjo [26], as well as the modelled current gain using the *oxide tunnelling model.* It is clear that the model cannot explain the observed temperature dependence (especially at higher temperatures), and so it can be concluded that tunnelling is not the dominant mechanism in devices without deliberately grown interfacial oxide layers.

Fig. 2.20(b) shows the experimental data of Ashburn and Soerowirdjo [26], as well as the modelled current gain using the *pseudo-grain boundary mobility model.* If it is assumed that the interface hole mobility is temperature independent, then the temperature dependence of the current gain is controlled by the difference in the band-gap narrowing between the base and emitter, as in a conventional metal contacted device (shown as the n=0 curve in fig. 2.20(b)). However, a fit cannot be made to the measured current gain, which implies that the hole mobility must be temperature dependent. If it is assumed that the interface hole mobility has a simple dependence of the form $\mu_{pgb}=AT^n$ (where A is a temperature independent constant), then an excellent fit to the experimental data can be achieved for $n=-0.65$.

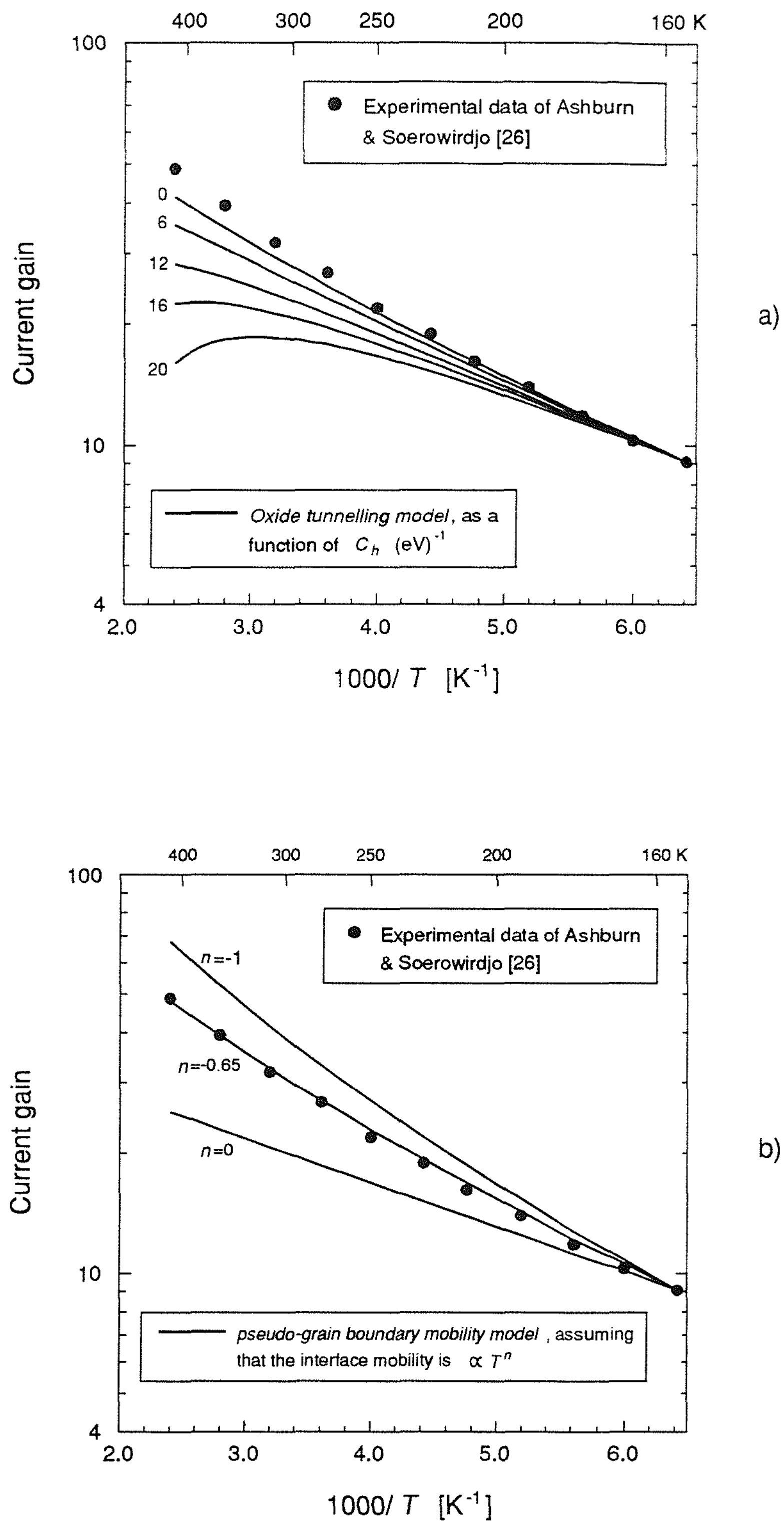

Fig. 2.20 Experimental data of Ashburn and Soerowirdjo [26] showing current gain as a function of inverse temperature for devices without a deliberately grown interfacial oxide layer. Also shown is the modelled base current, using a) the *oxide tunnelling model* (assuming S_I=0, and T_{block}<<S_g), as a function of the parameter c_h (in equation 2.13), and b) the *pseudo-grain boundary mobility model*

e) Effect of an interface anneal

Wolstenholme *et al.* [27] have performed the same interface anneal experiments with HF devices as with RCA devices, and the results are shown in fig. 2.21. These results show that the base current increases by a factor of 5.5 as the interface anneal temperature is increased from 800 to 1000°C. Also shown in fig. 2.21 is the modelled base current as a function of effective recombination velocity, S_p, and the modelled base current using the *extended emitter model.* Transmission electron microscopy (TEM) reveals that a dip-etch in hydrofluoric acid (HF) prior to polysilicon deposition (which is designed to remove any interfacial oxide), nevertheless produces a uniform oxide of approximately 4Å thickness [27]. After typical anneals at 900°C, thermal stressing causes the thin HF oxide to break-up, leading to a discontinuous layer varying in thickness from 0 to 8Å, and with approximately 30% of the interface oxide-free. This compares with the 1000°C interface anneal device, in which 90% of the interface is oxide-free. These results clearly indicate that the interfacial oxide controls the base current in an HF device. It is tempting to conclude therefore, that tunnelling through the interfacial oxide is the dominant mechanism, even in HF devices. However, as

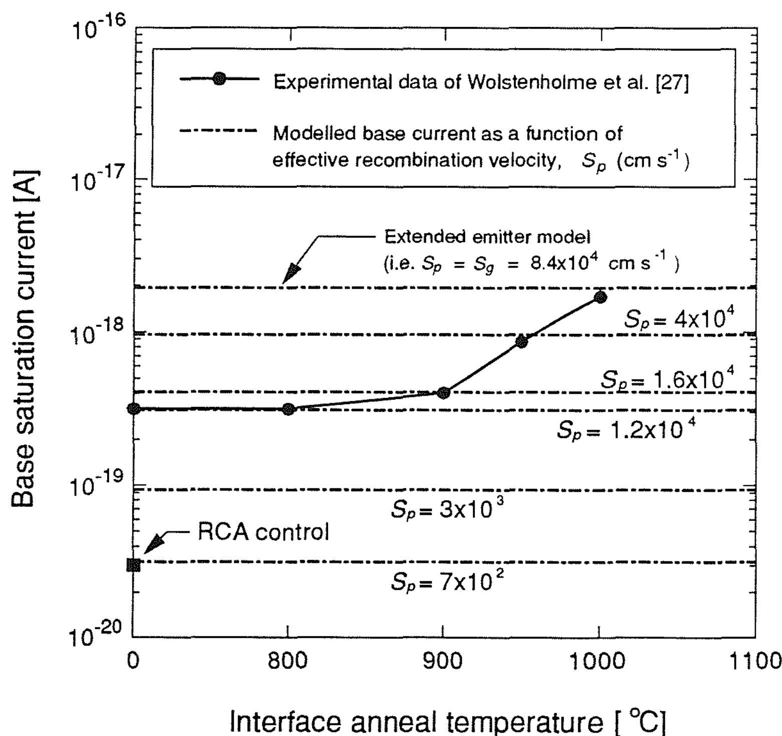

Fig. 2.21 Experimental data of Wolstenholme *et al.* [27] showing the base saturation current, as a function of interface anneal, for devices without a deliberately grown interfacial oxide layer. Also shown is the modelled base current as a function of the effective recombination velocity (S_p), and the modelled base current using the *extended emitter model* (i.e. with T_{block}=∞ and S_i=0).

already shown in fig. 2.20(a), this conclusion is inconsistent with the measured temperature dependence of the current gain, which is markedly stronger for the HF devices than for the RCA devices. In order to explain this apparent inconsistency, it is necessary to consider how a discontinuous interfacial oxide can be modelled in two dimensions.

2.5 Modelling a discontinuous interfacial oxide layer

Very little has been published on the two-dimensional modelling of the polysilicon/silicon interface, although Hamel *et al.* [34] have simulated the majority carrier flow in a polysilicon emitter as a function of oxide break-up. Their simulations revealed that the majority carrier current flow had a large lateral component, which was required to explain the observed decrease in emitter resistance with oxide break-up [31]. Recent attempts to model the minority carrier flow at the polysilicon/silicon interface in two-dimensions [41], have shown that the current flow is primarily through those regions of the interface free from oxide. Hence the lateral component of the minority carrier flow can be largely ignored, and this is the approach followed in this chapter.

The effect of a broken-up interfacial oxide layer on the base current is modelled by assuming that the emitter can be treated as two polysilicon emitter transistors connected in parallel, one with an interfacial oxide layer and the other without. The area of the interface which is oxide-covered is denoted by A_{ox}, and that which is oxide-free by A_{nox}. Each of these areas of the interface can then be described by an effective recombination velocity, T_{tun} (dominated by the *oxide tunnelling model*) and T_{pgb} (dominated by the *pseudo-grain boundary mobility model*). The overall recombination velocity, S_p can be then be calculated as a weighted mean of these two contributions:

$$S_p = T_{tun}\left(\frac{A_{ox}}{A_{EW}}\right) + T_{pgb}\left(\frac{A_{nox}}{A_{EW}}\right) \qquad (2.20)$$

where A_{EW} is the total emitter window area. Wolstenholme [17] and Gold [42] have used equation 2.20 to model the base current of polysilicon emitters as a function of the fraction of interface which is oxide-free, and the results are shown in fig. 2.22 for devices with a deliberately grown interfacial oxide layer. Also shown are some of the modelled recombination velocities from the experimental results in figs. 2.6 and 2.21. The value of T_{tun} used in fig. 2.22 for the situation of no oxide break-up has been fitted from the base current of the RCA control device. As the oxide breaks up, high

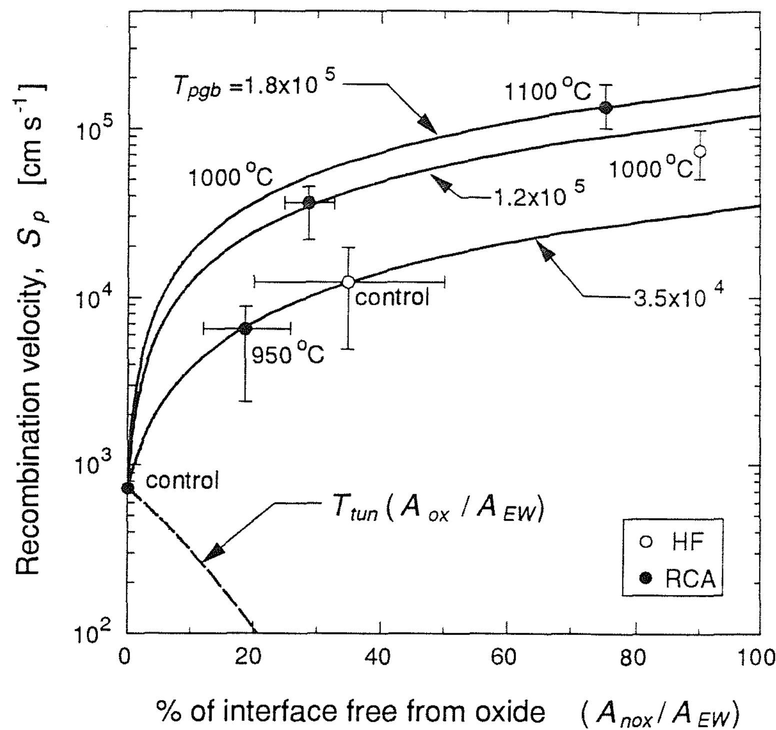

Fig. 2.22 Modelled recombination velocity, S_p as a function of the fraction of the interfacial layer which is oxide-free, for devices with a deliberately grown interfacial oxide layer (using equation 2.20). Also shown is a selection of the modelled experimental base currents from figs. 2.6 and 2.21. The modelled recombination velocity is only strictly relevant for those devices with a deliberately grown interfacial oxide layer (RCA). The dashed line corresponds to only the first term in equation 2.20.

resolution TEM has shown [27], [42] that it becomes thicker in some regions and thinner in others, with the overall oxide volume remaining constant. In order to model the tunnelling current through the oxide-covered regions (the first term in equation 2.20), T_{tun} has been calculated for each of the RCA devices, assuming an initial oxide thickness of 14Å and a constant oxide volume. The result of these calculations is shown as the dashed line in fig. 2.22. It is clear that, apart from the very early stages of oxide break-up ($A_{nox}/A_{EW} \leq 0.1$), the overall recombination velocity, S_p is dominated by the second term in equation 2.20. This means that the majority of the hole current in a device with a broken-up interfacial oxide flows through the oxide-free regions. Thus the factor of a 100 increase in base current of the RCA device with an interface anneal of 1100°C, compared with the control (fig. 2.6), can be partly explained as simply the increase in area of those portions of the interface which are free from oxide.

Another factor which is likely to influence S_p is the epitaxial re-growth of the polysilicon through the holes in the interfacial oxide [27], [42]. This re-growth is likely to affect the value of the pseudo-grain boundary recombination velocity, T_{pgb}, since the grain boundary moves further into the polysilicon as the oxide breaks-up. The effect of a change in the value of T_{pgb} is illustrated in fig. 2.22 for values ranging from

3.5×10^4 to 1.8×10^4 cm s^{-1}. A comparison between the measured and modelled results suggests that T_{pgb} increases as the interfacial oxide breaks-up. This could be caused either by a decrease in the amount of dopant segregated to the polysilicon/silicon interface, or by increased recombination in the single-crystal emitter.

Turning now to the devices without deliberately grown interfacial layers (HF devices), the modelling is somewhat complicated since there exists no 'control' device (i.e. a device with a uniform 4Å oxide at the interface). Nevertheless, if it is assumed that the value of T_{tun} used in equation 2.22 is much less than T_{pgb}, then the modelled curves in fig. 2.22 are still valid for the HF devices. The difference in recombination velocity between the control HF device and the 1000°C interface anneal device is a factor of 5.5, whilst the difference in the oxide-free area at the interface is only a factor of 3. The fact that the base current increases more than predicted by the difference in areas of the oxide-free regions of the interface, can be explained by an increase in the value of the pseudo-grain boundary recombination velocity, T_{pgb}, as was observed for the RCA devices. Therefore, in an HF device, it can be concluded that the majority of the hole current flow is through the gaps in the interfacial oxide, with the result that the device behaviour is dominated by the *pseudo-grain boundary model.* This conclusion is supported by the measurements of the temperature dependence of the current gain as shown in fig. 2.20(b).

The above analysis for the HF devices assumes that $T_{tun} << T_{pgb}$. In order for this to be true, it is necessary for the thin interfacial oxide (≈4Å thick) in the real HF 'control' device to present a significant barrier to holes. Calculations indicate that an effective barrier height to holes, χ_h, of around 2 eV is required for this to be the case, which compares with a value of 0.72 eV for the RCA devices, as discussed in section 2.4.1. This suggests that the HF interfacial oxide is different in nature to the RCA oxide, a conclusion which is consistent with the findings of Roulston *et al.* [43].

2.6 Conclusions

This chapter has critically reviewed the literature on polysilicon emitter bipolar transistors, and highlighted the need for a common approach to device modelling. A model has been proposed, based on existing models from the literature, which is simple enough to yield analytical results, but is also able to adequately model all the relevant physical processes. This model has then been applied to the experimental data in the literature, which has allowed the identification of the dominant physical mechanisms as a function of the fabrication conditions.

If devices are fabricated with a deliberately grown interfacial oxide layer, then the modelling has shown that tunnelling through the interfacial oxide layer can explain both the reduction in base current and the increase in emitter resistance, as well as the temperature dependence of these two quantities. The thermionic emission barrier created by segregated dopant at the interface cannot explain either the reduction in base current, or the increase in emitter resistance.

If devices are fabricated without a deliberately grown interfacial oxide layer, then the modelling has identified two distinct regions of device behaviour. Firstly, for low concentrations of arsenic in the polysilicon ($<10^{20}$ cm^{-3}) and/or high anneal temperatures (>1000°C), the recombination of carriers via the high density of interface states at the polysilicon/silicon interface dominates the base current. This results in a current gain which is decreased below that for an extended emitter device. Secondly, for arsenic concentrations of $1-2x10^{20}$ cm^{-3} and anneals around 900°C (as used in many commercial processes), the increased segregation of arsenic to the grain boundaries pacifies the interface states, which results in a reduction of base current. These devices show an increase in current gain above that for an extended emitter device. Thus the experimental observation of a reduction of base current as a function of segregated arsenic at the interface is shown to be due to a decrease in the density of recombination states, and not due to any barrier created at the interface by segregated dopant.

In order to fully explain this gain enhancement, it is necessary to model the discontinuous interfacial oxide in two dimensions. The use of a simple pseudo-two-dimensional model shows that the oxide covered regions of the interface are opaque to minority carriers, so that most of the current flows through the gaps in the oxide. The base current is therefore determined primarily by the fraction of the interface which is oxide-free, and hence is very sensitive to the detailed structure of the interfacial oxide. The dominant base current mechanism is thus reduced minority carrier mobility in the pseudo-grain boundary at the polysilicon/silicon interface.

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Chapter 3

Electrical Method for Measuring the Emitter Depth of Shallow Bipolar Transistors

3.1 Introduction

As the lateral dimensions of bipolar transistors shrink to sub-micron geometries with the advent of self-aligned processing technologies, the corresponding vertical junction depths (emitter/base and base/collector) must also scale if the effect of parasitic sidewall capacitances are to be kept to a minimum. The accurate modelling [1], [2] of modern high-speed bipolar transistors requires a good knowledge of the emitter profile, especially the emitter junction depth and the doping concentration at the emitter contact [3]. Unfortunately the measurement of these parameters by conventional methods is extremely difficult for the very shallow ($\leq 0.05\mu m$) junctions, which are employed in state-of-the-art bipolar processes. The widely used technique of secondary ion mass spectroscopy (SIMS) suffers from calibration problems, and by an inability to resolve fast changing profiles (at best SIMS can only resolve profiles no steeper than around 1 decade every $0.02\mu m$), whilst only supplying the chemical concentration profile. Spreading resistance (SR) measurements will supply the electrically active profile (if a mobility model is assumed) but again suffers similar resolution problems to the SIMS technique, as well as the phenomenon of 'carrier spilling' [4]. The analytical methods of SIMS and SR also have the added disadvantage that they require special sample preparation and the setting up and use of specialist equipment, both factors which add to the time and ultimately the cost of any such analysis.

The junction depth as determined by the SIMS technique can be improved in accuracy by taking advantage of the electric field coupling [5], [6] between arsenic and boron during diffusion. The electric field is associated with the steep gradients of the arsenic and boron profiles, which can result in enhanced boron diffusion, causing a 'dip' in the boron profile where the emitter/base junction occurs (this being the position of the maximum value of electric field). Typically, these results show that the emitter/base junction is located at a shallower depth than that indicated by the 'crossing' of the emitter and base profiles (see fig. 3.1), and so therefore indicates the unsuitability of SIMS for measuring shallow emitter depths. Unfortunately, strong electric field coupling is only seen on samples with very steep high concentration emitter and base profiles. For the devices analysed in this chapter, the implanted bases are too deep for any electric field coupling to take place.

This chapter will describe a simple electrical method for measuring the emitter junction depth which yields accurate values for very shallow junctions. A comparison is made with the values obtained from both spreading resistance and the SIMS technique, and it is shown that the measured emitter depth can be used to accurately model the collector current of a bipolar transistor.

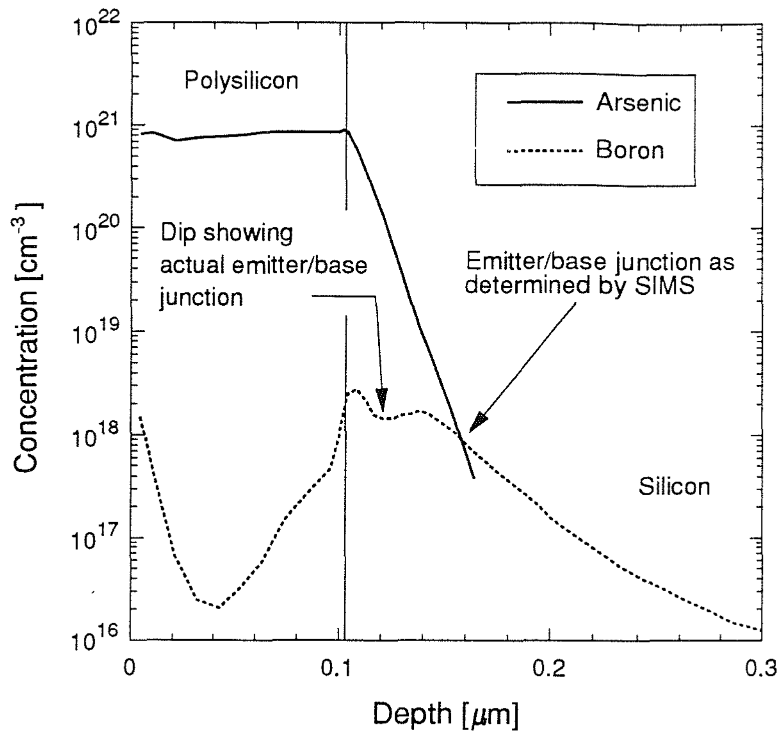

Fig. 3.1 Arsenic and boron SIMS data of Stork *et al.* [6] showing the 'dip' in the boron profile which indicates the actual position of the emitter/base junction. The position of the emitter/base junction indicated by the crossing of the arsenic and boron profiles is considerably deeper than the actual emitter/base junction.

3.2 Theory

The base layer of a bipolar transistor is usually characterised by a pinch sheet resistance, and fig. 3.2 shows a cross-sectional view of such a resistance monitor. The sheet resistance of the base pinch resistor (resistance under the emitter), R_{UE} of such a structure can be expressed as,

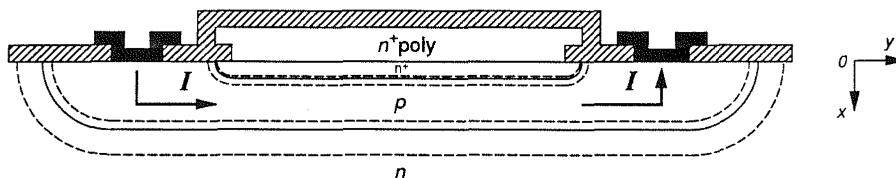

Fig. 3.2 Cross-sectional view of a pinched base sheet resistance monitor.

$$R_{UE} = \frac{1}{q\int_{W_E''}^{W_B} N_B(x)\mu_B(x)dx} \tag{3.1}$$

where $N_B(x)$ is the base dopant distribution, $\mu_B(x)$ is the *majority* carrier mobility in the base, W_B is the neutral base depth, and W_E'' is the metallurgical emitter depth, W_E' plus the extent of the emitter/base depletion region into the base (see fig. 3.2). Similarly, the sheet resistance of the intrinsic base layer (i.e. the resistance of the base layer without an emitter), R_{IB} can be expressed as,

$$R_{IB} = \frac{1}{q\int_0^{W_B} N_B(x)\mu_B(x)dx} \tag{3.2}$$

Splitting the range of integration of the integral in equation 3.2 into emitter and base regions,

$$\int_0^{W_B} N_B(x)\mu_B(x)dx = \int_0^{W_E''} N_B(x)\mu_B(x)dx + \int_{W_E''}^{W_B} N_B(x)\mu_B(x)dx \tag{3.3}$$

and substituting from equations 3.1 and 3.2 into 3.3 yields,

$$\frac{1}{qR_{IB}} = \int_0^{W_E''} N_B(x)\mu_B(x)dx + \frac{1}{qR_{UE}} \tag{3.4}$$

Since in most high performance bipolar processes the emitter is shallow ($\leq$0.1μm), this leads to the approximation $W_E''<<W_B$. Moreover, for the transistors considered in this study, the base profile is gaussian with the peak in the concentration profile situated at the silicon surface (x=0). Hence in the range x=0 to W_E'' the base doping is approximately constant and near its peak value, N_{Bpeak} (the validity of this assumption is discussed in more detail in the next section). Using these assumptions the integral in equation 3.4 can be simplified to,

$$\int_0^{W_E''} N_B(x)\mu_B(x)dx \approx W_E''N_{Bpeak}\mu_{Bpeak} = \frac{1}{q}\left[\frac{1}{R_{IB}} - \frac{1}{R_{UE}}\right] \tag{3.5}$$

and so,

$$W_E'' = \frac{1}{qN_{Bpeak}\mu_{Bpeak}}\left[\frac{1}{R_{IB}} - \frac{1}{R_{UE}}\right] \tag{3.6}$$

where μ_{Bpeak} is the majority carrier mobility at a doping concentration of N_{Bpeak}. Therefore, by measuring the sheet resistances R_{IB} and R_{UE}, and from a knowledge of the base profile, W_E'' can be easily calculated using the analytical expression in equation 3.6. If more accuracy is required and/or the base profile cannot be considered to be uniform close to the surface (i.e. the emitter is deep), it is still a relatively simple matter to numerically solve the integral in equation 3.4 to obtain the emitter depth.

To extract the actual metallurgical emitter depth, W_E' from W_E'', a value for the depletion depth into the base is required. This can either be extracted from a junction capacitance measurement, or as in the case of the devices discussed here, it is calculated directly form the profile using Poisson's equation and applying the depletion approximation.

3.3 Accuracy

Typical emitter depths for polysilicon contacted emitters used as diffusion sources are around 0.03 to 0.1μm. Over this range the base profile would be expected to fall in concentration by perhaps as much as 50% for shallow bases. At first sight this seems

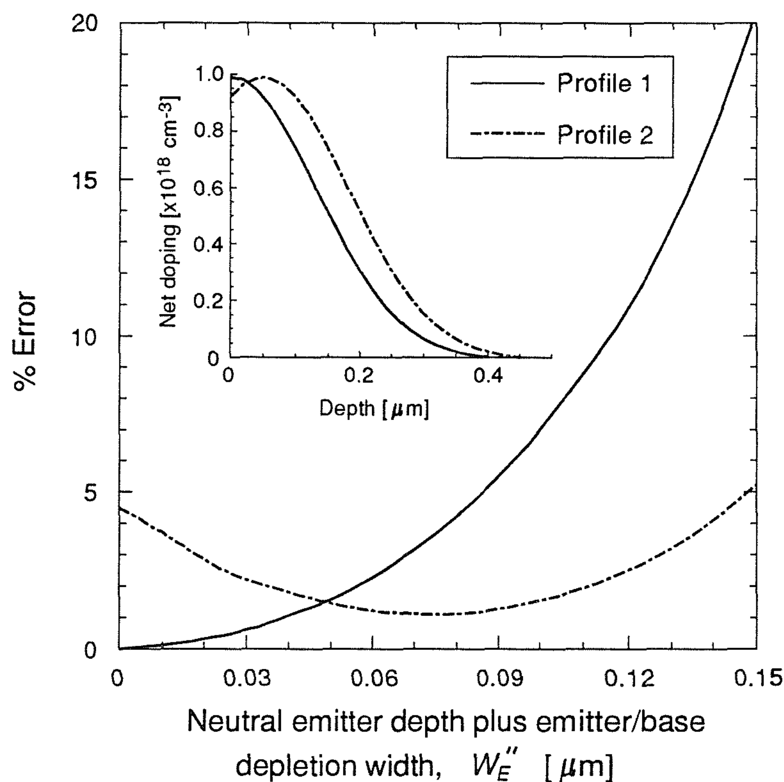

Fig. 3.3 Percentage error in using the approximation from equation 3.5 as a function of the neutral emitter depth plus the emitter/base depletion width, W_E'' for two typical base profiles which are shown in the inset.

an excessive error for the approximation used in equation 3.5. However, it must be remembered that it is the function $N_B\mu_B$ that is of interest, and not N_B. It is well known experimentally that the mobility of carriers vary as the inverse of doping concentration (i.e. mobility falls as doping increases). To put this more quantitatively (using the mobility data of Masetti *et al.* [7] for boron doped silicon) fig. 3.3 shows the percentage error in using the simplification in equation 3.5 as a function of neutral emitter depth, W_E'' for two base profiles. The first base profile is typical of that used for the devices in this study, whilst the second is typical of a base implant into bare silicon (inset of fig. 3.3). It can be seen that the error for profile 1 is around 20% for a 0.15μm junction depth but falls dramatically to less than 5% for junctions shallower than 0.09μm. The error for profile 2 remains under 6% for junction depths up to 0.15μm.

3.4 Experimental procedure

Table 3.1 summarises the processing conditions for the transistors used in this study. The bases of both the *npn* and *pnp* transistors were fabricated by direct ion-implantation through a 800Å screen oxide; the *npn* devices receiving a boron implant of dose 2×10^{13} cm^{-2} at 40keV energy, followed by an anneal at 950°C in dry N_2 for 30 minutes, and the *pnp* devices receiving a phosphorus implant of dose 2×10^{13} cm^{-2} at 80keV energy, followed by an anneal at 1000°C in dry N_2 for 30 minutes.

Device	Type	Base dopant	Emitter Dopant	Emitter Drive-in
1	*npn*	Boron	Phosphorus	10′ 900°C wet O_2
2	*npn*	Boron	Phosphorus	30′ 800°C wet O_2
3	*pnp*	Phosphorus	BF_2	60′ 850°C dry N_2
4	*pnp*	Phosphorus	BF_2	60′ 850°C wet O_2
5	*pnp*	Phosphorus	BF_2	60′ 850°C wet O_2
6	*pnp*	Phosphorus	BF_2	120′ 850°C dry N_2
7	*pnp*	Phosphorus	BF_2	120′ 850°C dry N_2
8	*pnp*	Phosphorus	BF_2	120′ 850°C wet O_2
9	*pnp*	Phosphorus	BF_2	180′ 850°C dry N_2
10	*pnp*	Phosphorus	BF_2	240′ 850°C dry N_2
11	*pnp*	Phosphorus	BF_2	240′ 900°C dry N_2

Table 3.1 Summary of processing conditions for the transistors used in this study.

After the opening of the emitter window, un-doped amorphous silicon was then deposited by LPCVD, at a temperature of 560°C. The emitter dopant was then implanted into the polysilicon; the *npn* devices receiving a phosphorus implant of dose $1x10^{16}$ cm^{-2} at 50keV energy, and the *pnp* devices receiving a BF_2 implant of dose $1x10^{16}$ cm^{-2} at 70keV energy. The subsequent high temperature drive-ins were chosen to give a wide range of junction depths (0 to 0.2μm) so that the electrical method could be fully tested. Both secondary ion mass spectroscopy (SIMS) and spreading resistance (SR) analysis were performed on a selection of the devices.

3.5 Results and discussion

3.5.1 Emitter junction depth

Typical SIMS results are shown in fig. 3.4(a) for the *npn* base profile and fig. 3.4(b) for the *pnp* base profile, and typical spreading resistance results are shown in fig. 3.5 for a *pnp* device. In order to obtain an accurate value for the emitter/base junction depth, it is crucial to achieve a good fit between the measured intrinsic base sheet resistance, R_{IB} and the simulated sheet resistance (from integrating the base profile and majority carrier mobility). The SIMS technique only provides the chemical concentration profile, which can be substantially different to the desired electrically active concentration profile. By integrating the base SIMS profiles in fig. 3.4 (using the

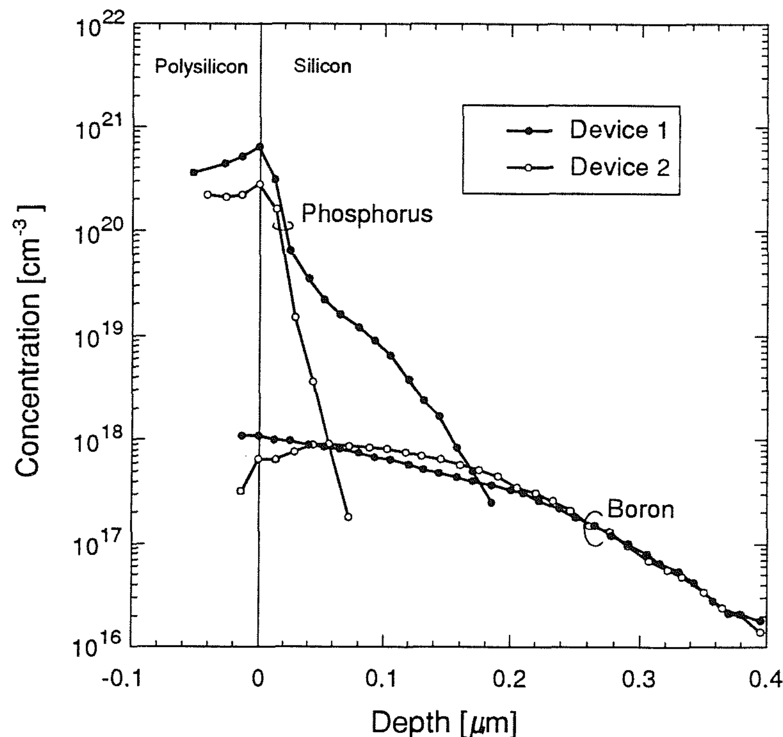

Fig. 3.4(a) Typical SIMS emitter and base profiles for the *npn* devices used in this study (devices 1 and 2).

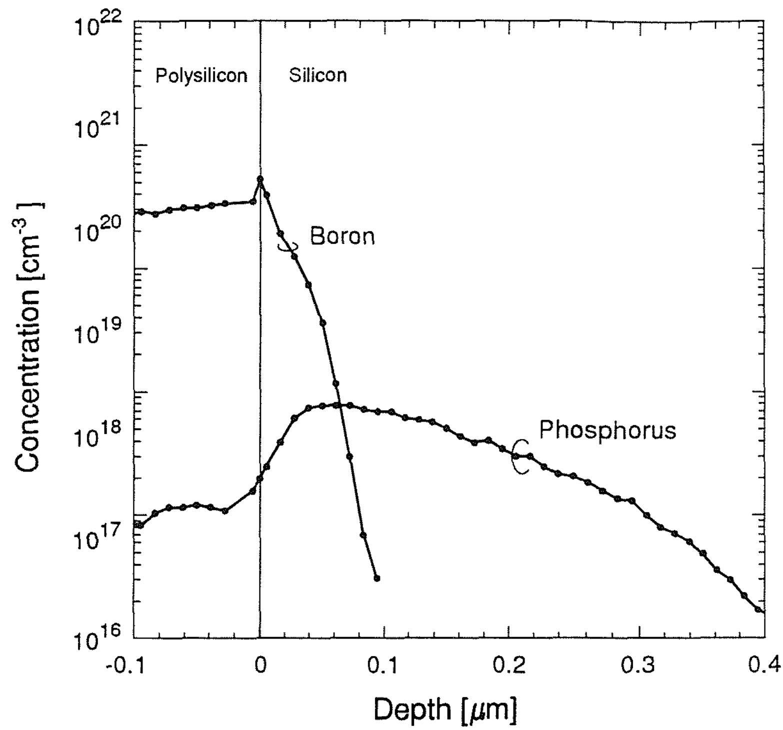

Fig. 3.4(b) Typical SIMS emitter and base profile for the *pnp* devices used in this study (device 7).

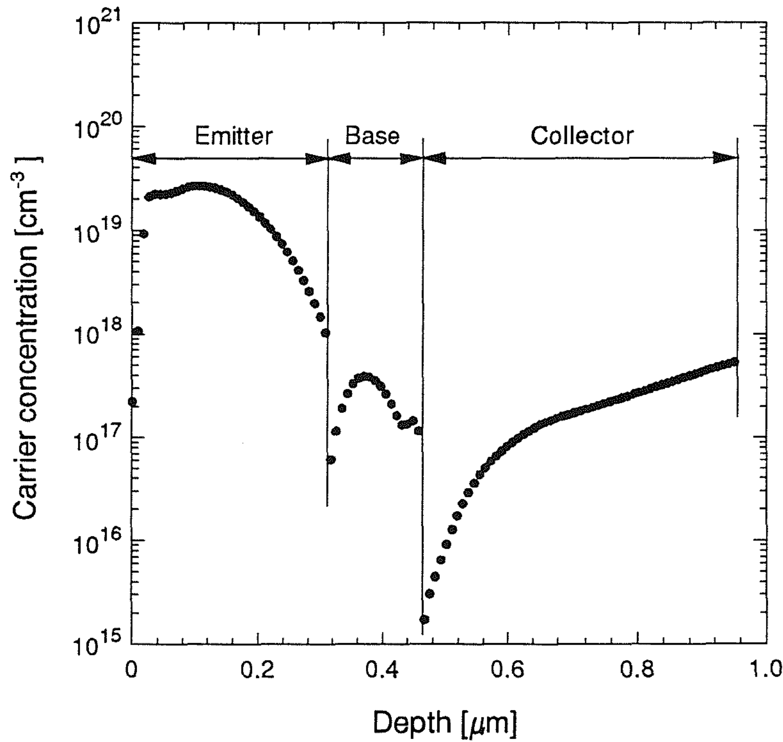

Fig. 3.5 Typical SR profile for the *pnp* devices used in this study (device 4).

mobility data of Masetti *et al.* [7]), simulated values for R_{IB} of around 2.0 kΩ/□ for *npn* devices, and 1.2 kΩ/□ for *pnp* devices are obtained. These results compare with measured values of 2.6–2.9 kΩ/□ for *npn* devices, and 1.6–2.0 kΩ/□ for *pnp* devices (see table 3.2), which implies incomplete activation of the base dopant for both types of devices. Delfino *et al.* [8] have discovered a much reduced electrical base profile, with a 46% reduction in peak doping and a 42% reduction in base depth compared with SIMS, for a base implant of 4×10^{13} cm^{-2} B^+ at an energy of 20keV (through a 300Å screen oxide), followed by a drive-in for 20 minutes at 875°C in N_2. This processing is similar to the devices in this study, and so it therefore seems reasonable that in order to obtain a fit between measured and simulated base sheet resistances, the peak base doping and base depth can be reduced by equal percentages from the SIMS values. Table 3.2 shows that reductions in the SIMS base profile in the range 9–28% allow a good fit between the simulated and measured base sheet resistance.

The fitted base profile was then integrated, and the required value of W_E'' was found which would satisfy the equality in equation 3.4. The metallurgical emitter depth,

Device	R_{IB} (meas) [kΩ/□]	N_{Bpeak} (fit) [cm^{-3}]	W_B (fit) [μm]	% decrease in SIMS base profile
1	2.9±0.2	7.5×10^{17}	0.332	21
2	2.63±0.06	8.0×10^{17}	0.353	16
3	1.62±0.03	7.0×10^{17}	0.330	17
4	1.63±0.04	7.0×10^{17}	0.328	18
5	1.54±0.03	7.6×10^{17}	0.356	11
6	1.57±0.03	7.1×10^{17}	0.336	16
7	1.48±0.03	7.7×10^{17}	0.364	9
8	1.43±0.02	7.6×10^{17}	0.356	11
9	1.52±0.02	7.4×10^{17}	0.350	12
10	1.50±0.03	7.6×10^{17}	0.356	11
11	2.01±0.08	6.1×10^{17}	0.288	28

Table 3.2 Fitted base profile peak concentration and depth to the measured intrinsic base sheet resistance (R_{IB}). Also shown is the overall percentage reduction of the SIMS base profile in order to fit the measured sheet resistance.

W_E' (elec) was calculated by subtracting the extent of the depletion width into the base (as calculated by numerical integration), from the neutral emitter depth W_E''. Table 3.3 shows the value of W_E' (elec) obtained in this way for the devices used in this study, as well as the emitter junction depths obtained from the SIMS and SR analysis.

Device	R_{UE} (meas) [kΩ/□]	W_E' (elec) [μm]	W_E' (SIMS) [μm]	W_E' (SR) [μm]
1	60±40	0.174	0.172	–
2	2.73±0.06	0	0.057	–
3	2.27±0.05	0.050	–	0
4	2.56±0.03	0.025	0.031	–
5	2.22±0.08	0.029	0.055	–
6	2.66±0.03	0.036	0.082	–
7	2.78±0.14	0.059	0.055	0.045
8	3.23±0.09	0.080	0.064	0.115
9	4.14±0.35	0.087	–	0.088
10	4.80±0.4	0.104	–	0.080
11	13±2	0.102	0.107	–

Table 3.3 Comparison of emitter depths obtained by the electrical method, SIMS, and SR. Also shown is the measured pinched base sheet resistance (R_{UE}).

Table 3.3 shows that excellent agreement is achieved between the electrical method and SIMS for the deeper junctions (devices 1 and 11), but there are serious discrepancies for the shallow junctions (most notably devices 2, 5 and 6), where the SIMS analysis produces consistently deeper junctions compared to the electrical method. This indicates that the resolution of the SIMS technique is inadequate for junction depths shallower than 0.1μm. Support for this conclusion can be obtained by considering the electrical characteristics of device 2 (fig. 3.6), which yielded an emitter depth of zero from the electrical method, whilst the SIMS analysis shows that the emitter junction depth is around 0.06μm. The base characteristic of this device exhibits a well defined 'kink' [9], which is symptomatic of SIS (semiconductor-insulator-semiconductor) behaviour, in which there is negligible penetration of dopant into the single-crystal emitter.

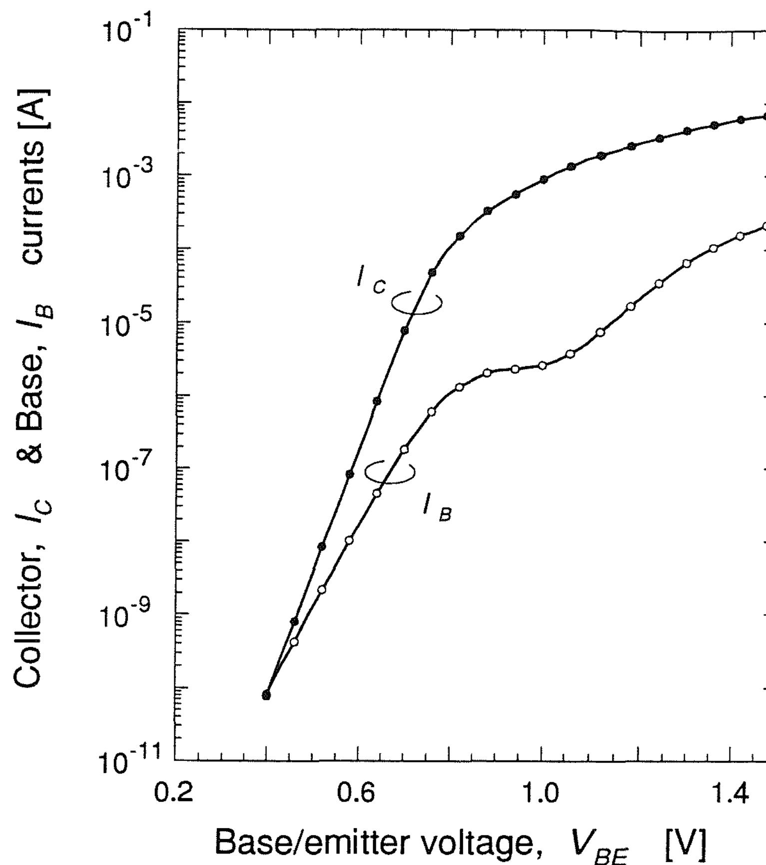

Fig. 3.6 Gummel plot for device 2 exhibiting a 'kink' which is characteristics of SIS emitter behaviour [9].

Also shown in table 3.3 are the emitter depths as obtained from spreading resistance (SR) analysis. Generally, the agreement between the emitter depths as obtained from the electrical method and SR is extremely good, especially for emitter junction depths less than 0.1μm. However, it must be noted that it is extremely difficult to extract single-crystal emitter depths from spreading resistance profiles since there is normally no indication as to where the polysilicon/silicon interface occurs (see fig. 3.5). Furthermore, spreading resistance analysis suffers from the phenomenon of 'carrier spilling' [4], whereby the junction depth as obtained from SR is less than that of the real metallurgical junction.

3.5.2 Modelling of collector currents

To further substantiate the results obtained for the junction depths, the measured collector current was compared with that modelled from SIMS (using the SIMS base profile and SIMS emitter depth) and that modelled from the electrical method (using the fitted base profile and electrical emitter depth). The base profile from the spreading resistance analysis was not used since the profile is unreliable [10]. This modelling

provides a good validation of the electrical method since the collector current depends on the base profile, base depth, and emitter depth. In order to obtain predictions of collector current, empirically fitted models for carrier mobility and band-gap narrowing are required. Table 3.4 shows the measured collector current density, and the corresponding modelled collector current density, from the SIMS and electrically measured base and emitter profiles. The band-gap narrowing and mobility data is from Slotboom *et al.* [11] and Arora *et al.* [12] respectively. It can be clearly seen that the electrical method provides a good fit to the measured collector current, which in nearly all cases is closer than the modelled current from the SIMS profile data. This at least indicates the validity of the electrical method for providing junction depths for use in modelling.

Device	J_{CO}(meas) [A cm^{-2}]	J_{CO}(SIMS) [A cm^{-2}]	J_{CO}(elec) [A cm^{-2}]
1	4.6x10^{-10} †	1.7x10^{-10} †	5.8x10^{-10} †
2	3.5x10^{-11} †	4.6x10^{-11} †	4.1x10^{-11} †
3	2.8x10^{-11}	–	2.3x10^{-11}
4	1.6x10^{-11}	2.5x10^{-11}	3.4x10^{-11}
5	3.0x10^{-11}	–	2.3x10^{-11}
6	2.2x10^{-11}	4.1x10^{-11}	3.7x10^{-11}
7	4.5x10^{-11}	3.3x10^{-11}	3.0x10^{-11}
8	5.7x10^{-11}	3.6x10^{-11}	4.2x10^{-11}
9	6.3x10^{-11}	–	4.9x10^{-11}
10	8.6x10^{-11}	–	6.1x10^{-11}
11	2.2x10^{-10}	5.7x10^{-11}	2.1x10^{-11}

Table 3.4 Measured collector current density (with V_{CB}=5V) of the devices used in this study. The modelled collector current density is obtained from the SIMS and electrically measured base and emitter profiles. The band-gap narrowing and mobility data is from Slotboom *et al.* [11] and Arora *et al.* [12] respectively (devices marked † are measured and modelled with V_{CB}=0V).

Recent work by del Alamo *et al.* [13] and Swirhun *et al.* [14] have shown that at high doping concentrations, the minority carrier mobility can be up to a factor of two larger than the corresponding majority carrier mobility, as measured by Arora *et*

al. [12] and used for modelling the collector currents in table 3.4. Moreover, del Alamo and Swirhun also measured simultaneously the band-gap narrowing, minority carrier mobility, and minority carrier lifetime on the same silicon sample. Table 3.5 shows the measured collector current density, and the corresponding modelled collector current density, from the SIMS and electrically measured base and emitter profiles, using the band-gap narrowing and minority carrier mobility data from del Alamo *et al.* [13] and Swirhun *et al.* [14]. Again the modelled collector current from the electrical method provides a better fit to the measured collector current than that from the SIMS profiles. However, on comparison with table 3.4 the modelled collector currents using the data from the Slotboom/Arora model still provide a better fit to experiment than the data from the del Alamo/Swirhun model. A Possible explanation for this discrepancy could be the silicon material on which the experiments are performed. Del Alamo and Swirhun used epitaxially grown *in-situ* doped silicon, whereby the bases for the devices in this study were fabricated from ion-implanted and diffused layers.

Device	J_{CO}(meas) [A cm^{-2}]	J_{CO}(SIMS) [A cm^{-2}]	J_{CO}(elec) [A cm^{-2}]
1	4.6×10^{-10} †	1.8×10^{-10} †	6.2×10^{-10} †
2	3.5×10^{-11} †	5.3×10^{-11} †	4.9×10^{-11} †
3	2.8×10^{-11}	–	1.4×10^{-11}
4	1.6×10^{-11}	1.4×10^{-11}	1.9×10^{-11}
5	3.0×10^{-11}	–	1.5×10^{-11}
6	2.2×10^{-11}	2.6×10^{-11}	2.2×10^{-11}
7	4.5×10^{-11}	2.0×10^{-11}	1.9×10^{-11}
8	5.7×10^{-11}	2.2×10^{-11}	2.9×10^{-11}
9	6.3×10^{-11}	–	3.5×10^{-11}
10	8.6×10^{-11}	–	4.5×10^{-11}
11	2.2×10^{-10}	4.0×10^{-11}	1.8×10^{-11}

Table 3.5 Measured collector current density (with V_{CB}=5V) of the devices used in this study. The modelled collector current density is obtained from the SIMS and electrically measured base and emitter profiles. The band-gap narrowing and mobility data is from del Alamo *et al.* [13] and Swirhun *et al.* [14] respectively (devices marked † are measured and modelled with V_{CB}=0V).

Recently Popp *et al.* [15] have investigated the use of band-gap narrowing and mobility models in simultaneously modelling the DC and high-frequency AC behaviour of *npn* polysilicon emitter transistors. They found, as in this study, that the Slotboom/Arora model provided a better fit to the collector current than the del Alamo/Swirhun model. However, they also showed that the del Alamo/Swirhun model provided a better fit to the forward transit time than the Slotboom/Arora model. To correct this disparity, Popp *et al.* [15] proposed a compromise whereby the del Alamo *et al.* [13] value for band-gap narrowing would be used for *both* *n*– and *p*–type silicon, with the minority carrier mobility of del Alamo *et al.* [13] for *n*–type silicon and Swirhun *et al.* [14] for *p*–type silicon. This compromise resulted in modelled DC and AC values within 30% of the measured values. Recently, the approach of Popp *et al.* [15] has been partially corroborated by the work of King *et al.* [16] who re-measured band-gap narrowing in *p*–type silicon using a novel contactless photoconductivity decay method. They found the band-gap narrowing in *p*–type silicon to be approximately mid-way between the original value from Swirhun *et al.* [14], and the value from del Alamo *et al.* [13] for *n*–type silicon. These recent conflicting results indicate that further experimental and theoretical work is needed to clarify the band-gap narrowing, mobility and lifetime models required for heavily doped silicon.

Further controversy has also recently materialised on the value of intrinsic carrier concentration in silicon, n_{io}, which is an important parameter for modelling the base and collector currents in bipolar transistors [17] (both collector and base currents vary as the *square* of the intrinsic carrier concentration). Recent measurements of the intrinsic carrier concentration by Green *et al.* [18] and Sproul *et al.* [19] have shown that the commonly accepted value for n_{io} of 1.45×10^{10} cm^{-3} [20] (at 300K) is overestimated by approximately 30-40%, giving possible errors in the modelled collector and base currents of between a factor of 1.5–2. The value of n_{io} used in this chapter is from Swirhun *et al.* [21] (who uses the commonly accepted value), and so should be consistent with the band-gap narrowing models of del Alamo *et al.* [13] and Swirhum *et al.* [14] (although del Alamo and Swirhun do not explicitly give the model they use for n_{io} in either [13] or [14]). This intrinsic carrier concentration model [21] is also partly valid for the Slotboom model (and so the modelled collector currents in table 3.4 and 3.5 are still valid), although close inspection of [11] reveals that Slotboom assumes that the value of n_{io} is a weak function of doping concentration (essentially to improve the fit between the band-gap narrowing model and the experimental data). These controversies mean that *all* minority carrier parameters in silicon need to be re-examined, and a consistent set put forward.

3.6 Conclusions

A simple electrical method to measure the electrically active emitter depth of shallow bipolar transistors has been presented in a simple analytical form. When compared with conventional methods, such as SIMS, it has shown itself to be comparable in accuracy for deep junctions, and to be more accurate for shallow junctions. Modelling of the collector current has validated the electrical method over that of SIMS. Furthermore, the band-gap narrowing data of Slotboom *et al.* [11] and majority carrier mobility of Arora *et al.* [12] has been shown to provide a better fit to the experimental data than the band-gap narrowing and minority carrier data of del Alamo *et al.* [13] and Swirhun *et al.* [14].

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Chapter 4

Investigation of Boron Diffusion in Polysilicon and its Application to the Design of *PNP* Polysilicon Emitter Bipolar Transistors with Shallow Emitter Junctions

4.1 Introduction

Polysilicon can be used not only to produce devices with enhanced gain (polysilicon emitter bipolar transistors) [1]–[3], but also as a diffusion source for both emitter and base fabrication [4], [5]. This results in very shallow, defect free base/collector and emitter/base junctions, and so permits a corresponding reduction in lateral dimensions, which improves packing density. This technique can also result in very narrow base widths, and therefore enhance the high-frequency device performance. Diffusion from polysilicon is also routinely used in self-aligned techniques [6], [7] for high-speed bipolar technologies, where it allows reductions of base/collector capacitance and extrinsic base resistance, and hence improvements in circuit performance. Both double diffusion [8] and self-aligned techniques [9] use boron doped polysilicon as an integral part of the process.

Up until the present time the study of polysilicon emitter contacts has been almost wholly confined to *npn* structures. For high-speed applications this choice is quite natural, since the minority carrier electron mobility in silicon is larger than the minority carrier hole mobility in silicon. However, recent work by Lu *et al.* [10], [11] and Warnock *et al.* [12]–[14] have shown that acceptable current gains and high frequency performance can be achieved for *pnp* polysilicon emitter transistors without a deliberately grown interfacial oxide layer. The study of vertical *pnp* polysilicon emitter bipolar transistors is therefore important, not only for analogue, complimentary and BiCMOS applications [15]–[17], but also in that they allow the physics of the polysilicon/silicon interface to be studied through its interaction with the opposite type charge carrier [18].

The majority of the reported work in the literature on *pnp* polysilicon emitter bipolar transistors with deliberately grown interfacial oxide layers [19], [20], has concentrated on *in-situ* boron doped polysilicon. Devices with no emitter anneal were produced, whereby the dopant penetration into the single-crystal silicon was negligible. These devices are unsuitable for exploitation because of their very non-ideal base currents and saturation of collector and base currents at low forward bias. Also, annealed devices were fabricated, which used the *in-situ* boron doped polysilicon as the diffusion source for the single-crystal emitter. A large improvement was obtained in the device characteristics, resulting in ideal collector and base currents and much improved high current behaviour, but at the expense of a large increase in emitter junction depth (>0.15μm) [19]. The *in-situ* doped devices with deliberately grown interfacial oxide layers [19] showed that a reduction in base current by a factor of 2 could be realised, but at the expense of an increase in emitter resistance by a factor of about 2. From a production point of view it would be expected that devices fabricated by ion-implantation, rather than *in-situ* doping, are much preferred because of the easier

control of batch-to-batch variability. It is also important to study devices with emitter junction depths shallower than the 0.15μm reported in [19], since the full benefits of polysilicon emitters, such as improved gains, are only obtained for junction depths less than 0.1μm.

In this chapter ion-implantation of boron into un-doped polysilicon is utilized, an approach which is analogous to that currently used in the fabrication of arsenic doped *npn* polysilicon emitters. The main goals of this chapter are to characterise the diffusion of implanted boron from polysilicon, and to correlate the diffusion behaviour with the electrical properties of shallow (<0.05μm) *pnp* polysilicon emitter bipolar transistors. It is shown that diffusion and electrical activity problems are encountered with boron polysilicon emitters which are not present with arsenic. These make it extremely difficult to simultaneously obtain emitter/base junction depths of <0.05μm and high activation levels at the polysilicon/silicon interface of $>3\text{x}10^{19}$ cm^{-3}.

4.2 Experimental Procedure

Secondary ion mass spectroscopy (SIMS) was used to study the influence of various implantation doses and drive-in temperatures on junction depths and polysilicon doping levels. Samples consisted of un-patterned wafers of 1 Ωcm resistivity, which received a dip etch in hydrofluoric acid (HF) immediately prior to deposition of 0.4μm of un-doped LPCVD amorphous silicon at 560°C. The wafers next received an implant of BF_2 ions at an energy of 70 keV, and doses of either $2.5\text{x}10^{15}$, $5.0\text{x}10^{15}$, or $1.0\text{x}10^{16}\ \text{cm}^{-2}$. A capping low temperature oxide was then deposited before the wafers received a drive-in for 60 minutes in dry nitrogen at temperatures of either 850, 900, or 950°C. The SIMS analysis used O_2^+ primary ion bombardment, and positive secondary ion detection to optimise boron sensitivity. The depth profile was calibrated against as-deposited polysilicon thickness, and the boron concentration profile was calibrated against the implantation dose on an as-implanted sample. SUPREM III modeling of the doping profiles was then performed, and diffusivities of boron in polysilicon and silicon were extracted.

The implantation of BF_2 was preferred over that of boron for two main reasons. Firstly, the ionisation energy of the BF_2 ion is lower than that of boron, and so it is easier to implement the high doses required (the BF_2 ion produces considerably larger beam currents). Secondly, the implant range of the BF_2 ion can be easily controlled down to 0.05μm (and so the as-implanted profile is similar to conventional shallow arsenic implants). However, the achievement of this range using boron is impossible using the Southampton University Microelectronics Centre ion-implanter. The minimum

boron energy achievable with this implanter, for a dose of $1x10^{16}$ cm^{-2}, is approximately 50 keV, producing a range of 0.16μm, which is unsuitable for the formation of shallow junctions.

All electrical devices used in this study received identical processing up to and including the base fabrication (see Appendix 2 for full *pnp* processing details). The silicon interfacial layer was characterised either by an HF dip etch (to remove any native oxide) or an RCA clean (to grow a thin oxide of thickness 14±2Å). Un-doped LPCVD amorphous silicon at a temperature of 560°C and thickness 0.4μm was then deposited immediately after surface preparation. The emitter was then formed by implanting BF_2 ions of 70 keV energy, and a dose of $1.0x10^{16}$ cm^{-2}. The amorphous silicon was then capped with a low temperature oxide, and an anneal at 850°C in dry nitrogen for either 60, 120, 180, or 240 minutes was then performed to uniformly dope the polysilicon, and form a shallow single-crystal emitter.

The electrically active boron doping profiles were measured using spreading resistance (SR) on actual device wafers, so that direct correlation could be made between the profiles and electrical results. A majority carrier mobility model for *p*–type single-crystal silicon was used to extract the carrier profiles for the emitter. This model may underestimate the doping concentration in the polysilicon by at most a factor of 2 [21], but will give the correct doping concentration in the single-crystal silicon and at the interface. However, if a large discrepancy in mobility does exist between the polysilicon and single-crystal silicon, then it would be expected that the measured carrier concentration would show a discontinuity across the interface. This was not observed in the results, and so therefore the use of a single-crystal hole mobility for the polysilicon layer is reasonable. To further quantify the emitter profiles, the junction depths of the devices were measured using the electrical method described in chapter 3 [22], which compares the base sheet resistance both with and without an emitter diffusion. Detailed electrical measurements were made on the collector and base currents as a function of base/emitter voltage (Gummel plots, see Appendix 3), which were then correlated to the doping profiles.

4.3 Results

4.3.1 SIMS results

Fig. 4.1 shows the boron SIMS profile for polysilicon implanted at a dose of $1x10^{16}$ cm^{-2}, and driven-in for 60 minutes in dry nitrogen at a temperature of either 850, 900 or 950°C. Also shown in fig. 4.1 is the as-implanted profile. The most prominent feature of all the profiles is the peak occurring near the polysilicon surface at a depth of 0.05μm. The position of this peak corresponds exactly with the peak of

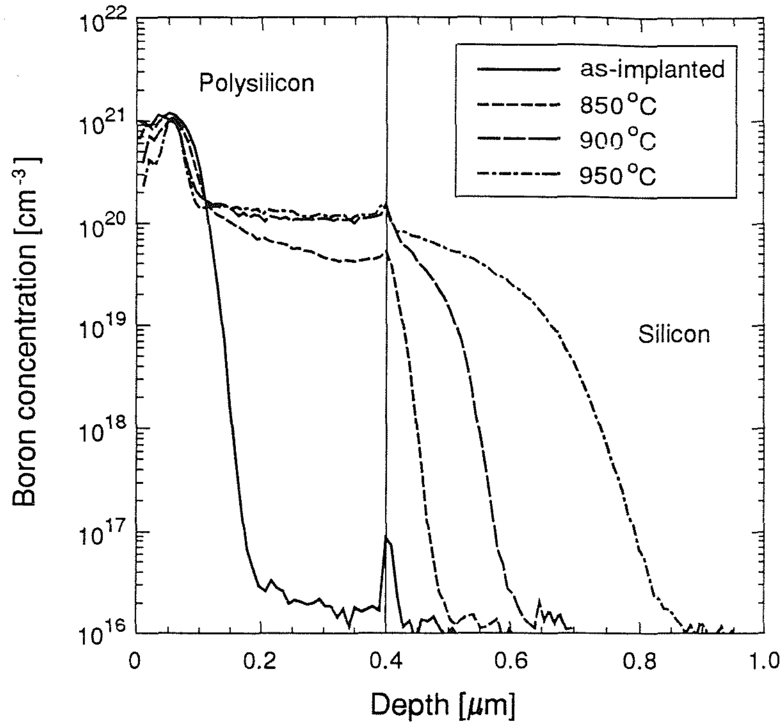

Fig. 4.1 SIMS boron profile for implanted BF_2 of dose 1×10^{16} cm^{-2}, driven-in for 60 minutes in dry nitrogen at temperatures of either 850, 900, or 950°C.

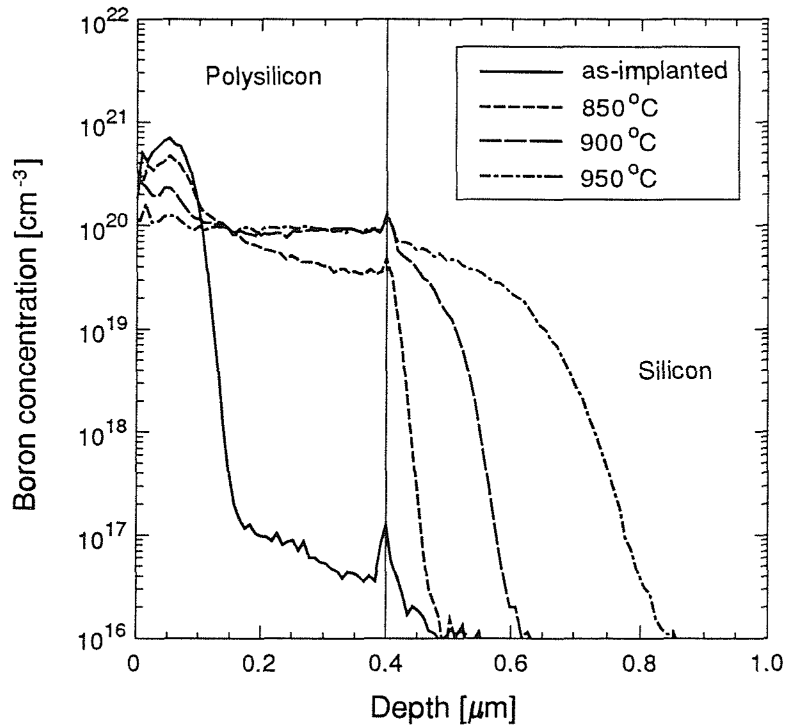

Fig. 4.2 SIMS boron profile for implanted BF_2 of dose 5×10^{15} cm^{-2}, driven-in for 60 minutes in dry nitrogen at temperatures of either 850, 900, or 950°C.

the as-implanted profile. From a depth of about 0.1 to 0.4μm (i.e. up to the polysilicon/silicon interface), the profile is relatively flat at a concentration of around 1.2×10^{20} cm^{-3} for the drive-ins at 900 and 950°C. For the 850°C drive-in the profile in the polysilicon is non-uniform, and shows a slight gradient, dropping in concentration from 1.2×10^{20} cm^{-3} at the edge of the surface peak, to a concentration of 4.2×10^{19} cm^{-3} near the polysilicon/silicon interface. At the interface all three drive-ins show a small segregation peak at a concentration of about 1.5×10^{20} cm^{-3} for the 900 and 950°C drive-ins, and 5.3×10^{19} cm^{-3} for the 850°C drive-in. The diffusion of the boron from the polysilicon into the underlying single-crystal silicon is characterised by gaussian-like profiles, with junction depths of 0.43, 0.20, and 0.09μm from the interface for the 950, 900, and 850°C drive-ins respectively.

Fig. 4.2 shows the boron SIMS profiles for identical processing conditions as in fig. 4.1, except for a reduction in implant dose by 50% to 5.0×10^{15} cm^{-2}. Again similar results are observed as in fig. 4.1, with the most prominent feature of the profiles being the surface peak at the as-implanted peak, although the peak has almost disappeared for the drive-in at 950°C. The 'plateau' region of the profile is flat at a concentration of 9×10^{19} cm^{-3} for the 900 and 950°C drive-ins. The 850°C drive-in again shows a non-uniform profile, with a gradient from about 1.1×10^{20} cm^{-3} at the edge of the surface peak down to a concentration of 4.3×10^{19} cm^{-3} near the polysilicon/silicon interface. A small segregation peak is again observed at the interface. The diffusion of the boron into the underlying single-crystal silicon is again characterised by gaussian-like profiles, with junction depths of 0.42, 0.20, and 0.08μm for the 950, 900, and 850°C drive-ins respectively. TEM analysis [23] of the polysilicon shows two very distinct regions. The first region from the surface down to a depth of 0.07μm consists of very small and heavily defective grains. This region almost exactly coincides with the surface peaks observed from the SIMS profiles. The second region, which extends from a depth of 0.07μm down to the polysilicon/silicon interface consists of large grained (~0.2μm) polysilicon. This second region coincides exactly with the 'plateau' region of the SIMS profiles.

Fig. 4.3 shows the boron SIMS profiles for identical processing conditions as in fig. 4.2, except for a reduction in implant dose by a further 50% to 2.5×10^{15} cm^{-2}. Again very similar results are observed as for figs. 4.1 and 4.2, except that the profiles for the 900 and 950°C drive-ins show the complete absence of any peak at the surface, with the boron concentration uniform across the polysilicon layer at a value of 5×10^{19} cm^{-3}. However, the 850°C drive-in profile still shows the presence of a peak at the surface, with a concentration gradient in the polysilicon which varies from

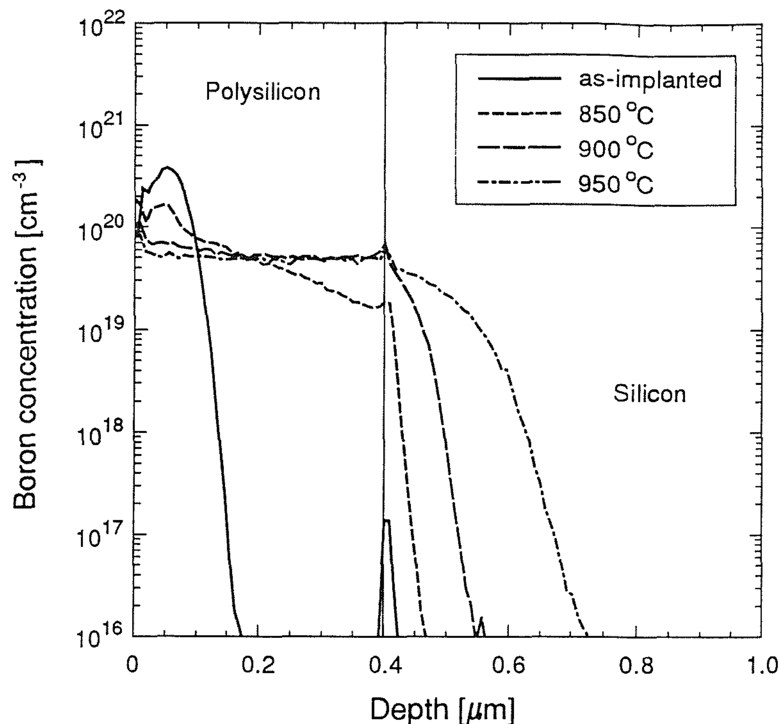

Fig. 4.3 SIMS boron profile for implanted BF_2 of dose $2.5\text{x}10^{15}$ cm^{-2}, driven-in for 60 minutes in dry nitrogen at temperatures of either 850, 900, or 950°C.

$9\text{x}10^{19}$ cm^{-3} at the edge of the surface peak, down to a value of $1.6\text{x}10^{19}$ cm^{-3} near the polysilicon/silicon interface. Again all three profiles show a small segregation peak at the interface, and the dopant penetration into the single-crystal silicon is characterised by gaussian-like profiles, with junction depths of 0.33, 0.14, and 0.06μm for the 950, 900, and 850°C drive-ins respectively.

4.3.2 Spreading resistance results

Fig. 4.4 shows the spreading resistance profiles for device wafers which were driven-in for either 60, 120, 180, or 240 minutes in dry nitrogen at 850°C. From the previous SIMS analysis it was decided to limit the drive-in temperature to 850°C to ensure that the emitter junction depth was shallower than 0.1μm.

For the 60 minute drive-in device, the electrically active profile is very non-uniform, with the concentration varying from $2\text{x}10^{19}$ cm^{-3} at the surface, and falling to zero at the emitter/base junction, which exists at the polysilicon/silicon interface. The devices driven-in for either 120, 180 or 240 minutes all show similar profiles. The main characteristic is a peak electrically active concentration of around $3\text{x}10^{19}$ cm^{-3}, which occurs at depths between about 0.1 to 0.2μm from the polysilicon surface. The electrically active profile then drops to a value between $1\text{–}2\text{x}10^{19}$ cm^{-3} near the polysilicon/silicon interface. Two of the profiles (180 and 240 minutes) show a small

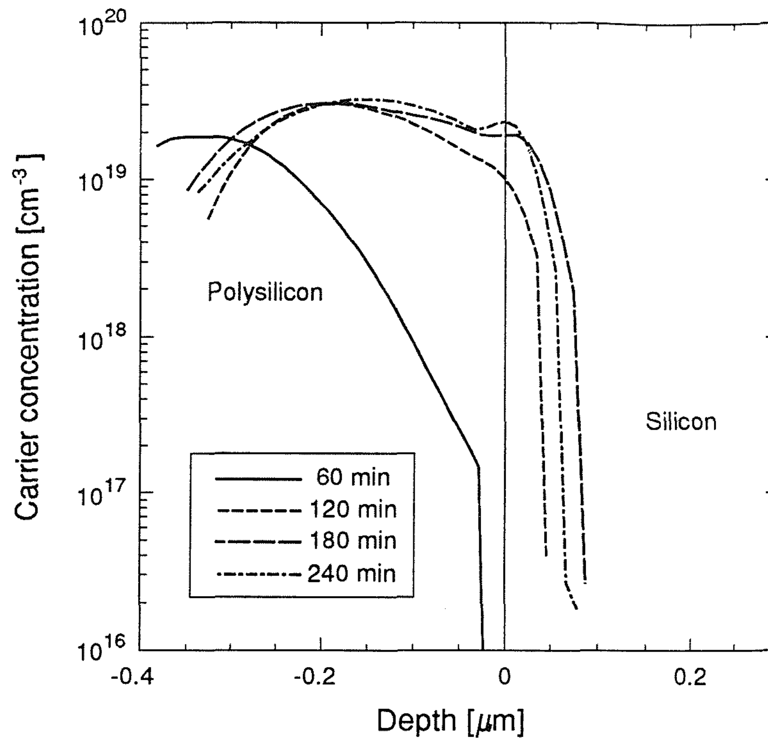

Fig. 4.4 Spreading resistance profiles for devices driven-in for 60, 120, 180, and 240 minutes in dry nitrogen at 850°C.

peak about 0.30 to 0.35μm from the polysilicon surface, which has been identified as the polysilicon/silicon interface [24]. The profiles then show dopant penetration into the single-crystal silicon, indicating that the emitter/base junctions reside at depths of 0.046, 0.087, and 0.079μm from the interface for devices driven-in for either 120, 180, or 240 minutes respectively.

The emitter/base junction depths extracted from fig. 4.4 are summarised in table 4.1. Also included in table 4.1 are the junction depths of the devices which were

Emitter Drive-in time [min]	Emitter Depth [μm] (Elec)	Emitter Depth [μm] (SR)
60	0.005	0
120	0.059	0.046
180	0.087	0.087
240	0.104	0.079

Table 4.1 Measured emitter junction depths using the electrical method outlined in [22] (Elec), and from spreading resistance (SR).

measured using the electrical method described in chapter 3 [22]. As can be seen there is reasonable agreement between the two techniques, with both showing that increases in drive-in time result in an increased junction depth.

4.3.3 Electrical results

Measurements of collector and base current density against base/emitter voltage (Gummel plots) are shown in fig. 4.5 for HF and RCA devices, which were driven-in for 60 minutes in dry nitrogen at 850°C. The HF device is characterised by a non-ideal base current (ideality factor of 1.6) at low values of base/emitter voltage. Similarly the RCA device also has a non-ideal (n=1.6) base current at low base/emitter voltages (V_{BE}<0.7 Volts), although the magnitude of the base current is a factor of 4 lower than the corresponding HF device. Since the only difference between the two devices is the deliberately grown interfacial oxide, this indicates that the oxide layer provides a blocking barrier for minority carrier electron injection into the emitter. Between a base/emitter voltage of 0.8 to 1.2 Volts the base current of the RCA device exhibits a 'kink', which is independent of base/collector voltage. Furthermore, the collector

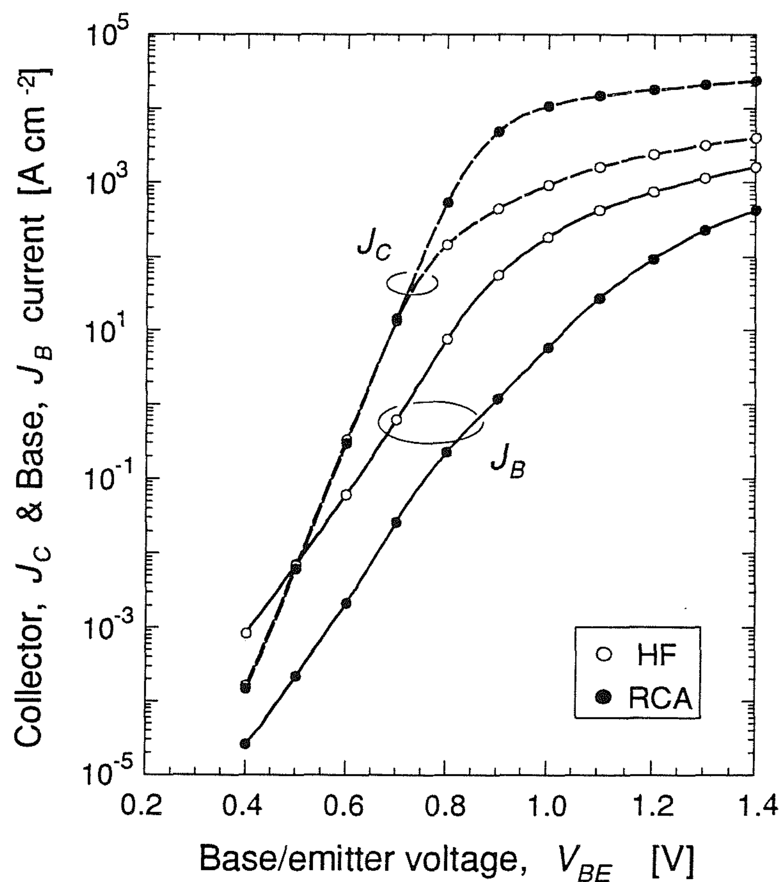

Fig. 4.5 Gummel plot of devices with a HF or RCA interfacial treatment, followed by an emitter drive-in of 60 minutes in dry nitrogen at 850°C (V_{CB}=5V, T=295K, A_{EW}=10.8X10.8 μm^2).

current saturates at a very low value of ~10^3 Acm^{-2} for the RCA device, which compares with a value of $2x10^4$ Acm^{-2} for the HF device. Both the presence of the kink and the low saturation of the collector current are indicative of negligible penetration of dopant from the polysilicon into the single-crystal [25], and table 4.1 does indeed show an emitter depth of zero.

Fig. 4.6 shows the Gummel plot for devices with identical processing to that in fig. 4.5, but with a drive-in of 120 minutes in dry nitrogen at 850°C. The HF device displays an almost ideal base characteristic, with typical ideality factors of 1.02. The RCA device also shows a much improved base current (n=1.05–1.10), although a slight 'kink' can still be observed at high base/emitter voltage (V_{BE}~0.8 Volts). A reduction in base current by a factor of 10 can also be seen for the RCA device when compared to the HF device. The saturation of the collector currents is also much improved over that obtained for the 60 minute drive-in device.

The Gummel plots for devices driven-in for 180 minutes in dry nitrogen at 850°C are shown in fig. 4.7, and it can be seen that the base currents for both RCA and HF devices are ideal (n=1.02). By comparing with the spreading resistance profiles (fig. 4.4)

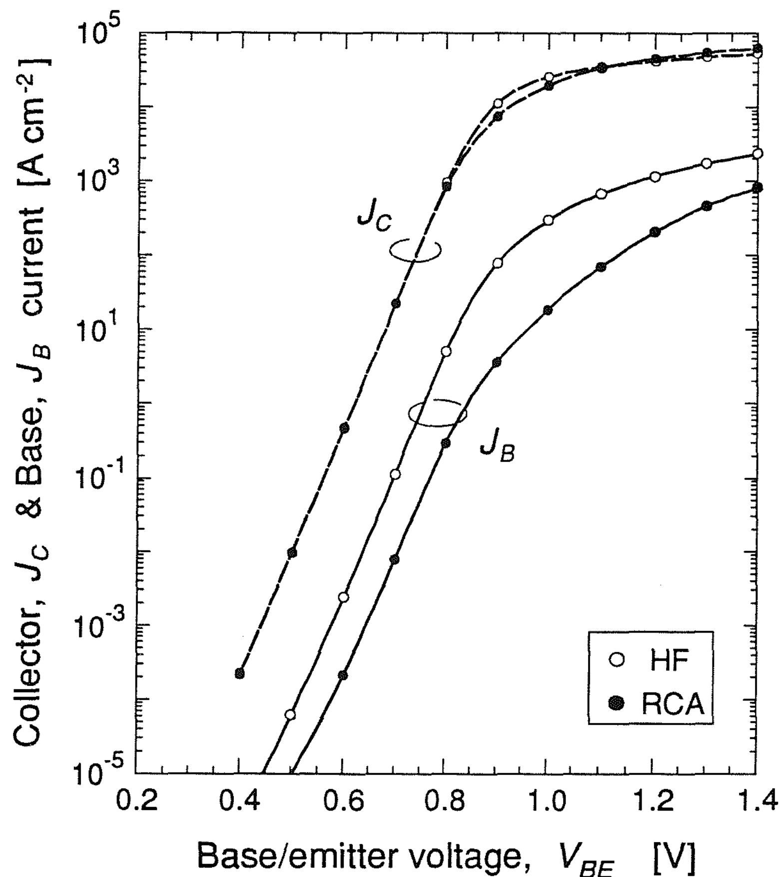

Fig. 4.6 Gummel plot of devices with a HF or RCA interfacial treatment, followed by an emitter drive-in of 120 minutes in dry nitrogen at 850°C (V_{CB}=5V, T=295K, A_{EW}=10.8X10.8 μm^2).

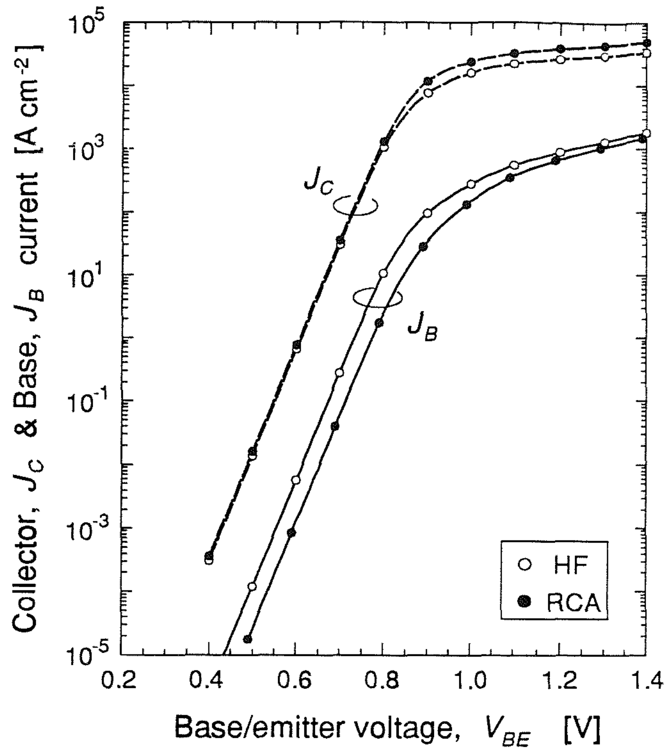

Fig. 4.7 Gummel plot of devices with a HF or RCA interfacial treatment, followed by an emitter drive-in of 180 minutes in dry nitrogen at 850°C (V_{BC}=5V, T=295K, A_{EW}=10.8X10.8 μm^2).

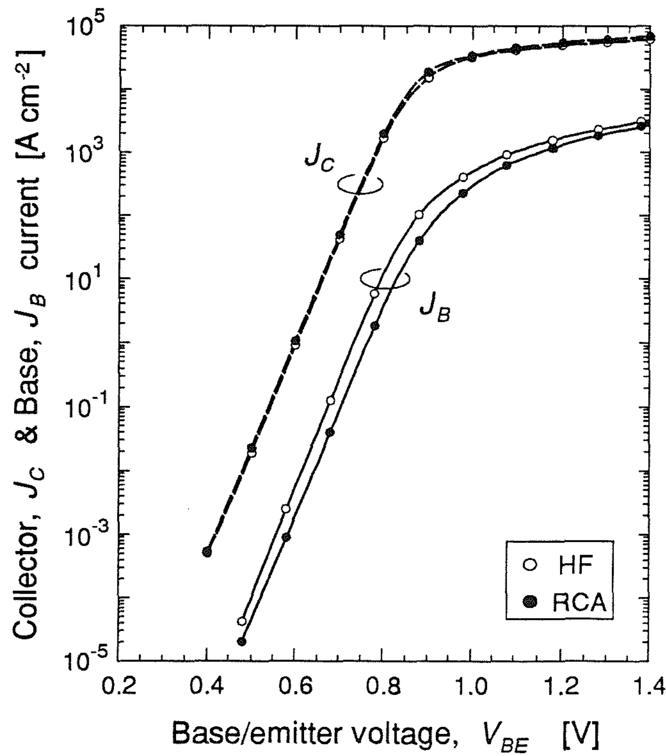

Fig. 4.8 Gummel plot of devices with a HF or RCA interfacial treatment, followed by an emitter drive-in of 240 minutes in dry nitrogen at 850°C (V_{BC}=5V, T=295K, A_{EW}=10.8X10.8 μm^2).

and emitter depth measurements (table 4.1) this is of no surprise since the emitter depths are deeper at 0.088µm, so that the emitter/base depletion region will reside entirely in the single-crystal silicon. Again a good base current reduction of a factor of 4 is obtained for RCA devices over HF devices. Very similar behaviour is also observed from the 240 minute drive-in devices (fig. 4.8), although the base current reduction for the RCA device is only a factor of 2 over that of the HF devices.

4.4 Discussion

The dopant peaks which occur at the polysilicon surface, corresponding in position to the as-implanted peak, are caused by boron precipitation. Similar studies in single-crystal silicon have shown the boron in these peaks to be immobile [26], [27] and electrically inactive [28]. Comparison of the SIMS profile (fig. 4.1) with the spreading resistance profile (fig. 4.4, 60 minute drive-in device) does indeed indicate that the precipitation peak is electrically inactive. This suggests that the majority of the implanted boron is unavailable to alter the electrical properties of the polysilicon. The maximum concentration of boron, before precipitation occurs (i.e. the solid solubility limit), can be defined to exist at the shoulder of the peak [27], and this analysis has been carried out on the SIMS profiles in figs. 4.1 to 4.3, with the results summarised in table 4.2. These indicate that for the drive-in temperatures studied (850–950°C), boron precipitation limits the boron concentration at the polysilicon/silicon interface to around $1–2\text{x}10^{20}$ cm^{-3}, with higher dose implants merely adding to the concentration of precipitated boron. This effect can be seen graphically in fig. 4.9 where the data from figs. 4.1 and 4.2 have been re-plotted on the same axis. As can be clearly seen, increasing the dose from $5\text{x}10^{15}$ to $1\text{x}10^{16}$ cm^{-2} has virtually no effect on the emitter profile. This behaviour differs markedly from that of arsenic in polysilicon, where an increase in arsenic dose generally results in an increase of doping level in the polysilicon, and an accompanying increase of emitter junction depth.

The solid solubility levels in table 4.2 compare with values in single-crystal silicon of approximately $3\text{x}10^{19}$, $6\text{x}10^{19}$, and $9\text{x}10^{19}$ cm^{-3} [27], [29], [30] for annealing temperatures of 850, 900, and 950°C respectively. These values in single-crystal silicon are about a factor of 2 less than the values inferred from the SIMS analysis in table 4.2.

Temperature [°C]	850	900	950
Boron solid solubility in polysilicon [cm^{-3}]	$1.0\text{-}1.5\text{x}10^{20}$	$1.5\text{-}2.0\text{x}10^{20}$	$2.0\text{x}10^{20}$

Table 4.2 Boron solid solubility in polysilicon as a function of temperature, for a drive-in of 60 minutes in dry nitrogen.

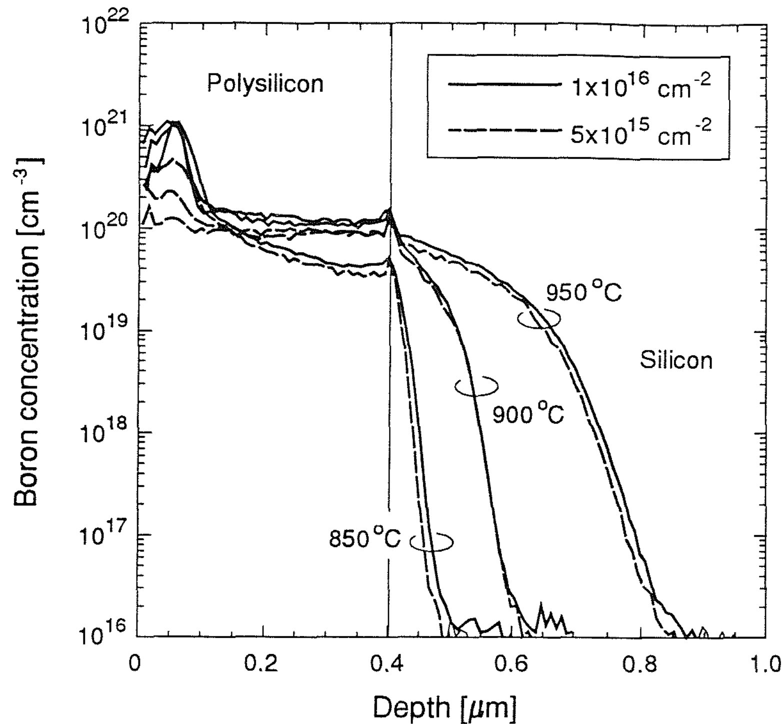

Fig. 4.9 SIMS boron profile for implanted BF_2 of doses 5×10^{15} and 1×10^{16} cm^{-2}, driven-in for 60 minutes in dry nitrogen at 850, 900, and 950°C (re-plotted data from figs. 4.1 and 4.2).

Also the single-crystal boron solid solubilities vary exponentially with temperature, whereas the solid solubility values in table 4.2 only have a small temperature dependence. Recently Park *et al.* [31] have observed very similar behaviour for boron diffusion in polysilicon, and measured the boron solid solubility in polysilicon to be 1.3×10^{20} cm^{-3} (for a 6 hour anneal at 850°C), which is approximately a factor of 2–3 above the solid solubility limit of boron in single-crystal silicon. They hypothesized that this behaviour is due to the formation and diffusion of B–defect complexes along the grain boundaries.

The boron as-implanted profile (for a dose of 1×10^{16} cm^{-2}) has a peak occurring at a concentration of 10^{21} cm^{-3}, which is nearly two orders of magnitude above the solubility limit (at 850°C), and so therefore a large proportion of the implanted boron will precipitate. This behaviour differs markedly when compared with implanted arsenic in polysilicon, where no precipitation peaks are usually observed. The reason for this is that arsenic has a much larger solid solubility in silicon than boron. For example, a typical emitter implant of energy 70 keV and dose 1×10^{16} cm^{-2} (as in an *npn* device), the as-implanted peak is at a concentration of 2×10^{21} cm^{-3}. The solid solubility of arsenic is about 10^{21} cm^{-3} [29] at 900°C, and so the majority of arsenic is free to diffuse throughout the polysilicon.

In an effort to understand the fundamental physical processes involved with boron diffusion in polysilicon and silicon crystal silicon, modelling of the SIMS profiles was undertaken. It should be pointed out here that the samples used in this study were implanted with BF_2, and the modelling program SUPREM III does not explicitly model the diffusion of BF_2 implanted layers. However, SIMS analysis of the fluorine in the polysilicon (fig. 4.10) indicate that the majority of the fluorine after the drive-in either evaporates from the surface, remains confined at the as-implanted peak, or segregates to the grain boundaries. Kim *et al.* [32] have investigated isochronal furnace annealing of BF_2 implants into single-crystal silicon, and found no significant chemical interaction between the boron and fluorine during annealing. It is thus reasonable to assume that the influence of the fluorine on the boron diffusion in the polysilicon is minimal, and hence it is expected that the results presented in this section should be equally valid for identical layers implanted with boron only. Fig. 4.11(a) shows the SUPREM III simulations for the 850, 900, and 950°C profiles of fig. 4.3 (2.5×10^{15} cm^{-2} dose) and fig. 4.11(b) shows the SUPREM III simulations for the 850, 900, and 950°C profiles of fig. 4.2 (2.5×10^{15} cm^{-2} dose). There was no need to model the 1×10^{16} cm^{-2} dose profiles, since as explained earlier, there is essentially no difference in the profiles for

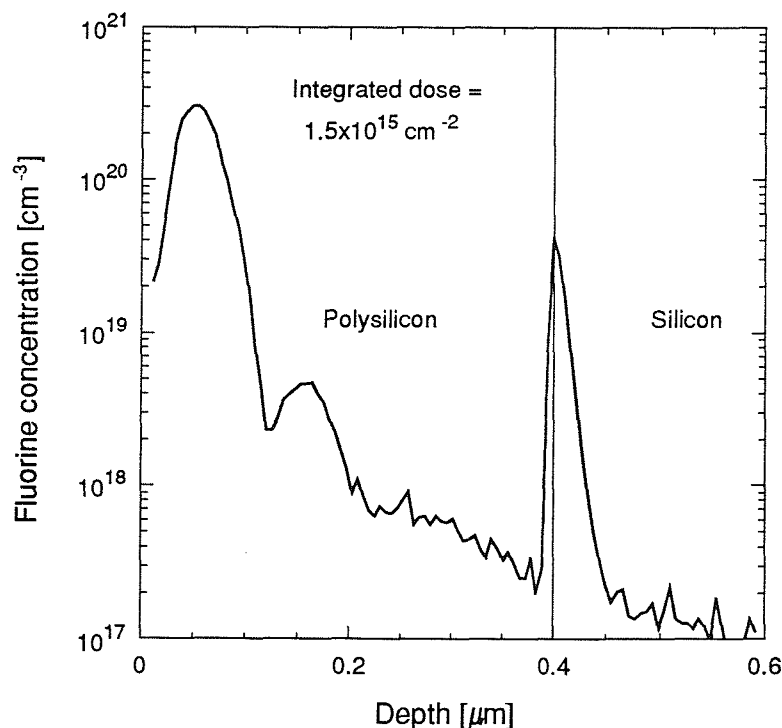

Fig. 4.10 SIMS fluorine profile for implanted BF_2 of dose 1×10^{16} cm^{-2}, driven-in for 120 minutes in dry nitrogen at 850°C. The integrated profile has a dose of only 1.5×10^{15} cm^{-2} which indicates that the majority of the fluorine has evaporated during the anneal.

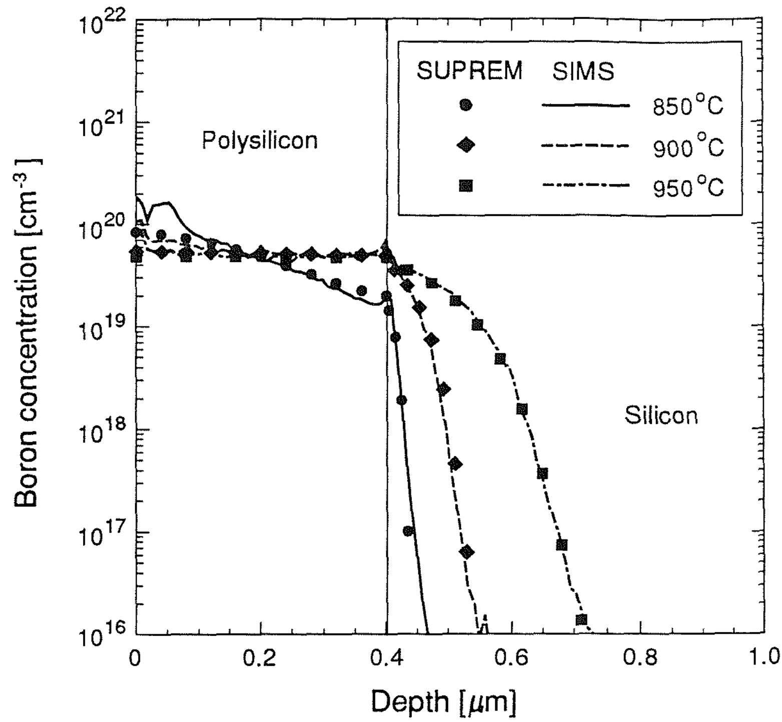

Fig. 4.11(a) SUPREM III simulations and SIMS profiles for implanted BF_2 of dose 2.5×10^{15} cm^{-2}, driven-in for 60 minutes in dry nitrogen at 850, 900, and 950°C.

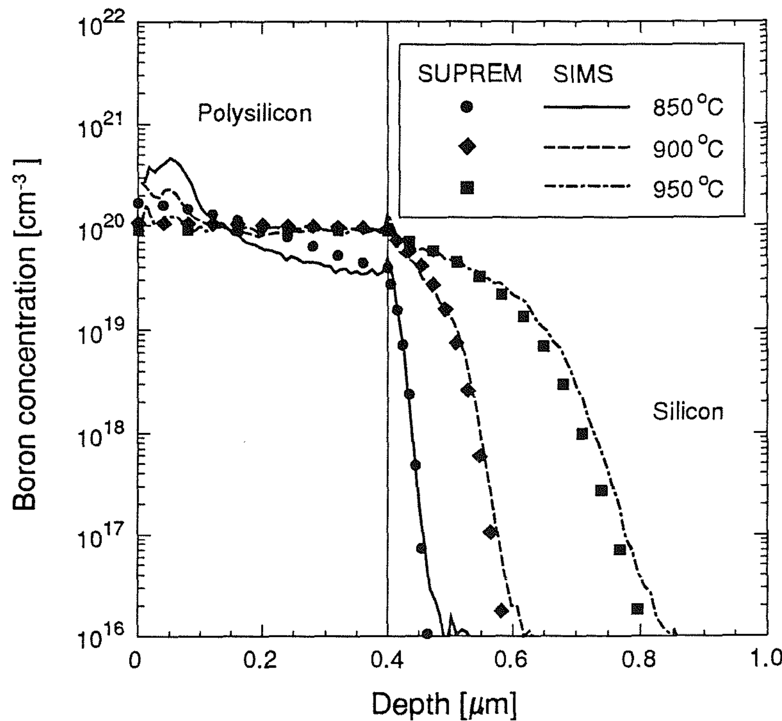

Fig. 4.11(b) SUPREM III simulations and SIMS profiles for implanted BF_2 of dose 5×10^{15} cm^{-2}, driven-in for 60 minutes in dry nitrogen at 850, 900, and 950°C.

doses over 5×10^{15} cm^{-2}. The first point to note from the SUPREM analysis is that as expected the precipitation peak at the polysilicon surface cannot be modelled.

The diffusion of boron in the polysilicon was modelled using an intrinsic diffusivity only, which took the form of an Arrhenius relationship,

$$D_{Bpoly} = D_{Bp1}\exp\left(-\frac{E_a}{kT}\right) \quad \text{cm}^2\ \text{s}^{-1} \tag{4.1}$$

where D_{Bpoly} is the diffusivity of boron in polysilicon, D_{Bp1} is a pre-exponential factor, E_a is the activation energy (the default SUPREM III value of 3.46eV was used), k is Boltzmann's constant, and T is the absolute temperature. The value of D_{Bp1} in equation 4.1 was allowed to take only one value for all the conditions in figs. 4.11(a) and 4.11(b). This fitted value for D_{Bp1} is summarised in table 4.3, and is a factor of 50 larger than the default SUPREM III value (3.7 cm^2 s^{-1}).

Implant Dose [cm^{-2}]	D_{Bp1} [cm^2 s^{-1}]	D_{Bs1} [cm^2 s^{-1}]	D_{Bs2} [cm^2 s^{-1}]
2.5×10^{15}	185	0.83	0.17
5.0×10^{15}	185	1.83	0.17

Table 4.3 Summary of modelled boron diffusivities in polysilicon and single-crystal silicon from SUPREM III simulations.

In order to model the diffusion of boron in the underlying single-crystal silicon, both a low concentration (intrinsic) and high concentration (extrinsic) diffusivity had to be modelled, as shown in equation 4.2,

$$D_{Bsil} = D_{Bs1}\exp\left(-\frac{E_a}{kT}\right) + D_{Bs2}\left(\frac{p}{n_i}\right)\exp\left(-\frac{E_a}{kT}\right) \quad \text{cm}^2\ \text{s}^{-1} \tag{4.2}$$

where D_{Bsil} is the diffusivity of boron in single-crystal silicon, D_{Bs1} is a pre-exponential factor for the intrinsic diffusivity in silicon, D_{Bs2} is a pre-exponential factor for the extrinsic diffusivity in silicon, E_a is the activation energy (the default SUPREM III value of 3.46eV was used), p is the *electrically active* boron concentration, and n_i is the intrinsic carrier concentration. It was found that the default SUPREM III value for D_{Bs2} (0.72 cm^2 s^{-1}) had to be reduced by a factor of 4.3 (see table 4.3) in order to model all the conditions in figs. 4.11(a) and 4.11(b). In order to fit the tail of the profiles the intrinsic diffusivity pre-exponential factor, D_{Bs1} had to be increased by a

factor of 2.2 for an increase of the implantation dose from 2.5x10^{15} to 5.0x10^{15} cm^{-2} (see table 4.3). This behaviour has also been observed by Orr-Arienzo *et al.* [33] for boron diffusion at high concentrations in single-crystal silicon. They attributed this to the supersaturation of the native defects (self interstitials). These fitted values of D_{Bs1} correspond to an increase by a factor of 22 and 50 over the default SUPREM III value (0.037 cm^2 s^{-1}), for the 2.5x10^{15} and 5.0x10^{15} cm^{-2} implantation doses respectively.

It is useful to define a diffusion enhancement factor (DEF) for dopant diffusion in polysilicon compared with that in single-crystal silicon, as given by the ratio of D_{Bpoly} and D_{Bsil},

$$\mathrm{DEF} = \frac{D_{Bpoly}}{D_{Bsil}} = \frac{D_{Bp1}}{D_{Bs1} + D_{Bs2}(p/n_i)} \tag{4.3}$$

Values of n_i in the temperature range 850-950°C are typically 10^{18} cm^{-3}, and p is around 3–9x10^{19} cm^{-3}, and so therefore $p/n_i \approx 30-100$. Using the fitted values of D_{Bp1}, D_{Bs1}, and D_{Bs2} from table 4.3, a value of between 50 and 220 for DEF can be extracted for boron. This same procedure has been carried out for arsenic implanted polysilicon layers, from which values for DEF between 7x10^3 [34] and 10^4 [35] have been obtained. However, it should be pointed out that in [34] and [35] the polysilicon was deposited at a higher temperature (625°C), and hence the final grain structure after anneal is likely to be different to the layers used in this study.

It is worthwhile here to examine the consequences to the doping profiles, and hence device characteristics, of various values of DEF. The ideal situation would be for the dopant species to have as large a value as possible for DEF. Then, during a high temperature drive-in the polysilicon would become uniformly doped to a high concentration very rapidly, and thereafter the dopant would diffuse much more slowly into the single-crystal silicon to give a very shallow emitter/base junction depth. This is essentially the situation for arsenic doped polysilicon emitters. During the first few seconds of a high-temperature drive-in the arsenic is distributed quickly along the grain boundaries (which are characterised by a large diffusivity [36]). After the first few minutes of the anneal the grain boundaries become saturated with arsenic, and subsequently the arsenic slowly diffuses into the bulk of the grains, and into the underlying single-crystal silicon. Thus it is relatively easy to adjust the temperature and time of the emitter drive-in to produce a highly doped polysilicon and a shallow emitter junction simultaneously.

Taking the example to the other extreme for low values of DEF (close to 1), the emitter profile becomes gaussian as in conventional implanted emitters, and so the inherent problems of fabricating shallow junctions are encountered. The situation for boron doped polysilicon emitters is part-way between these two extreme cases, but sufficiently close to the DEF=1 case to make it more difficult to obtain highly doped polysilicon and shallow emitter junctions for *pnp* devices. If the emitter drive-in for the *pnp* devices is too long or the temperature too high, for example the 950°C drive-in or to a lesser extent 900°C drive-in for 60 minutes (fig. 4.1), a high boron concentration can be obtained at the polysilicon/silicon interface, but the boron penetrates too deep into the single-crystal silicon. Alternatively, if the drive-in time and temperature are too short, for example the 850°C drive-in for 60 minutes (fig. 4.1), a shallow junction can be obtained, but the dopant concentration at the polysilicon/silicon interface is too low. This situation causes the emitter/base depletion region to extend to the polysilicon/silicon interface, with the resulting loss of gain, poor high current behaviour, and the appearance of the 'kink' in the base characteristic [25].

The explanation for the low value of DEF for boron depends on two factors. Firstly, a value of DEF much greater than 1 is due to an enhanced value of grain boundary diffusivity. The low values of DEF for boron therefore indicates that the grain boundary diffusivity is lower for boron than for arsenic. The second factor which determines the DEF is the amount of segregation of dopant to the grain boundaries. For arsenic doped polysilicon a large segregation peak is usually observed at the polysilicon/silicon interface (between a factor of 2 [37] to 20 [38] increase in the concentration of arsenic in the grain boundaries, compared to the arsenic concentration in the bulk of the grains). During high temperature anneals the growth of the grains also helps to 'sweep' arsenic evenly through the polysilicon [39]. Now turning to the case of boron doped polysilicon, it is clear from the SIMS profile that very little boron segregates to the interface [40], [41] (only about a 25% increase in boron at the interface compared to the value in the bulk of the polysilicon). It is therefore the combination of the two factors of reduced grain boundary diffusivity and reduced segregation which contributes to the reduced value of DEF for boron when compared to arsenic.

Problems are also encountered with a low electrical activity in the polysilicon. It would be expected that the electrical activity will be limited to a maximum value by the solid solubility, which for boron in single-crystal silicon is about 3×10^{19} cm^{-3} at 850°C. In general the spreading resistance profiles in fig. 4.4 do indeed indicate that the electrical activity in the polysilicon does not exceed this value. These low values of electrical activity mean that the spread of the emitter/base depletion region will extend further into the emitter, with the result that for very shallow junctions it is likely to intersect the interface. This is the explanation for the electrical characteristics

in fig. 4.5 for the device driven-in for 60 minutes at 850°C, which displays a 'kink' in the base current and poor high current behaviour. These characteristics denote SIS (Semiconductor-Insulator-Semiconductor) emitter behaviour [25], which is observed in devices with very shallow emitter junctions. As can be seen from the corresponding spreading resistance profile (fig. 4.4) and emitter depth measurement (table 4.1), the emitter depth is indeed close to zero for this device.

Returning to the devices annealed for 120 minutes at 850°C (fig. 4.6), it is evident that the RCA devices still exhibit the remnants of an SIS 'kink' at moderate to high forward bias. However, measurements of the emitter junction depth (table 4.1) yield values around 0.046–0.059μm. Estimates of the emitter/base depletion width (assuming a Gaussian emitter profile with peak concentration of $1\times10^{19}cm^{-3}$) reveal that the edge of the depletion region will extend no more than about 0.02μm into the emitter. It is therefore highly unlikely that the depletion region will intersect the polysilicon/silicon interface, and so the device characteristics should be non-SIS.

An insight into this problem can be gained by studying the device characteristics as a function emitter window area, as illustrated in fig 4.12. Both devices are plotted by current density so that differences in device area are eliminated. Fig. 4.12 clearly shows that the smaller emitter window size is far more susceptible to SIS effects than the larger area device. The reason for this behaviour can be explained by referring to fig. 4.13, which shows a scale cross-section through a device with a 2μm emitter window. Due to the topography at the edge of the emitter window, the deposited polysilicon is thicker around the emitter periphery. The implanted boron in these regions will therefore have to diffuse through a thicker portion of polysilicon, so causing the emitter junction to become shallower at the emitter edge. The resulting device will therefore consist of an SIS device in parallel with a polysilicon emitter device, with the SIS device increasing its dominance as the emitter area is reduced.

It is interesting to note that a similar 'narrow emitter effect' has been observed in sub-micron arsenic doped *npn* self-aligned polysilicon emitter transistors [42], [43]. The most notable consequence of this behaviour is an increase in the emitter-collector punch-through voltage, BV_{ECS} as the emitter size reduces, which was attributed to a reduction in emitter junction depth, caused by the diffusion of arsenic into the undoped sidewall regions. However, this behaviour is generally absent from arsenic doped *npn* polysilicon emitter transistors with emitter dimensions above a few microns, for two main reasons. Firstly, the arsenic diffusion in polysilicon is enhanced because of the increased diffusivity of arsenic along the grain boundaries. Therefore, again during the first few seconds of an anneal, the arsenic diffuses rapidly down the grain boundaries, distributing evenly along the polysilicon/silicon interface, and thereby producing a

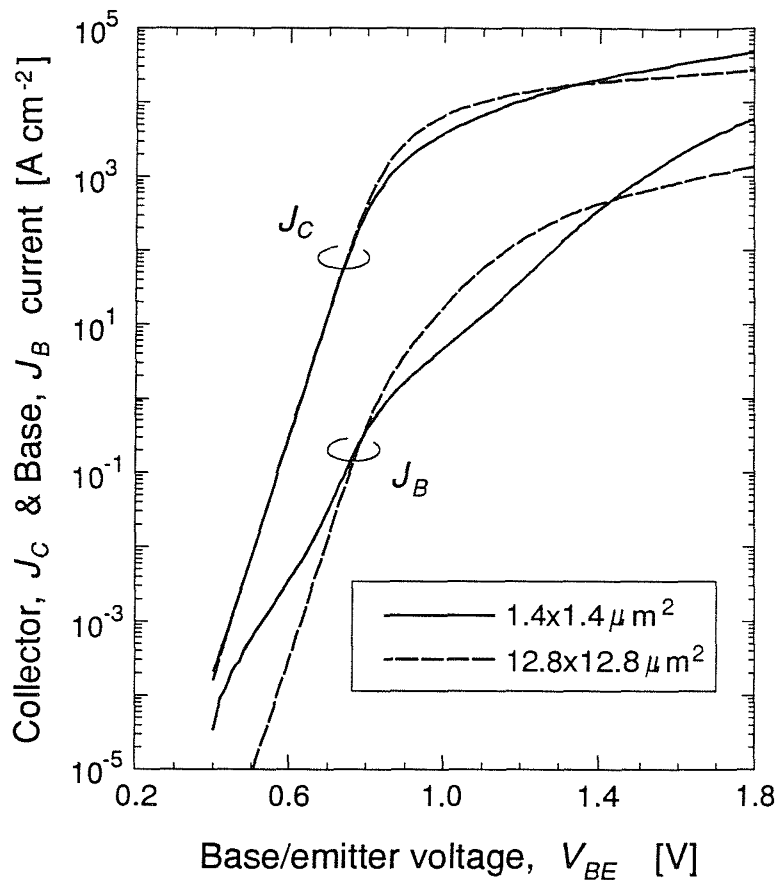

Fig. 4.12 Gummel plot of devices with a RCA interfacial treatment, followed by an emitter drive-in of 120 minutes in dry nitrogen at 850°C. Two emitter windows sizes of 1.4x1.4μm^2 (solid line) and 12.8x12.8μm^2 (dashed line) are shown, which demonstrate that SIS behaviour is more susceptible for the smaller emitter window (V_{CB}=0V, T=295K).

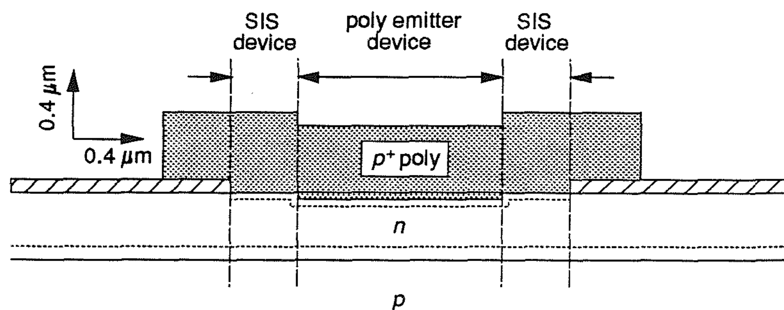

Fig. 4.13 Cross-section of a 2x2μm^2 *pnp* polysilicon emitter transistor drawn to scale. It is clear that a 'parasitic' SIS device is present around the periphery of the device.

uniform diffusion front in the single-crystal silicon [44]. The presence of a thicker polysilicon layer around the perimeter of the emitter therefore has little effect on base current. On the other hand, as discussed previously, boron diffusion in polysilicon is quite different to arsenic, in that very little of the boron is segregated to the grain boundaries, as well as the grain boundary diffusivity of boron being much lower than arsenic. In this case, boron around the periphery of the emitter window takes considerably longer to reach the interface, thereby giving rise to SIS characteristics.

4.5 Conclusions

A comprehensive study of the chemical and electrical profiles of boron doped polysilicon has been undertaken. Precipitation of boron was found to occur in the polysilicon which limited the chemical concentration to around $1-2\times10^{20}$ cm^{-3}, and the electrically active concentration in the emitter to about $1-2\times10^{19}$ cm^{-3}. SUPREM modelling of the boron profiles revealed that the boron diffusivity in polysilicon is only a factor of 50–220 larger than the diffusivity of boron in single-crystal silicon. The reason for this has been attributed to both a low value of grain boundary diffusivity, and lack of boron segregation to grain boundaries. These low values of diffusivity enhancement and electrical activity make the fabrication of shallow emitter *pnp* polysilicon emitter bipolar transistors more difficult than for conventional arsenic doped *npn* polysilicon emitter transistors.

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Chapter 5

Analysis of the Role of the Interfacial Oxide in *PNP* and *NPN* Polysilicon Emitter Transistors

5.1 Introduction

Studies of *npn* polysilicon emitter transistors have shown that the use of a deliberately grown interfacial oxide layer at the polysilicon/silicon interface can improve the current gain by a factor of between 10 and 30 [1], when compared to devices without deliberately grown interfacial layers. Modelling of these devices in chapter 2 has identified tunnelling through the oxide layer as the dominant base current mechanism [2]. This oxide also presents a tunnelling barrier to majority carriers which manifests itself as an increase in emitter resistance [3].

It is clear from the Gummel plots in chapter 4 that the use of a deliberately grown interfacial oxide layer can significantly improve the current gain of *pnp* polysilicon emitter transistors, without a serious increase in the emitter resistance. In this chapter measurements of base current and emitter resistance are performed on selected devices from chapter 4, and these are compared with values from *npn* devices with identical interfacial treatments. Barrier heights for electrons and holes are then extracted for both *pnp* and *npn* devices, and it is shown that an inconsistency is present in the values for these barrier heights, if the interfacial layer is treated as a perfect insulator. However, this inconsistency can be accounted for, if it is assumed that the interfacial oxide layer can be treated as a wide band-gap semiconductor. With a consistent set of conduction and valence band-offsets for the interfacial 'oxide' layer in both *pnp* and *npn* devices, it is shown that band bending in the interfacial layer can explain the observed asymmetry in electron and hole barrier heights.

5.2 Experimental Procedure

All devices received conventional *pnp* polysilicon emitter processing up to and including base formation (see Appendix 2). After the opening of emitter windows the interface was characterised either by an RCA clean (which was designed to grow a uniform oxide of thickness 14±2Å) or a HF etch (which leaves a thin discontinuous oxide of thickness between 0 and 8Å). Immediately after the interfacial treatment, 0.4μm of undoped amorphous silicon was deposited by LPCVD at a temperature of 560°C. The amorphous silicon was then implanted with BF_2 at a dose of $1x10^{16}$ cm^{-2} and 70 keV energy, which was followed by an emitter drive-in at 850°C for times in the range 60 to 240 minutes in dry nitrogen. This anneal is designed to uniformly dope the polysilicon and form a shallow emitter junction (see chapter 4).

Detailed electrical measurements were made of the collector and base currents as a function of base/emitter voltage (Gummel plots, see Appendix 3), and emitter resistance using the method of Ning and Tang [4], with the specific interfacial layer resistance extracted according to the method of Wolstenholme *et al.* [5]. These electrical measurements were then used to extract values of oxide barrier heights, which were

compared to *npn* devices with identical interfacial treatments. The device simulator HQUPETS (Appendix 5) was then used to investigate the concept of treating the interfacial layer as a wide band-gap semiconductor by constructing band diagrams for the interfacial layer.

5.3 Theory

5.3.1 Effective recombination velocity and heavy doping parameters

The modelling of the devices analysed in this chapter will make use of the concept of an effective recombination velocity, which was discussed in detail in chapter 2, and defines the recombination velocity on the right-hand side of the polysilicon/silicon interface (see fig. 2.5). This approach of using recombination velocity is useful in that the effects of recombination in the single-crystal emitter, and differences in mobility and band-gap narrowing between *pnp* and *npn* devices can in theory be eliminated. In order to obtain modelled values of recombination velocity, S_p, from the measured base current, J_{BO}, the approach of del Alamo *et al.* [6] is adopted (as described in section 2.3.1), who derived the following analytical relationship:

$$J_{BO} = \frac{q n_{io}^2}{G_{eff}(W_E) + N_{Eeff}(W_E)/S_p}\left[1 + \int_0^{W_E} \frac{G_{eff}(W_E) - G_{eff}(x)}{\tau_p(x) N_{Eeff}(x)} dx + \frac{N_{Eeff}(W_E)}{S_p}\int_0^{W_E} \frac{dx}{\tau_p(x) N_{Eeff}(x)}\right] \tag{5.1}$$

where $G_{eff}(x)$ is the 'effective' emitter Gummel number,

$$G_{eff}(x) = \int_0^x \frac{N_{Eeff}(x)}{D_p(x)} dx \tag{5.2}$$

and $N_{Eeff}(x)$ is the 'effective' doping concentration in the emitter,

$$N_{Eeff}(x) = N_E(x) \exp\left[\frac{-\Delta E_g^{app}(x)}{kT}\right] \tag{5.3}$$

$D_p(x)$ and $\tau_p(x)$ are the minority carrier diffusivity and lifetime in the emitter respectively, ΔE_g^{app} is the '*effective*' or '*apparent*' band-gap narrowing in the emitter, $N_E(x)$ is the electrically active emitter doping concentration, and x=0 is defined as the edge of the

emitter/base depletion region and $x=W_E$ is the position of the polysilicon/silicon interface. To calculate values for the functions $N_{Eeff}(x)$ and $G_{eff}(x)$ in the emitter, it is necessary to assume a functional form for the emitter doping profile, $N_E(x)$. This has been chosen to be a Gaussian, which is constructed by fitted it to the emitter doping concentration at the polysilicon/silicon interface (inferred from sheet resistance and spreading resistance measurements), and the emitter/base junction depth (using the method outlined in chapter 3). The integrals in equation 5.1 are then solved numerically, from which the base saturation current density, J_{BO} can be expressed as a function of the recombination velocity, S_p, for any specific emitter profile, and a given set of minority carrier parameters.

The term in square brackets in equation 5.1 models the recombination in the single-crystal emitter, which for the *pnp* devices used in this study contributes no more than about 15% to the base current of devices with deliberately grown interfacial oxide layers. However, due to the higher emitter doping concentration for the *npn* devices modelled in this study, recombination in the single-crystal emitter for these devices contributes to around 80% of the total base current. This means that the extracted recombination velocity for the *npn* devices can only be considered a maximum, which in turn allows only a minimum estimate of the hole barrier height to be made.

It is also necessary to assume values for the minority carrier recombination and transport parameters, such as lifetime, τ_p, mobility, μ_p ($=qD_p/kT$), and band-gap narrowing, ΔE_g^{app}. Values for these parameters, as a function of doping, will be taken from the work of del Alamo *et al.* [7] for *n*–type silicon and Swirhun *et al.* [8] for *p*–type silicon. The use of this set of parameters will be termed the 'DAS' model.

Recently, Popp *et al.* [9] have found that closer agreement between theory and experiment could be obtained by using the less severe band-gap narrowing data of del Alamo *et al.* [7] for both *n*– and *p*–type silicon, as discussed in chapter 3. Hence, the modelling in this chapter will also follow this approach (termed the 'Popp' model), whereby the band-gap narrowing data of del Alamo *et al.* [7] is used for both *n*– and *p*–type silicon, although the models for minority carrier mobility and lifetime remain unchanged from the 'DAS' model (i.e. the 'DAS' and 'Popp' models will yield the same minority carrier parameters in *n*–type silicon). Further evidence supporting the 'Popp' results has been supplied experimentally by King *et al.* [10], who have re-measured band-gap narrowing in *p*–type silicon, and found that the values lie between those of the models of del Alamo *et al.* [7] and Swirhun *et al.* [8]. It is therefore probable that the real minority carrier parameter set for *p*–type silicon lies somewhere between the 'DAS' and 'Popp' models.

5.3.2 Tunnelling currents and resistances

The following expression will be used to convert the modelled recombination velocity, S_p to an electron barrier height for *pnp* devices with deliberately grown interfacial oxide layers [1], [2], [11]–[13],

$$S_p = \frac{A_{ei}^* T^2}{q N_c} \cdot \frac{\exp(-b_e)}{1 - c_e kT} \tag{5.4}$$

where,

$$b_e = \frac{4\pi\delta}{h}\sqrt{2 m_{ei}^* \chi_e} \tag{5.5a}$$

$$c_e = \frac{2\pi\delta}{h}\sqrt{\frac{2 m_{ei}^*}{\chi_e}} \tag{5.5b}$$

and χ_e is the oxide barrier height to electrons, m_{ei}^* is the effective mass of electrons in the oxide, δ is the oxide thickness, A_{ei}^* is the effective Richardson constant for electrons in the oxide, and N_c is the effective density of states in the conduction band. A similar expression holds for *npn* devices, in which the electron effective mass and barrier height are replaced by their equivalent values for holes. Table 5.1 summaries the values of the parameters that will be used in equations 5.4 and 5.5, whilst the electron, χ_e (*pnp* device) and hole, χ_h (*npn* device) barrier heights will be used as fitting parameters.

Similarly, the following expression will be used to convert the measured specific emitter interfacial resistance, R_{int} to the hole oxide barrier height for *pnp* devices with deliberately grown interfacial oxide layers [13], [18],

$$R_{int} = \frac{(1 - c_h kT)}{q c_h T^2 A_{hi}^*} \cdot \exp(b_h) \cdot \exp\left(\frac{E_F - E_V}{kT}\right) \tag{5.6}$$

where,

$$b_h = \frac{4\pi\delta}{h}\sqrt{2 m_{hi}^* \chi_h} \tag{5.7a}$$

$$c_h = \frac{2\pi\delta}{h}\sqrt{\frac{2 m_{hi}^*}{\chi_h}} \tag{5.7b}$$

and χ_h is the oxide barrier height to holes, m_{hi}^* is the effective mass of holes in the oxide, δ is the interfacial oxide thickness, A_{hi}^* is the effective Richardson constant for

Parameter	Value	Reference
Electron effective mass in the interfacial oxide layer (m_{ei}^*)	$0.42m_o$	[11]
Hole effective mass in the interfacial oxide layer (m_{hi}^*)	$0.42m_o$	[11]
Effective Richardson constant for electrons in the interfacial oxide layer (A_{ei}^*)	$0.42A_o$	[11]
Effective Richardson constant for holes in the interfacial oxide layer (A_{hi}^*)	$0.42A_o$	[11]
Effective density of states in the conduction band (N_c)	3.14×10^{19} cm^{-3}	[14]
Effective density of states in the valence band (N_v)	1.78×10^{19} cm^{-3}	[14]
Interfacial oxide layer thickness (δ)	14±2Å	[15]
Temperature (T)	295K	–
Polysilicon doping level for *npn* devices	5.0×10^{19} cm^{-3}	[16]
Polysilicon doping level for *pnp* devices	1.5×10^{19} cm^{-3}	[17]

Table 5.1 Parameter values used in this chapter to extract oxide barrier heights (m_o is the free electron mass, and A_o is the Richardson constant for free electrons, $=4\pi q m_o k^2/h^3$).

holes in the oxide, and $E_F - E_V$ is the separation of the fermi level from the valence band edge. In order to obtain an analytical expression for $(E_F - E_V)/kT$, the approximate solutions as reviewed by Blakemore [19] have been utilized,

$$\frac{E_V - E_F}{kT} = \frac{\ln(u)}{1-u^2} + \frac{(3\sqrt{\pi}u/4)^{2/3}}{1+[0.24+1.08(3\sqrt{\pi}u/4)^{2/3}]^{-2}} \tag{5.8}$$

where u is the normalised acceptor concentration ($=N_A/N_v$). The expression used in equation 5.8 is valid for the full range of u (from complete non-degeneracy, up to degeneracy), with an error of less than 0.6%. Again, a similar expression to equation 5.6

holds for electrons in *npn* devices, and table 5.1 summaries the values of the parameters that will be used in equations 5.6 to 5.8, whilst the hole, χ_h (*pnp* device) and electron, χ_e (*npn* device) oxide barrier heights will be used as fitting parameters.

5.4 Electrical Results

5.4.1 Base current

Gummel plots for *pnp* devices annealed for either 60, 120, 180, or 240 minutes have been presented earlier in figs. 4.5 to 4.8 (chapter 4). A summary of the base and collector saturation current densities, as a function of drive-in time, is shown in fig. 5.1. Where the base currents are non-ideal (most notably for the devices driven-in for 60 and 120 minutes, see chapter 4), then J_{BO} was assumed to be equal to J_{CO}/β_{max}, where β_{max} is the maximum current gain. The general trend in fig. 5.1 for the RCA devices, shows a decrease in base current by a factor of 2–3 as the drive-in time is increased from 60 to 120 minutes. This is due to a reduction in the non-ideal components of the base current, as the emitter/base junction depth is increased from approximately zero for the 60 minute anneal, to around 0.05μm for the 120 minute anneal. However, as the drive-in time is increased beyond 120 minutes, an increase in base current is observed by a factor of 4 and 5 for the 180 and 240 minute drive-in times respectively.

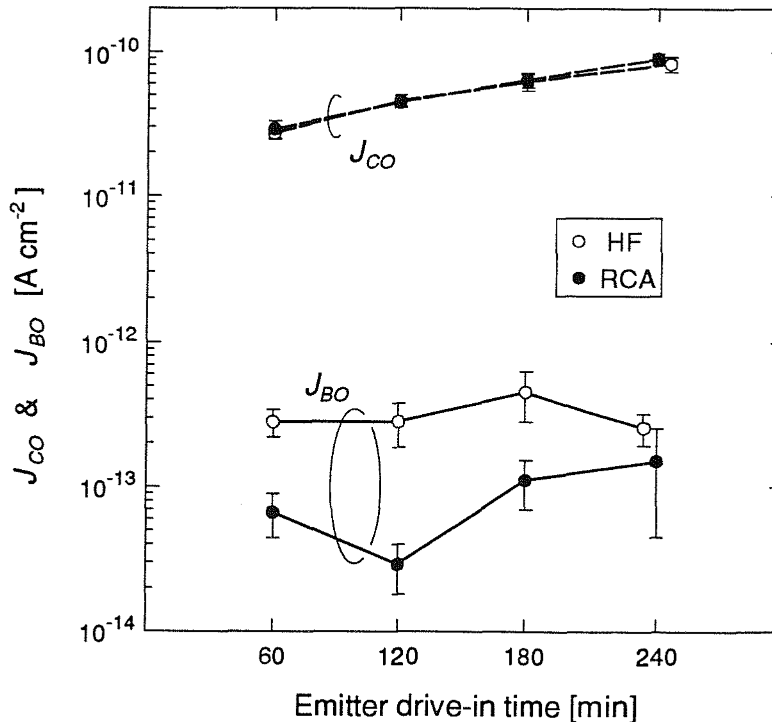

Fig. 5.1 Summary of collector, J_{CO} and base, J_{BO} saturation current densities for *pnp* devices as a function of emitter drive-in time. The error bars represent the standard deviation from measuring at least 20 devices across a wafer (V_{CB}=5V, T=295K, A_{EW}=10.8x10.8μm^2).

The most likely explanation for this increase of base current with drive-in time is thermal stressing of the interfacial oxide, leading to partial thinning and break-up of the oxide. This will in turn reduce the blocking ability of the oxide, and so will lead to an increase in base current. SIMS analysis of the *pnp* devices (fig. 4.10) reveals that fluorine segregates to the polysilicon/silicon interface in concentrations up to $5x10^{19}$ cm^{-3}. Recent work by Kouvatsos *et al.* [20] into the effect of fluorine on the kinetics of oxide growth have shown that the presence of fluorine can dramatically reduce the inherent stress between oxide and silicon. It is thus possible that the segregation of the fluorine to the polysilicon/silicon interface could facilitate the break-up of the interfacial oxide, and therefore contribute to the increase of base current in fig. 5.1. Further work is therefore required to investigate the possible effect of the fluorine (or boron) on the break-up of the interfacial oxide.

The 120 minute drive-in device will be chosen for modelling, since it combines an ideal base current (n=1.05–1.10), a shallow emitter/base junction depth (0.046–0.059μm), and probably an intact interfacial oxide layer. It is therefore reasonable to assume that the base current will be dominated by tunnelling through the interfacial oxide, such that the tunnelling expressions in equations 5.4 and 5.6 can be applied unambiguously. Furthermore, a large area device (EW=12.8x12.8 μm^2) has been chosen to be modelled so that the influence of the peripheral SIS characteristics are reduced. A Gummel plot is shown in fig. 5.2, where it can be seen that the 'kink' in the base characteristic is almost eliminated.

5.4.2 Emitter resistance

The emitter resistance of the *pnp* devices were measured using the method of Ning and Tang [4], and an example of a 'Ning-Tang' plot is illustrated in fig. 5.3 for RCA and HF devices driven-in for 120 minutes (i.e. similar to those devices in fig. 5.2). If the y-axis intercept ('Ning-Tang' intercept) is plotted as a function of reciprocal emitter window area, then the specific emitter interfacial resistivity is equal to the gradient of the straight line produced (the other components of emitter resistance, notably the contact resistance are therefore eliminated). Fig. 5.4 shows the plots of the 'Ning-Tang' intercept against the reciprocal emitter window area, again for the RCA and HF devices driven-in for 120 minutes. The specific emitter interfacial resistivities for the devices in fig. 5.4 are summarised in fig. 5.5, along with the results for RCA and HF devices annealed for either 180 or 240 minutes. The decrease in emitter resistance as the drive-in time increases is further confirmation that the interfacial oxide is breaking-up under increased thermal stressing. The specific emitter interfacial resistivities for the devices driven-in for 120 minutes are 360±60 $\Omega\mu m^2$ and 90±20 $\Omega\mu m^2$ for the RCA and HF interfacial treatments respectively.

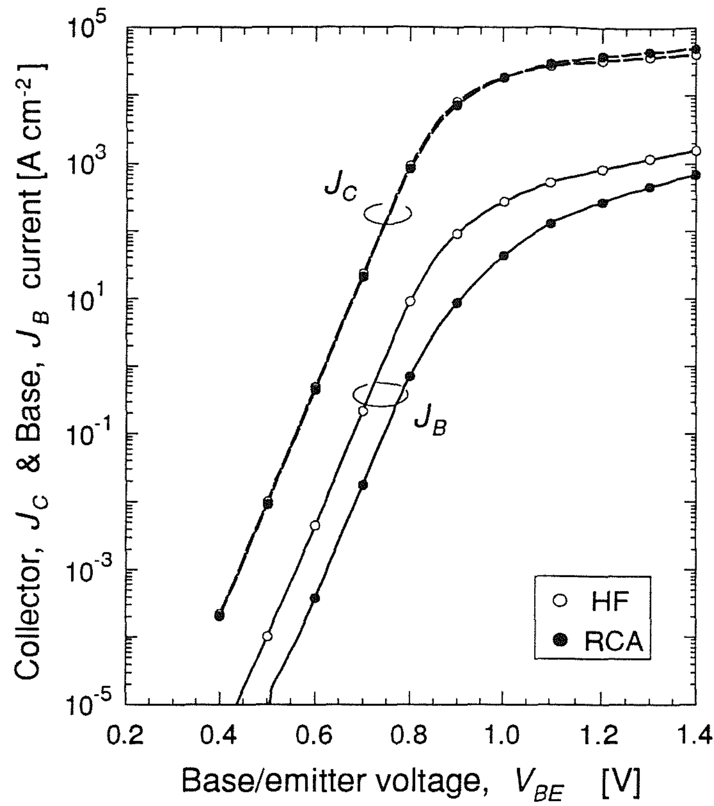

Fig. 5.2 Gummel plot of *pnp* devices either with an RCA or HF interfacial treatment, followed by an emitter drive-in of 120 minutes at 850°C in dry nitrogen (V_{CB}=5V, T=295K, A_{EW}=12.8X12.8μm^2).

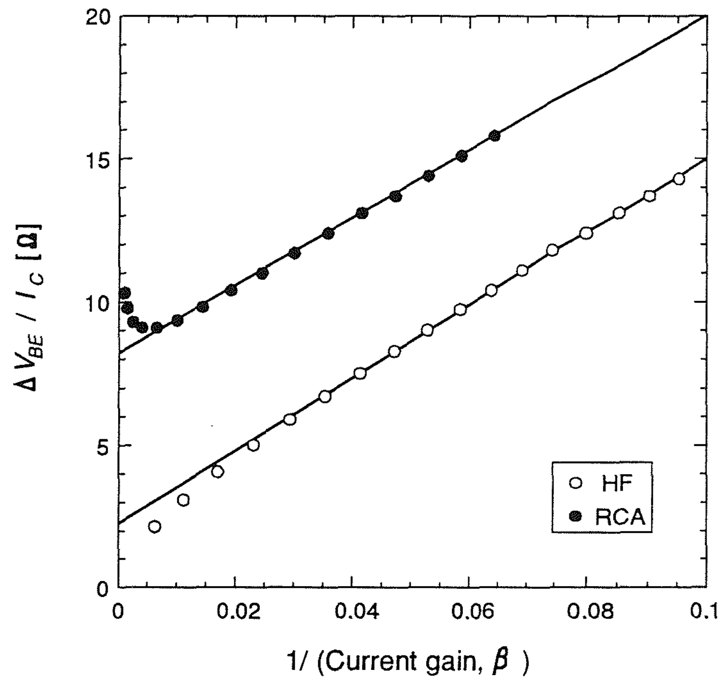

Fig. 5.3 'Ning-Tang' plot of $\Delta V_{BE}/I_C$ against reciprocal current gain, where ΔV_{BE} is the voltage dropped across the emitter and base resistances. The devices shown are similar to those in fig. 5.2 (V_{CB}=5V, T=295K, A_{EW}=6.9X6.9μm^2).

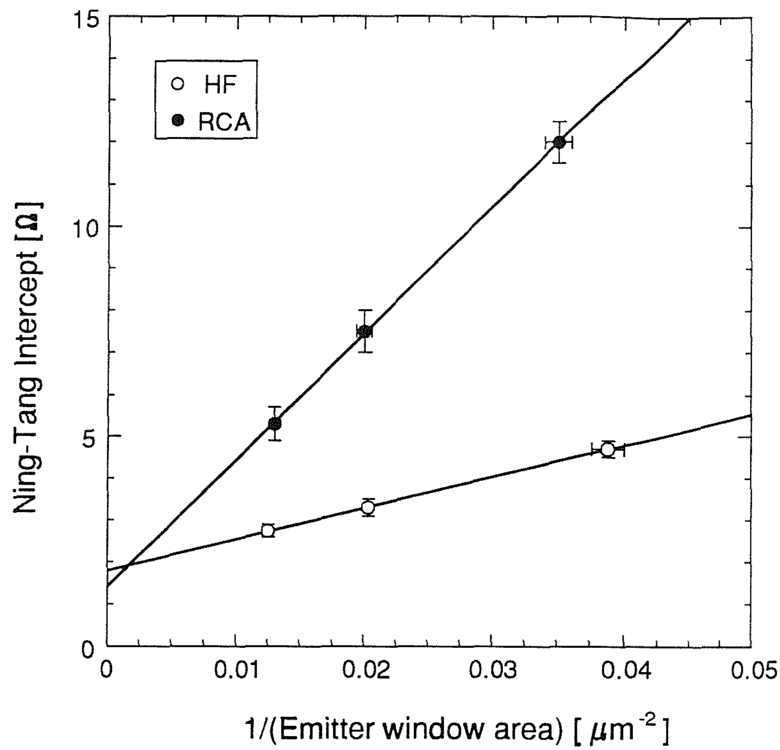

Fig. 5.4 'Ning-Tang' intercept against reciprocal emitter window area, for the *pnp* devices given either an RCA or HF interfacial treatment in fig. 5.2. The error bars represent the standard deviation from measuring at least 10 sites across a wafer.

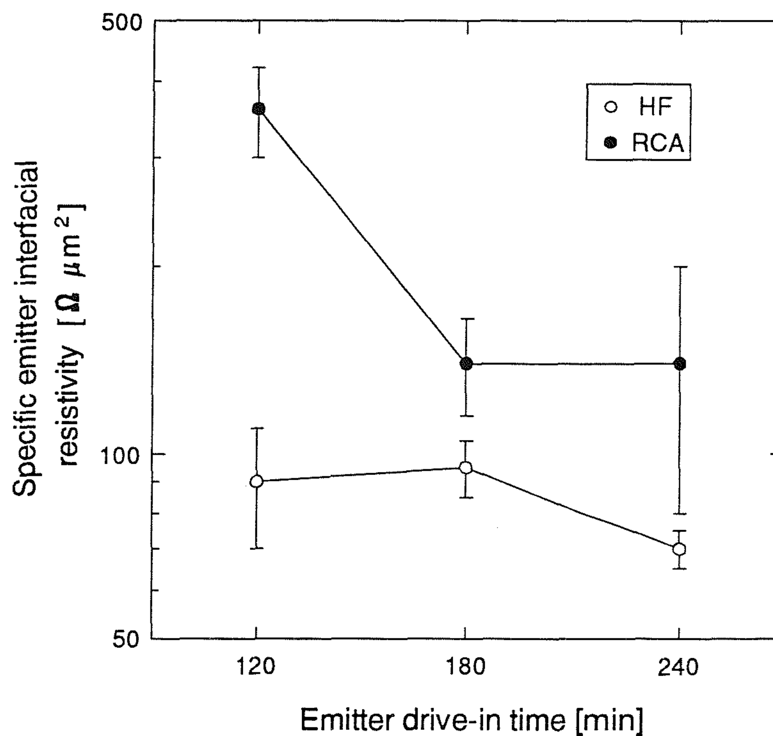

Fig. 5.5 Summary of specific emitter interfacial resistivity for the *pnp* devices, as a function of emitter drive-in time. The error bars represent the standard deviation from measuring at least 10 sites across a wafer.

5.5 Discussion

5.5.1 Extraction of oxide barrier heights

In order to eliminate the effects of recombination in the single-crystal emitter from the measured base current, the recombination velocity at the polysilicon/silicon interface can be extracted by solving equation 5.1, and this has been performed in figs. 5.6(a) and (b) for the *pnp* RCA and HF devices from fig. 5.2. Furthermore, the two band-gap narrowing and minority carrier parameter sets of the 'DAS' and 'Popp' models have also been used. From fig. 5.6(a) it can be seen that recombination velocities of $6.39 \pm 2.19 \times 10^3$ cm s^{-1} for the HF device, and $5.51 \pm 2.50 \times 10^2$ cm s^{-1} for the RCA device can be extracted from the measured base current by using the 'DAS' model parameters. Alternatively, in fig. 5.6(b), recombination velocities of $2.50 \pm 0.86 \times 10^4 cms^{-1}$ for the HF device, and $2.42 \pm 0.95 \times 10^3$ cm s^{-1} for the RCA device result from using the 'Popp' model parameters.

These values of recombination velocity compare with values from the literature of 8×10^3 cm s^{-1} [21], [22] (using the 'DAS' model) for *pnp* transistors with a deliberately grown interfacial oxide layer, and 1.5×10^4 [21], [22] to 1.4×10^5 cm s^{-1} [23] (again using the 'DAS' model) for *pnp* transistors with no deliberately grown interfacial oxide layer. It can be seen that the values of recombination velocity from this study are considerably lower than those found in the literature. The most likely explanation for this is variations in the integrity of the interfacial oxide, caused by either differences in the oxide growth conditions, or in the emitter drive-in conditions. For example, the devices in [21] were driven-in at 900°C for 30 minutes, compared with a drive-in at 850°C for 120 minutes in this study. Moreover, the chemical oxidising treatment in [21] was only carried out for 10 minutes, which compares to 20 minutes in this study. It is also useful to compare these values of recombination velocity with those from *npn* transistors with identical interfacial oxide treatments. For example, using the devices of Wolstenholme *et al.* [16] (which have identical interfacial treatments to the *pnp* devices in this study), values of recombination velocity for *npn* devices both with and without a deliberately grown interfacial oxide layer can be extracted as $<6.6 \times 10^2$ and 1.2×10^4 cm s^{-1} respectively (using either the 'DAS' or 'Popp' models). It is therefore evident that the recombination velocities of *pnp* and *npn* devices, with deliberately grown interfacial oxides, are very comparable.

The incorporation of an interfacial oxide layer, as seen previously (fig. 5.2), can result in an increase in current gain, although it is well documented that an increase in emitter resistance usually ensues. Indeed the results from this, and other studies, indicate that this is the case. For example, values of emitter resistance of 270 $\Omega\mu m^2$ [22] have been quoted for *pnp* devices with a deliberately grown interfacial oxide layer, and values of 30–200 $\Omega\mu m^2$ [21], [24], [25] for devices without a deliberately grown

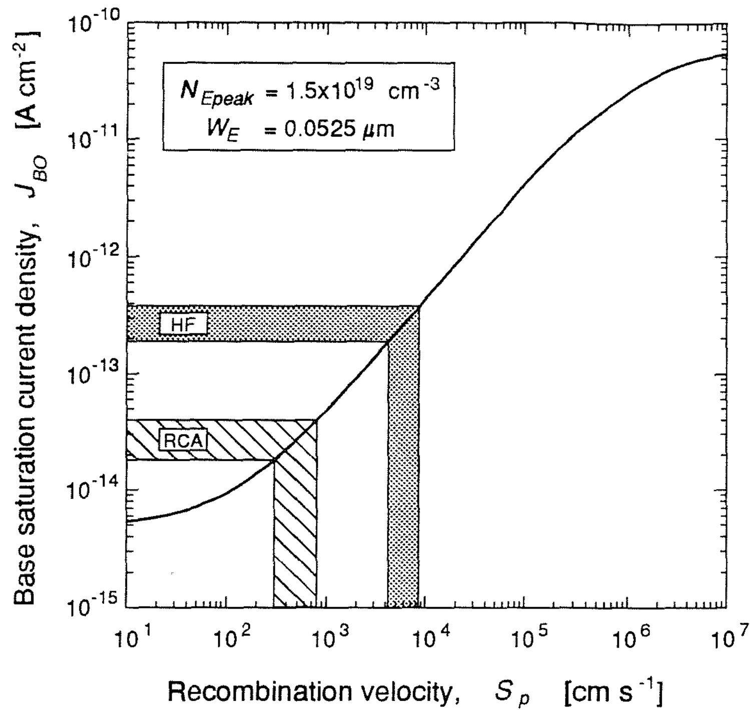

Fig. 5.6(a) Modelled base saturation current density, J_{BO} as a function of recombination velocity, S_p for *pnp* devices with either an RCA or HF interfacial treatment. The band-gap narrowing and minority carrier data of the 'DAS' model have been used.

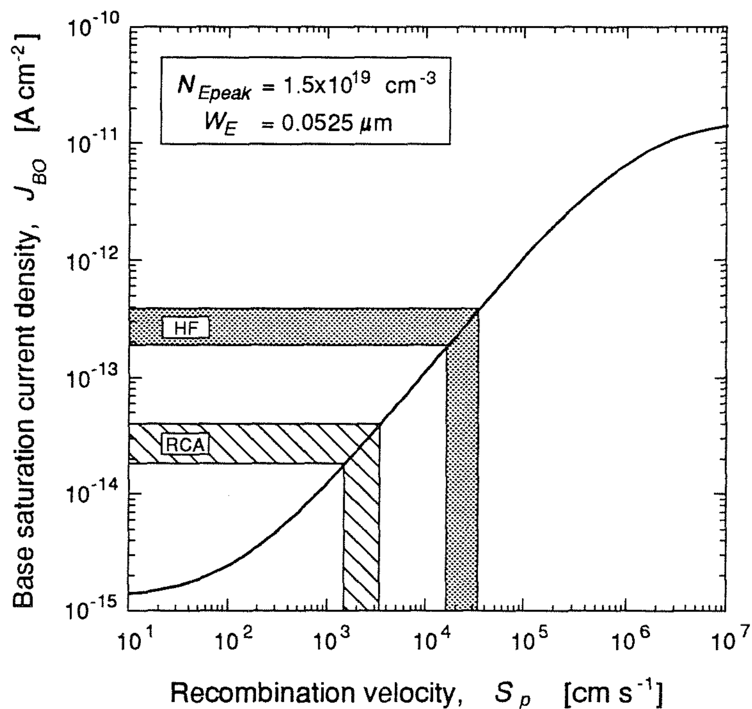

Fig. 5.6(b) Modelled base saturation current density, J_{BO} as a function of recombination velocity, S_p for *pnp* devices with either an RCA or HF interfacial treatment. The band-gap narrowing and minority carrier data of the 'Popp' model have been used.

interfacial oxide layer. These compare with values from this study of 360±60 $\Omega\mu m^2$ for devices with deliberately grown interfacial oxide layers (RCA), and 90±20 $\Omega\mu m^2$ for devices without deliberately grown interfacial layers (HF). Again, on comparing these values with results obtained from *npn* transistors with identical interfacial layers [16], specific interfacial resistivities of 330±40 $\Omega\mu m^2$ and ~70 $\Omega\mu m^2$ are obtained for devices either with or without a deliberately grown interfacial oxide layer respectively. It is therefore evident that the emitter resistances of *pnp* and *npn* devices, with deliberately grown interfacial oxides, are very comparable.

For the *pnp* RCA devices it would be expected that both the base current and emitter resistance are dominated by tunnelling through the interfacial oxide layer [18]. If this is the case then it is possible to convert the interface recombination velocity, S_p into an effective barrier height, χ_e for electron tunnelling, and the specific emitter interface resistivity, R_{int} into an effective barrier height, χ_h for hole tunnelling. Fig. 5.7 shows the modelled value of recombination velocity, S_p, as a function of electron barrier height, χ_e for three values of oxide thickness using equation 5.4. The values of oxide thickness chosen are consistent with the measured value of 14±2Å from high resolution

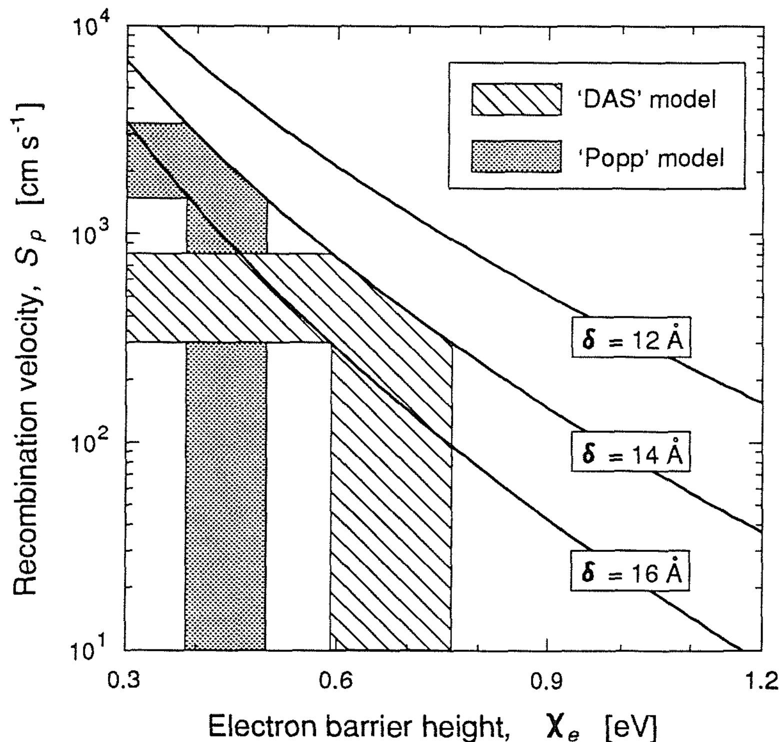

Fig. 5.7 Modelled recombination velocity, S_p as a function of electron barrier height, χ_e, using the expression in equation 5.2, for three interfacial oxide layer thicknesses of 12, 14 and 16Å. The two modelled values of S_p from the 'DAS' and 'Popp' minority carrier parameter sets have been used to extract the electron barrier height.

transmission electron spectroscopy (HRTEM) [15]. The measured value of recombination velocity for the *pnp* RCA device ($5.51\pm2.50 \times10^2$ cm s^{-1} for the 'DAS' model and $2.42\pm0.95 \times10^3$ cm s^{-1} for the 'Popp' model) therefore corresponds to an electron barrier height, χ_e of 0.68±0.08 eV ('DAS' model), and 0.44±0.06 eV ('Popp' model). The corresponding situation for *npn* transistors with an RCA interfacial treatment, is that the hole barrier height, χ_h controls the base current. By using the *npn* RCA device of Wolstenholme *et al.* [16], a hole barrier height, χ_h of >0.72 eV can be modelled. As pointed out previously, since about 80% of the base current of the *npn* device is composed of recombination in the single-crystal emitter, this means that only a lower estimate of the hole barrier height can be made.

Turning now to the majority carrier tunnelling current, which is controlled by the emitter resistance, fig. 5.8 illustrates the modelled specific emitter interfacial resistivity, R_{int} for the *pnp* devices, as a function of hole barrier height, χ_h for three values of oxide thickness, using equation 5.6. Also shown is the measured value of specific emitter interfacial resistivity (360 ± 60 $\Omega\mu m^2$) for the *pnp* RCA device annealed for 120 minutes, from which a hole barrier height, χ_h of 0.31±0.02 eV can be implied. Similarly, the same process can be carried out for the *npn* RCA devices of Wolstenholme *et al.* [16], which yields an electron barrier height, χ_e of 0.40±0.01 eV. Table 5.2 summarises

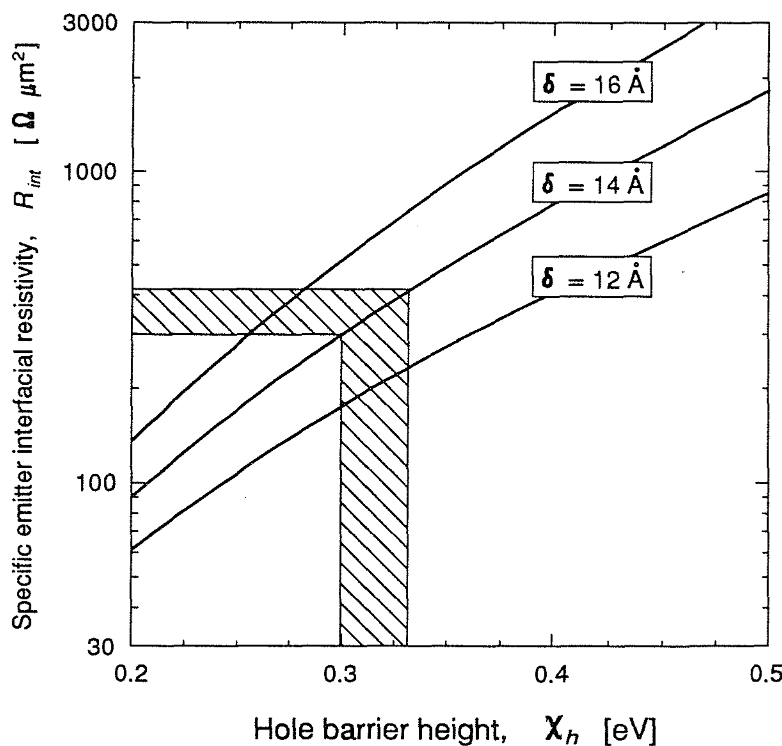

Fig. 5.8 Modelled specific emitter interfacial resistivity, R_{int} as a function of hole barrier height, χ_h using the expression in equation 5.4. R_{int} has been modelled for three interfacial oxide layer thicknesses of 12, 14 and 16Å.

The barrier heights in table 5.2 are extracted by assuming that the interfacial oxide layer is stoichiometric (i.e. SiO_2), such that the layer acts as a perfect insulator. If this is the case then the extracted electron and hole barrier heights in table 5.2 should be equal to the bulk values of χ_e=3.1 eV and χ_h=4.7 eV for Si/SiO_2 [a]. Clearly this is not observed in table 5.2, and therefore raises some doubt as to the applicability of a bulk SiO_2 model for the thin chemically grown interfacial oxides used in this study. Furthermore, using an effective mass of $0.5m_o$ (calculated for an SiO_2 band structure [b]) in equations 5.4 and 5.6, results in electron and hole barrier heights as shown in table 5.2(a). However, there still remains the inconsistency between barrier heights extracted from *npn* and *pnp* devices, as well as the magnitude of the heights being inconsistent with those for the Si/SiO_2 system.

Studies of chemically grown oxides at the polysilicon/silicon interface show that it is non-stoichiometric [c] (i.e. SiO_x, with x between 1 and 2), and also contains impurities, such as carbon, up to concentrations approaching 10^{22} cm^{-3} [d]. It is likely under such circumstances that the band structure of the interfacial 'oxide' layer could deviate significantly from that of SiO_2. It therefore seems a reasonable approximation to treat the interfacial 'oxide' layer as a wide-bandgap semiconductor, and such an approach is used in the next section to explain the inconsistency between electron and hole barrier heights in table 5.2.

Electron barrier height, χ_e [eV]		Hole barrier height, χ_h [eV]	
npn	*pnp*	*npn*	*pnp*
0.37±0.01	0.60±0.07 'DAS' 0.40±0.05 'Popp'	>0.64	0.29±0.02

Table 5.2(a) Summary of hole and electron oxide barrier heights using the same parameters as in table 5.2, except for an electron and hole effective mass in the interfacial oxide of $0.5m_o$ [b].

[a] J. Maserjian and G.P. Petersson, "Tunneling through thin MOS structures: Dependence on energy (E-k)*", *Appl. Phys. Lett.*, vol. 125, pp. 50–52, 1974.

[b] J.R. Chelikowsky and M. Schlüter, "Electron states in α–quartz: A self consistent pseudopotential calculation", *Phys. Rev. B*, vol. 15, pp. 4020–4029, 1977.

[c] J.M.C. Stork, M. Arienzo and C.Y. Wong, "Correlation between the diffusive and electrical properties of the interface in polysilicon contacted n^+–p junctions", *IEEE Trans. Electron Devices*, vol. ED–32, pp. 1766–1770, 1985.

[d] G.L. Patton, J.C. Bravman and J.D. Plummer, "Physics, technology, and modeling of polysilicon emitter contacts for VLSI bipolar transistors", *IEEE Trans. Electron Devices*, vol. ED–33, pp. 1754–1768, 1986.

	Electron barrier height, χ_e [eV]		Hole barrier height, χ_h [eV]	
	npn	*pnp*	*npn*	*pnp*
Experimentally determined	0.40±0.01	0.68±0.08 'DAS' 0.44±0.06 'Popp'	>0.72	0.31±0.02
No band-bending in interfacial layer	0.50	0.50	0.50	0.50
With band-bending in interfacial layer	0.33	0.65	0.65	0.31

Table 5.2 Summary of hole and electron oxide barrier heights determined from the experimentally measured values of base current and emitter resistance, from *npn* and *pnp* devices with deliberately grown interfacial oxide layers. Also shown is the electron and hole barrier heights assuming that the interfacial layer can be treated as a wide-bandgap material, with $\Delta E_c = \Delta E_v = 0.5$ eV. Two specific cases are shown, one for no band-bending in the interfacial layer, and the second with substantial band-bending in the interfacial layer.

the extracted oxide barrier heights of holes and electrons from both *pnp* and *npn* transistors, from which it can be clearly seen that there exists an inconsistency in the values of barrier height extracted from the two types of device.

5.5.2 A Heterojunction Tunnelling Model

The asymmetry in oxide barrier heights to electrons and holes in *npn* polysilicon emitter transistors has been investigated theoretically by O'Neill [26]. The electrons and holes are assumed to tunnel through the thin oxide layer by complex (evanescent) states which extend into the oxide band-gap, and are derived from reflections of the oxide conduction and valence bands. Since the curvature of the valence band is far less than that of the conduction band, the evanescent states associated with the valence band decay too quickly to have any significance for tunnelling currents. Thus both the electrons and holes tunnel through the oxide via states associated with the conduction band. Since the hole and electron energies are always separated by the silicon band-gap, this means that the tunnelling probability for holes is always lower than that for electrons. In other words the hole barrier height is larger than the electron barrier height by an amount equal to the silicon band-gap. This theory has been extended by Chu and Pulfrey [27] into a one-band oxide model (one-band because both carriers tunnel via the evanescent states derived from the conduction band) for MIS tunnel junctions.

The results from this chapter, however, clearly contradict the one-band oxide model (see table 5.2). It is also worth noting that Laser *et al.* [22] attempted to use the one-band oxide model, to model *pnp* polysilicon emitter transistors with deliberately grown interfacial oxide layers. They subsequently found that they could not

simultaneously model the base current and emitter resistance with a consistent set of electron and hole barrier heights. In fact, to alleviate this problem Laser *et al.* [22] proposed that the oxide thickness be reduced (equivalent to a reduction in hole barrier height) in order for the model to fit the measured value of emitter resistance.

If the interfacial oxide layer is assumed to be a perfect insulator, then due to the large dielectric relaxation time (the order of months), an equilibrium fermi level cannot be constructed in the oxide. Therefore, the electron and hole barrier heights should remain constant regardless of the emitter dopant type being n– or p–type. Furthermore, bulk SiO_2 has a band-gap of around 9 eV and an electron affinity of 0.9 eV, which translates to an electron barrier height, χ_e of 3.1 eV and a hole barrier height, χ_h of 4.7 eV. For thin oxide layers, it is likely that image force barrier lowering [28], [29] will reduce the size of these barriers, although studies have shown [26] that the barrier lowering is not enough to explain the observed magnitude of oxide barrier heights. It therefore seems apparent that treating the interfacial oxide layer as a perfect insulator cannot explain the experimental results presented in this chapter.

Investigations of the integrity of chemically grown interfacial oxides show that it is non-stoichiometric [30] (i.e. SiO_x, with x between 1 and 2), and also contains large amounts of impurities such as carbon and segregated arsenic. Therefore, it seems reasonable to assume that the interfacial oxide can be treated as semiconducting, rather than insulating, such that a fermi level can be constructed in the interfacial layer. Moreover, the band-gap of the interfacial layer will be assumed larger than that of silicon. This situation is akin to that for SIPOS (Semi-Insulating Polycrystalline Silicon) [31]–[33], which is polysilicon deposited with a high oxygen concentration. When the SIPOS material is used as the emitter contact in bipolar transistors, an improvement in current gain is achieved, which has been attributed to the SIPOS exhibiting wide-bandgap emitter behaviour [34].

When two semiconducting materials of different band-gaps, but the same doping type, are brought together (isotype heterojunction), then band-bending at the interface will occur as charge depletes from the wide-band-gap material and accumulates in the narrow-band-gap material, in order that the fermi level remains constant in equilibrium. Simulation [35], [36] results are shown in fig. 5.9 for an Nn heterojunction illustrating this behaviour. The level of this band-bending is dependent on both the value of the conduction band offset, and the doping concentrations on either side of the junction. As the doping concentration is increased in such a system, the depletion and accumulation widths decrease. For example, a doping concentration of $3\text{x}10^{20}$ cm^{-3} (with conduction and valence band offsets of 0.5 eV) the depletion width is $\approx$16Å (fig. 5.10), which is comparable with the 14Å thickness of the interfacial layer.

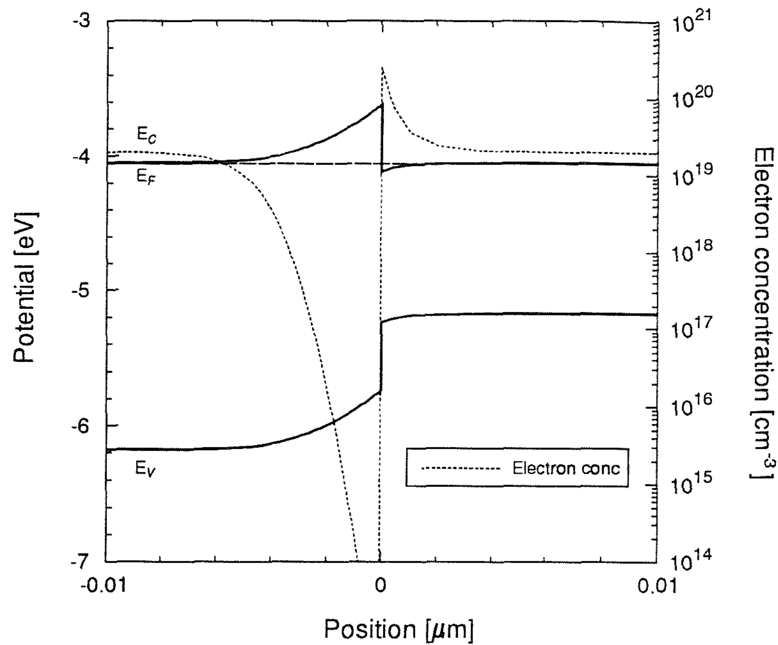

Fig. 5.9 Band-diagram of an *Nn* isotype heterojunction, doped to a concentration of $2x10^{19}$ cm^{-3}, and with conduction and valence band offsets of 0.5 eV. Also shown is the electron distribution across the junction, which highlights the accumulation and depletion regions on either side of the junction.

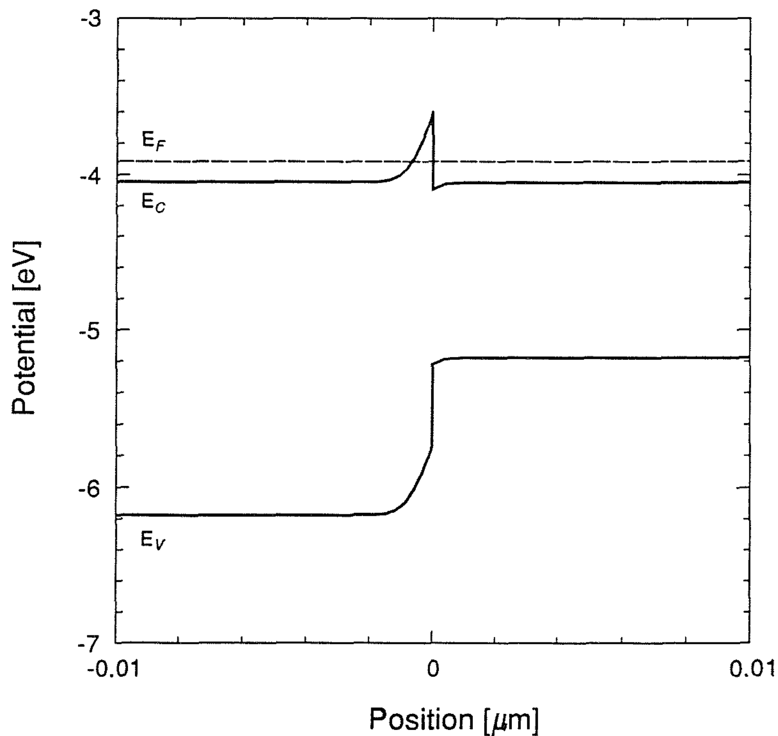

Fig. 5.10 Band-diagram of an N^+n^+ isotype heterojunction, doped to a concentration of $3x10^{20}$ cm^{-3}, and with conduction and valence band offsets of 0.5 eV. By comparing with fig. 5.9, it can be seen that the increased doping concentration has considerably shortened the accumulation and depletion widths.

The case of a wide band-gap interfacial 'oxide' layer sandwiched between the single-crystal silicon and polysilicon emitter, can be treated as two isotype heterojunctions placed back to back. For example, fig. 5.11 shows the band diagram of an *nNn* heterojunction, with a 14Å thick wide band-gap interfacial 'oxide' layer, as would be found in an *npn* polysilicon emitter bipolar transistor. The conduction and valence band offsets have been chosen to be equal at 0.5 eV, and the interfacial 'oxide' layer is doped to a concentration of $5x10^{19}$ cm^{-3}. On one side of the interfacial layer is the polysilicon emitter and on the other side the single-crystal silicon emitter, which are both also doped to a concentration of $5x10^{19}$ cm^{-3}. It can be clearly seen that potential barriers are present in both valence and conduction bands, as required by the tunnelling model. The barriers are approximately rectangular in shape, with symmetrical electron and hole barrier heights, which are equal to the assumed valence and conduction band offsets. There is a small amount of band-bending within the interfacial layer, which is consistent with that for a single isotype heterojunction doped at $5x10^{19}$ cm^{-3}.

Although the band diagram in fig. 5.11 successfully explains the presence of the potential barriers, it does not explain the observed asymmetry in the barrier heights.

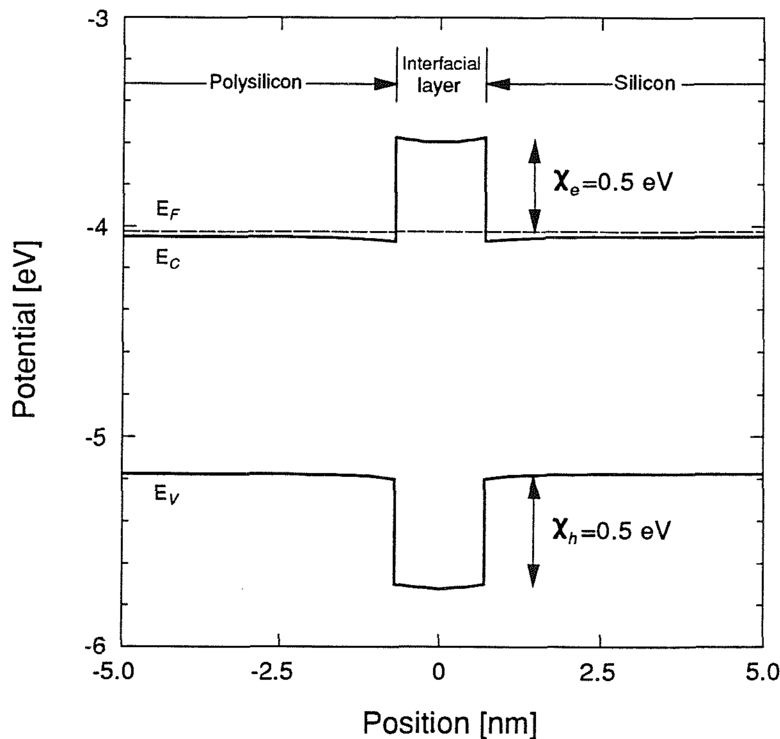

Fig. 5.11 Band-diagram of an *nNn* polysilicon/'oxide'/silicon isotype heterojunction, doped to a concentration of $5x10^{19}$ cm^{-3}, and with conduction and valence band offsets of 0.5 eV. Since the band-bending in the interfacial layer is minimal, the electron and hole barrier heights are approximately symmetrical, and equal to the conduction and valence band offsets. It has been assumed that permitivity in the interfacial 'oxide' layer is the same as that in silicon (11.9).

One way of explaining this asymmetry would be to introduce an asymmetry in the conduction and valence band discontinuities, such that $\Delta E_c=\chi_e\approx0.4$ eV and $\Delta E_v=\chi_h\approx0.7$ eV, as shown in fig. 5.12(a). However, this presents an insurmountable problem when the complementary case of the *pnp* device is considered, as shown in fig. 5.12(b), which has the same conduction and valence band offsets as in fig. 5.12(a). It can be clearly seen that the electron barrier height ($\approx$0.4 eV) and the hole barrier height ($\approx$0.7 eV) are unchanged on going from the *npn* (fig. 5.12(a)) to the *pnp* (fig. 5.12(b)) device, which therefore cannot explain the experimental results in table 5.2.

An alternative approach is to assume that the doping concentration in the interfacial 'oxide' layer is increased beyond that in the polysilicon and single-crystal silicon, such that the depletion width in the interfacial layer is approximately equal to the interfacial layer thickness. In this case the band-bending effectively lowers the electron barrier height, and increases the hole barrier height. This is shown in fig. 5.13(a) for an nN^+n heterojunction (i.e. equivalent to an *npn* device), with an interfacial 'oxide' layer doped to $3\text{x}10^{20}$ cm^{-3}, and with conduction and valence band offsets of 0.5 eV. The resultant electron and hole barrier heights are consistent with the experimentally determined barrier heights, as shown in table 5.2. Correspondingly, for the case of the *pnp* device, a similar amount of increase in the doping concentration in the interfacial 'oxide' layer ($3\text{x}10^{20}$ cm^{-3}) can effectively lower the hole barrier height and increase the electron barrier height. This is shown for a pP^+p heterojunction in fig. 5.13(b), where it can be seen that the barrier heights are again consistent with the experimentally determined values in table 5.2 (using the 'DAS' model parameter set). Therefore, even though the conduction and valence band discontinuities are the same for both *npn* and *pnp* devices, the band-bending can explain the observed asymmetries in the minority and majority carrier tunnelling barriers observed in both *npn* and *pnp* devices.

The above discussion has indicated that a large amount of band-bending in the interfacial 'oxide' layer is required to provide the asymmetry in the experimentally determined barrier heights. It is well known that, in *npn* devices, arsenic segregates to the polysilicon/silicon interface in concentrations between a factor of 5 [37] and 20 [38] above the polysilicon doping level. This segregated dopant could therefore account for the extra interfacial layer doping required to facilitate band-bending. It should be pointed out here that the segregated dopant in the interfacial 'oxide' layer has to be electrically active [39], so as to reduce the depletion width in the interfacial layer. Moreover, the band-bending does not depend on the effective doping concentration at the interface (unlike the thermionic *segregation model* in chapter 2), and so a relatively small amount of segregation to the interface can significantly alter the barrier heights. However, for the *pnp* devices, boron does not generally segregate to the polysilicon/silicon interface (chapter 4), and thus it would be expected that band-bending

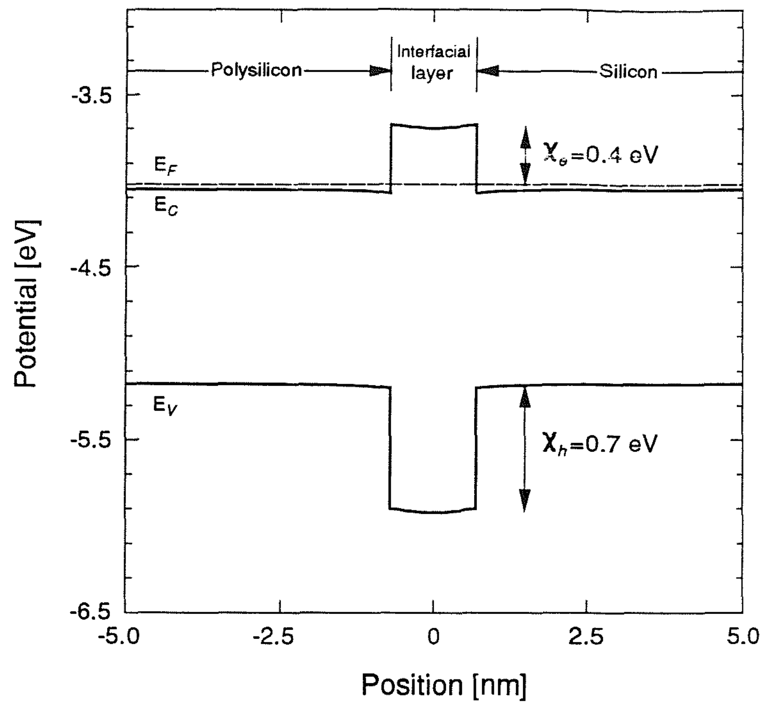

Fig. 5.12(a) Band-diagram of an *nNn* isotype heterojunction, doped to a concentration of 5×10^{19} cm^{-3}. The conduction band offset has been chosen at 0.4 eV, which is equal to the modelled electron barrier height, and the valence band offset at 0.7 eV which equal to the modelled hole barrier height.

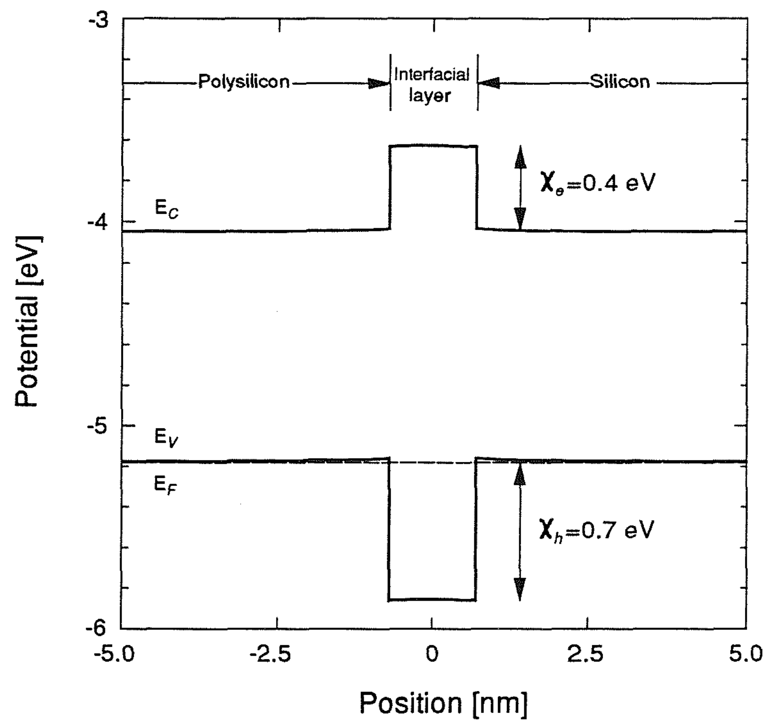

Fig. 5.12(b) Band-diagram of an *pPp* isotype heterojunction, doped to a concentration of 1.5×10^{19} cm^{-3}. The conduction band offset of 0.4 eV, and the valence band offset of 0.7 eV have been chosen to be equal to those in fig. 5.12(a). It can be clearly seen that the resulting electron and hole barrier heights are inconsistent with the experimentally determined values.

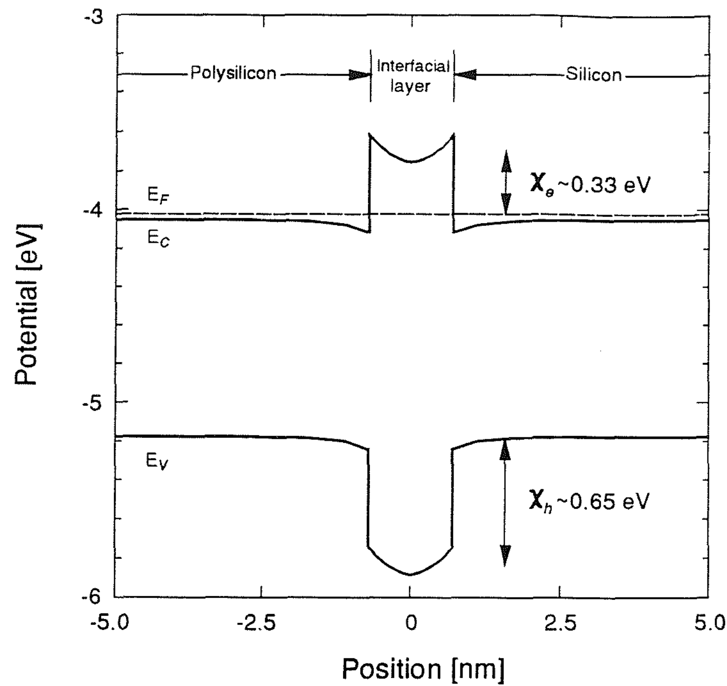

Fig. 5.13(a) Band-diagram of an $nN^{+}n$ isotype heterojunction, with the silicon and polysilicon doped to a concentration of 5×10^{19} cm^{-3}, and the interfacial layer doped to a concentration of 3×10^{20} cm^{-3}. The conduction and valence band offsets have been chosen to be equal at 0.5 eV, although the band bending in the interfacial layer increases the hole barrier to 0.65 eV and reduces the electron barrier to 0.33 eV.

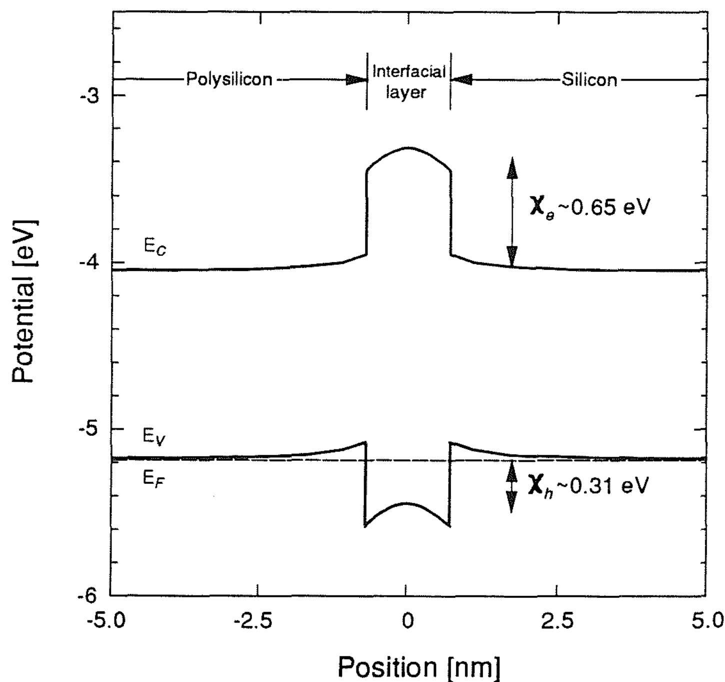

Fig. 5.13(b) Band-diagram of an $pP^{+}p$ isotype heterojunction, with the silicon and polysilicon doped to a concentration of 1.5×10^{19} cm^{-3}, and the interfacial layer doped to a concentration of 3×10^{20} cm^{-3}. The conduction and valence band offsets have been chosen to be equal at 0.5 eV, although the band bending in the interfacial layer increases the electron barrier to 0.65 eV and reduces the hole barrier to 0.31 eV.

in the interfacial 'oxide' layer would be minimal. This does, however, seem to be in agreement with the roughly symmetrical electron and hole barrier heights extracted using the 'Popp' model parameters, as shown in table 5.2.

Returning to the conclusions presented in chapter 2, analysis of the devices with deliberately grown interfacial layers, clearly pointed to tunnelling as the dominant mechanism for both base current and emitter resistance. The main evidence for this conclusion was obtained from modelling the temperature dependence of current gain and emitter resistance. Therefore, any mechanism which proposes to explain the base current reduction and emitter resistance increase for devices with deliberately grown interfacial 'oxide' layers, must be dominated by tunnelling in order to explain the experimental results. Clearly, the potential barriers in the valence and conduction bands in figs. 5.13(a) and 5.13(b) do indeed present tunnelling barriers, and are therefore consistent with the experimental results and modelling in chapter 2. It is also interesting to note that Yung *et al.* [40] could not model the temperature dependence of emitter resistance with a trapezoidal barrier, but had to introduce a triangular barrier. This again, is consistent with the roughly triangular barriers produced by band-bending in fig. 5.13(a).

The choice of conduction and valence band offsets (0.5 eV) and interfacial doping concentration ($3\text{x}10^{20}$ cm^{-3}) provide unique fits to the electron and hole barrier heights in *npn* and *pnp* devices. This point can be illustrated by considering the effect of different band offsets and interfacial doping concentrations on these barrier heights. For example, if the conduction and valence band offsets are increased (or for that matter decreased) from the 0.5 eV required to fit the electron and hole barrier heights, then this systematically increases (or decreases) the barrier heights. This behaviour is shown in fig. 5.14 for an *npn* device with conduction and valence band offsets of 0.7 eV and an interfacial doping concentration of $3\text{x}10^{20}$ cm^{-3}. On comparing with fig. 5.13(a) (which is identical to fig. 5.14, except for reduced band offsets of 0.5 eV), it can be clearly seen that the increase of 0.2 eV in the conduction and valence band offsets has increased *both* the electron and hole barrier heights by approximately 0.2 eV, such that χ_e and χ_h are now 0.52 and 0.87 eV respectively. This cannot explain the experimental observations, and so it can be concluded that a conduction and valence band offset of around 0.5 eV therefore provides a unique fit to the electron and hole barrier heights.

Similarly, if the interfacial doping concentration is increased, then this increases the asymmetry between electron and hole barrier heights. This is illustrated in fig. 5.15 for an *npn* device with conduction and valence band offsets of 0.5 eV and an increased interfacial doping concentration of $1\text{x}10^{21}$ cm^{-3}. Again, on comparing with fig. 5.13(a) (which is identical to fig. 5.15, except for an interfacial layer doping of $3\text{x}10^{20}$ cm^{-3}),

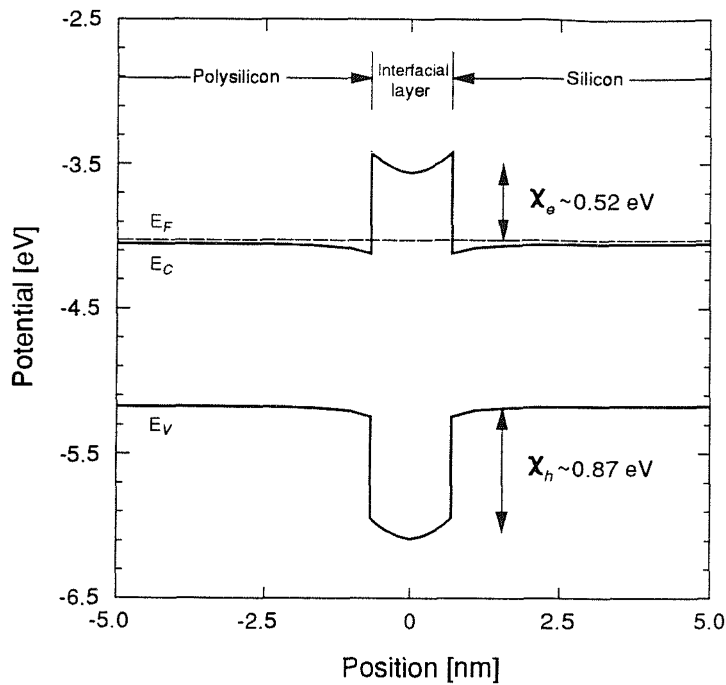

Fig. 5.14 Band-diagram of an $nN^{+}n$ isotype heterojunction, with the silicon and polysilicon doped to a concentration of $5\text{x}10^{19}$ cm^{-3}, and the interfacial layer doped to a concentration of $3\text{x}10^{20}$ cm^{-3}. The conduction and valence band offsets have been chosen to be equal at 0.7 eV. Band-bending in the interfacial layer has resulted in a hole barrier of 0.87 eV and an electron barrier of 0.52 eV.

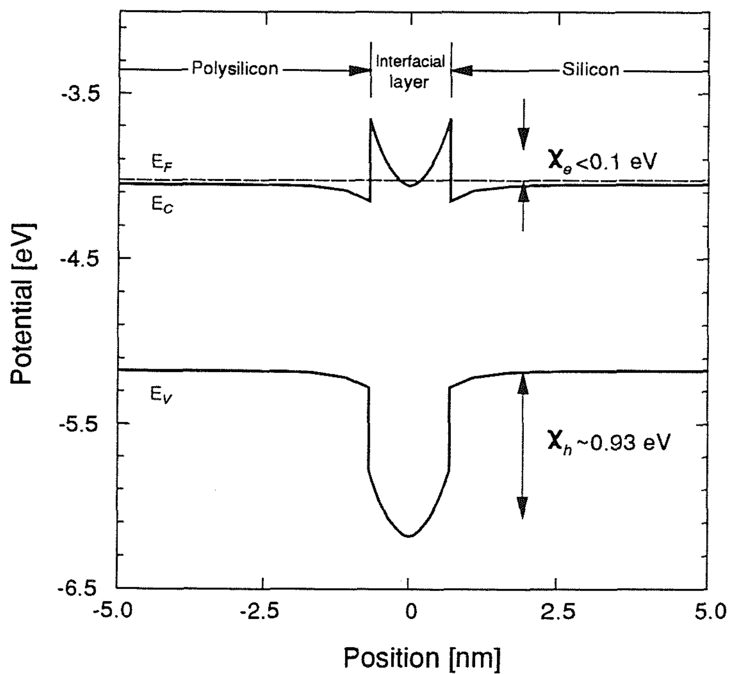

Fig. 5.15 Band-diagram of an $nN^{+}n$ isotype heterojunction, with the silicon and polysilicon doped to a concentration of $5\text{x}10^{19}$ cm^{-3}, and the interfacial layer doped to a concentration of $1\text{x}10^{21}$ cm^{-3}. The conduction and valence band offsets have been chosen to be equal at 0.5 eV. Band-bending in the interfacial layer has resulted in a hole barrier of 0.93 eV and an electron barrier of <0.1 eV.

it can be clearly seen that the increase in doping concentration has virtually eliminated the electron barrier, whilst substantially increasing the hole barrier height to 0.93 eV. As before, this cannot explain the experimental observations, and so it can be concluded that an interfacial doping of around 3×10^{20} cm^{-3} provides a unique fit to the electron and hole barrier heights.

It is worthwhile here to re-examine some of the experimental results for HF devices discussed in chapter 2. It was shown that the base current of HF devices decreased rapidly with increased arsenic segregation to the polysilicon/silicon interface (section 2.4.2 and fig. 2.16). This was attributed to the passivation effect the arsenic performed in reducing the interface state density. It is tempting to suggest that the heterojunction tunnelling mechanism presented in this chapter can also explain the experimental results for HF devices. However, on closer inspection, 2-dimensional modelling of the discontinuous interfacial oxide (section 2.5) clearly pointed to the base current being dominated by those portions of the interface free from oxide. Furthermore, the temperature dependence of the current gain for HF devices (fig. 2.20) also confirmed that tunnelling was not the dominant current gain mechanism. The evidence therefore suggests that the heterojunction tunnelling model presented in this chapter can explain the barrier height inconsistency for *npn* and *pnp* devices with RCA interfacial oxide layers, but cannot explain the base current of HF devices.

5.6 Conclusions

Measurements of base saturation current density and specific emitter interfacial resistivity have been made on *pnp* polysilicon emitter bipolar transistors, with deliberately grown interfacial oxide layers. Interfacial oxide barrier heights for these devices have been extracted, which yield values of 0.31 ± 0.02 eV for holes and either 0.68 ± 0.08 eV or 0.44 ± 0.06 eV for electrons, depending on whether the 'DAS' or 'Popp' band-gap narrowing data has been used. Conversely, barrier heights extracted from *npn* devices, with identical interfacial layer treatments to the *pnp* devices, yield values of >0.72 eV for holes and 0.40 ± 0.01 eV for electrons. It has been shown that if the interfacial oxide layer is treated as a perfect insulator, then this cannot explain this observed asymmetry in barrier heights for electron and holes. An alternative approach has been proposed which assumes that the interfacial 'oxide' layer can be treated as a wide-bandgap semiconductor. The action of segregated dopant in the interfacial layer can cause band-bending, which in turn alters the magnitude of the electron and hole barrier heights. A consistent set of conduction and valence band offsets and interfacial layer doping can be chosen which will fully explain the observed asymmetries in electron and hole barrier heights of *pnp* and *npn* devices.

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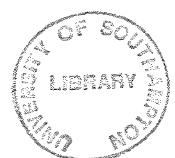

Chapter 6

Conclusions and Further Work

A thorough review of the theoretical and experimental aspects of *npn* polysilicon emitter transistors was undertaken in an attempt to highlight the dominant current gain mechanisms, as a function of fabrication conditions. It was found that if devices were fabricated with a deliberately grown interfacial oxide layer (e.g. an RCA treatment prior to polysilicon deposition), then both the base current and emitter resistance were dominated by tunnelling through the interfacial oxide layer. For devices without a deliberately grown interfacial oxide layer (e.g. a dip etch in HF prior to polysilicon deposition), two distinct regions of operation were found. Firstly, for low concentrations of arsenic in the polysilicon ($<10^{20}$ cm^{-3}), the recombination of carriers via interface states dominated carrier transport, which resulted in a current gain lower than that for an extended emitter device. Secondly, for typical arsenic concentrations of $1-2x10^{20}$ cm^{-3} (as used in many commercial processes), the increased arsenic segregation to the polysilicon/silicon interface passivated the interface states, resulting in a gain enhancement compared with an extended emitter device. In order to fully explain this gain enhancement, it was necessary to model the discontinuous interfacial oxide in two-dimensions. The use of a simple pseudo 2-D model showed that the oxide covered regions of the interface were opaque to minority carriers, so that most of the current flows through the gaps in the oxide. The base current was therefore controlled by the fraction of the interface which is oxide-free, and thus the dominant base current mechanism was the reduction of minority carrier mobility at the polysilicon/silicon interface.

A simple electrical method of measuring the emitter/base junction depth in shallow bipolar devices was presented, based on the measured differences in base sheet resistance for structures either with or without an emitter diffusion. Good agreement was achieved with analytical techniques, such as SIMS and spreading resistance, at deep emitter depths ($>0.1\mu m$). However, the electrical method proved itself more accurate for shallow emitter junction depths ($<0.05\mu m$), which is precisely the regime employed in state-of-the-art bipolar processes.

Investigations of boron diffusion in polysilicon and single-crystal silicon were undertaken in an effort to characterise the necessary anneals required to produce shallow emitter junction *pnp* devices. It was shown that the enhancement of boron diffusivity in polysilicon was only a factor of 50–220 larger than boron diffusivity in single-crystal silicon, which compares with values of around 10^4 for arsenic. This made the attainment of shallow emitter *pnp* devices ($<0.05\mu m$) considerably more difficult than for arsenic doped *npn* devices. Further problems were also encountered, such as boron precipitation in the as-implanted peak, which limited the maximum boron concentration in the polysilicon to $1-2x10^{20}$ cm^{-3}, and a low solid solubility, which limited the maximum electrically active boron concentration to $1-2x10^{19}$ cm^{-3} (for 850°C anneals).

The diffusion analysis of boron in polysilicon employed amorphous as-deposited silicon layers, although it was argued that the results should not be too dissimilar for as-deposited polycrystalline silicon layers. This assumption could be easily tested by comparing both the boron diffusion and device properties of as-deposited amorphous and polycrystalline layers. Furthermore, it was also assumed that the effect of fluorine on the boron diffusivity in polysilicon should be negligible. This hypothesis could be similarly tested by comparing boron diffusion in polysilicon for BF_2 and boron implantations. The effect of fluorine on the integrity of the interfacial oxide could also be studied. It is well known that fluorine reduces oxide stress, which will in turn should accelerate the break-up of the interfacial oxide layer. This behaviour has been observed on RTA annealed samples, and if present in furnace annealed samples, could explain the sharp increase in base current for *pnp* devices annealed for 180 and 240 minutes, compared to a 120 minute drive-in.

Using the shallow emitter *pnp* devices described above, the role of the deliberately grown interfacial oxide layer in influencing the base current and emitter resistance was studied. Effective oxide barrier heights were extracted for these devices, which yielded asymmetrical values of 0.31±0.02 eV for holes and either 0.68±0.08 eV or 0.44±0.06 eV for electrons, depending on which band-gap narrowing model was used ('DAS' or 'Popp'). This same procedure was carried out for *npn* devices with identical interfacial oxide treatments, which also yielded asymmetrical values of >0.72 eV for holes and 0.40±0.01 eV for electrons, although these barrier heights were not consistent with values from the *pnp* devices. It was shown that if the interfacial oxide was treated as a perfect insulator, then this could not explain the observed values of barrier heights. An alternative solution was proposed in which the interfacial layer was treated as a wide-bandgap semiconductor, which predicted tunnelling barriers in both the conduction and valence bands, as required by the modelling analysis. Furthermore, it was shown that the action of segregated dopant in the interfacial layer would facilitate band-bending, which could fully explain the observed barrier height asymmetry in both *pnp* and *npn* devices.

Further work could be attempted to validate the above method of treating the interfacial oxide layer as a wide-bandgap semiconductor. One such way would be to increase the arsenic segregation to the interface in an *npn* device by, for example, reducing the drive-in temperature. If the wide-bandgap semiconducting interfacial 'oxide' layer hypothesis is correct, then the electron barrier should reduce, and the hole barrier increase, for increased segregation to the interface. The tunnelling mechanism itself could also be further validated in one of two ways. Firstly, the thickness of the interfacial 'oxide' layer could be varied, which should result in

exponential changes to both the base current and emitter resistance. Secondly, the temperature dependence of the current gain and emitter resistance of the *pnp* devices with interfacial oxide layers could be investigated.

Appendices

Appendix 1

Derivation of expressions used to describe the blocking mechanisms at the interface in polysilicon emitter transistors

a) Oxide tunnelling model

The expression for the net hole current density tunnelling through the interfacial oxide layer is given by (assuming an *npn* device) [1],

$$J_{pT} = J_{block} = \frac{4\pi q m_{hi}^{*}}{h^{3}} \int_{-\infty}^{E_x} dE\{f_1(E) - f_2(E)\} \int_{-\infty}^{0} T_h(E_x) dE_x \qquad \text{(A1.1)}$$

where m_{hi}^{*} is the effective mass of holes in the oxide, $f_1(E)$ and $f_2(E)$ are the Fermi-Dirac distribution functions for holes in the single-crystal silicon and polysilicon respectively (see fig. A1.1), $T_h(E_x)$ is the hole tunnelling probability, E_x is the energy component of the incident holes in the x direction, q is the electronic charge, and h is Planck's constant. The zero energy reference is taken to be the valence band edge in the monosilicon region. Since holes are minority carriers in the emitter, this means that the Fermi-Dirac distribution functions can be replaced by their Maxwell-Boltzmann approximations,

$$f_1(E) \approx \exp\left[-\frac{(E_{Fp1} - E)}{kT}\right] \qquad \text{(A1.2a)}$$

$$f_2(E) \approx \exp\left[-\frac{(E_{Fp2} - E)}{kT}\right] \qquad \text{(A1.2b)}$$

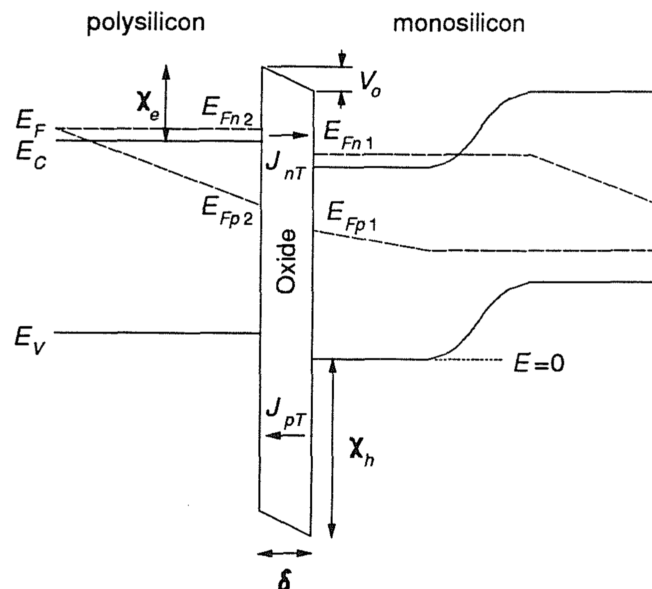

Fig. A1.1 Band-diagram of a polysilicon emitter transistor with an interfacial oxide layer.

[1] R. Stratton, "Volt-current characteristics for tunnelling through insulating films", *J. Phys. Chem. Solids*, vol. 23, pp. 1177–1190, 1962.

where k is Boltzmann's constant, T is the absolute temperature, and E_{Fp1} and E_{Fp2} are the hole quasi-fermi levels on the polysilicon and single-crystal silicon side of the interfacial layer respectively. Substituting equations A1.2a and b into equation A1.1 and evaluating $\int(f_1-f_2)\ dE$ gives,

$$\int_{-\infty}^{E_x} dE\{f_1(E)-f_2(E)\} = kT\left[\exp\left(-\frac{E_{Fp2}}{kT}\right) - \exp\left(-\frac{E_{Fp1}}{kT}\right)\right]\exp\left(\frac{E_x}{kT}\right) \qquad \text{(A1.3)}$$

Using the WKB approximation, the hole tunnelling probability, $T_h(E_x)$, can be expressed as,

$$T_h(E_x) \approx \exp\left[-\frac{4\pi}{h}\int_{x_1}^{x_2}\sqrt{2m_{hi}^*\{V(x)-E_x\}}\ dx\right] \qquad \text{(A1.4)}$$

where $V(x)$ is the barrier potential, and x_1 and x_2 are the classical turning points. Assuming that the tunnelling barrier is rectangular, with a height of χ_h and thickness δ, the hole tunnelling probability can be evaluated as,

$$T_h(E_x) = \exp\left[-\frac{4\pi\delta}{h}\sqrt{2m_{hi}^*(\chi_h+E_x)}\right] \qquad \text{(A1.5)}$$

Expanding the terms under the root sign in equation A1.5 using the binomial series yields,

$$T_h(E_x) \approx \exp\left[-\frac{4\pi\delta}{h}\sqrt{2m_{hi}^*\chi_h}\left\{1 + \frac{1}{2}\left(\frac{E_x}{\chi_h}\right)\right\}\right]$$

$$= \exp(-b_h)\exp(-c_hE_x) \qquad \text{(A1.6)}$$

where,

$$b_h = \frac{4\pi\delta}{h}\sqrt{2m_{hi}^*\chi_h} \qquad \text{(A1.7a)}$$

$$c_h = \frac{2\pi\delta}{h}\sqrt{\frac{2m_{hi}^*}{\chi_h}} \qquad \text{(A1.7b)}$$

Substituting equations A1.6 and A1.3 into equation A1.1 and performing the integration yields,

$$J_{block} = \frac{4\pi q m_{hi}^*(kT)^2}{h^3}\cdot\frac{\exp(-b_h)}{1 - c_hkT}\cdot\left[\exp\left(-\frac{E_{Fp2}}{kT}\right) - \exp\left(-\frac{E_{Fp1}}{kT}\right)\right] \qquad \text{(A1.8)}$$

Now, the hole concentrations, p_1 and p_2 on either side of the interfacial layer can be expressed as,

$$p_{1,2} = N_v\exp\left(-\frac{E_{Fp1,2}}{kT}\right) \qquad \text{(A1.9)}$$

where N_v is the effective density of states in the valence band,

$$N_v = 2\left[\frac{2\pi m_v^*kT}{h^2}\right]^{3/2} \qquad \text{(A3.10)}$$

and m_v^* is the valence band effective density of states mass. Substituting equation A1.9 into equation A1.8 yields the following expression for the tunnelling current,

$$J_{block} = \frac{A_{hi}^* T^2}{N_v} \cdot \frac{\exp(-b_h)}{1 - c_h kT} \cdot (p_1 - p_2) \tag{A1.11}$$

where A_{hi}^* is the effective Richardson constant,

$$A_{hi}^* = \frac{4\pi q m_{hi}^* k^2}{h^3} \tag{A1.12}$$

The effective blocking recombination velocity for holes tunnelling through the oxide layer is thus,

$$T_{block} = \frac{A_{hi}^* T^2}{q N_v} \cdot \frac{\exp(-b_h)}{1 - c_h kT} \tag{A1.13}$$

which is identical to equation 2.13 in chapter 2.

b) Pseudo-grain boundary mobility model

The interfacial region can be treated as a pseudo-grain boundary of thickness Δ, which is characterised by a minority carrier diffusivity D_{pgb}. The hole diffusion current in the pseudo-grain boundary is given by,

$$J_{pgb}(x) = -q D_{pgb} \frac{d p_{pgb}(x)}{dx} \tag{A1.14}$$

where $p_{pgb}(x)$ is the hole distribution in the pseudo-grain boundary. Assuming that the pseudo-grain boundary is thin enough so that recombination occurs only at the interface between the grain boundary and the crystalline silicon (as described through S_l), and not in the bulk of the layer, then (see fig. A1.2),

$$\frac{d p_{pgb}(x)}{dx} \approx -\frac{(p_{IR} - p_{IL})}{\Delta} \tag{A1.15}$$

Substituting equation A1.15 into equation A1.14 then gives an expression for the hole current in the interfacial layer,

$$J_{block} = q \frac{D_{pgb}}{\Delta} (p_{IR} - p_{IL}) \tag{A1.16}$$

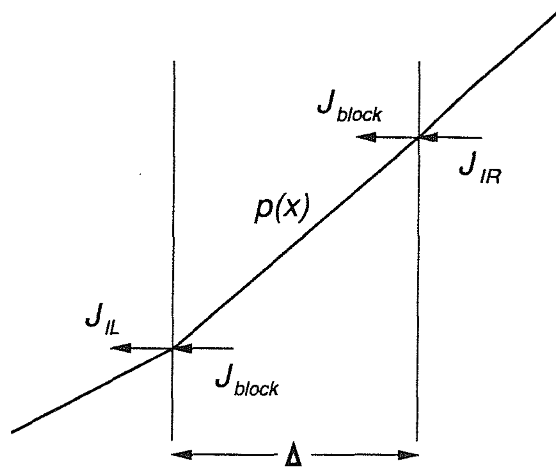

Fig. A1.2 Schematic diagram showing the excess hole concentration in the pseudo-grain boundary.

The effective blocking recombination velocity for hole transport in the pseudo-grain boundary is thus,

$$T_{block} = \frac{D_{pgb}}{\Delta} = \frac{kT}{q}\cdot\frac{\mu_{pgb}}{\Delta} \tag{A1.17}$$

which is identical to equation 2.16 in chapter 2.

c) Segregation model

The thermionic emission currents, J_1 and J_2 for holes emitted across the segregation barrier can be written as (see fig. A1.3) [2],

$$J_1 = p_1\frac{A_h^* T^2}{N_v}\exp\left(-\frac{\nu_b}{kT}\right) \tag{A1.18a}$$

$$J_2 = p_2\frac{A_h^* T^2}{N_v}\exp\left(-\frac{\nu_b}{kT}\right) \tag{A1.18b}$$

where T is the absolute temperature, p_1 and p_2 are the excess hole concentrations on the right and left side of the segregation barrier (see fig. A1.3) respectively, ν_b is the height of the segregation barrier, and N_v is the valence band effective density of states. A_h^* is the effective Richardson constant, which is given by,

$$A_h^* = \frac{4\pi q m_{hth}^* k^2}{h^3} \tag{A1.19}$$

and m^*_{hth} is the effective mass for holes thermionically emitted over the segregation barrier.

The net thermionic emission current is,

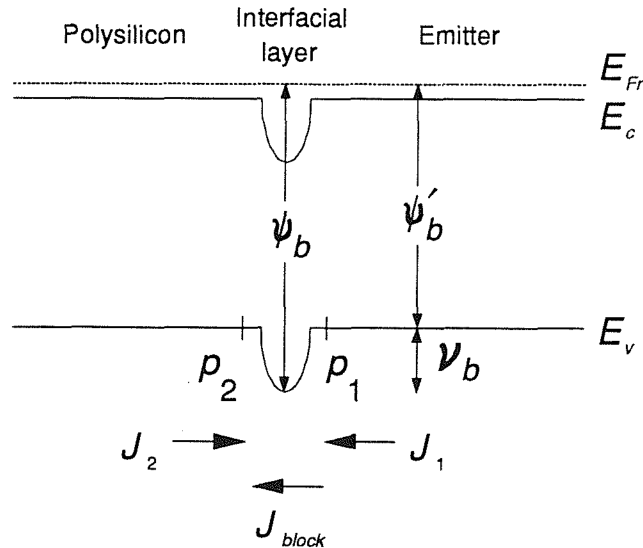

Fig. A1.3 Band-diagram of polysilicon emitter with electrically active dopant segregation barrier at the polysilicon/silicon interface.

[2] B. Jalali and E.S. Yang, "A general model for minority carrier transport in polysilicon emitters", *Solid-State Electron.*, vol. 32, pp. 323–327, 1989.

$$J_{th} = J_{block} = J_1 - J_2$$

$$= \frac{A_h^* T^2}{N_v} \cdot \exp\left(-\frac{v_b}{kT}\right) \cdot (p_1 - p_2) \qquad \text{(A1.20)}$$

The effective blocking recombination velocity for holes thermionically emitted over the segregation barrier at the interface is thus,

$$T_{block} = \frac{A_h^* T^2}{qN_v} \cdot \exp\left(-\frac{v_b}{kT}\right) \qquad \text{(A1.21)}$$

By referring to fig. A1.3 it can be seen that the barrier height v_b can be expressed as,

$$v_b = \psi_b - \psi_b' \qquad \text{(A1.22)}$$

where ψ_b' is the separation of the fermi level and valence band in the emitter, and ψ_b is the separation of the fermi level and valence band at the interface. Now the *equilibrium* hole concentration in the emitter, p_E and at the interface, p_{Int} can be expressed as,

$$p_E = N_v \exp\left[-\frac{\psi_b'}{kT}\right] = \frac{n_{io}^2}{N_E} \qquad \text{(A1.23a)}$$

$$p_{Int} = N_v \exp\left[-\frac{\psi_b}{kT}\right] = \frac{n_{io}^2}{N_{Int}} \qquad \text{(A1.23b)}$$

where N_E and N_{Int} are the electrically active doping concentrations in the emitter and at the interface respectively. Substituting equations A1.23a and b into equation A1.22, and then into equation A1.21 gives,

$$T_{block} = \frac{A_h^* T^2}{qN_v} \cdot \frac{N_E}{N_{Int}} \qquad \text{(A1.24)}$$

which is identical to equation 2.17 in chapter 2.

Appendix 2

Standard pnp processing details

This Appendix describes in detail the standard *pnp* processing schedule that was used for the majority of the devices presented in this thesis. The processing schedule is broken-up into 5 main components, namely field oxide, base/collector formation, emitter formation, extrinsic base formation and metalization. The numbers in braces correspond to the complete process listing, which is given at the end of the Appendix.

a) Field oxide

The starting material is <100> *p*–type boron doped 4 inch silicon wafers (resistivity <0.01Ωcm). A *p*–type boron doped epitaxial silicon layer is then grown with a thickness 2.5–3.0μm and resistivity 0.5–1.5Ωcm (equivalent to a doping concentration of around 1×10^{16} cm^{-3}), which forms the collector region of the bipolar transistor. This epitaxial layer is either grown in-house or provided ready grown by the vendor. A field oxide of thickness 4500–4700Å is then grown {2} in a wet oxygen ambient at a temperature of 1100°C. The time of the oxidation to grow the required thickness of oxide is around 40 minutes (for furnace 4), although a check run is usually performed first. After the required oxide thickness has been obtained, a boron field implant of dose 1×10^{12} cm^{-2} and energy 160keV is performed {4} (see fig. A2.1). This is needed to ensure that the silicon surface remains *p*–type, since many common clean room contaminants (such as sodium and other alkali ions) are essentially *n*–type dopants in silicon (characterised with large diffusivities), and so could invert the surface.

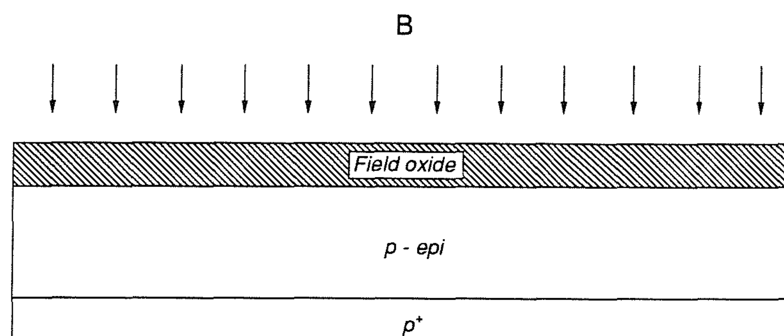

Fig. A2.1 Field oxide formation and boron field implant.

b) Base/collector formation

The base area is defined by mask BA {5}. The field oxide is etched in these regions {7}, exposing the silicon surface (see fig. A2.2). The base area is then oxidised {10} in a dry oxygen ambient at a temperature of 1100°C, to a thickness of 800±50Å. The time of the oxidation is around 18 minutes, although check runs are usually performed first. Phosphorus is then implanted {12} (see fig. A2.3) at a dose of 2×10^{13} cm^{-2} and energy 80keV, through the base oxide, which protects the underlying silicon from implantation damage. The implant energy and base oxide thickness are chosen so that the implant peak resides at the oxide/silicon interface. The base implant is then followed by an anneal at 1000°C for 30 minutes in a dry

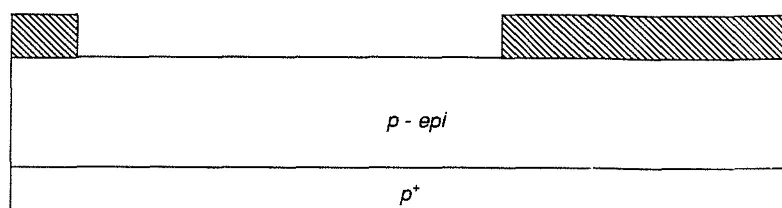

Fig. A2.2 Base area formation.

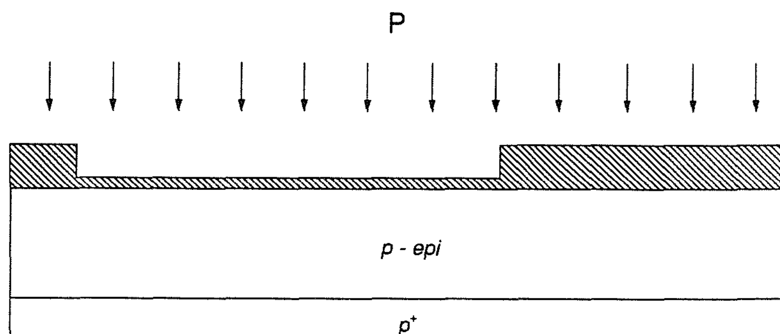

Fig. A2.3 Base implant through the base oxide.

nitrogen ambient {13} to anneal out any implantation damage, and diffuse the phosphorus into the silicon substrate, so forming the base layer. Typically, the base/collector junction is around 0.4μm from the surface. The collector contact is defined by mask NC {15}. The field oxide is etched in these regions {17}, exposing the silicon surface (see fig. A2.4).

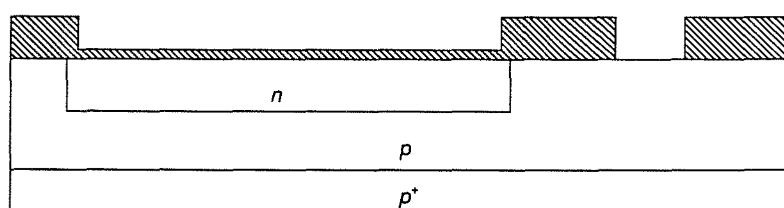

Fig. A2.4 Collector contact formation.

c) Emitter formation

The emitter contact is defined by mask EW {20}. The base oxide is etched in these regions {22}, exposing the silicon surface (see fig. A2.5). Immediately prior to amorphous silicon deposition, the silicon surface at the emitter contact is characterised by an interfacial treatment. This is either a short etch (30 seconds) in hydro-fluoric acid (HF) {26} which is designed to remove any oxide at the surface, or a chemical clean (such as an RCA clean) {27}, which is designed to grow a thin oxide (14±2Å) at the silicon surface. Within 5 minutes of the interfacial treatments, amorphous silicon is deposited {28} at a temperature 560°C and to a thickness of 0.4μm. [The next stage is optional, and involves masking the fronts of the wafers with resist {30} so that the amorphous silicon deposited on the backs of the wafers

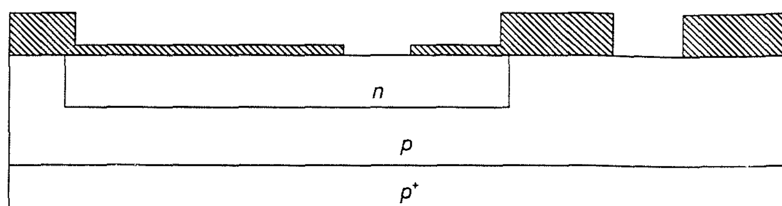

Fig. A2.5 Emitter window formation.

can be removed by a dry etch {32}, after which the resist is removed from the fronts of the wafers {33}. This procedure is required if the substrate is to be used as the collector contact}. Boron difluoride (BF_2) is then implanted {36} at a dose of typically 1×10^{16} cm^{-2} and energy 70keV (see fig. A2.6), which is used as the emitter dopant. The polysilicon emitter is defined by mask P (light field) {37}, and the amorphous silicon is then dry-etched {39} from the remaining areas. After the amorphous silicon has been etched the resist is left on the emitter areas (see fig. A2.7).

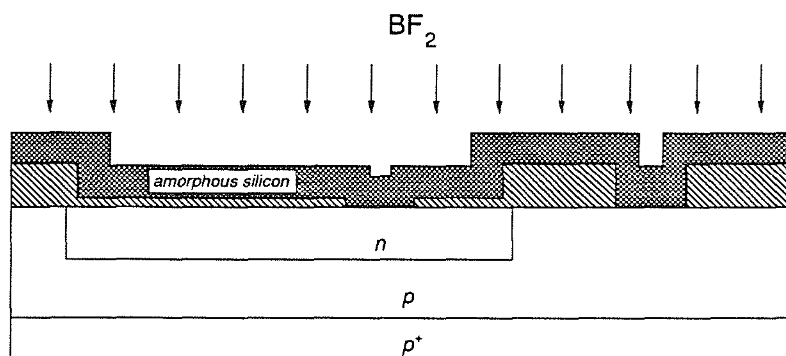

Fig. A2.6 Amorphous silicon deposition and implant.

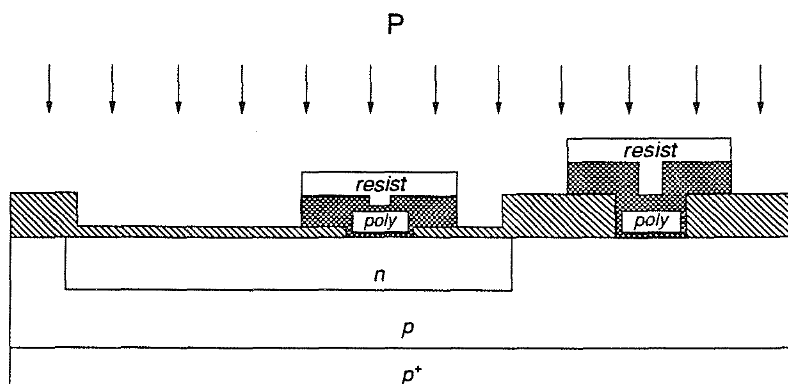

Fig. A2.7 Amorphous silicon etch and extrinsic base implant.

d) Extrinsic base formation

The extrinsic base is formed by implanting phosphorus {41} at a dose of $4x10^{15}$ cm^{-2} and energy 80keV. Those ares covered by resist (i.e. the emitter and collector areas) are protected by the implant (see fig. A2.7), and the extrinsic base region is therefore self-aligned to the emitter contact. The masking resist is next removed from emitter and collector areas {42}, and a low temperature oxide (LTO) deposited {44} to a thickness of 5400–6600Å. A high temperature anneal is then performed {45}, which is typically for 60–240 minutes at a temperature of 850°C in a dry nitrogen ambient. This is designed to activate and diffuse the boron through the polysilicon, forming a shallow emitter/base junction (typically 0.05–0.10μm) in the single-crystal silicon substrate. The anneal also diffuses and activates the extrinsic base implant (see fig. A2.8).

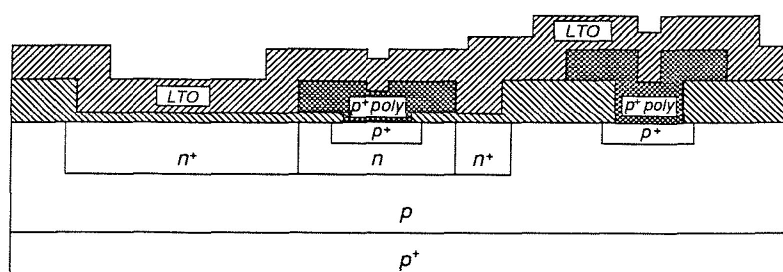

Fig. A2.8 Low temperature oxide (LTO) deposition and emitter drive-in to form shallow single-crystal emitter.

e) Metalization

The contact windows are defined by mask CW {47}. The oxide is etched in these regions {49}, exposing the silicon surface (see fig. A2.9). Immediately prior to metalization, the contact windows are subjected to a 60 second dip etch in 20:1 HF {52}, which ensures that the windows are oxide free. The metal is deposited by sputtering {53}, and consists of a 100nm layer of titanium, followed by 1000nm of aluminium (with 1% silicon). The titanium is used as a barrier layer to prevent the aluminium from diffusing into the silicon, thus causing the emitter and base junctions to short in severe cases (spiking). The metalized regions are then defined by mask M {54}, and the metal dry-etched from the remaining areas {56} (see fig. A2.10). Finally, the contacts are alloyed for 15 minutes at 300°C in a nitrogen/hydrogen ambient to ensure that ohmic contacts are obtained.

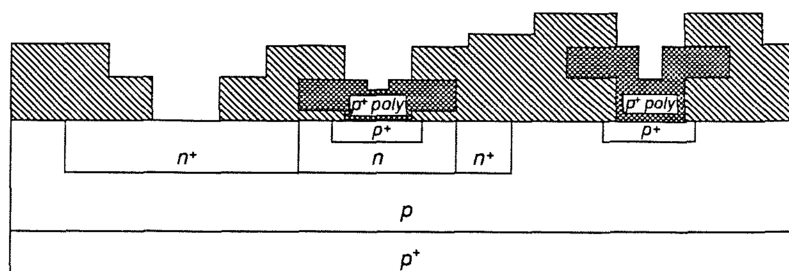

Fig. A2.9 Contact window etch.

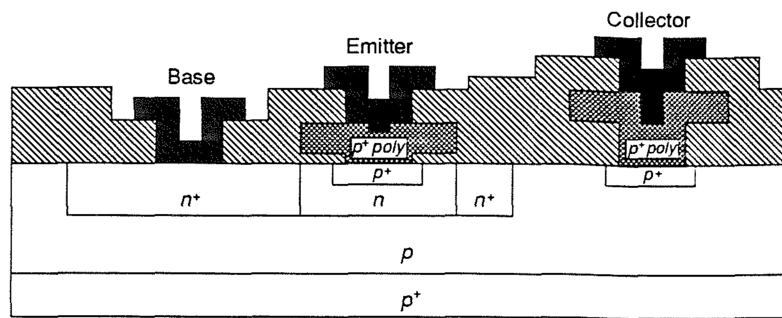

Fig. A2.10 Completed *pnp* polysilicon emitter device.

[PROCESSM STANDARD PNP POLYSILICON EMITTER PROCESSING
[MASK K516M I. POST

1	g/g6	[Batch title page
2	f/f4.7	[Oxidation wet O2, 1100C, Tox=0.45-0.47um
3	g/g11	[See process engineer before proceeding
4	i/ib0	[Boron field implant 1E12 cm-2, 160keV
5	p/pg	[Photolith mask BA dark field
6	p/phb	[Hardbake for wet etch
7	w/w21	[Etch in 7:1 HF at 25C till hydrophobic
8	d/d1	[Resist strip in asher
9	g/g11	[See process engineer before proceeding
10	f/f4.0	[Base oxidation, dry O2, 1100C, Tox=75-85nm
11	g/g11	[See process engineer before proceeding
12	i/ip0	[Phosphorus implant 2E13 cm-2, 80keV
13	f/f10.0	[Base anneal 30mins, 1000C, dry N2
14	g/g11	[See process engineer before proceeding
15	p/pg	[Photolith mask NC dark field
16	p/phb	[Hardbake for wet etch
17	w/w21	[Etch in 7:1 HF at 25C till hydrophobic
18	d/d1	[Resist strip in asher
19	g/g11	[See process engineer before proceeding
20	p/pg	[Photolith mask EW dark field
21	p/phb	[Hardbake for wet etch
22	w/w21	[Etch in 7:1 HF at 25C till hydrophobic
23	d/d1	[Resist strip in asher
24	w/w1	[RCA clean
25	g/g11	[See process engineer before proceeding
26	w/w11	[HF interface treatment
27	w/w14	[RCA interface treatment
28	l/lp5	[Amorphous silicon deposition 400nm, 560C
29	g/g11	[See process engineer before proceeding
30	p/p4	[Frontspin resist, no mask exposure
31	p/phb	[Hardbake for dry etch
32	d/d6	[Dry etch amorphous/poly from backs
33	d/d1	[Resist strip in asher
34	x/x3	[Inspect for complete resist removal
35	g/g11	[See process engineer before proceeding
36	i/ibf0	[BF2 implant 1E16 cm-2, 70keV
37	p/pg	[Photolith mask P light field
38	p/phb	[Hardbake for dry etch
39	d/d5	[Dry etch polysilicon SRS
		[DO NOT RESIST STRIP AFTER THIS STAGE
40	g/g11	[See process engineer before proceeding
41	i/ip0	[Phosphorus implant 4E15 cm-2, 80keV
42	d/d1	[Resist strip in asher
43	x/x3	[Inspect for complete resist removal
44	l/lo1	[LTO deposition 540-660nm
45	f/f7.0	[Emitter drive-in 120 mins, 850C, dry N2
46	g/g11	[See process engineer before proceeding
47	p/pg	[Photolith mask CW dark field
48	p/phb	[Hardbake for wet etch
49	w/w21	[Etch in 7:1 HF at 25C till hydrophobic
50	d/d1	[Resist strip in asher
51	g/g11	[See process engineer before proceeding
52	w/w43	[Pre-metal dip etch in 20:1 HF for 60 secs
53	m/mm3	[Sputter 100nm Ti + 1000nm AlSi

54 p/pg [Photolith mask M light field
55 p/phb [Hardbake for dry etch
56 d/d9 [Dry etch AlSi & Ti SRS
57 d/d1 [Resist strip in asher
58 g/g11 [See process engineer before proceeding
59 f/f9.4 [Alloy/anneal 300C H2/N2, 15 mins

Appendix 3

Electrical measurements set-up

The basic system used to perform electrical measurements, such as Gummel plots and sheet resistance etc., is shown schematically in fig. A3.1. At the heart of the system is a HP4145A semiconductor parameter analyser, which is basically a very versatile programable voltage source, current source, voltmeter and ammeter. The parameter analyser is connected directly to the probe station via 4 SMU's (Source and Measurement Units) which apply the necessary voltages/currents, and then sense the resulting currents/voltages. The SMU's are connected to the wafer via probes which connect directly onto the relevant metal pads (emitter, base, collector etc.) on the wafer surface. It is possible to program the parameter analyser directly from the front panel, although better flexibility is provided if the parameter analyser is programmed through a microcomputer. Connection between the parameter analyser and microcomputer, and periphery devices (such as printer and plotter) is achieved via a HP interface bus (IEEE 488).

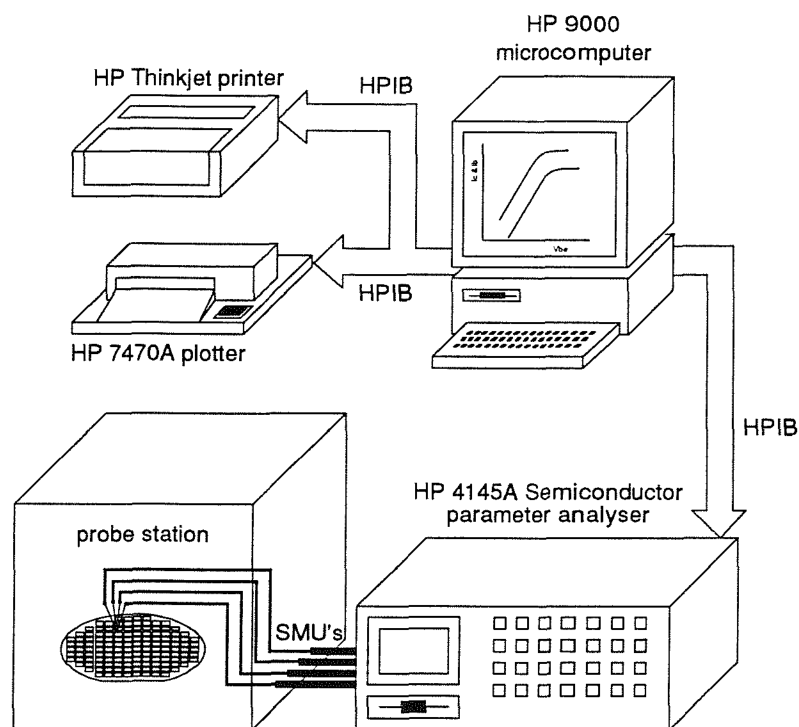

Fig. A3.1 Schematic diagram of electrical measurement set-up.

A suite of software programs have been written ('MEGA') which will automatically program the parameter analyser to provide the correct voltages/currents, measure the resulting voltages/currents, and then read the data into the computer. The following is a brief summary of the main features of 'MEGA'[1].

[1]'MEGA' is run from the softkey panel, with on screen instructions for SMU connections etc.

a) Gummel plots

To produce Gummel plots, the SMU connections are as follows: SMU1 to the emitter, SMU2 to the base, and SMU3 to the collector. Generally, if the transistor has two base contacts then these are tied together to reduce base contact resistance. Furthermore, the collector contact is usually taken from the back of the wafer to limit collector resistance. To perform the measurement, 'MEGA' sets the base (SMU2) and collector (SMU3) to zero volts, and the emitter contact (SMU1) is swept from, say, -0.4 to -1.4 Volts for *npn* transistors (or 0.4 to 1.4 Volts for *pnp* transistors). If collector resistance becomes a problem (the base current exhibits a large increase at high forward bias), then it may be necessary to reverse bias the collector base junction. This is performed by applying, say, 5 Volts to the collector contact (SMU3) for *npn* transistors (or -5 Volts for *pnp* transistors).

b) Van der Pauw sheet resistance

SMU's 1 to 4 are used, which are connected clock-wise around the van der Pauw structure. After selecting the required current range, four measurements of sheet resistance are taken (north, east, south and west around the structure), which are then displayed. If the resulting sheet resistances are non-ohmic, then this can be alleviated by either reducing the measuring current, or using the voltage sources (VS1 & VS2) which have an improved accuracy over the SMU's.

c) 'Ning-Tang' plots

After Gummel data has been measured (or retrieved from disk), then selecting the *Ning-Tang* softkey will cause 'MEGA' to calculate and plot the Ning-Tang data. Selecting the *Analysis* softkey will allow the extraction of the Ning-Tang intercept and gradient. Also produced is data concerning the maximum current gain, base and collector current ideality factors, and base and collector saturation current.

Appendix 4

Mask set details

The design for mask set K516M, which was used for the majority of devices fabricated for this thesis, can be found on the trice ring in //ircp87r/k516mdir. The overall mask design, incorporating all layers, is shown in fig. A4.1.

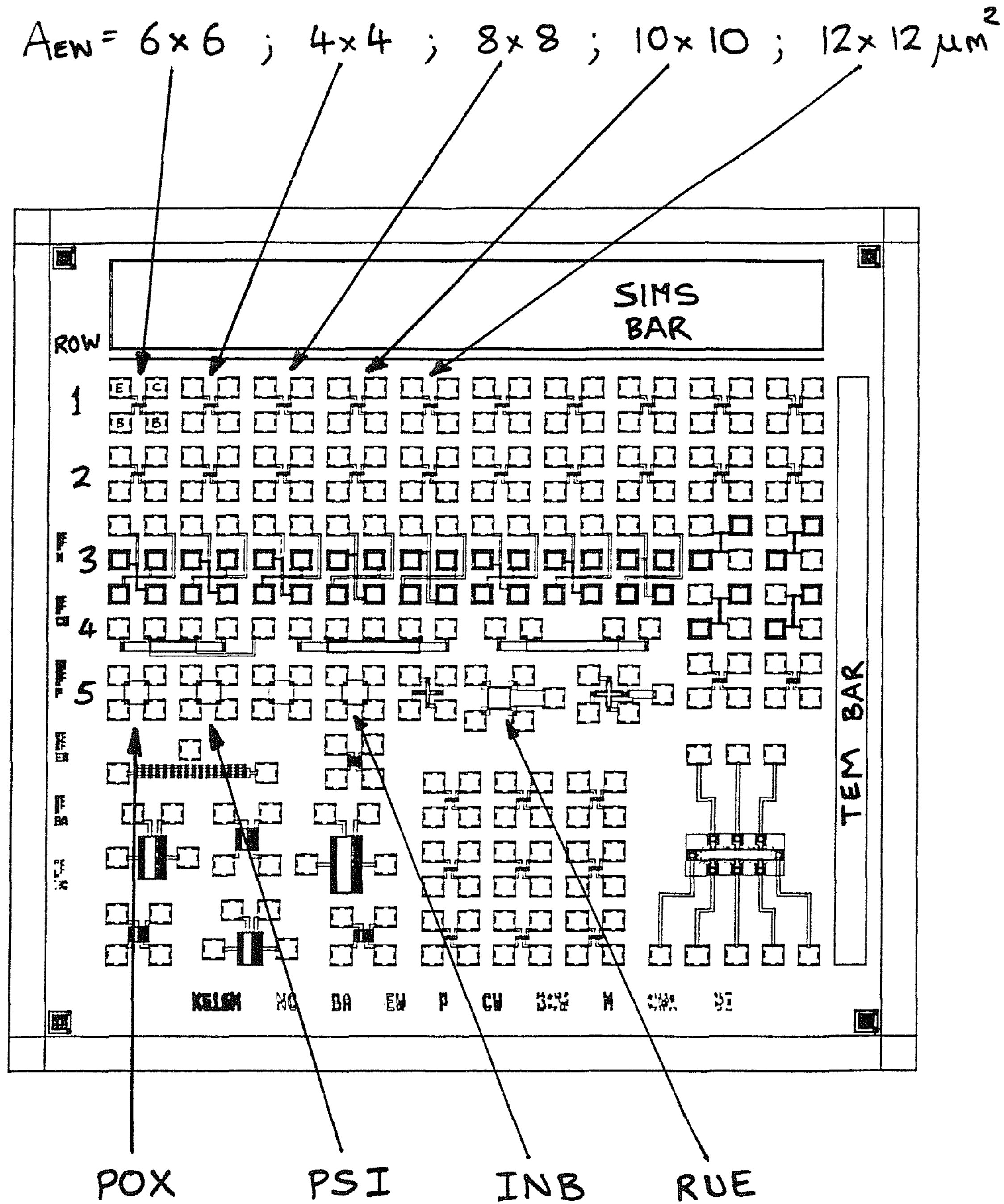

Fig. A4.1 Test mask K516M used for *pnp* polysilicon emitter transistor characterisation.

The top two rows contain discreet transistors with either various emitter window sizes (4X4, 6X6, 8X8, 10X10, 12X12μm^2) with an equal contact window size (6X6μm^2), or various contact window sizes (4X4, 6X6, 8X8, 10X10, 12X12μm^2) with an equal emitter window size (6X6μm^2). Specific transistors that were used for obtaining Gummel plots and performing Ning-Tang analysis are highlighted in fig. A4.1. Row 3 contains 4– and 6–terminal Kelvin structures for measuring emitter and base contact resistances. Rows 4 and 5 contain bar and van der Pauw structures for measuring the sheet resistance of polysilicon (POX), polysilicon with an emitter diffusion (PSI), and base resistance either with (RUE) or without (INB) an emitter diffusion. The 8 transistors in the lower left of the mask are large area devices (ranging from an emitter window area of 12X48 to 80X320μm^2), which are useful for diode capacitance measurements. The matrix of 9 transistors at the lower centre of the mask have sun-micron emitter windows (ranging from 3.0X3.0μm^2 down to 0.3X0.3μm^2), whilst the structure in the lower right-hand corner is for performing Hall measurements on the polysilicon. The large bar structure at the top of the mask (0.5X4mm^2) is used for SIMS and spreading resistance analysis, whilst the bar on the right-hand side is useful for cross-sectional TEM.

Fig. A4.2 shows a close-up of the as-drawn dimensions of a typical polysilicon emitter transistor used in this study to measure collector and base currents (EW=10X10μm^2).

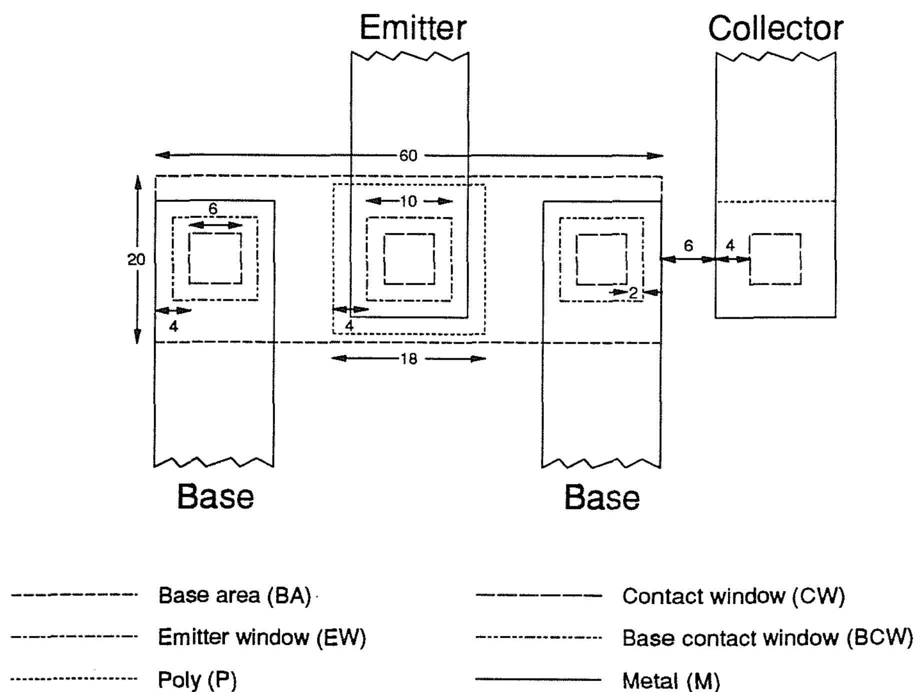

Fig. A4.2 Plan view of an as-drawn polysilicon emitter transistor with a 10X10μm^2 emitter window.

Appendix 5

HQUPETS input files for generating barrier band diagrams

The following Appendix lists and describes the necessary files to allow HQUPETS to generate band diagrams for the heterojunction barriers discussed in chapter 5. The following example will describe files which are needed to generate the band diagram for the barrier in the *npn* device in fig. 5.13(a). The interfacial layer is taken to be 14Å thick, with a band-gap of 2.125 eV (with equal conduction and valence band offsets of 0.5 eV) and doped to a concentration of 3×10^{20} cm^{-3}. On either side of the interfacial layer are the *n*–type polysilicon and silicon which are doped to a concentration of 5×10^{19} cm^{-3}. The *n*–type silicon is modelled by the single-crystal emitter of a wide-bandgap emitter bipolar transistor, whilst the wide bandgap emitter is used to model the interfacial oxide and *n*–type polysilicon by varying the affinity and band-gap in the wide bandgap emitter.

The generic name for the HQUPETS files is assumed to be 'barrier'. The input file (barrier.inp) is as follows (refer to the HQUPETS manual for the meaning of each keyword):

```
BARRIER.INP
RUNTYPE:       SIMULATION of isotype heterojunction barriers
STRUCTURE:     SYMMETRICAL
COMM:          Model barrier as SiC emitter
COLLECTOR:     BEG=0.0  END=7.0  DEP=0.19  PROF=CONST  CONC=1E16
BASE:          BEG=0.0  END=6.0  DEP=0.13  PROF=CONST  CONC=5E17
EMITTER:       BEG=0.0  END=1.0  DEP=0.02  PROF=CONST  CONC=5.049E19
SIC:           BEG=0.0  END=1.0  DEP=0.01  PROF=INPUT  DIFF=1E-8
E-CONTACT:     BEG=0.0  END=1.0  BIAS=0.0
B-CONTACT:     BEG=3.0  END=6.0  BIAS=0.0
S-CONTACT:     BEG=0.0  END=7.0  BIAS=0.0
SCP:           AFF=INPUT  GAP=INPUT
MESH:          YMIN=0.0004  XMIN=17
TEMP:          SIMTEMP=295
OUTPUT:        LEVEL=3
END
```

Additional files are also required which describe the doping profile in the wide bandgap emitter (barrier.sic), and the affinity (barrier.aff) and bandgap (barrier.gap) in the wide bandgap emitter. These files are listed below:

```
BARRIER.SIC
0.0000         5.00E19
0.0050         5.00E19
0.0060         5.00E19
0.0000         5.00E19
0.0070         5.00E19
0.0080         5.00E19
0.0085         5.00E19
0.0086         3.00E20
0.0087         3.00E20
0.0090         3.00E20
0.0095         3.00E20
0.0100         3.00E20
```

BARRIER.AFF	
0.0000	4.05
0.0050	4.05
0.0060	4.05
0.0000	4.05
0.0070	4.05
0.0080	4.05
0.0085	4.05
0.0086	3.55
0.0087	3.55
0.0090	3.55
0.0095	3.55
0.0100	3.55

BARRIER.GAP	
0.0000	1.125
0.0050	1.125
0.0060	1.125
0.0000	1.125
0.0070	1.125
0.0080	1.125
0.0085	1.125
0.0086	2.125
0.0087	2.125
0.0090	2.125
0.0095	2.125
0.0100	2.125

The output from the HQUPETS simulation is contained in the file 'barrier.out' in the form of potential against distance. From this data it is then a simple task to extract the band edges (i.e. conduction band edge = potential – affinity, and valence band edge = conduction band edge – band-gap).

Appendix 6

Published papers resulting from the work in this thesis

[1] I.R.C. Post and P. Ashburn, "Fabrication and characterisation of pnp polysilicon emitter bipolar transistors", *Proc. 19th European Solid-State Device Research Conference (ESSDERC) 1989*, pp. 453–456.

[2] I.R.C. Post and P. Ashburn, "Electrical method for measuring emitter depths of shallow bipolar transistors", *Electron. Lett.*, vol. 26, pp. 30–31, 1990.

[3] I.R.C. Post and P. Ashburn, "Investigation of Boron diffusion in polysilicon and its application to the design of p–n–p polysilicon emitter bipolar transistors with shallow junctions", *IEEE Trans. Electron Devices*, vol. 38, pp. 2442–2451, 1991.

[4] I.R.C. Post, P. Ashburn and G.R. Wolstenholme, "Polysilicon emitters for bipolar transistors: A review and re-evaluation of theory and experiment", *IEEE Trans. Electron Devices*, vol. 39, 1992.

[5] I.R.C. Post, P. Ashburn and A. Nouailhat, "An investigation of the inconsistency in barrier heights for p–n–p and n–p–n polysilicon emitter bipolar transistors", *Submitted to IEEE Trans. Electron Devices.*

Appendix 7

List of symbols

Symbol	Description
A_{EW}	Emitter window area (μm^2)
A_{ox}	Emitter area with an interfacial oxide layer (μm^2)
A_{nox}	Emitter area without an interfacial oxide layer (μm^2)
A_{ei}^*	Effective Richardson constant for electrons in the interfacial oxide layer (A cm^2 K^2)
A_{hi}^*	Effective Richardson constant for holes in the interfacial oxide layer (A cm^2 K^2)
A_h	Effective Richardson constant for holes in silicon (A cm^2 K^2)
A_o	Richardson constant for free electrons (1.202×10^6 A cm^2 K^2)
χ_e	Electron interfacial oxide layer barrier height (eV)
χ_h	Hole interfacial oxide layer barrier height (eV)
c_p	Capture cross-section for interface states (cm^2)
D_g	Hole diffusivity in the polysilicon grain (cm^2 s^{-1})
D_{Bpoly}	Boron diffusivity in polysilicon (cm^2 s^{-1})
D_{Bp1}	Pre-exponential factor for intrinsic boron diffusivity in polysilicon (cm^2 s^{-1})
D_{Bsil}	Boron diffusivity in silicon (cm^2 s^{-1})
D_{Bs1}	Pre-exponential factor for intrinsic boron diffusivity in silicon (cm^2 s^{-1})
D_{Bs2}	Pre-exponential factor for extrinsic boron diffusivity in silicon (cm^2 s^{-1})
DEF	Diffusion enhancement factor
E_a	Activation energy for boron diffusion in polysilicon and silicon (eV)
E_C	Conduction band edge (eV)
E_F	Fermi level (eV)
E_{Fn}	Electron quasi-fermi level (eV)
E_{Fp}	Hole quasi-fermi level (eV)
E_V	Valence band edge (eV)
δ	Interfacial oxide layer thickness (Å)
Δ	Pseudo-grain boundary thickness (Å)
ΔE_g^{app}	Apparent bandgap narrowing (eV)
G_{eff}	Effective emitter Gummel number (s cm^{-4})
h	Planck's constant (6.626×10^{-34} J s)
I_B	Base current (A)
I_C	Collector current (A)
J_{BO}	Base saturation current density (A cm^{-2})
J_{CO}	Collector saturation current density (A cm^{-2})
J_B	Base current density (A cm^{-2})
J_C	Collector current density (A cm^{-2})
J_{nt}	Electron tunnelling current density (A cm^{-2})
J_p	Hole current density (A cm^{-2})
J_{pt}	Hole tunnelling current density (A cm^{-2})
k	Boltzmann's constant (1.38×10^{-23} J K^{-1})
L_g	Hole diffusion length in the polysilicon grain (cm)

L_p	Hole diffusion length (cm)
m_c^*	Conduction band effective density of states mass (kg)
m_{ei}^*	Effective electron mass in the interfacial oxide layer (kg)
m_{hi}^*	Effective hole mass in the interfacial oxide layer (kg)
m_{hth}^*	Effective mass of holes for thermionic emission (kg)
m_o	Free electron mass (9.109×10^{-31} kg)
m_v^*	Valence band effective density of states mass (kg)
μ_B	Majority carrier mobility in the base (cm^2 V^{-1}s^{-1})
μ_p	Minority hole mobility (cm^2 V^{-1}s^{-1})
μ_{pgb}	Pseudo-grain boundary minority carrier mobility (cm^2 V^{-1}s^{-1})
N_c	Effective density of states in the conduction band (cm^{-3})
N_B	Electrically active base doping concentration (cm^{-3})
N_E	Electrically active emitter doping concentration (cm^{-3})
N_{Bpeak}	Base doping concentration at the emitter contact (cm^{-3})
N_{Epeak}	Emitter doping concentration at the emitter contact (cm^{-3})
N_{Eeff}	Emitter effective doping concentration (cm^{-3})
N_{Int}	Electrically active doping concentration at the polysilicon/silicon (cm^{-3})
n_{io}	Intrinsic carrier concentration in silicon (cm^{-3})
N_{it}	Interface state density (cm^{-2})
N_v	Effective density of states in the valence band (cm^{-3})
p	Excess hole concentration (cm^{-3})
q	Electronic charge (1.602×10^{-19} C)
R_{IB}	Base sheet resistance without emitter diffusion (Ω/□)
R_{UE}	Base sheet resistance under the emitter (Ω/□)
R_{int}	Specific emitter interfacial resistance (Ω μm^2)
S_g	Recombination velocity for carrier transport in the polysilicon (cm s^{-1})
S_I	Recombination velocity via traps at the polysilicon/silicon interface (cm s^{-1})
S_p	Recombination velocity at the polysilicon/silicon interface (cm s^{-1})
S_M	Recombination velocity at the metal contact (cm s^{-1})
T	Absolute temperature (K)
τ_p	Hole lifetime (s)
T_{block}	Blocking recombination velocity at the polysilicon/silicon interface (cm s^{-1})
T_{pgb}	Pseudo-grain boundary blocking recombination velocity (cm s^{-1})
T_{th}	Segregation thermionic emission blocking recombination velocity (cm s^{-1})
T_{tun}	Oxide tunnelling blocking recombination velocity (cm s^{-1})
V_{BE}	Base/emitter voltage (V)
V_{CB}	Collector/base voltage (V)
v_{th}	Thermal velocity (cm s^{-1})
W_E	Quasi neutral emitter depth (cm)
W_E'	Metallurgical emitter depth (cm)

W_E''	Quasi neutral emitter depth plus depletion width (cm)
W_B	Quasi neutral base depth (cm)
W_p	Polysilicon thickness (cm)