Switching mechanisms of Cu/SiC resistive memories with W and Au counter electrodes

Katrina A. Morgan[1], Junqing Fan[2], Robert P. Gowers[2], Liudi Jiang and Cornelis H. de Groot[1]
[1]*Nano Research Group, Electronics and Computer Science, University of Southampton, Southampton, Hampshire, SO171BJ, UK*
[2] *Faculty of Engineering and the Environment, University of Southampton, Southampton, Hampshire, SO171BJ, UK*
Email: kam2g11@soton.ac.uk

Introduction

Resistive memory is an emerging non-volatile memory, with high density, low power and a simple structure [1]. The memories switch between high resistance state (HRS) and low resistance state (LRS). The physical mechanism is based upon a conductive filament forming and rupturing between two electrodes. In electrochemical metallization memory (ECM) this filament is made from cations, originating from an active electrode, e.g. Cu or Ag [2]. The counter electrode is normally an inert material such as Pt or W. Although much research has been conducted into resistive memory, the role of the filament reduction at the counter electrode in ECM memories is still not fully understood.

Device Results

Amorphous SiC Cu/a-SiC/Au memory devices have been fabricated the University of Southampton, as described in previous publications [3,4]. These devices exhibit extremely high $R_{OFF}/R_{ON} \geq 10^8$, the highest for ECM memories. The ON state conduction is identified as ohmic, through Cu filaments, whilst the OFF state is Schottky emission. These memories withstand extreme high doses of gamma radiation, with no change in conduction mechanisms or switching properties, indicating use for harsh environments. In order to further investigate the filament reduction mechanism of these devices, Cu/a-SiC/W memories were fabricated. Measurements of memories with Au and W electrodes are shown and discussed.

Fig. 1 and 2 shows typical Au and W memories with multiple DC and pulsed cycles with ultra-high ratio for both electrodes. A difference in OFF state current can be seen, whereby the Cu/a-SiC/W memory exhibits a lower OFF state current. This could be attributed to fewer remaining filaments following the RESET. A lower OFF state current leads to higher R_{OFF}/R_{ON}, beneficial for multi-level switching. Both the W and Au memories exhibit multi-level switching. This can be seen in Fig.3 for Cu/a-SiC/W for multiple DC cycles, whereby the current is limited in the SET, using different current compliances. A relation between current compliance and I_{RESET} can be seen, showing a smaller current is required for RESET, when a reduced current compliance is used in the previous SET. For multi-level switching applications it is the I_{ON} rather than the I_{RESET} that would be measured. Fig 4. Displays I_{ON} and I_{OFF}, taken from 0.1V DC reads, after SET and RESET DC cycles for multiple SET current compliances. The boxplots show statistical variation between device-to-device and cycle-to-cycle. The W devices indicate 4 different ON levels, compared to the 3 levels for Au devices. The Au devices were unable to remain ON when a current compliance of 1e-7A was used, unlike the W devices. This indicates the counter electrode material choice impacts on the filament formation mechanism. To verify the filament conduction mechanism in the ON state, I-V plots were measured as shown in Fig. 5. This clearly shows both Au and W LRS conduction is ohmic. Further investigations into the SET and RESET mechanisms were conducted using pulsed measurements as shown in Fig. 6 for W devices. In comparison to previously published results for Au, as presented in [2], the W devices display the same relations between pulse time and SET and RESET voltages, in agreement with an analytical model [5]. For Au an ion hopping distance of 1.52nm was extracted, compared to a value of 1.12nm for W. A difference in V_{RESET} exists whereby a higher voltage for W devices is required. The filament diameter extracted using eq. 1, gives ~1nm for W, compared to a much larger ~4nm for Au. This difference in filament diameter indicates a difference in filament reduction at the counter electrode.

$$\tau_{pulse} \propto e^{\frac{E_{A0}8\rho k_{th}}{kV^2}} \quad (1)$$

Conclusion

Ultra-high R_{OFF}/R_{ON} SiC resistive memory have been fabricated. The counter electrode material type has shown to affect the switching properties of resistive memories. Reduced OFF state resistance, ability to SET with lower current compliances, and a smaller diameter are seen for Cu/a-SiC/W devices, compared to Cu/a-SiC/Au. Further comparison of this data with analytical model will further develop the understanding of the filament reduction at the counter electrode and therefore the switching mechanism.

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[3] K. Morgan *et al.*, *AIP Advances*, vol.56, p. 077121, (2015). [4] L. Zhong *et al.*, *Sol. State Elec.*, vol. 94, p. 98, (2014).
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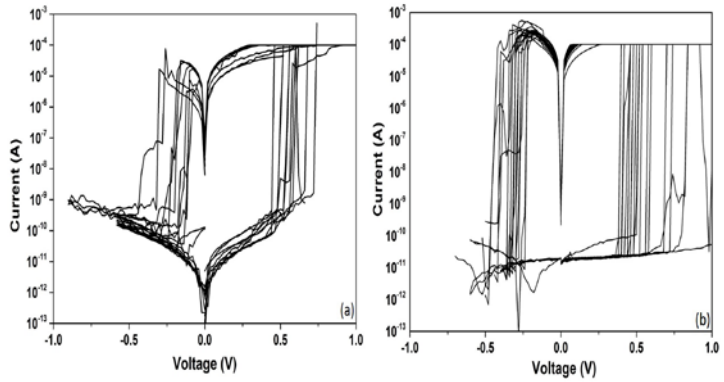

Fig. 1. Typical DC sweep of ultra-high R_{OFF}/R_{ON} Cu/SiC resistive memory with counter electrodes of (a) Au and (b) W.

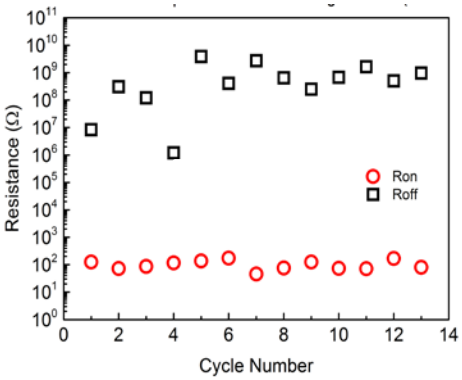

Fig. 2. Pulsed measurements for Cu/SiC/W with R_{ON}~100Ω and R_{ON}~1GΩ.

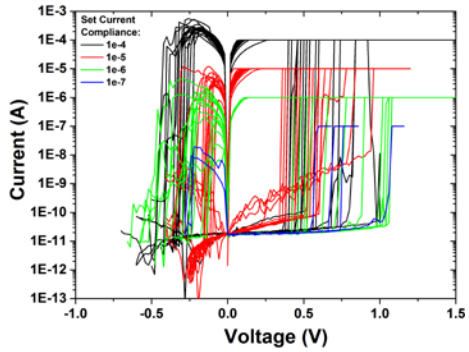

Fig. 3. Cu/SiC/W DC sweeps showing multi-level switching using four different current compliance levels.

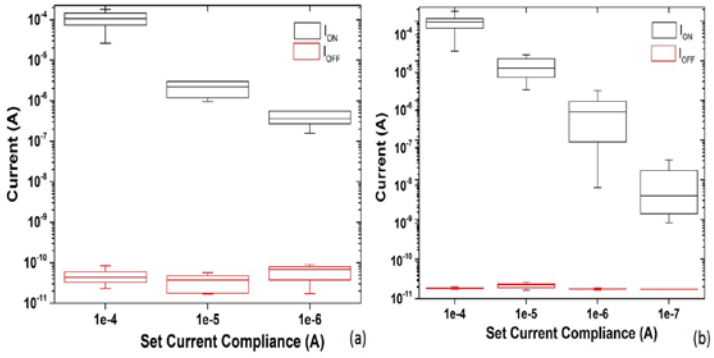

Fig. 4. Boxplots of I_{OFF} and I_{ON} read during DC cycles, using 0.1V DC read. Different current compliance levels used during SET, reducing I_{ON}, whilst I_{OFF} remains unchanged. 3 levels seen for Cu/SiC resistive memories with (a) Au counter electrodes, whilst 4 levels seen for resistive memories with (b) W counter electrodes.

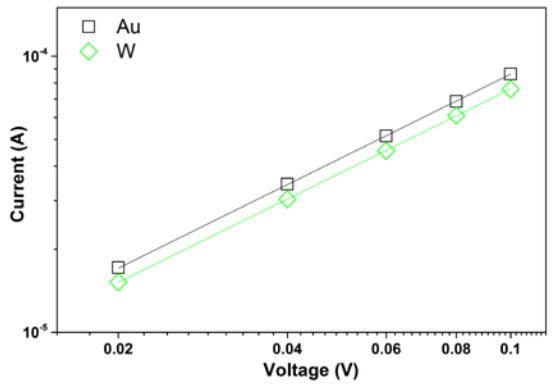

Fig. 5. I-V plots of Cu/SiC memories with Au and W electrodes showing LRS with gradient of 1.00 for both materials indicating ohmic conduction.

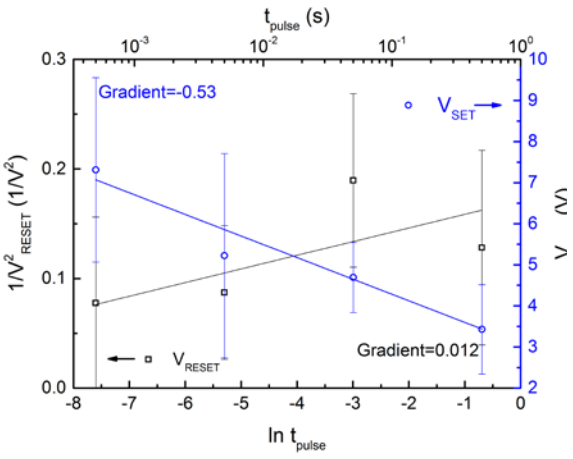

Fig. 6. Time dependencies of pulsed switching for Cu/SiC/W memories, using pulse widths of 500µs-0.5s.