An FPGA-based Instrument for en-masse RRAM Characterisation with ns Pulsing Resolution

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***Abstract*—An FPGA-based instrument with capabilities of on-board oscilloscope and nanoscale pulsing ($70\,ns@\pm 10\,V$) is presented, thus allowing exploration of the nano-scale switching of RRAM devices. The system possesses less than $1\,\%$ read-out error for resistance range between $1\,k\Omega$ to $1\,M\Omega$, and demonstrated its functionality on characterizing solid-state prototype RRAM devices on wafer; devices exhibiting gradual switching behaviour under pulsing with duration spanning between $30\,ns$ to $100\,us$. The data conversion error-induced degradation on read-out accuracy is studied extensively and verified by standard linear resistor measurements. The integrated oscilloscope capability extends the versatility of our instrument, rendering a powerful tool for processing development of emerging memory technologies but also for testing theoretical hypotheses arising in the new field of memristors.**

***Index Terms*—FPGA, RRAM, Crossbar, memristor array.**

I. Introduction

RESISTIVE Random Access Memory (RRAM) is a quickly evolving field promising to bring cheap, extremely downscaled electronic components (memristors [1]), intrinsically capable of storing information [2] to a wide range of applications. These would include memory arrays [3], reconfigurable circuits [4], [5], logic [6] and neuromorphic computing [7], [8].

RRAM's scaling promise hinges on two key advantages: The first is the arrangement of devices in highly compact crossbar arrays, whereby sets of mutually perpendicular word-line (WL) and bit-line (BL) electrodes sandwich the active material of a cell at each junction point, as shown in Fig. 1(a). If all inactive (i.e. not leading to the target device) WLs and BLs are shorted together, any idealised (i.e. negligible parasitics) crossbar array can be reduced to a 2×2 architecture as in Fig. 1(b). This simplifies analysis [9] and is based on a connectivity feature employed by most, common crossbar biasing schemes [10]. However, even an ideal crossbar configuration suffers from the issue of sneak paths [11], where a voltage applied to a target device causes current to flow through unselected devices within the crossbar. The problem is exacerbated by the presence of parasitics, most notably

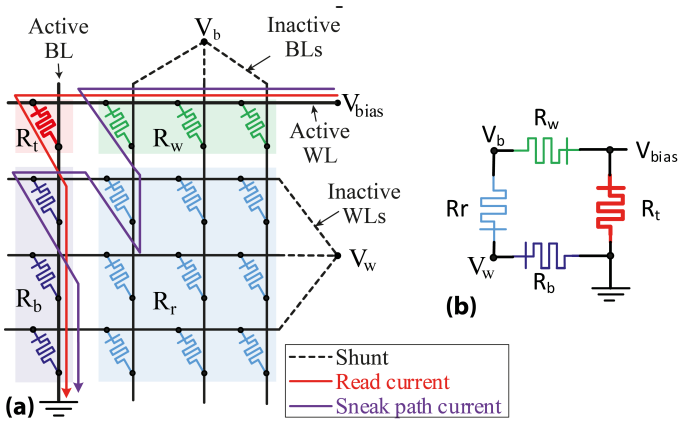

Figure 1. Crossbar array fundamentals. (a) Diagram of crossbar array illustrating the sneak path problem. (b) Reduction of ideal crossbar array to a 2×2 architecture when all inactive word- and bit-lines (WL, BL) are shorted together. Red memristor: target device R_t. Green memristors: devices sharing WL with R_t (WL complement), lumped into R_w. Blue memristors: BL complement, lumped into R_b. Light blue memristors: Rest-of-array, lumped into R_r.

electrode ("line") resistance. As a result, cell read-out accuracy is reduced and write operations may disturb the memory state of adjacent devices, which is why strategies to mitigate sneak path effects are an area of active research. These include introducing CMOS [12], or emerging devices [13] as 'selector' elements to isolate the target device from the rest of the array, and the employment of active biasing of inactive WLs and BLs in order to divert sneak currents [10] amongst other techniques [14]. The second key advantage of RRAM concerns the potential for single-device, multi-level memory cells [2].

Systems that can control multi-level crossbar memory arrays with optimised read-out accuracy and limited write cross-talk have already been built for the purpose of process development automation and applications employing small crossbars [15], [16]. These array control instruments consist of custom-made array handler printed circuit boards (PCBs) paired with a micro-controller-based (LPC1768) control module running custom-made software. This configuration allows great operational flexibility at a low price, but performance is typically limited by the low speed of the micro-controller's data converters. In this work we present results from an upgraded array control instrument that utilises the handler PCB from [15] with an in-house designed field-programmable gate array-based (FPGA) control module employing high speed data converters. The system is capable of sourcing $70\,ns$ pulses at up to $\pm10\,V$ (full-duration, half-maximum (FDHM)) and can sample analogue input signals at up to $65\,MHz$. We demonstrate

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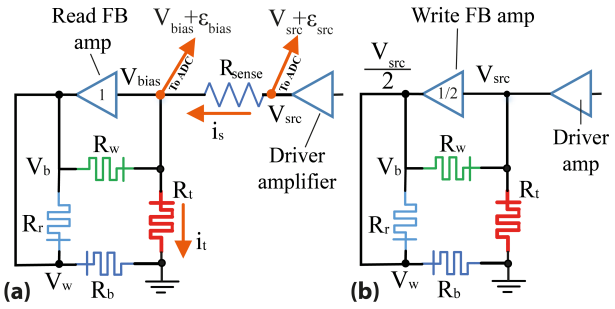

Figure 2. Read and write bias schemes used by our array control instrument. (a) Read-out configuration: Bias is applied to the target device (R_t) via a sense resistor whilst a buffer (unity gain) amplifier bootstraps R_w to ensure that i_t matches i_s as closely as possible. (b) Write configuration: Feedback ensures that the voltage applied to the WL and BL complements is half the voltage across R_t whilst potentially very low resistance path through R_r is kept shunted.

exploration of RRAM device switching characteristics under ns-scale pulsing as well as transient RRAM device behaviour capture via on-board oscilloscope capabilities serving as a cheap, fully customisable, user-friendly integrated platform.

The paper is organized as follows: Section II specifies the read- and write-mode biasing schemes used by our instrument and briefly discusses the influence of basic data converter-induced read-out errors. Section III presents the key aspects of system implementation. In section IV, we benchmark the performance of the upgraded system vs. its predecessor, show results from our on-board oscilloscope and demonstrate the instrument's capability for ns-scale pulsing. In section V we use our developed system to explore prototype RRAM device switching characteristics under pulsing stimulation. Section VI provides a discussion on the results and concludes the paper.

II. Theoretical Framework

The array control instrument used in this work, employs the potential divider-based read-out scheme illustrated in Fig. 2(a) with $V_{src} = 0.5\,V$ for consistency with previous work [15]. It is worth noting that other read-out schemes are also possible including continuous current schemes with different line voltage arrangements, but also more advanced implementations such as switch-capacitor-based CDS [17]. We plan to study these in the near future. The write scheme is the standard '$V_{write}/2$' method [10], as in Fig. 2(b) that offers a good compromise between reducing unwanted cross-programming and restricting write operation power dissipation [18]: Gain $1/2$ amplifiers act as a cross-talk protection mechanism by ensuring that the bit- and word-complement devices are not subjected to more than half the voltage applied to the DUT during the write operation. Simultaneously, the voltage drop across R_r remains close to zero. This dramatically reduces the potential for write cross-talk (where modifying the resistive state (RS) of the DUT causes modifications in non-DUT devices).

During the read procedure, the driver amplifier applies a voltage to the crossbar array via a sense resistor R_{sense}. Buffer amplifiers ensure that R_w (R_r) remain shunted (bootstrapped) respectively and thus conduct a minimum amount of current. This ensures that the current through R_{sense} is closely matched to the current through target device R_t. By measuring the voltages at nodes V_{bias} and V_{src}, knowing the value of R_{sense} and assuming good grounding is maintained we can calculate the value of R_t, that in the ideal case is given by:

$$R_t = \frac{V_{bias} \cdot R_{sense}}{V_{src} - V_{bias}} \tag{1}$$

In practice, when assessing the resistance of R_t, reading errors will be induced by buffer amplifier offset voltages, address multiplexer (access) resistances and line resistance within the crossbar. Although the effects of such circuit imperfections have been studied extensively through simulation and experiment [9], [15], [18], the role of inaccuracies in capturing voltage values (in this case at V_{bias} and V_{src}) due to imperfect data converters is still unknown.

We can introduce error terms ε_{bias} and ε_{src} in eq. 1 to represent the V_{bias} and V_{src} misreads, respectively. These may result from non-zero data converter Differential and Integral Non-Linearity (DNL/INL), or incorrect zero/gain calibration if applicable, and will include quantisation and offset errors. Eq. 1 then becomes:

$$R_{tc} = \frac{V_{bias} + \varepsilon_{bias}}{(V_{src} + \varepsilon_{src}) - (V_{bias} + \varepsilon_{bias})} R_{sense} \tag{2}$$

where R_{tc} is the calculated target resistance value and the ADC conversion error may be positive or negative.

These error terms will be distributed within certain ranges $[\varepsilon_{bias,min}, \varepsilon_{bias,max}]$, $[\varepsilon_{src,min}, \varepsilon_{src,max}]$ and may to some extent be mutually correlated (e.g. due to cross-talk from similar groups of neighbouring signals, transmission of errors from the driver amplifier through R_{sense} etc.). In this work we take the worst case by first assuming no correlation and then studying the worst corner, when they are anti-correlated.

In the scenario where V_{bias} and V_{src} are measured concurrently by two different ADC channels and assuming conversion errors are independently distributed within $[\varepsilon_{bias,min}, \varepsilon_{bias,max}]$ and $[\varepsilon_{src,min}, \varepsilon_{src,max}]$ respectively, the R_{tc} maximum and minimum values in the absence of any errors introduced by the crossbar itself, can be expressed as:

$$R_{tc,max} = \frac{(V_{bias} + \varepsilon_{bias,max}) \cdot R_{sense}}{(V_{src} + \varepsilon_{src,min}) - (V_{bias} + \varepsilon_{bias,max})} \tag{3}$$

$$R_{tc,min} = \frac{(V_{bias} + \varepsilon_{bias,min}) \cdot R_{sense}}{(V_{src} + \varepsilon_{src,max}) - (V_{bias} + \varepsilon_{bias,min})} \tag{4}$$

for $V_{src} > 0$ and $\varepsilon_{src}, \varepsilon_{bias}$ small enough to leave the sign of numerator and denominator unaffected. $R_{tc,max}$ and $R_{tc,min}$ depend on the choice of R_{sense}, as well as on V_{src} and target resistance R_t (through V_{bias} - eq. (1)) and the conversion error distribution (through ε).

In this work, our system read accuracy was benchmarked through using the fractional read-out error metric, defined as $F = \frac{R_{tc} - R_t}{R_t}$. Fig. 3(a) plots F for $R_{tc,max}$ and $R_{tc,min}$ as a function of R_t at fixed $R_{sense} \approx \sqrt{R_{t,min} \cdot R_{t,max}}$ [19] and three different values of V_{src}. We have chosen an example

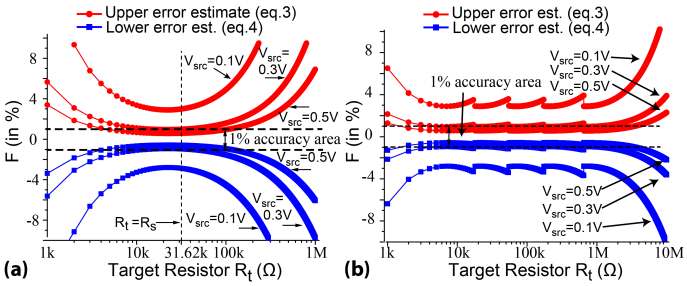

Figure 3. Fractional read-out errors caused by small ADC conversion errors vs. R_t following from eq (3), (4). (a) Fixed R_{sense} scenario ($= \sqrt{R_{t,min} \cdot R_{t,max}}$). $R_{t,min} = 1k\,\Omega$, $R_{t,max} = 1M\,\Omega$. (b) Wide R_t range ($[100\Omega, 10\,M\Omega]$) distributed over five sense resistors (see table I). Both panels: $|\varepsilon_{src}| = |\varepsilon_{bias}| = 1LSB = 0.488\,mV$. Plots shown for $V_{src} \in \{0.1, 0.3, 0.5\}\,V$.

Table I
SENSE RESISTOR BANK AND ALLOCATED R_t MEASUREMENT RANGES.

$R_{sense}(\Omega)$	10k	30k	100k	300k	1M
R_t **range** ($k\Omega$)	0 - 17.3	17.3 - 54.7	54.7 - 173	173 - 547	547 - ∞

working R_t range between $1\,k\Omega$ and $1\,M\Omega$, and V_{src} values ranging from $0.1\,V$ [20] to our instrument's $0.5\,V$ setting. ε parameters were bounded to $\pm 0.488\,mV$, corresponding to ± 1 least significant bit (LSB) in our hardware implementation in order to illustrate the effects of a single 'unit' of mis-reading at the data-converter.

We observe that at R_t values close to R_{sense} the conversion error effect is minimised, with the optimum read-out R_t shifting away from $\sqrt{R_{t,min} \cdot R_{t,max}}$. The significant increase in errors towards the low and high boundaries of the operating range can be explained by either V_{bias} (excessively low R_t case) or $V_{src} - V_{bias}$ (excessively high R_t case) becoming close to zero. In both cases, small conversion errors (ε) may become key determining factors in eq. (2) and thus cause large changes in calculated R_t. Meanwhile, lowering the read-out voltage disproportionately increases the smallest achievable error ($\approx \pm 0.57\,\%$ to $\approx \pm 0.95\,\%$ to $\approx \pm 2.85\,\%$ for $V_{src} = \{0.5, 0.3, 0.1\}\,V$ respectively). These results suggest that implementing a bank of sense resistors attuned to different R_t ranges helps mitigate the effects of conversion errors. Fig. 3(b) shows predicted conversion error-induced F as simulated for a system that allocates different R_t ranges to a bank of sense resistors as in our instrument (summarised in table I).

III. SYSTEM IMPLEMENTATION

The overall system architecture of the array control instrument presented in this work is shown in Fig. 4 where the partitioning into the array handler and the control modules is visible. The array handler is taken from [15] and hosts the array under test (AUT - max. size: 32×32 elements), the access framework used to select the target device and the biasing/measurement environment used to implement the biasing schemes detailed in section II. The control module consists of an EFM-02 FPGA development board ($45\,nm$, Spartan 6) and a data converter board (DCB). The whole

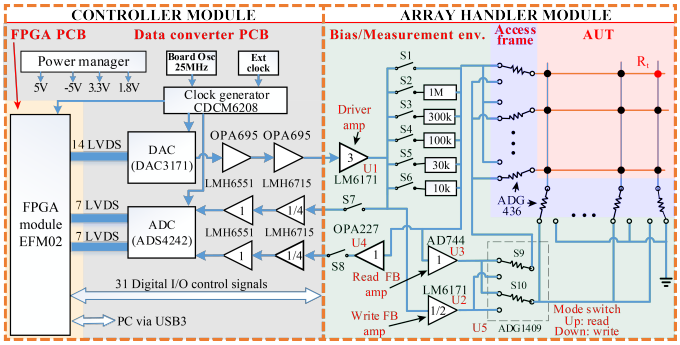

Figure 4. Simplified array control instrument diagram. The system is partitioned into a controller and an array handler module. The data converter PCB was designed in-house. The array handler is described in detail in [15]. AUT: array under test.

system is controlled through a PC-based Python interface, interacting with VHDL code running on the FPGA board.

The DCB, designed specifically for this work, is split into the analogue-to-digital (AD) and digital-to-analogue (DA) pathways. The DA pathway employs a high-speed, high-precision ($500\,MHz$, 14-bit), current-output digital-to-analogue converter (DAC) (DAC3171) operated flexibly at up to $312.5\,MHz$ (burst mode - 32k points max.). This is followed by a cascade of two, high bandwidth, ultra-high slew rate ($4.3\,MV/\mu s$, $1.4\,GHz$) interfacing amplifiers (OPA695) that convert the DAC output to voltage and boost its signal range from $\pm 2V$ to $\pm 4\,V$ respectively. The array handler bias generator amplifier was switched to a high slew rate ($3.6\,MV/\mu s$), $\pm 15\,V$ power supply amplifier (LM6171) capable of achieving the $\pm 12\,V$ bias voltage swing required by our instrument.

The AD pathway utilises a dual-channel, high-speed, high-precision ($65\,Msps$, 14-bit, 11.4-bit ENOB, 2 LSB max. INL), differential input ADC (ADS4242) operated flexibly at up to $50\,Msps$ (burst mode - 16k points max.). The array handler provides single-ended analogue signals, pre-amplified through a voltage amplifier (OPA227 - U4), whose gain was reduced to unity in this work. We thus exchanged input voltage range against noise performance with respect to the original instrument design [15] (original instrument: max. input voltage $0.5\,V$, current instrument: $4\,V$). These signals pass through a $\approx 1/4$ gain damper (LM6715), followed by a single-end to differential signal converter (LM6551). This allows a $\pm 4\,V$ input signal range to be mapped to a $2\,V_{pp}$ differential signal, suitable for the ADC. As a result, 1 ideal LSB corresponds to a $0.488\,mV$ change in raw input signal, as provided by the array handler.

Clocking control for both AD and DA pathways is provided by a low-jitter ($265\,fs$ RMS), adjustable clock generator module (CDCM6208). Clock frequencies for both the ADC and the DAC can be adjusted independently, which allows our system to flexibly trade off timing resolution for acquisition/stimulation window duration respectively and thus ensure optimal use of our limited Random Access Memory (RAM) resources inside the FPGA. Further flexibility is built into the system through software-controlled (VHDL level) down-

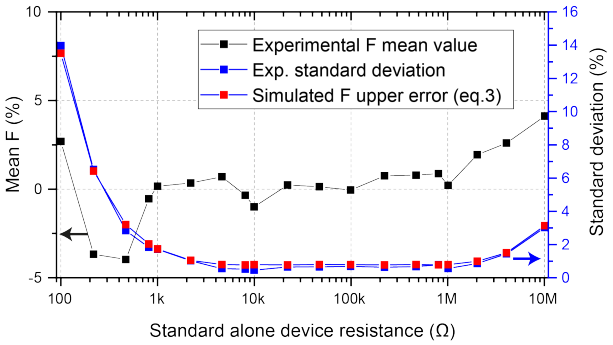

Figure 5. Discrete, linear resistor fractional read-out errors F vs. target resistance R_t, and associated read-out standard deviation σ. The average conversion error ε is estimated by fitting simulated data to measurements as approx. $1.34\,LSBs$. Each data point corresponds to 100 samples.

sampling of the data arriving from the ADC channels and/or padding of the data emitted by the DAC (multiple clock cycles per data point).

IV. Experimental results

Our upgraded array control instrument was tested in three stages: First, read-out accuracy was assessed on stand-alone linear resistors and on a reference 32×32 resistor crossbar array as in [15]. Second, sinusoidal stimulation was applied on a linear resistor and on a RRAM prototype device (both in stand-alone configuration - device fabrication described in [15]). The on-board oscilloscope continuously assessed device under test (DUT) static resistance throughout the entire stimulation cycle and the resulting data allowed the generation of I-V curves. Third, oscilloscope traces were obtained from the active and inactive WLs and BLs showing the limits of the instrument's pulsing capabilities and confirming that the write cross-talk protection feedback mechanism works as expected.

A. Read-out operation assessment

Initially, a series of discrete, linear resistors ranging from $100\,\Omega$ to $10\,M\Omega$ were used to test our system read-out performance. Fig. 5 shows average read-out errors (100 samples) and associated standard deviations (useful indicator of data spread even if underlying distribution is not necessarily Gaussian). Results are comparable to [15], although systematic errors affect our system more due to the downgrade of the gain of amplifier U4 in Fig. 4. The standard deviation plot indicates that indeed towards the edges of the operating range results become more inconsistent, as would be expected by the widening error ranges in Fig. 3(b). The amount of read-out variation indicates that in our instrument voltages are sampled with more than ± 1 LSB fluctuations (best fit - $1.34\,LSB$), which may be attributable to data converter imperfections (INL, DNL etc.) and/or the presence of noise.

Next, the performance of the system was assessed on a 32×32 reference linear resistor crossbar array. Test array configuration and measured read-out errors are shown in Fig.6. Typical crossbar parasitic-induced read-out error patterns can be observed, similar to those described in [18]. These include: a) overestimates due to non-zero access framework resistance

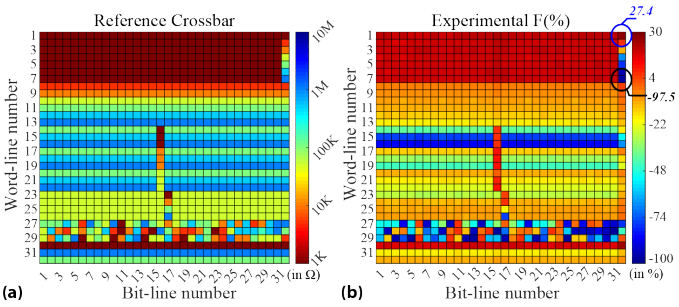

Figure 6. Measuring a linear resistor reference crossbar array. (a) Reference array configuration. (b) Fractional read-out errors. Devices read with the highest over- and under-estimates are circled in blue and black respectively.

in WLs with many low resistance cells (top 7 WLs) and b) underestimates appearing when high RS cells share a line with cells of much lower RS (WLs 13 vs 16) amongst others. This indicates that the current system operates in crossbar-limited, rather than instrument-limited regime.

B. On-board oscilloscope capability assessment

The array control instrument's on-board oscilloscope was tested by outputting a digitised, $3.5\,V$ sinusoidal stimulation signal (DA signal pathway - 32k points, $1\,s$/cycle) first to a linear, reference resistor ($2.2\,k\Omega$) and then to a prototype RRAM device. The system was operated in the 'read' configuration (Fig. 2(a)) throughout the procedure, with V_{src} and V_{bias} concurrently sampled at 16k points/s (AD pathway). For this experiment, a $1\,k\Omega$ sense resistor was specially introduced to ensure sufficient voltage transmission from V_{src} to V_{bias} because our prototype devices switch at biases in the range of $1 - 2\,V$, and operate in the $1 - 10\,k\Omega$ range. The sinusoidal input was kept at low frequency ($1\,Hz$) in order to limit the effect of parasitic capacitances on results. Target resistance R_t was calculated as per eq. (1).

Testing the reference resistor reveals that our instrument can correctly calculate static resistance throughout most of the cycle by direct division of measured applied voltage over measured current (Fig. 7(a), lower panel). At higher input stimulus frequencies parasitic capacitances have to be taken into account and specific parasitic connectivity models need to be taken into account (improvement of performance at high frequency currently under progress). An important exception, however, appears when the input signal is very close to zero (around the zero crossing). In that case we observe an amplification of resistance measurement uncertainty due to the low levels of signals involved even though the measured voltage and current values themselves are still well-defined. Fitting the corresponding I-V from Fig.7 (b) to a linear model yields an estimated resistance of $2.212\,k\Omega$. Tests on the RRAM device illustrate the non-linear nature of its I-V characteristic as well as exemplifying the effects of a single, abrupt switching event on results (Fig. 7(c,d)). The abrupt switching event occurred at the $76\,ms$ mark, under a net bias voltage of $V_{bias} \approx 1.52\,V$. Repeating the stimulation cycle confirmed the device had undergone a marked I-V behaviour change.

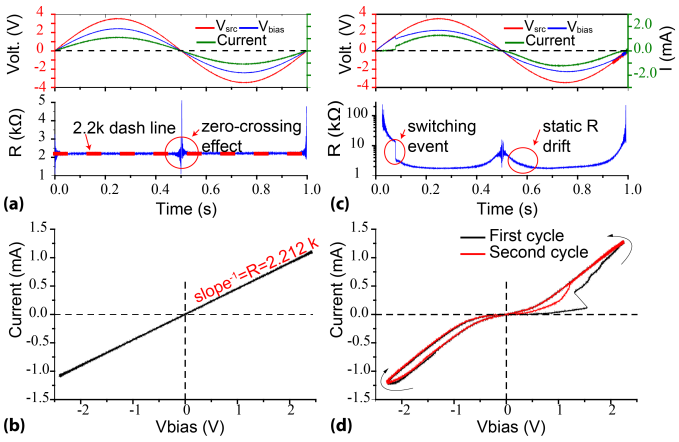

Figure 7. On-board oscilloscope operation. (a) Upper panel: traces of V_{src} and V_{bias}, as captured by on-board oscilloscope during test on reference resistor ($3.5\,V$ sine on $2.2\,k\Omega$ resistor). Lower panel: Inferred DUT static resistance at every sampled point. (b) Associated I-V curve. (c) As in (a), for prototype RRAM device. (d) Associated I-V curve (black) and follow-up cycle (red - same stimulation waveform). Effects such as zero crossing-induced measurement uncertainty amplification, measured static resistance drift due to inherent I-V nonlinearity and resistive switching are circled in panels (a) and (c). $R_{sense} = 1\,k\Omega$ for this experiment.

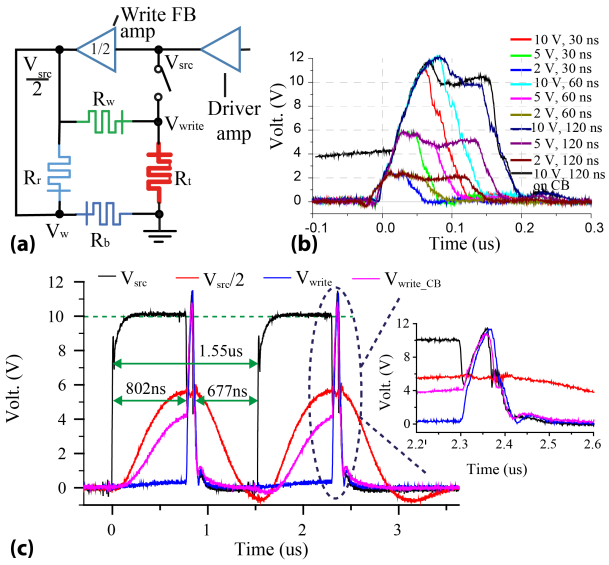

Figure 8. Write operation performance. (a) 'Write' configuration (Fig. 2(b)) with strobing switch explicitly shown. (b) Examples of write pulses at different amplitudes and durations under standalone and crossbar loading. Nominal pulse spec values shown in figure. $10\,V$, $30\,ns$ pulse gives rise to $\approx$ $(10\,V, 70\,ns)$ pulse (FDHM). (c) Application of two, consecutive $10\,V, 30\,ns$ (nominal) pulses indicating bottleneck of inactive line feedback settling. Loading in all cases is either $10\,k\Omega$ linear resistor (standalone case) or array from Fig. 6 with $R_t = 10\,k\Omega$ (device at (WL,BL) location (9,1) - crossbar case). All waveforms captured and exported by $3\,GHz$ oscilloscope.

Increasing the AD pathway sampling rate allows monitoring of DUT resistive state evolution with greater time resolution at the expense of acquisition window duration due to the burst-mode operation of the on-board oscilloscope. Notably, the current instrument's flexibility to trade-off sampling rate against acquisition window was not present in the previous, microcontroller-based implementation where the acquisition rate was limited to $200\,ksps$ (see table II and LPC1768 datasheet).Moreover, employing higher input stimulus frequencies will cause reactive loading effects to become more pronounced and thus offers a way of assessing DUT complex impedance. Benchmarking of this capability lies outside the scope of this paper.

C. Write operation assessment

In a practical implementation, feedback provided during the write operation must be applied on the array throughout the entire duration of each programming pulse. For this reason, when implementing the conceptual biasing scheme from Fig. 2, a strobing switch is included (Fig. 8(a) - S1 in Fig. 4). This allows the inactive WLs and BLs to precharge to $V_{src}/2$, following which the strobing switch is activated and V_{src} is flashed to the active WL. Because the active WL also charges towards $V_{src}/2$ by leakage currents through the crossbar whilst S1 is open, producing a pulse at voltage V_{src} is facilitated. The procedures and performance of our system's write operation are illustrated in Fig. 8, where we show oscilloscope traces for signals $V_{src}, V_{src}/2$ and V_{write} and characteristic pulse shapes at $< 200\,ns$ duration under both standalone and crossbar loading conditions. These signals were probed at the AUT pins and thus include the effects of the switches of the access framework (Fig. 4). The significant rise-time difference between V_{src} and $V_{src}/2$ occurs due to different capacitive loading. It takes a minimum of $1.55\,\mu s$ for the system to precharge the inactive lines, apply a stimulus pulse and return the array to GND, however multi-pulse burst-mode operation is also possible (pre-charge once, apply multiple pulses by repetitive strobing). The timing resolution of the waveform is controlled to a minimum of $3.2\,ns$/data point. The relatively large overshoots observed in Fig. 8(c) are due to impedance mismatch between load (variable in RRAM) and driver amplifier output. Key pulse stimulation performance characteristics and comparisons to other relevant work are summarised in table II.

V. RRAM Device Testing Applications

A. RRAM device switching characterisation

The presented system was utilised to study the switching behaviour of the prototype RRAM devices from [15] under ns pulse stimulation. Fig. 9 illustrates test results obtained from standalone devices subjected to the 'biasing parameter optimiser' testing algorithm [22]. The optimiser attempts to repeatedly induce switching in a DUT by administering multiple, fixed-duration/incrementing-amplitude voltage pulse ramps of alternating polarities (panel (a)) and is a generalisation of the well-established incremental step pulse programming routine (ISPP) [23]. Switching is considered achieved when DUT resistance hits pre-defined minimum and maximum target levels. The amplitude of the last stimulus pulse is defined as the 'switching voltage', though resistive state assessments following each write pulse keep a record of the effects of every individual pulse on DUT resistive state (panel (b)). This allows us to also define a 'switching threshold' level, which corresponds to the pulse amplitude when DUT resistive state

Table II
KEY PERFORMANCE METRICS FOR ON-BOARD OSCILLOSCOPE READ-OUT (ABOVE DOUBLE LINE) AND PULSE STIMULATION (BELOW DOUBLE LINE).

Pulse properties	**Proposed system min/max**	**Ref. [15] system** ** **min/max**	**Keithley 4225PMU**† **min/max**	**Unit**
Sampling rate	-/65	-/0.2	-/200	Msps
Acquisition window*	492 / $> 1E^{6}$‡	indef.▽	N/A	μs
Output voltage	$-11/11$	$-11/11$	$-10/10$	V
Pulse period	$1.55E^{-6}/8.45$	$8E^{-6}/4.29E^{3}$	$20E^{-9}/1$	s
Pulse width	$30E^{-9}/8.39$	$4E^{-6}/2.15E^{3}$	$10E^{-9}/\approx 1$	s
Pulse time gap	$677E^{-6}/327$	-/-	-/-	ms
Timing resolution	3.2	1000	10	ns/pt

* 'min' defined as max. acquisition window length at max. sampling rate.
** From direct measurements on system.
† From Keithley 4225PMU datasheet [21]. 10V range, source-only timing specification used (maximum speed and accuracy case).
‡ Work is under way to implement a 'continuous acquisition' mode which is expected to allow 'indefinite acquisition windows' at a max. rate limited by the PC speed and/or the USB3.0 PC-FPGA link. This will be a software-only upgrade.
▽ Indefinite: Limited at the PC-end.

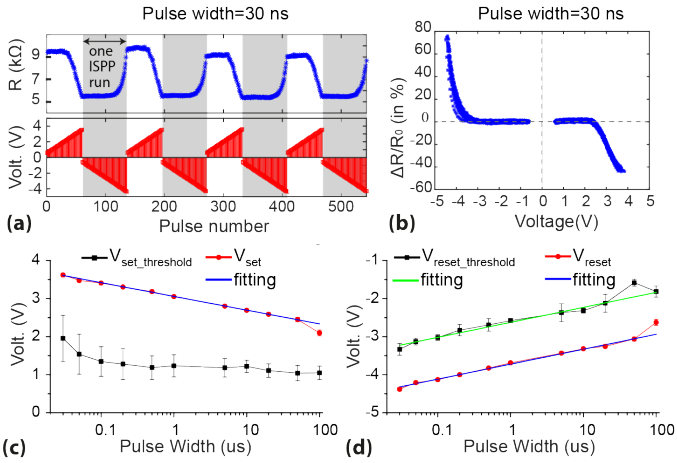

Figure 9. Standalone prototype RRAM device switching behaviour vs. stimulus pulse parameters. (a) Resistive state change (top trace) in response to successive ISPP sequences of alternating polarities (bottom trace) for pulse duration fixed at 30 ns. (b) Corresponding normalised changes in DUT resistive state caused by each individual stimulus pulse as a function of pulse amplitude (20 ISPP runs in each polarity shown together). (c) Switching and threshold voltages and standard error bars for SET transitions (switching towards R_{min}) as a function of pulse duration. Pulse widths range from 30 ns to 100 μs. (d) Corresponding plot for RESET transitions. Voltage step employed in all ISPP runs equals 50 mV. Switching target levels were set at $R_{min} = 5\,k\Omega$ and $R_{max} = 10\,k\Omega$. Each data point in (c) and (d) represents data from 20 ISPP runs. Normalised resistive state change calculated as $\frac{|R_c - R_0|}{R_0}$ where R_c is current and R_0 is initial resistive state.

has diverged from its value at the beginning of the test by more than 2% ($\frac{|R_c - R_0|}{R_0} > 2\%$ - R_c is current and R_0 is initial resistive state). By repeating this test for different stimulus pulse durations in both polarities, the influence of pulse duration on switching and threshold voltages can be investigated (panels (c) and (d)). All measurements are performed on a single DUT.

Results show that our sample DUT switches in multi-level bipolar mode[1] with an asymmetric dependence of resistive state changes vs. voltage, positive voltages being able to induce comparable resistive switching at lower magnitudes than negative voltages. Furthermore, a clear pulse voltage-duration trade-off is observed, also known as the voltage-time dilemma [24], for both polarities with exponential fits reasonably describing positive polarity switching voltage and negative polarity switching and threshold voltages (table III). Fits were carried out using the MATLAB bisquare linear fit method. Notably, adjusted $R^2 > 0.975$ in all cases and the maximum 95% confidence interval is $\pm 22\,mV/dec$. Conversely, the positive polarity threshold voltage behaviour seems to be characterised by faster-than-exponential decay of $V_{set\_threshold}$ with pulse width, further exhibiting progressively larger uncertainties as pulse durations decrease. The reasons behind this require further study.

B. RRAM crossbar manipulation with cross-talk suppression

In order to test the capabilities of the system to mitigate write cross-talk effects in RRAM crossbars in-operando, the write procedure was further assessed in a 32 × 32 crossbar

[1]Bipolar: opposite polarities induce switching in opposite resistance change direction. Multi-level: Able to take many RS values lying between the operational RS floor and ceiling regardless of ON/OFF ratio.

Table III
VOLTAGE-TIME TRADE-OFF TEST RESULTS

	Slope 95% confidence	**Units**	**Adjusted R^2**
V_{set}	-157 ± 9.5	mV/dec	0.9938
V_{reset}	171 ± 14.0	mV/dec	0.9888
$V_{reset\_threshold}$	171 ± 21.7	mV/dec	0.9753

(same device technology as in previous section - see [15]). For this test, three devices were chosen with (WL,BL) locations selected as shown in Fig.10(a). The objective was to demonstrate successful RS manipulation of 'target' cell M1 whilst leaving the RS of the two 'cross-talk' cells M2 and M3 (one each on the bit- and word-line complements of M1 respectively) undisturbed.

All three test devices were first tested with the 'biasing parameter optimiser' routine to confirm that they are functional (capable of switching). Indicative raw results from cell M3 are shown in Fig. 10(b) along with the time evolution of the device's switching voltages over the duration of this preliminary test phase (Fig. 10(c)). Despite a slight drift in the device's operating RS range we notice that the switching voltages remain remarkably stable. The SET and RESET switching voltages for all test devices as summarised in table IV. Notably, the SET and RESET voltage polarity of device M3 was adverse to that of the other two devices.

In the main part of the experiment, the RS of the 'cross-talk' cells (M2, M3) was first assessed 20 times through low-voltage, non-invasive read operations as described in previous sections. Then, $-1.9\,V, 100\,\mu s$ SET pulses and $2\,V$ RESET

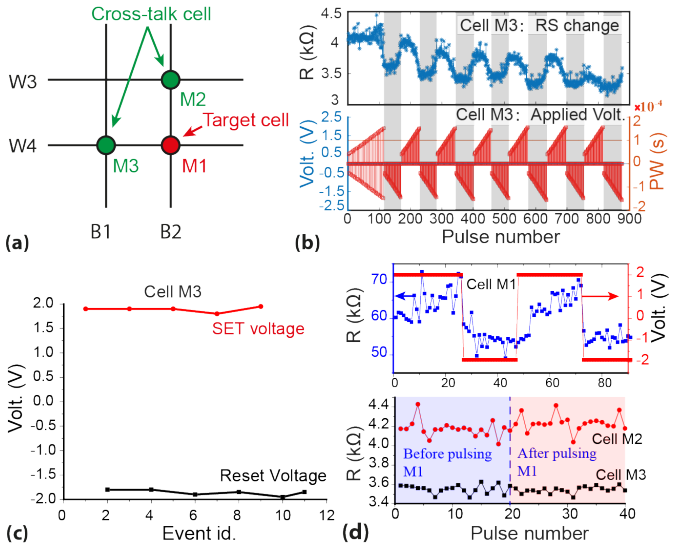

Figure 10. Prototype RRAM array crossbar operation under pulse stimulation. (a) Three cells ((WL,BL) locations: (4,1), (4,2), (3,2)) were specifically chosen in order to demonstrate the cross-talk-robust write operation. (b) Resistive state change of M3 and its corresponding applied pulse stimulus. (c) Extracted SET and RESET voltage changes along with the switching event. (d) upper panel: Resistance state change on device M1 under a pulse sequence with SET voltage of $-1.9\,V$ and RESET voltage of $2\,V$. lower panel: resistance assessments before and after pulse sequence applied on device M1. All the pulse duration were fixed at $100\,\mu s$.

Table IV
SWITCHING PARAMETERS FOR CELLS UTILISED THROUGHOUT THE CROSS-TALK SUPPRESSION TEST PROCEDURE

Cell	V_{SET} **range (V)**	V_{RESET} **range (V)**
M1	[-2, -1.65]	[1.8, 2.1]
M2	[-1.25, -1.2]	[1.4, 1.55]
M3	[1.8, 1.95]	[-1.95, -1.8]

pulses were applied on device M1 and the resulting resistive state changes were recorded and are shown in Fig.10(d), upper panel. Gradual, but significant RS changes are observed in reaction to the cumulative effects of the pulsed stimulation. Notably, the RS of cell M1 was cycled fully twice and left in a different state than it originally had. This was done in order to try and destabilise the 'cross-talk' cells as much as possible throughout this stage of the test. Finally, the RS of cells M2 and M3 was once again assessed twenty-fold. The statistically insignificant changes in the RS of M2 and M3 indicate towards the effectiveness of the cross-talk protection mechanism adopted in the system.

VI. DISCUSSION AND CONCLUSIONS

A. System performance

In sections II and IV we have noted that the best read-out accuracy can be obtained when the target DUT resistance is similar to the sense resistor used. One might be tempted to think that the high read-out accuracy range of the instrument may be significantly extended by the addition of very high ($\geq 10\,M\Omega$) and very low ($\leq 100\,\Omega$) sense resistor options. Whilst some improvement may still be possible, we can expect that at the very low resistance corner, DUT resistive state will gradually become comparable to the parasitic resistance in the access framework, which may introduce significant errors. These will be exacerbated in crossbar configurations, where the access switch may be required to channel current for an entire WL of very low resistive state DUTs. On the other hand, at the very high resistance corner, we can expect leakages through solid state switches in the access framework and read-out amplifier (U4 in Fig. 4) input bias currents to reach disruptive levels. Whilst some of these issues can be mitigated by employing relays (low leakage) or constraining our choice of read-out amplifiers to low-leakage MOSFET-based ones, some performance metric (e.g. speed) would likely have to be sacrificed in exchange. Another factor limiting the read-out precision by adopting the read-out circuits in Fig.2(a) is inaccuracy of R_{sense}. We note that the R_t calculation from Eq.1 is linearly dependent on the R_{sense}, which means 1% R_{sense} deviation would cause 1% read-out accuracy degradation. For this reason, high accuracy components should be used otherwise large systematic error would be induced. By simply adopting 0.1% tolerance components, this issue drops in significance to the extent where other issues discussed throughout this paper become much more important.

B. Implementation strategy

Transitioning to an FPGA-based solution was not the only viable implementation option for massively upgrading the timing specifications of the previous system version [15]. An alternative approach would be to outsource the speed element to other PCB components such as e.g. micro-timers and sequencers. Whilst such an approach was implemented, tested and showed promising results, the FPGA-based approach was chosen and pursued for this work on the basis that additional beneficial features could be obtained with comparable design effort:

- The FPGA board could overcome the $200\,ksps$ read-out limitation of the microcontroller board and supported USB3.0 communication with the PC at up to $300\,MBps$ as opposed to USB2.0 for the microcontroller board (operated through a serial link at a maximum of $921\,k$ baud rate). Both the FPGA and the microcontroller versions of the instrument require both PC-side and microcontroller/FPGA-side code. The communication bottleneck between PC and microcontroller had previously forced us to allocate some high-level functionality to the microcontroller side (e.g the optimiser module from [22]), which can now be entirely shifted to a single, unified, PC-based interface that doesn't have to be designed around the limited resources of the microcontroller board.
- The FPGA board featured a much large number of input/output (I/O) pins (191 vs. 25 for the previous version, which after a series of upgrades has already become pad-limited).
- Adding micro-timers and other such circuitry would unnecessarily complicate the PCB design if such functionality can simply be provided directly from the FPGA.

C. Conclusions and future work

In conclusion, we have presented a custom made system that builds upon our previous efforts by adding nanoscale pulsing and on-board oscilloscope capabilities to an instrument designed to handle both standalone devices and crossbar arrays for read and write purposes. The on-board oscilloscope allows the extraction of DUT transient behaviour and I-V data whilst the ns pulsing capabilities mark an above two order of magnitude improvement in write pulse timing resolution. These improvements offer enhanced operational flexibility covering an increased number of memory technologies. Moreover, we have studied the extent to which data conversion errors may influence the results of the accuracy-critical task of reading a DUT resistive state. We conclude that even in the absence of crossbar effects, small conversion errors may induce increasingly large misreads as read-out voltage drops. Thus ADC selection and calibration become increasingly critical design considerations, an effect that can be mitigated by attempting to evenly distribute the voltage within the DUT-R_{sense} potential divider. Finally, our array control instrument was successfully used to obtain the switching characteristics of a prototype RRAM technology under pulsed stimulation as a function of pulse amplitude and duration. Data spanning a pulse duration interval between sub-$100\,ns$ and $100\ \mu s$ was recoded using a cheap, portable, user-friendly RRAM testing platform.

Based on the learnings in this work, some future system improvements are suggested (currently under development) such as: a) Splitting the AD pathway between a fast, coarse branch for the on-board oscilloscope and a slow, high-precision branch for the accuracy-critical read operation. b) Transitioning the array handler to a trans-resistance amplifier-based read-out scheme [18] so that precise, direct control over the bias voltage across the DUT is maintained at all times, including during on-board oscilloscope operation. With these upgrades we intend to further enhance read-out accuracy.

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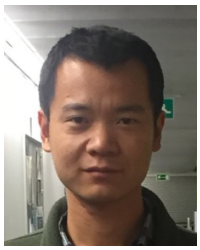

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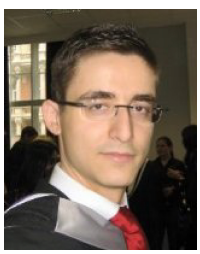

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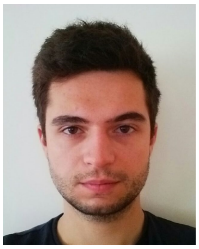

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