Energy-Efficient Hardware Implementation of LR-aided K-Best MIMO Decoder for 5G Networks

Basel Halak, Mohammed El-Hajjar, Ogeen H. Toma and Zhuofan Cheng
ECS, University of Southampton, Southampton SO17 1BJ, UK
Email:{bh9,meh}@ecs.soton.ac.uk

Abstract: Energy efficiency is a primary design goal for future green wireless communication technologies. Multiple-input multiple-output (MIMO) schemes have been proposed in literature to improve the throughput of communication systems, they are expected to play a prominent role in the upcoming 5th generation (5G) standard. This paper presents a novel high efficiency MIMO decoder based on the K-Best algorithm with lattice reduction. We have designed a novel hardware architecture for this decoder, which was implemented using 32nm standard CMOS technology. Our results show that the proposed decoder can achieve on average a four-fold reduction in the power costs compared to recently published designs for 5G networks. The throughput of the design is 506 Mbits/sec, which is comparable to existing designs.

Keywords: Sphere Decoding (SD), Lattice Reduction, K-Best Algorithm, MIMO, Green Communication, Low Power, VLSI, Hardware Design.