EPITAXIAL INTERDIGITATED BACK CONTACT (IBC) SOLAR CELL TEST PLATFORM FOR NOVEL LIGHT TRAPPING SCHEMES

A.Nawabjan[1,4]*, T.Rahman[1], A.Tarazona[2], D.M.Bagnall[3], S.A.Boden[1]

[1] Electronics and Computer Science, University of Southampton, Southampton, SO17 1BJ, UK
[2] EcherKon Technologies Ltd., 20 Springfield Road, Crawley, West Sussex, RH11 8AD, UK
[3] School of Photovoltaic and Renewable Energy Engineering, The University of New South Wales, Sydney, NSW 2052, Australia
[4] Electronics and computer Engineering, Universiti Teknologi Malaysia, 81310 Skudai, Johor, Malaysia

ABSTRACT: An Interdigitated Back Contact (IBC) solar cell is being developed for evaluation of emerging light trapping schemes of silicon nanowire arrays on pyramidal textured surfaces. The front surface of the baseline IBC cell design was optimized with a thin film coating considering both antireflection and passivation to reduce surface recombination. Addition of a front surface field (FSF) was shown to improve the surface passivation of the cell. PC2D simulations of the baseline device predict an efficiency of 17.4%. Silicon nanowire arrays and hybrid structures of silicon nanowires on pyramids were successfully fabricated. Hemispherical reflectance measurements show that a weighted average reflectance of just 1.89% was achieved. With adequate surface passivation, these highly-effective antireflective structures could result in a power conversion efficiency increase compared to traditional light trapping methods when incorporated into the IBC cell.

Keywords: IBC, HWCVD, Si Nanowires

1 INTRODUCTION

Many methods have been explored in the search for ways of increasing efficiency of solar cells, to thus reduce the cost-per-watt of PV. This has led to research into novel sub-wavelength antireflection (AR) and light trapping (LT) schemes such as plasmonic metal nanoparticle arrays [1], bio-mimetic ‘moth-eye’ structures [2], Mie resonators arrays [3], silicon nanowire (SiNW) arrays [4], and hybrid surfaces of SiNWs on micron-scale pyramids [5]. A solar cell test platform is needed to facilitate the comparison of these new AR and LT methods with more traditional thin film and micron-scale texturing approaches. Since the front surface of the cell is free of any contacts, the interdigitated back contact (IBC) monocrystalline silicon solar cell design is well suited to fulfil this need [6].

The IBC design has a number of advantages over conventional solar cell design. Complete elimination of front metal contacts enable the individual optimization of optical and electrical properties. Absence of front metal contacts also leads to higher short circuits due to absence of shadowing loss, and also lower resistive losses. The cell design offers easier interconnection and increased packing density within a module [7]. Furthermore, the approach improves aesthetics, increasing the likelihood of large scale adoption in building integrated PV. The concept has been adopted commercially for large-area cells by, for example, Sunpower, who have demonstrated power conversion efficiencies of over 24% [8].

The first part of this paper describes the steps towards the development of a planar Hot Wire Chemical Vapour Deposition (HWCVD) based IBC cell for comparing novel AR and LT schemes with traditional thin film and micron-scale texturing. In the IBC solar cell design, most of the photo generation takes place near to the front of the cell. These light generated carriers can be easily lost by recombining at the front surface and thus surface passivation plays a crucial role in efficient devices.

The second part of this paper describes the enhancements to the front surface of the basic design. These include the addition of a thin SiO_2 passivation layer between the thin film AR coating and the incorporation of a front surface field via the formation of an n^+ layer using a $POCl_3$ diffusion step.

In the third part of this paper, PC1D and PC2D simulations are used to quantify the improvements to the design of the front surface and to predict the performance of the baseline IBC solar cell. The final part of the paper describes the fabrication and optical characterisation of SiNW-pyramid hybrid AR structures on silicon.

2 IBC CELL DESIGN

Figure 1 shows the schematic of the IBC cell proposed in this work and Figure 2 shows the simplified outline of the fabrication process.

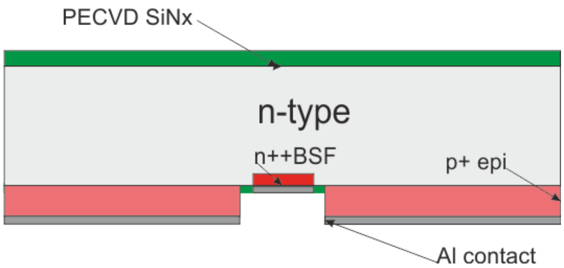

Figure 1: Schematic of the simple IBC cell designs for this study.

The process begins with cleaning of a silicon wafer (n-type, cz grown, <100>, 1-10 Ω.cm). A photolithography and dry etch stage is then used to define the n-type contact pattern on the rear of the cell, through which the n^+ back surface field (BSF) is formed by $POCl_3$ diffusion at $900^{O}C$. This is followed by deposition of an 85 nm thick silicon nitride AR layer by Plasma Enhanced CVD (PECVD). A second photolithography and dry etch stage is then used to define the p-type contacts. The epitaxial p^+ contacts are then fabricated by HWCVD and lift-off. Finally, a third photolithography process followed by aluminium evaporation and lift-off forms the ohmic contacts to the n and p regions. The wafer is then diced to form 1 cm^2 individual devices. The process listing includes the option of texturing the surface with a KOH etch after the initial wafer cleaning stage, however the baseline device features a planar surface.

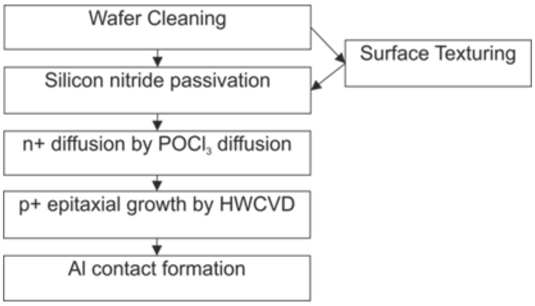

Figure 2: Simplified outline of the IBC cell fabrication process.

3 FRONT SURFACE OPTIMIZATION

The design presented above uses an 85nm SiN_X layer grown by PECVD for the front surface coating. This thickness was optimized by simulation, maximizing absorption in an underlying silicon substrate, using OPAL2, an implementation of the transfer matrix method [9]. Refractive index and extinction coefficient data (n and k) for the SiN_X material were obtained by ellipsometry and used as input for the simulations. The design of the front surface treatment should also consider ways to reduce surface recombination, a major source of loss in IBC cells. Hence the following two improvements to the design were developed.

3.1 Thermal oxide passivation

Thermally grown oxide is known as an effective passivation layer for silicon (Si) that saturates dangling bonds at the surface and therefore reduces surface recombination. In this study, the addition of a 10 nm thermal SiO_2 layer beneath the SiN_x layer was found to significantly improve the carrier lifetime of a sample, measured using the quasi steady state method (Sinton WCT-120). A lifetime of 182.4 µs was measured for a silicon sample with an oxide and nitride surface coating compared to 86.3 µs for the oxide coating alone (Table I). A single nitride layer was shown to provide some passivation but only increased the lifetime to 60 µs compared to bare silicon at 6.5 µs. The improvement in lifetime when oxide and nitride layers are combined in a double layer is thought to be due to the enabling of two mechanisms that reduce surface recombination. Firstly, chemical passivation is provided by the thermal oxide layer that saturates dangling bonds at the surface. Secondly, fixed positive charges in the nitride as a result of non-stoichiometric growth repel minority carriers (holes) in the n-type material away from the surface. The hole concentration at the front surface is therefore lower, reducing recombination rate.

Furthermore, addition of the thin SiO_2 layer was found not to have a significant effect on the optical properties of the surface and the AR effect of the coating remained (see Figure 3)

This double layer thin film coating exhibits a weighted average reflectance R_w, of 5% and a carrier lifetime of 182.4 µs when deposited on an n-type Si test wafer. This compares to an R_w of 33.5% and carrier lifetime of 6.5 µs on the untreated wafer.

Table I: Measured carrier lifetimes of thin film materials deposited on silicon considered for passivation of IBC solar cell front surface.

Material	Lifetime (µs)
Bare silicon	6.5
30 nm PECVD SiN_X	60
10 nm SiO_2	86.3
10 nm SiO_2 beneath a 85 nm PECVD SiN_X	182.4

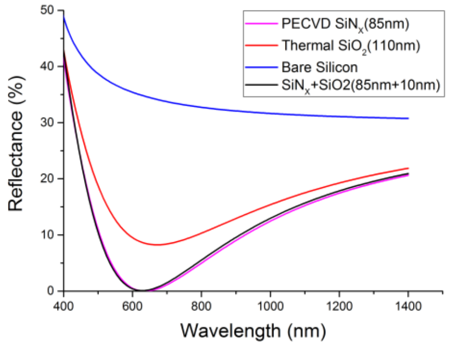

Figure 3: Simulated reflectance spectra for different thin film coatings on silicon (including bare silicon).

3.2 Front Surface Field (FSF)

In addition to passivation provided by the thin film coating, formation of a Front Surface Field (FSF) is a well-known method to further reduce front surface recombination by repelling minority carriers from the surface.

The process for forming a FSF using $POCl_3$ diffusion was developed for incorporation into the full cell fabrication flow illustrated in Figure 2. A target value for sheet resistance of 148 ohm/sq was chosen from an optimization study on FSF for IBC cells reported in the literature [10]. The FSF is formed by $POCl_3$ diffusion carried out at 750°C for 20 mins, followed by an anneal at 1000°C for 8 mins. The annealing process is combined with the thermal oxidation step to produce a FSF with a passivating 10 nm thick thermal oxide. For electrical testing of the FSF, the thermal oxide was the stripped and then a four point probe measurement was carried out. The resulting sheet resistance was 147 ohm/sq, which is close to the target value of 148 ohm/sq [10]. The resulting measured carrier lifetime of the sample following this process was 839 µs at injection level of 4×10^{15} cm^{-3} which is far above the lifetime of the best sample from the thin film passivation study.

4 PC2D SIMULATION

Fabrication of the optimized design for the baseline device presented above is currently underway. However, in the meantime, simulations can be used to provide a prediction of the likely performance of the cell. The widely-used PC1D solar cell simulation program is limited to modelling cells in one dimension. Analysis of IBC cell designs involves effects in two dimensions and as such cannot by modelled using PC1D. Basore *et al.* developed PC2D, a circular reference solar cell device simulator in spreadsheet form that enables simulation of IBC and other complex cell design [11]. PC2D was employed to simulate the IBC cell in this work, with input from experimental results, parameters from literature, and values from PC1D simulations. The input parameters used for the PC2D simulation are listed in Table II .

Table II: Simulation parameters for PC2D simulation.

DEVICE PARAMETERS	VALUES
[a]Device area	1 cm^2
[a]Base doping	$5\times10^{15}cm^{-3}$
[a]Effective lifetime	375 µs
[a]Base Thickness	275 µm
[a]AR layer	85 nm SiN_x + 10 nm SiO_2 DLAR
[b]J_0 at metal contacts	1000 fA/cm^2
[a]J_0 at passivated surface	10 fA/cm^2
[c]J_0 at passivated FSF	40 fA/cm^2
[a]J_0 at p^+ region	114 fA/cm^2
[a]J_0 at n^{++} region	260 fA/cm^2

[a] Measured value
[b] Taken from literature
[c] From PC1D simulation using measured values

The simulated I-V curve for the IBC cell design with the front surface improvements described in this study is presented in Figure 4, predicting a power conversion efficiency of 17.4%.

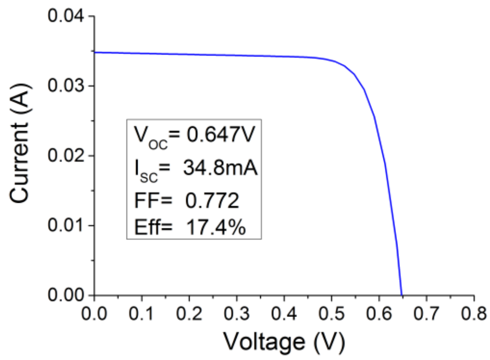

Figure 4: I-V curve of IBC cell simulated using PC2D.

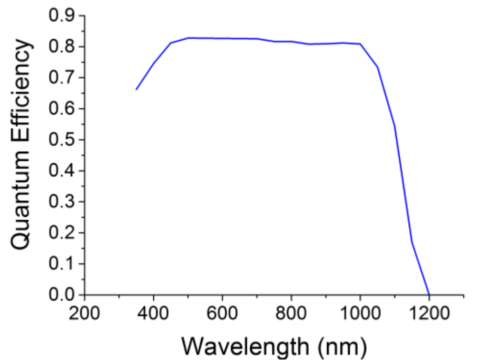

Figure 5: EQE of IBC cell simulated in PC2D.

The simulated EQE spectrum of the optimized cell design (Figure 5) shows values above 80% over the spectral range 450nm-1000nm. Good performance of the device in the blue part of the spectrum indicates that front surface recombination has been effectively suppressed with the improvements to the design presented in this work.

5 SiNW ANTIREFLECTIVE STRUCTURES

In parallel with the device development, three different AR schemes based on texturing of silicon have been developed in this work. First, a process for KOH etching to form arrays of micron scale pyramids was developed. This is a widely-used, conventional approach for AR in silicon solar cells. Secondly, a process for fabricating SiNWs by means of a Metal Assisted Chemical Etching (MACE) method was developed. Finally, these two surface treatments were combined to form hybrid structures of pyramids and nanowires.

5.1 Fabrication

The optimization of the process for fabricating random pyramid arrays, based on a recipe by King et al. [12], is described elsewhere [13]. After cleaning, c-Si wafers (n-type, <100>, 1-10 Ωcm) were etched in a 1.5% KOH, 3.8% IPA solution at 70°C for 30 minutes. The wafers were rinsed, dried and the inspected by scanning electron microscopy (SEM) to confirm successful fabrication of a dense array of pyramids (Figure 6).

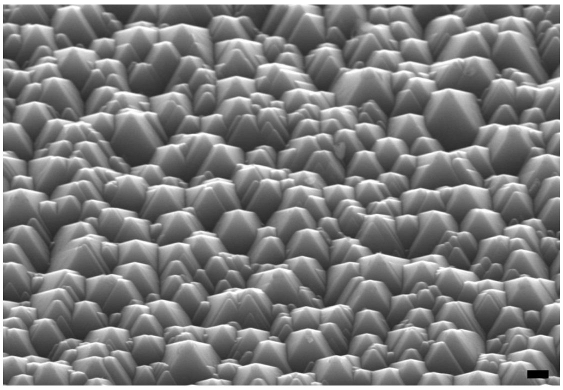

Figure 6: SEM images of etched random pyramids by KOH etching (scale bar is 1µm).

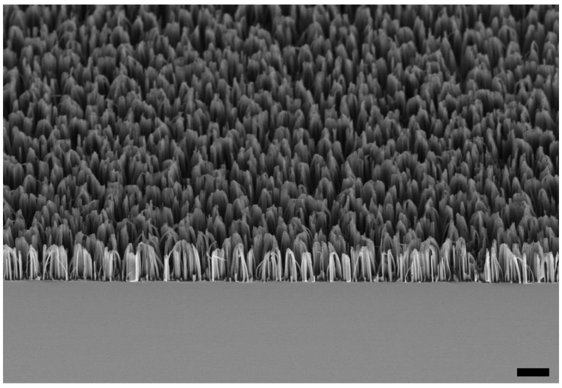

Figure 7: SEM image of SiNWs formed from MACE process (scale bar is 1µm).

The MACE technique for SiNWs was taken from previous work [5]. The SiNW etching process starts with cleaning the sample in piranha solution (H_2SO_4: H_2O_2) in the ratio of 3:1. The sample is then rinsed in DI water to remove any piranha solution that might be on the sample. The sample is then dipped in 5% HF to remove any native oxide on the sample. Then the sample is placed in MACE etching solution which consists of mixture of diluted silver nitrate ($AgNO_3$, 0.06M) solution and HF (3M) solution in a 1:1 ratio. The sample is etched for 2.5

minutes resulting in SiNWs with lengths of ~1.3µm, and diameters of between 60 nm and 100 nm (Figure 7).

Finally the two methods were combined to fabricate hybrid structures of the nanowires on pyramids as shown in Figure 8.

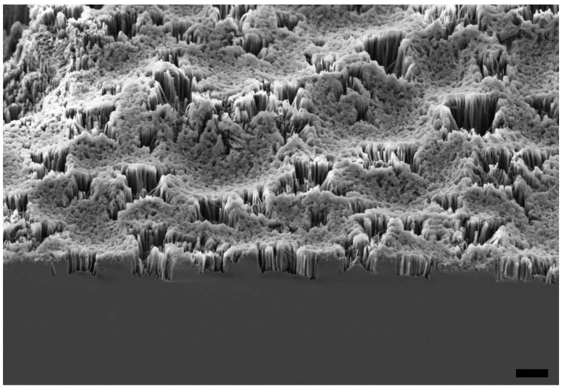

Figure 8: SEM image of hybrid SiNWs on pyramids (scale bar is 1µm).

The fabricated structures were then characterized using an integrating sphere hemispherical reflectance measurement system (Bentham Instruments). It can be clearly seen that the hybrid surface possesses AR properties that are far superior to the pyramids or SiNWs alone. The average reflectance (R_w), weighted to the AM1.5 spectrum, of the hybrid structure is just 1.89%, which is significantly better than the best pyramid sample (R_w =13.54%), the best SiNW sample (R_w =6.1%) and bulk silicon (R_w =33.5%) measured in this study.

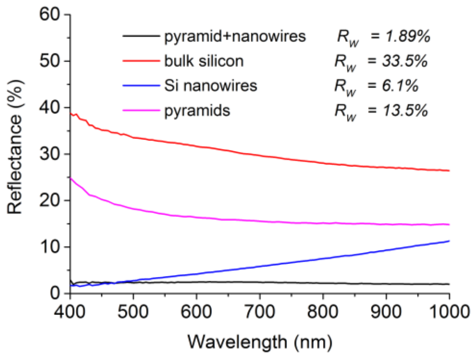

Figure 9: Reflectance comparison of different light trapping scheme, bulk silicon (red line) included as comparison.

With the optical enhancements conferred by a SiNW-pyramid hybrid scheme now confirmed, the challenge is to develop a suitable thin film deposition technique to passivate the resulting textured surface and therefore limit surface recombination. Recent studies reported in the literature indicate that Al_2O_3 can be effective for this purpose and that efficiencies >22% are possible [14].

6 CONCLUSION

A HWCVD-based epitaxial IBC solar cell for use as a test platform for novel antireflection and light trapping schemes is being developed. The thin film AR coating for the baseline device was optimized for both front surface reflection reduction and front surface recombination reduction, leading to a coating design consisting of 85 nm of silicon nitride on top of 10 nm of silicon dioxide layer. An experimental process for formation of a FSF using a $POCl_3$ diffusion was developed which incorporated a process to grow a thermal oxide. The carrier lifetime of the wafer with FSF and thermal oxide was measured to be 839 µs which represents a significant improvement on the untreated wafer which exhibited a lifetime of just 6.5 µs. With full device fabrication currently underway, PC2D simulations of the baseline device predict an efficiency of 17.4 %. Broadband antireflective hybrid surfaces of SiNWs grown on pyramidal-textured silicon have been successfully fabricated, using a scalable, maskless wet etch method, with a weighted average reflectance as low as 1.89%. Incorporation of the SiNW surfaces into the IBC cell design, with adequate passivation, will allow the comparison of these emerging AR schemes with traditional thin films and pyramids and could lead to improvements in power conversion efficiency.

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