Transport properties in silicon nanowire transistors with atomically flat interfaces

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Abstract

We have fabricated ultra-narrow (sub-10nm) short channel (100nm) silicon (Si) nanowire transistors with atomically flat interfaces based on Si-on-Insulator (SOI) substrates. The raised source and drain electrodes were patterned together with the gate electrode. The smaller threshold voltage in the narrower nanowire suggests self-limiting oxidation during the gate oxide formation.

(Keywords: narrow channel effect, silicon nanowire, SOI, TMAH, self-limiting oxidation)

Introduction

Due to the stronger immunities against short channel effects compared with FinFETs [1], Si nanowire transistors have attracted significant interests for various applications [2-5] in nanoelectronics beyond conventional Complementary Metal Oxide Semiconductor Field Effect Transistors (CMOSFETs). Si Nanowire FETs are promising for sensors [2], single electron devices [3], and quantum technologies [4]. However, fabrication of highly uniform sub-10nm Si nanowires is still a big challenge even with the state-of-the-art large-scale manufacturing technologies.

In order to avoid line-edge roughness, we used tetramethylammonium hydroxide (TMAH) etching [5] to define Si nanowires with the atomically flat interfaces. The raised source and drain method is implemented to pattern source/drain electrodes and gate electrode at the same time.

Device Fabrication

The device design and structure are shown in Fig. 1. We used SOI wafers with the standard (100) SOI layer on the 145nm-thick buried-oxide (BOX). The SOI layer was shrunk down to 24nm before making the nanowire. The 21nm-thick SiO_2 layer was formed by oxidation for the hard-mask to pattern Si nanowires. The initial patterning was made by electron-beam lithography with a Hydrogen-Silsesquioxane (HSQ) layer as a resist. Then, dry etching was implemented to etch the SiO_2 layer down to 3.6nm. The remaining SiO_2 layer was removed by hydro-fluoric (HF) etching. The combination with dry etching and wet etching can prevent the damage of the Si layer caused by dry etching. Subsequent TMAH etching was carried out to form triangle or trapezoid nanowires. The planar view of the nanowire was taken by Scanning Electron Microscope (SEM, Fig. 2). We oxidized the surface of Si nanowire to form a gate oxide layer. The nominal widths of the Si nanowires after oxidation were 1nm, 21nm and 71nm respectively. Then, the contact windows for source and drain were opened by dry etching. Subsequently, the polycrystalline-Si (Poly-Si) layer was deposited by low-pressure chemical vapour deposition (LPCVD). After doping the Poly-Si layer with phosphorus, we used electron-beam lithography and inductively coupled plasma (ICP) dry etching to make the source, drain, and gate electrodes simultaneously. After deposition of the SiO_2 layer by plasma-enhanced CVD (PECVD), metal contact windows were opened by wet etching, followed by Al/Ti layers deposition and patterning. The optical micrograph of the final device is shown in Fig. 3.

Electrical Characteristics

We characterized the transport properties by using a semiconductor parameter analyser (B1500A, Agilent), and a probe station at room temperatures. The background noise level was below 100fA. We confirmed excellent sub-threshold characteristics (Figs. 4 and 5). The narrowest device (nominal 1nm width) showed an on-current (I_{on}) of 342nA (0.342mA/μm) at 1.0V. The variation of threshold voltages and sub-threshold slopes are shown in Figs. 6 and 7 against nominal Si nanowire width. The sub-threshold slope in the narrowest device (nominal 1nm) was 60mV/decade at the drain voltage of 1.0V, which shown strong controllability [6], since our device is nearly a gate-all around nanowire FET. We also found that the threshold voltage of the device with the nominal width of 21nm was higher than the device with the width of 71nm. This would be attributed to the quantum mechanical confinement and subsequent band-gap increase in the narrower transistor [7]. However, the threshold voltage of the transistor with the nominal width of 1nm was smaller than the device with the width of 21nm. This can be explained by self-limiting oxidation due to the strain in the nanowire [8]. We expect the actual width of the nanowire should be much larger than the nominal value.

Conclusion

We fabricated nanowire transistors with TMAH etching to achieve atomically flat nanowires. The raised source/drain and gate electrodes were patterned simultaneously by dry etching. The threshold voltage shift due to quantum confinement was found in sub-100nm MOSFETs. We found that the self-limiting oxidation phenomenon occurred during the gate oxidation.

Acknowledgments

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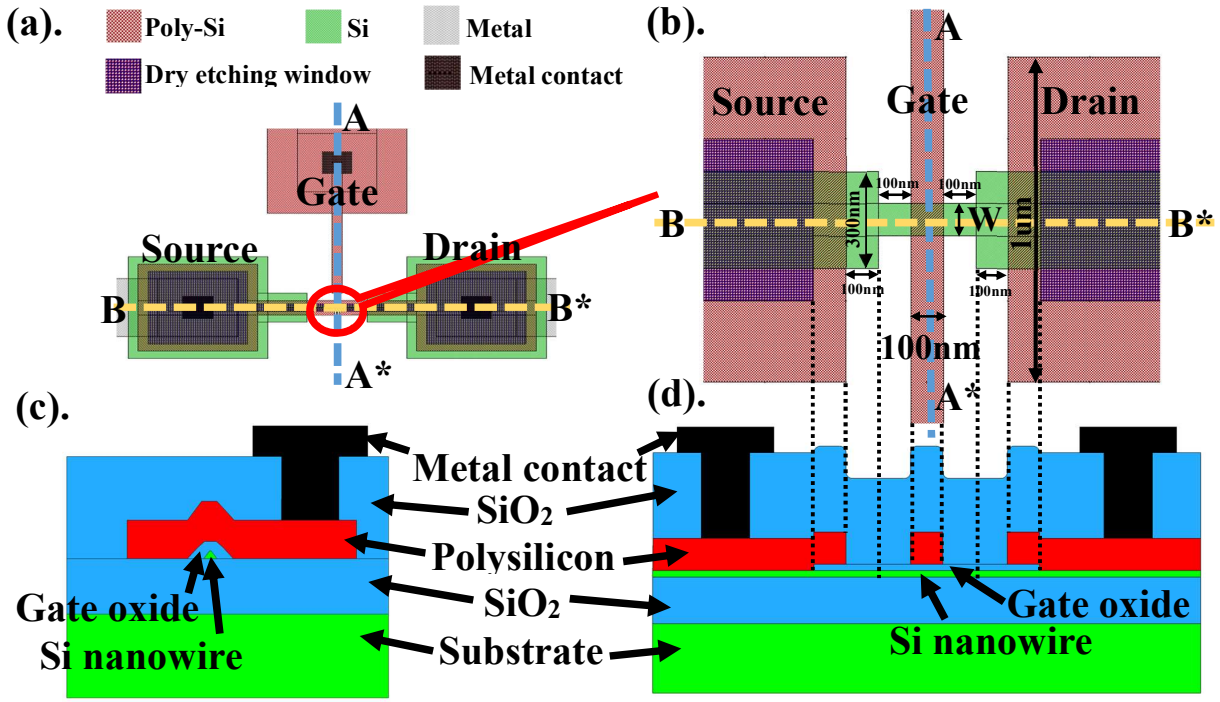

Fig. 1: Mask design and cross sections of the device. (a) Planar view of device region. (b) Planar view of nanowire region. (c) Cross section view in AA* direction (blue dash line). (d) Cross section view in BB* direction (yellow dash line).

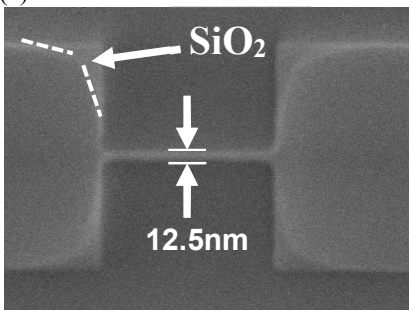

Fig. 2: SEM view of nanowire after TMAH etching (12.5nm). At the corners of the source and drain, the SiO_2 hard mask was suspended.

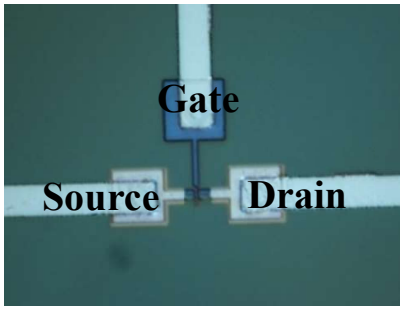

Fig. 3: Optical micrograph of Si nanowire transistor. The gate electrode is made of LPCVD Poly-Si, while the same Poly-Si layer was used for raised source and drain.

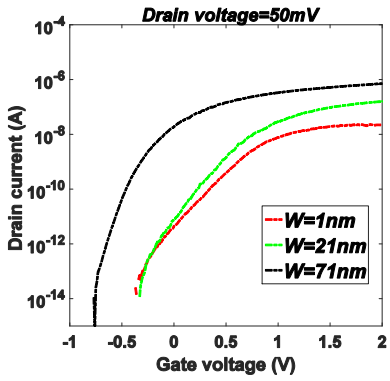

Fig. 4: Drain current vs Gate voltage curve at 50mV Drain voltage

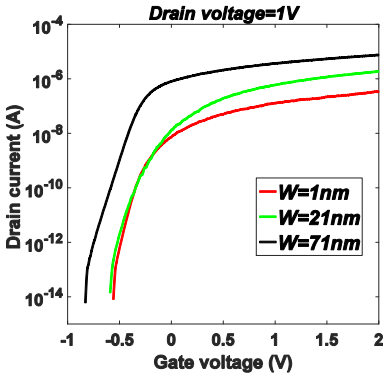

Fig. 5: Drain current vs Gate voltage curve at 1V Drain voltage

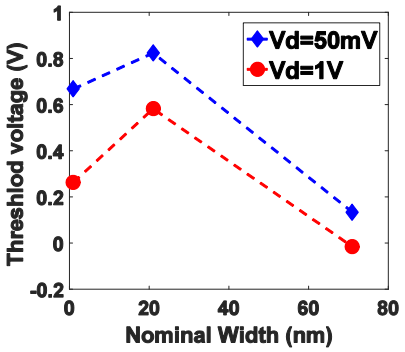

Fig.6 Threshold voltage with silicon nanowire width size dependent.

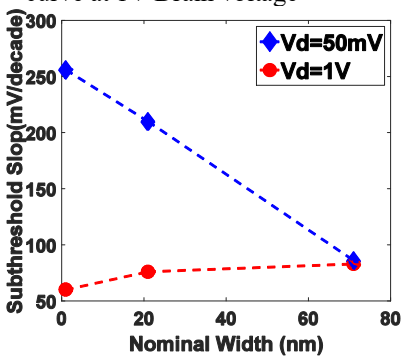

Fig.7 Subthreshold slope with silicon nanowire width size dependent.