Low-loss slot waveguides with silicon (111) surfaces realized using anisotropic wet etching

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Abstract

We demonstrate low-loss slot waveguides on silicon-on-insulator (SOI) platform. Waveguides oriented along the (11-2) direction on the Si (110) plane were first fabricated by a standard e-beam lithography and dry etching process. A TMAH based anisotropic wet etching technique was then used to remove any residual side wall roughness. Using this fabrication technique propagation loss as low as 3.7dB/cm was realized in silicon slot waveguide for wavelengths near 1550nm. We also realized low propagation loss of 1dB/cm for silicon strip waveguides.

1 Introduction

The slot waveguide structure was first proposed by Almeida et al. (Almeida et al., 2004) as a simple way to achieve extremely strong optical confinement in a low refractive index medium. Typically, an all-dielectric slot waveguide is formed by two high index waveguiding regions (e.g. silicon) separated by a narrow region of low index material (e.g. air, silica or polymer). Due to the discontinuity in the electric field at the high index contrast interfaces, such a structure supports an optical mode which can confine and guide light along the nanometer-size region of low index material, as shown in Fig. 1. This unique property of slot waveguides has been exploited in many areas such as sensing (Barrios et al., 2007; Carlborg et al., 2010), nonlinear optics (Martínez et al., 2010; Muellner et al., 2009), electro-optic modulation (Koos et al., 2009; Baehr-Jones et al., 2008; Chen et al., 2009), light sources (Guo et al., 2012; Tengattini et al., 2013) etc. However, a major limitation of slot waveguides is their high propagation loss. Since the light is more confined in the slot region, any surface roughness, introduced during the fabrication process, causes significant scattering loss. Therefore, fabrication of low loss slot waveguides is challenging and the lowest reported propagation loss was 10dB/cm (Baehr-Jones et al., 2005) from a standard vertical slot waveguide. There are different approaches proposed in the literature to reduce this propagation loss. For example, strip-loaded slot waveguides have been proposed with improved propagation loss of

6.5dB/cm (Ding et al., 2010); albeit for a reduced mode confinement in the slot region. Spott et al. reported a record low propagation loss of 1.7dB/cm (Spott et al., 2011) from a slot waveguide by introducing different silicon arm widths. This geometry also compromises the mode confinement in the slot region due the asymmetry in the waveguide geometry. Alasaarela et al. adopted a different approach to reduce the propagation loss by coating the waveguide surface by a thin layer of titanium dioxide (Alasaarela et al., 2011). This layer with intermediate refractive index effectively reduces the optical field intensity at the high index contrast interface and they reported a propagation loss of 7dB/cm for a slot waveguide.

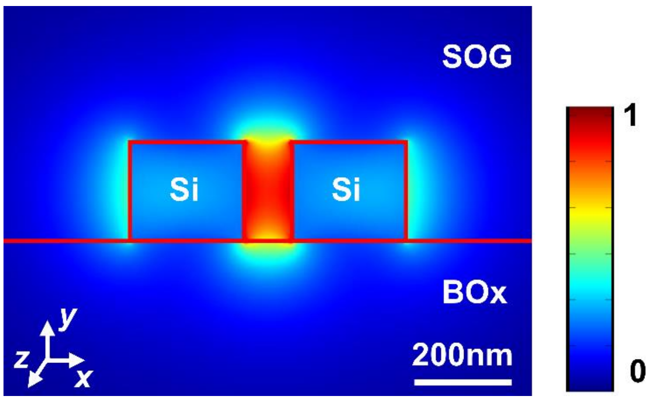

Fig. 1. Dominant Electric field (│Ex│) of the fundamental TE mode guided by the silicon slot waveguide on a buried oxide (BOx) substrate with a spin-on glass (SOG) surrounding medium. The waveguide is 220nm high and the slot width is 100nm with 225nm wide silicon arms on both sides.

In this letter we present a new and simple method of reducing waveguide loss by surface smoothening using a combination of dry and anisotropic wet etching processes. The wet etching process was used to smoothen the residual side wall roughness after dry etching. Here we used an aqueous solution of Tetramethylammonium hydroxide (TMAH), which is widely used for anisotropic wet etching of silicon. Due to its strong alkalinity, TMAH reacts very differently with silicon depending on the crystallographic orientation of the exposed region. For example, while (100) and (110) planes are etched by a TMAH solution, (111) planes remains almost unaffected. Since this is a completely chemical process and strongly depends on the crystallographic orientation of the etched surface, ideally we should expect an ultra-smooth surface with atomic level irregularity. Previously sub-dB propagation loss in silicon strip waveguides have been demonstrated using TMAH based wet etching process (Debnath et al., 2016; Lee et al., 2001). In this work, by combining dry and wet etching processes we managed to reduce the propagation loss of a slot waveguide with 200nm slot width from 10.5dB/cm to 3.7dB/cm and for a strip waveguide from 2.7dB/cm to 1dB/cm.

2 Fabrication Process

The fabrication process flow is shown in Fig. 2. The slot waveguides were fabricated on two Silicon-on-Insulator (SOI) substrates, namely sample A and sample B. Both the SOI substrates had 220nm thick layers of Si with (110) surface orientation on 2µm thick Buried Oxide (BOx). The advantage of choosing the (110) oriented substrate lies in the fact that (111) planes are normal to the (110) surface along (112) direction. As a result, when the waveguides are designed along the (112) directions, the (111) planes will act as an etch stop during the smoothening process. During the fabrication process, first a 20nm thick layer of SiO_2 was thermally grown by annealing the SOI substrates at 1000^{o}C in O_2 (dry anneal) for 6 minutes in a quartz furnace tube. The substrates were then spin-coated with a

250nm thick ZEP-520A positive e-beam resist layer. Using e-beam lithography, the desired waveguide patterns were exposed onto the ZEP layer via a 5nm spot size. The waveguides were designed to align along the (11-2) direction on the SOI substrates. After developing the exposed resist layer, the waveguide patterns were transferred to the SiO_2 hard mask and subsequently to the SOI layer in an inductively coupled plasma (ICP) etcher using a SF_6/C_4F_8 chemistry. After the dry etching process, the remaining resist was removed in an O_2 plasma asher. Final cleaning was carried out in fuming nitric acid and then diluted hydrofluoric acid. Surface roughness smoothening using anisotropic wet etching was carried out only on sample B. To avoid the formation of any native oxide layer, immediately after the HF cleaning process, the substrate was immersed in a 25% aqueous solution of TMAH at room temperature for 10 minutes. This duration was sufficient to significantly reduce the roughness from the waveguide surfaces. During this wet etching process, the top surfaces of the waveguides were protected by the SiO_2 hard mask while any roughness on the waveguide side walls was reduced. Since the etch rate is very slow along the (111) direction we expect an atomically flat and vertical side walls after the wet etching process. For comparison the wet etching step was omitted for sample A. Figure 3a and 3b show the SEM images of the slot waveguides without (sample A) and with (sample B) roughness smoothening using TMAH wet etching respectively. From the images, it is obvious that the surface roughness has been significantly reduced after the wet etching process. We have further carried out a detailed sidewall roughness analysis using Atomic Force Microscopy (AFM). We have used a special tapered AFM tip from Bruker (CDF100) to easily access the vertical side walls of the waveguides. The AFM image was then processed using Gwyddion AFM analysis software to extract the surface roughness information of the sidewalls. In the images Fig. 3c and Fig. 3d, the y-axis is along the length and the x-axis is along the height of the waveguide, whereas the surface roughness is represented along z-axis. The AFM images clearly reveals that the roughness reduces from an rms value of 6.7nm (Fig. 3c) for the dry etched waveguide to 1.4nm (Fig. 3d) for the wet etched waveguide. It is also important to note here that the slot waveguides which had undergone the wet etching step had 20nm larger slot width than designed, due to the slow etching of (111) plane. This slow etching of the (111) plane can also be used to precisely control the slot width by simply optimizing the wet etching time. Although in this work we have used e-beam lithography due to its quick turned around time, the same wet etching process can be used to smoothen the waveguide surfaces realized using standard photolithography processes. Finally, another thermal oxidation was carried on both the substrates to grow a 5nm thick layer of SiO_2, which acts as a surface passivation layer. In most applications the slot waveguides are cladded with low index materials such as polymers (Koos et al., 2009) or silica (Martínez et al., 2010). Here we spin coated the substrate with 500nm thick spin-on glass (SOG, Fox-16, Dow Corning) and annealed at 400^{o}C in N_2 environment for 4 hours to cure the SOG. This acts as a low-loss cladding for the slot waveguides which has the refractive index of around 1.45, similar to silica.

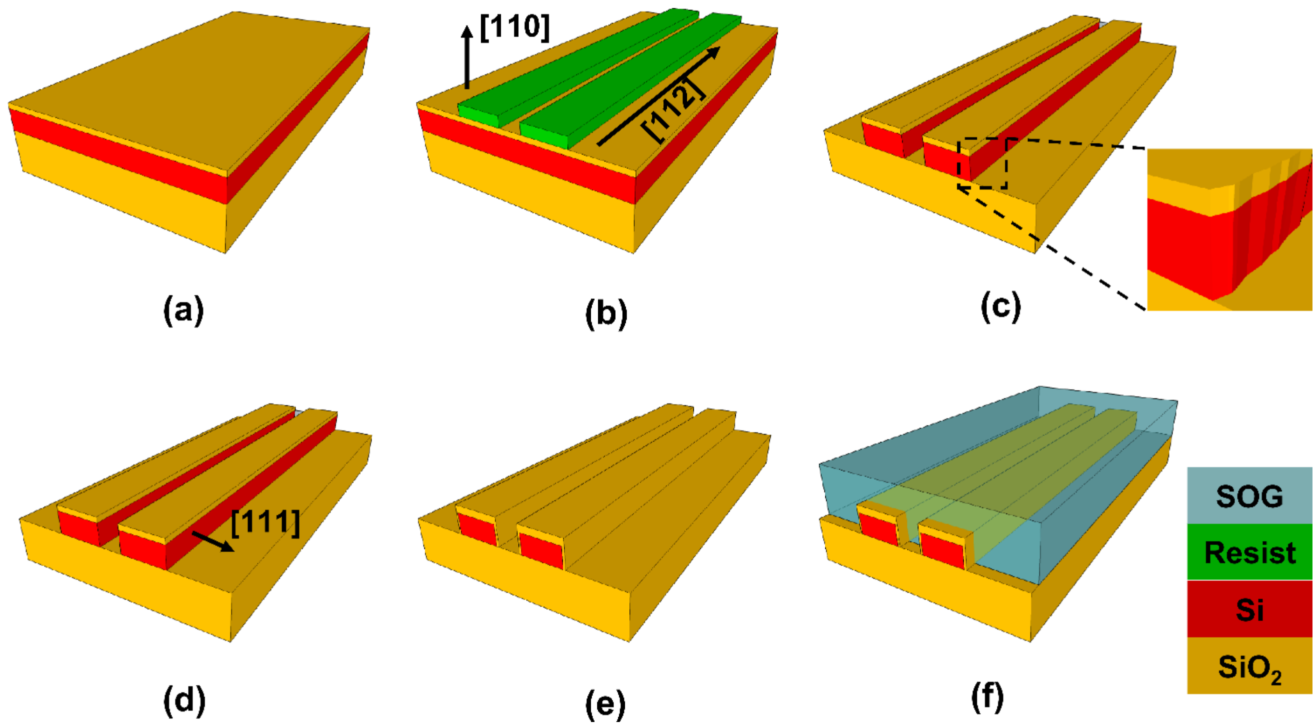

Fig. 2. Fabrication process flow: (a) a 20nm thick layer of SiO_2 was thermally grown on SOI substrate; (b) slot and strip waveguide patterns were written on the resist layer using e-beam lithography; (c) waveguide patterns were transferred to the silicon layer using ICP dry etching process; (d) SOI substrate was dipped into TMAH solution to remove any surface roughness (only for sample B); (e) a thin SiO_2 layer was thermally grown to serve as surface passivation; (f) finally 500nm thick layer of SOG was spin coated and cured.

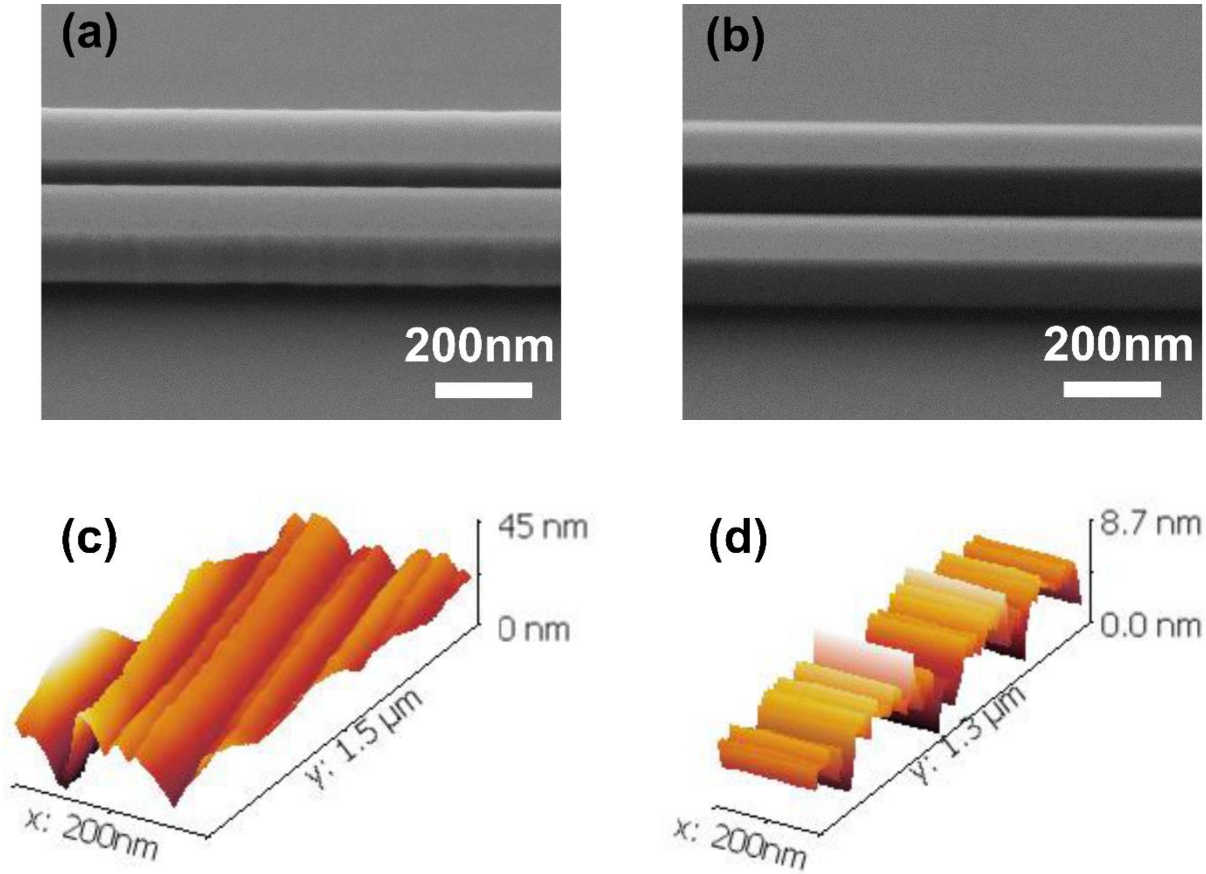

Fig. 3. SEM images of a waveguide (a) on the dry etched only sample (sample A) and (b) on the TMAH treated sample (sample B), imaged at an angle of 45°; (c) AFM image of the side wall of dry etched waveguide with rms roughness of 6.7nm; (d) AFM image of the side wall of wet etched waveguide with rms roughness of 1.4nm.

2.1 Measurement and results

The transmission through the fabricated slot waveguides was measured using a fibre-coupled tunable laser source with a tuning range from 1530nm to 1630nm. For all the measurements 10dBm laser power was used. Since the slot mode is a TE mode, the input of only TE polarized light was ensured with a fibre polarization controller. Coupling light onto the chip was achieved by fibre-grating couplers (Covey et al., 2013). The wavelength was scanned using the built-in sweeping ability of the laser, and the detector automatically recorded the output spectra. For both samples, the total fibre to fibre insertion loss was around 20dB, which includes the system loss and the grating coupler losses. For estimating the propagation loss in the strip waveguide and slot waveguides a cut-back method was used. Waveguides with four different lengths ranging from 2mm to 8mm were designed. For strip waveguides the waveguide width was 450nm. For slot waveguides, we designed 3 different slot widths of 100nm, 150nm and 200nm with 225nm wide silicon arms on both sides. Figure 4 shows the normalized transmission spectra, represented in light colors, of a set of slot waveguides with fixed slot width of 100nm and varied lengths. The peak transmission values for each length were estimated from the fitted curve using a quadratic function to match the grating coupler spectrum. The fitted curves are represented in dark colors in Fig. 4. We also observed ~1dB ripple in the measured transmission spectra. We attribute such fluctuations to the imperfect coupling region between the strip and slot section of the waveguide (shown in the inset of Fig. 4). This is caused due to sudden change in effective index of the optical mode at the coupling region. The coupling efficiency between the strip and slot waveguide region can be improved by carefully designing the coupling region as proposed previously in Han et al., 2016; Säynätjoki et al., 2011 and Passaro, 2012.

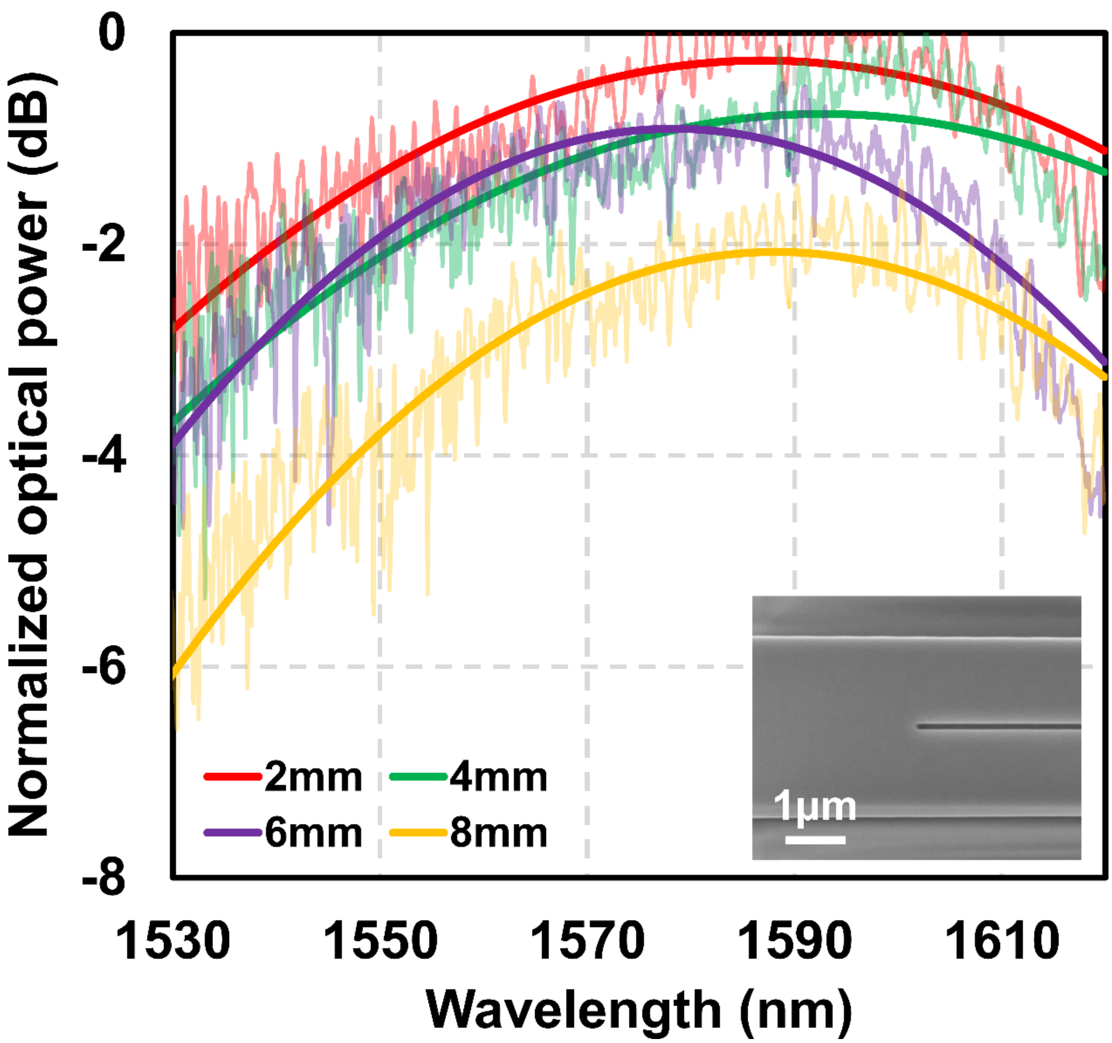

Fig. 4. Spectrum and quadratic function fitting for different waveguide lengths with slot width of 100nm. The inset shows the coupling region between the strip region and the slot region of the waveguide.

Figure 5 shows the cutback measurement results for different waveguide geometries under different etching conditions. In order to avoid any unwanted variation in the coupling condition, for each propagation length, we have measured a set of four waveguides and considered the average value for estimating the propagation loss. To emphasize the effect of our surface smoothening process on the waveguide loss, we have also normalized the waveguide transmission by setting the background loss (i.e. setup and coupling loss) to 0dB. In Fig. 5a-5d, the black circles represent the normalized transmission for dry etched waveguides on sample A and the red squares represent the normalized transmission of the waveguides after the surface smoothening step on sample B. The dashed lines represent the linear fits for the transmission data. For every waveguide geometry, we observed a significant reduction in the propagation loss. For strip waveguides the propagation loss reduced from 2.7dB/cm to 1dB/cm and for slot waveguides with 100nm, 150nm and 220nm the propagation loss dropped from 12dB/cm to 4.1dB/cm, 10.7dB/cm to 5dB/cm and 10. 5dB/cm to 3.7dB/cm respectively. We expected that the slot waveguide loss to monotonically reduce with increasing slot width, since the optical confinement also reduces with increasing slot width. However, we found that, although waveguide with 200nm slot has lower loss in comparison to waveguide with 100nm slot, the loss of 150nm slot is relatively higher. We believe this is due to experimental error and within our error limit. Also, we would like to mention that 20nm increase in slot width after wet etching should not have a significant effect on the propagation loss and according to our experimental results for such variation in the slot width we expect to see the loss value to change by less than 0.3dB/cm.

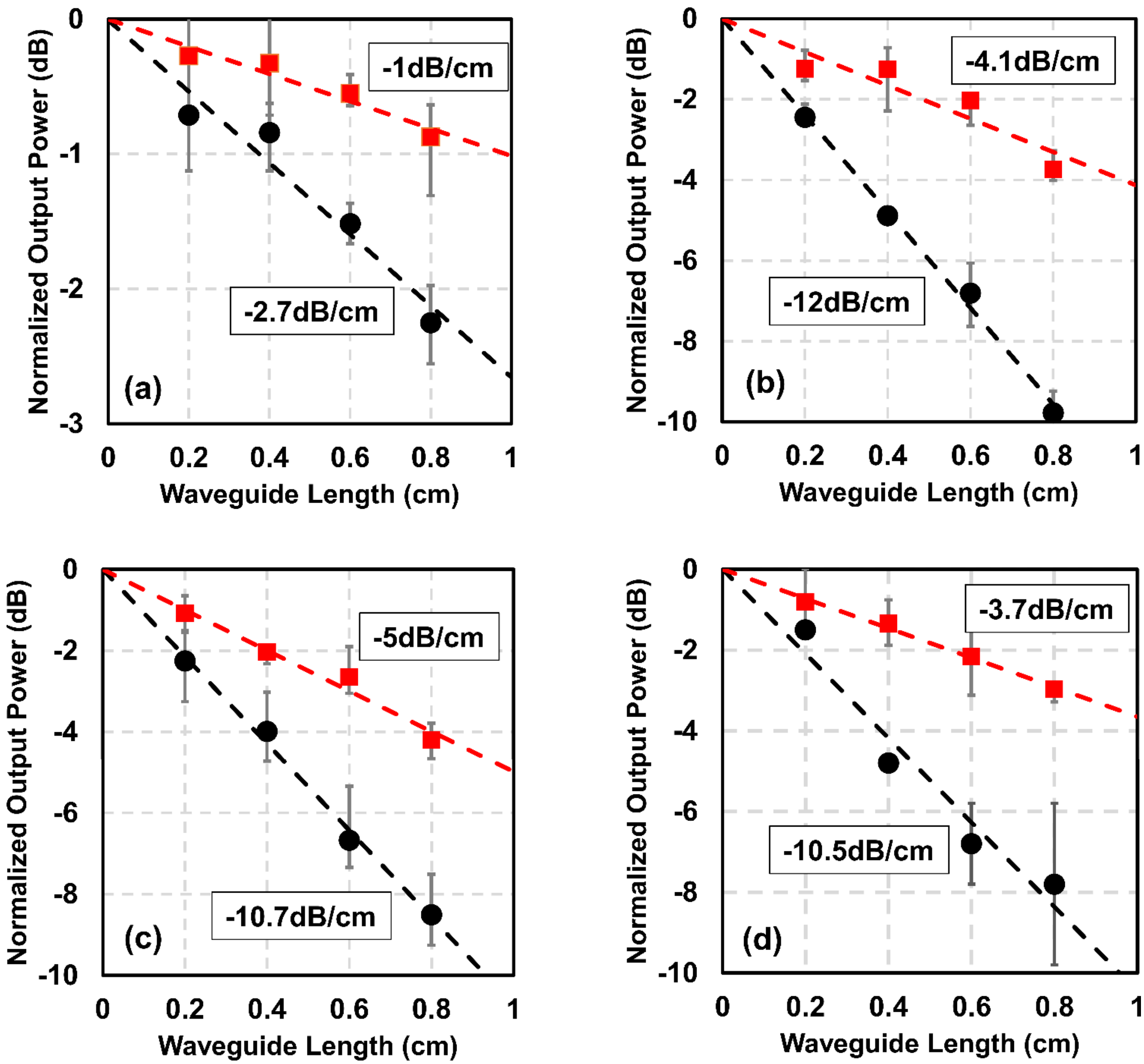

Fig. 5. Normalized optical output power vs. waveguide length after dry etching (black circle) and wet etching (red square) for (a) strip waveguide with no slot and slot waveguides with slot widths of (b) 100nm, (c) 150nm and (d) 200nm.

3 Conclusion

To summarize, in this letter, we have proposed and demonstrated a simple fabrication technique to realize low-loss strip and slot waveguides on SOI platform. Here we combined both dry and anisotropic wet etching processes to reduce propagation loss. The waveguides were first defined during the dry etching process and then the anisotropic wet etching process was used to remove any sidewall roughness. Using this fabrication technique we realized a slot waveguide with a minimum propagation loss of 3.7dB/cm for a slot width of 200nm. There are several advantages of our proposed fabrication technique. First, without using any asymmetry or multilayer structures, the propagation loss can be reduced in a symmetric slot waveguide. Secondly, our surface smoothening technique can be applicable to patterns realized using standard photolithography. Finally the slow etching rate of the (111) plane can be used to precisely control the slot width.

Anisotropic wet etching is very selective to crystallographic orientation of silicon. Although on one hand this allowed us to realize atomically flat surfaces and reduce propagation loss through silicon waveguides; due to its dependence on the crystallographic planes, out fabrication process restricts designing of nanophotonic components only along certain directions. This limitation can be avoided by adopting a hybrid fabrication process, where only certain components of the photonic integrated circuit, e.g. slot waveguide, undergoes the roughness smoothening process using anisotropic wet etching.

4 Acknowledgements

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5 Data Availability

All data supporting this study are available upon request from the University of Southampton repository at http://dx.doi.org/10.5258/SOTON/397774.

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