

Journal of Computational Electronics

Drain Current Multiplication In Thin Pillar Vertical MOSFETS Due to Depletion Isolation And Charge Coupling --Manuscript Draft--

Manuscript Number:	JCEL-D-16-00029
Full Title:	Drain Current Multiplication In Thin Pillar Vertical MOSFETS Due to Depletion Isolation And Charge Coupling
Article Type:	Manuscript
Keywords:	Vertical MOSFETS; Partially depleted; Fully depleted; Floating body effects.
Corresponding Author:	Mohammad Mojammel Al Hakim, PhD East West University Dhaka, BANGLADESH
Corresponding Author Secondary Information:	
Corresponding Author's Institution:	East West University
Corresponding Author's Secondary Institution:	
First Author:	Mohammad Mojammel Al Hakim, PhD
First Author Secondary Information:	
Order of Authors:	Mohammad Mojammel Al Hakim, PhD C. H. de Groot, PhD S. Hall, PhD Peter Ashburn, PhD
Order of Authors Secondary Information:	
Funding Information:	
Abstract:	<p>Drain current multiplication in vertical MOSFETS due to body isolation by the drain depletion region and gate-gate charge coupling are investigated at pillar thicknesses in the range 200-10 nm. For pillar thickness > 120 nm depletion isolation does not occur and hence the body contact is found to be completely effective with no multiplication in drain current, whereas for pillar thicknesses < 60 nm depletion isolation occurs for all drain biases and hence the body contact is ineffective. For intermediate pillar thicknesses of 60-120 nm, even though depletion isolation is apparent, the body contact is still effective in improving floating body effects and breakdown. At these intermediate pillar thicknesses, a kink is also observed in the output characteristics due to partial depletion isolation. The charging kink and the breakdown behaviour are characterized as a function of pillar thickness and a transition in the transistor behavior is seen at a pillar thickness of 60 nm. For pillar thickness greater than 60 nm, the voltage at which body charging occurs decreases (and the normalized breakdown current increases) with decreasing pillar thickness, whereas for pillar thickness less than 60 nm, the opposite trend is seen. The relative contributions to the drain current of depletion isolation and the inherent gate-gate charge coupling are quantified. For pillar thickness between 120 and 80 nm, the rise in the drain current is found to be mainly due to depletion isolation., whereas for pillar thicknesses < 60 nm, the increase in the drain current is found to be governed by the inherent gate-gate charge coupling.</p>

[Click here to view linked References](#)

1 J Comput Electron

2 DOI

3 Drain Current Multiplication In Thin Pillar Vertical MOSFETS Due to 4 Depletion Isolation And Charge Coupling

5
6
7
8
9
10
11 M. M. A. Hakim¹, C. H. de Groot², S. Hall³ and Peter Ashburn²12 *1 Dept. of Electrical & Electronic Engineering, East West University, Dhaka-1212, Bangladesh*13 *2 Nano Research Group, University of Southampton, Highfield, Southampton SO17 1BJ, UK*14 *3 Dept. of Electrical Engineering & Electronics, University of Liverpool, Brownlow Hill, Liverpool L69 3GJ, UK*15 *Email:dmmah@ewubd.edu*

16
17
18 **Abstract** Drain current multiplication in vertical
19 MOSFETs due to body isolation by the drain depletion
20 region and gate-gate charge coupling are investigated at
21 pillar thicknesses in the range 200-10 nm. For pillar
22 thickness > 120 nm depletion isolation does not occur
23 and hence the body contact is found to be completely
24 effective with no multiplication in drain current,
25 whereas for pillar thicknesses < 60 nm depletion
26 isolation occurs for all drain biases and hence the body
27 contact is ineffective. For intermediate pillar
28 thicknesses of 60-120 nm, even though depletion
29 isolation is apparent, the body contact is still effective
30 in improving floating body effects and breakdown. At
31 these intermediate pillar thicknesses, a kink is also
32 observed in the output characteristics due to partial
33 depletion isolation. The charging kink and the
34 breakdown behaviour are characterized as a function of
35 pillar thickness and a transition in the transistor
36 behavior is seen at a pillar thickness of 60 nm. For
37 pillar thickness greater than 60 nm, the voltage at
38 which body charging occurs decreases (and the
39 normalized breakdown current increases) with
40 decreasing pillar thickness, whereas for pillar thickness
41 less than 60 nm, the opposite trend is seen. The relative
42 contributions to the drain current of depletion isolation
43 and the inherent gate-gate charge coupling are
44 quantified. For pillar thickness between 120 and 80 nm,
45 the rise in the drain current is found to be mainly due to
46 depletion isolation., whereas for pillar thicknesses < 60
47 nm, the increase in the drain current is found to be
48 governed by the inherent gate-gate charge coupling.

49
50 **Key words** Vertical MOSFETs, Partially depleted,
51 Fully depleted, Floating body effects.

52 53 54 **1 Introduction**

55 Aggressive scaling of CMOS devices has highlighted
56 the requirement for fully depleted double or surround

57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000

gate MOSFETS in order to control short channel
effects at very short channel lengths [1]. The fully
depleted channel region and the double gate reduce the
field penetration from drain to source [2-3] and hence
give devices with almost ideal subthreshold slopes and
excellent short channel behavior. An additional
advantage of the increased gate control is that the
punch through stopper ($>10^{18}/\text{cm}^3$) required for
conventional bulk MOSFETs can be avoided and lower
channel doping can be used. This eliminates the
disadvantages of a high channel doping such as
increased leakage current [1], degraded mobility [4],
and threshold voltage variations due to random
microscopic fluctuations of dopant atoms both in
numbers and placement [5]. Therefore, fully depleted
double (DG) or surround gate MOSFETs are extremely
promising for high density, low voltage, and low power
DRAM, SRAM, and conventional CMOS applications.
Technologically these fully depleted double or
surround gate MOSFETs can be realized using DG SOI
[2,3,6-8], FinFETs [9-11] or vertical MOSFETs [12-
17].

Though a major advantage of DG SOI and FinFET
technologies is the ease of device isolation, in most
cases the body is left floating and hence, these devices
can suffer from floating body effects whereby weak
avalanche in the drain causes hole injection to the body
which raises the potential there. The rise in body
potential reduces the threshold voltage and also
forward biases the source-body junction which can
result in parasitic bipolar transistor (PBT) latch-up.
Extensive work has been done on floating body effects
in both partially depleted (PD) and fully depleted (FD)
planar SOI transistors [18-21].

Fig. 1 (a) and (b) show respectively, schematic cross-
sectional views of planar partially depleted SOI and
depletion isolated vertical MOSFET. The floating body
effects (FBE) are somewhat different for these two
architectures and a bulk MOSFET. The SOI device
usually experiences a steepening of the sub-threshold

slope for low drain voltage, leading to a latch effect due to the PBT, at higher drain voltage. The SOI-PBT gain tends to be emitter efficiency limited and so can be controlled by source engineering [20]. In a body contacted bulk MOSFET, floating body effects arise due to a resistive voltage drop caused by the flow of generated holes to the body contact, although for very short channel devices, a direct PBT action also contributes as generated holes preferentially flow from the body into the source. In the case of the vertical MOSFET with drain at the bottom (Fig. 1(b)) generated holes are separated by the geometry of the architecture. Holes are swept both upwards towards the source, causing the FBE and also downwards where they diffuse to the body contact.

Surround-gate vertical MOSFETs have the advantage that it is easier to make a body contact and hence, the floating body effect should potentially be less severe than in planar SOI MOSFETs. But with the scaling of pillar thickness the floating body effect is also observed in vertical MOSFETs during source on top mode of operation, even if a body contact is provided [22]. This effect has been termed depletion isolation [22] and is caused by the penetration of the depletion region of the bottom drain junction towards the center of the pillar and the eventual isolation of the pillar from the body contact as shown in fig. 1(b). In vertical MOSFETs the floating body effect therefore depends on both pillar thickness and drain bias, and hence is very different from the floating body effect seen in planar SOI transistors. Terauchi et al [22] found depletion isolation in partially depleted vertical MOSFETs and showed how this effect influenced the output and substrate current characteristics. However, no work has been reported on the transition from partially depleted to fully depleted operation in vertical MOSFETs or on the relative contributions of depletion isolation and gate-gate charge coupling to the drain current during this transition.

In this article a comprehensive investigation is undertaken of the transition from partial to fully depleted operation in vertical MOSFETs to better understand the depletion isolation effect. Floating body effects are simulated for different pillar thickness to characterize the impact of the body contact during the transition from partially depleted to fully depleted operation. Subsequently the contributions to drain current of depletion isolation and gate-gate charge coupling are quantified. It is found that the transition from partially depleted to fully depleted operation is different in vertical MOSFETs than in planar MOSFETs because the body contact affects the drain current even after depletion isolation. This result is explained by the strength of the potential barrier

formed by the merged drain depletion regions and the ability of holes of the isolated body to surmount the barrier.

2 Modeling Procedure

Analysis of the floating body effect was performed with the aid of numerical simulations using the Silvaco Atlas device simulator [23], implemented on a SUN workstation. A 100 nm channel length vertical ion-implanted double gate nMOSFET as shown in fig. 1(b), was simulated for different pillar thicknesses (T_{Si}). The gate oxide thickness was 2 nm and the gate electrode chosen was a metal with a work function of 4.5 V. The metal gate was chosen for optimal characteristics with no gate depletion problem [24] and low gate resistance. Employing a single metal approach, the gate work function needs to be somewhere near the mid-gap of the gate dielectric, hence making the work function difference ϕ_{ms} equal to zero. The bandgap of the gate dielectric, in this case, silicon dioxide, is about 9eV, which sets the work function of the gate electrode to be 4.5eV. The body doping was $10^{18}/\text{cm}^3$ and in source/drain regions a heavily doped region of $1 \times 10^{20} \text{ cm}^{-3}$ was surrounded by a lightly doped region of $1 \times 10^{19} \text{ cm}^{-3}$.

A 2D coupled Poisson's drift-diffusion solver was used to investigate the device operation. It is known that for a pillar thickness, $T_{Si} > 5 \text{ nm}$, quantum mechanical effects on threshold voltage (V_t) are not significant [25], suggesting that a classical distribution of inversion-layer electrons is still an appropriate approximation. This allowed the use of the 2D coupled Poisson's/drift diffusion solver in the pillar thickness range of 10 nm to 200 nm. To account for the reduced carrier concentration in heavily doped regions, Fermi-Dirac statistics were used to predict the carrier distribution and the effect of bandgap narrowing was also included.

To invoke the dependence of carrier mobility on the parallel and transverse fields in non-planar devices like vertical MOSFETs, the Lombardi CVT model was used [23]. In this model, the dependences of the transverse field, doping and temperature are given by three terms that are combined using Mathiessen's rule. These components are the surface mobility limited by scattering with acoustic phonons (μ_{AC}), the mobility limited by surface roughness (μ_{sr}) and the mobility limited by scattering with optical intervalley phonons (μ_b). The mobility parameters in the simulator were calibrated against a bulk silicon transistor [23]. In particular the mobility degradation due to surface roughness arising from dry etch of vertical pillar was

accounted for by adjusting the surface roughness factor in the model.

Impact ionization was modeled by the Selberherr law for the generation rate and the model parameters have already been optimized for submicron bulk silicon transistors [26]. The model for carrier emission and absorption processes proposed by Shockley-Read-Hall (SRH) was used to reflect the recombination phenomenon within the device. The electron and hole lifetimes τ_n and τ_p were modeled as concentration dependent. The simulations were performed at room temperature and the silicon parameter values were taken from [23, 26].

Fig. 2 compares the simulated I_d - V_g characteristics of a 100 nm channel length vertical MOSFET with the experimental characteristics reported in literature [15]. During this calibration we took the substrate-doping concentration to be $10^{18}/\text{cm}^3$ and the source/drain doping densities were taken from the SIMS profile of the fabricated device [15], where a heavily doped region of $10^{20}/\text{cm}^3$ was surrounded by a lightly doped region of $1 \times 10^{19} \text{ cm}^{-3}$. The gate electrode was polysilicon and polysilicon depletion was taken into account. It can be seen that satisfactory agreement between simulated and experimental characteristics is obtained when the surface roughness factor in the CVT model is reduced from $\delta(\text{elec}) = 5.82 \times 10^{14}$ and $\delta(\text{holes}) = 2.0546 \times 10^{14}$ to $\delta(\text{elec}) = 2.91 \times 10^{13}$ and $\delta(\text{holes}) = 1.027 \times 10^{13}$.

3 Results

Fig. 3 shows the output characteristics of the simulated vertical MOSFETs with and without a body contact, for three different pillar thicknesses and for source on top mode of operation. In the body contacted thick pillar vertical MOSFET (Fig. 3(a)), ideal characteristics are obtained with no evidence of a breakdown kink at high drain voltages. In contrast in the vertical MOSFET without a body contact, a breakdown kink can be seen at a drain voltage of around 4.4V, and the values of drain current are higher (1.73 times at $V_d=2\text{V}$) than equivalent values in the body contacted device at all drain voltages. These results indicate that in the thick pillar device, the pillar does not become isolated by the drain depletion region and the body contact is completely effective in suppressing floating body effects.

For the intermediate pillar thickness in fig. 3(b), the vertical MOSFET without a body contact shows similar characteristics to the equivalent device in fig. 3(a), although the impact ionization effect is sharper and the

values of drain current at a given drain voltage are slightly higher. In contrast, the body contacted device is considerably different than the equivalent body contacted device in fig. 3(a). In particular, the device shows an impact ionization effect at a drain bias around 4.4V and higher values of drain current at all drain voltages (1.15 times at $V_g=1.5\text{V}$ and $V_d=1.5\text{V}$). When comparing characteristics of the devices with and without a body contact, it can be seen that the body contacted device has lower values of drain current at all drain biases and the breakdown occurs at a slightly higher drain voltage.

For the thinnest pillar in fig. 3(c), the characteristics for vertical MOSFETs with and without a body contact are very similar, indicating that depletion isolation has occurred and the body contact is ineffective at this pillar thickness. The values of drain current are significantly higher than those for the device in fig. 3(b) (2.38 times at $V_g=1.5\text{V}$ and $V_d=1.5\text{V}$), and the avalanche breakdown effect is less severe because of the drain de-biasing effect due to the elevated body potential. This moderate floating body effect in fully depleted MOSFETs is well known [19].

To further investigate the role of impact ionization, fig. 4 compares the output characteristics of the device presented in fig. 3(b) with the output characteristics of the same device with a body contact but without impact ionization. The characteristic for the device without impact ionization represents the situation without any body charging. The characteristics for body contacted devices with and without impact ionization are similar at low drain biases ($\leq 2\text{V}$ for $V_g=1\text{V}$), clearly indicating that the body is not isolated at these voltages. For drain voltages above 2V, a kink in the output characteristics of the body contacted devices can be clearly seen, indicating body charging by holes from weak avalanche and the presence of depletion isolation at this pillar thickness. The difference in drain current between the devices with and without a body contact for drain biases above 2V indicates that floating body effects are less severe in the body contacted devices even after depletion isolation. This result indicates that the body contact has an effect on the drain current even after depletion isolation.

We now quantify the effect of the pillar thickness on the drain voltage at which body charge-up occurs. Fig. 5 shows the simulated values of charge-up drain voltage (V_{db}) as a function of pillar thickness for several values of gate voltage. The charge-up drain voltage (V_{db}) was calculated by comparing the output characteristics of body contacted devices with and without impact ionization, and identifying the voltage at which the characteristics diverged. A transition is

observed in the dependence of V_{db} at a pillar thickness of 60 nm. For pillar thicknesses ≥ 60 nm, V_{db} reduces with decreasing pillar thickness, whereas for pillar thicknesses < 60 nm, V_{db} increases with decreasing pillar thickness. A similar transition can also be seen in the dependence of V_{db} on gate voltage, V_g . For pillar thicknesses ≥ 60 nm, V_{db} decreases with increasing V_g , whereas for pillar thickness < 60 nm, V_{db} increases with increasing V_g .

To characterize the role of the body contact on the impact ionization effect we have quantified the severity of breakdown at high drain bias (5V) by calculating the normalized breakdown current. This was defined as the difference in drain current of devices with and without impact ionization divided by the drain current without impact ionization, ie, Normalized breakdown current = $(I_D \text{ with impact ionization} - I_D \text{ without impact ionization}) / I_D \text{ without impact ionization}$. Fig. 6 shows the normalized breakdown current of vertical MOSFETs with and without a body contact as a function of pillar thickness for various values of gate voltage. Three different regimes of vertical MOSFET operation can be identified. In the thick pillar regime, the pillar is not isolated and hence the simulated drain currents of body contacted devices with and without impact ionization are similar, giving low values of normalized breakdown current. In contrast, the device without a body contact shows floating body effects, giving a high value of normalized breakdown current. For pillar thickness between 120 and 60 nm, the impact ionization effect is observed in both devices with and without a body contact, though the normalized breakdown current is always lower in the device with a body contact. It can therefore be seen that even though the pillar is isolated, the normalized breakdown current is still lower in body contacted devices. This indicates that even when the pillar is depletion isolated, the body contact still plays an important role in improving the breakdown behavior and in reducing the normalized breakdown current. For pillar thicknesses < 60 nm, the devices are depletion isolated at all drain biases and devices with and without body contact show similar breakdown characteristics and hence similar values of normalized breakdown current. In this regime the body contact is ineffective. A similar transition to that observed in fig. 5 can be seen in the normalized breakdown current of body contacted vertical MOSFETs, at a pillar thickness of 60 nm. For pillar thickness ≥ 60 nm, the normalized breakdown current of body contacted devices increases with decreasing pillar thickness, whereas for pillar thickness < 60 nm the normalized breakdown current decreases with decreasing pillar thickness.

4 Discussion

In this section the role of the body contact after depletion isolation and the origin of the charging kink are physically explained using the depletion isolation phenomenon. Fig. 7 shows the simulated depletion region edges of body contacted vertical MOSFETs at low (0V) and high (5V) drain bias (before and after depletion isolation) for various pillar thicknesses. For a pillar thickness of 200 nm (fig. 7(a)), no depletion isolation occurs within the range of drain biases shown in fig. 3. Therefore, no body charging occurs and the output characteristic of the body contacted vertical MOSFET does not exhibit any breakdown trend or charging kink as seen in fig. 3(a). The difference in current in fig. 3(a) between the vertical MOSFETs with and without a body contact at high drain biases is the well-known impact ionization effect, which has been explained elsewhere in the literature [18-20]. The difference in current found, at low drain bias in the weak impact ionization regime can be mainly attributed to the body potential differences between the vertical MOSFETs with and without body contact. In the body contacted vertical MOSFET potential profile of body is different than that of the vertical MOSFET without body contact due to forced grounding of the body. This difference in current between devices with and without a body contact is also seen in planar devices [21].

For pillar thicknesses of 120 and 80 nm (fig. 7(b)), pillar is not isolated at low drain bias. At high drain bias the depletion region from the bottom drain region gradually isolates the Si pillar from the substrate and divides the body into two distinct regions. In body contacted vertical MOSFETs region two still remains connected to the body contact at the bottom of the pillar after the depletion isolation, whereas region 1 is isolated. In vertical MOSFETs without a body contact both regions are isolated. The effect of such a separation of regions 1 and 2 on drain current will be discussed later. However, contrary to the thick pillar case, the observed breakdown behaviour in the body contacted vertical MOSFETs of 80 nm pillar thickness (Fig. 3(b)) definitely reflects the existence of depletion isolation as can be seen from the presence of the impact ionization effect in the body contacted device. However, the body contact still influences the output characteristics at this pillar thickness, as can be seen from the different values of drain current at all drain biases in devices with and without a body contact. It is worth noting that the change from total depletion (i.e., insignificant majority carrier concentration) to perfect neutral is not abrupt and the transition between the depleted and neutral region extends over 2-3 Debye lengths on each side of the pillar. For a body doping of

$10^{18}/\text{cm}^3$ there is a 10-15 nm of transition region for depletion isolation consideration. Therefore, once depletion regions from the two sides of the pillar overlap, the strength of the merged depletion region depends on pillar thickness due to Debye length considerations. Moreover, this also controls the actual PD-FD boundary [27].

For a pillar thickness of 60 nm, fig. 7(c) shows that the pillar is isolated at all drain biases and hence the pillar is fully depleted. Therefore, for pillar thickness of 60 nm or less, the output characteristics of devices with and without a body contact are very similar, as can be seen in fig. 3 (c) for a pillar thickness of 10 nm. A moderate breakdown kink is also found at this pillar thickness, which has already been explained by Fossum et al. [19] by classical gate coupling theory [28].

To help explain the different output characteristics in fig. 3(b) for devices with and without a body contact, fig. 8 shows the hole concentration contour plot and the drain body potential barrier at the middle of the pillar for pillar thicknesses of 80 and 60 nm at $V_g=1$ V and $V_d=5$ V. At this bias condition pillar is isolated in both devices. For pillar thickness of 80 nm (fig. 8(a)), it can be seen that even if the pillar is isolated, some holes surmounts the potential barrier of the depletion region merged at the bottom of the pillar. This is possible because the potential barrier is small, with a value of 0.052 eV (i. e., 2kT). In contrast, for a pillar thickness of 60 nm, fig. 8(b) shows that the potential barrier is much bigger (0.52eV) and hence the hole flow from the pillar to the substrate is almost stopped This indicates that even though the pillar is isolated, the strength of the merged depletion region at the bottom of the pillar controls the hole flow to the body contact, hence the device behaviour. Therefore, even though the body is isolated, the body contact still influences the output characteristic as shown in fig. 3(b) for a 80 nm pillar.

We now discuss the transition in the charge up drain bias (V_{db}) seen in fig. 5 at a pillar thickness of 60 nm. This can be explained from the above relationship between the pillar thickness and depletion isolation at the bottom of the pillar. Reducing the pillar thickness at a fixed gate bias brings the depletion regions at the bottom of the pillar closer together. In addition, increasing the gate voltage at a given pillar thickness also brings depletion regions closer together. Therefore, as the pillar thickness is reduced from 120 to 60 nm, the charge up drain bias (V_{db}) decreases with decreasing pillar thickness because depletion isolation occurs at progressively lower values of drain bias. Similarly, the increased drain depletion width resulting from an increased gate voltage also causes V_{db} to decrease with increasing gate voltage. In contrast, for

pillar thicknesses < 60 nm, the pillar is fully depleted and isolated even at zero drain bias. Scaling of the pillar thickness from 60 nm to 10 nm results in a transition to a more strongly depleted regime of operation and therefore, V_{db} increases with decreasing pillar thickness and also increases with increasing gate voltage at a given pillar thickness.

We now explain the impact ionization effect in fig.6. The convergence of the normalized breakdown current for devices with and without a body contact and the peak in the normalized breakdown current of the body contacted device at a pillar thickness of 60 nm can be explained by the same relationship between the pillar thickness and depletion isolation at the bottom of the pillar. Reducing pillar thickness from 120 to 60 nm, results in the strengthening of drain-body potential barrier due to the merged depletion regions. This causes the body contact to become gradually less effective for any fixed bias condition with the scaling of the pillar thickness and results in the convergence of the normalized breakdown current for devices with and without a body contact. In contrast, the reduction in the normalized breakdown current for pillar thickness < 60 nm is due to the fully depleted regime of operation. The behaviour found for pillar thicknesses < 60 nm, corresponds to the film thickness scaling effect seen in planar SOI MOSFETs [21].

To fully explain the output characteristics in fig. 3 and the behaviour in the depletion isolation region in figs 5 and 6, we need to consider the effect of the charge coupling of the two gates. In thin pillar, depletion isolated vertical MOSFETs we would expect the threshold voltage to decrease due to the coupling of the fields from the two gates. This would reduce the source-body potential barrier (ϕ_{SB}) and cause a rise in drain current with decreasing pillar thickness. At the same time holes generated by impact ionization would forward bias the body and result in a further increase in drain current. To isolate the effects of depletion isolation and gate-gate charge coupling we have simulated devices at various pillar thickness with and without impact ionization. A relative drain current was then calculated by dividing the drain current of the device at a given pillar thickness by the drain current of the 200 nm pillar device with impact ionization deactivated. The drain current at the pillar thickness of 200 nm was chosen because at this pillar thickness there is no coupling of the gates and also there is no depletion isolation. Therefore the curve without impact ionization allows us to see the rise in the drain current due to the gate-gate charge coupling, whereas the curve with impact ionization takes account of both depletion isolation and gate-gate coupling. Fig. 9 shows the

relative drain current as a function of pillar thickness for vertical MOSFETs with and without impact ionization and for $V_g=2$ V and $V_d=3.5$ V. We see that for pillar thickness ≥ 140 nm, the relative drain currents with and without impact ionization are identical. This indicates that at these pillar thicknesses, the pillar is not isolated and there is no gate-gate charge coupling. The rise in drain current due to gate-gate coupling starts at a pillar thickness of 100 nm, whereas the effect of depletion isolation starts at a pillar thickness of 120 nm. For pillar thicknesses between 120 and 80 nm, we see that the rise in relative drain current is mainly due to depletion isolation, for a pillar thickness 60 nm the two mechanisms contribute similar amounts to the rise in current, and for pillar thicknesses ≤ 40 nm, the rise in current is mainly due to the gate-gate charge coupling. This result indicates that depletion isolation dominates the device behaviour for pillar thicknesses in the range of 120-80 nm. However, for pillar thicknesses ≤ 40 nm the depletion isolation effect is suppressed and the device operates in the fully depleted regime where the behaviour is dominated by the inherent gate-gate charge coupling.

We also investigate the combined effect of depletion isolation and coupling of channels on the source-body potential barrier (ϕ_{SB}). Fig. 10 shows the simulated source body potential barrier (ϕ_{SB}) in vertical MOSFETs with and without a body contact as a function of pillar thickness for various values of gate voltage. ϕ_{SB} were calculated in the middle of the pillar at $V_{DS}=5$ V (heavy impact ionization regime). It is found that for the device without a body contact, ϕ_{SB} decreases slowly with reducing pillar thickness, whereas for the body contacted device a sharp decrease is observed, beginning at a pillar thickness of 120 nm and ending at a pillar thickness of 60 nm. This behaviour is due to depletion isolation raising the potential of the body and thereby decreasing the source/body potential barrier (ϕ_{SB}). The effect of the change in ϕ_{SB} on recombination is exemplified in fig. 8(b). A drastic increase of the recombination is observed in body contacted devices when the pillar thickness is reduced below 120 nm.

Finally we investigate the effect of body separation by depletion isolation on the drain current. Two types of devices were simulated to study this effect as shown in fig. 11. Fig. 11(a) corresponds to a device with a large body region below the pillar, whereas fig. 11(b) corresponds to a device with a small body region below the pillar. Fig. 12 shows the output characteristics of the two types of device presented in fig. 11. It is found that device 12(a) and 12(b) show identical output characteristics both in body contacted and floating

body conditions, indicating that carriers below the pillar has no effect on the drain current.

4 Conclusions

We have investigated depletion isolation and the effect of the body contact in vertical MOSFETs with pillar thicknesses in the range 200-10 nm to study the drain current multiplication in vertical MOSFETs during transition from partial to fully depleted operation. For pillar thicknesses > 120 nm the body contact is completely effective with no multiplication in drain current and the output characteristics do not exhibit any breakdown trend, whereas for pillar thickness < 60 nm the body contact is ineffective. For pillar thickness between 120 and 60 nm depletion isolation gives rise to a charging kink in the output characteristics of body contacted devices due to body charging after depletion isolation. Though depletion isolation occurs in this regime, the body contact is still partially effective after depletion isolation, as can be seen from improved floating body effects and improved breakdown behaviour. In this regime the voltage at which the charging kink occurs and the normalized breakdown current vary with pillar thickness and shows a transition at a pillar thickness of 60 nm. For pillars thicker than 60 nm, the body charging voltage decreases (and the normalized breakdown current increases) with decreasing pillar thickness, while for pillars thinner than 60 nm the opposite trend is seen. For the pillar thicknesses > 60 nm, the trend observed with reducing pillar thickness are explained by the occurrence of depletion isolation at progressively lower drain voltages and the strengthening of the potential barrier at the drain due to the merged depletion regions. Whereas the trend observed for pillar thickness < 60 nm, are explained by the fully depleted regime of operation. For pillar thickness between 120 and 80 nm, it has been shown that depletion isolation dominates the drain current of body contacted devices, whereas for pillar thicknesses of ≤ 40 nm, the inherent gate-gate charge coupling under the two gates dominates, because the device is operating in the fully depleted regime.

Acknowledgements

The authors would like to acknowledge the support of the Commonwealth High Commission and the European Union (SINANO project).

References

1. Y. Taur et al.: CMOS scaling into nanometer regime. Proc. IEEE, **85**, 486-504 (1997).
2. K. Kim and J. G. Fossum: Double-gate CMOS: symmetrical-versus asymmetrical-gate devices. IEEE Trans. on Electron Devices, **48**, 294-299 (2001).
3. M. leong et al.: DC and AC performance analysis of 25 nm symmetric/asymmetric double-gate, back-gate and bulk CMOS. In: IEEE Simul. Semicond. Process Devices Conf., Seattle, WA, pp. 147-150 (2000).
4. T. Ghani et al.: Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors. In: Symp. VLSI Tech. Dig. Tech. Papers, pp. 174-175 (2000).
5. R. W. Keyes: The effect of randomness in the distribution of impurity atoms on FET threshold. Applied Physics A: Mater. Sci. Process, **8**, 251-259 (1975).
6. T. Tanaka, K. Suzuki, H. Horie and T. Sugii: Ultrafast operation of V_{th} -adjusted p+n+ double gate SOI MOSFETs. IEEE Electron Device Lett., **15**, 386-388 (1994).
7. J. P. Cloinge et al.: Silicon-on-insulator gate all around device. In: IEDM Tech Dig., San Francisco, CA, pp. 595-598 (1990).
8. J. H. Lee et al.: Super self aligned double-gate (SSDG) MOSFETS utilizing oxidation rate difference and selective epitaxy. In: IEDM Tech. Dig., Washington, DC, pp. 71-74 (1999).
9. Y. Liu et al.: Ideal rectangular cross-section Si-Fin channel double-gate MOSFETs fabricated using orientation-dependent wet etching. IEEE Electron Device Letters, **24**, 484-486 (2003).
10. Bin Yu et al.: Finfet scaling to 10 nm gate length. In: IEDM Tech. Dig., pp. 251-253 (2002).
11. Digh Hisamoto et al.: Finfet-a self aligned double-gate MOSFET scalable to 20 nm. IEEE trans. on Electron Devices, **47**, 2320-2325 (2000).
12. T.Schulz, W.Roesner, L.Risch, and U.Langemann: 50-nm Vertical Sidewall Transistors with High Channel Doping Concentrations. In: IEDM Tech. Dig., pp. 61-64 (2000).
13. M. Masahara, T. Matsukawa, K. Ishii, Y.Liu, and H. Tanoue et al.: 15-nm-Thick Si Channel Wall vertical Double-Gate MOSFET. In: IEDM Tech. Dig., pp. 949-951 (2002).
14. X. Zheng, M. Pak, J. Huang, S. Choi, and K. L. Wang: A vertical MOSFET with a leveling, surrounding gate fabricated on a nanoscale island. In: IEEE Device Research Conf. Dig., pp. 70 – 71 (1998).
15. T. Schulz, W. Rosner, L. Risch, A. Korbel, and U. Langmann: Short-channel vertical sidewall MOSFETs. IEEE Trans. Electron Devices, **48**(8), 1783–1788 (2001).
16. J. Moers, S. Trelenkamp, M. Goryll, M. Marso, A. van der Hart, and S. Hogg et al.: Top contacts for vertical double-gate MOSFETs. Microelectronic Engineering, **64**, 465-471 (2002).
17. C.P.Auth and J.D.Plummer: Vertical, Fully-Depleted, Surrounding Gate MOS-FETs on sub-0.1um Thick Pillars. In: IEEE Device Research Conf. Dig., pp. 172–175 (1996).
18. G. A. Armstrong, S. D. Brotherton and J. R. Ayres: A comparison of the kink effect in polysilicon thin film transistors and silicon on insulator transistors. Solid State Electronics, **39**, 1337-1346 (1996).
19. J. G. Fossum, S. Krishnan, O. Faynot and S. Cristoloveanu: Subthreshold kinks in fully depleted SOI MOSFET's. IEEE Electron Device Letters, **16**, 542-544 (1995).
20. Kelvin Hui et al.: Body self bias in fully depleted and non-fully depleted SOI devices. In: Proceedings 1994 IEEE International SOI Conference, pp. 65-66 (1994).
21. F. Balestra et al.: Moderate kink effect in fully depleted thin-film SOI MOSFET's. Electronic Letters, **31**, 326-327 (1995).
22. M. Terauchi, N. Shigyo, A. Nitayama and F. Horiguchi: Depletion isolation effect" of surround gate transistors. IEEE Trans. on Electron Devices, **44**, 2303-2305 (1997).
23. Silvaco international, Atlas User's Manual Device Simulation Software, Silvaco International Ltd., Santa Clara, Dec., (2002).
24. M. Orshansky et al.: Polysilicon depletion and inversion layer quantization on NMOSFET scaling. In: IEEE Conf. Dig., 56th Annual Device Research, pp. 18-19 (1998).
25. H. Wong et al.: Device design considerations for double-gate ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation. In: IEDM Tech. Dig., pp. 407 (1998).
26. R. Van Overstraeten and H. De Man: Measurements of the ionization rates in diffused silicon p-n junctions. Solid State Electronics, **13**, 583-608 (1970).
27. F. Allibert et. al.: Transition from partial to full depletion in silicon-on-insulator transistors: Impact of channel length. Applied Physics Letters, **84**, 1192-1194 (2004).
28. H.-K. Lim and J. G. Fossum: Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's. IEEE Trans. on Electron Devices, **30**, 1244-1251 (1983).

List of figures

Fig. 1 Schematic cross-sectional view of a) planar SOI and b) vertical MOSFET operated in the depletion isolated mode.

Fig. 2 Comparison of simulated and measured transfer characteristics (I_d vs V_g) of the 100 nm channel length ion-implanted vertical MOSFET reported in [15].

Fig. 3 Simulated output characteristics (I_d vs V_d) of vertical MOSFETs with and without a body contact for pillar thicknesses of a) 200 nm, b) 60 nm and c) 10 nm.

Fig. 4 Simulated output characteristics (I_d vs V_d) of vertical MOSFETs with and without a body contact at a pillar thickness of 80 nm and with impact ionization (II) turned on and off. Dashed lines represent the vertical MOSFET with impact ionization and without a body contact, solid lines represent the body contacted vertical MOSFET with impact ionization and circles represent the body contacted vertical MOSFET without impact ionization.

Fig. 5 Simulated values of charge-up drain voltage (V_{db}) as a function of pillar thickness and for several values of gate voltage. V_{db} was calculated by comparing the output characteristics of body contacted devices with and without impact ionization and identifying the voltage at which characteristics diverge.

Fig. 6 Simulated normalized breakdown current of vertical MOSFETs with and without a body contact as a function of pillar thickness and for several values of gate voltage. The normalized breakdown current was defined as the difference in drain current of devices with and without impact ionization divided by the drain current without impact ionization.

Fig. 7 Cross-sectional views of body contacted vertical MOSFETs before and after depletion isolation, for pillar thicknesses of a) 200 nm, b) 120 and 80 nm and c) 60 nm. In the figure x and y-axis represents device dimensions in micron.

Fig. 8 Hole concentration contour plot and the drain body potential barrier of the vertical MOSFET at the middle of the pillar, for pillar thicknesses of a) 80 nm, and b) 60 nm. The gate voltage was 1V and the drain voltage was 5V.

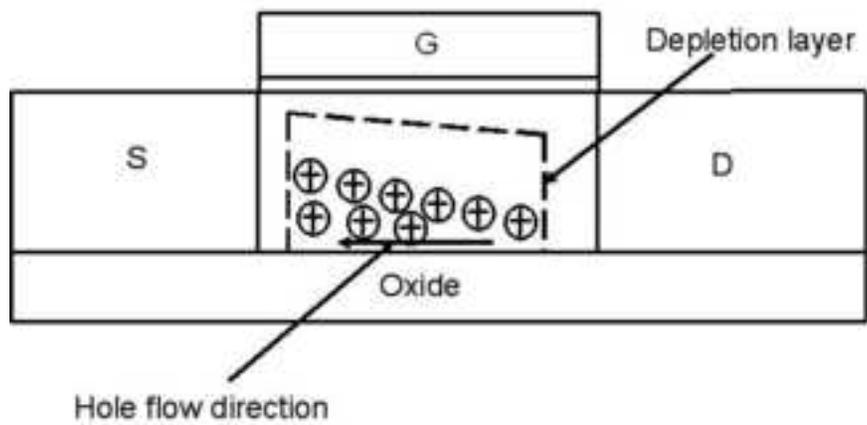
Fig. 9: The relative drain current of vertical MOSFETs as a function of pillar thickness with and without impact ionization for $V_g=2$ V and $V_d=3.5$ V. The relative drain current was calculated by dividing the drain current of the device at various pillar thicknesses by the drain current of the device for a pillar thickness of 200 nm with impact ionization inactivated.

1
2
3 **Fig. 10:** Source body potential barrier (ϕ_{SB}) and the recombination
4 rate in vertical MOSFETs with and without a body contact as a
5 function of pillar thickness for various values of gate voltage. The
6 drain bias was 5V.

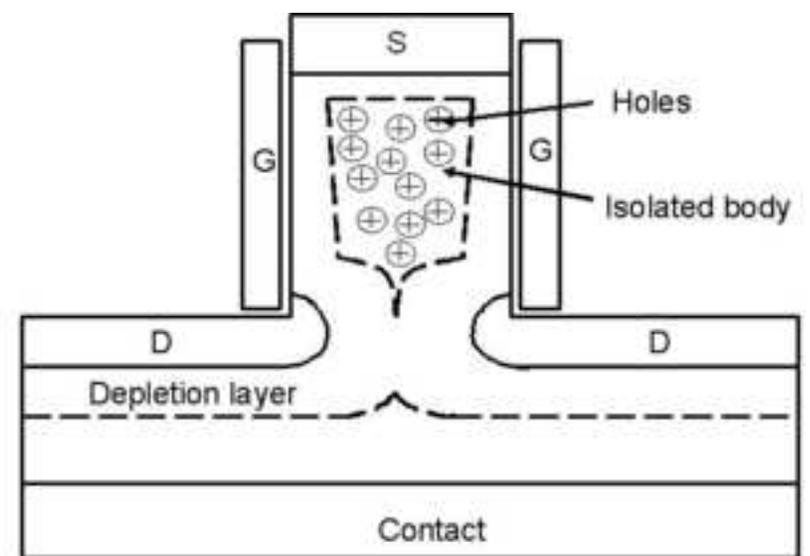
7 **Fig. 11** Schematic cross-sectional views of vertical MOSFETs with
8 large (a) and small (b) body regions below the pillar (region 2).

9 **Fig. 12** Simulated output characteristics (I_d vs V_d) of vertical
10 MOSFETs with large and small body regions below the pillar (fig.
11). Results are shown for devices with and without a body contact.

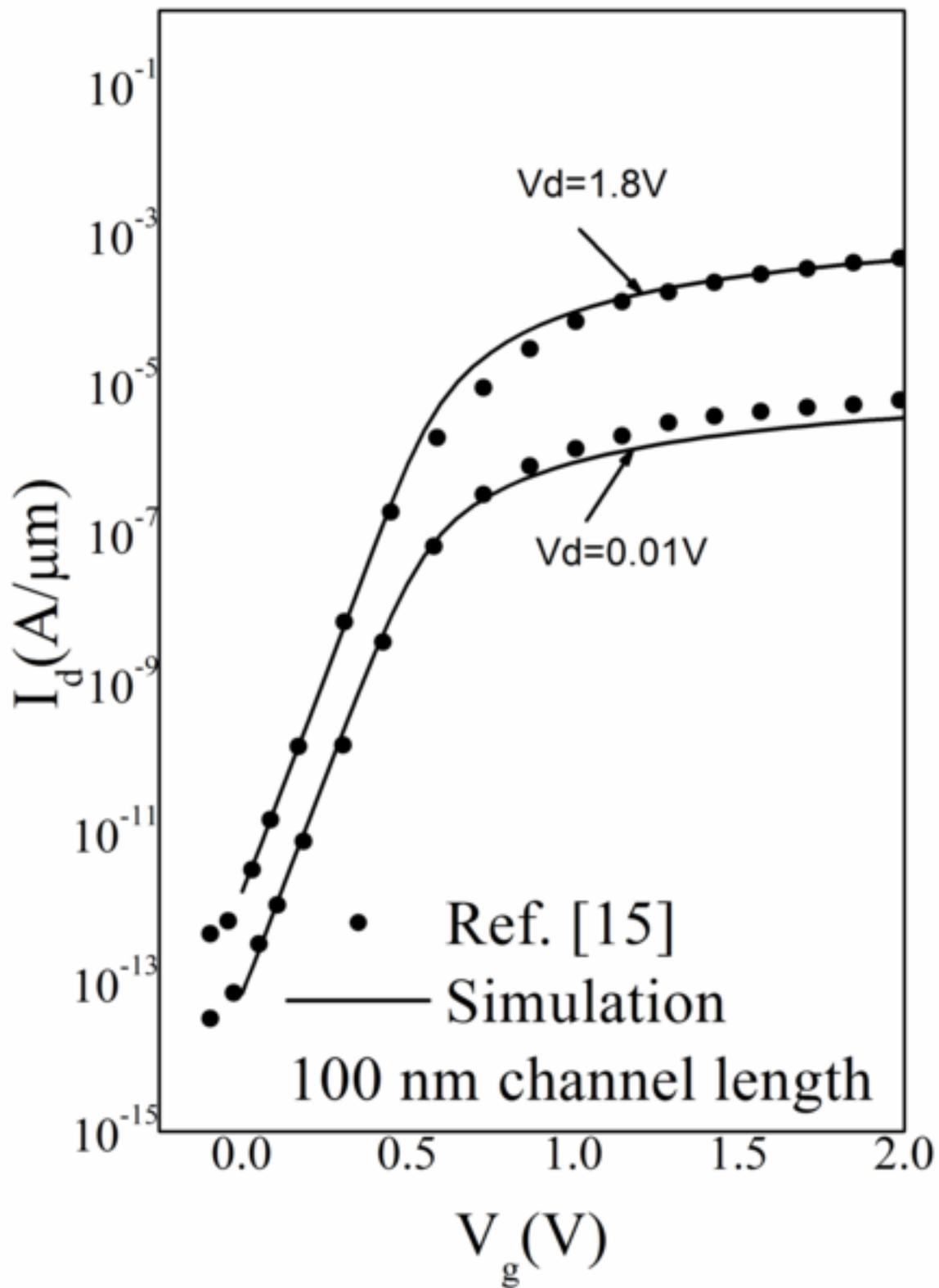
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65

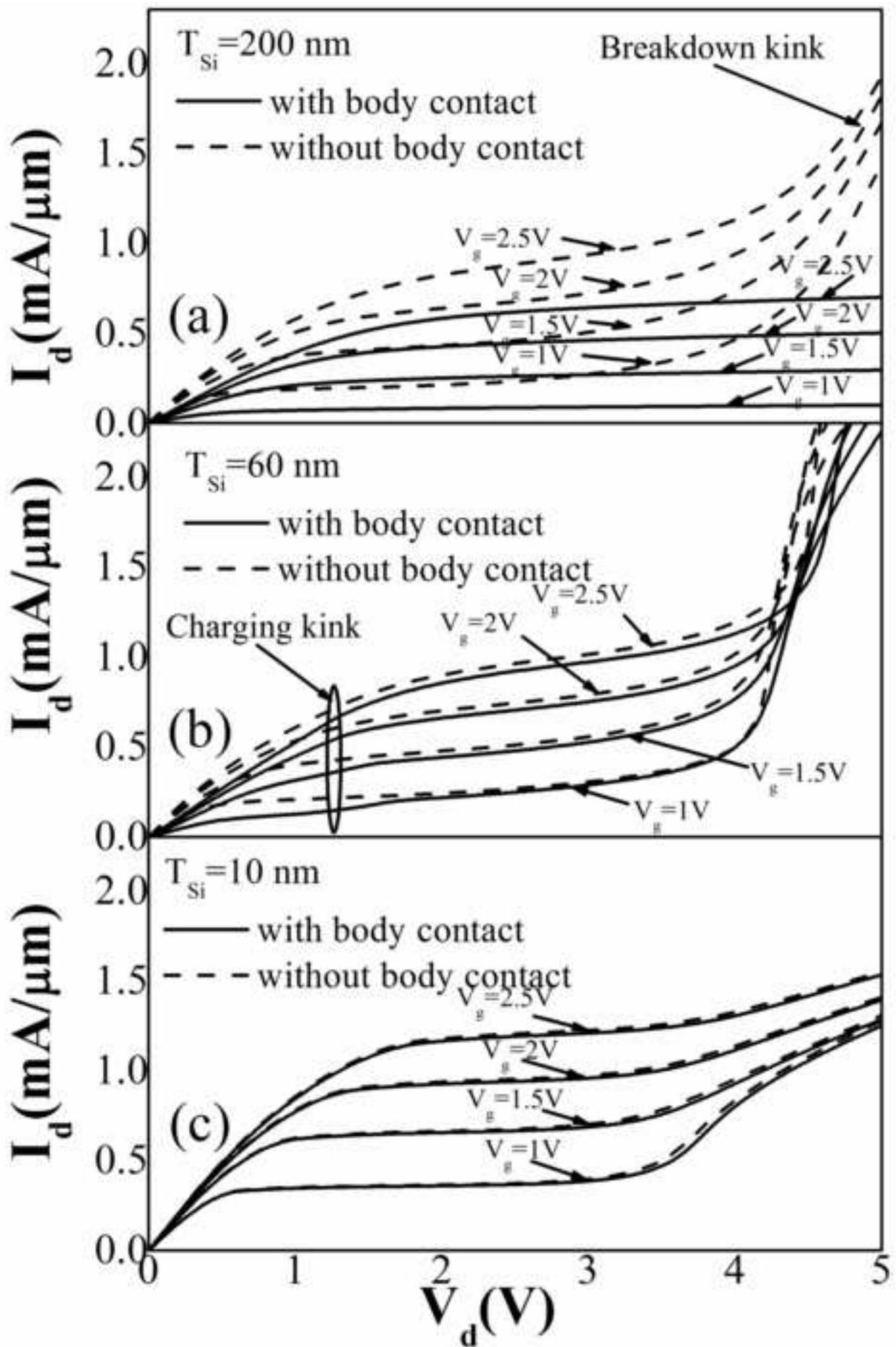


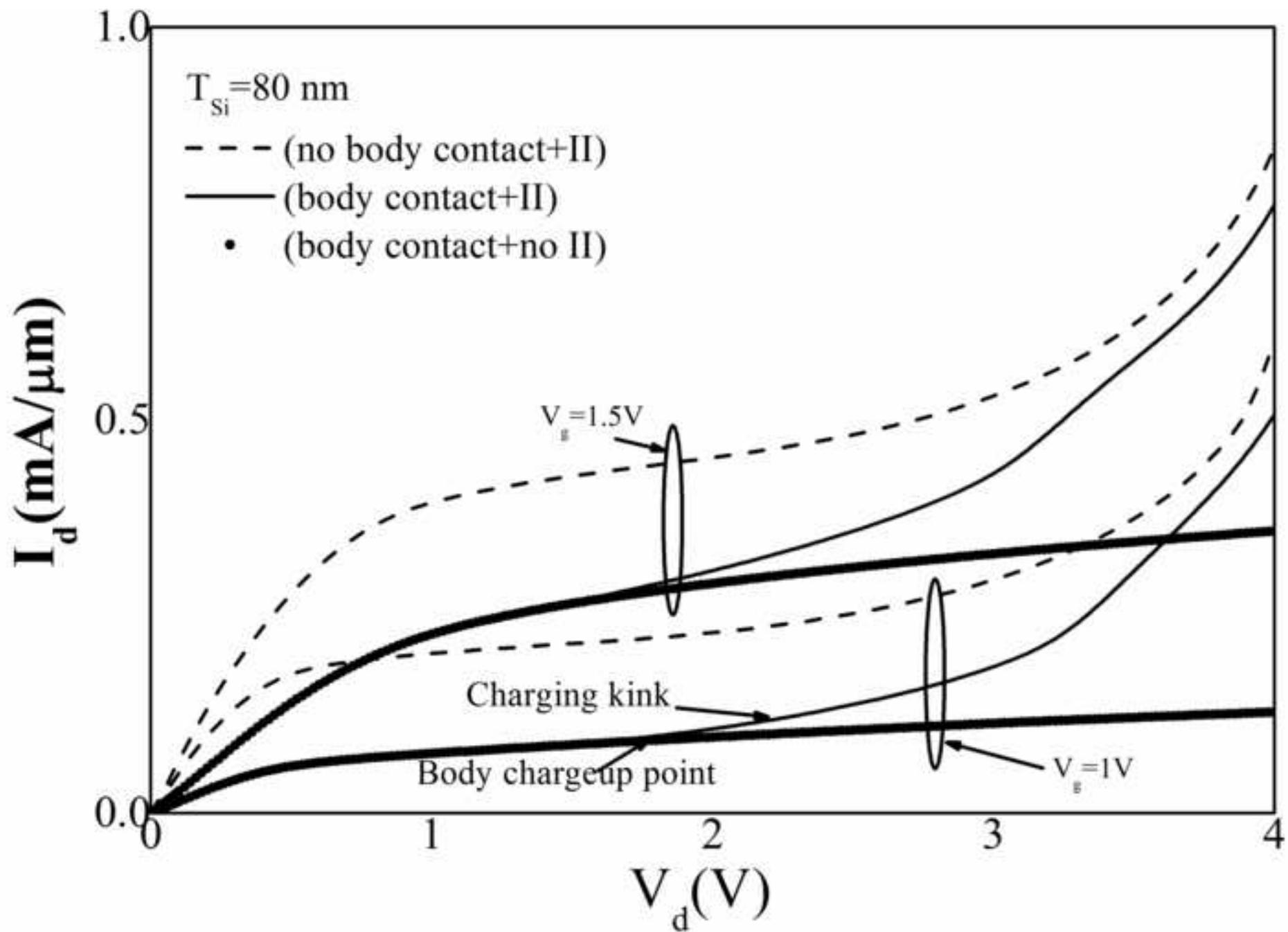
(a)

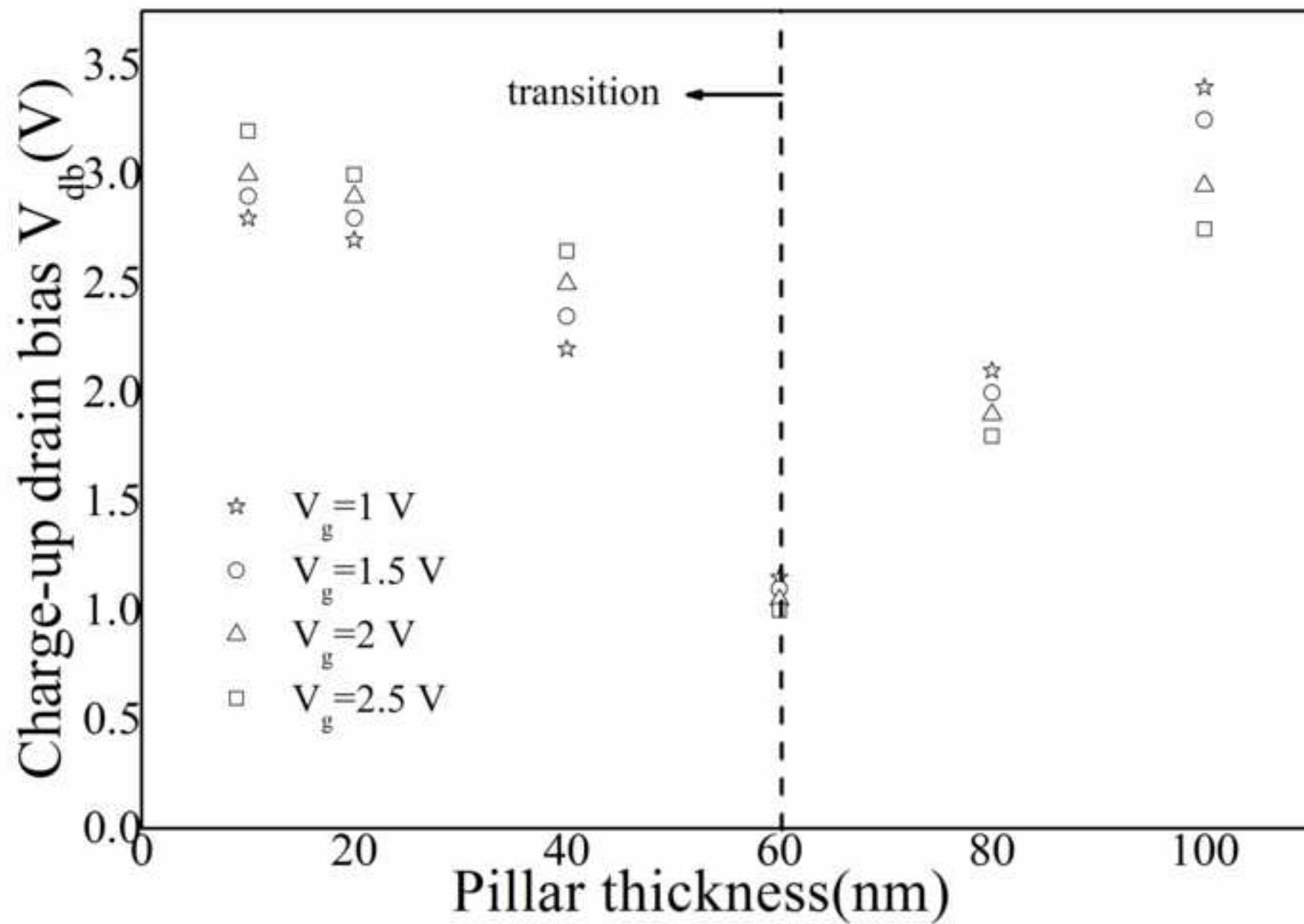


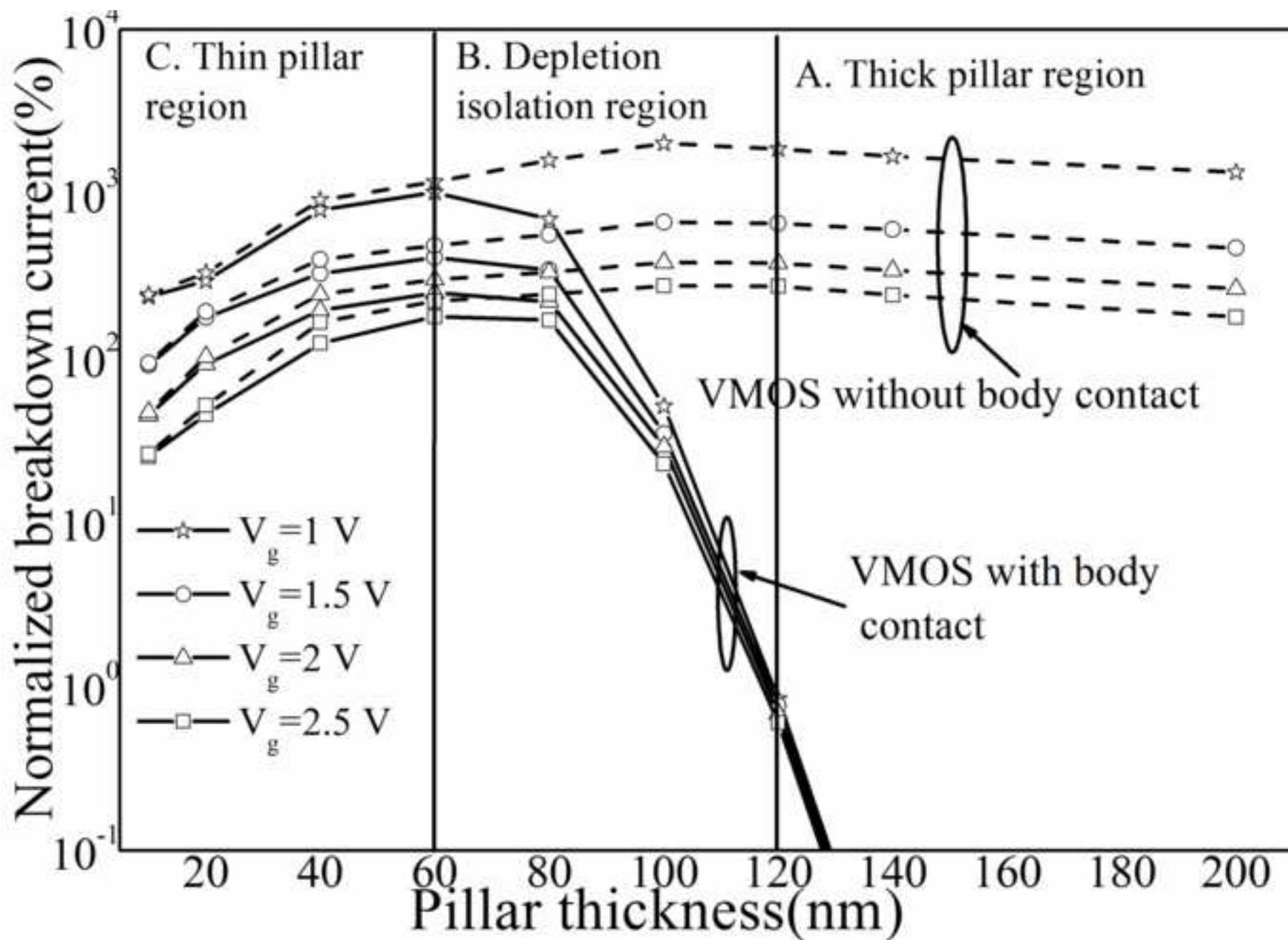
(b)

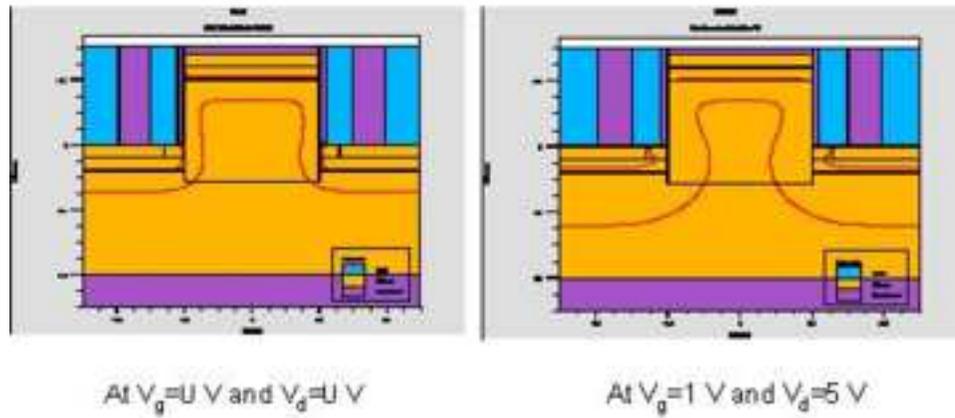
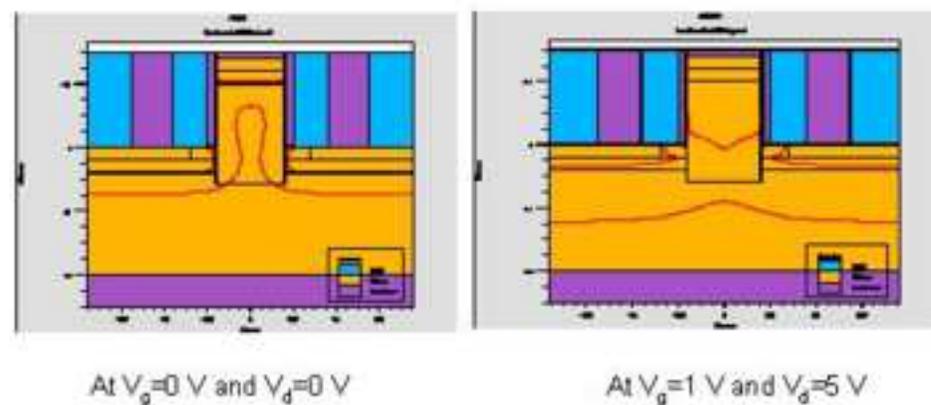
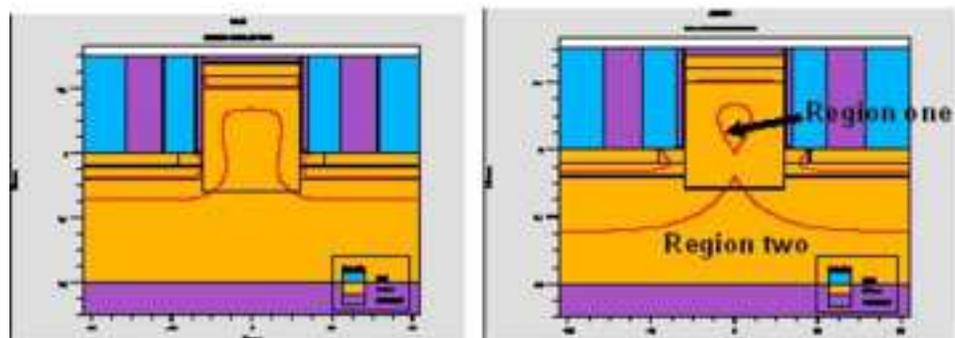
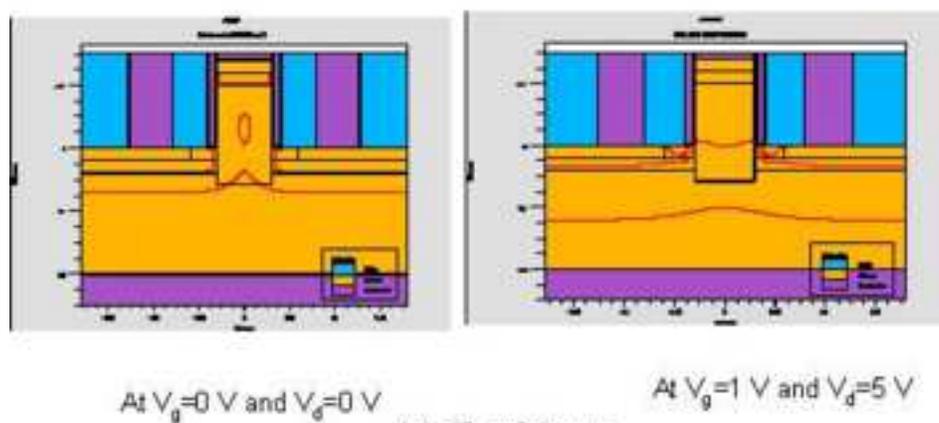


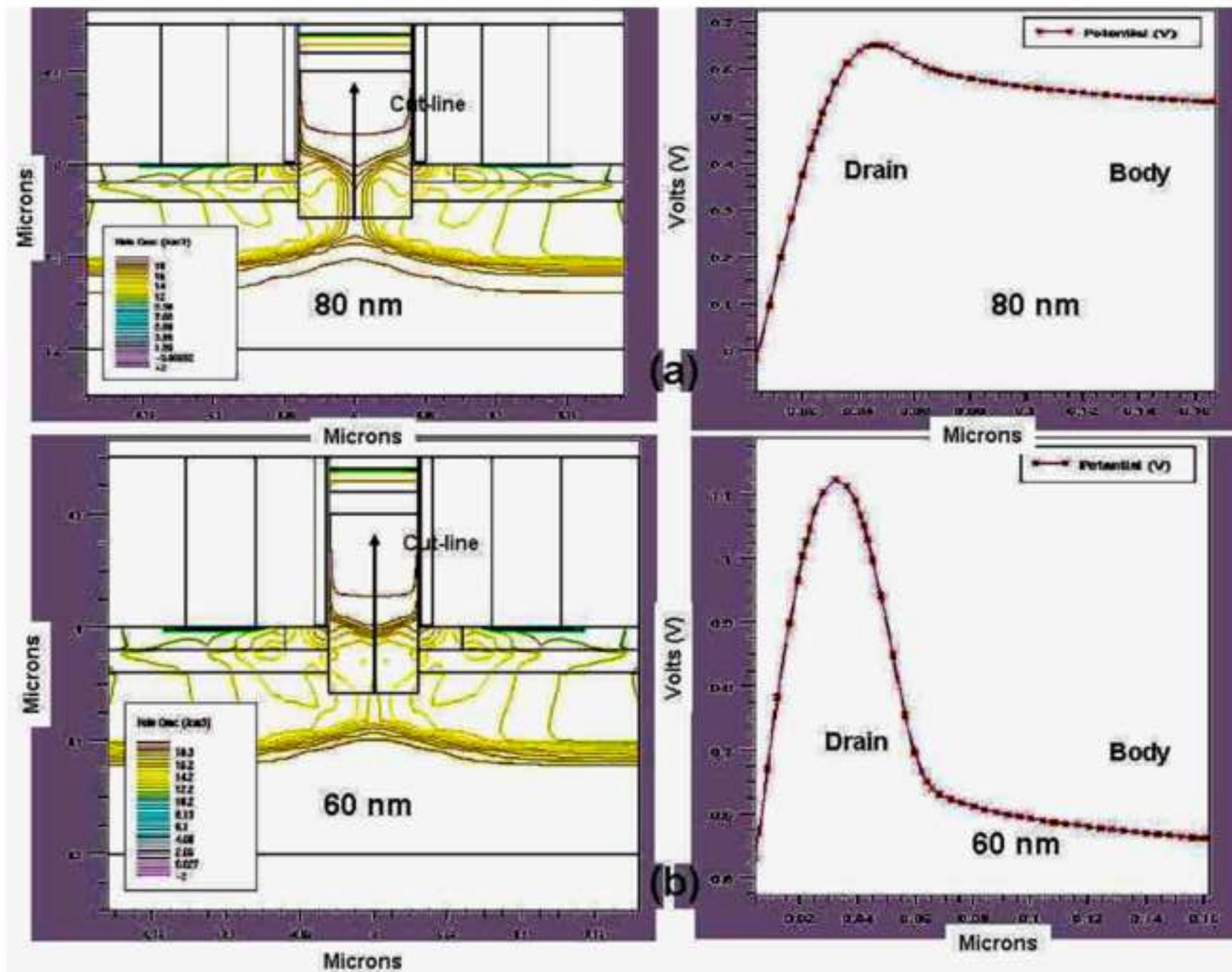


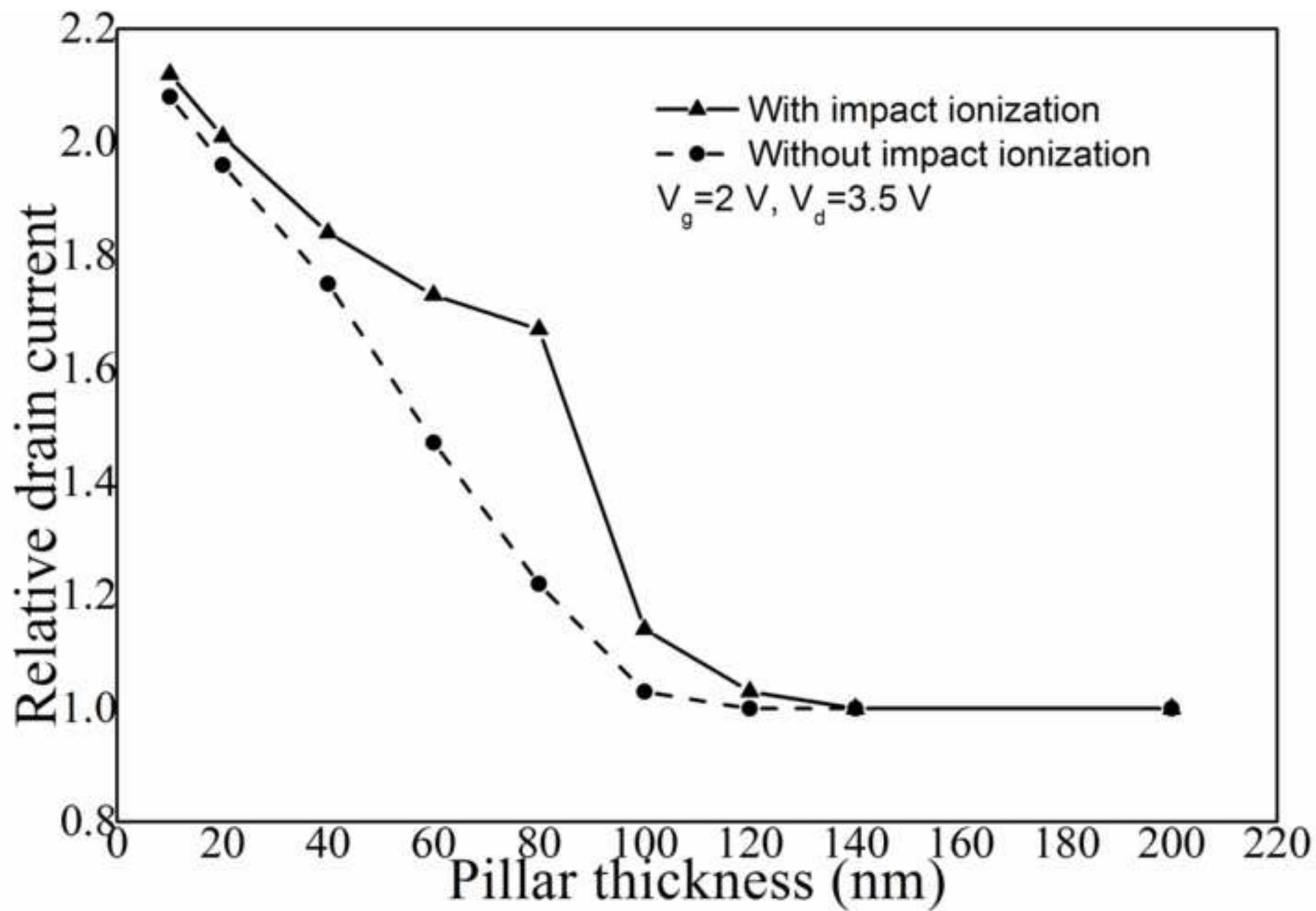


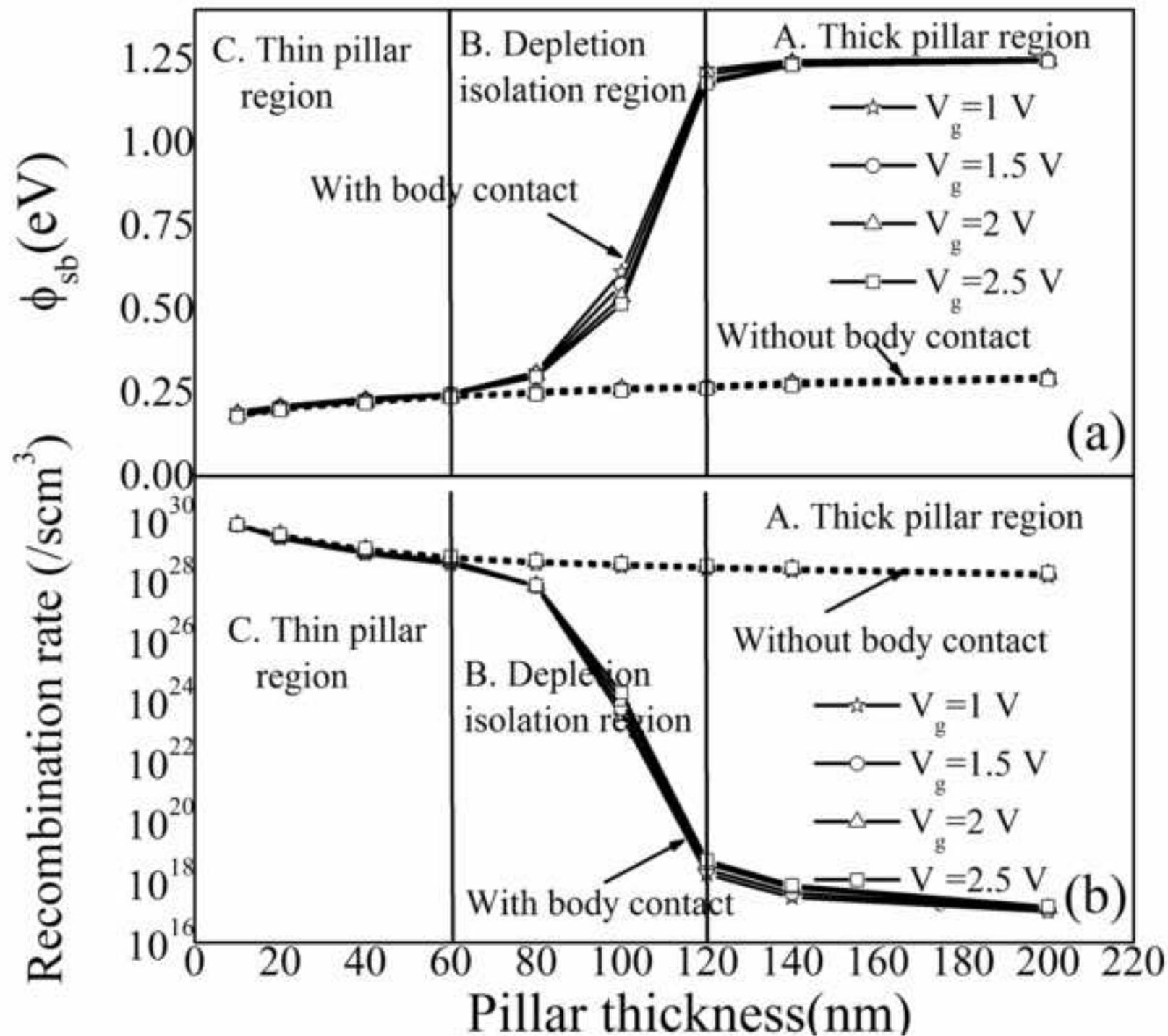


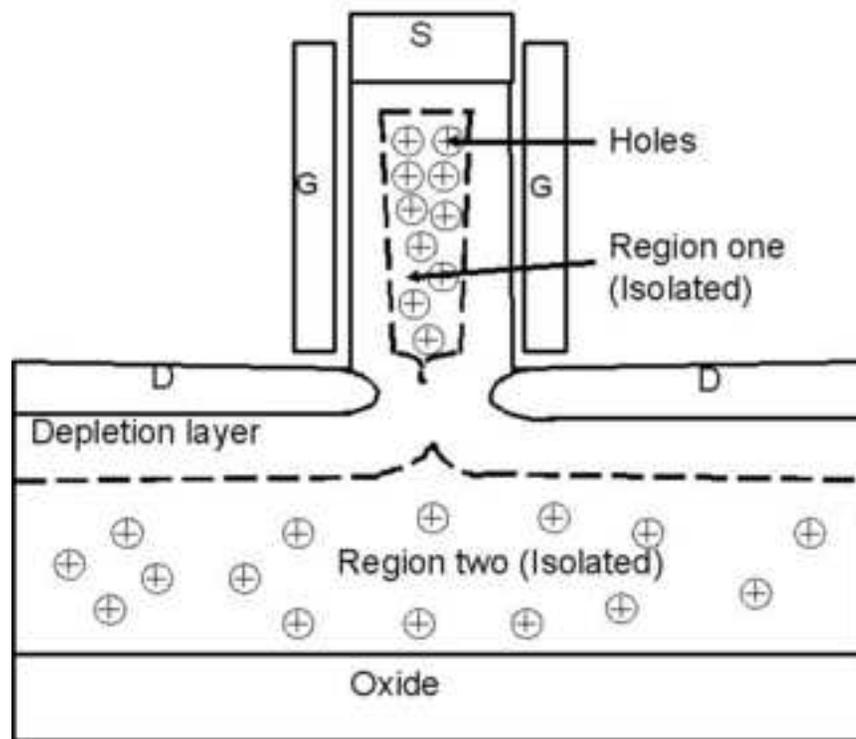


(a) $T_{si}=200$ nm(b) $T_{si}=120$ and 80 nm(c) $T_{si}=60$ nm

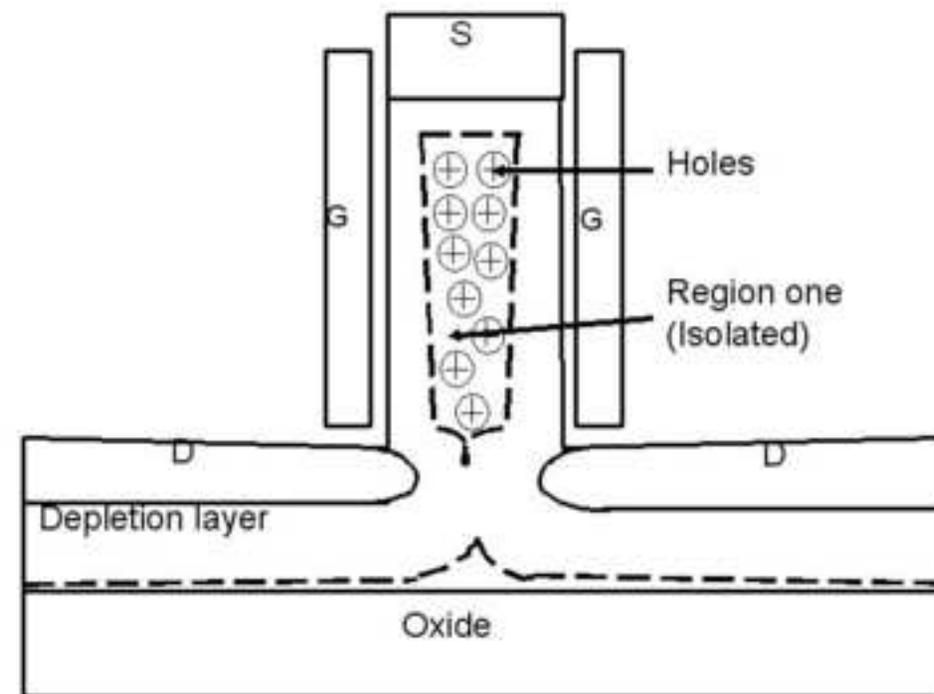








(a) Device with a large body region below the pillar



(b) Device with a small body region below the pillar

