The Impact of BTI Aging on the Reliability of Level Shifters in Nano-scale CMOS Technology

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Abstract. **On-chip level shifters are the interface between parts of an Integrated Circuit (IC) that operate in different voltage levels. For this reason, they are indispensable blocks in Multi-Vdd System-on-Chips (SoCs). In this paper, we present a simulation flow that we propose for a comprehensive evaluation of the effects of Bias Temperature Instability (BTI) aging on the delay and the power consumption of level shifters. We evaluate the standard High-to-Low/Low-to-High level shifters, as well as several recently proposed level-shifter designs, implemented using a 32nm CMOS technology. We demonstrate that the delay degradation due to BTI aging varies for each level shifter design: it is 83.3% on average and it exceeds 200% after 5 years of operation for the standard Low-to-High and the NDLSs level shifters, which is 10x higher than the BTI-induced delay degradation of standard CMOS logic cells. Similarly, we show that the examined designs can suffer from an average 38.2% additional power consumption after 5 years of operation that, however, reaches 180% for the standard level-shifter and exceeds 163% for the NDLSs design. The high susceptibility of these designs to BTI is attributed to their differential signaling structure, combined with the very low supply voltage. Moreover, we show that recently proposed level-up shifter design employing a voltage step-down technique are much more robust to BTI aging degradation. To the best of our knowledge, this is the first work addressing the effects of BTI on the the delay and power consumption of level shifters.**

***Index Terms*—Level shifters, BTI, aging, multi-voltage, multi-power domains, propagation delay, power consumption**.

1. Introduction

Aggressive technology scaling has accelerated the aging of CMOS devices. Particularly, scaling to 32nm technology nodes and below leads to reliability effects that are characterized by a progressive degradation of the performance of devices and system components induced by aging phenomena. This is caused by several mechanisms, namely: Bias Temperature Instability (BTI); Hot Carrier Injection (HCI); and Time-Dependent Dielectric Breakdown (TDDB) [1, 2].

BTI is usually considered as the primary reliability concern in modern technologies [3]. Negative bias temperature instability (NBTI) in pMOS transistors prevails over positive bias temperature instability (PBTI) exhibited by nMOS devices in the latest process technology, especially after the introduction of nitrogen into gate stacks. This technique reduces boron penetration and gate leakage, but leads to worse NBTI degradation [4]. This mechanism is characterized by a positive shift in the absolute value of the threshold voltage of the pMOS device. Such a shift is typically attributed to hole trapping in the dielectric bulk and the breakage of Si-H bonds at the Si-dielectric interface [5]. However, with the use of high-K dielectric stacks, also PBTI exhibited by nMOS transistors is significant and can no longer be neglected. The main BTI aging effect is propagation delay increase over time of various components in System-on-Chips (SoCs). If this performance degradation exceeds circuit time margins, it may lead to system failure, thus reducing its long term reliability [1, 2, 6].

The effects of aging on the performance and reliability of systems on chips (SoCs) have been extensively addressed in the literature [7-12]. However, to the best of our knowledge, BTI aging degradation of level shifters have not been studied yet.

Level shifters are key components in modern multi-V_{dd} SoCs, which are SoCs that are partitioned into multiple voltage islands that may contain parts that operate simultaneously in different operating voltages [13, 14, 15]. In these systems, performance-critical circuits operate at higher supply voltage, while other circuits operate at lower supply voltage in order to reduce power. This voltage variation between different parts imposes a real problem for traditional, static CMOS logic gates. When a logic gate operates at a voltage sufficiently lower than the gate it drives, noise margins and performance degrade, while the driven circuit will consume significantly higher power that could eventually result in unreliable signal switching [15]. For this reason, additional circuitry is necessary to handle the differences in both magnitude and timing that can occur between different voltage islands. Therefore, to enhance the reliability of multi-V_{dd} SoCs, these systems integrate on-chip level shifters to operate as such interface between circuits that have to exchange signal values, while operating at different voltage levels. However, the delay overhead of level has to be considered to properly set design margin timing constraints, because it affect the overall performance of the system. Although the latency of level shifters is usually taken into account at the design planning stage, the BTI-induced delay degradation on level shifters and its contribution on the path delay degradation has not been examined.

In this paper, we present a comprehensive analysis of the effects of BTI aging on delay and power consumption of level shifters. To accomplish this goal, we developed a simulation flow allowing us to simulate all the considered level shifters accounting for the proper BTI-induced V_{th} degradation for each transistor composing the circuit under analysis. We evaluate the standard High-to-Low/ Low-to-High level shifters [16] and the most recently proposed Dual Step Level-up Shifters (DSLSs) [17] and Nanosecond Delay Level-up Shifters (NDLSs) [18], synthesized using a 32nm CMOS technology. The latter have been targeting both low power and high performance ICs applications. We demonstrate that BTI degradation of those devices does not necessarily follow the same pattern as standard logic gates. Indeed, level shifters with differential signaling structure exhibit significantly more degradation in their electrical characteristic compared to standard logic cells. The proposed simulation flow can assist marginal based design approaches of Multi-Vdd SoCs in order to prevent timing-induced failures by accurately considering the BTI-induced delay degradation of level shifters.

The remainder of this paper is organized is as follows. Section 2 overviews the analytical BTI aging model utilized to estimate the threshold voltage degradation caused by BTI aging in CMOS technologies. Section 3 reviews both standard and recently published designs of level shifters. In Section 4, we first describe the proposed simulation flow for aging analysis. Then, we show and discuss the obtained simulation results obtained for the considered level shifters. Conclusions are drawn in Section 5.

2. Bias Temperature Instability Model

BTI consists of Negative Bias Temperature Instability (NBTI) in pMOS transistors and Positive Bias Temperature Instability (PBTI) in nMOS transistors. It causes a threshold voltage shift (ΔV_{th}) in MOS transistors when they are ON (stress phase), at elevated temperatures [17]. The BTI-induced degradation is partially recovered when the MOS transistors are OFF (recovery phase). The reaction diffusion model has been proposed in [19] which allows designers to estimate the drift of V_{th} (ΔV_{th}) induced by BTI aging as a function of technology parameters, operating conditions and time. However, it is not suitable to model long-term BTI degradation. By considering that the drift of V_{th} does not depend on the frequency of input signals, but only on the total amount of the stress time, in [20, 21] a closed form analytical model has been proposed that allows designers to estimate the long-term, worst-case threshold voltage shift ΔV_{th} as a function of applied voltage, stress/recovery time and temperature as follows:

$$\Delta V_{th} = \chi K \sqrt{C_{ox}(V_{dd} - V_{th})} \exp\left(\frac{-E_a}{k_B T_A}\right)(\alpha t)^n, \quad (1)$$

where:

C_{ox}	is the oxide capacitance;
t:	is the operating time;
α:	is the fraction of the operating time during which a MOS transistor is under a stress condition. It has a value
E_a:	is the activation energy ($E_a \cong 0.1$eV);
k_B:	is the Boltzmann constant;
T_A:	is the aging temperature;
χ:	is a coefficient to distinguish between PBTI and NBTI. Particularly, χ equals 0.5 for PBTI, and 1 for NBTI;
n	is the time exponent;
K:	lumps technology specific and environmental parameters.

The time exponent *n* varies with process, voltage and temperature. According to [21], we have selected n=1/6 for our long-term BTI degradation estimation, since it matches with long-time measured data. Parameter *K* has been estimated to be 2.7 $V^{1/2}F^{-1/2}s^{-1/6}$ by fitting the model with the experimental results reported in [4] for a 32nm high-*k* CMOS technology. In Figure 1, we depict the typical trend of ΔV_{th} when a transistor is always under stress DC stress, and for alternate stress/recovery phases (AC stress). The BTI-induced voltage shift ΔV_{th} of a transistor under DC stress can be derived by (1) with α=1, while the worst-case trend over time of V_{th} of a transistor under AC stress (dashed line in Figure 1) is computed by considering the proper α< 1.

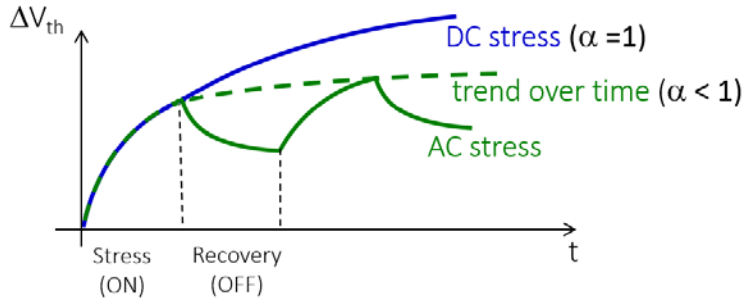

Figure 1. BTI-induced AC and DC stress trend over time.

3. Overview of Level Shifters

Level shifters can be categorised according to their functionality into two types: level down and level up. This section briefly summarises existing architectures in each of these categories.

3.1. Level-Down Shifters

Figure 2 shows a level-down shifter, which can be used to convert high input voltage to the low voltage V_{DDL} [16]. It is composed by 2 inverters which are used as pull-up or pull-down logics. The first inverter reverses IN to V_{SS} or V_{DDL}, and then the OUT port generates V_{DDL} or V_{SS} separately. When the input voltage switches from low to high (i.e., from V_{SS} to V_{DDH}), the output of the first inverter becomes V_{SS}. Therefore, the OUT port will propagate V_{DDL}. Conversely, if the input voltage changes form high to low (from V_{DDH} to V_{SS}), the output of the first inverter will become V_{DDL}. Correspondingly, the OUT port will become V_{SS}. Hereafter,

we refer to this design as standard level down shifter and we denote it by ‘Std HL’.

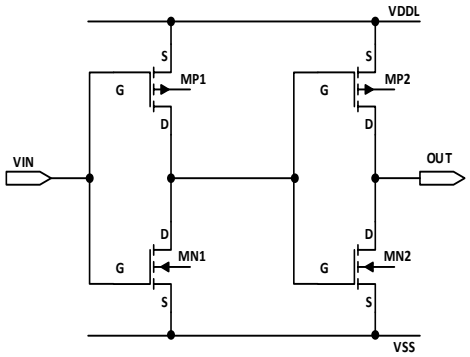

Figure 2 Schematic of standard high-to-low (Std HL) level shifter [16].

3.2. Level-up Shifters

Figure 3 shows the schematic of a standard level-up shifter (‘Std LH’) composed by 10 transistors [16]. It receives as input low supply voltage V_{DDL} and produces as output high supply voltage V_{DDH}. In Figure 3, the combination of MN1, MN2, MP1 and MP2 could sustain the stress from a high power supply. Whereby, MP1 and MP2 are regarded as cross-coupled load. It should be noted here that the increased complexity of the level up shifter compared to level down shifters is mainly due to the differential signalling structure (MP1, MP2, MN1 and MN2) used to level up the signal to a high voltage region.

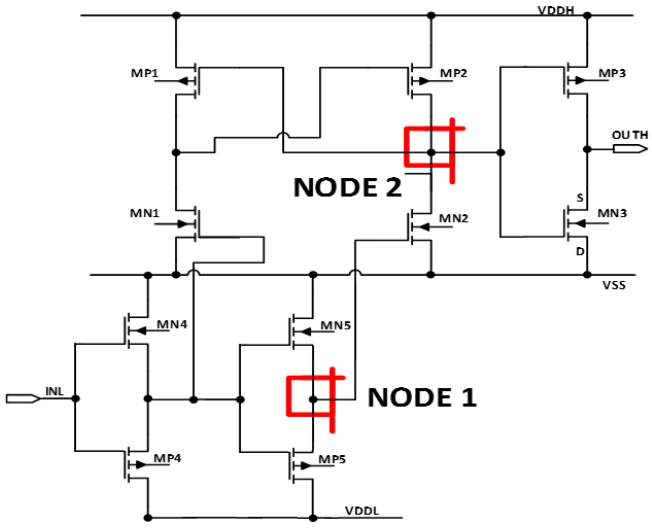

Figure 3 Schematic of standard low-to-high (Std LH) level shifter [16].

A similar structure is also presented for a recently developed level shifter called *nanosecond delay level-up shifter* (NDLS) [17] shown in Figure 4. This design comprises of two parts, the basic level shifter circuit and transmission gate based feedback network (circled with dotted lines), which helps stabilize the output signals against variations of temperature and load conditions.

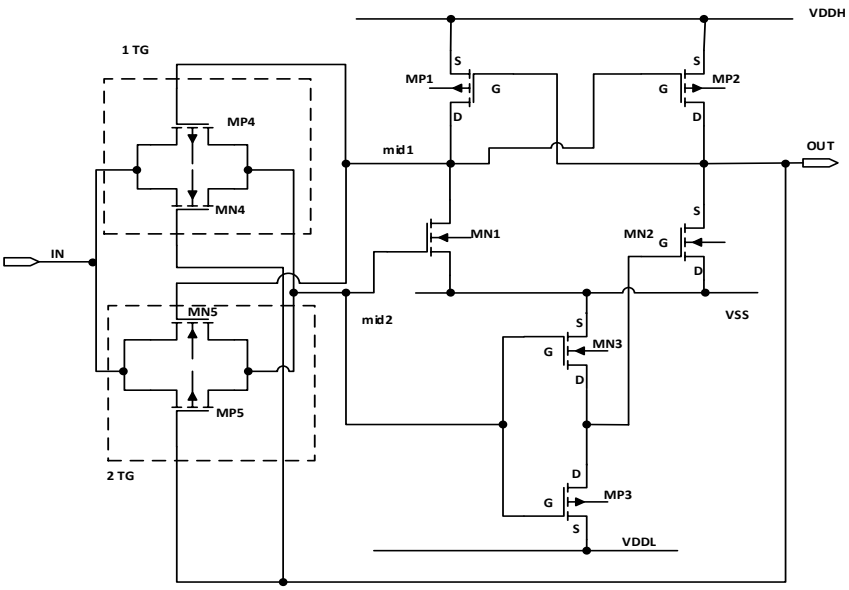

Figure 4 Schematic for low-to-high NDLS design [17].

Another low to high level shifter called *dual step level-up shifter* (DSLS) has been recently proposed in [18] for low power high performance mobile devices. Figure 5 illustrates the schematics for DSLS. It has a stepping level-up structure where each inverter of the buffer structure is supplied by different voltages. The back inverter which consists of MP2 and MN2 is supplied V_{DDH}, whereas the front inverter which consists of MP1 and MN1 is supplied with a voltage lower than V_{DDH}. The transistors MPX is always on and is used to step-down the effective supply voltage applied to MP1 in order to reduce its electric stress. When the voltage at input node INL switches to 0V, *Node 1* is charged through the series of MP1and MPX. Thus V_X becomes V_{DDH}-$R_X I_{DS}$, where R_X is the equivalent resistance of the always ON transistor MPX, thus reducing the electric stress at the source junction of MP1. It is worth noticing that, for the CMOS technology used in this paper, it is $|V_{thP}| > V_{DDH} - V_{DDL}$, so MP1 is OFF when voltage V_{DDL} is applied at its input. This, however, is not a requirement of the design proposed in [18], but a result of the simulation set-up. If the previous condition is not satisfied, a static current may flow from V_{DDH} to ground when $V_{INL}= V_{DDL}$. Therefore, careful sizing of MPX transistor is needed in order to ensure sufficient flow of current to charge *Node 1*, yet controlling the static current when the level shifter is idle [18]. One of the important differences between this design compared and standard schematics of level shifter is that the fact that it does not have a feedback structure.

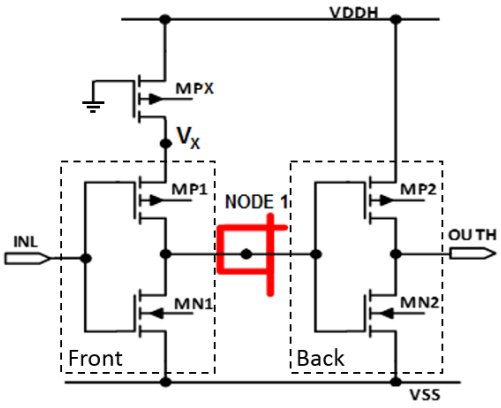

Figure 5 Schematic for low-to-high DSLS design [18].

4. Experimental Setups and Results

4.1. Simulation setup

In order to estimate the impact of BTI aging on level shifters, we have used a predictive 32nm CMOS high-*k*, metal gate technology model from [22]. The BTI-induced V_{th} shift has been estimated based on the model presented in Section II.

In Figure 6, we show the approach that we have followed to embed aging effects in our simulation flow. Following the procedure in [23] given power supply V_{DD} and operating conditions (aging temperature T_A and stress ratio α), the threshold voltage degradation ΔV_{th} is estimated. The ΔV_{th} value obtained for each considered operating time interval is then utilized to customize the SPICE device model and simulate the level-shifters with the proper BTI degradation. Particularly, in this analysis we have considered a duty-cycle of the input signal equal to 50% and T_A = 75°C. The proper stress ration α has been evaluated for each of the transistors composing the considered level shifters. In this regard, it is worth noticing that all transistors composing the standard LH level shifter are under stress for the same amount of time, and for all of them it is α=0.5. The same consideration applies to the NDLS structure. As for the DSLS circuit, it is still α=0.5 for the transistors composing the two inverters, whereas transistor MPX is always under stress (α=1). Furthermore, the proper electric stress has been evaluated for the transistors operating either in the low-voltage domain (V_{DDL}) or in the high voltage one (V_{DDH}). As for the operating time, we have considered 1 month, 6 months, 1 year, 2 years and 5 years. SPICE simulations allow designers to properly estimate the trend over time of both propagation delay and power consumption of level-shifters. These simulation results are then fed to a standard design flow of a multi-V_{dd} SoCs.

We have investigated the following four level shifters: Std HL (Figure 2), Std LH (Figure 3), NDLS (Figure 4) and DSLS (Figure 5). All gates have are minimum sized and symmetric (i.e., pMOS transistors have an aspect ratio properly larger than that of nMOS in the same gate, in order to have the gate symmetric). Transistor MPX in Figure 5 has been sized with a double aspect ratio compared to the other pMOS transistors in the design. The initial delays and power consumptions of the level shifters investigated in this study are shown in Table I. The impact of aging on delay and power will be discussed in the following two subsections.

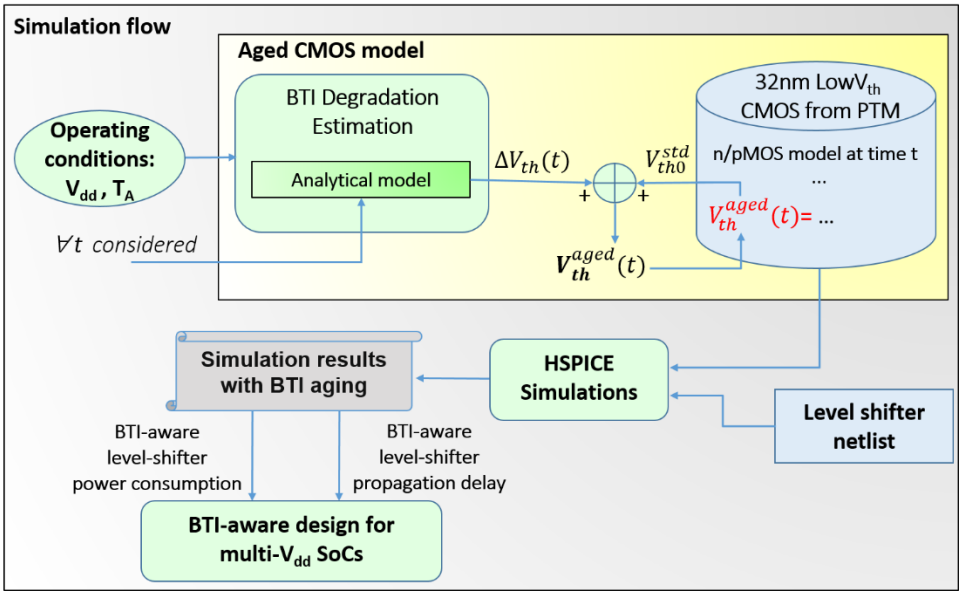

Figure 6 Developed simulation flow.

4.2. Impact of aging on the delay of level shifters

Figure 7 shows the percentage increases in the propagation delay of level shifter designs over the respective delay exhibited at t=0. Propagation delay has been evaluated as $\tau_{prop}(t) = [\tau_{0\to1}(t) + \tau_{1\to0}(t)]/2$, considering the delay from the 50% of the input signal variation to the 50% of the output signal variation. Propagation delay increase for an inverter chain (10-cascaded inverters) is also depicted as term for comparison, and used as a benchmark for assessing the impact of BTI on the propagation delay of standard CMOS logic gates. The results show that the propagation delay increase of both Std HL level shifters (V_{DDH} = 1.2V - V_{DDL}=0.9V and V_{DDH}=1.1V - V_{DDL}= 0.8V) overlaps and reaches 12.5% after 5 years of operation. As expected, this is similar to that of the inverter chain with V_{DD} = 1.2V, which is slightly lower than 16% after 5 year of operations. As for the LH level shifter implemented with the DSLS design, it exhibits a 40% delay increase over 5 years, which is much higher than the delay degradation exhibited by the inverter chain. This can be attributed to the cumulative effect of the two series pMOS transistors in the input stage. However, both the Std LH level shifter design and the NDLS design suffer from a much more significant degradation, with an estimated propagation delay increase over the value exhibited at t=0 of around 200% after 5 years of operation at supply voltages (V_{DDL} = 0.8V, V_{DDH} = 1.1V).

TABLE I Initial Delay and Power Figures of Level Shifters

Level shifter structure	Power		Delay	
	0.8V-1.1V	0.9V-1.2V	0.8V-1.1V	0.9V-1.2V
Std HL	3.59µW	4.52µW	13.9ps	12.1ps
Std LH	8.88µW	5.81µW	178ps	79.1ps
NDLS	9.16µW	5.38µW	201ps	96.4ps
DSLS	7.84µW	15.2µW	92.9ps	80.8ps

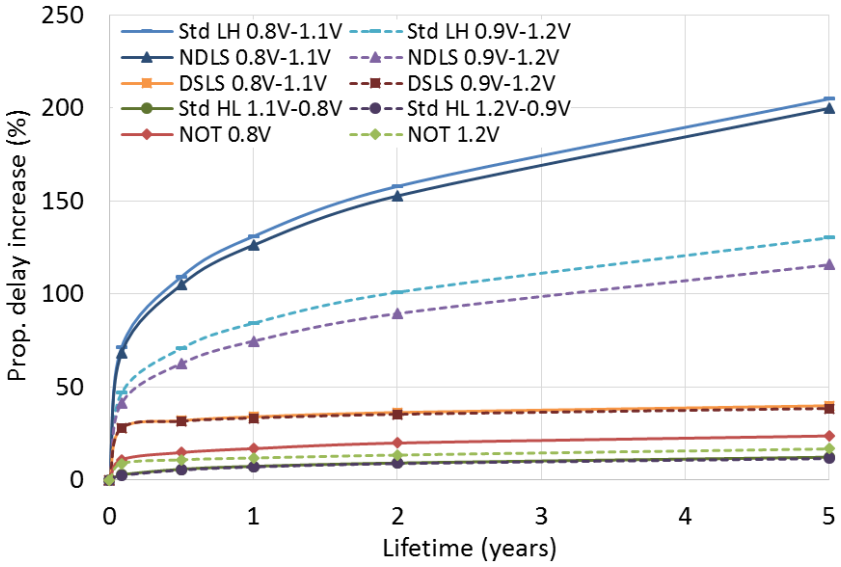

Figure 7 Aging-induced delay increase of level shifters.

Another interesting observation that can be made is that the delays of both standard level-up and the NDLS shifters degrade significantly more when the supply voltage is reduced. For example, the delay increase of the NDLS scheme after 5 years is around

110% when the low and high voltage supplies are V_{DDL}=0.9V and V_{DDH}=1.2V, respectively, and become 200% or higher for the case using V_{DDL}= 0.8V and V_{DDH}=1.1V, respectively, which presents the same voltage swing of 0.3V. This observation appears to contradict the standard model of aging-induced delay degradation as shown in (1), which indicates that the higher the supply voltage the more the increase in the threshold voltage of a transistor and the higher the latency of the device.

It is worth analysing the impact of level-shifter delay degradation on the delay of a whole path. As an example, let us consider a logic path composed by 10 cascaded inverter belonging to a low voltage domain, either supplied by a V_{DDL}= 0.8V or V_{DDL}= 0.9V. In the first case, the logic path is connected to a standard LH level shifter interfacing the voltage domains V_{DDL}= 0.8V and V_{DDH} = 1.1V. Similarly for the second case for the voltage domains V_{DDL}= 0.9V and V_{DDH} =1.2V.

In Figure 8, we report the obtained simulation results. The solid lines depict the normalized propagation delays of the whole paths (NOT chain and level shifter) accounting for the actual degradation of level-shifter delay over time. Instead, the dashed lines show the normalized propagation delay expected by designers assuming that level-shifter delay degrades over time the same as logic path delay. Finally, the dotted line represents a 30% time margin allocated by designers to deal with delay degradation. The normalization factors are the path delays experienced in both cases (V_{DDL}= 0.8V and V_{DDL}= 0. 9V) at *time 0*. As can be seen, while the expected path delays satisfy time margin constraints during the entire operating interval (equal to 5 years), the actual path delays violates this constraint after only a few months of operation. These results point out the need of a proper characterization of level-shifter delay degradation over time, in order not to incur in system malfunctions due to violation of time margin.

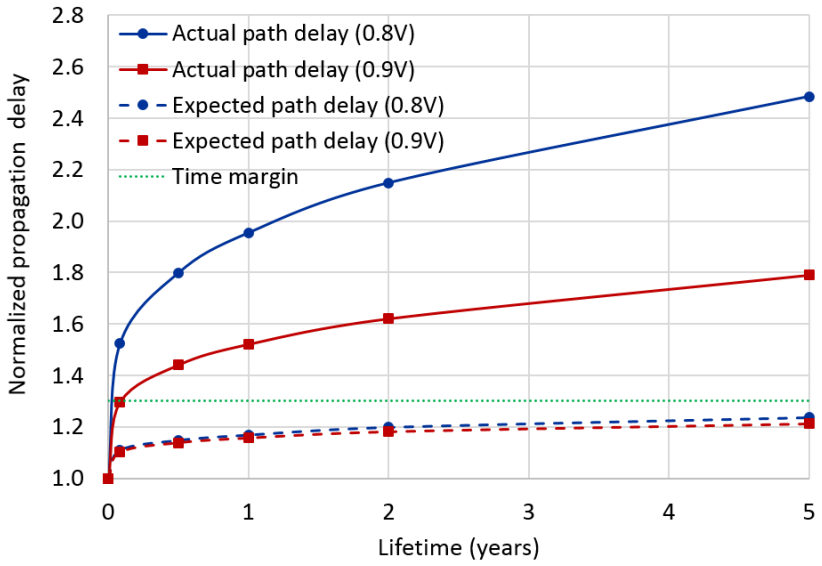

Figure 8 Path delay degradation over time (normalization factors: 258ps for V_{DDL}=0.8V; 149ps for V_{DDL}=0.9V).

To further investigate the level shifter delay trends discussed above, we have carried detailed SPICE level simulations of both standard and DSLS schemes as shown in Figures 9, 10 and 11. Figure 9 shows the SPICE simulations of the input/output and internal node (*Nodes 1* and *2*) of standard level-up shifter (as depicted in Figure 3). The obtained results are very similar to those for the NDLS structure (Node 2 coincides with the output in the NDLS design). The signal waveforms show the degradation of delay over five years of operations. It can be seen that the delay degradation at *Node 2* is significantly higher than at the other internal node (*Node 1*).

A closer inspection shows that *Node 2* is the output of a differential signaling structure (MP1, MP2, MN1 and MN2), therefore the time it takes for the signal to reach a stable level is related to the relative driving strengths of these transistors, which in turn is a function of their respective threshold voltages. BTI aging increases the threshold voltage of all transistors, hence weakens their driving strengths which leads to a longer signal resolution time at this node, and hence more delays. Indeed, when the input INL = 0V (Figure 3), it is V_{NODE1} = 0V, and transistor MN2 is OFF. Moreover, transistor MN1 is ON, thus discharging the gate voltage of transistor MP2 to ground. Therefore, transistor MP2 is ON, thus charging *Node 2* to V_{DDH} = 1.1V and switching OFF transistor MP1. When V_{INL} switches from 0V to V_{DDL}=0.8V, V_{NODE1} switches to V_{DDL} as well after the delay introduced by the two input inverters, thus switching ON transistor MN2. MN1, instead, it is switched OFF after the delay introduced by a single inverter. Transistor MP2, however, it is still ON, and therefore opposes to the discharge of *Node 2*. The time it takes to resolve the electrical conflict between MP2 and MN2 depends on both node capacitance and conductance ratio between the two transistors. Since BTI aging reduces the conductance of both transistors, the resolution time increases considerably over time. On top of that, it should be considered that transistor MN2 is fed with a V_{DDL}=0.8V, which makes it more sensitive to BTI-induced degradation. An analogous consideration holds true for the electrical conflict between MN1 and MP1 when the opposite transition at INL occurs. The absolute value of the resolution time could be reduced by increasing the size of MN2. However, this would not impact the relative increase over the propagation delay exhibited at t=0, as depicted in Figure 7. As a conclusion, the very large propagation delay increase exhibited by the Std LH (NDLS) level shifter is therefore attributed to the increase in the resolution time at *Node 2* (OUT).

Despite the fact that lower supply voltages typically lead to smaller BTI degradation (i.e., lower increases in threshold voltages), in this case the reduction in supply voltage may further degrade the delay as can be seen by comparing the results in Figures 9 and 10. This is because reducing the supply voltage further decreases transistor driving strengths (i.e., at *Node 2*), which leads to longer signal resolution time, hence more delays.

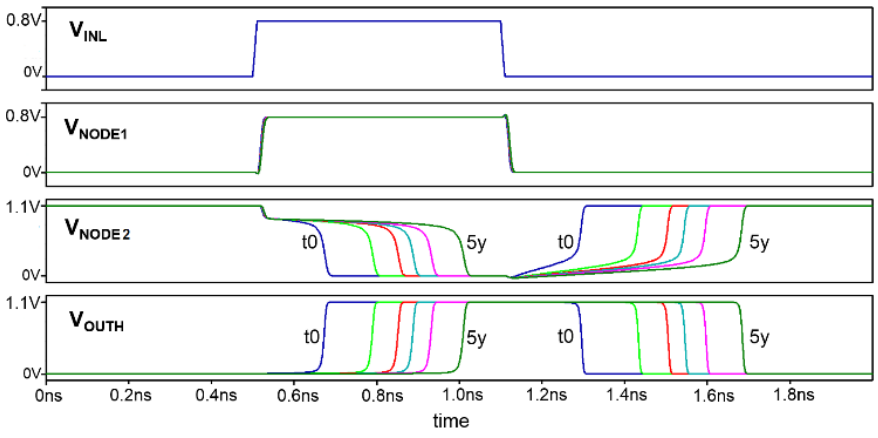

Figure 9 SPICE simulations of delay degradation for standard level up shifter (V_{DDL}= 0.8V; V_{DDH} = 1.1V).

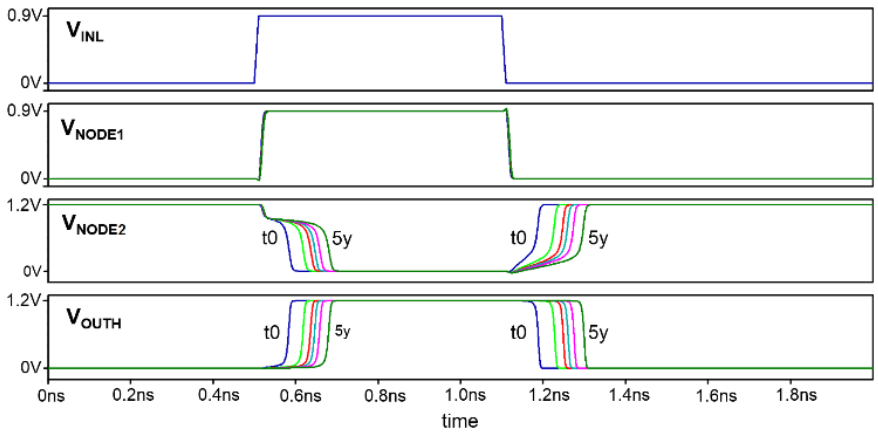

Figure 10 SPICE simulations of delay degradation for standard level up shifter (V_{DDL}= 0.9V; V_{DDH}= 1.2V).

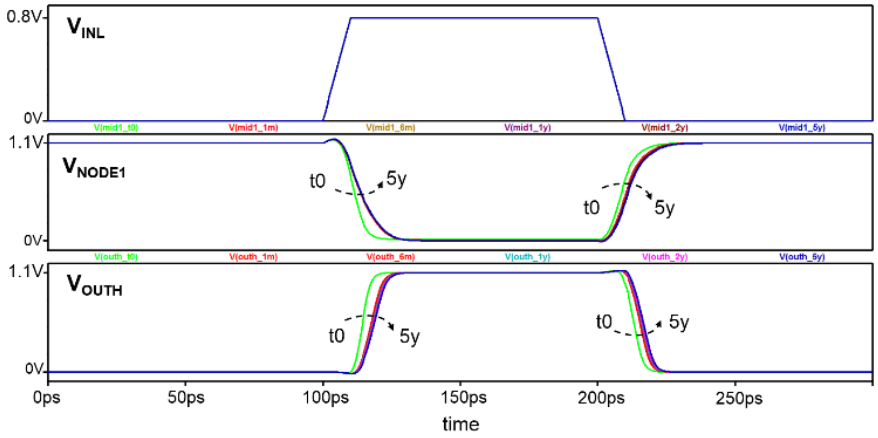

Figure 11 SPICE -level Simulations of Delay Degradation for DSLS (V_{DDL}= 0.8V; V_{DDH}= 1.1V).

SPICE level simulations of the internal node of DSLS schemes shown in Figure 11 indicate that the delay degradation is as expected, and that the largest degradation is experienced within the first month of operation. This confirms that level shifters which do not have the differential signaling structures are more resilient to ageing effects.

4.3. Impact of aging on the power consumption of level shifters

Similar trends have also been observed when evaluating the increase in power consumption due to aging as evident from the results presented in Figure 12. The power consumption figures have been estimated by computing the total average power consumed by each level shifter to perform a low/high followed by high/low signal transition.

The most significant increase in power consumption due to aging is found in both the standard level up and NDLS shifters, which have a differential signaling structure in their respective circuits shown in Figures 3 and 4. These results are consistent with the results we obtained for delay degradation, because the increase in level shifter delay leads increase the time it takes for the signal to make low/high to high/low transition which in turn increases the power consumption due to short-circuit current. To illustrate this point we have carried out detailed SPICE simulations of the current waveforms of both the standard and DSLS level shifters as shown in Figures 13 and 14.

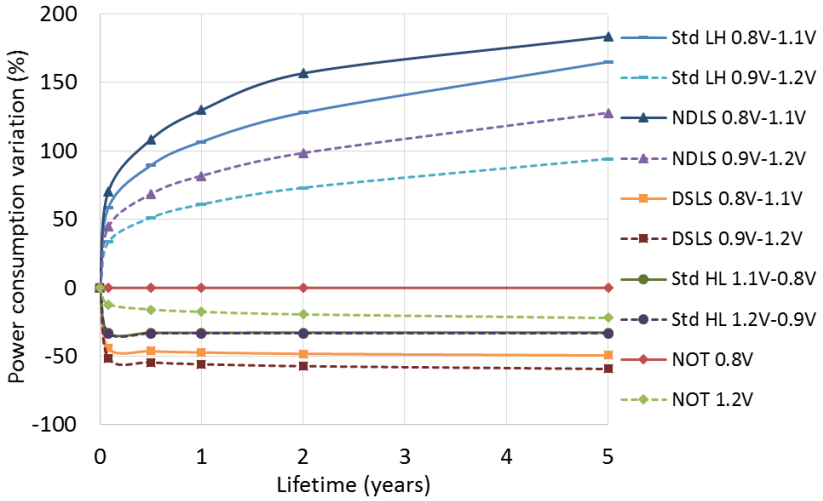

Figure 12 Aging Induced power consumption degradation of level shifters.

Figure 13 depicts the input (V_{INL}) and output (V_{OUTH}), as well as the current provided by both V_{DDL} and V_{DDH} power supplies during the considered transitions. It can be seen that the current (hence the power) provided by V_{DDL}, which supplies the two input inverters, does not change considerably over time. The pulse with of the current provided by V_{DDH}, which supplies the differential signalling structure and the output inverter, increases considerably over time (as expected). Therefore, even if the max value of the current slightly decreases (conductivity of transistors decreases), power consumption is going to increase considerably over time. A similar same behaviour is also observed in the NDLS scheme.

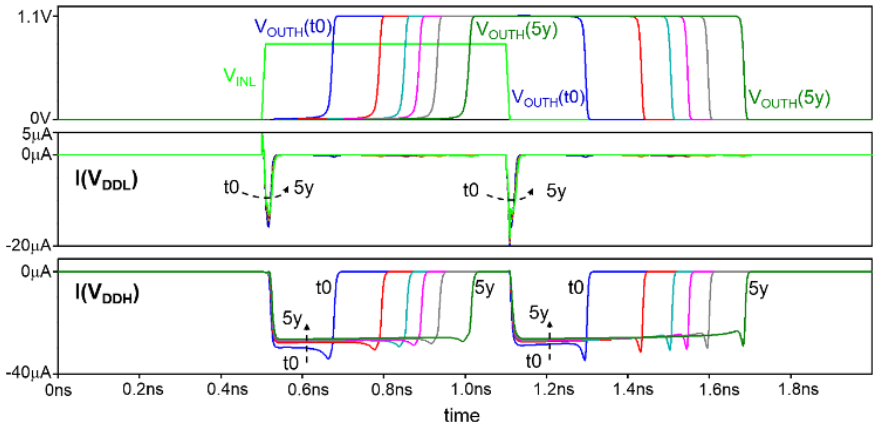

Figure 13 SPICE -level Simulations of Current waveforms for standard level up shifter (V_{DDL}= 0.8V ; V_{DDH}= 1.1V).

The DSLS results presented in Figure 14 show that in this case, the pulse width of the current does not change considerably, whereas the max current reduces over time due to the reduction in the conductivity of the transistors. As a result, the power consumption reduces over time. Note that the static current (when the level shifter does not switch) reduces also over time. Indeed, because the conductivity of the transistors reduces since V_{th} increases, the static current decreases as well [24, 25].

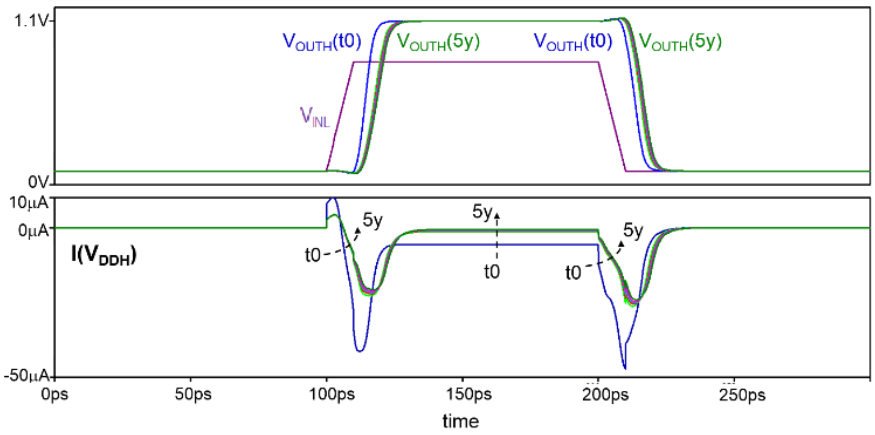

Figure 14 SPICE -level Simulations of current waveforms for DSLS (V_{DDL}= 0.8V ; V_{DDH}= 1.1V).

5. Conclusions

Level shifters are essential blocks of energy efficient systems which use multiple supply voltages. This paper has investigated the effects of BTI aging on level shifters. We have shown that level shifters based on differential signaling exhibit significantly higher BTI-induced power and delay degradation compared to standard logic cells, which reaches 200% and 180%, respectively, in 5 years of operation. This can be attributed to weaker driving strength of their transistor due to BTI aging, and to the consequent increase of signal resolution time at the output of the differential signalling structure typically found in level shifters. This additional delay must be properly taken into account by margin based design approaches in order to avoid aging induced system failures caused by timing violations. Analogously, the high power degradation highlighted by our simulations must be properly considered for energy efficient designs. Alternatively, designers may need to use level shifters which do not have feedback loops such as DSLS, which have been proven to be the most resilient to BTI -induced degradation among the level shifters we have examined.

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