Amorphous SiC resistive memory with embedded Cu nanoparticles

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Abstract

Amorphous SiC with embedded Cu nanoparticles (a-SiC:Cu) was investigated as the insulator layer of Cu/a-SiC:Cu/Au resistive memory. The effect of the Cu embedding on resistive switching characteristics was studied for 20 and 30 vol% Cu. Reduced forming and SET voltages and increased endurance was observed for devices with 30Cu%. At the same time, all key advantageous characteristics of amorphous SiC resistive memory such as ON/OFF ratio of 10^7 and the co-existence of bipolar and unipolar modes were maintained upon Cu embedding. All above suggests that Cu embedding could be considered as a promising method to improve the overall performance of Cu/a-SiC:Cu/Au resistive memories.

Keywords: Resistive memory; Silicon carbide; Cu embedding; Resistive switching

1. Introduction

Non-volatile flash memories face downscaling difficulty in the future due to the intrinsic limitation of both transistors and floating gate [1]. Resistive memory has been identified as one of the most promising alternative memory devices which could replace flash memories in the future. Conductive bridge resistive memory (RM) has simple metal-insulator-metal stacked structure and the write and erase of such RMs are based on the formation (SET) and rupture (RESET) of conductive filaments in the insulator layer, induced by applying a programming voltage across the active and counter metal electrodes. Formation and rupture of the conductive filament switches the RM between high resistance state (HRS) and low resistance state (LRS). The resistance of the device in the LRS and HRS are often noted as R_{ON} and R_{OFF}, respectively. Typical conductive filaments such as Cu filament have a size below 10nm, which indicates great scaling potential for RMs use Cu filament [2-5].

Two basic switching modes are commonly observed in different RMs: bipolar and unipolar. Bipolar refer to RMs which use SET and RESET with opposite voltage polarities and the rupture of the filament is predominantly drift-based. Unipolar refers to RMs which use SET and RESET with the same voltage polarity and the rupture of the filament is predominantly diffusion-based. The majority of RMs presents only one of these two resistive switching modes. Bipolar RMs are more likely to have lower operation power [6] compare with unipolar RMs, while unipolar RMs are more likely to have more simplified peripheral circuit [7] as only one voltage polarity is required. The co-existence of bipolar and unipolar modes hence could be considered as an advantage as they can potentially expand application scopes of RMs [8].

RMs can be divided into those that where the conduction mechanism involves the formation of a conductive metal filament and those where oxygen vacancies are playing the key role. Many different types of solid state electrolytes and insulators have shown to be suitable materials for RMs as described in the following reviews [9, 10]. In particular, Cu-based dielectric RMs using Cu_xO have shown reversible resistive switch behaviour and long data retention [11]. However, the reported ON/OFF ratio (R_{OFF}/R_{ON}), are mostly in 10^2 to 10^4 range. Large ON/OFF ratio is desirable for future high density memory device applications [12] because it would make the periphery circuit very easy to distinguish the storage information (“1” or “0”) [13] as well as enable multilevel storage to increase the data density efficiency [14]. Recently SiC has been shown to function as an insulator layer for resistive memory [15-18]. Amorphous SiC (a-SiC) has been considered a promising material which could be exploited for future CMOS interconnection dielectric and Cu diffusion barrier [19]. Potential integration of RMs in the back-end-of-line layer e.g. a-SiC on top of CMOS logic circuits has been considered desirable to achieve improved system performance [18]. These make a-SiC an attractive material as RM dielectric for embedded applications. We have shown that amorphous SiC (a-SiC) based RMs can be made to have ultra-high ON/OFF ratio up to 10^9 [20], co-existence of bipolar and unipolar modes, as well as high stability [6]. The a-SiC based RMs also show promising performance under high radiation conditions [4]. Despite the promising results thus far,

it was also observed that relatively high forming voltage (V_{FORM}), typically 4 to 5 V, were needed to switch a pristine a-SiC based RM into LRS [21]. This is likely attributable to the low Cu drift rate in SiC which requires high electric field to form the Cu filament in the a-SiC matrix. Thus, there is a trade-off between high state stability and V_{FORM}. In order to achieve reduced V_{FORM} while still maintain the high ON/OFF ratio and stability for which we need the a-SiC device layer to remain insulating, in this study, we embedded Cu nanoparticles in an amorphous SiC matrix (a-SiC:Cu) as the insulator layers to form Cu/a-SiC:Cu/Au RMs. Our previous study has shown the resistivity of a-SiC:Cu films decreased with the increase of Cu vol% and started to present metallic behaviour when Cu vol% was higher than 30% [22]. To ensure the large R_{OFF} and thus high ON/OFF ratio, Cu vol% up to 30% was used as the middle device layer in Cu/a-SiC:Cu/Au RMs. The effect of Cu embedding on forming and SET voltages, resistive switching modes, conduction mechanism in LRS and HRS, and endurance over repeated switching were studied.

2. Experiment

Cu nanoparticles embedded amorphous SiC(a-SiC:Cu) films were deposited using co-sputtering from SiC (99.5%) and Cu (99.99%) targets in a Kurt J. Lesker sputter system. Different Cu vol% (Cu%) in the deposited films was achieved by adjusting the target powers as described in [22]. Microstructure of the a-SiC:Cu films was analysed using X-ray diffraction (XRD) and Transmission electron microscope (TEM). Cu/a-SiC:Cu/Au RMs with 0%, and 20%, and 30% Cu% in a-SiC:Cu, were fabricated on Si wafers covered with a 1µm thick thermal SiO_2 layer. 300nm Au was deposited by magnetron sputtering followed by a reactively sputtered SiO_2 layer of 250nm in thickness. Photolithography and reactive ion etching were then conducted to pattern and expose the active device areas. Subsequently, 40 nm thick a-SiC:Cu and 300 nm thick Cu layers were deposited without breaking the sputtering chamber vacuum on the patterned substrates. Finally, a lift-off process was used to realise the device structure. Scanning electron microscope (SEM) was used to observe the cross-section of the fabricated device. Current-Voltage (I-V) measurements of the Cu/a-SiC:Cu/Au RMs were conducted by grounding the Au electrode and applying a voltage to the Cu electrode, using a Keithley 4200SCS parameter analyser. 100µA current compliance was used for forming and SET. No current compliance was used for RESET. The 0.02V/0.5Sec ramping rate was used in DC measurements. Pulsed SET and RESET were used in repeated switching. Resistance of the states was readout at 0.1V.

3. Results and discussion

Fig.1a shows XRD pattern of a-SiC:Cu films with 0%, 20%, and 30% Cu vol% (Cu%), which were later used as the insulator layer in Cu/a-SiC:Cu/Au RMs. The typical SiC (111) peak at 35.7° [23] could not be observed, suggesting amorphous status of the sputtered SiC. The characteristic Cu (111) XRD peak at 43.6° [24] is clearly evident in the 20% and 30% samples, suggesting crystalline status of embedded Cu. TEM image of a-SiC:Cu in Fig.1b shows well distributed Cu particles in the material. The size of these particles is approximately 2-5 nm which roughly agree with the results from XRD analysis we reported previously [22]. Selected area electron diffraction (SAED) image of a-SiC:Cu is shown in the inset of Fig.1b. The four indicated fringe patterns have radii in the ratio of $\sqrt{3}:\sqrt{4}:\sqrt{8}:\sqrt{11}$, which corresponds to the (111), (200), (220), and (311) planes of crystalline Cu with face-centered cubic (FCC) structure [25].

Fig.2a shows the cross-sectional SEM image of a typical Cu/a-SiC:Cu/Au RM, and the 40nm thick insulator layer is clearly observed. Fig.2b shows the forming I-V of multiple pristine Cu/a-SiC:Cu/Au RMs with 0%, 20% and 30% Cu%, respectively. In the pristine state, all the Cu/a-SiC:Cu/Au RMs with different Cu% show very high resistance, typically larger than 3GOhm at 0.1V. When the voltage applied on the device increases to V_{FORM}, an abrupt increase of current towards the 100µA current compliance could be observed and is attributable to the formation of Cu conductive filament. Average values of V_{FORM} of Cu/a-SiC:Cu/Au RMs with 0%, 20% and 30% Cu% are 9.4V, 6.8V, and 2.8V, respectively. It is likely that the reduction of V_{FORM} is due to the existing of embedded Cu nanoparticles in the a-SiC:Cu layers. It has been reported that the existence of metal nanoparticles in an insulator film increases the electric field adjacent to the metal nanoparticles [26, 27]. The reduction of V_{FORM} is hence attributable to the increase of electric field in the a-SiC:Cu layer, which accelerates the drift of Cu inside a-SiC:Cu from Cu electrode towards Au electrode.

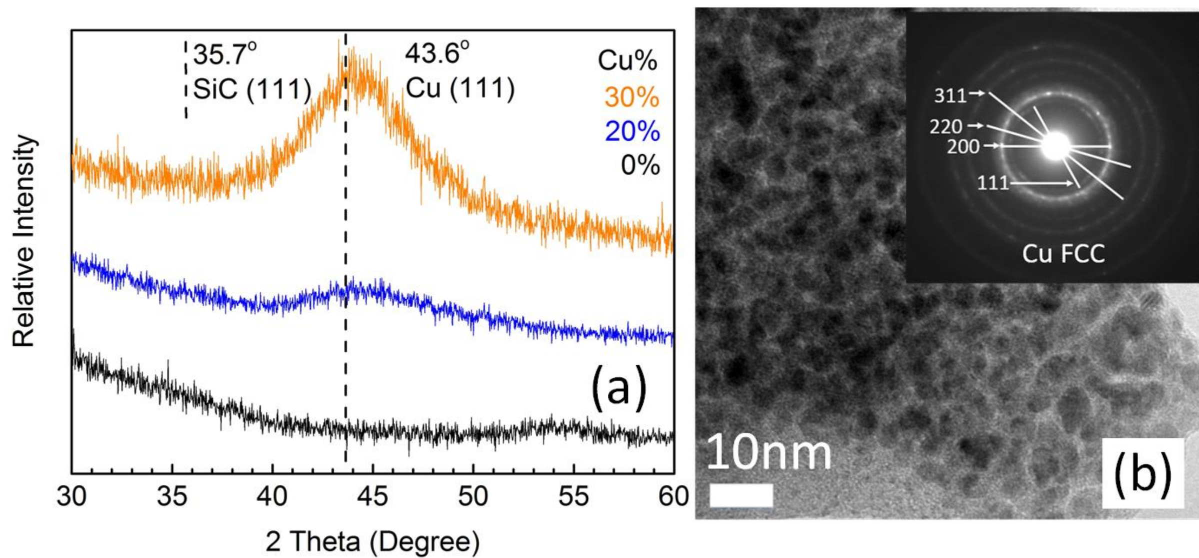

Fig.1. (a) XRD pattern of a-SiC:Cu films with different Cu%. (b) TEM image and SAED image in the inset of a-SiC:Cu.

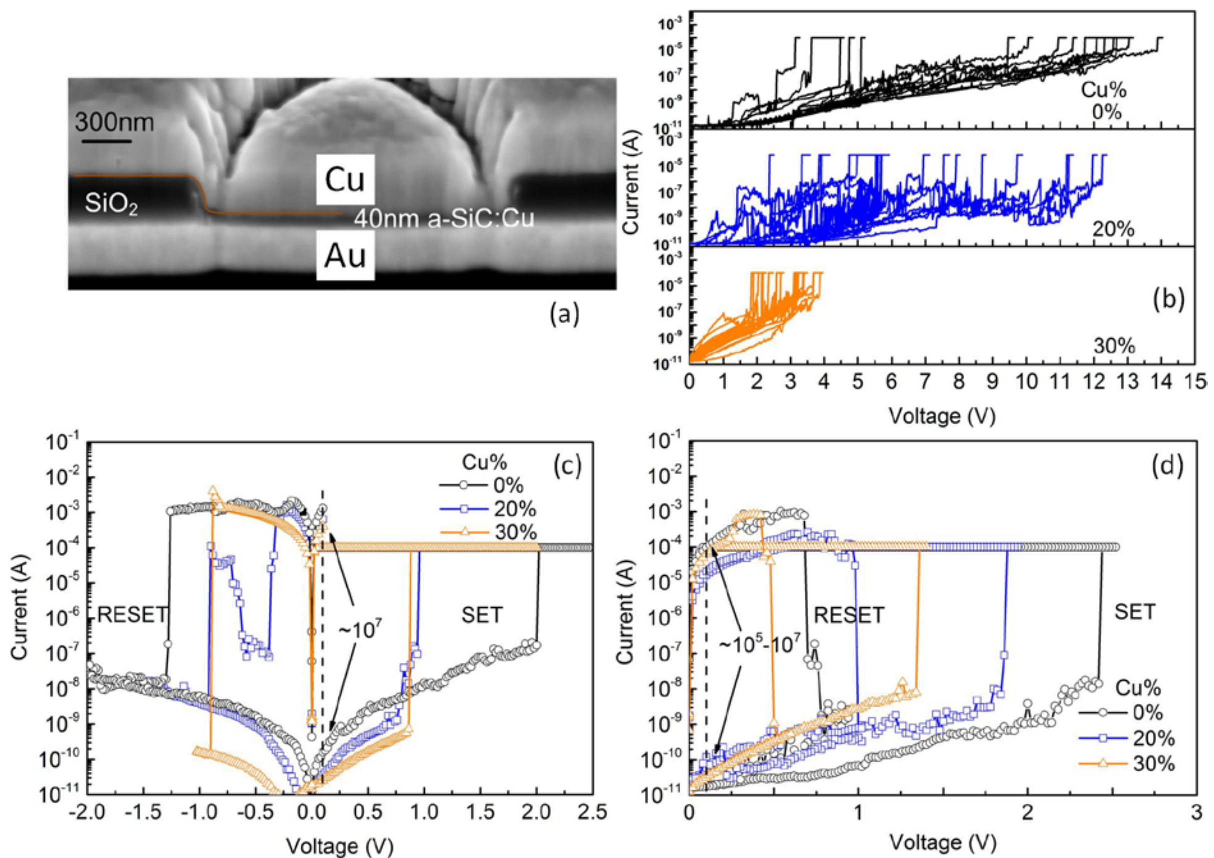

Fig.2. (a) Cross-section SEM image of a Cu/a-SiC:Cu/Au RM. (b) Forming I-V of multiple Cu/a-SiC:Cu/Au RMs with 0%, 20%, and 30% Cu%. I-V of switching cycles. (c) Bipolar and (d) unipolar modes of Cu/a-SiC:Cu/Au RMs with different Cu%.

Fig.2c and Fig.2d show typical I-V characteristics of the stable switching cycles of Cu/s-SiC:Cu/Au RMs with 50×50 μm^2 device area and different Cu% in bipolar and unipolar modes, respectively. The co-existence of bipolar and unipolar modes, which is a desired feature [8], could be observed for all RMs with different Cu% and thus is not affected by Cu embedding. SET voltage (V_{SET}), RESET voltage (V_{RESET}), R_{ON} and R_{OFF} measured at 0.1V, and ON/OFF ratio of the devices are summarised in Table.1. V_{SET} of Cu/a-SiC:Cu/Au RMs shows a reduction with increased Cu% in both bipolar and unipolar modes, which is attributable to the existence of embedded Cu

nanoparticles. Potential mechanism of V_{SET} reduction with increased Cu% are discussed in the following section. Furthermore, Cu/a-SiC:Cu/Au RMs with different Cu% show comparable ON/OFF ratios of approximately 10^7 in bipolar and 10^5 to 10^7 in unipolar modes. These ratios are higher than the typical ratio of $<10^4$ for the majority of resistive memories not based on SiC, suggesting great application potential for Cu embedded SiC.

Table.1. V_{SET}, V_{RESET}, R_{ON}, R_{OFF}, and ON/OFF ratio of Cu/a-SiC:Cu/Au RMs with different Cu%.

RM with different Cu%	V_{SET} (V)	V_{RESET} (V)	R_{ON} (Ohm)	R_{OFF} (10^9 Ohm)	ON/OFF ratio (10^6)
Bipolar mode					
0%	2	-1.26	76	0.6	8.2
20%	0.94	-0.9	157	2.8	18
30%	0.86	-0.88	249	3.9	16
Unipolar mode					
0%	2.42	0.68	1030	5.2	5
20%	1.86	0.98	4910	1.7	0.4
30%	1.34	0.48	1600	2.9	1.8

I-V analysis has been widely used as a method to decipher the conduction and switching mechanisms of RMs [6, 8]. Fig.3a and 3b show the LRS current conduction behaviour of Cu/a-SiC:Cu/Au RMs with different Cu% in bipolar and unipolar modes, respectively. The slope of linear fits of LRS in log(I)-log(V) plot are all close to 1, which indicates Ohmic conduction. We believe the Ohmic conduction in our devices with $+V_{SET}$ is attributable to the formation of Cu conductive filament [6]. The formation process of the Cu conductive filament could be described with the well-known electrochemical metallisation model [10]. In this model, when a positive voltage is applied on the Cu electrode, Cu atoms would be oxidised into Cu cations and drift toward the negatively charged Au electrode. Due to the low Cu drift rate, Cu cations would likely start to reduce before they reach the Au electrode and form Cu conductive filament which gradually grows towards the Au electrode. In Cu/a-SiC:Cu/Au RMs, the growth of Cu conductive filament might also pass a few position in where embedded Cu particles are located. Hence, for RM with embedded Cu particles, the Cu atoms required to form the Cu conductive filament may be reduced as in comparison with RM with 0% Cu, contributing to the reduction of V_{FORM} (Fig.2b) and V_{SET} (Table.1).

Fig.3c and 3d show the HRS I-V of Cu/a-SiC:Cu/Au RMs with different Cu% in bipolar and unipolar modes, respectively. Linear fits in Ln(I)-√V plots of Cu/a-SiC:Cu/Au with all different Cu% suggest Schottky emission conduction following [28]:

$$I = AA^{*}T^{2}\exp(\frac{-q\Phi_B}{kT} + \frac{q}{kT}\sqrt{\frac{qE}{4\pi\varepsilon}}) \quad (1)$$

where A is the device area, is A^{*} Richardson's constant, Φ_B is Schottky barrier height, E is the electrical field, q is the electronic charge, k is the Boltzmann's constant, ε is permittivity of the insulator layer, and T is absolute temperature. The existence of Schottky contact is likely a contributing factor to the up to 5Gohm R_{OFF}, and consequently high ON/OFF ratio of up to 10^7 of our Cu/a-SiC:Cu/Au RMs [6]. The results suggest that Cu embedding would not change the existence of Schottky emission conduction mechanism in HRS.

To test the effect of Cu embedding on the endurance of Cu/a-SiC:Cu/Au RMs, pulsed SET and RESET were used to switch the RMs repeatedly. Resistance after each switch was read out at 0.1V to avoid large disturbance on the resistance state. Fig.4 show multiple cycles of Cu/a-SiC:Cu/Au RMs with 0%, 20%, and 30% Cu%, respectively. In Fig.4a-4c, Cu/a-SiC:Cu/Au RM with 30Cu% shows most stable switching performance and the longest endurance. Its 10^6 ON/OFF ratio is only slightly reduced with respect to devices with less Cu embedded. Despite limited number of switching test cycles, our results suggest that Cu/a-SiC:Cu/Au RMs could be used in applications where different trade-offs between ON/OFF ratio, stability and endurance are required than in the consumer market, such as in harsh environment application [4].

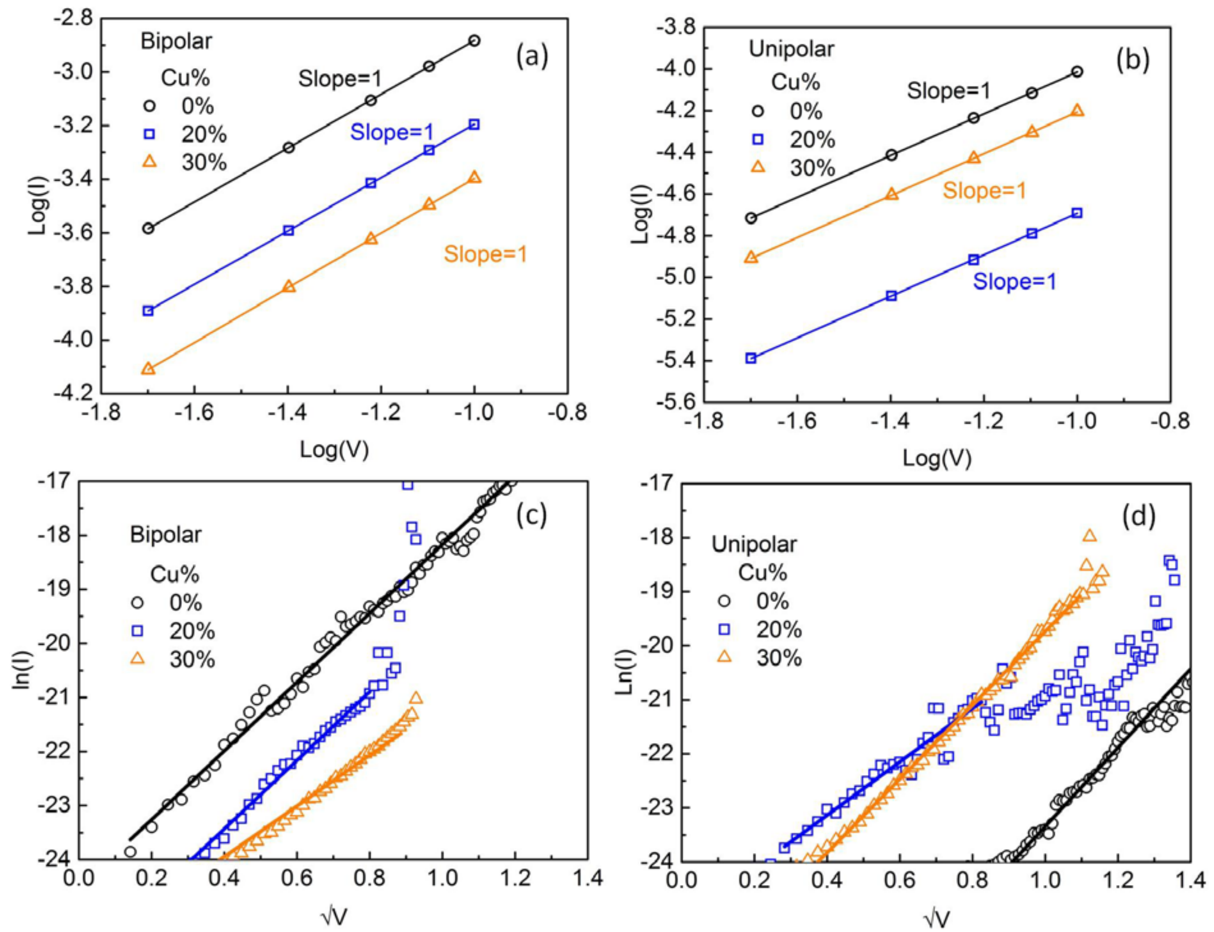

Fig.3. Current-Voltage characteristics of LRS and HRS of Cu/a-SiC:Cu/Au resistive memory for different modes (a) LRS bipolar, (b) LRS unipolar, (c), HRS bipolar, and (d) HRS unipolar. Unity slope in the double log I-V curves of LRS indicate ohmic conduction. Linear fits in log I-V curves of HRS indicate Schottky emission conduction.

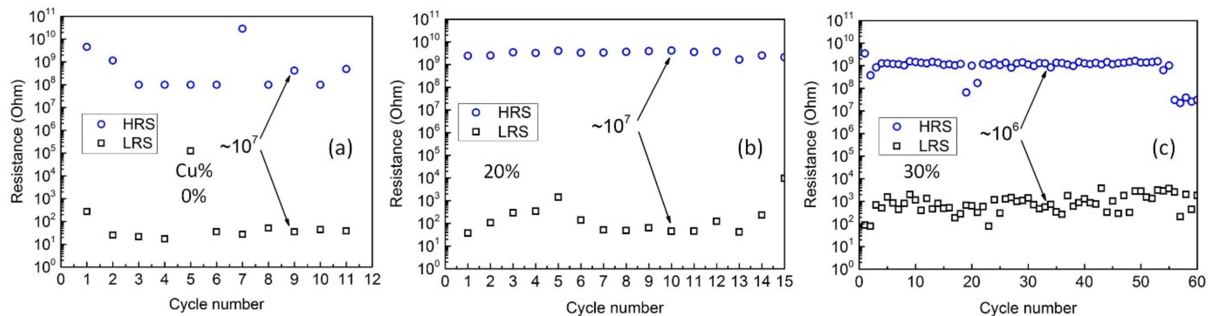

Fig.4. Endurance of pulsed switching of Cu/a-SiC:Cu/Au RMs with (a) 0%, (b) 20%, and (c) 30% Cu%.

Conclusions

Reduced V_{FORM} and V_{SET} and increased endurance were observed in Cu/a-SiC:Cu/Au RMs where Cu embedded a-SiC layers were used as insulator device layer, most noticeable at 30Cu%. Furthermore, Cu/a-SiC:Cu/Au RMs with different Cu% show comparable ON/OFF ratios of approximately 10^7 in bipolar and 10^5 to 10^7 in unipolar modes. While a-SiC RMs shows advantageous switching characteristics, Cu embedding in the a-SiC device layer presents a novel and promising method to improve the overall performance of Cu/a-SiC:Cu/Au resistive memories

Acknowledgments

All data supporting this study are openly available from the University of Southampton repository at http://dx.doi.org/10.5258/SOTON/403082.

References

[1] A. Chung, J. Deen, J.-S. Lee, M. Meyyappan, Nanotechnology 21(41) (2010) 412001.
[2] U. Celano, L. Goux, A. Belmonte, K. Opsomer, A. Franquet, A. Schulze, C. Detavernier, O. Richard, H. Bender, M. Jurczak, Nano Lett. 14(5) (2014) 2401-2406.
[3] J. Guy, G. Molas, E. Vianello, F. Longnos, S. Blanc, C. Carabasse, M. Bernard, J. Nodin, A. Toffoli, J. Cluzel, 2013 IEEE International Electron Devices Meeting, IEEE, 2013, pp. 30.2. 1-30.2. 4.
[4] K. Morgan, J. Fan, R. Huang, L. Zhong, R. Gowers, L. Jiang, C.H. de Groot, AIP Adv. 5(7) (2015) 077121.
[5] S. Rahaman, S. Maikap, W. Chen, H. Lee, F. Chen, M. Kao, M. Tsai, Appl. Phys. Lett. 101(7) (2012) 073106.
[6] L. Zhong, P. Reed, R. Huang, C.H. de Groot, L. Jiang, Microelectron. Eng. 119 (2014) 61-64.
[7] M.-C. Wu, T.-H. Wu, T.-Y. Tseng, J. Appl. Phys. 111(1) (2012) 014505.
[8] L. Goux, J.G. Lisoni, M. Jurczak, D.J. Wouters, L. Courtade, C. Muller, J. Appl. Phys. 107(2) (2010) 024512.
[9] R. Waser, R. Dittmann, G. Staikov, K. Szot, Adv. Mater. 21(25 - 26) (2009) 2632-2663.
[10] I. Valov, R. Waser, J.R. Jameson, M.N. Kozicki, Nanotechnology 22(25) (2011) 254003.
[11] J.-W. Han, M. Meyyappan, AIP Adv. 1(3) (2011) 032162.
[12] S.-J. Choi, J.-H. Lee, H.-J. Bae, W.-Y. Yang, T.-W. Kim, K.-H. Kim, IEEE Electron Device Lett. 30(2) (2009) 120-122.
[13] Y.C. Yang, F. Pan, Q. Liu, M. Liu, F. Zeng, Nano Lett. 9(4) (2009) 1636-1643.
[14] M. Terai, Y. Sakotsubo, S. Kotsuji, H. Hada, IEEE Electron Device Lett. 31(3) (2010) 204-206.
[15] W. Lee, J. Park, M. Son, J. Lee, S. Jung, S. Kim, S. Park, J. Shin, H. Hwang, IEEE Electron Device Lett. 32(5) (2011) 680-682.
[16] W. Lee, M. Siddik, S. Jung, J. Park, S. Kim, J. Shin, J. Lee, S. Park, M. Son, H. Hwang, IEEE Electron Device Lett. 32(11) (2011) 1573-1575.
[17] D. Chen, S. Huang, J. Micro/Nanolithogr. MEMS MOEMS 15(3) (2016) 035005.
[18] Y. Fan, S.W. King, J. Bielefeld, M.K. Orlowski, ECS Trans. 72(2) (2016) 35-50.
[19] S. King, M. French, J. Bielefeld, W. Lanford, J. Non-Cryst. Solids 357(15) (2011) 2970-2983.
[20] L. Zhong, P. Reed, R. Huang, C.H. de Groot, L. Jiang, Solid-State Electron. 94 (2014) 98-102.
[21] L. Zhong, L. Jiang, R. Huang, C.H. de Groot, Appl. Phys. Lett. 104(9) (2014) 093507.
[22] J. Fan, L. Jiang, L. Zhong, R.P. Gowers, K.A. Morgan, C.H. de Groot, Mater. Lett. 178 (2016) 60-63.
[23] A. Gupta, D. Paramanik, S. Varma, C. Jacob, Bull. Mater. Sci. 27(5) (2004) 445-451.
[24] R. Zhou, X. Wu, X. Hao, F. Zhou, H. Li, W. Rao, Nucl. Instrum. Methods Phys. Res., Sect. B 266(4) (2008) 599-603.
[25] S.-H. Wu, D.-H. Chen, J. Colloid Interface Sci. 273(1) (2004) 165-169.
[26] T.-H. Hou, J. Lee, J.T. Shaw, E.C. Kan, MRS Proceedings, Cambridge Univ Press, 2008, pp. 1071-F02-01.
[27] C.-W. Cheng, Y.-C. Tseng, T.-B. Wu, L.-J. Chou, J. Mater. Res. 19(04) (2004) 1043-1049.
[28] S.M. Sze, K.K. Ng, Physics of semiconductor devices, John wiley & sons2006.