RC Relaxation Oscillators (RxO) are attractive for integrated clock sources compared to LC and ring oscillators (RO), as LC oscillators pose integration challenges and RO designs have limited voltage and temperature (V-T) stability. RxOs generate a clock whose time period \( T_P \) depends only on the timing resistor (R) and capacitor (C). Ideally, \( T_P \) is independent of V-T; however, most RxOs use a reference voltage (VREF) against which the voltage of C \( (V_C) \) is compared. Generating a V-T independent VREF is non-trivial and causes variations in RxO frequency. A common approach is the use of VDD-independent current sources or band-gap or device-Vt based VREF [1]. The former are generally high-power options [2] while the latter is subject to process and V-T variations. A correct-by-design approach was adopted in [3] demonstrating VDD-independent operation by cancelling variations through differential sampling of VDD. Further, the power overhead of a supply-independent VREF is overcome by exploiting differential integrator virtual ground. However, 4V^2/R power in the RC tank and high power VCO increase the energy/cycle. 

This work achieves supply-independence using VREF that is a fixed ratio of VDD. This scheme is shown Fig 5.6.1. VREF is generated using a small switched capacitor reference (SCR) such that \( V_{REF} = VDD/3 \) (BY3). SCRs are relatively robust to temperature and switching frequency variations especially in the absence of large load currents as in this design. The conceptual waveforms in Fig 5.6.1 show \( V_C \) while C is being discharged from VDD=0.9 and 1.5V to their corresponding BY3 voltages. Note that \( T_P \) is dictated only by the RC elements and is independent of VDD. The power expended in the RC tank is reduced to 0.44V^2/R giving substantial power savings. Simulation waveforms show how VDD-induced variations in \( X1 \) speed affect the RxO \( T_P \), highlighted by inset waveforms. The 0.9V curve crosses the BY3 trip point at the correct time but experiences a delayed trigger. Likewise, an early trigger at 1.5V results in shorter \( T_P \). To reduce this effect, \( X1 \) must be designed to have sufficient bandwidth at VDDmin which costs power [4]. However, this large bandwidth is only necessary at times when \( V_C \) is very close to VREF.

Observe that \( X1 \) is idle for \( V_C >> V_{REF} \) and can potentially be power gated if it can be turned ON in time for a precise comparison as \( V_C \) approaches VREF. This sub-cycle duty cycling (SDD) of \( X1 \) significantly reduces energy/cycle in the proposed design. Thus, the scheme in Fig 5.6.1 is developed to that in Fig 5.6.2. A coarse low-power comparator \( (X2) \) can be used to determine when \( V_C \) is close to VREF. A Schmitt trigger with device-Vt-based trip points is employed here. If \( X2 \)'s lower trip point is sufficiently greater than VREF across PVT, its output (VCDIG) can be used for SDD. Conceptual waveforms for both VDD=0.9 and 1.5V are shown. When VCDIG=0, M3 turns X1 ON to perform a precise comparison without any loss of accuracy in \( T_P \). X3 is used to clamp the output of \( X1 \) (QCMP) high when \( X1 \) is OFF. Simulated power breakdown in Fig 5.6.2 shows 83% reduction in \( T_P \) when SDD is enabled. Note that SCR is clocked from RxO output revealing a potential start-up problem. Also, the conceptual schematic in Fig 5.6.2 functions only when \( X1 \) and \( X2 \) independently control M1 and M2. However the path through \( X1 \) is fast and always wins over \( X2 \). Also, the delay through \( X3 \) and X4 should be large enough to allow the capacitor to charge to VDD before QCMP turns M1 OFF. These design issues are addressed in the schematic in Fig 5.6.3. SR latch implemented using X5 and X6 prevents a race between QCMP and VCDIG. X7 and X2, implemented as Schmitt NOR, allow SDD to be selectively enabled. X8 overrides SDD so VCDIG may be independently monitored. Individual leakage and dynamic power measurements are possible using EN of X9. A combination of poly and diffusion resistors was used to exploit opposing temperature coefficients and improve RxO temperature stability. C was implemented using MiM while the output of the SCR was decoupled using MOS-caps to reduce ripple-induced RxO jitter. To investigate start-up, a separate leakage-based oscillator (X13) is implemented with the option of a divided clock for the SCR. Finally, a stacked-diode reference (DSR) \( (X14) \) allows evaluation of power-stability trade-off.

VCDIG determines \( X1 \) on-time \( (TON) \) as shown in Fig 5.6.2 which increases with voltage. This means at higher voltages \( X1 \) is turned ON too early in each cycle increasing RxO power. A 200 logic-gate digital assist scheme (DAS) was implemented for run-time measurement of TON and retuning X2 trip point using DTUNE (Fig 5.6.3). This is shown in Fig 5.6.4. X11 is a NAND-based RO enabled for the duration of TON and feeds an 8-bit counter \( (X12) \). A state machine (STM) latches the counter output \( (Q) \) compares with pre-defined thresholds and modifies DTUNE to minimize TON. Measured \( Q \) vs VDD with and without DAS demonstrates reduction in \( T_{ON} \) as \( V_{DD} \) increases. The STM clock (SCK) is self-enabled (ENSK) each time a retune is initiated and is only ON until STM completion. Oscilloscope waveforms in Fig 5.6.4 show the DAS operation with the top pane showing ENSK, start (ST), latch (LAT) and VCDIG signals. The LH bottom waveform shows X11 disabled by VCDIG=1. This ensures \( X11 \) and \( X12 \) run once and only for the duration of TON each time a retune is initiated. This minimises the power overhead of DAS. The tuning settings are only altered when \( X1 \) is OFF. The RH bottom waveform shows TON of 120ns before retune and 80ns upon STM completion. In practice, retune may be initiated by the system at regular intervals. The overhead of DAS is <0.1% of RxO energy even when retuning is initiated at 10ms intervals. Measured results tabulated in Fig 5.6.5 show an 89% reduction with SDC. This includes a 1% overhead due to X2. At 1.4V, DAS provides a further 7% power reduction. While comparator and reference-induced variations in \( T_P \) have been addressed, second-order effects such as digital path speed-up at higher voltages and M1, M2 device-Vt variations due to temperature also induce slight variations in \( T_P \). DAS also helps offset these. Fig 5.6.5 shows the measured \( \Delta T_P \) vs VDD. Compared to DSR, SCR provides 6% better stability. A ±2%/V variation is observed with DAS disabled. DAS improves voltage stability to ±0.49%/V by applying 3 tuning settings at run-time. 96 ppm/c°C stability was measured with SCR. \( T_P \) settles to within 2% in 3 cycles despite RxO SCR being self-clocked. Fig 5.6.6 compares the proposed design with state-of-the-art. Fig 5.6.7 shows the chip plot with the RxO macro using 0.005mm^2 area. The proposed design demonstrates using ratio-reference for VDD-independent RxO and SDC for 0.68nW/kHz operation with DAS for reduced power and improved voltage stability.

Acknowledgements: The authors would like to thank co-researchers at University of Southampton and ARM research for valuable support and Europractice for providing MPW services.

References:

5.6 A 0.68nW/kHz Supply-Independent Relaxation Oscillator with ±0.49%/V and 96ppm/C Stability

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Figure 5.6.1: Schematic of RxO using SCR generated VREF for supply independence with conceptual and simulated waveforms.

Figure 5.6.2: Duty-cycling of comparator in RxO with conceptual waveforms and simulated power breakdown.

Figure 5.6.3: Fully developed scheme as implemented on silicon with poly and diffusion resistance for temperature compensation and testability features.

Figure 5.6.4: Schematic of DAS for on-chip comparator TON measurement, measured counter values and oscilloscope waveforms.

Figure 5.6.5: Measured power reduction due to SDC of comparator and further due to DAS, voltage and temperature stability and start-up.

Figure 5.6.6: Comparison with state-of-the-art for voltage and temperature stability vs nW/kHz and table summarising measured results.
Figure 5.6.7: Chip photo and annotated layout including placed and routed DAS.