Resistive switching of Pt/TiO$_x$/Pt devices fabricated on flexible Parylene-C substrates

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Abstract

Pt/TiO$_x$/Pt resistive switching (RS) devices are considered to be amongst the most promising candidates in memristor family and the technology transfer to flexible substrates could open the way to new opportunities for flexible memory implementations. Hence, an important goal is to achieve a fully flexible RS memory technology. Nonetheless, several fabrication challenges are present and must be solved prior to achieving reliable device fabrication and good electronic performances. Here, we propose a fabrication method for the successful transfer of Pt/TiO$_x$/Pt stack onto flexible Parylene-C substrates. The devices were electrically characterised, exhibiting both digital and analogue memory characteristics, which are obtained by proper adjustment of pulsing schemes during tests. This approach could open new application possibilities of these devices in neuromorphic computing, data processing, implantable sensors and bio-compatible neural interfaces.

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Keywords: microfabrication, memristor, flexible electronics, resistive switching & RRAM, bio-compatible devices
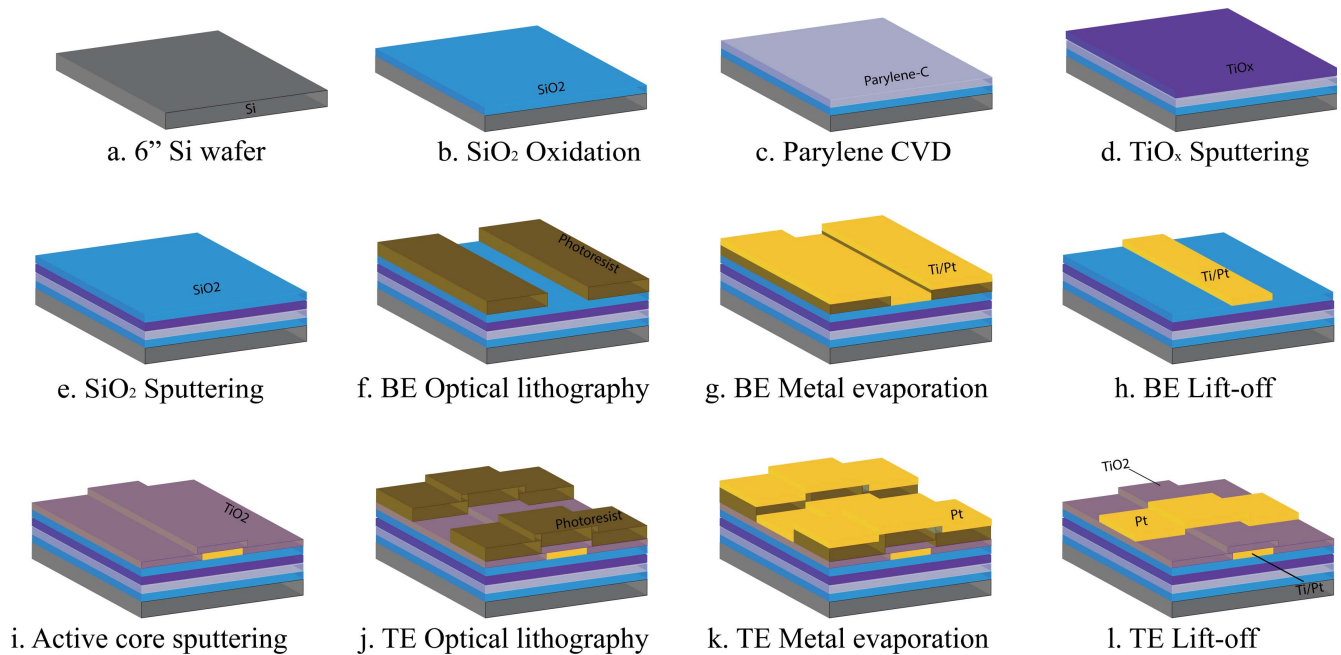
SQ1   (Some figures may appear in colour only in the online journal)

Introduction

Development of flexible electronics [1] and the emergence of memristors [2] for future memory devices lead inevitably to their aggregation to exploit their potential for hybrid and bio-compatible applications. Indeed, the interest in flexible electronics is rapidly increasing due to its immense application potential in flexible screens, smart-phones and implantable sensors for health monitoring and disease diagnosis [1, 3–5]. These applications require higher memory capabilities, which memristors are known to provide. Memristors are also attractive thanks to their intrinsic characteristics of non-volatile storage, distinct OFF/ON resistive states, either analogue (gradual) or digital (abrupt) switching, along with their promising high memory density capability thanks to their simple structure and potential back-end of line

compatibility [6–11]. Nevertheless, many challenges still remain before achieving memristor integration into flexible substrates, such as temperature compatibility, surface roughness and materials compatibility.

Choi *et al* previously demonstrated flexible non-volatile memory devices based on polyethersulfone (PES) and Parylene substrates. They have presented studies using Al and ITO as electrodes, and a-TiO$_2$, Graphene Oxide, ZnO and Al$_x$O$_y$ as oxides [12–14]. Recently, the same team has presented 1T1M memory device [15]. Other groups [16–21] have used PES, polyethylene terephthalate, polyethylene naphthalate or polyimide based flexible substrates. Aluminium, IZO, TaN and Ni electrodes were utilised with various oxide layers such as Polymer, HfON, Al$_2$O$_3$ or TiO$_2$. It is worth noticing that Parylene can be used as flexible substrate as well as switching medium, as demonstrated in [22]. On the

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a. 6" Si wafer	b. SiO₂ Oxidation	c. Parylene CVD	d. TiOₓ Sputtering
e. SiO₂ Sputtering	f. BE Optical lithography	g. BE Metal evaporation	h. BE Lift-off
i. Active core sputtering	j. TE Optical lithography	k. TE Metal evaporation	l. TE Lift-off

Figure 1. Main fabrication steps of flexible resistive switching devices.

other hand, previous studies have demonstrated that one of the most promising memristive stacks on traditional rigid Silicon (Si) substrates is Pt/TiO$_x$/Pt [6, 23, 24]. It presents interesting electrical characteristics such as analogue and digital switching and good endurance; it also can store multiple bits/cell thanks to its intrinsic multistate characteristics [11, 25]. All these attributes make it attractive for data processing, neuromorphic computing, sensors and selector based 3D crossbar resistive switching (RS) memory applications [23, 26–31]. Nonetheless, similar characteristics and devices comprising this stack have not been demonstrated in flexible biocompatible substrates.

Parylene-C is an attractive material; it is generally used for encapsulation and as moisture/dielectric barrier. It is well known as a bio-compatible, temperature resistant, pinhole free and low dielectric constant material [32–37]. Our objective in this work is to transfer Pt/TiO$_x$/Pt stack to Parylene flexible technology. Up to now the fabrication of this stack has mainly been done on Si substrates/wafers. This stack has not been fabricated yet on flexible substrates because the technology transfer raises some important challenges, such as high temperatures (up to 1000 K) during film depositions and more importantly during switching [38], flatness and roughness qualities of flexible substrates affecting device's quality and thus the overall switching reliability. In this study, we have demonstrated successful fabrication of flexible Pt/TiO$_x$/Pt memristors using Parylene-C as substrate protected by TiO$_x$ and SiO$_2$ films. Our prototypes' electrical characteristics from sweeping and pulsing mode experiments demonstrate that our devices can exhibit gradual, abrupt and even multistate switching, with excellent endurance. These results could pave the way to the memristor integration in bio-compatible devices based on Parylene-C substrates.

Method

Transferring Pt/TiO$_x$/Pt memristors from rigid Si substrate to flexible Parylene substrate required several modifications in the fabrication flowchart (figure 1), when compared to previously fabricated TiO$_x$ ReRAM [10, 11, 23, 28, 39]. Here, a Si support substrate was used for achieving similar insulating characteristics and surface roughness quality. 200 nm thick SiO$_2$ was thermally grown in a furnace at 1000 °C on standard ⟨100⟩ 6″ Si wafer, polished on one-side only (figure 1(b)). Then, a Parylene-Coater was employed to deposit 8 μm Parylene-C film (figure 1(c)) by chemical vapour deposition (CVD) with a pressure of 15 mTorr at a temperature of 690 °C. These conditions guarantee an excellent film quality, in term of surface roughness, homogeneity and absence of pinholes. The Parylene-C surface was gently treated with oxygen plasma: 10 s reactive ion etching (RIE) was used with an O$_2$ flow of 50 sccm at a pressure of 100 mTorr, power of 100 W and DC bias of 220 V. This makes the film hydrophilic and ensures better adhesion of the subsequent film, TiO$_x$. Hence, TiO$_x$ was sputtered (figure 1(d)) from a Ti metal target in a dual magnetron Sputterer, Leybold Helios Pro XL Sputterer, under the following conditions: 35 sccm Ar and 8 sccm O$_2$ flows, 2 kW cathode power and 15 sccm of O$_2$ in an additional plasma source, powered at 2 kW. This ensures further oxidation and achieve near stoichiometric TiO$_x$, with $x = 1.94$ [40]. Right after and without breaking the vacuum, SiO$_2$ was deposited (figure 1(e)) using the following sputtering conditions: Si target was used with a flow of 30 sccm Ar, 12 sccm O$_2$ and 2.5 kW power at the cathode. Finally, 10 sccm of O$_2$ flow and 2 kW at the additional plasma source was also used to achieve stoichiometric film. Both films, TiO$_x$ (50 nm) and SiO$_2$ (50 nm), were sputtered at room temperature.
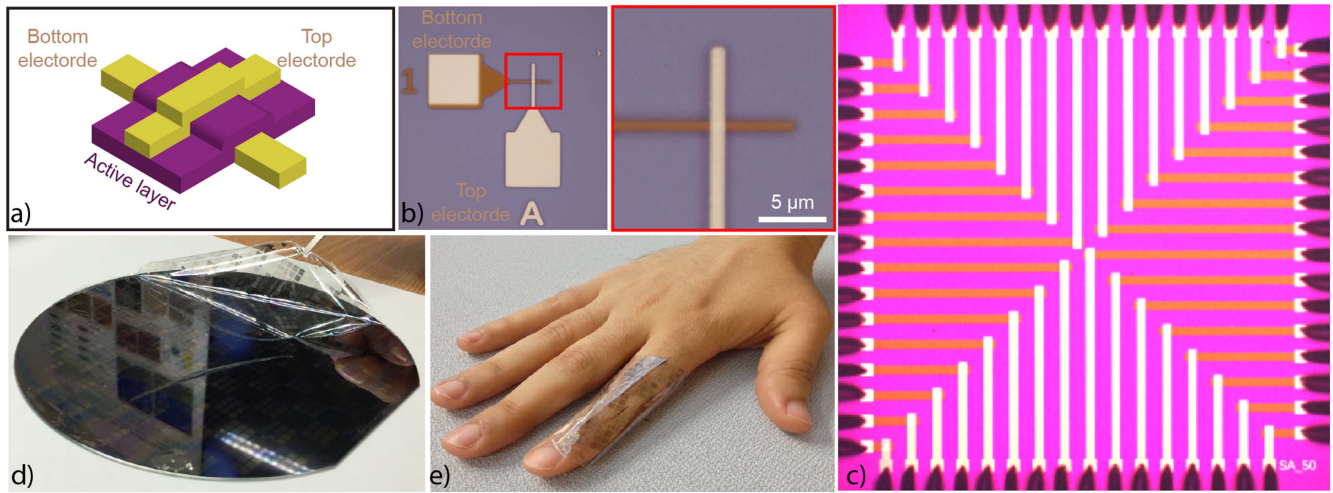
Figure 2. Fabricated devices. (a) Schematic of a crossbar device, (b) microscopic image of 2×2 μm^2 single device, (c) 32×32 array of single RRAM devices, (d) peeling process of the flexible devices from SiO$_2$/Si wafer, (e) image illustrating devices' flexibility.

Photolithography was used for the three patterned layers contained in this fabrication flowchart. Negative photoresist AZ2070 was chosen to create negative side-walls after development that ensured good liftoff quality. Also, a mild oxygen plasma treatment was performed to remove any residual resist remained on the surface of the developed areas. Leybold optics LAB700EB electron beam (e-beam) evaporator was used for bottom (BE) and top (TE) electrodes metallization: 5 nm thick adhesive Ti then 10 nm Platinum (Pt) films for BE and 10 nm Pt for TE were deposited (figures 1(g) and (k)). Between BE and TE, 25 nm thick TiO$_x$ active layer was patterned and sputtered using similar condition to the previously deposited TiO$_x$ film (figure 1(i)). Liftoff process (figures 1(h) and (l)) was chosen instead of etching to avoid affecting the films' quality, particularly superficial layers which might interfere in the devices' behaviour. Moreover, gentle oxygen plasma clean was carried after each step to guarantee the cleanest possible interfaces.

The developed process flow allowed the successful fabrication of the following stack: Pt/TiO$_x$/Pt/Ti/SiO$_2$/TiO$_x$/Parylene-C/SiO$_2$/Si stack (figure 1), where Pt/ TiO$_x$/Pt is the memristive device. Schematic and microscopic images of a 2×2 μm^2 single cell are shown in figures 2(a) and 1(b), successively, followed by and array of 32×32 single devices (figure 2(c)). Figure 2(d) shows the peeling process of the flexible substrate comprising devices, from SiO$_2$/Si rigid wafer. Finally, figure 2(e) illustrates the flexibility of the devices for an eventual bio-compatible application.

The electrical characterisation of our prototypes was carried out via DC and pulsing modes. For both a custom made electronic hardware with an mBED LPC1768 microcontroller board [41] was used. This instrument is capable of addressing RRAM arrays up to 1 kb in size (32×32 cells). During all the measurements, the voltage bias was applied to the TE, while maintaining the BE grounded.

Results

Figure 3 shows the first electrical characterisations performed on Parylene-based devices. Here, 100 current–voltage (I–V) DC sweeping cycles were realised (figure 3(a)). For each cycle, the voltage was swept from 0 to -1.8 V then to $+1.8$ V and back to 0 V with steps of 0.05 V. All the cycles show pinched hysteresis loops with zero crossing (see the inset in figure 3(a)), indicating memristive behaviour. Figure 3(b) shows the equivalent resistance-voltage characteristics. A clear opening is observed for all the cycles, depicting OFF and ON resistive states. This is confirmed with the cumulative probability figure shown in figure 3(c), where a clear window is present between the high resistive state (HRS or OFF) and the low resistive state (LRS or ON). Larger variability at HRS is observed due to the dominating effect of randomly dispersed percolation branches in the absence of continuous conducting filaments across the active switching film [25].

In DC sweep mode, the electroforming was found to occur at both negative and positive polarities. However, the devices tend to breakdown quickly after a negative forming because of the required high voltage thresholds (see supplementary materials figure S1). It is worth mentioning that the device from which figure 3 results were obtained was electroformed in pulsing mode.

Pulse characterisation allows the fine tuning of the RS and less invasive manipulation of the devices. To electroform the device, 1 ms pulses were applied with gradual increments of 0.2 V in amplitude, start from $+1$ to $+12$ V with 10 pulses at each step. A series resistance of 10 kΩ was introduced to further protect the devices. For all the pulsing experiments, the resistive values were assessed with non-invasive pulses of 0.2 V. 75% of the devices electroformed at 7.5 ± 1 V, with an additional two or three repeated ramps required for some of the devices. As an example, the device shown in figure 4(a) electroformed at the first ramp, at 7 V.

Figure 4(b) shows that the device subjected to positive and negative pulse cycles supports analogue switching. The
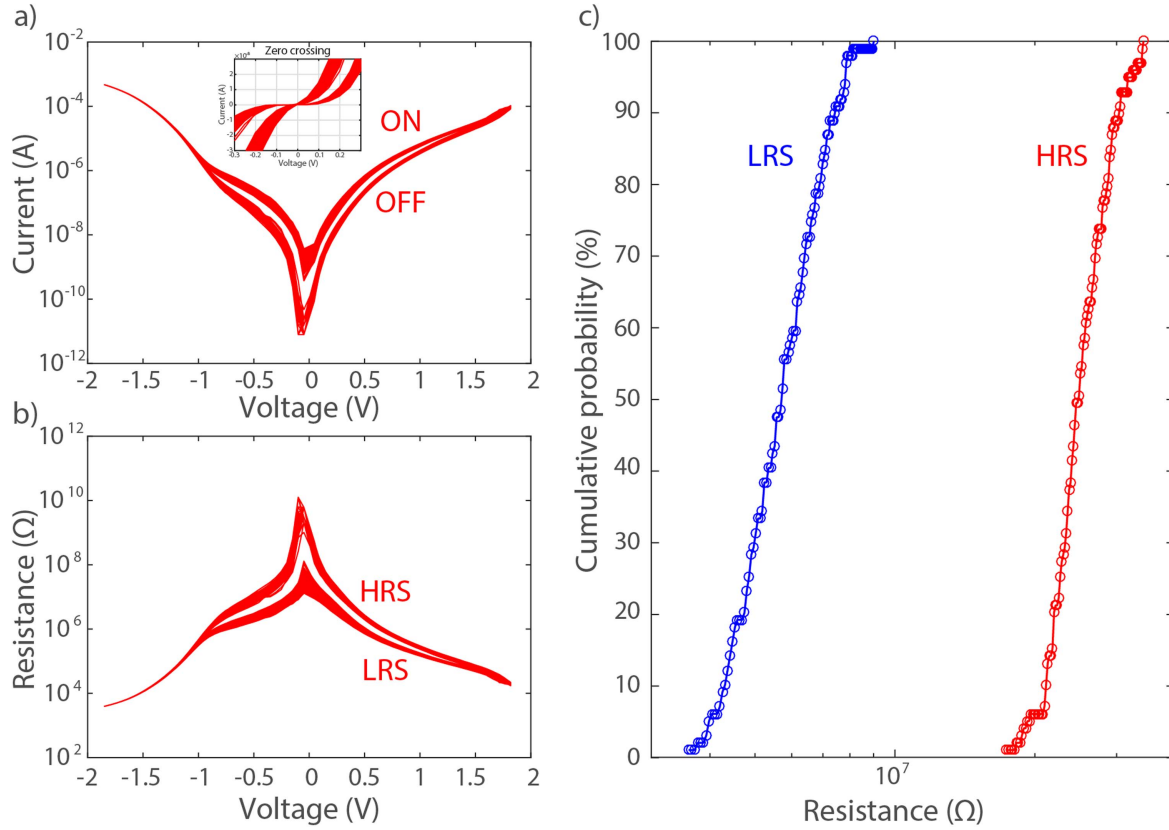
Figure 3. 100 DC sweeping cycles: (a) *I–V* characteristics with the inset depicting the pinched hysteresis and zero crossing characteristics, (b) *R–V* characteristics, (c) cumulative probability for OFF and ON states.

pulsing scheme consists of ramps from +0.2 to +2.7 V then from −0.2 to −2.7 V, with ±0.1 V step increments. 10 pulses of 5 μs duration each were applied at each voltage level followed by non-invasive 0.2 V pulses for assessing the devices memory states. The maximum applied voltage, for positive and negative polarities, is set by a tolerance band, which consists of the change in resistance from the initial value right after reversing the pulsing polarity. For this experiment, this tolerance band was fixed arbitrarily at 5% resulting in resistive states toggling between ≈44.6 ± 1 kΩ and ≈47 ± 1 kΩ. Positive voltage reduces the RS and negative one increases it. Figure 4(c) depicts the digital switching capability of the device. Here, another device was subjected to trains of 1 positive and 1 negative pulses of ±1.9 V, with a pulse width of 15 μs. RS changes were not bounded artificially by a tolerance band, achieving RS changes between ≈180 kΩ and ≈530 kΩ. Nonetheless, applying longer pulses or of higher amplitudes can change the operating RS levels away from the equilibrated values of figure 4(c).

During the endurance experiment, voltage pulses were sent to the device in cycles, where each cycle comprised positive/negative pulses with amplitudes of ±2.1 V and duration of 5 μs, the readout was carried out by sending non-invasive pulses of 0.2 V. This is shown in figure 5 where a clear opening window separating the OFF and the ON resistive states, toggling between ≈580 kΩ and ≈460 kΩ is observed (inset b). About 2×10^3 cycles were obtained successfully (inset a), after which the ON/OFF resistive ratio

collapses. Particularly, HRS was moving towards LRS, until breakdown.

To investigate the role of pulse amplitude and width in achieving multistate operation, each of them was varied independently. Figure 6(a) shows the multistate characteristics obtained after pulse amplitude changes: the pulsing scheme consists of sending batches of pulse trains with each train containing 100 cycles of positive/negative pulses. The amplitude of the positive pulses was varied for each train while the negative ones remained constant at 2.5 V and 5 μs. The negative pulse amplitudes were varied from −2.3 to −2.7 V then back to −2.3 V, with ±0.1 V increments, the pulse duration was maintained constant at 5 μs. Figure 6(a) shows that the LRS is relatively stable, however, the HRS was changing by ≈600 Ω after each increment. Reading was done with 0.2 V pulses. The higher the pulse amplitude the larger OFF/ON resistive ratio becomes. Figure 6(b) shows similar behaviour of another device when, this time, the pulse widths (positive and negative polarities) were varied while maintaining the pulse voltage amplitudes constant, at ±1.9 V. For this experiment the pulse widths were varied from 5 to 30 μs then back to 5 μs, with ±5 μs increments. It is interesting to note that resistance change at LRS is smaller than that of HRS. On average, varying the pulse widths at LRS changes the resistance by ≈5 kΩ, while, at HRS it changes by ≈20 kΩ. Moreover, increasing (decreasing) the pulse width produces a wider (narrower) OFF/ON resistive window. Figure 6(c) shows a combination of the two changes, pulse
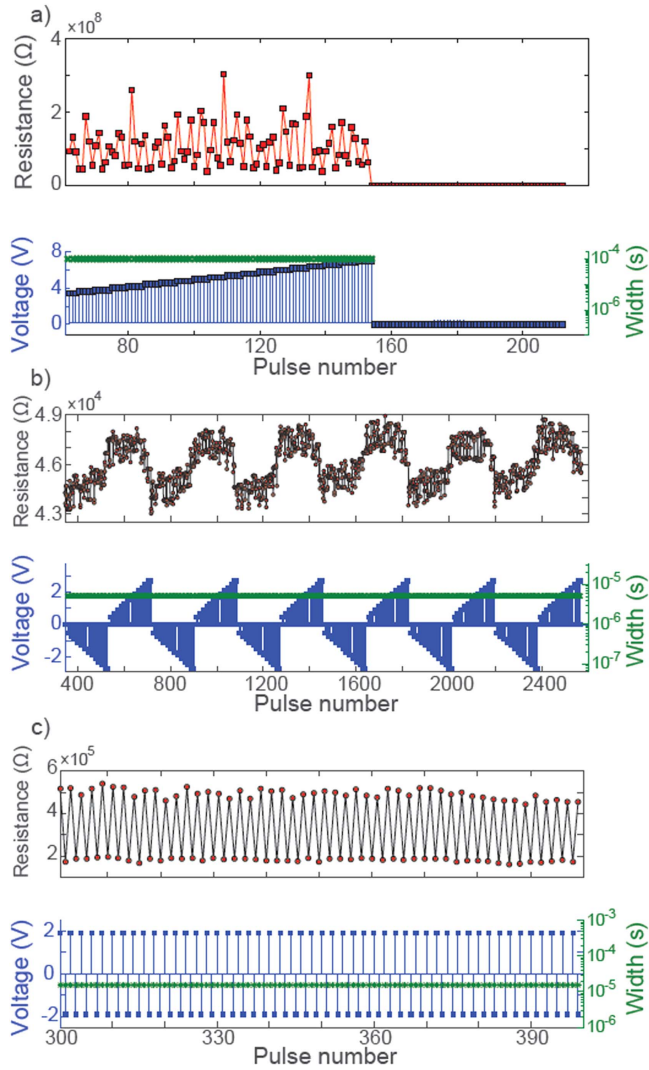
Figure 4. Device characterisation in pulsing mode: (a) electroforming the device with positive pulsing ramp, (b) analogue 'gradual' switching of the device with voltage increase at positive and negative polarities, and (c) digital 'abrupt' switching of the device using one pulse only at each polarity.

amplitude and width successively; first the pulse width was fixed at $5\,\mu s$ and the voltage amplitude was increased from ± 1.7 to ± 1.8 V then to ± 1.9 V. After that, the amplitude was not changed and the pulse width was increased gradually to $30\,\mu s$ with steps of $5\,\mu s$. A continuous and gradual opening of the OFF/ON resistive envelope is observed, which was caused by gradual increase of the pulse amplitude then its width.

Understanding the volatility of the devices is very important for real applications. Therefore, an experiment consisting of sending a ramp of single pulses, from 2.4 to 1.5 V then back to 2.4 V in steps of 0.1 V and widths of $5\,\mu s$ was carried out. However this time reading was done continuously for 60 s after each pulse at 0.2 V read-out amplitude to assess the volatility component. Figure 7(a) shows the results done on flexible devices before peeling. The devices are clearly volatile; this case be seen better when relatively high voltages are used because they drag the device's resistive
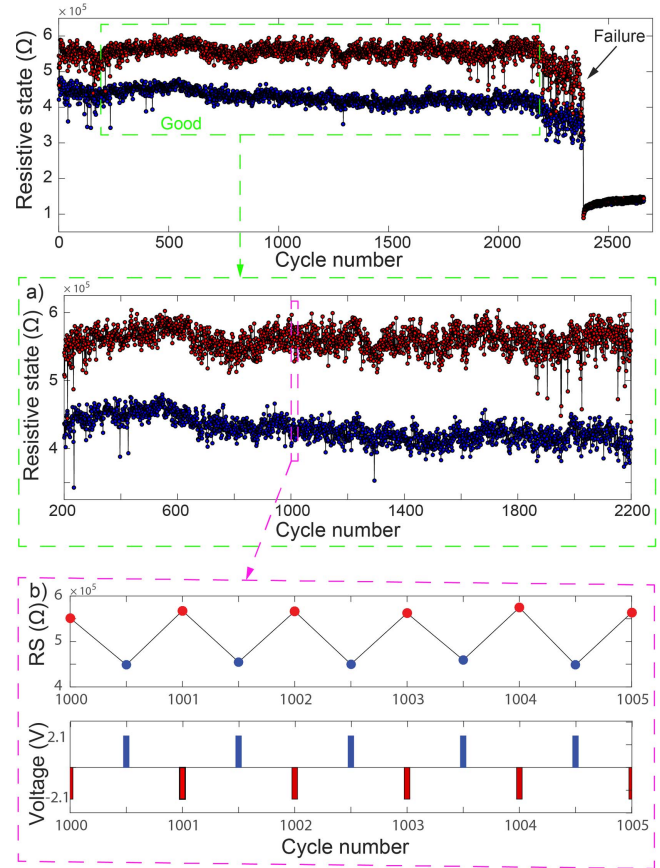
Figure 5. Endurance test with the inset (a) depicting 2×10^3 cycles while the inset (b) showing a close-up on five RS cycles and their corresponding pulsing scheme.
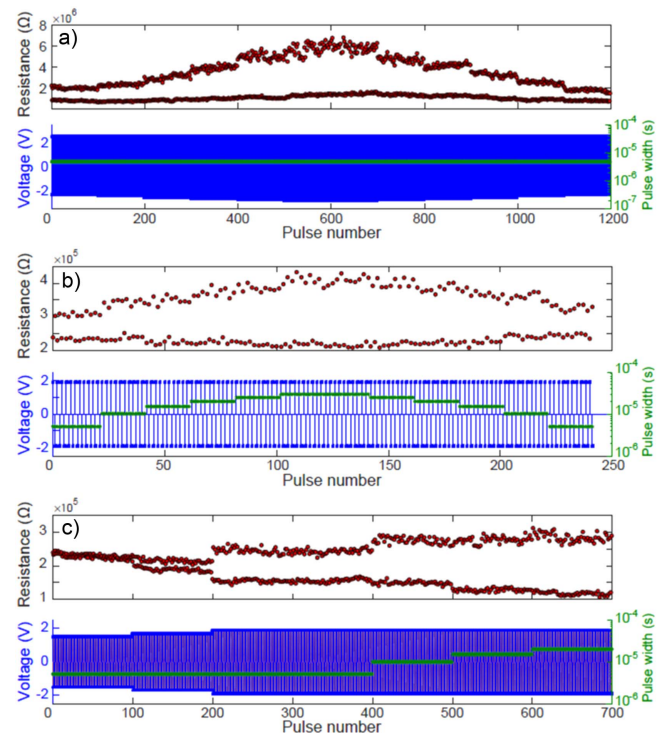
Figure 6. Influence of (a) voltage amplitude, (b) pulse duration, and (c) pulse amplitude and width on the device's RS.
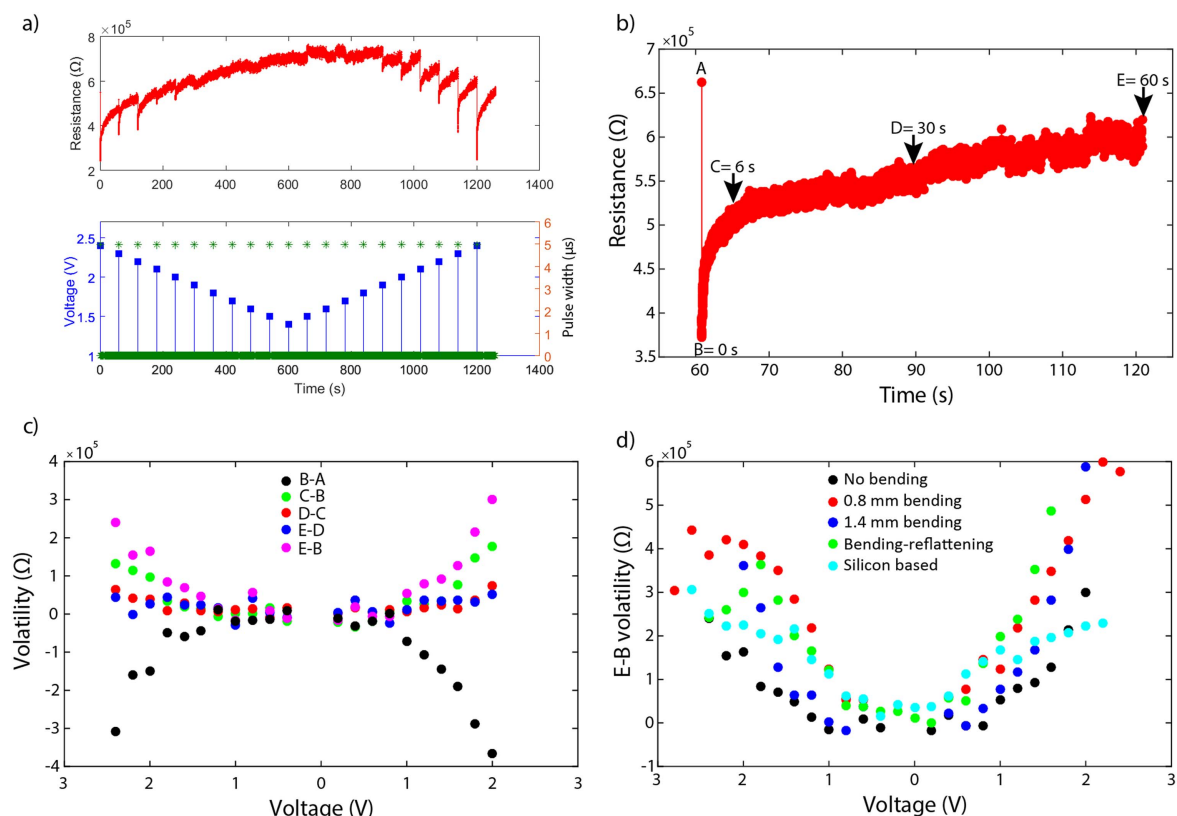
Figure 7. Volatility measurements. (a) 60 s volatility measurements after various voltage pulse amplitudes, (b) example of single volatile curve (close-up image from a, at 2.3 V pulse), (c) Resistive change of the 2.3 V pulse (B-A shown in figure (b) and between different relaxation times (C-B, D-C, E-D and E-B shown in figure (b)), (d) E-B volatilities for different pulse voltages of 5 configurations: No bending, 0.8 mm bending radius, 1.4 mm bending radius, bending then reflattening and silicon based devices.

states to even lower values before it relaxes back. Figure 7(b) shows a close-up of figure 7(a), after applying 2.3 V pulse then read during 60 s. To have better understanding of the relaxation curve, 5 markers are put in it: a before pulsing, B the first reading value, C reading value after 6 s (10% of reading time), D reading value after 30 s (at 50%), E reading value after 60 s (100%), thereafter, figure 7(c) is extracted. It shows the change in resistive states between consecutive markers. We observe that the device relaxes fast at the beginning then it slows down gradually.

Robustness of the devices was studied by carrying out bending experiments. In these experiments we compared the volatility results from 5 configurations: Parylene-based (no bending), Parylene-based (0.4 mm bending radius), Parylene-based (1.4 mm bending radius), Parylene-based (bending-reflattening) and silicon-based devices. All the results are shown in supplementary materials (figure S2). The results shown in figure 7(d) depict the 60 s relaxation (E-B) of each configuration after various voltage pulse stimuli, were we conclude that they are relatively comparable.

After peeling the Parylene-C substrate (figure 8(a)), containing the devices, bending it and folding it over as shown in figures 8(a) and (b), the sample was put back on a flat surface (figure 8(c)) to allow a good contact of the probe needles for performing post-bending tests. This configuration is the most invasive to the devices, compared to different bending radii, therefore we have chosen it for the endurance

characterisation. Figure 8(d) shows endurance results indicating that the sample supports over 8×10^3 OFF/ON RS cycles even after the peeling-reflattening process. Finally, as a comparison endurance test was done on a similar stack, Pt/TiO$_x$/Pt, fabricated on a rigid Si wafer (without Parylene-C) and the results are depicted in figure 8(e), where 5×10^3 OFF/ON RS cycles are achieved.

Discussion

Several technological challenges had to be overcome to obtain the flexible Pt/TiO$_x$/Pt/Ti/SiO$_2$/TiO$_x$/Parylene-C stack. The Si wafer chosen as a base substrate is one-side polished only, which makes the evaporated (CVD) Parylene-C film quality good on one side and poor one the other. This quality difference was noticeable even after SiO$_2$ thermal growth on Si. To accomplish an easy and homogeneous peel-off of the devices, at the end of fabrication, adhesive product was avoided during Parylene-C deposition. Consequently, Van der Waals force was the unique force responsible for Parylene-C adhesion to the wafer. Obviously, the adhesion is poorer at the back-side of the wafer because of its high surface roughness. Moreover, the wafer stage (holder) shape affects the evaporation homogeneity at the back-side of the wafer. These aspects make spinning of the photoresist challenging because of vacuum failure, particularly at the latest
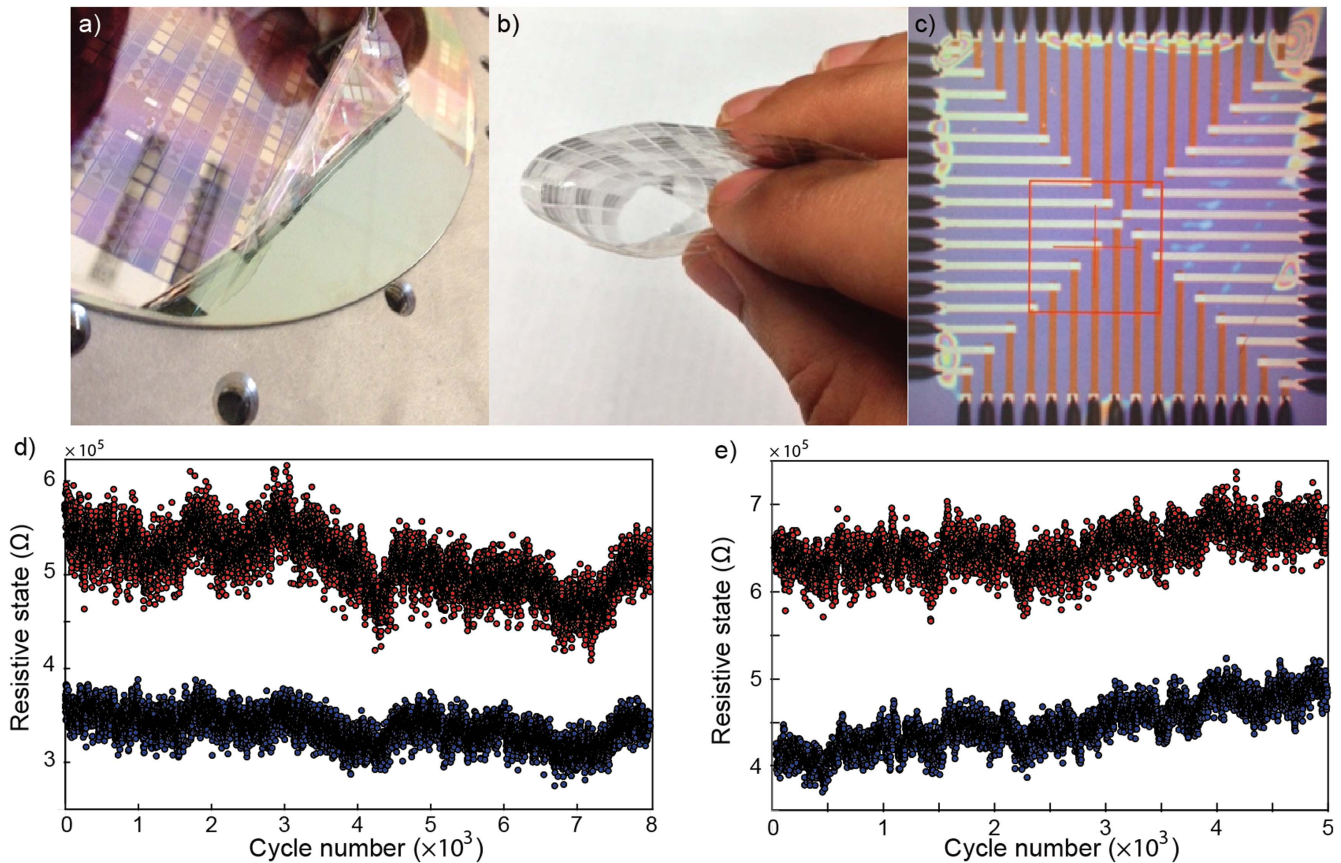
Figure 8. Flexible devices: (a) peeling-off, (b) bending, (c) probes-pads connexion after peeling-reflattening process where some air bubbles are still visible, (d) endurance test after peeling the device showing 8×10^3 OFF/ON cycles, (e) endurance test of silicon-based device with 5×10^3 cycles, as comparison.

stages of fabrication, as the Parylene-C film quality degrades gradually. The attempt to protect the wafer's back-side from Parylene-C deposition was successful; however, Parylene-C cannot handle different vacuum pressures during RIE and NMP liftoff processes. Consequently, Parylene-C was lifted than peeled-off because its adhesion force to Si/SiO$_2$ wafer became weaker. The solution to this problem was to envelop the whole wafer by Parylene-C. This is accomplished by avoiding protecting the back-side of the wafer and by lifting the wafer up, at three distinguished points, from the wafer stage during CVD process.

Parylene-C is an electrical insulator, therefore, one might assume depositing the stack Pt/TiO$_x$/Pt straight on top would be enough to successful fabrication of the devices. Nonetheless, Parylene-C is affected by the resist developer which etches it slightly, hence resulting in electrodes of lower quality when compared to the solid Si-based flowchart. Moreover, using e-beam evaporation technology to evaporate Pt requires high evaporation temperature. Even though the temperature of the wafer holder never exceeds 70 °C, the deposited Pt grains on the wafer surface remains extremely hot. This affects Parylene-C in the developed areas, particularly in the small areas where the consequences of this effect is more pronounced, such as 2 μm wide electrodes. Using any other technology, such as sputtering which uses lower deposition temperatures, results in having fences after liftoff

process. This is caused by the stage rotation, and particularly by the small target-wafer distance ($\sim$10 cm) contrarily to the 1.25 m distance of the used e-beam evaporator where excellent laminar flow of the metal evaporation is achieved.

To resolve the two issues caused by resist developer and Pt hot grains, protective stoichiometric SiO$_2$ layer was sputtered on Parylene-C, before BE photolithography. However, because of the poor adhesion quality between Parylene-C and SiO$_2$ many holes were created across the wafer during different process steps, which originated peeling-off the devices from Parylene-C film. Therefore, two supplementary steps were added to ensure better adhesion: short RIE process to transform Parylene-C from hydrophobic to hydrophilic film followed by sputtering near stoichiometric insulating TiO$_x$ layer that sticks well to the previously deposited Parylene-C and to the following sputtered SiO$_2$ film.

SiO$_2$/TiO$_x$ films play two other important roles which consist of improving the surface quality for better Pt/TiO$_x$/Pt depositions and protecting Parylene-C film from any damage during electrical characterisation, where high temperatures are generated particularly during electroforming step [38]. This is of paramount importance for implantable flexible device implementations. The surface roughness difference between Parylene-based and silicon-based devices is in the order of 5 nm, which is small enough to preserve a good uniformity of different deposited layers (figure S3). Consequently, no major

difference in the electrical measurement results was observed. Figure S3 shows atomic force microscope topography measurements after each fabrication step for both cases: before top electrode, after bottom electrode, after active layer and after top electrode depositions. The final obtained stack, Pt/TiO$_x$/Pt/Ti/SiO$_2$/TiO$_x$/Parylene-C/SiO$_2$/Si, was found to be the best configuration for testing and peeling-off the flexible devices. Devices along 6″ sized flexible Parylene-C film were successfully fabricated.

The fabricated devices belong to valance change memory (VCM) family [42, 43]. VCM switching mechanism involves ions migration in the oxide layer that affects, as a consequence, the device internal resistance, toggling it between different resistive states. Oxygen vacancies are thought to be responsible for the switching in this class of devices. Initially, the devices are found in a highly insulating pristine state: the forming step makes the formation of oxygen ions possible. The vacancies start to drift due to the external electric field that leads to the vacancies accumulation [44–46] building up a small, confined and conductive region within the oxide layer, the conductive filament. The filament can connect the electrodes completely or partially. In our case, the difference between a fully connected and a partially connected filament can explain the difference in the resistance ranges found, for example, between the high (figure 3) and low (figure S1) resistive operating ranges [47]. The negative DC sweep completely forms a filament bridging the electrodes, therefore operating the devices in lower resistive ranges. Hence, the DC SET and RESET operations connect and disconnect the formed filament.

The difference in the devices' behaviour under different electroforming routines can be explained within the filamentary operating framework. During the electroforming, it was proven [48] that ionic defects such as oxygen vacancies are injected in the oxide film and subsequently drifted under the action of an electric field. Oxygen vacancies are known to be positively charged. During negative electroforming, a negative bias is applied to the top electrode and the bottom electrode is grounded. Hence, vacancies tend to accumulate in a region close to the top electrode, where the nucleation of the filament can begin. The filament growth will then continue along the electric field lines, with the filament's tip pointing towards the bottom electrode. On the contrary, when a positive electroforming is applied, the filament grows from the bottom towards the top with the tip pointing towards the top electrode. When the filament is formed, the RS involves the interaction between the oxygen-deficient filament, the electrode, the surrounding oxide film and the external environment in the top electrode side. Indeed, it has been proven that during RS oxygen can be exchanged with the environment which can act as an effective oxygen reservoir [49, 50].

Similar TiO$_2$-based ReRAMs have been previously reported to achieve a RS related to the formation and disruption of a conductive filament [31, 51]. Thus, the difference between positive and negative electroforming can be related with the filament behaviour at different interfaces during the switching. Oxygen exchange is favoured when the filament tip is close to the surface [50], strongly affecting switching

dynamics. This is the case for positive electroforming. On the other hand, when the tip is close to the bottom electrode (negative electroforming case) the probability of oxygen exchange with the atmosphere becomes much lower. This difference could lead to an easier switching in the first case, where the oxygen exchange is favoured. Oxygen from the atmosphere can help restoration of the initial insulating properties of the filament tip, returning device to its HRS under the action of an electric field. On the contrary, when oxygen exchange is less favoured, the resistive state restoration could be more difficult, resulting in a less reliable RS phenomenon.

The pulse operation allows a better control on the stress induced in the device during the forming step. In particular, the amount of energy is generally lower and more controllable by the proper tuning of voltage amplitude and time width. It is therefore possible to argue that in case of pulsed operation, the electroforming step forms a filament which is partially connected only, either being too thin or with a thin oxide region present between its tip and the electrode. This can be evidenced by the rectifying *I–V* curves, either in OFF or ON states, shown in the inset of figure 3(a). It is important reiterating that this device was electroformed in pulsing mode.

This interpretation offers an explanation for the origin of the analogue and multistate behaviour demonstrated during pulsed characterisation. These two latter operations reported can be related to the small changes in the conductivity of the filament tip/electrode interface. As an example, the remaining thin oxide layer between the tip of the filament and the electrode could be the responsible for analogue and multistate variation of the resistive states that affects the oxide based conduction mechanisms (Schottky or Fowler–Nordheim emission, direct and trap-assisted tunnelling) enhancing or depressing them. Alternatively, the same effect can be obtained by the change in the local oxygen vacancies concentration that similarly affects the local conductivity and therefore allowing the resistive state tuning.

This interpretation can also explain the reason that the chosen 5% tolerance band allowed achieving a relatively non-destructive switching, probably due to a gentle and small movement of the ions/vacancies. On the contrary, in order to have abrupt switching, further invasive voltages were needed to inject higher energies to the device thus generating sudden changes in the resistive state. Moreover, the devices gain their HRS after a certain waiting time and any fast recovery needs an extra-pulse with an opposite polarity. This allowed us to characterise the endurance of the devices. However, the volatility component has to be considered before any implementation of these devices.

Peeling process consists on folding over the Parylene-C substrate for more than 135°, nonetheless, after reflattening it and testing the devices again similar results, to prior-peeling and to Si-based devices, were obtained. The same was observed in bending experiments. This proves the robustness of the devices even after peeling and bending processes, which makes it interesting candidate for flexible applications.

Conclusion

In summary, $Pt/TiO_x/Pt$ resistive memory stacks were transferred successfully onto flexible substrates. Several fabrication challenges were identified and addressed. The detailed fabrication method presented here will allow faithful reproduction of the devices. The devices were validated by electrical characterisations in sweeping and pulsing modes resulting, demonstrating the devices capacity to support both abrupt and gradual switching, with multiple storage capabilities generated by amplitude and duration changes of the applied pulses. In this work the volatility characteristic of these devices is also studied and finally a good endurance of 8×10^3 cycles achieved after peel-off and bending processes. The digital and analogue behaviours are related with a full or partial filament formation in the VCM cell due to oxygen vacancies' drift under the action of an external electric field. The results presented in this work are comparable with those coming from Si-based devices, indicating a promising future for these devices for neuromorphic, flexible and bio-compatible applications.

Acknowledgments

Data availability

The data for this paper can be found at: http://dx.doi.org/10.5258/SOTON/397944

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