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# A circuit model for defective bilayer graphene transistors



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## ARTICLE INFO

### Article history:

Received 18 August 2015

Received in revised form 7 December 2015

Accepted 10 February 2016

Available online 27 February 2016

The review of this paper was arranged by Dr. Y. Kuk

### Keywords:

Graphene  
Helium ion  
SPICE model  
Defective

## ABSTRACT

This paper investigates the behaviour of a defective single-gate bilayer graphene transistor. Point defects were introduced into pristine graphene crystal structure using a tightly focused helium ion beam. The transfer characteristics of the exposed transistors were measured ex-situ for different defect concentrations. The channel peak resistance increased with increasing defect concentration whilst the on-off ratio showed a decreasing trend for both electrons and holes. To understand the electrical behaviour of the transistors, a circuit model for bilayer graphene is developed which shows a very good agreement when validated against experimental data. The model allowed parameter extraction of bilayer transistor and can be implemented in circuit level simulators.

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## 1. Introduction

The high electron mobility and saturation velocity in graphene makes it suitable for analogue electronics applications despite the lack of an energy band gap [1].

However, despite the absence of a bandgap in large scale graphene, the long mean free path of electrons and the high carrier mobility allows circuits to operate at high frequencies. Following the achievement of impressive GHz cut-off frequency for graphene transistors [2–4], a number of applications in RF electronics have been reported which include frequency mixers and multipliers [5–7] and oscillators [8]. Equally, a graphene based integrated circuit consisting of active and passive components in the signal amplification, filtering and downconversion mixing units has been demonstrated [9].

The mean free path is limited by the presence of charged impurities (such as trapped charges in the underlying substrate), structural defects, corrugation, etc., which cause scattering of charge carriers. Experimental evidence shows that pristine suspended graphene has an exceptionally high carrier mobility as the substrate effects are eliminated [10,11]. Although carrier transport properties in graphene are well understood, practical models which are useful for circuit level simulation are still lacking. In this work, we systematically investigate the transport characteristics of a pristine bilayer graphene transistor subjected to a deliberate intro-

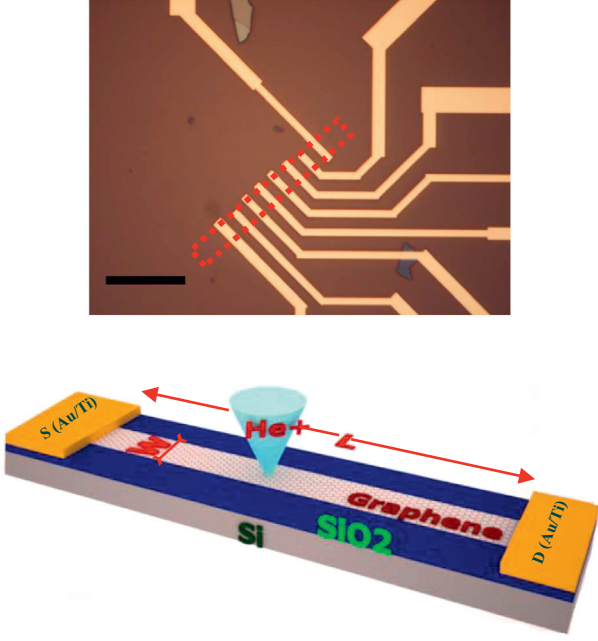
duction of point defects with precise defect concentration. We subsequently derive a circuit model for the defective graphene transistor which can be embedded in commercial circuit simulators such as Pspice.

## 2. Graphene device fabrication

Our bilayer graphene exfoliated from graphite (NGS Naturgraphit, GmbH) on a 300 nm-thick silicon oxide, which sits on a highly doped silicon substrate. The bilayer nature of our graphene flakes was determined using Raman spectroscopy and by measuring the intensity of the green component (which allows the best contrast relative to the SiO<sub>2</sub> layer) in RGB images taken by an optical microscope [12]. The graphene channels were fabricated using electron beam lithography and oxygen plasma etching. To contact the BGFET channels, we used Au and Ti (95 nm/5 nm) to define electrodes which were fabricated using electron beam lithography and a liftoff process. The device principal is sketched in Fig. 1. Prior to any electrical measurements using an Agilent B1500A Semiconductor Device Analyser, the BGFETs were annealed at 350 °C for several hours to eliminate atmospheric contamination.

The irradiation with helium ions He<sup>+</sup> was performed in high vacuum inside a helium ion microscope (Zeiss Orion) [13–16]. The acceleration voltage used was 30 kV whilst the current was kept at 1 pA. To avoid variations of contact resistance, contacts were not exposed to the He<sup>+</sup> beam and only graphene channels were irradiated. This was possible by the high precision patterning

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**Fig. 1.** The sketch of the device showing the BGFET channel, the radiating focused helium ion beam, the source, the drain and the dimensions of the channel. The highly doped silicon substrate is used as a control gate. The inset shows various transistors with different widths situated within the dashed area, and source and drain contacts. The scale bar is 15  $\mu\text{m}$ .

offered by the helium ion microscope, with a  $\text{He}^+$  beam spot size of 0.7 nm. The channels were perfectly mapped using an embedded pattern generator. The measurement were performed immediately after each irradiation run. The channels were exposed to doses of  $1.5 \times 10^{13}$  ion/ $\text{cm}^2$ ,  $2.35 \times 10^{13}$  ion/ $\text{cm}^2$  and  $4.15 \times 10^{13}$  ion/ $\text{cm}^2$ . The estimated defect concentration corresponding to these doses are  $n_d = 6 \times 10^{10}$  defect/ $\text{cm}^2$ ,  $9.4 \times 10^{10}$  defect/ $\text{cm}^2$  and  $1.66 \times 10^{11}$  defect/ $\text{cm}^2$  respectively [17,15].

### 3. Capacitance model

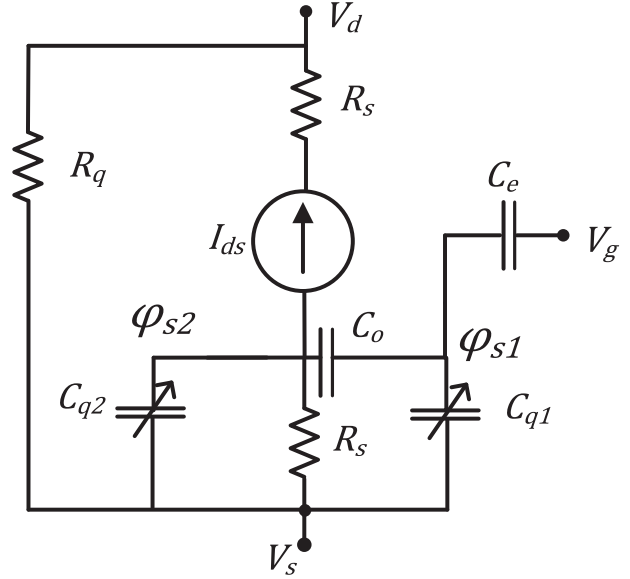
By taking into consideration the geometric structure of the BGFET, a circuit-level schematic is shown in Fig. 2. Here,  $C_e$  is the gate dielectric capacitance,  $C_o$  is the interlayer capacitance,  $C_q$  is the quantum capacitance,  $R_s$  is the contact resistance and  $R_q$  is the off-current resistance. Although both contacts are expected to have different resistances during conduction, for simplicity, an equal resistance is used.

In this work, the graphene layers are identified based on their proximity to the gate terminal. The layers are numbered in ascending order starting with the layer closest to the gate. On each layer a quantum capacitance,  $C_q$ , is present, this is a measure of the energy required to pump carriers into the channel [18]. Hence, it is a derivative of the net charge in the channel to the potential of the channel.

The varying quantum capacitance with surface potential is [19]

$$C_{qvar} = q^2 \frac{2}{\pi} \frac{q|\varphi_s|}{(\hbar v_f)^2} \quad (1)$$

where  $\varphi_s$  is the potential difference between the channel and the source terminal,  $V_s$ ,  $v_f$  is the Fermi velocity [20], electronic charge  $q$  and the reduced Plank's constant  $\hbar$ . The bilayer transistor is modelled as two single layers coupled together by capacitance  $C_o$ . As such Eq. (1) is applied to both layers of the transistor. At charge neu-



**Fig. 2.** Equivalent circuit-level diagram for a single gate graphene field effect transistor. Where  $R_q$  is the off-current resistance,  $R_s$  is the contact resistance,  $C_q$ ,  $C_o$  and  $C_e$  are the quantum capacitance, the interlayer capacitance and the gate capacitance respectively,  $\varphi_s$  is the surface potential and  $V_s$ ,  $V_g$  and  $V_d$  are the source, gate and drain voltages respectively.

trality when the density of states vanishes, a minimum carrier density,  $n_0$ , results in a capacitance

$$C_{qmin} = \frac{q^2 \sqrt{n_0}}{\sqrt{\pi} \hbar v_f} \quad (2)$$

Published works report a minimum carrier sheet density in the vicinity of  $0.5 \times 10^{12} \text{ cm}^{-2}$  at the Dirac point [21,2]. Hence, by applying the Drude model, the quantum capacitance,  $C_q$ , takes into consideration the capacitance due to both the minimum charge and the induced charge into the channel [22,23]. Thus, Eqs. (1) and (2) can be algebraically added to give

$$C_q(\varphi_s) = \frac{C_{qmin}^2 + C_{qvar}(\varphi_s)^2}{\sqrt{C_{qvar}(\varphi_s)^2 + C_{qmin}^2}} \quad (3)$$

Since graphene transport is governed by charged impurities, the Drude-Boltzmann model presents a good understanding of the channel conductivity at high charge densities [24,25]. The Drude model is used to evaluate the charge density in the channel using the relation  $n = \sqrt{n_0^2 + n[V_g]^2}$ , where  $n[V_g]$  is the charge density due to the action of the gate potential and  $n_0$  takes into consideration the residual charge in the channel at the Dirac point.

Since the transistor layout has only one gate, it will have only one threshold voltage,  $V_o$ . From Eq. (4), this threshold voltage is the gate potential at which the surface potential,  $\varphi_{s1}$  is zero.

$$V_{gs} - V_o = \varphi_{s1} \frac{C_o + C_e + C_{q1}}{C_e} - \varphi_{s2} \frac{C_o}{C_e} \quad (4)$$

The surface potentials of all layers are zero at the charge neutrality point, CNP. This implies that the threshold voltage cannot be optimised [23,12]. Graphene FET threshold voltage is still widely researched [26], whereby it has been reported that chemical doping of the graphene channel can result in a shift of the threshold voltage [26].

As the action of the gate both electrostatically dopes the channel and modulates the doping intensity, both the surface potential

and quantum capacitance of each of the layers has to be solved self-consistently in computing  $\phi_s$ .

#### 4. Carrier transport

The  $I$ - $V$  characteristic of bilayer graphene has been reported to have three regions [21,22]. For field effect transistors the gate capacitance modulates the source potential barrier. As such the net charge density is

$$Q(x) = -C_{top}(V_{gs} - V(x) - V_0) \quad (5)$$

where  $V(x)$  is the channel potential at  $x$ .  $x$  is taken from the source to the drain.  $C_{top}$  is the effective capacitance between the gate and the source.

$$C_{top} = \frac{C_e C_{q1}(C_o + C_{q2}) + C_e C_o C_{q2}}{(C_e + C_{q1})(C_o + C_{q2}) + C_o C_{q2}} \quad (6)$$

For clarity the capacitances will not be shown as a function of  $\phi_s$ . The electric field between the source and the drain drifts carriers between both terminals giving rise to drain current [27,28]

$$I_{ds} = -WQ(x)v_E(x) \quad (7)$$

where  $W$  is the channel width and  $v_E(x)$  is the carrier drift velocity. Large electric fields between the drain and source can be reached, resulting in the carriers attaining a saturation velocity. Hence, due to a field dependent mobility the drift velocity is [29–32]

$$v_E = \frac{\mu E}{1 + (\mu E/v_{sat})} \quad (8)$$

where  $E$  is the electric field between the source and drain,  $\mu$  is the carrier mobility,  $v_{sat} = \mu E_c$  is the saturation velocity,  $E_c$  is the critical electric field.

Considering a series resistance,  $R_c$ , at both the source and drain terminals, the electric potential in the channel is  $V(0) = I_{ds}R_c$  and  $V(L) = V_{ds} - I_{ds}R_c$  for the source end and drain end respectively. This makes the assumption that in Fig. 2 both series resistances are equal [33].

By applying the above equations and using an electric field of  $E = -\partial V/\partial x$ , the general current characteristics of this region is

$$I_{ds} = \frac{W\mu \int_{V(0)}^{V(L)} C_{top}(V_{gs} - V_0 - V(x))\delta V/\delta x}{\int_0^L \left[1 + \frac{\mu(-\partial V/\delta x)}{v_{sat}}\right]} \quad (9)$$

where  $L$  is the length of the active area of the channel. The turning point of the drain current with respect to the drain voltage defines the beginning of the saturation region. At the turning point  $\delta I_{ds}/\delta V_{ds} = 0$ .

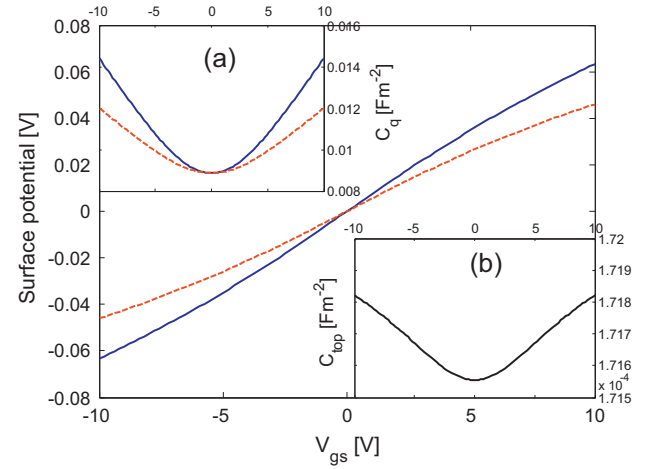
##### 4.1. Surface potential

The surface potential of both layers are plotted for a sweep of the gate voltage in Fig. 3 where a residual charge density of  $0.5 \times 10^{-12} \text{ cm}^{-2}$  [21] is used.

From Eqs. (3), (4) and (6) the behaviour of the quantum capacitance for each of the layers and their respective surface potentials is shown in Fig. 3. To accurately model the capacitance between  $V_g$  and  $V_s$  the quantum capacitance has to be taken into consideration.

##### 4.2. Transfer characteristics model

Furthermore, by solving Eq. (9) the resulting drain current during hole (sign above) and electron (sign below) conduction is [22]



**Fig. 3.** Surface potential characteristics for both the first (solid line) and second (dash line) layer against the gate voltage. Inset: (a) are the respective quantum capacitances of both the first (solid line) and second (dash line) layer against the gate voltage and (b) is the effective gate capacitance against the gate voltage.

$$I_{ds} = \frac{1}{4R_s} \left[ V_c \mp V_{ds} \pm 2\gamma \left( \frac{V_{ds}}{2} - V_{ov} \right) - \sqrt{\left( \pm V_c + V_{ds} + 2\gamma \left( \frac{V_{ds}}{2} - V_{ov} \right) \right)^2 \mp 4V_c V_{ds}} \right] \quad (10)$$

where  $V_c = Lv_{sat}/\mu$ ,  $\gamma = Wv_{sat}C_{top}R_s$ ,  $V_{ov} = V_{gs} - V_0$ ,  $v_{sat}$  is the velocity saturation,  $\mu$  is the carrier mobility and  $R_s$  is the contact resistance. The equation above approximates the carrier transport in the channel when the doped charge density is by far greater than the minimum charge density. Therefore, by fitting the experimental data against the proposed model, information about the carrier mobility ( $\mu$ ) and the contact resistance for the on-current ( $R_s$ ) can be determined.

At charge neutrality, the conductivity,  $\sigma_n$ , calculated from Eq. (10) tends to zero. To account for the drain current at the charge neutrality point (CNP), a minimum conductivity,  $\sigma_0$  is added to  $\sigma_n$  as shown in Eq. (11).

$$R_{total} = \frac{L}{W} \frac{1}{\sqrt{\sigma_0^2 + \sigma_n^2}} \quad (11)$$

Conductivity at the charge neutrality point is determined by scattering due to charged impurities, defects and dislocations in the crystal lattice. The conductivity is calculated using the relation [34–36]

$$\sigma_0 = (4q^2)/h[n_{imp}/(5n_0) + \eta]^{-1} \quad (12)$$

where  $\eta$  is a constant parameter and has a value of 0.1 for low impurity densities [34]. As the channel is bombarded with  $\text{He}^+$ , the transport characteristics changes, so does  $n_0$ . Therefore,  $n_0$  is determined using a linear equation of the form [35]

$$\sigma_n = C \left| \frac{n}{n_{imp}} \right| q + \sigma_{res} \quad (13)$$

where  $\sigma_{res}$  is the residual conductivity and  $C$  is a constant. Using this equation,  $\sigma_{res}$  is given as the point where the lines for both the hole and electron conduction meet. Hence,  $n_0$  can be computed from the expression  $\sigma_{res} = qn_0\mu$ .

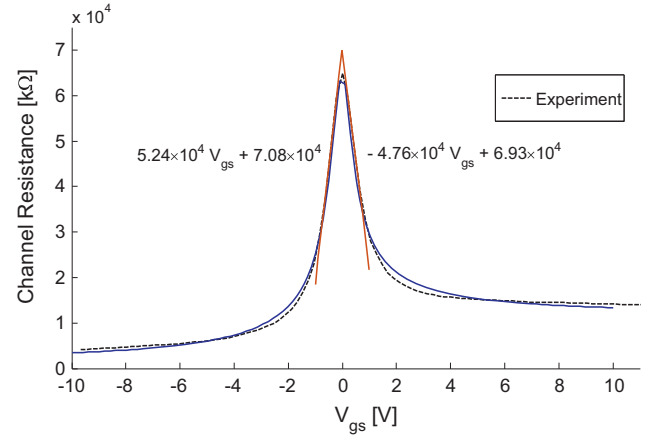
## 5. Experimental validation

Results of the measurements of the device shows an ambipolar FET as illustrated by a good conduction of both holes and electrons carriers. To extract the carrier mobility of the device, the experimental data of the transfer characteristics is fitted with the proposed model. Using a relative dielectric constant ( $\kappa$ ) of 3.9, for a thickness of 300 nm of silicon dioxide, the device has a capacitance of 11.5 nF/cm<sup>2</sup> (The value of the gate capacitance is estimated using the conventional capacitance equation,  $C_e = \kappa\epsilon_0/t_{ox}$ ).

From Fig. 1, a portion of the gate lies underneath both the source and drain contacts. Both contacts are identical with a length of 0.5  $\mu$ m. Titanium (Ti) metal exhibits a good adhesion to the graphene channel and it has been widely used in graphene FET either as the sole metal contact or as a part of a stack of metals [37,38].

In Fig. 4, The model shows a good agreement against experimental data with a peak resistance,  $R_q = 53.03$  k $\Omega$ ,  $R_s = 300$   $\Omega$  and  $\mu = 38,700$  cm<sup>2</sup>/Vs for hole conduction, and  $R_s = 5.75$  k $\Omega$  and  $\mu = 26,680$  cm<sup>2</sup>/Vs for electron conduction. Two lines are extended from both modes of conduction and from Eq. (13),  $n_0 \approx 0.3 \times 10^{11}$  cm<sup>-2</sup>. Resulting in  $n_{imp}$  of  $1.0 \times 10^{11}$  cm<sup>-2</sup>. Reported measurement using Raman data on graphene samples estimates a charge impurity of  $2.33 \times 10^{11}$  cm<sup>-2</sup> [39]. The improvement in  $n_{imp}$  can be attributed to the absence of a dielectric above the graphene channel. The estimated minimum charge density and charged impurities indicates that the sample is clean. An  $I_{on}/I_{off}$  ratio of about 20 is achieved for hole conduction and a ratio of about 3.7 is achieved for electron conduction. The off-current is measured at  $V_{gs} = 0$  V while the on-current for hole and electron conduction are measured at  $V_{gs} = -10$  V and  $V_{gs} = 10$  V respectively. This voltage range is used in all test cases in computing the on-off current. The higher on-off current ratio for hole conduction compared to electron conduction shows that the graphene channel below the contacts are doped p-type. Therefore, for electron conduction, an additional contact resistance results due to a more pronounced p-n junction formed underneath the contacts. This is illustrated in the lower carrier mobility and higher contact resistance for electron conduction as compared to hole conduction.

In Fig. 5, the FET is exposed to the first dose of He<sup>+</sup> radiation with an estimated defect density in the graphene channel of  $6 \times 10^{10}$  defect/cm<sup>2</sup>. The model shows a good fit against the experimental data with a peak resistance,  $R_q = 64.8$  k $\Omega$ ,  $R_s = 390$   $\Omega$  and

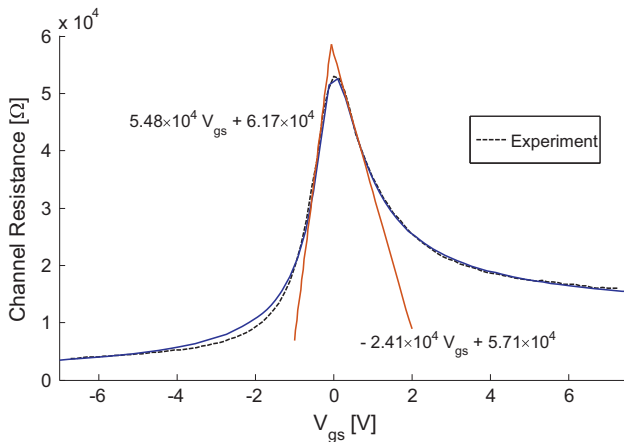


**Fig. 5.** Transfer characteristics of the channel resistance against the gate voltage for the first exposure of the channel to He<sup>+</sup> beams. The plot shows the experimental data (dash lines) against the model (solid lines). The crossing of the lines for the hole and electron conduction given by the expressions  $5.24 \times 10^4 V_{gs} + 7.08 \times 10^4$  and  $-4.76 \times 10^4 V_{gs} + 6.93 \times 10^4$  defines the point of residual conductivity.

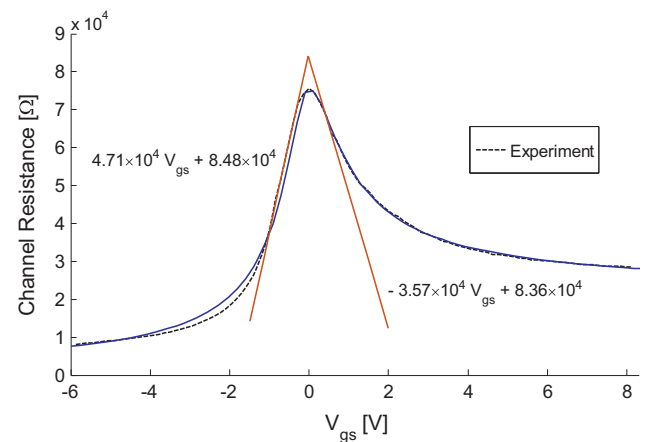
$\mu = 32,300$  cm<sup>2</sup>/Vs for hole conduction, and  $R_s = 5.74$  k $\Omega$  and  $\mu = 36,900$  cm<sup>2</sup>/Vs for electron conduction, with  $n_0$  of  $0.24 \times 10^{11}$  cm<sup>-2</sup> and  $n_{imp}$  of  $1.1 \times 10^{11}$  cm<sup>-2</sup>. An  $I_{on}/I_{off}$  ratio of about 19 is achieved for hole conduction and a ratio of about 4.85 is achieved for electron conduction.

Introducing defects in the channel increases scattering in the channel and creates regions that are not modulated by the change in the gate voltage. Thus, resulting in additional series resistance and a reduction in both the on-off current ratio and carrier mobility. On the other hand, a high on-off current ratio and carrier mobility observed for electron conduction results in a slightly decreased in  $n_0$  while  $n_{imp}$  remained unchanged. This implies that the bombardment of the channel with He<sup>+</sup> causes a strain in the graphene channel, reducing the effective mass of electrons.

In the second dose of He<sup>+</sup> radiation, a defect density of  $9.4 \times 10^{10}$  defect/cm<sup>2</sup> is estimated in the channel. By fitting the resulting experimental data against the proposed model as shown in Fig. 6, a good agreement is achieved with a peak resistance,  $R_q = 75.6$  k $\Omega$ ,  $R_s = 300$   $\Omega$  and  $\mu = 23,000$  cm<sup>2</sup>/Vs for hole conduction, and  $R_s = 11$  k $\Omega$  and  $\mu = 14,200$  cm<sup>2</sup>/Vs for electron conduc-



**Fig. 4.** Transfer characteristics of the channel resistance against the gate voltage without any exposure to He<sup>+</sup> beam. The plot shows the experimental data (dash lines) against the model (solid lines). The crossing of the lines for the hole and electron conduction given by the expressions  $5.48 \times 10^4 V_{gs} + 6.17 \times 10^4$  and  $-2.41 \times 10^4 V_{gs} + 5.71 \times 10^4$  defines the point of residual conductivity.



**Fig. 6.** Transfer characteristics of the channel resistance against the gate voltage for a second exposure of the channel to He<sup>+</sup> beams. The plot shows the experimental data (dash lines) against the model (solid lines). The crossing of the lines for the hole and electron conduction given by the expressions  $4.71 \times 10^4 V_{gs} + 8.48 \times 10^4$  and  $-3.57 \times 10^4 V_{gs} + 8.36 \times 10^4$  defines the point of residual conductivity.



tion, with  $n_0$  of  $0.3 \times 10^{11} \text{ cm}^{-2}$  and  $n_{\text{imp}}$  of  $1.7 \times 10^{11} \text{ cm}^{-2}$ . An  $I_{\text{on}}/I_{\text{off}}$  ratio of about 15.8 is achieved for hole conduction and a ratio of about 2.8 is achieved for electron conduction. A reduction in the mobility compared to the first dose of  $\text{He}^+$  radiation shows that effect due to scattering outweighs an improved mobility resulting from strain. In both cases a increase in  $R_q$  is observed.

Fig. 7 shows the transfer characteristics of the BGFET when subjected to a third dose of  $\text{He}^+$  radiation. The defect density in the channel is estimated at  $1.66 \times 10^{11} \text{ defect/cm}^2$ . Here, the model shows a good agreement against experimental data for a peak resistance,  $R_q = 145.2 \text{ k}\Omega$ ,  $R_s = 300 \Omega$  and  $\mu = 5000 \text{ cm}^2/\text{Vs}$  for hole conduction, and  $R_s = 16.7 \text{ k}\Omega$  and  $\mu = 2800 \text{ cm}^2/\text{Vs}$  for electron conduction, with  $n_0$  of  $0.8 \times 10^{11} \text{ cm}^{-2}$  and  $n_{\text{imp}}$  of  $8.7 \times 10^{11} \text{ cm}^{-2}$ . An  $I_{\text{on}}/I_{\text{off}}$  ratio of about 7.25 is achieved for hole conduction and a ratio of about 2.4 is achieved for electron conduction.

By steadily increasing the number of exposures of the graphene channel to  $\text{He}^+$  bombardment as shown in Fig. 8, there is an increase in the peak resistance. The peak resistance shows a linear relationship for the first two exposures and a much steeper slope for the third exposure. Despite a steady increase in  $R_q$ , only after the first exposure does the transistor show an improved transfer characteristic suggesting the increase in  $R_q$  was due or a reduction in the  $n_0$  and  $n_{\text{imp}}$ . Although in the experimental data the Dirac point is centred at  $V_{\text{gs}} = 0$ , the Dirac point actually shifts on exposure to  $\text{He}^+$  bombardment.

Graphene channel on  $\text{SiO}_2$  substrate have been reported to show contaminated by beam-induced hydrocarbon deposition [40,41]. Thus leaving residual conductivity after been etched by a low dose of  $\text{He}^+$ . The  $\text{He}^+$  bombardment on the graphene FET not only breaks carbon bonds but also causes disorder in the gate dielectric. As such an increase in  $R_q$  is measured for an increase in the number of exposures. From Fig. 10,  $n_0$  is a function of the  $I_{\text{on}}/I_{\text{off}}$  ratio. A decrease in  $n_0$  after the first exposure despite  $n_{\text{imp}}$  being unchanged is as a result of an improved current ratio observed for electron conduction. Measurements after the second and third exposures show a decrease in both  $n_0$  and  $I_{\text{on}}/I_{\text{off}}$  despite a steady increase in off current resistance. A strongly degraded carrier mobility is responsible for the fall in the on-off current (see inset in Fig. 8) and an increase in both  $n_0$  and  $n_{\text{imp}}$  after the second and third exposures as illustrated in Figs. 10 and 9.

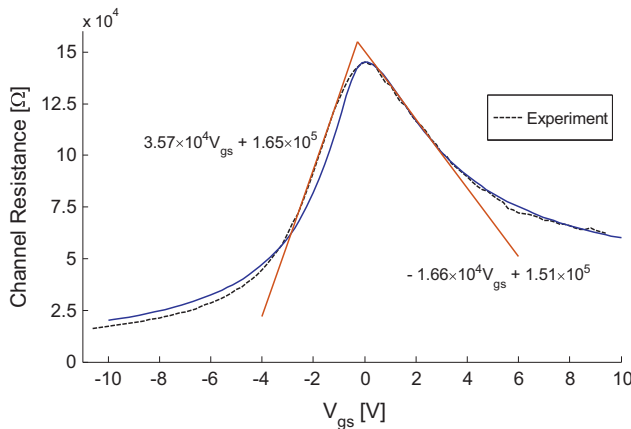


Fig. 7. Transfer characteristics of the channel resistance against the gate voltage for a third exposure of the channel to  $\text{He}^+$  beams. The plot shows the experimental data (dash lines) against the model (solid lines). The crossing of the lines for the hole and electron conduction given by the expressions  $3.57 \times 10^4 V_{\text{gs}} + 1.65 \times 10^5$  and  $-1.66 \times 10^4 V_{\text{gs}} + 1.51 \times 10^5$  defines the point of residual conductivity.

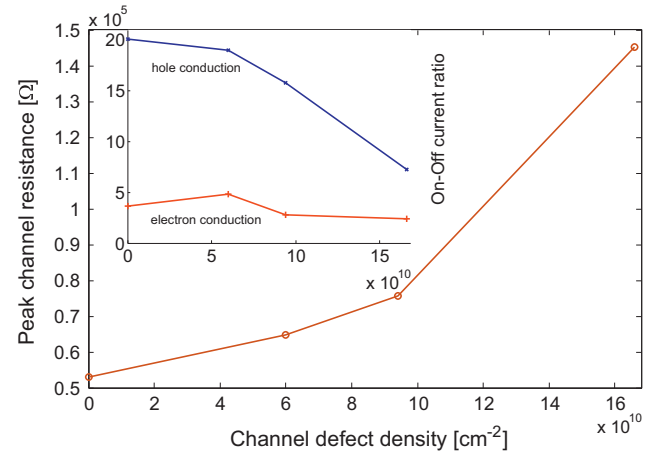


Fig. 8. The peak channel resistance against the number of exposures of the FET to  $\text{He}^+$  beams. Inset are the on-off current ratios for both the hole and electron conduction against the number of  $\text{He}^+$  exposures of the channel.

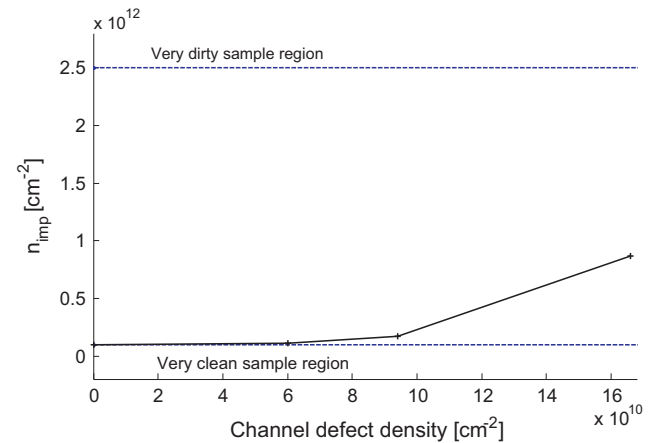


Fig. 9. The density of impurity charges as a function of the number of  $\text{He}^+$  bombardment of the graphene channel.

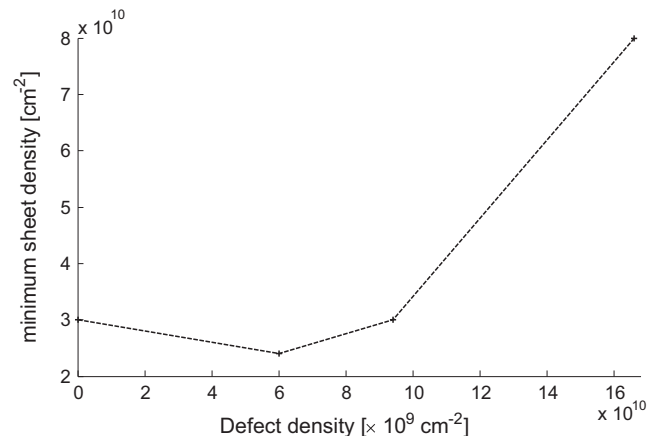


Fig. 10. The residual sheet charge density against  $\text{He}^+$  induced defects in the graphene channel.

## 6. Conclusion

In this paper we presented the transfer characteristics of a single-gate bilayer graphene FET with defects in the crystal lattice. Point defects were introduced by exposing the channel to a helium ion beam using a high precision He<sup>+</sup> microscope. All measurements were carried out ex-situ. To understand the behaviour of the BGFETs, a model was developed to characterise the transistor which shows a good agreement when validated against the experimental data of the device transfer characteristics.

Prior to the introduction of defects, the charged impurity density value indicates that the fabricated samples are clean. After the first exposure, the electron branch showed an improved on-off current ratio while the hole branch remain relatively unchanged and also with an unchanged charge impurity level. The improved transfer characteristics results from a lower minimum charge density. This phenomenon may be due to an increase in the strain on the channel.

Subsequent exposure to He<sup>+</sup> beam leads to a further increase in the peak resistance, but unlike the first exposure, the transistor shows a decrease in the carrier mobility and an increase in the contact resistance. The impurity charge density increases from a clean sample to a dirty sample after the third exposure.

The developed model allows various parameters extraction of bilayer transistor and can be implemented in circuit level simulators.

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