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Agenda item: 8.1.4.3
Source: AccelerComm
Title: Enhanced turbo codes for URLLC
Document for: Discussion

I. INTRODUCTION

The following channel coding simulation assumptions have been agreed for the Ultra Reliable Low Latency Communication (URLLC) scenario [1].

Agreements: Simulation assumptions : URLLC and mMTC

- Evaluate BLER performance versus SNR

Channel*	AWGN			
Modulation	QPSK, 16 QAM			
Coding Scheme	Convolutional codes	LDPC	Polar	Turbo
Code rate	1/12, 1/6, 1/3			
Decoding algorithm**	List-X Viterbi	min-sum	List-Y	Max-log-MAP
Info. block length*** (bits w/o CRC)	20, 40, 200, 600, 1000			
* Fading channels will be simulated in the next stage ** These algorithms are starting points for further study. Other variants of agreed algorithms can be used for encoding and decoding (Complexity details should be illustrated) *** At least these info. block length and code rate shall be evaluated. Other info. block lengths and code rates are not precluded. Similar info and encoded block lengths should be used for the evaluation. Total coded bits = info. Block length/code rate. Note: these info. block length and code rate are only for initial performance evaluations. They are not interpreted as design targets or assumptions for complexity analysis.				

- General guidelines
  - Existing code constructions can be used for evaluation
  - Whenever feasible, performance comparison should adopt coding constructions with matching computational complexities
  - BLER simulations down to 10^{-4} is recommended (to observe the error floor) for URLLC

This paper presents Block Error Ratio (BLER) performance results for the enhanced turbo code of [2], as included in the attached spreadsheet and as implemented in the attached Matlab code. These BLER results are compared with corresponding results for the Low Density Parity Check (LDPC) code of [3] and the Parity Check (PC)-polar code of [4]. The computational complexity and decoding latency of these codes are also compared.

II. BLER PERFORMANCE

Figure 1 plots the BLER performance of the enhanced turbo code of [2], for code rates of $R \in \{1/12, 1/6, 1/3\}$ and information block lengths of $K \in \{32, 80, 208, 400, 992\}$ bits, when using Quaternary Phase Shift Keying (QPSK) modulation for transmission over an Additive White Gaussian Noise (AWGN) channel. Likewise, Figure 2 provides the corresponding results for the case of using 16-ary Quadrature

Amplitude Modulation (16QAM). In all plots, $I = 8$ iterations of scaled Max-Log-MAP (MLM) decoding with a scaling factor of 0.75 is assumed. Before commencing the first decoding iteration, short forward and backward recursions are performed within the 10 trellis stages at either end of the trellises used by the upper and lower decoders, in order to warm-up the tail-biting.

As shown in Figures 1 and 2, the enhanced turbo code does not exhibit any error floors for BLERs down to 10^{-4} for any of the combinations of modulation, code rate and information block length considered for URLLC scenarios.
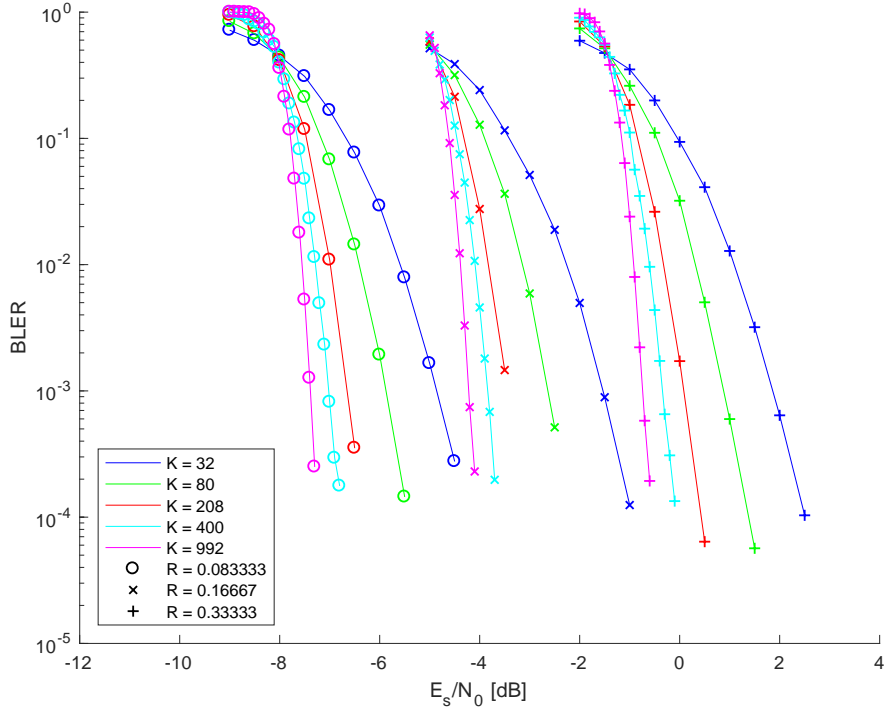

Fig. 1. BLER performance of enhanced turbo code for $K \in \{32, 80, 208, 400, 992\}$, $R \in \{1/12, 1/6, 1/3\}$, QPSK modulation and AWGN channel.

Observation 1: The enhanced turbo code does not exhibit any error floors for BLERs down to 10^{-4}.

Figure 3 plots the Signal to Noise Ratio (SNR) values required in Figure 1 to achieve a BLER of 10^{-3}. These results are compared with the corresponding results provided in [5] for LDPC and PC-polar codes that are designed for URLLC scenarios. More specifically, [5] considers the LDPC code of [3] employing scaled Normalised Min-Sum (NMS) decoding with $I = 25$ iterations, as well as the PC-polar code of [4] employing Successive Cancellation List (SCL) decoding with a list size of $L = 8$. As shown in Figure 3, the enhanced turbo code of [2] offers superior BLER performance to both the LDPC code of [3] and the PC-polar code of [4], at all combinations of code rate and information block length considered for URLLC scenarios.

Observation 2: The enhanced turbo code offers superior BLER performance to LDPC and PC-polar codes that are designed for URLLC scenarios.

III. COMPUTATIONAL COMPLEXITY

As discussed in [6] and illustrated in Figure 4, the computational complexity of the enhanced turbo decoder remains constant for all code rates R. By contrast, the computational complexity of LDPC
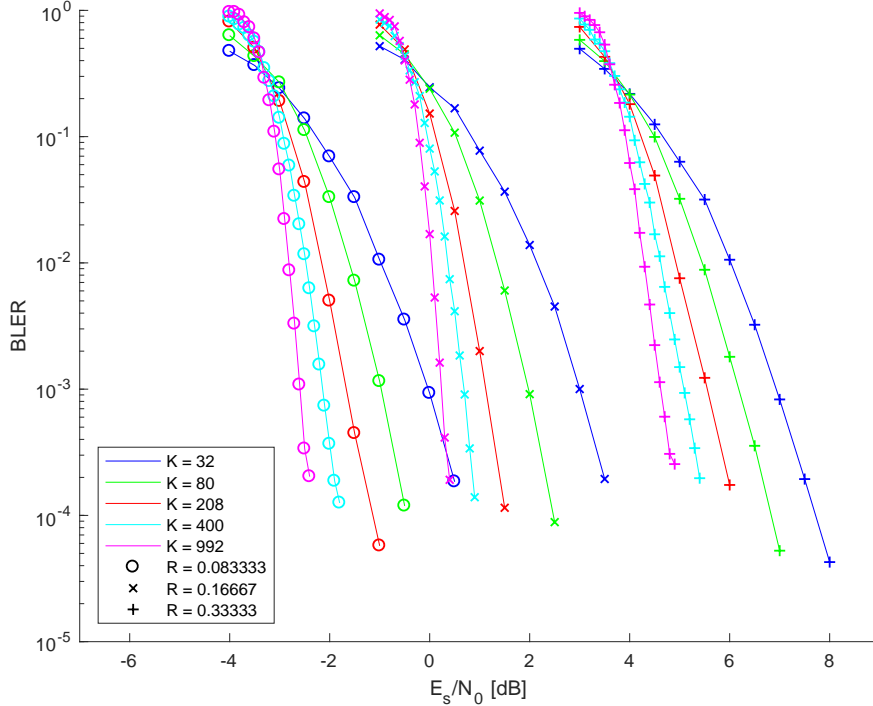
Fig. 2. BLER performance of enhanced turbo code, for $K \in \{32, 80, 208, 400, 992\}$, $R \in \{1/12, 1/6, 1/3\}$, 16QAM modulation and AWGN channel.

and PC-polar decoders increase at the low code rates of URLLC scenarios. As shown in Figure 4, the enhanced turbo decoder employing scaled MLM decoding with $I = 8$ iterations has a lower computational complexity than the LDPC decoder of [3] employing scaled NMS decoding with $I = 25$ iterations, at all code rates R considered in URLLC scenarios. Indeed, the computational complexity of the enhanced turbo code is an order of magnitude lower than that of the LDPC code at a code rate of $R = 1/12$. Likewise, at a code rate of $R = 1/12$, the enhanced turbo decoder has a lower computational complexity than the PC-polar decoder of [4] employing SCL decoding with a list size of $L = 8$.

Note that in order to avoid the high computational complexity of LDPC codes at low code rates R, it has been agreed that the LDPC code for enhanced Mobile BroadBand (eMBB) data will use a mother code rate of $R = 1/5$, with circular buffer repetition for lower code rates [7]. However, this may be expected to compromise the BLER performance at these lower code rates, rendering the eMBB data LDPC code unsuitable for use in URLLC scenarios, where low codes rates are particularly important.

Observation 3: The enhanced turbo decoder has lower computational complexity than LDPC decoders at all code rates considered in URLLC scenarios. The enhanced turbo decoder has lower computational complexity than PC-polar decoders at the lowest code rates considered in URLLC scenarios.

Observation 4: The eMBB data LDPC code is likely to be unsuitable for use in URLLC scenarios.

IV. DECODING LATENCY

The turbo decoder Application Specific Integrated Circuit (ASIC) of [8] can flexibly decode all 188 information block lengths K supported by the LTE turbo code. It operates on the basis of $P = 8$ parallel radix-2 processors, which each perform the MLM forwards and backwards recursions simultaneously, for a different window comprising K/P trellis stages. Each half-iteration therefore requires K/P clock cycles, requiring a total of $2IK/P$ clock cycles to complete I decoding iterations. When $I = 8$ iterations are
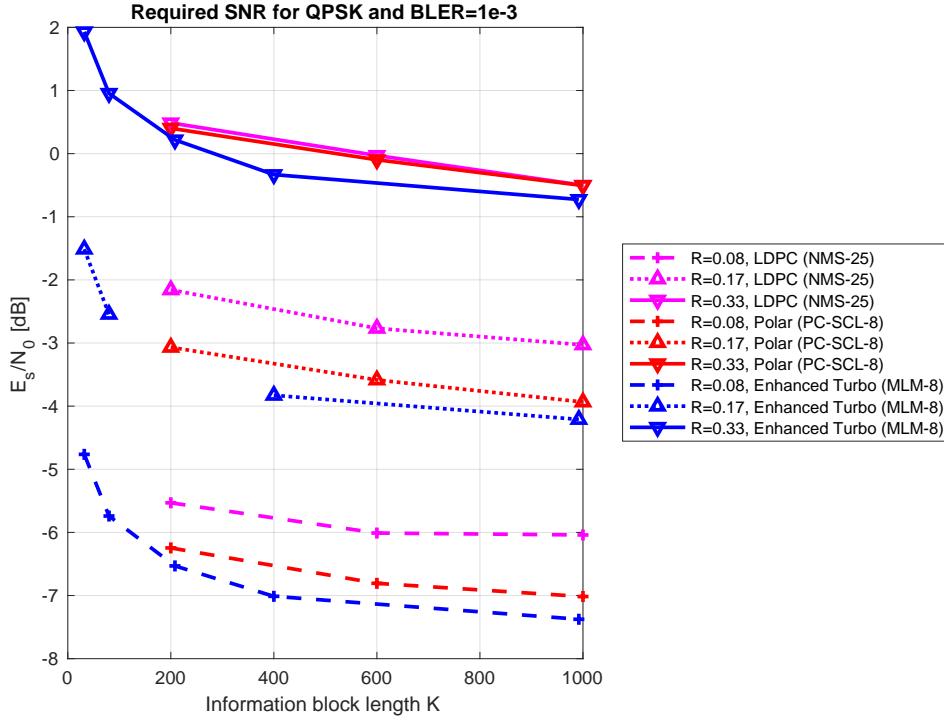
Fig. 3. SNR required to achieve a BLER of 10^{-3} for enhanced turbo, LDPC and PC-polar codes, for QPSK modulation and AWGN channel.

performed, a total of 2 clock cycles are therefore required per information bit. Using 90 nm technology, the ASIC of [8] achieves a clock frequency of 625 MHz, leading to a decoding latency of 3.2 ns per information bit. For the maximum information block length of $K = 1000$ considered in URLLC scenarios, the corresponding decoding latency is 3.2 μs. Note however that lower latencies may be expected by employing a lower ASIC technology scale, using radix-4 processors, using a greater number P of parallel processors and/or using shuffled turbo decoding [9] (wherein the upper and lower decoders are operated simultaneously). Regardless, 3.2 μs is sufficient to meet the strictest latency requirement for URLLC scenarios, which is quantified as 4.66 μs in [10]. Note that it may be expected that the strictest latency requirements of URLLC scenarios can also be met by ASIC implementations of the enhanced turbo decoder, since its enhancements relative to the LTE turbo decoder do not affect the number of information bits per clock cycle that it can recover. Furthermore, these enhancements do not affect the critical clock frequency, since the modifications required to natively support lower code rates can be readily pipelined, leaving the critical path length unchanged and unmoved from the forward and backward recursions.

Note that [10] suggests that the strictest latency requirements of URLLC scenarios cannot be met by PC-polar codes and that they can only be met by LDPC decoders when using row parallel decoding and for a code rate of $R = 1/3$.

Observation 5: The enhanced turbo decoder can meet the strictest latency requirements of URLLC scenarios.

V. CONCLUSIONS

This paper has characterised the BLER performance, complexity and decoding latency of the enhanced turbo code of [2]. These have been compared with those of the LDPC code of [3] and the PC-polar code of [4].

Observation 1: The enhanced turbo code does not exhibit any error floors for BLERs down to 10^{-4}.
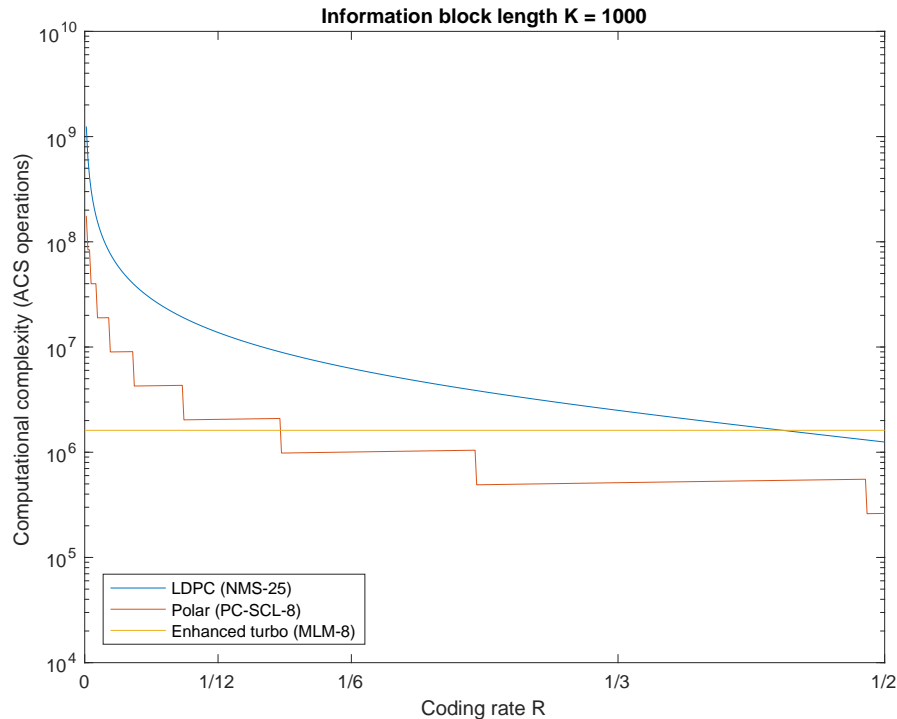
Fig. 4. Computational complexity for enhanced turbo, LDPC and PC-polar decoders.

Observation 2: The enhanced turbo code offers superior BLER performance to LDPC and PC-polar codes that are designed for URLLC scenarios.

Observation 3: The enhanced turbo decoder has lower computational complexity than LDPC decoders at all code rates considered in URLLC scenarios. The enhanced turbo decoder has lower computational complexity than PC-polar decoders at the lowest code rates considered in URLLC scenarios.

Observation 4: The eMBB data LDPC code is likely to be unsuitable for use in URLLC scenarios.

Observation 5: The enhanced turbo decoder can meet the strictest latency requirements of URLLC scenarios.

Proposal 1: Enhanced turbo codes are selected for URLLC scenarios.

REFERENCES

[1] Chairman, "R1-163961 Final Report," in *3GPP TSG RAN WG1 #84bis*, Apr. 2016.
[2] IMT, "R1-1612938 Enhanced Turbo Codes for NR: Performance Evaluation for eMBB and URLLC," in *3GPP TSG RAN WG1 #87*, Nov. 2016.
[3] Qualcomm, "R1-1610137 LDPC rate compatible design overview," in *3GPP TSG RAN WG1 #86bis*, Oct. 2016.
[4] Huawei, "R1-1608862 Polar Code Construction for NR," in *3GPP TSG RAN WG1 #86bis*, Oct. 2016.
[5] CATT, "R1-1700243 Performance comparison of LDPC and polar codes for URLLC," in *3GPP TSG RAN WG1 AH NR*, Jan. 2017.
[6] AccelerComm, "R1-1612306 On the hardware implementation of channel decoders for short block lengths," in *3GPP TSG RAN WG1 #87*, Nov. 2016.
[7] Chairman, "Draft Report," in *3GPP TSG RAN WG1 AH NR*, Jan. 2017.
[8] R. Shrestha and R. P. Paily, "High-throughput turbo decoder with parallel architecture for LTE wireless communication standards," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 9, pp. 2699–2710, Sept 2014.
[9] J. Zhang and M. P. C. Fossorier, "Shuffled iterative decoding," *IEEE Trans. Commun.*, vol. 53, no. 2, pp. 209–213, Feb 2005.
[10] Samsung, "R1-1700981 Discussion on Channel Coding for URLLC Channel," in *3GPP TSG RAN WG1 AH NR*, Jan. 2017.