Single Carrier Trapping and De-trapping in Scaled Silicon Complementary Metal-Oxide-Semiconductor Field-Effect Transistors at Low Temperatures

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Abstract.

The scaling of Silicon (Si) technology is approaching the physical limit, where various quantum effects such as direct tunnelling and quantum confinement are observed, even at room temperatures. We have measured standard Complementary Metal-Oxide-Semiconductor Field-Effect-Transistors (CMOSFETs) with wide and short channels at low temperatures to observe single electron/hole characteristics due to local structural disturbances such as roughness and defects. In fact, we observed Coulomb blockades in sub-threshold regimes of both *p*-type and *n*-type Si CMOSFETs, showing the presence of quantum dots in the channels. The stability diagrams for the Coulomb blockade were explained by the potential minima due to poly-Si grains. We have also observed sharp current peaks at narrow bias windows at the edges of the Coulomb diamonds, showing resonant tunnelling of single carriers through charge traps.

1. Introduction

Silicon (Si) industry is seeking for a new disruptive application in quantum technologies by using the platform of existing infrastructure to fabricate scaled complementary-metal-oxide-semiconductor field-effect-transistors (CMOSFETs). According to International Technology Roadmap for Semiconductors 2.0 (ITRS 2.0) [1,2], which was issued in 2015 to replace the previous ITRS, the single electron transistor (SET) is considered strong candidates for RF-mixers [1, 3, 4], which is an important part of RF front end. SETs are based on sequential single electron tunnelling [5] through two tunnelling barriers and a quantum dot with small self-capacitor [6, 7]. By changing the bias condition, the single electron sequential tunnelling is either unblocked or blocked, and SETs are controlled between on and off states, accordingly [8].

In the early stage of the research, scientists used metal [6,9] or III-V semiconductor [10,11] as materials to study the characteristics of SETs and single electron phenomena. From the manufacturing point of view, Silicon (Si) SETs have their advantages due to the compatibility with CMOS fabrication technology [12]. Si-based SETs have already been demonstrated [13–15]. However, we must design complicated device structures with quantum confinement using dedicated processes, such as nanowire-defined dots [16], top gates [17], and side gates [18], which increases the complexity of fabrication. Besides complicated structures, the feature size must be comparable to or smaller than the thermal de Broglie length of single electrons to maintain a larger charging energy than thermal energy [19]. For the standard CMOSFETs, the fabrication processes are well established, and the minimum feature size of CMOSFETs were as small as 14nm [20] in 2014, which is already smaller than the thermal de Broglie length of 17nm for electrons in Si at 300K. Therefore, we should observe various quantum mechanical effects in conventional CMOSFETs. For example, random telegraph noise based on single electron trapping is a serious issue to secure reliabilities [21–24]. The purpose of this work is to investigate and establish the relationship between scaled Si CMOSFETs and Si SETs. Previously, the SET characteristics of Si nanowire FinFETs on SOI were observed at room temperatures [25, 26], and low temperatures [27–29]. But, the single electron phenomena in conventional CMOSFETs based on bulk Si at low temperatures has not been fully investigated.

2. Experiments

The MOSFETs were fabricated by using a standard 65nm technology node. The wide channel width of 10μm was chosen to increase the chance to observe single carrier trapping and de-trapping phenomena. The channel length was 55nm/75nm for pMOSFET/nMOSFET, respectively. The gate electrode was made of doped poly-crystalline silicon (poly-Si). The gate dielectric material was SiON with the Equivalent Oxide Thickness (EOT), t_{ox}, of 2.4nm. The value of current at each bias was obtained by averaging over 10^5 data points each with a duration of 2μs.

3. Results

The drain current (I_d) on the gate bias (V_g) characteristics of the two MOSFETs were measured at 300K and 5K respectively, as shown in figure 1, at the drain bias (V_d) of $\mp$50mV.

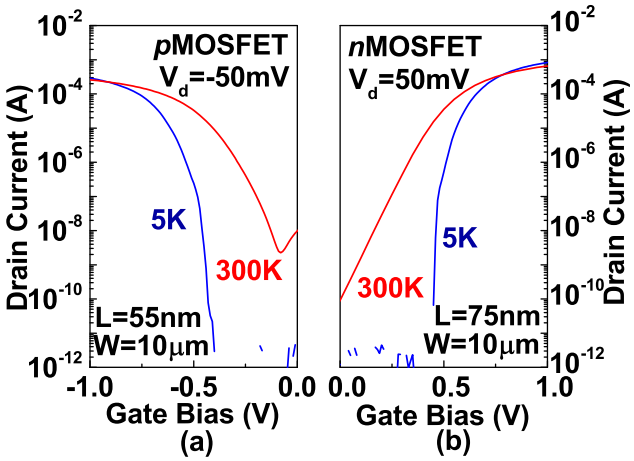

Figure 1: Subthreshold characteristics for (a) pMOSFET and (b) nMOSFET at the temperatures 300K and 5K. The threshold voltages were shifted when the devices were cooled down.

The threshold voltages were -0.45V/0.47V at 300K and -0.60V/0.62V at 5K, for pMOSFET/nMOSFET, respectively (figure 1). The on-currents were larger for both pMOSFET and nMOSFET at 5K, because of the increase in mobility [30] and the increase of the saturation velocity [31]. The sub-threshold slopes were 14.9mV/decade for pMOSFET and 5.7mV/decade for nMOSFET at 5K, while they were 82.4mV/decade for pMOSFET and 80.3mV/decade for nMOSFET at 300K. The off-current was below our detection limit ($\sim$1pA) at 5K. In the sub-threshold regime at 5K, the channel resistance of both pMOSFET and nMOSFET were larger than 25.8kΩ, which was a necessary condition of observing single-electron effects in SETs.

In fact, we observed typical SET characteristics at 5K, as shown in figure 2.

The dependences of the I_d-V_d characteristics upon changing the V_g implies the presence of a quantum dot in the channel of both devices. In figure 2 (a), at V_g

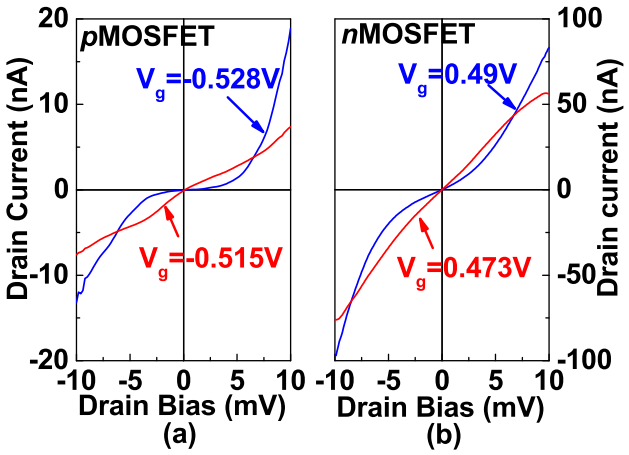

Figure 2: Coulomb blockade in (a) *p*MOSFET and (b) *n*MOSFET at 5K. The gate was biased at -0.528V (OFF state) and -0.515V (ON state) for *p*MOSFET, and was biased at 0.473V (ON state) and 0.49V (OFF state) for *n*MOSFET.

of -0.528V, $I_{\rm d}$ of the *p*MOSFET was blocked in the $V_{\rm d}$ range between -2.5mV and 2.5mV, while $I_{\rm d}$ was not blocked at $V_{\rm g}$ of -0.515V. The similar Coulomb blockade behaviour was also observed in *n*MOSFET (figure 2(b)).

We measured $I_{\rm d}$ in more detail by changing both $V_{\rm g}$ and $V_{\rm d}$ to check the single carrier trapping and de-trapping characteristics, as shown in the two-dimensional (2D) contour plot of $I_{\rm d}$ (figure 3). Several Coulomb diamonds were found in *p*MOSFET while only one Coulomb diamond was found in *n*MOSFET. Different Coulomb diamonds, which corresponded to different hole/electron states in a quantum dot, are marked as H0, H1, H2, H3 in figure 3 (a) and E0, E1 in figure 3 (b). In figure 3 (a), the size of Coulomb diamond shrinks as $|V_{\rm g}|$ was increased. It means that the coupling capacitance of quantum dot was changed as we changed $V_{\rm g}$. This is a marked difference from the standard characteristics predicted by the conventional mesoscopic model of metallic tunnelling junction [32], in which all coupling capacitance in equivalent circuit are fixed. In figure 3 (b), only one diamond was observed in the current map of *n*MOSFET. *n*MOSFET showed similar behaviour to *p*-MOSFET. The Coulomb diamond was observed when $V_{\rm g}$ is between 0.47V and 0.51V. Above 0.51V where the coupling resistance becomes smaller than quantum resistance, no diamond was observed.

When $V_{\rm g}$ was larger than 0.47V, the Coulomb diamond started to be observed. The diamond was not observed at 0.51V where the coupling resistance became smaller than quantum resistance.

By comparing *p*MOSFET with *n*MOSFET (figure 2), we found that $I_{\rm d}$ in *n*MOSFET was almost

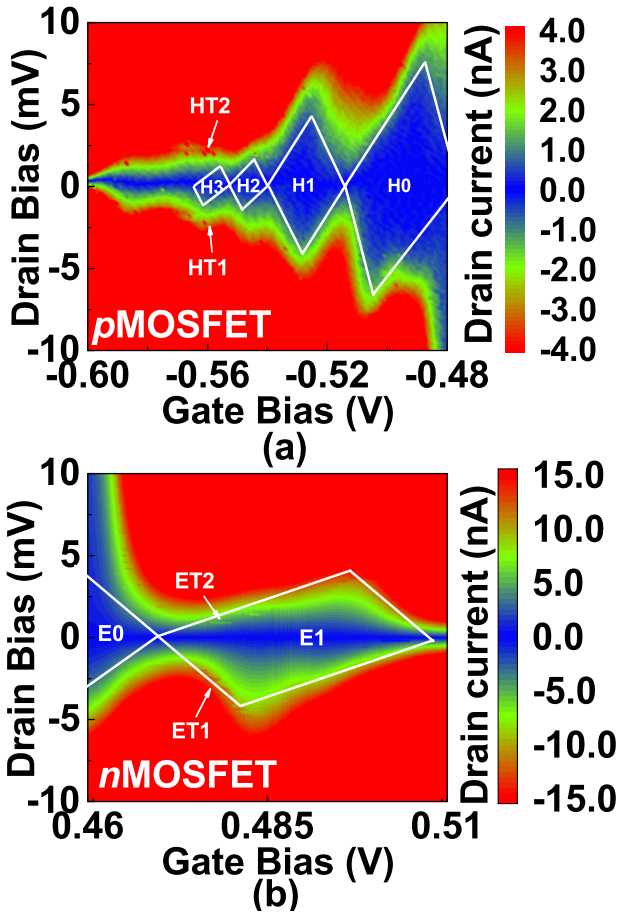

Figure 3: Contour plot of drain current versus gate voltage and drain voltage in (a) *p*MOSFET and (b) *n*MOSFET at 5K. The border of the Coulomb diamonds are determined by fitting with the standard mesoscopic model.

three times larger than that in *p*MOSFET. This may be explained by the mobility difference between the electrons and holes. The single electron/hole tunnelling event was only observable in corresponding sub-threshold region in the figure 1.

We also found that current peaks at the edges of Coulomb diamond for both devices. At narrow bias windows, which are marked as Hole Traps (HT1 and HT2) in figure 3 (a), and Electron Traps (ET1, ET2) in figure 3 (b), the current exhibited sharp peaks. The sharp current peaks were found at the edge of the Coulomb diamond blockade region in both figure 3 (a) and figure 3 (b).

4. Discussion

The standard mesoscopic model was used to estimate parameters for SETs [33], as shown in figure 4 (a). The carrier concentration was around 10^{10}~10^{12}cm^{-2} in Si

two-dimensional electron gas [34], which corresponds to 10∼100nm electron-electron distance. This is on the same magnitude as thermal de Broglie length of electron in Si at 5K, 133nm, and much larger than the Bohr radius in Si, 5.2nm. Under this condition, the electrons trapped in quantum dot can be treated as non-interactive electrons [35].

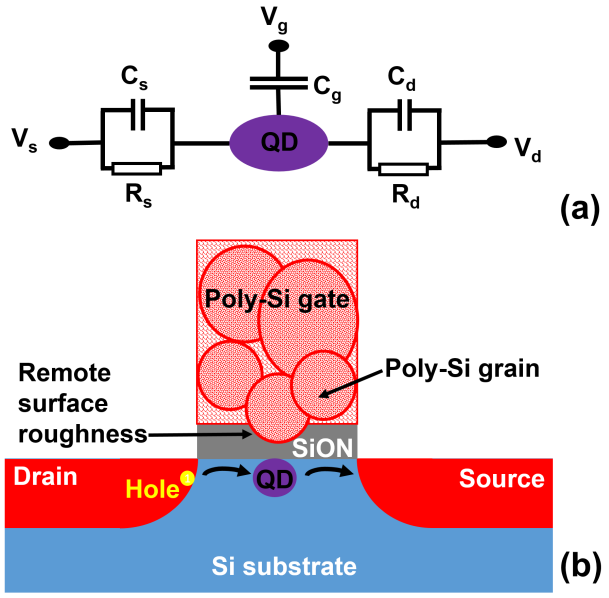

Figure 4: Circuit model and physical model of the quantum dot. (a) shows the standard equivalent circuit model and (b) shows a schematic diagram of the assumed remote poly-Si roughness for the quantum dot structure.

At the sub-threshold regime, the channel current is dominated by single hole/electron transistor current. Therefore, the carrier concentration can be approximately estimated:

$$N_{\text{channel}} = \frac{1}{WL} = 1.8 \times 10^{8}\text{cm}^{-2}. \quad (1)$$

In this weakly inverted condition, the impact of poly-Si depletion layer is negligible.

However, the inversion layer thickness caused by quantum confinement near the SiON/Si interface cannot be neglected. The inversion layer thickness, t_{inv}, is ∼2nm [34,36,37]. Therefore, the total capacitive effective thickness is

$$t_{\text{eff}} = t_{\text{ox}} + \frac{\varepsilon_{\text{ox}} t_{\text{inv}}}{\varepsilon_{\text{Si}}} = 3.1\text{nm}, \quad (2)$$

where ε_{ox} is the dielectric constant of SiO_2 and ε_{Si} is the dielectric constant of Si.

The coupling capacitances of each hole state shown in figure 3 (a) were different. As $|V_{\text{g}}|$ increased, more holes were occupied in the quantum dot. The gate coupling capacitance (C_{g}), source coupling capacitance (C_{s}), and drain coupling capacitances (C_{d}) to the quantum dot also increased. This implies that the coupling capacitances were connected to the inversion layer capacitance [38]. If $|V_{\text{g}}|$ increased after depletion layer reached its maximum width, the channel would start to be inverted. Therefore, both inversion layer capacitance per unit area [39], C_{inv}, and oxide capacitance per unit area, C_{ox}, contributed to C_{g} as shown in

$$\frac{1}{C_{\text{g}}} = \frac{1}{C_{\text{ox}} S} + \frac{1}{C_{\text{inv}} S}, \quad (3)$$

where S was the area of the quantum dot. We can extract C_{g} from the periodicity of Coulomb oscillations related to each Coulomb diamond, ΔV_{g},

$$C_{\text{g}} = \frac{e}{\Delta V_{\text{g}}}. \quad (4)$$

The extracted capacitances of *p*MOSFET and *n*MOSFET are shown in table 1 and 2, respectively. In H3, V_{g} was about -0.56V, which was quite close to the threshold voltage of *p*MOSFET. The carrier density in H3 C_{inv} was much higher than that in H0, H1 and H2. Therefore, C_{inv} in H3 would be the largest compared with H0, H1 and H2. Since C_{inv} was the largest, here we assume that the dominant contribution to C_{g} would be C_{ox} in H3, and neglect the contribution of C_{inv}. We can estimate the size of the quantum dot from C_{g} in H3, $C_{\text{g}}(H3)$, based on this approximation. If we assume the quantum dot is a circle, we can caculate the diameter, d,

$$d = \sqrt{\frac{4C_{\text{g}}(H3)}{\pi \varepsilon_{\text{ox}}/t_{\text{eff}}}} = 38.5\text{nm}. \quad (5)$$

The inversion layer capacitance in table 1 was extracted by assuming the diameter of the quantum dot in *p*MOSFET was 38.5nm.

Table 1: Coupling capacitance using mesoscopic model for *p*MOSFET

Diamond	H3	H2	H1	H0
Gate Capacitance (aF)	13.4	12.6	6.2	4.2
Drain Capacitance (aF)	34.7	33.8	15.8	6.4
Source Capacitance (aF)	62.0	52.8	22.8	10.7
Inversion Layer Capacitance (aF)	N/A	211.1	11.5	6.1
Charging Energy (meV)	1.5	1.6	3.6	7.5

Table 2: Coupling capacitance using mesoscopic model for *n*MOSFET

Diamond	E1
Gate Capacitance (aF)	4.2
Drain Capacitance (aF)	11.6
Source Capacitance (aF)	23.5
Charging Energy (meV)	4.1

The charging energy in H0 was 7.5meV for *p*MOSFET, much smaller than the value reported in single dopant transistor [26, 28, 40], which is roughly 30meV. Therefore, it is unlikely that the quantum dots were made of impurities in the channel due to the large size of the quantum dot. It implies that the quantum dots in both *p*MOSFET and *n*MOSFET come from physical structures defined by the surface roughness or poly-Si grains [41]. Grain boundaries of poly-Si cause remote surface roughness at poly-Si/SiON interface, as shown in figure 4 (b). The remote surface roughness at poly-Si/SiON interface results in local variations of equivalent oxide thickness [42, 43]. This forms a dip of surface potential near the interface of grain boundary area, and single carriers would be confined near the peak region. The dimension of poly-Si grains can be around 50nm [44], which is comparable with the size of the quantum dot that we estimated from *p*MOSFET. If poly-Si grains were responsible for this Coulomb blockade phenomena, we should only be able to observe SET characteristics if the channel length is comparable with the size of poly-Si grains. Otherwise, the currents are superpositions of various channels through multiple connections of SETs.

The increase of drain and source coupling capacitance upon increasing $|V_g|$ (table 1) can be explained by the changes of tunnelling barrier height and the forming of an inversion layer. The barrier height was continuously reduced when we increased $|V_g|$, and the capacitive coupling between source and drain also became stronger [45]. As a result, the Coulomb diamond shrinks significantly. The formation of inversion layer also contributed to the shrink of the Coulomb diamond. When $|V_g|$ was large enough to invert the channel, the inversion layer was initially formed around the source region [39]. When $|V_g|$ increased and the channel was inverted further, inversion layer started to expand from source to drain.

Next, we discuss about current peaks observed at the edges of the Coulomb diamond region. In order to analyse the current peak in detail, we plotted the I_d-V_d characteristics and the current map near the noise region in figure 5.

The current peak was only observable at a very narrow window in bias condition. In figure 5 (a), at V_g of -0.561V, a current peak is clearly observed if V_d was at -4mV. When V_g was at -0.559V and -0.574V, the peak was not observed. The fact that current peaks were found at the edge of the Coulomb diamonds implies that the current peaks were related to charge traps. The window of bias condition to observe this current peak is much narrower than the bias condition to observe Coulomb diamonds. This sharp current peak implies that the energy level broadening must be small in the charge trap, and resonant

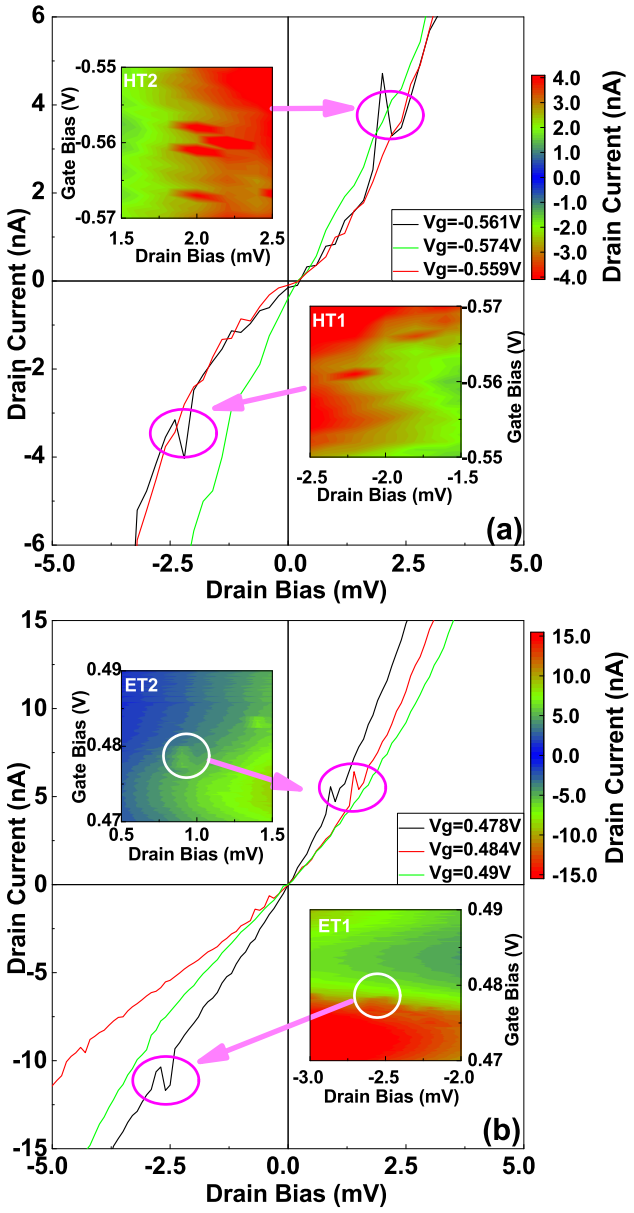

Figure 5: Sharp current peaks observed at the edges of Coulomb diamond. The current peaks are shown in both current map and I_d - V_d characteristics. (a) indicates the influence of a single charge trap in *p*MOSFET with different gate bias. (b) shows the influence of a single charge trap in *n*MOSFET with different gate bias.

tunnelling was responsible for this phenomena. We were able to observe similar phenomenon in figure 5 (b), showing similar characteristics in the *n*MOSFET. More investigation is needed to identify the nature of these current peaks.

5. Conclusion

We observed single carrier trapping and de-trapping phenomena by measuring standard short-channel MOSFETs at low temperatures. We observed single hole/electron tunnelling phenomena at sub-threshold regions in both standard *p*-type and *n*-type short-channel MOSFETs. The size of the Coulomb diamond was shrinking with decreasing gate bias in *p*-MOSFET. The quantum dot corresponding to the Coulomb diamond was considered to have originated from the potential minimum created by the poly-Si grains. We also observed current peaks at the edge of Coulomb diamond at certain bias conditions. The current peaks were considered to have originated from the charge traps, which will potentially link reliability issues in advanced MOSFETs. Therefore, the low temperature measurements will be useful to investigate the single carrier trapping and de-trapping process in MOSFETs, which will help in understanding the quantum effects and pave the way to establish the relationship between scaled Si CMOSFETs and Si SETs.

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