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A Full Wafer Dicing Free Dry Release Process for MEMS Devices

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Abstract

This paper presents a full wafer, dicing free, dry release process using hydrofluoric acid (HF) vapour phase etching (VPE) for MEMS sensors and actuators fabricated using silicon on insulator (SOI) wafers. It is particularly beneficial to MEMS sensors whose performance benefits from a large proof mass, for example accelerometers and gyroscopes. Such a fabrication method was first proposed by Overstolz *et al.* where the wafer level release steps for a tilting platform measuring $2 \times 2 \text{ mm}^2$ were presented [1]. In the work described here, the process is extended to the full wafer release of an accelerometer with a large proof mass measuring $4 \times 7 \text{ mm}^2$. The sensor was successfully fabricated with a yield of over 95%.

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Keywords: HF VPE; dry release; dicing free release; DRIE; MEMS; micro fabrication; accelerometer.

1. Introduction

For many MEMS sensors the size of the proof mass is directly proportional to crucial performance characteristics such as noise floor and scale factor. For ultra-high performance inertial sensors a large, free-standing proof mass is therefore required. A fabrication process using Silicon on Insulator (SOI) wafers based on deep reactive ion etching (DRIE) is usually the preferred choice. However, typical SOI processes described in the literature [2-3] are not directly applicable for a proof mass larger than 2-3 mm on each side as the release of the free standing structure is difficult to achieve.

The aim of this work is to develop a fabrication process for an accelerometer with a large proof mass of $4 \times 7 \text{ mm}^2$. For this purpose a dicing free and dry release method for SOI wafers was developed and successfully used for the fabrication of such a sensor. The method proposed here can be extended to the fabrication of any MEMS SOI device with a large proof mass.

Fabrication of bulk micromachined devices like accelerometers and gyroscopes from SOI wafers is a process involving steps such as photolithography, dry etching, release of the proof mass by removing the sacrificial silicon dioxide layer, and dicing. The SOI wafer used here consists of a device layer of $50 \mu\text{m}$ where the device features are formed, a silicon handle wafer of $500 \mu\text{m}$ to hold and anchor the device features, and an intermediate insulating and sacrificial silicon dioxide layer of $2 \mu\text{m}$ that separates the device and handle layers. After photolithography, the device features are patterned to the front side of the SOI wafer by DRIE. It is normally desirable for the device features to have vertical sidewalls. For this reason, DRIE was chosen over other types of etching techniques like isotropic or anisotropic wet etching. For the large proof mass considered in this study, it is a necessity to remove the

handle wafer underneath the proof mass for two reasons: i) SOI wafers usually have an inherent high stress level leading to wafer bow. When a large proof mass is released and only anchored at a few points, it tends to tilt due to the stress. This tilting can be larger than the thickness of the sacrificial silicon dioxide layer and therefore make the proof mass touch the handle wafer if it is not removed. ii) For a large proof mass the well known problem of stiction to the handle wafer is a major issue. Even when a vapour phase HF etcher is used, stiction of the proof mass to the handle wafer is a potential problem. In order to remove the handle wafer underneath the proof mass both sides of the wafer have to be consecutively patterned and etched by DRIE to form the device layer and etch away a block of the handle wafer underneath the proof mass. This process is not straightforward as most DRIE tools have a backside cooling gas function to cool down the wafer during processing. When areas or trenches etched on the front and backside overlap, the oxide layer tends to rupture due to the pressure difference on the two sides of the wafer. This usually leads to destruction of the wafer inside the process chamber. For this reason the wafer has to be attached to a carrier wafer to enable a double sided process. There are several attachment techniques to temporarily bond the two wafers together such as using photoresist, crystal bond or thermal grease. However, each of these techniques has certain disadvantages that complicate the process and even for the best choice, the delicate device features are at risk of being damaged during the detachment process.

After DRIE, the devices can be released by etching the sacrificial silicon dioxide in a liquid or vapour form HF acid medium. In the case of wet release, the sensitive device components like the comb fingers or proof mass can stick to anchored features; or if the backside of the proof mass is not released, they can also stick to the handle layer because of surface tension forces generated during wet processing. In order to solve this, several other techniques like continuous exchange of the etching medium have also been proposed; however, they add additional steps and complications to the process [4]. In this work, an HF VPE was used where the devices are released in an HF vapour medium without any direct contact with liquid. The release process would normally be followed by dicing but this requires reliable protection of the delicate device features, which is difficult to achieve. Therefore, it is beneficial to develop a dicing free, dry release process applicable to wafer level fabrication, which is described in the following.

2. Design and Fabrication

Fig. 1.a shows the layout of the trenches (in white) on the front side and the device area (in dark blue), with the proof mass and associated comb fingers for which the layout details are not shown. The trenches are used for device release and separation as explained later. Fig. 1.b shows the layout of trenches on the backside; the inner trench circumferences the device features area on the front side and is used to define the handle wafer block that is removed underneath the proof mass. The outer trench defines the device border and is used for separation. All trenches on the front and backside are 50µm wide, and it should be especially noted that they do not overlap anywhere. This prevents a potential rupture of the silicon dioxide as mentioned above. The trench on the front side and the outer trench on the backside have a spatial offset of 400µm (fig. 2.c).

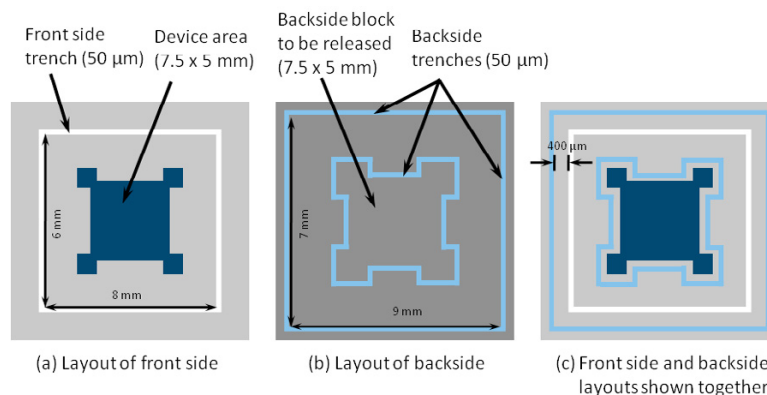


Fig. 1. (a) Layout of the front side showing the front side trench and device area. (b) Layout of the backside showing the backside trenches and block to be released. (c) Front and backside trenches separated by 400µm are shown on the same layout.

Fig. 2 shows the fabrication flow used in this work. As the first step, the handle layer is patterned with a $9\mu\text{m}$ thick AZ9260 type positive photoresist, followed by DRIE up to the oxide layer to define the backside trenches (fig. 2.a). After stripping the backside photoresist by AZ100 solvent and ashing in oxygen plasma to remove the remaining organic contamination, the front side of the SOI wafer is patterned by a diluted $3\mu\text{m}$ AZ9260 photoresist and etched in DRIE down to the oxide layer to define the device features, etch release holes, and front side trenches (fig. 2.b). The front side is etched after the backside to protect the delicate front side features against damage due to direct contact with the spinner's chuck and the platen of the DRIE. The front and backside trenches are designed in such a way that they never intersect each other and there is always a constant offset between them. This feature eliminates the need to use a carrier wafer during DRIE and hence avoids the problems related to wafer attachment.

After DRIE, the devices, the proof mass of the device, and the backside block underneath each proof mass are etched in an HF VPE system (fig. 2.c). Release holes on the front side are present in the areas where the silicon dioxide is supposed to be removed, which is underneath the proof mass and the spatial offset areas between the front and backside trenches. The release holes ensure that HF vapour can penetrate to the silicon dioxide layer; they have a diameter of $18\mu\text{m}$ and a pitch of $35\mu\text{m}$. The etch process separates the individual devices from the rest of the wafer; the latter forms a grid structure (see fig. 3.d). In fig. 2.d the actual separation process is depicted. The wafer is carefully removed from the HF VPE system and placed with the front layer up on a flat surface. The wafer grid structure is removed with a pair of tweezers, and the individual devices remain on the surface. When an individual device is lifted up, a block of silicon is left behind, which is the handle wafer underneath the proof mass. This separation technique makes a dicing step unnecessary eliminating the complications of protection of the device layer during dicing.

There are three release areas: i) the proof mass, ii) the handle wafer block underneath the proof mass, and iii) the outer trenches on the front and backside (fig 2). The spacing between the release holes and the trenches is designed deliberately different varying from 30 to $55\mu\text{m}$ in the three areas, respectively. The varying offset on the overlap areas are critical as they determine in which order the regions are released, i.e. the proof mass first then the block underneath the proof mass, and finally the individual devices from the wafer grid. Noting that the wafer is held upside down in the HF VPE, this order ensures that the weight of the block underneath the proof mass is carried by the anchored part of the device at all times and not by the proof mass.

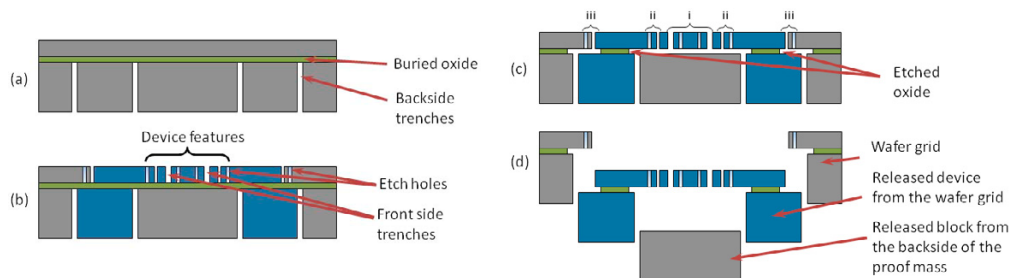


Fig. 2. Fabrication flow of the accelerometers: (a) Backside etching in DRIE to define the backside trenches. (b) Front side etching in DRIE to pattern the device features, release holes, and front side trenches. (c) The three release regions etched consecutively in HF VPE. (d) Device separation after release; devices can now be unloaded with the backside block left behind.

Fig. 3.a shows a part of the full wafer after front side DRIE, which is not released yet and fig. 3.b shows a part of the full wafer after release in an HF VPE system; the level difference between the devices and the wafer grid observed in the picture shows that the devices are fully released. In order to unload the devices, the wafer grid that is initially holding the devices together is simply removed. Fig. 3.c shows photographs of the devices after the wafer grid is removed whereas the wafer grid is shown in fig. 3.d. At the end of the process, 143 devices were successfully released from a 6 inch wafer *at once* without the need for dicing, which shows the effectiveness of the process. Apart from the individual devices, a predetermined area underneath the proof mass is also released, which enables the proof mass to move freely even when tilted due to stress or unequal suspension beams. This is shown in fig. 4.a, where the actual device (flipped over) and released block is shown at the upper right and left hand side of the image, respectively. The front side of the device is also shown at the lower right hand side for completeness.

Fig. 4.b is the SEM image of a released device showing front and backside overlapping areas, release holes, and backside trenches.

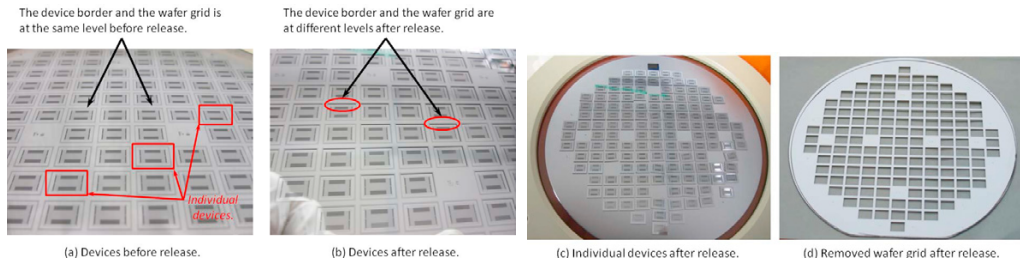


Fig. 3. Partial view of the wafer showing the devices (a) before and (b) after release. The level difference between the device outline and wafer grid proves that the devices are fully released. (c) After release, the wafer grid is carefully lifted up to expose the separated individual devices. (d) Photo of the wafer grid after it is removed.

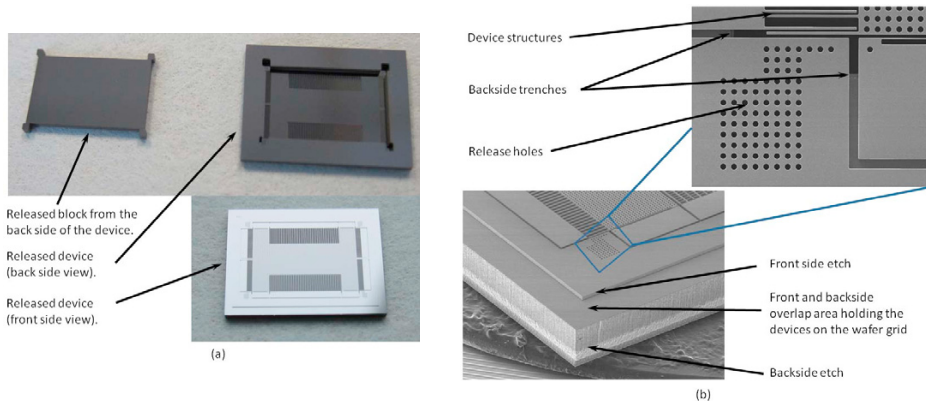


Fig. 4. Individual device (a) backside view (top right), front side view (bottom right), and released block (top left) and (b) SEM image of a device showing overlap areas and backside trenches.

3. Conclusions

A full wafer, dicing free release process is presented exemplary for an accelerometer. The process is suitable for a wide range of MEMS sensors and especially useful for devices with a large proof mass. The option to release the handle wafer at the back of the proof mass has the advantage that the proof can tilt freely and parasitic capacitances are minimized. In effect there is no limitation to the size of the released block at the back of the proof mass. The process can therefore be used for the fabrication of high performance sensors and devices where out of plane motion is required.

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