Fabrication of silicon slot waveguides with 10nm wide oxide slot

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***Abstract*— We propose and demonstrate a fabrication technique to realize extremely narrow dielectric slots in silicon waveguides. Using this method, we have demonstrated a silicon slot waveguide with 10 nm dielectric slot with a measured propagation loss of 13.6 dB/cm.**

Keywords*— *Silicon photonics, slot waveguide, accumulation type modualtor, light source.

I. INTRODUCTION

A slot waveguide consists of two high index ridges, e.g. silicon, separated by a narrow low index region, e.g. air or SiO_2. Due to such refractive index discontinuity, this structure allows one of the propagating modes to confine its energy within the slot region. For many applications, extremely narrow slot regions are essential [1-6]. For example, in silicon slot waveguides with Erbium doped SiO_2, the spontaneous emission efficiency increases with reduced slot region [2]. In opto-mechanical resonators reducing slot width increases the opto-mechanical coupling rate [3]. In one of the photonic applications, i.e. accumulation type electro-optic modulator, ultra-narrow dielectric slot is particularly very essential [4-6]. The design of accumulation modulator is based on MOS capacitor and the efficiency of the modulator depends mainly on the thickness of the dielectric region of the capacitor. Typically the dielectric width needs to be below 10 nm. Such dielectric slot is extremely difficult to realize with existing fabrication methods. In this work, we present a new fabrication method to realize arbitrarily narrow dielectric slot region in a silicon waveguide. Using this technique, we realized a silicon slot waveguide with 10 nm wide SiO_2 slot and measured a propagation loss of 13.6 dB/cm through such slot waveguide.

II. FABRICATION

Fabrication of the slot waveguides was carried out on a Silicon-on-Insulator (SOI) substrate. The SOI substrate had a 220 nm thick layer of Si with (110) surface orientation on a 2 µm thick SiO_2. Figure 1 outlines the fabrication steps used in this work. First a 20 nm-thick layer of SiO_2 was thermally grown on the top silicon layer (Fig. 1a). Then trenches of different widths and lengths were etched through the thin SiO_2 and top silicon layers. The side-walls of the trenches were smoothened by Tetramethylammonium hydroxide (TMAH) based wet etching process [7,8]. After the trenches were created, another thermal oxidation step was performed. During this step the dielectric region of the slot waveguide was formed. Here we oxidized the substrates to achieve 10 nm thermal oxide on the side walls of the trenches. Since, we are using thermal oxidation process to create the dielectric slot, the thickness of the slot can be precisely controlled. Then the grown thermal oxide was selectively removed from everywhere expect from one of the side walls of the trenches (Fig. 1b). A 300 nm-thick amorphous silicon layer was then deposited using plasma enhanced chemical vapor deposition (PECVD) system. The substrate was then annealed at 1000°C in N_2 for 10 hours. The aim of this step was to crystallize the amorphous silicon using the exposed single crystal top silicon layer as the seed. After the recrystallization process, the top layer was planarised down to 200 nm using chemical mechanical polishing (CMP). Finally rib waveguides were fabricated with 10 nm oxide region at the center of the waveguide (Fig. 1d). The rib waveguides were 450 nm wide with 80 nm high slab regions. The waveguides were then coated with a 1 µm thick PECVD SiO_2 cladding before transmission loss measurement.

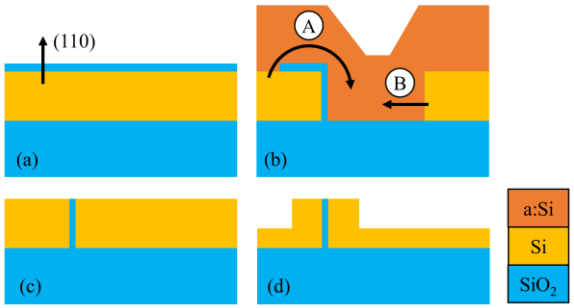

Fig. 1: Fabrication process flow: (a) 20 nm thick thermal oxide was grown on a (110)-oriented SOI wafer, (b) 300 nm of amorphous silicon was deposited using PECVD system, filling the trench region. The arrows indicate the two different recrystallization paths of the deposited silicon within the trench region, (c) The silicon layer was planarized using CMP down to 200 nm, (d) Rib waveguide was fabricated with 10 nm oxide region at the center of the waveguide.

Figs. 2a shows the cross-sectional view of the sample around the trench region after the CMP process. The position of the 10 nm oxide slot and the deposited and SOI layer regions are highlighted. We have used different trench width to find the right condition for recrystallization of the deposited silicon within the trench region. We found that for a 500 nm wide trench, the deposited silicon recrystallizes completely. But for wider trenches we found poly grains near the center of the trenches. This suggests that chance of recrystallization improves with reduced trench width. However, for narrow trenches, PECVD deposition rate

is slower and there is also the possibility of creating voids within the deposited layer. Therefore, it is more reliable to use wider trenches. For wider trenches, even though near the center the deposited silicon turns into poly, we found that closer to the oxidized side wall the deposited silicon became completely crystallized. Figure 2b shows the fabricated rib waveguide with 10 nm oxide slot at the center and fig. 2c gives a zoomed in view of the waveguide with the 10 nm slot region clearly visible. To highlight the oxide slot, we dipped the sample in HF for 10 minutes to remove some of the thermal oxide within the slot. In Fig. 2b, we could easily see the poly silicon grain boundaries away from the waveguide region, however, within the rib region we did not see any poly grain boundaries and we achieved purely single crystal silicon near the slot region.

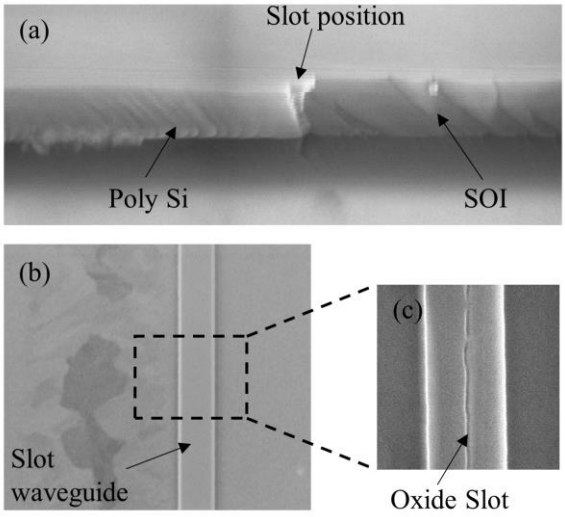

Fig. 2: (a) Cross-sectional SEM image of the substrate around the 10 nm SiO_2 slot region after CMP, (b) Fabricated rib waveguide with 10 nm oxide slot at the center. (c) The position of the exposed oxide trench after HF etch.

III. Optical Loss Measurement

For estimating the propagation loss of the fabricated slot waveguides we used a cut back method. We designed trenches with 5 different lengths: 200 µm, 500 µm, 1 mm, 2 mm and 5 mm, which gave us slot waveguides with 5 different lengths. The waveguides were tested using a tunable laser source with a tuning range from 1530 to 1620 nm. Quasi-Transverse Electric (TE) polarized light was launched into the waveguide using a fiber-grating coupler setup. The collected light was then sent to a photodetector, which automatically plots the output vs wavelength. In Fig. 3, the red circles represent the normalized output power vs. waveguide lengths. From the linear fit (black line), we estimated the slot waveguide propagation of 13.6 ±3 dB/cm.

IV. Conclusion

To summarize, we have demonstrated a new fabrication method to realize arbitrarily narrow slot waveguides in silicon. Using a sequential fabrication approach we have realized silicon slot waveguide with 10 nm oxide slot. We also introduced a recrystallization step to achieve single crystal silicon on both sides of the slot region. This was done to reduce the propagation loss of the slot waveguides. The estimated propagation loss of the fabricated slot waveguides was found to be 13.6 ±3 dB/cm. We believe that the major contributor to this loss is the surface roughness of the top silicon layer after the CMP process, which was around 8 nm (rms value) and we can significantly reduce this loss by minimizing the surface roughness using an optimized planarization process.

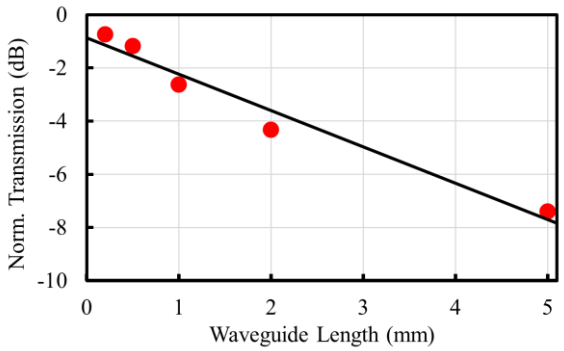

Fig. 3: Normalized optical output power (red circles) vs. waveguide length for the slot waveguide with 10 nm wide slot at 1550 nm wavelength. From the linear fit (black line), the estimated propagation loss was 13.6 ±3 dB/cm.

V. Acknowledgement

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VI. References

[1] R. Guo, B. Wang, X. Wang, L. Wang, L. Jiang, Z. Zhou, *Opt. Lett.*, vol. 37, pp. 1427-1429, May 2012.

[2] Y. C. Jun, R. M. Briggs, H. A. Atwater, and M. L. Brongersma, *Opt. Exp.*, vol. 17, pp. 7479-7490, Apr. 2009.

[3] Y. Li, J. Zheng, J. Gao, J. Shu, M. S. Aras, and C. W. Wong, *Opt. Exp.*, vol. 18, pp. 23844-23856, Nov 2010.

[4] G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, *Nat. photon.*, vol. 4, pp. 518-526, Jul. 2010.

[5] B. Milivojevic, S. Wiese, J. Whiteaway, C. Raabe, A. Shastri, M. Webster, P. Metz, S. Sunder, B. Chattin, S. P. Anderson, and B. Dama, *Proc. SPIE*, vol. 8990, pp. 899013-899013, Mar. 2010.

[6] M. Douix, D. Marris-Morini, C. Baudot, S. Crémer, D. Rideau, D. Perez-Galacho, A. Souhaité, R. Blanc, E. Batail, N. Vulliet, and L. Vivien, *Proc. IEEE*, pp. 90-91, Aug 2016.

[7] K. Debnath, H. Arimoto, M. K. Husain, A. Prasmusinto, A. Al-Attili, R. Petra, H. M. H. Chong, G. T. Reed, and S. Saito, *Front. Mat.*, vol. 3, pp. 10, Feb. 2016.

[8] K. Debnath, A. Z. Khokhar, S. A. Boden, H. Arimoto, S. Z. Oo, H. M. H. Chong, G. T. Reed, and S. Saito, *Front. Mat.*, vol. 3, pp. 51, Nov. 2016.