22.1 A Self-Tuning Resonant-Inductive-Link Transmit Driver Using Quadrature Symmetric Phase Switched Fractional Capacitance

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Inductive coupling for power transfer is increasingly popular in many applications such as RFID and wireless charging. While much recent work has focussed on receivers [1,2], less consideration has been given to the transmit function. High-Q antenna circuits are beneficial for several reasons. Activation of a link at a distance requires a large magnetic field from the transmitter, so for a given antenna current, lower driver voltages may be used, simplifying the driver and its power supplies, and improving overall efficiency. Further, the inherent filtering allows a high-efficiency switching driver to be used while reducing harmonics in the current. However, the consequent narrow bandwidth requires precise tuning to resonance. The excitation frequency may be varied in some applications, but this transfers the tuning problem to the receiver. Any transmit tuning circuitry must be linear with large voltages (from a few V to kV) and currents (mA to many A). A conventional technique is to use multiple external capacitors selected by large switches [3] or even relays. The number of selectable elements needed depends on the Q factor, component tolerances, and environmental effects, with a typical system requiring 5 or more extra capacitors and associated HV switches (Fig. 22.1.1), plus extra IC pins, adding to system cost and volume.

An alternative tuning approach common at RF is to intermittently connect a capacitance to the LC circuit such that the time-averaged fractional value achieves the desired resonant frequency. At GHz operation, synchronism between the oscillation and the switching is not realistic; the switching rate is set significantly below the resonant frequency and phase-noise shaping is applied. In low-frequency power applications, harmonics and losses due to such switching are more important, but now it is possible to impose zero-voltage synchronous switching on a fractional capacitance (Fig. 22.1.1). Hence a single additional capacitor C_2 and HV switch SW_1 can provide a large continuous tuning range, (of the order of 50%, depending on capacitor values), and if switching is ideally at the zero voltage instants, losses, transients and harmonics will be minimised. Zero-voltage switching at resonance implies that the switch SW_1 opens and closes at symmetrical time points in quadrature with the antenna-loop drive voltage, i.e. either side of the current minima. This is easy to arrange if the circuit is already resonating, but the issue of determining precise resonance still remains. To avoid the need for lossy sense resistors, one can vary the drive frequency and measure the peak voltage V_C on the capacitors, but the system must go offline.

Instead of trying to determine the required timing from an unknown state, if we simply impose the ideal quadrature switching for the fractional capacitance, then observation of the voltage across the capacitor switch SW_1 provides a direct means of detecting any tuning error [4]. Figure 22.1.2 shows the concept; SW_1 is opened and closed symmetrically by φ_{SW} in quadrature with the excitation V_{DR}, using a classical PWM arrangement. The voltage across SW_1, V_{SW} is then sensed immediately before it closes. A change of sign with respect to the ideal peak implies that SW_1 must have closed too late; the same sign as the ideal peak of V_{SW}, means SW_1 has closed too early (Fig. 22.1.2). When the sensed voltage is essentially zero, the circuit must be at resonance. These logical outputs are fed to an error integrator, which then sets the PWM timing, driving the circuit to ideal resonance and maintaining it so in real time. Figure 22.1.3 shows the architecture of a fully integrated self-tuning inductive antenna driver using quadrature symmetric-switched fractional capacitance, fabricated in a 1.8/5V/20V CMOS/LDMOS process. The basic self-tuning concept [4] requires an ideal low-R, HV bi-directional switch (Fig. 22.1.2), but to avoid practical difficulties in an IC implementation, the fixed and fractional capacitances and associated switching are realised as two switched capacitors C_N and C_P, controlled by N and P LDMOS devices, referred to internal HV supplies. At any given time, one of these is ON for at least half the period, ensuring that at resonance there is negligible reverse voltage across either switch transistor. There is a slight penalty in terms of the available tuning range, since the maximum in-circuit capacitance ratio is 1:2 and hence a 1:1.41 min:max operating frequency, but this is easily enough for most practical demands.

The demonstrator IC was intended to operate over frequency ranges commonly used by wireless charging, security and agricultural applications (75kHz to 2MHz) with moderate power levels, limited by the breakdown voltage of the available LDMOS devices and the resistance/die area trade-off acceptable in this project. Data modem functions were not included. The excitation drive signal V_{DR} is generated internally by a current-integrator oscillator whose frequency is set by a digitally controlled V-I function (fine) and switchable capacitors (coarse). This provides a reference ramp V_{TR} for the PWM timing circuit in quadrature with a square signal to the simple Class-D driver. The tuning is controlled by an analog signal V_{TUNE_P} (plus a negative copy V_{TUNE_N} wrt the reference level for V_{TR}). Combining these with V_{TR} creates two switch-control signals φ_{SW_N} and φ_{SW_P}. $V_{TUNE\_N,P}$ is generated by internal 8b DACs driven by the error feedback circuits; a direct analog-tuning input facility is also available for testing. The voltages across the LDMOS switches are sensed and the signs sampled, generating up/down error signals for a variable gain digital integrator. The system response time (e.g., to ferromagnetic objects or operating frequency changes) can thus be traded against ripple in the settled tuning value. The switch voltages can be much larger than the safe limits for internal circuitry, thus the sense-sample function incorporates thick-oxide capacitive dividers with programmable attenuation at the comparator inputs (Fig. 22.1.4). While either LDMOS switch is ON there is ideally no sense input, so the DC levels at the comparator inputs can be reset each cycle. To ensure sign sampling occurs before the switches turn OFF, small delays (insignificant at 125kHz) are inserted into the LDMOS gate drive/level shift circuits.

Measurements are shown using a 1.3mH air-cored loop with an in-circuit Q of 30. Switch control signals $\varphi_{SW\_N,P}$ are both depicted at the HV level shifter inputs, and HIGH indicates ON. Figure 22.1.5 shows the response of the self-tuning system as the excitation frequency is stepped abruptly from 100kHz to 130kHz. At 100kHz, the switches are ON almost all the time, and the switch voltages $V_{SW\_N,P}$ show only small peaks. After the frequency step, the voltage at the L-C node V_C decreases rapidly as resonance is lost; the switch controls then begin to change immediately, so that they are OFF for nearly half the new excitation period. $V_{SW\_N,P}$ can now be seen to have large, nearly half-sinusoidal peaks. Within 300µs, the system has returned to ideal resonance. Note that the self-tuning operates reliably even when protection devices clamp off-tune excursions outside the HV supplies to ~0.5V. Figure 22.1.6 shows the response to a frequency sweep from 130kHz to 100kHz over 1.4ms with self-tuning disabled, with an expected peak in V_C at resonance. Above resonance, the switch voltages $V_{SW\_N,P}$ can be seen to be non-zero just before they turn back ON. The measured (10 samples) tuning error over the operating frequency range is < 2.5°, determined from the phase difference between V_{DR} and V_c (ideally 90° at resonance). For comparison, estimates are also given for the die area and pin count required to achieve similar static tuning performance with a conventional selectable capacitor system in the same technology; however, no comparable dynamic tuning behaviour would be possible. For a given tuning accuracy, the fractional capacitance technique offers significant benefits, as well as eliminating the need for offline calibration periods. The system architecture is quite generic; with the IC technology available, a mainly analog system was preferred. With denser, faster logic, many functions can be made digital; for higher power/voltage, external switch devices may be used.

[1] L. Cheng et al., "Adaptive On/Off Delay-Compensated Active Rectifiers for Wireless Power Transfer Systems", *IEEE JSSC*, Mar. 2016.
[2] K-G Moh et al., "A Fully Integrated 6W Wireless Power Receiver Operating at 6.78MHz with Magnetic Resonance Coupling", *ISSCC*, Feb. 2015.
[3] "AS3909/AS3910 13.56 MHz RFID Reader IC" data sheet, p.64, AMS AG, www.ams.com.
[4] W. Redman-White et al., "Adaptive Tuning of Large-Signal Resonant Circuits Using Phase-Switched Fractional Capacitance", *accepted to IEEE TCAS-II.*

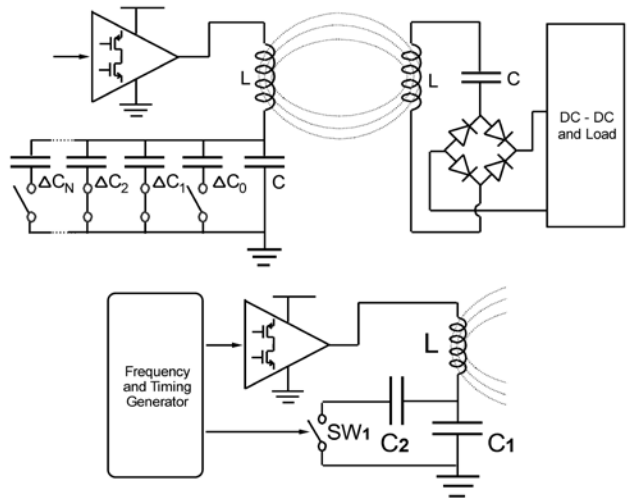


Figure 22.1.1: Top: Conventional inductive link with selectable tuning capacitors; Bottom: Switched fractional capacitor continuous tuning.

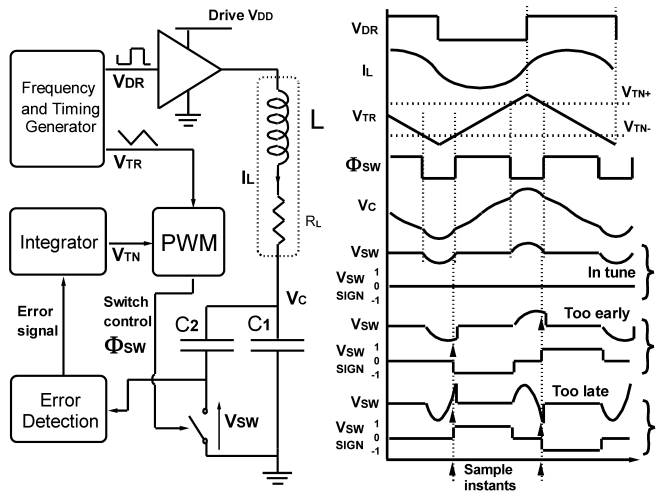


Figure 22.1.2: Left: System-level diagram of self-tuning inductive antenna driver; Right: Timing diagram for sensing resonance and deriving error signals.

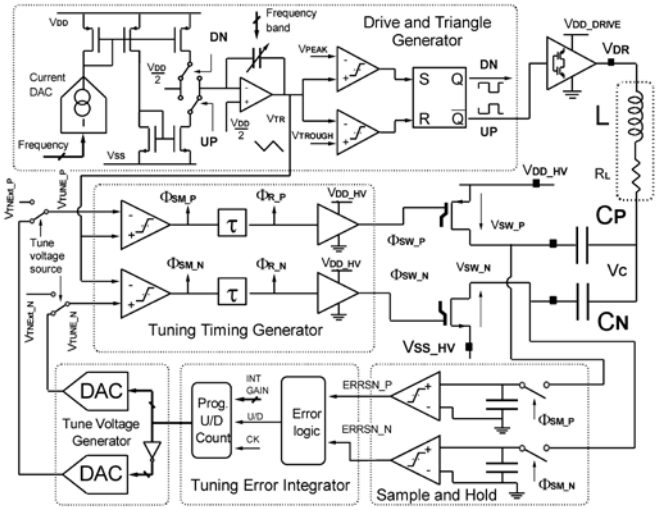


Figure 22.1.3: Circuit architecture of integrated self-tuned inductive antenna driver.

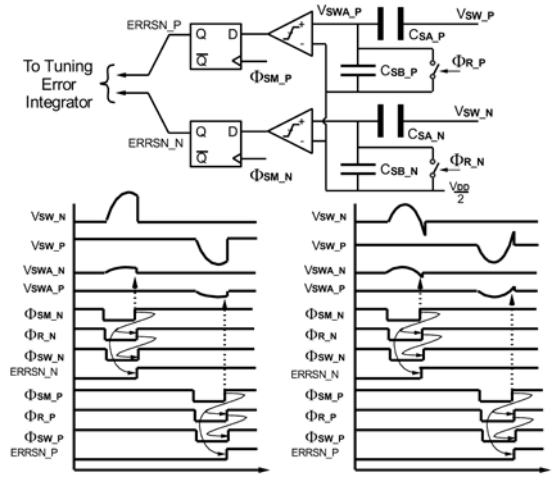


Figure 22.1.4: Top: attenuating resetting sense-sample architecture; Bottom: Sense-sample function timing for below-resonance (left) and above-resonance (right) conditions.

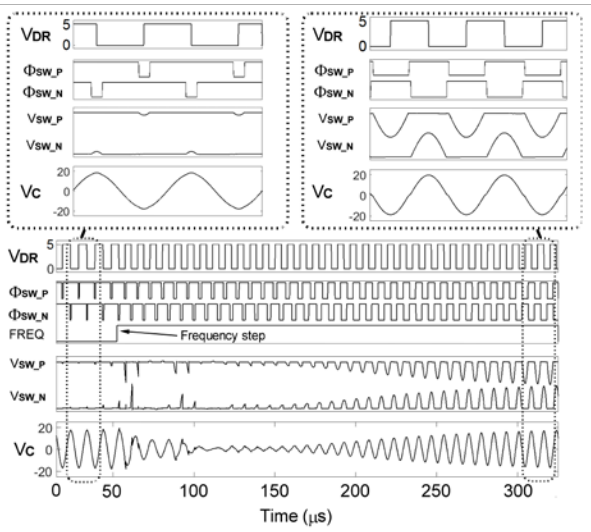
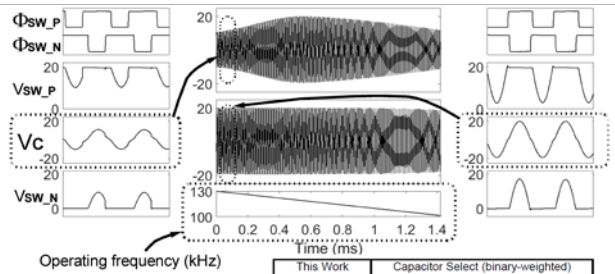


Figure 22.1.5: Response of self-tuning system to step increase in drive frequency (100kHz to 130kHz).



Operating frequency (kHz)		This Work Avg. 10 samples		Capacitor Select (binary-weighted) Equivalent perfomance		3dB bandwidth	
Operating Q factor		30		30		30	
Test centre frequency		110kHz	1.3MHz	110kHz	1.3MHz	110kHz	1.3MHz
Phase error at resonance (Deg)		0.97	2.26	> 1	> 2.5	> 45	> 46
HV switches	Number of switch devices	2		11	10	5	5
	Number of package pins	2		11	10	5	5
	PMOS resistance (ohm)	4.89		10.6 (1)		10.6 (1)	
	NMOS resistance (ohm)	5.80		10.6 (1)		10.6 (1)	
	Total active area (μm²)	1360		3740	3400	1700	1700
	Other HV circuitry area (mm²)	0.246		1.35	1.10	0.615	0.615
Implementation specifications	Process geometry (μm)	0.18					
	Total die area (mm²)	3.17					
	Max. drive current (mA)	100					
	Max. HV switch voltage (V)	20					
	Frequency range	75kHz - 2MHz					
Power consumption (excluding driver)		79mW					

(1) Total aggregate resistance of switches to achieve equivalent Q factor

Figure 22.1.6: Top: L-C node (V_C) response to freq. sweep (130kHz to 100kHz). Upper: self-tuning disabled; Lower: self-tuning enabled (fast integrator response). Bottom: performance comparison table.

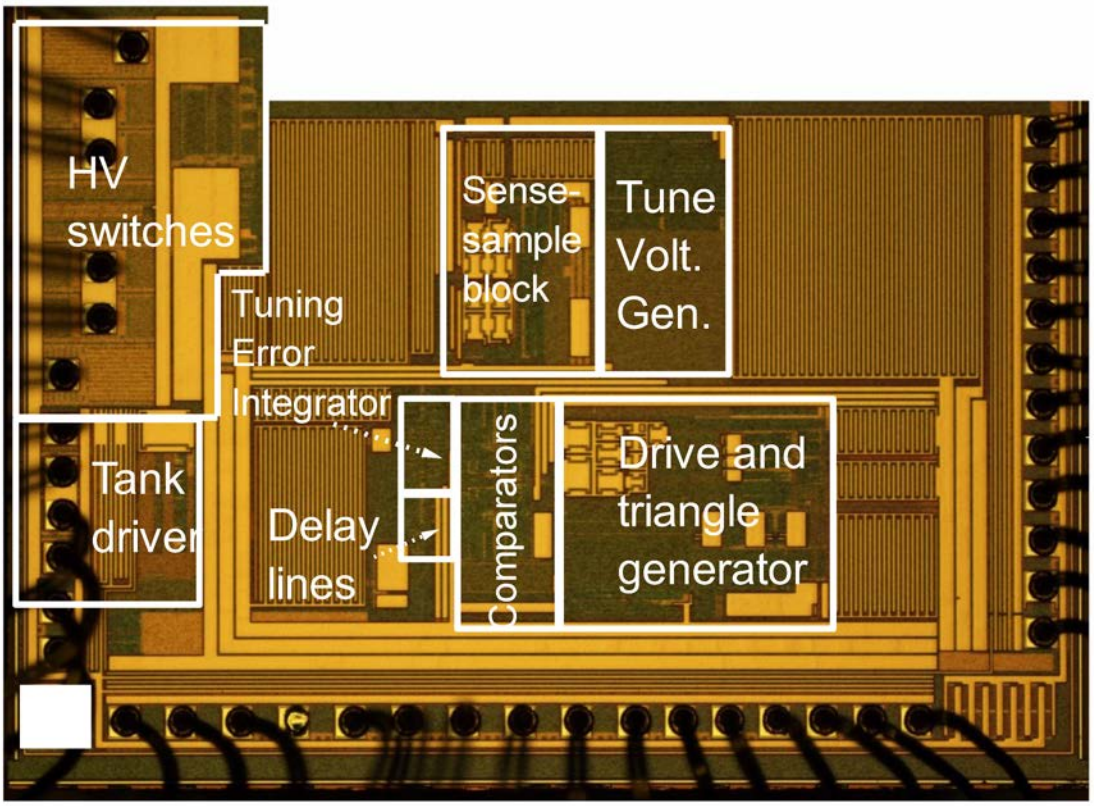


Figure 22.1.7: Die micrograph of integrated driver in a 0.18μm 20V process. Decoupling capacitance added between active blocks.