Research data for

Active Counter Electrode in a-SiC Electrochemical Metallization Memory

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The manuscript contains all information required to reproduce the results that it contains. Here, the numerical data results are given by a xlsx file.

The xlsx file contains data for each figure, with each figure data located on an individual sheet, named accordingly.

The sheet named Fig 1a contains current-voltage data point for Cu/a-SiC/Au DC sweeps. The sheet named Fig 1b contains current-voltage data point for Cu/a-SiC/W DC sweeps.

The sheet named Fig 2 contains current voltage data points for Cu/a-SiC memories in the LRS or ON state, with the tables labelled appropriately with tungsten or gold.

The data sheet named Fig 3 contains current voltage data points for Cu/a-SiC/W memories in pristine states (PRS) in one table and high resistance states (HRS) in another, labelled accordingly.

The data sheet named Fig 4a contains data points for device area vs. current, along with the standard error, for the pristine state (PRS), high resistance state (HRS) and low resistance state (LRS) for Cu/a-SiC/Au memories. The sheet named Fig 4b contains the same layout of data but instead for Cu/a-SiC/W memories.

The sheet named Fig 6a contains current voltage plots for different current compliances for Cu/a-SiC/Au memories. The different current compliances are separated, with labels at the top. The sheet named Fig 6b has the same layout but instead for Cu/a-SiC/W memories.

The sheet named Fig 7a contains current readings at 0.1V for different current compliances for both the ON current (Ion) and OFF current (Ioff) for Cu/a-SiC/Au memories. This data is used to produce the boxplots seen in Fig 7a. Ion and Ioff are in separate tables. Fig 7b is the same instead for Cu/a-SiC/W memories.

The sheet named Fig 8a contains resistance vs. cycle number data points for Cu/a-SiC/Au memories. The resistances are for OFF and ON state and are labelled as Roff and Ron, respectively. Fig 8b contains the same layout but for Cu/a-SiC/W memories.

The data sheet named Fig 9 contains data points of natural log of time (ln(t)) and 1/V^2 for RESET and V for SET, in two separate tables for RESET and SET. Std dev is also included for each table.

The data sheet named Fig 10a contains current vs voltage data points for multiple DC sweeps for forming in the negative bipolar regime for Cu/a-SiC/W memories. The data sheet named Fig 10b contains the same data format but this time for SET and RESET DC sweeps in the negative bipolar regime for Cu/a-SiC/W memories.

The data sheet named Fig10b insert contains voltage vs current data pts used to plot the insert in Fig 10b in the manuscript, for negative bipolar LRS state in Cu/a-SiC/W memories.