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# Integrated Reciprocal Conversion with Selective Direct Operation for Energy Harvesting Systems

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***Abstract*—Energy harvesting IoT systems aim for energy neutrality, i.e. harvesting at least as much energy as is needed. This however, is complicated by variations in environmental energy and application demands. Conventional systems use separate power converters to interface between the harvester and storage, and then to the CPU system. Reciprocal power conversion has recently been proposed to perform both roles, eliminating redundancy and minimizing losses. This paper proposes to enhance this topology with 'selective direct operation', which completely bypasses the converter when appropriate. The integrated system, with 82% bidirectional conversion efficiency, was validated in 65nm CMOS with only the harvester, battery and decoupling capacitors being off-chip. Optimized for operation with cm$^2$ photo-voltaic cell and a 32-bit sub-threshold processor, the scheme enables up to 16% otherwise wasted energy to be utilized to provide >30% additional compute cycles under realistic indoor lighting conditions. Measured results show 84% peak conversion efficiency and energy neutral execution of benchmark sensor software (ULPBench) with cold-start capability.**

***Index Terms*—Energy Harvesting, Sub-threshold, Switched Capacitor Converters, MPPT, Cold-start.**

## I. Introduction

WIRELESS sensor systems are expected to represent a large proportion of IoT devices. Powering these from batteries will be a major challenge, but may be overcome by harvesting energy from the environment. In general, designers aim for *energy-neutrality* – a condition where systems harvest energy at least as much as is required to carry out their activities. In simple terms, the aim is to harvest as much energy as possible and convert with high efficiency to maximize the amount of useful work done. However, this represents a complex optimization problem for circuit and system designers: the available energy depends on ambient conditions and is limited by power conversion efficiency, while the energy expended depends on run-time conditions and software workloads. These problems are exacerbated in volume-constrained applications, which have to make do with small energy harvesting and storage devices. Sensor systems with cm$^2$ form factors are attractive as they offer a good balance between harvesting and storage capacity, and overall cost.

A typical energy harvesting sensor system is shown in Fig. 1 [1]. For this work, the CPU and its associated elements are referred to as the 'CPU system'. Energy is stored in a supercapacitor or battery, which acts to decouple the CPU system from the dynamics of the energy harvester. An input converter allows the spatio-temporally variable harvested energy to charge the storage device. The design challenge here is to ensure that the harvester and input converter in combination can *maximize harvested energy*. This means that the converter must be designed to minimize conversion losses and also ensure maximum power transfer by impedance matching (e.g. using maximum power point tracking, MPPT). An output power converter provides a regulated supply to the CPU system. The challenge for the combination of CPU system and the output converter is to *expend minimum energy* while undertaking sensory activities.

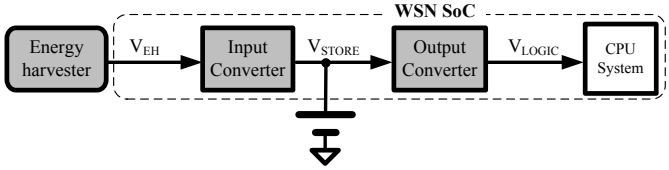


Fig. 1. Conventional power conversion in energy harvesting systems [1].

This work focuses on the aforementioned design challenges and demonstrates a cm$^2$ system that achieves energy-neutrality while running the ULPBench software benchmark [2]. The design is centered on a highly efficient *reciprocal power converter*, which can perform both input and output power conversion, and system optimization steps for *selective direct operation* of the CPU system in certain modes, bypassing the conversion stages entirely. The key contributions are:

1) an integrated energy harvesting scheme that allows otherwise wasted energy to be used for computation.
2) a reciprocal converter with the highest bidirectional conversion and area efficiency.
3) the demonstration of a cm$^2$ energy-neutral system executing an industry-standard IoT software benchmark at very low indoor light levels (160 lux).

This work first presents real-world measurements of cm$^2$ photo-voltaic (PV) cells and analyzes the characteristics of state-of-the-art minimum energy (MinE) CPU systems (Section II). The analysis reveals an opportunity to exploit redundancies and improve energy utilization. The proposed design is presented (Section III), along with corresponding measured block-level results (Section IV). Overall system performance is then presented (Section V). The work focuses on cm$^2$ PV cells, but the techniques presented can be applied to other forms of energy harvesting e.g. thermoelectric generators.

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TABLE I
COMPARISON OF STATE-OF-THE-ART MINE CPU SYSTEMS

| | | MSP430 [3] | Subliminal [4] | CoreVA [5] | SleepWalker [6] | Cricket [7] |
|---|---|---|---|---|---|---|
| **Technology** | | 65nm | 180nm | 65nm | 65nm | 65nm |
| **Typ. Supply Voltage** | $V_{DD}$ | 1.2V | 1.8V | 1.2V | 1.2V | 1.2V |
| **Retention Power** | $P_{RET}$ | 1µW | 0.55nW | NR | 1.7µW | 80nW |
| **Min. Energy Point** | $E_{MIN}$ (pJ/Hz) | 27.2 @500mV, 435kHz | 2.7 @400mV, 1.1MHz | 9.9 @325mV, 135kHz | 2.2 @375mV, 23MHz | 11.7 @390mV, 688kHz |
| **Minimum Voltage** | $V_{min\text{-}LOGIC}$ | 200mV @ 10kHz | 200mV @ 200kHz | 240mV @ 10kHz | 300mV @ 10MHz | 200mV @ 27kHz |
| **Max. CPU Frequency** | $F_{MAX}$ | 1.1MHz @ 600mV | 12MHz @ 0.8V | 100MHz @ 1.2V | 71MHz @ 0.5V | 66MHz @ 0.5V |
| **Integrated DC-DC** | | YES | NO | NO | YES | YES |

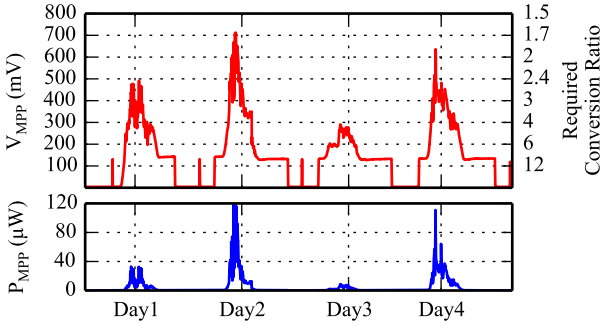


Fig. 2. Measured output from cm$^2$ PV cell, and required conversion ratio for a 1.2V output.

## II. POWER REQUIREMENTS OF IOT DEVICES

To identify the design and operating requirements of energy harvesting IoT devices, a good understanding of the characteristics of both MinE CPU systems and micro-scale harvesters is essential. Table I summarizes the properties of leading MinE CPU systems. MinE operation is possible at lower supply voltage [8] which is of the order 300-500mV for current CMOS technology nodes. Note that (from Table I) MinE CPU systems feature µW order sleep/retention power and 8∼10x higher power in active mode at the minimum energy point (MEP). Although the MEP in most systems is achieved at ≈370mV, the minimum functional voltage ($V_{min\text{-}LOGIC}$) is about 200mV. Notable exceptions are the MSP430 clone [3] where MEP of 500mV is dictated by the large SRAM array and SleepWalker [6] where LP/GP process mix contributes to an increase in the minimum functional voltage (300mV).

### A. Voltage Conversion Requirements

The output converter performs the important task of converting energy available at $V_{STORE}$ to $V_{LOGIC}$ levels. Therefore, the output converter must be very efficient at conversion and also track the minimum energy point (MEP) of the CPU system. In contrast, the input converter must be designed to efficiently support a range of conversion ratios to charge the energy storage device from available ambient energy ($V_{EH}$). Tightly coupled fully-integrated converters are desirable to help with fast dynamic voltage and frequency scaling (DVFS) to enable MinE operation. For best integration it is desirable to have power converters designed as switched-capacitor converters (SCC) since high-quality inductors are difficult to obtain in low-cost digital CMOS processes.

To better understand the conversion ratio requirements in real applications, field measurements were taken from a cm$^2$ PV cell indoors (office environment, mix of artificial and natural light, 25°C) over a 4-day test period. The PV cells were subjected to continuous I-V sweeps [9] to record the maximum harvested power ($P_{MPP}$) and the voltage levels at which $P_{MPP}$ was achieved ($V_{MPP}$) (Fig. 2). The figure is further annotated with the required conversion ratio of the input converter in this application. This assumes an output of 1.2V which is the nominal for both NiMH batteries and 65nm technology (Table I).

The wide input voltage variation would require a ratio ranging between 1.5∼12. However, SCC loss depends on its conversion ratio [10]. The power conversion efficiency of SCCs is given as (1), and (2) gives a breakdown of conversion loss ($P_{LOSS}$).

$$\eta_{CONV} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \tag{1}$$

$$P_{LOSS} = P_{SW} + P_{CAP} + P_{SSL} \tag{2}$$

Here, $P_{SW}$ and $P_{CAP}$ are switching loss and bottom-plate loss, respectively. $P_{SSL}$ is the I$^2$R conduction loss due to the inevitable drop across the output impedance of the SCC. Each of these loss components increase at higher conversion ratios [10] because of the increased number of switching and reactive elements (capacitors). This increase in conversion loss at lower input voltages sets an artificial limit on the converter input voltage ($V_{min\text{-}DCDC}$).

If the input converter ratio is fixed at 2 (so as to maximize conversion efficiency) then the $V_{min\text{-}DCDC}$ is approx. 0.6V. This can be detrimental in the case of cm$^2$ PV cells where the $V_{MPP}$ rarely exceeds 0.6V, even under bright light. For micro-scale sensor systems this means that either a larger PV cell or an array with multiple cells is required or the system throughput will require throttling. Note, however, that for sub-threshold systems $V_{min\text{-}LOGIC}$ is well below 0.6V with the potential of utilizing part of the energy available at sub-$V_{min\text{-}DCDC}$ levels, provided the CPU system can be carefully managed.

Apart from this additional energy utilization, conversion losses can be minimised by eliminating redundancy. Note that most integrated output converters in state-of-the-art CPU systems (Table 1) include a voltage doubler (conversion ratio of 2). While some works do include additional ratios [3], [7],

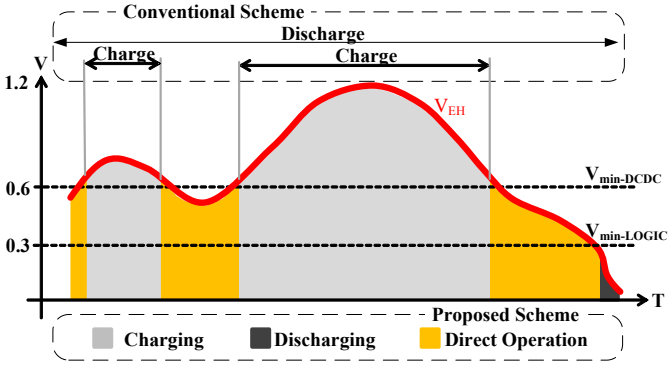


Fig. 3. Conceptual representation of energy harvesting through converter-less operation of CPU system.

peak efficiency is reported for a ratio of 2. Input converters also prefer this ratio, as described in recent published works [11] [12]. This results in multiple converters performing the same function which can be eliminated by design.

### B. Two Stage vs Reciprocal Conversion

The need for minimising lossy conversion stages has been recognised in prior works [13] [14] [15] and various improvement schemes have been proposed. Some implementations [13] have employed multiple converters where a primary converter is used when available energy is limited and two stage conversion becomes excessively lossy. If sufficient energy is harvested, a secondary converter is enabled to charge a storage device. A third backup converter is employed to power the load using stored energy at times when no ambient energy is available. This modular approach is useful so that each converter can be optimised for its specific purpose, but the area overhead is significant. Further, an off-chip inductor is used (although it is time-shared among all converters) which poses integration challenges. Other works in contrast, [14] use a single, fully-integrated SCC. However, the load uses a further stage of regulation (low drop-out regulator) which limits conversion efficiency to 66%. Neither of these approaches overcome the harvesting limit imposed by $V_{min\text{-}DCDC}$.

A recent work [15] explores stacking of PV cells to increase their output voltage which partly alleviates the problem of $V_{min\text{-}DCDC}$. Powering the load (a video monitoring SoC) directly helps avoid conversion losses. However, the observation of a flat $V_{MPP}$ (based on simulation results) was used to preclude MPPT techniques and associated overheads. This is contrary to measurements carried out which show wide $V_{MPP}$ variation with ambient energy (Fig. 2).

## III. Proposed Single Converter and Direct Operation Scheme

The work described in this paper:

1) avoids two-stage conversion using a single reciprocal converter with high bidirectional conversion efficiency which can adapt to varying light levels.
2) enables use of optimum conversion ratio and overcomes the harvesting limit imposed by $V_{min\text{-}DCDC}$ by enabling selective direct operation to exploit the ultra-low $V_{min\text{-}LOGIC}$ offered by state-of-the-art MinE CPU systems.

To present the proposed scheme of selective direct operation, $V_{MPP}$ measurement in Fig. 2 is approximated in Fig. 3 as $V_{EH}$ which varies depending on ambient light. For the conventional two converter scheme, the battery would only be charged when $V_{EH}$ exceeds $V_{min\text{-}DCDC}$ and drained by the CPU system during its operation. In contrast, the proposed method allows the battery discharge to be limited to the region $V_{EH}<V_{min\text{-}LOGIC}$. This is possible by allowing the CPU system to operate directly without a series converter during phases where $V_{min\text{-}LOGIC}<V_{EH}< V_{min\text{-}DCDC}$. Thus three operational modes are possible:

1) **Charging:** $V_{EH} > V_{min\text{-}DCDC}$.
2) **Direct Operation:** $V_{min\text{-}LOGIC} < V_{EH} < V_{min\text{-}DCDC}$.
3) **Discharging:** $V_{EH} < V_{min\text{-}LOGIC}$.

The converter and CPU system interface for implementing the three modes is illustrated in Fig. 4. Note that the interface between the harvester, load and the storage device is through a single converter which is enabled only during charging and discharging phases. The use of this single reciprocal converter eliminates the losses associated with a two stage conversion process. The energy path during the three modes of operation is highlighted. The switching frequency for the reciprocal converter (SC clock) allows MPPT during the charging phase. During direct operation the CPU clock is varied such that the rail impedance presented by the CPU matches the harvester output impedance. Measured results presented in section V-D show that the CPU impedance varies between 2kΩ and 200kΩ during direct operation. During the discharge phase the SC clock targets maximum conversion efficiency. Thus MPPT, MinE and maximum efficiency tracking may be achieved in corresponding modes. The frequency requirements for the SCC ($F_{SCC}$) and the CPU system ($F_{CPU}$) during charging, direct operation and discharging modes is summarised as (3), (4) and (5) respectively.

$$F_{SCC}, F_{CPU} = F_{MPPT} \tag{3}$$

$$F_{SCC} = 0, F_{CPU} = min(F_{MPPT}, F_{CPUmax}) \tag{4}$$

$$F_{SCC} = F_{EFFmax}, F_{CPU} = F_{MinE} \tag{5}$$

To implement such a system, reciprocal converters with high bi-directional conversion efficiency are needed, along with

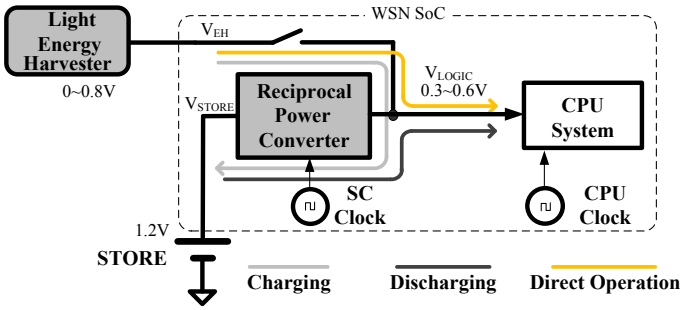


Fig. 4. Proposed scheme to avoid two stage conversion and enable selective direct operation.

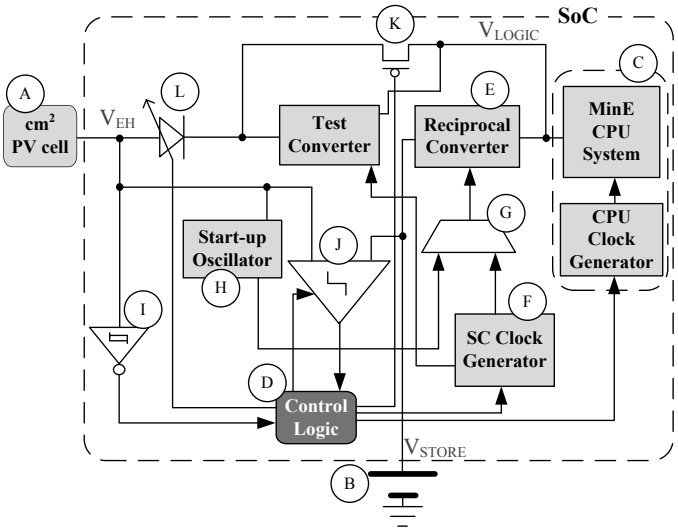


Fig. 5. Energy harvesting sensor SoC implementation with proposed reciprocal conversion and MinE CPU system.

low-power programmable clock generators (PCG) for MPPT. Since the scheme relies on $V_{EH}$ for determining the mode of operation, low-power comparators are necessary. The next section describes the design of these circuits.

## IV. System Design and Modular Results

The energy harvesting sensor system was implemented in 65nm along with the MinE CPU system. As indicated in Fig. 5, apart from the 0.88cm$^2$ PV cell (A), the 0.68x0.23cm ($\phi$xh) 6mAh battery (B) and decoupling capacitors, all other features required to implement the proposed scheme is included on the SoC. The MinE CPU system (C) includes an internal clock generator which can be tuned by the control logic (D) to match the CPU $F_{CPUmax}$ or $F_{MPPT}$ during direct operation. Under optimal settings the CPU clock generator tracks the PV output for MPPT achieving a near 99% tracking efficiency, similar to recent works [15]. The reciprocal converter (E) allows the battery to be recharged from harvested energy and also battery-powers the CPU system when harvested energy is insufficient. It must be noted that although the CPU system is at it's MEP of 0.39V, the MEP for CPU + IVR is at ≈0.52V. This shift in MEP is due to converter overheads [7] which better matches with the converter output when the conversion ratio is 2.

A wide range PCG (F) is used for the SCC which can be programmed for MPPT while harvesting or to achieve maximum efficiency when in discharge mode. The multiplexer (G) allows the reciprocal converter to be clocked from the PCG or a start-up oscillator (H) to enable cold-start. Cold-start is a critical feature of energy harvesting systems as it allows the system to boot-up with zero initial energy. The Schmitt inverter (I) allows coarse low-voltage detection to start the control algorithm. When sufficient harvester output is available, the control logic uses a clocked comparator (J) for MPPT using the fractional $V_{OC}$ method [16].

If the harvester output is insufficient for either direct operation or charging, the PV cell is disconnected from the internal regulated node ($V_{LOGIC}$) using a switch (K). For the control algorithm to be able to sense the actual $V_{EH}$ in isolation

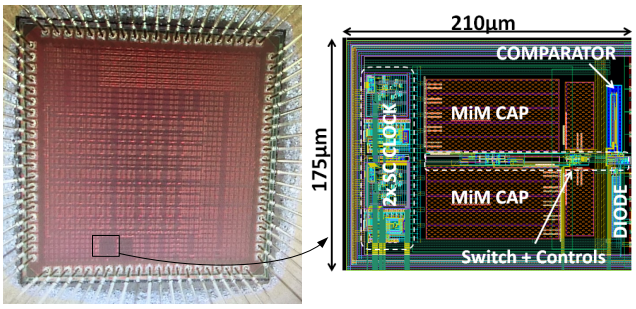


Fig. 6. Die photo and annotated layout.

from $V_{LOGIC}$ when the switch is closed, the two nodes need isolation. A programmable diode (L), built using zero-$V_T$ (ZVT) devices provides this isolation and prevents reverse current into the PV cell under low-light conditions.

The macro was implemented in an area of 210x175µm. The die photo is shown in Fig. 6 with annotated converter fly-caps, programmable clock generator, low power comparator and protection diode.

### A. Reciprocal Converter

SC converters can be modelled as two port reciprocal networks assuming ideal switches [10]. Many techniques can be used to achieve near-ideal behaviour in switches. The transmission gate-like switch implementation is a popular approach [11]. Other methods use gate over-drive and well-biasing. Switches designed using transmission gates ease the design of drivers and non-overlapping clock generators, but they increase switching losses as they use up to 2x more gate capacitance per driver. Using well-biasing requires triple-well processes or large N-well isolation which costs area. Gate over-drive is easy to implement provided the over-drive voltage can be generated without significant overheads (charge-pumps etc). This design relies on the battery voltage being 1.5-2x that of both the harvester voltage and the converter output voltage to ensure that the switches turn off reliably during normal operation.

The converter schematic is shown in Fig 7. Two phase-interleaved converters work on complementary phases of the

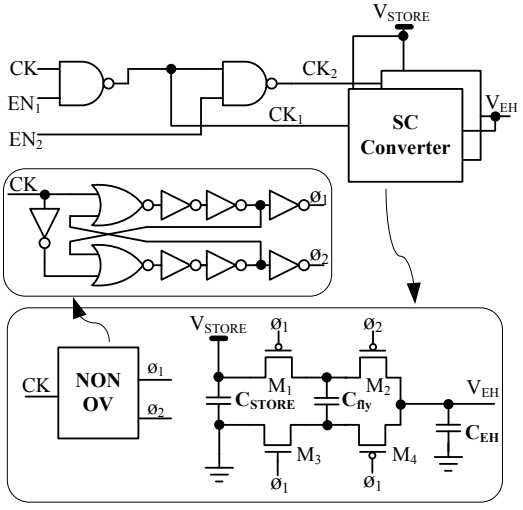


Fig. 7. Proposed reciprocal SC conversion scheme.

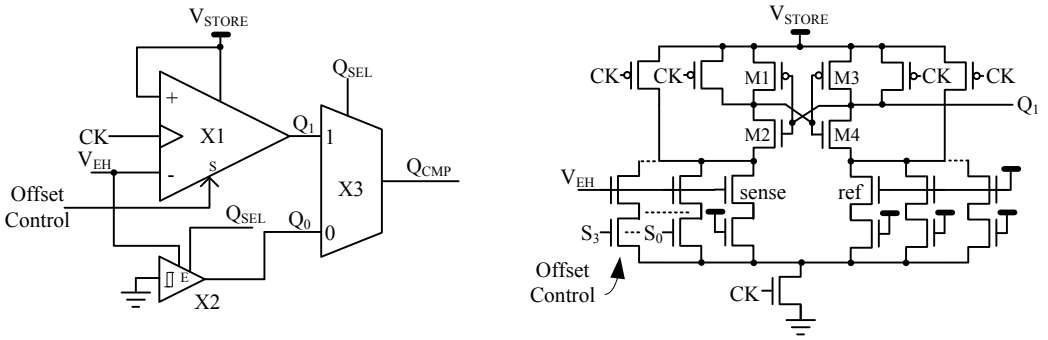


Fig. 8. Proposed low power comparator scheme (a) coarse and fine comparator, (b) programmable offset clocked comparator.

clock. The choice of sufficiently wide PMOS switches for M1 and M2 allows reliable turn-on even if the battery voltage is lower than harvester voltage. This means that the M1 and M2 have significant off-leakage, especially during a cold-start, but this scenario resolves quickly when sufficient charge is transferred from the harvester to the storage device. A single non-overlapping clock generator is sufficient since shoot-through currents are only possible through M1 and M2. M3 and M4 are never continuously ON simultaneously as they are complementary devices and are gated by the same phase.

### *B. Low Power Comparators*

High-power analog assist components degrade the benefits of MinE CPU systems. Designing power-matched mixed-signal blocks is essential, as are high-efficiency converters and low-power CPU systems. Conventional comparator designs suffer from significant quiescent current making system-level energy-neutrality a difficult objective. In this work, as illustrated in Fig. 8a, two comparators are employed to better match available power: 1) low-power coarse Schmitt comparator and 2) programmable clocked comparator.

Clocked comparators are typically used for low quiescent power comparison. However most designs [3] [13] employ reference voltage generators or resistive dividers with significant continuous power. In order to avoid this power overhead, reference generators is avoided in this design and instead the inherent offset in the comparator is tuned to achieve variable trip points (Fig. 8b).

The input and offset control transistors are matched using common-centroid layout techniques with large channel lengths and widths. This minimizes on-chip variation and helps with linearity. The reference input for the comparator is derived from $V_{STORE}$ and the sense input is connected to $V_{EH}$. The input devices on the sense side are sized in a binary fashion to give fifteen linearly increasing trip points for corresponding settings of S[3:0].

Fig. 9 shows measured comparator trip points from multiple dies. The observed linearity of trip point vs. offset control bit setting is sufficient to reliably sense $V_{EH}$ at 50mV steps. The control logic incrementally varies the offset control bits until the output of the comparator is a logic 1. The offset-control value represents $V_{EH}$ at this point.

For $V_{EH}$ below 400mV, this comparator is disabled and the Schmitt inverter, with a fixed trip point of 350mV, is used for comparison. The Schmitt inverter has negligible quiescent power but uses a device $V_T$-based threshold to enable a coarse comparison at low voltages (Fig. 8c). Further, the Schmitt inverter is powered from the harvester output so that no stored energy is expended for this comparison. To ensure that the control logic can read the low-voltage output of the Schmitt, a wide range level-shifter [17] is used. The level-shifter is disabled when the control logic is not sampling the Schmitt inverter output.

### *C. Programmable SC Clock Generators*

This module was developed over two iterations with the first revision using off-chip clock sources to understand the

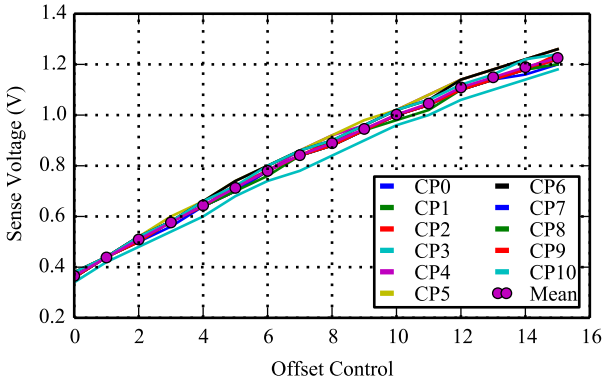


Fig. 9. Measured comparator trip-points vs offset-control for multiple chips.

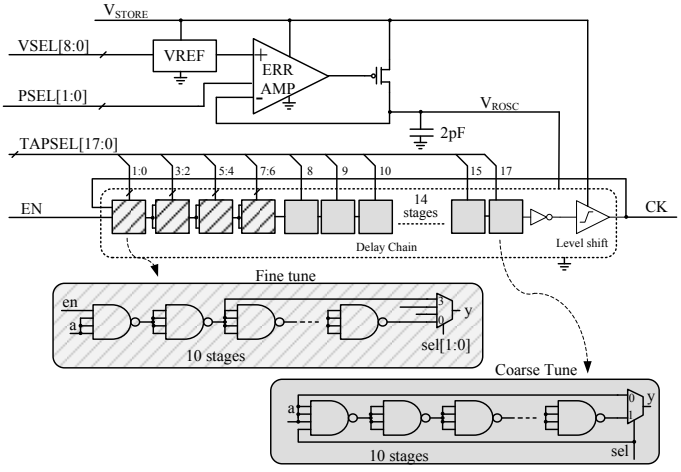


Fig. 10. Proposed scheme for low-power programmable clock source.

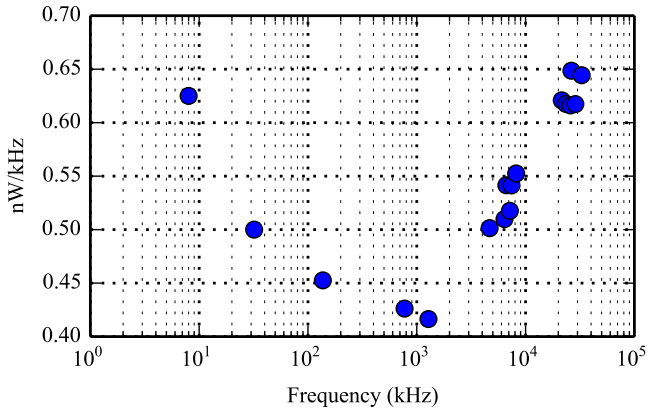


Fig. 11. Measured nW/kHz for the programmable SC clock generator.

required range of frequencies under dynamically varying light conditions. Corresponding measurements revealed the need for a 10kHz∼30MHz range for the SCC to ensure MPPT over a wide dynamic range of ambient energy. It is imperative that the overheads of clock sources should be minimal. Low-cost PCGs can be designed using ring oscillators with dividers. However, for low frequencies the power expended in the initial stages of the divider clocked from a fast ring oscillator would defeat the objective of system energy-neutrality. Slow ring oscillators on the other hand would require very long chains, costing area.

An alternate method is to use voltage controlled oscillators (VCO) or current-starved oscillators (CSO). Both VCOs and CSOs, however, suffer from excessive quiescent current in the error amplifier. This design employs dynamic power-bandwidth tuning to minimize quiescent power in the error amplifier. Further dynamic power in the delay chain was reduced to obtain an integrated PCG operating at sub-nW/kHz over a wide range of frequencies.

Fig. 10 shows the schematic of the PCG with 18 bits for tap selection (TAPSEL[17:0]) and 9 bits for VCO voltage selection (VSEL[8:0]). The quiescent power is controlled using PSEL[1:0] bits. These bits are exercised in a manner so as to allow high bandwidth for the error amplifier for deterministic settling of the oscillator each time settings are changed. Once settled, the ring oscillator presents a relatively static load and the high bandwidth is redundant allowing the quiescent power to be gradually reduced using PSEL bits.

The delay chain is designed using 14 coarse and 4 fine delay stages with each stage using 10, 4 input NAND gates. The stack-effect in the 4 input NAND limits the dynamic short circuit current lowering power. Further, the tap selection multiplexers gate the edge from propagating needlessly when a specific stage is excluded from the ring. Fig. 11 shows the measured frequency range (using only VSEL and coarse selection bits) vs. nW/kHz. The measured energy of <0.65nW/kHz ensures low power overheads due to PCG.

## V. Measured System Results

This section presents the measurement setup and results obtained for converter efficiency, dynamic tracking and overall system performance.

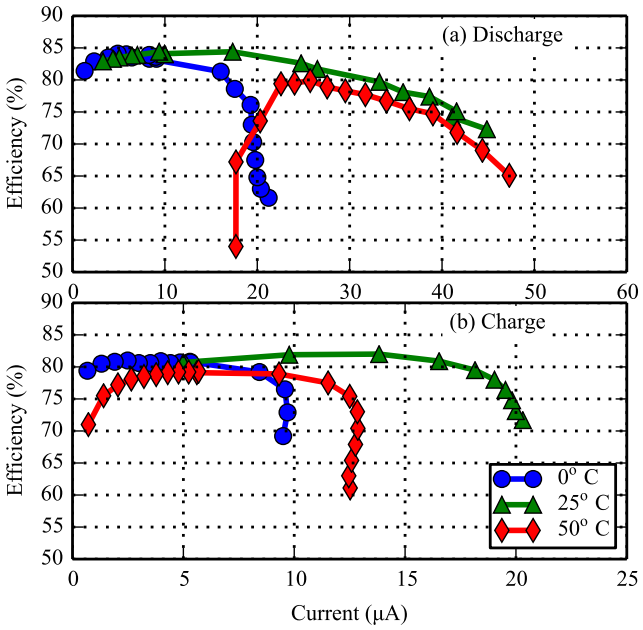


Fig. 12. Measured reciprocal conversion efficiency across temperature. (a) Discharge and (b) Charge

### A. Reciprocal Converter Efficiency

Fig. 12 shows the SCC conversion efficiency for both charging and discharging modes. Charging efficiency was measured with a 6mAh, 1.2V NiMH battery while discharge efficiency measurement used a variable resistive load. The SCC frequency was tuned to maximize efficiency. The measurements were recorded for both low (0°C) and high temperatures (50°C). Under normal operating conditions the peak conversion efficiency in discharge mode is 84% while the charging efficiency is 82%. Over the measured temperature range, the charging current remains relatively fixed as it depends largely on battery initial voltage. The discharge current however increases as the charge transfer capability of the converter increases at higher temperatures (due to better device conductance). However, increased switching losses degrade the discharge efficiency.

### B. Dynamic Tracking

To observe the dynamic tracking capability of the proposed system the control flow was set up as shown in Fig.13a. When no harvested energy is available, the control logic is in a slow (10s sample time) loop monitoring the Schmitt output. If the Schmitt indicates availability of sufficient energy, the clocked comparator is turned ON to evaluate the harvester $V_{OC}$. If $V_{OC}$ exceeds 0.6V then reciprocal converter is turned ON, else direct operation mode is enabled. The comparator is read through a function call as shown in Fig.13b.

MPPT was tested by using a variable intensity light source with the wavelength of the test lamp chosen to closely match that of indoor fluorescent/LED lighting. Fig. 14 shows the illumination variation over the 20 minute test-period. The specific levels of intensity were arbitrarily chosen between 4 and 1118 lux. Multiple PV cells were tested and the harvested power level is shown in the lower pane of Fig.14. The minimum light levels at which the control loop decides to

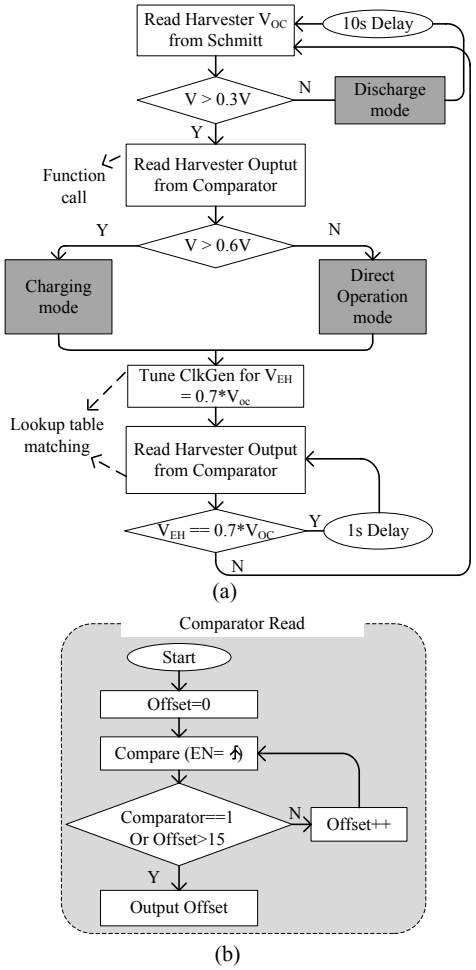


Fig. 13. Control algorithm (a) for fractional $V_{OC}$ tracking and (b) function call for reading comparator.

enable harvesting depends on PV cells as does the magnitude of harvested power. Note that peak power harvested at about 20 lux is in excess of 1µW, with 100µW at 1000 lux. These values are in line with prior findings [18].

The control algorithm autonomously detects changes in light levels according to the flowchart in Fig. 13 and tunes the converter frequency for MPPT. When the light level changes

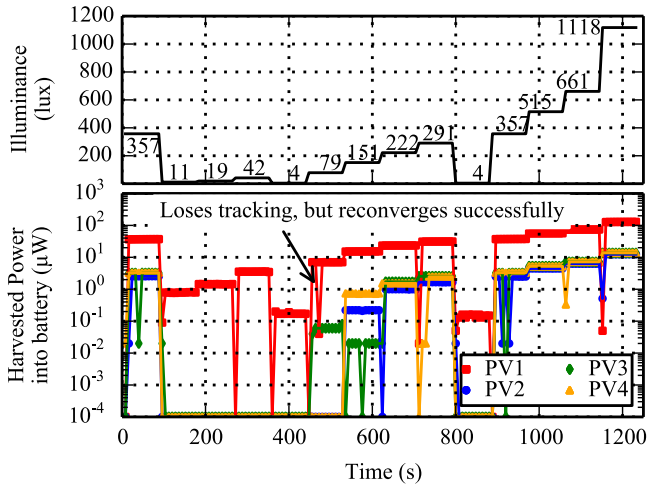


Fig. 14. Runtime performance of control algorithm for varying light levels measured for multiple harvesters.

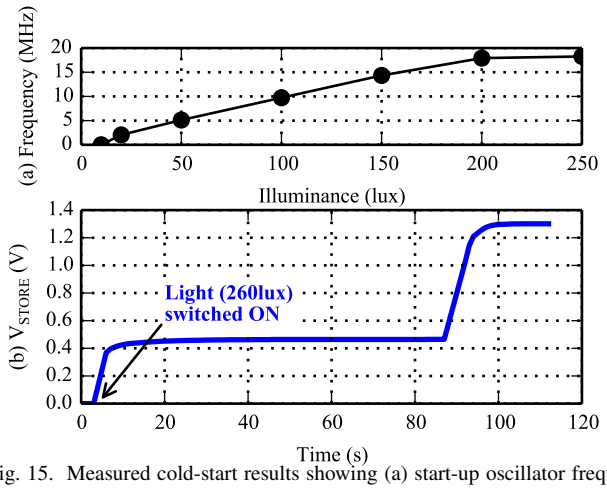


Fig. 15. Measured cold-start results showing (a) start-up oscillator frequency vs. illuminance and (b) voltage build up on a capacitor with zero initial voltage vs. time.

significantly, the loop restarts resulting in zero harvested power for a short duration. However, for moderate intensity changes the loop self-adjusts as though a minor MPPT perturbation was observed. There are cases where the algorithm loses tracking, potentially because of comparator jitter, despite ambient conditions remaining static, but manages to successfully reconverge to the optimal setting (highlighted in Fig. 14). Note that this loss of convergence does not affect execution of the ULPBench benchmark software as the loss of harvested energy is limited to at most 1s (loop speed), which is easily covered by the decoupling capacitance used in the system.

### C. Cold Start

Cold-start is necessary in autonomous energy harvesting systems to ensure they can boot-up from zero initial energy. Converters and control logic should therefore be designed to operate from very low voltages. At low voltages, converter switches have poor conductance but will remain functional as would the fly-capacitors. The bigger challenge to enable cold-start is a reliable clock source. To overcome this problem prior works [12] have used a self-oscillating SC converter while others [11] have employed short chain CSO. For the latter case, the oscillator speed at higher voltages is limited by loading internal nodes of the CSO with large (1.2pF) capacitors costing dynamic power. This design uses a 96 stage ring oscillator with start-up voltages as low as 90mV. The frequency may be non-optimal [11] for the converter at higher input voltages but as long as $V_{STORE}$ can charge to sufficient levels to allow the control logic to take over, a deterministic boot-up is possible.

Fig. 15 (a) illustrates the start-up oscillator frequency vs. illuminance. Oscillations start reliably at very low light levels but for indoor light levels (250-500 lux) the frequency can be in excess of 16MHz. To accelerate testing and to overcome assistance from battery self-recovery, this measurement was carried out with a fully discharged 33µF electrolytic capacitor. The results in Fig. 15 (b) show the capacitor voltage at 260 lux. Once oscillations start, $V_{STORE}$ charges to 400mV and then saturates as the start-up oscillator is too fast for the SCC. Once $V_{STORE}$ reaches ≈450mV, the control logic enables the PCG allowing a more suitable switching frequency. $V_{STORE}$ reaches ≈1.25V before saturating.

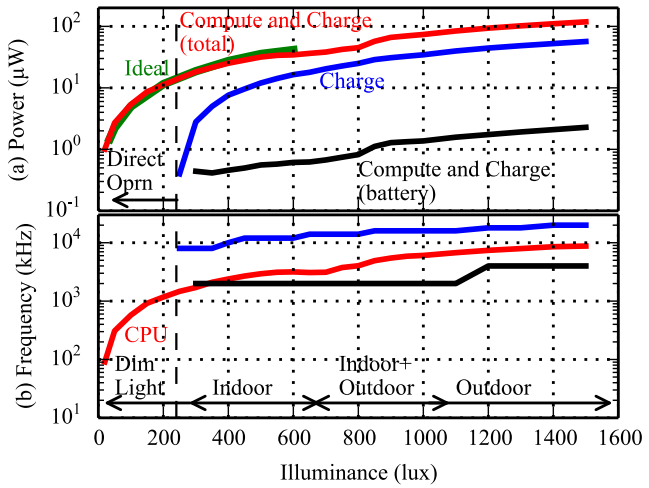


Fig. 16. Measured results showing benefits of direct-operation with (a) Extracted power in different modes and (b) corresponding CPU-system and SC converter frequency vs. light levels.

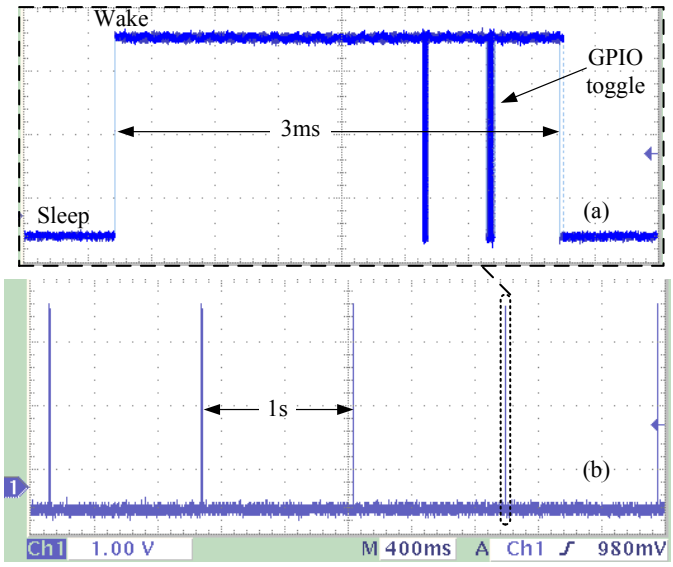


Fig. 17. Oscilloscope waveform demonstrating ULPBench execution .

### D. System Performance

Sensor workloads are heavily duty-cycled and the energy requirements depend on the active:sleep ratio. The results here are captured for 100% CPU activity and CPU sleep mode so that any real-world application would lie between these two extremes depending on the active:sleep ratio as dictated at run-time. Fig. 16 shows the overall system behavior and performance vs. incident light levels. Both direct operation and charge modes are shown. At low light levels the reciprocal converter is disabled and only power drawn by the MinE CPU system for computation (checksum) is shown. At higher light levels (>220 lux), the converter is enabled and some of the energy is used to charge the battery as indicated by the 'Compute and Charge (battery)' trace.

When the CPU is in sleep mode, all harvested energy is used to charge the battery. The corresponding CPU system and converter frequencies are shown in Fig. 16b. During CPU operation the converter frequency is reduced to minimize the power drawn from storage, and when the CPU system sleeps over long intervals the SCC frequency is chosen to ensure MPPT. Note that for most indoor and dim light conditions the utilized power matches the ideal PV harvested power. This is evidence of CPU rail-impedance matching PV cell's output impedance during direct operation. The ideal output power trace was obtained using IV sweeps to identify the maximum power point.

TABLE II
SYSTEM POWER BREAKDOWN IN DISCHARGE MODE.

| | |
|---|---|
| CPU system | 0.6 $\mu$W |
| Converter overhead (worst-case 60%$\eta$) | 0.4 $\mu$W |
| PCG + mux at 14MHz for 5ms | 0.05 $\mu$W |
| Control logic (worst-case, same as CPU) | 0.6 $\mu$W |
| **Total** | **1.65 $\mu$W** |

Based on measurements (Fig. 2), 16% additional harvested energy is used by the CPU system without associated conversion losses when voltage of harvested energy is below 0.6V. Even assuming the converter retains peak efficiency in both directions over the entire load current range, this 16% additional energy translates to 30% additional compute cycles for the same cm$^2$ harvester and ambient conditions.

### E. Energy-Neutrality and Operation of EEMBC Benchmark

Energy-neutral operation is possible if the system can survive the worst case energy drain on the 6mAh battery. the discharge mode of operation exhibits the worst case energy drain compared to both charging and direct operation modes. During discharge mode of operation, the control logic, PCG and the mulitplexer (Fig. 5) add to the overheads. The slow Schmitt comparator is used at 10s intervals but this is powered from the PV cell and hence does not drain the battery. Therefore the available 24hr power budget from the 6mAh, 1.2V battery is 144μW (assuming a non-ideality factor of 0.48 [19] to account for voltage drop during battery discharge and other temperature related effects). The power breakdown for the system in discharge mode (Table II) indicates that the system can operate for 87days before requiring a full recharge

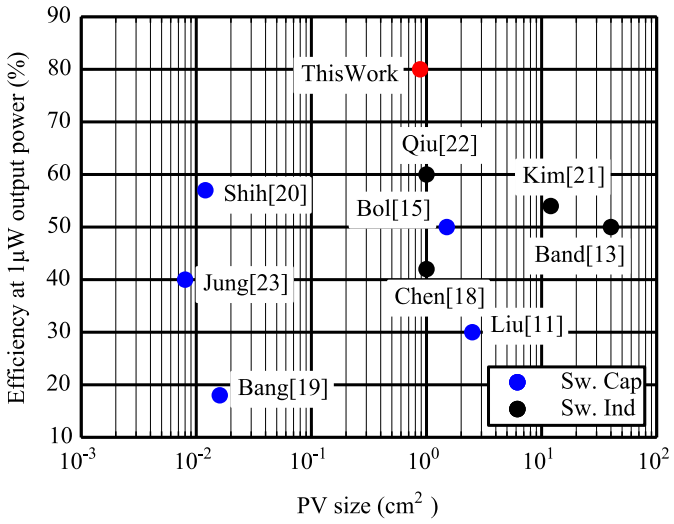


Fig. 18. Comparison with prior-works for low-light efficiency (1μW).

TABLE III
HARVESTER PERFORMANCE COMPARED WITH RELATED WORKS

| | Liu [11] | Bol [15] | Chen [20] | Bang [21] | Shih [22] | Kim [23] | Qiu [24] | Band [13] | Jung [12] | This work |
|---|---|---|---|---|---|---|---|---|---|---|
| **Node (nm)** | 180 | 65 | 65 | 180 | 350 | 350 | 250 | 350 | 180 | 65 |
| **$V_{in,pv}$(V)** | 1.1-1.5 | 0.95-2.7 | >0.08 | 0.36-0.8 | 1.8 | 1.5-5 | 0.5-2 | 0.15-0.75 | 0.14-0.5 | 0.58-1.5* |
| **$V_{out}$(V)** | 3.3 | 3 | 1.3 | 3.3 | 1.4 | 4 | 5 | 1.8 | 2.2-5.2 | 1.2 |
| **$P_{out}$(µW)** | <21 | 5-10000 | <80 | 0.013-20 | <10 | 800 | 5-1000 | 2500 | 0.005-5 | 0.02-100 |
| **$\eta_{peak}$(%)** | 86.4 | 80 | 72 | 39.8 | 58 | 84 | 70 | 87 | 50 | 84$ |
| **$\eta_{1\mu W}$(%)** | <30 | - | <42 | <18 | <57 | <54 | <60 | - | 40 | >80 |
| **$A_{macro}$ ($mm^2$)** | 2.25 | 0.48 | 0.245 | 0.95 | 0.42 | 4.71 | 10.34 | 25 | 0.86 | 0.037 |
| **$A_{pv}$ ($cm^2$)** | 2.5 | 1.5 | ideal | 0.016 | 0.012 | 12 | ideal | 40 | 0.008 | 0.88 |
| **Reactance** | Int. C | Int. C | L | Int. C | Int. C | L | L | L | Int. C | Int. C |

*To support charge+compute. Minimum $V_{in,pv}$ depends on ambient light. $ From Fig.12

Fig. 17 shows the MinE CPU system running ULPBench benchmark code. The measurement was carried out at 160 lux. Fig. 17b shows the system waking up at 1s intervals and performing sensor activities. Fig. 17a shows the active duration with the system performing initialization sequences and the GPIO toggle initiated during code execution [2]. From the results in Fig. 14 it can be seen that the system can be energy-neutral when exposed to 50 lux continuously or 250 lux (indoor lighting) for as little as 2 hours per day. Fig. 18 compares state-of-the-art energy harvesting converters vs. harvester area showing 80% conversion efficiency while harvesting into a 1.2V battery from a $cm^2$ PV cell.

Table III presents a comparison with prior works. This work presents the smallest SCC macro with integrated clock sources. The converter offers a peak conversion of 84%. The system can also cold-start at 260 lux and exploits the low functional voltages of sub-threshold CPUs to enable selective direct operation achieving energy-neutral operation.

## VI. CONCLUSION

Energy-neutrality is a challenging objective in energy harvesting systems especially when the harvester volume is constrained to $cm^2$ form-factor. This work presented selective direct operation and reciprocal conversion techniques to reduce silicon area and maximize energy utilization, and was shown to achieve energy-neutral operation from a compact PV cell under indoor lighting conditions. The proof of concept prototype chip was demonstrated for a system executing industry-standard sensor benchmark software which demands approximately 20k instructions per second. The reciprocal converter presented has the highest bidirectional conversion efficiency. Circuit novelties were presented for low power analog assist blocks (comparator and PCG) to achieve an optimal system performing autonomous MPPT. Successful cold-starting was demonstrated at low light levels. Future work is anticipated to demonstrate successful functionality while harvesting energy from other energy sources such as thermoelectric generators. The techniques presented in this work demonstrate potential solutions to key challenges in enabling energy-neutral sensing systems.

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