Fabrication of Arbitrarily Narrow Vertical Dielectric Slots in Silicon Waveguides

Kapil Debnath, Ali Z. Khokhar, Graham T. Reed, Shinichi Saito

***Abstract*— Slot waveguides are used for many photonic applications. However, existing fabrication techniques impose restrictions on the width of the slot region. Here we propose and experimentally demonstrate a fabrication process to realize an arbitrarily narrow vertical dielectric slot in a silicon waveguide. Using this fabrication method we have realized silicon slot waveguides with a 10 nm oxide slot region. The propagation loss of the fabricated slot waveguide was 1.36±0.3 dB/mm.**

***Index Terms*—Silicon photonics, slot waveguide, accumulation type modulator, light source, opto-mechanics.**

I. Introduction

SLOT waveguides, due to their unique light confinement capability, have been exploited for many different photonic applications, such as sensing [1], light emission [2,3], nonlinear photonics [4], opto-mechanics [5,6]. In its simplest form, a slot waveguide consists of a low-refractive-index-contrast dielectric region (e.g. SiO_2 or polymer) sandwiched between two high-refractive-index (e.g. silicon) waveguide regions. Due to such a refractive index profile, one of the propagating modes tends to confine the optical energy within the low-refractive-index slot region, as shown in Fig. 1. More importantly, the energy density within the narrow slot region increases as the slot width decreases, resulting in a stronger light-matter interaction. For example, Jun et al. [3] has analytically shown that for a silicon slot waveguide with Erbium-doped oxide in the slot region, the spontaneous emission efficiency increases monotonically when the width of the slot region is reduced and for a 20 nm wide slot, the efficiency increases by over an order of magnitude. For optomechanical systems, utilizing slotted waveguide designs, we can see that the optomechanical coupling rate increases as the slot width reduces [5]. Another important application in silicon photonics which also needs an extremely narrow dielectric slot (<10 nm) within a silicon waveguide is an accumulation-type electro-optic modulator. Such devices work on the same principle as a Metal-Oxide-Semiconductor (MOS) capacitor and the device efficiency strongly depends on the width of the oxide region. Such a modulator design was first discussed in [7] and shown to have better modulation efficiency in comparison to existing modulation mechanisms [8,9]. However, realizing vertical dielectric slots with widths below 50 nm is relatively difficult with standard lithography techniques.

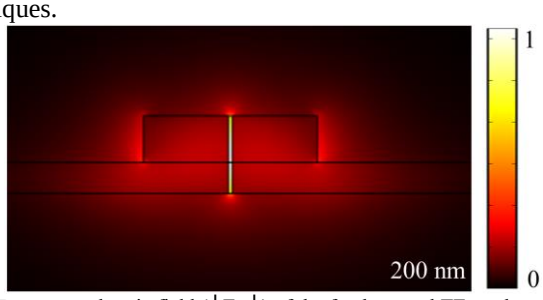

Fig. 1. Dominant electric field ($|Ex|$) of the fundamental TE mode guided by the silicon slot waveguide on a buried oxide (BOx) substrate with a PECVD deposited oxide surrounding medium. The waveguide is 200 nm high and the slot width is 10 nm with 225 nm wide silicon arms on both sides. The slab height is 80 nm.

In this letter, we propose and demonstrate, to our knowledge for the first time, a fabrication method to realize silicon waveguides with an arbitrarily narrow vertical dielectric slot region. Unlike the conventional fabrication process where both the slot and the waveguide are fabricated simultaneously, we used a sequential approach to realize the slot and the waveguide. In our structure, one section of the waveguide is single-crystal silicon-on-insulator (SOI) and the other side is a deposited silicon layer and the dielectric slot region is a thermally grown oxide layer. Due to the use of thermal oxide, we could precisely control the width of the slot region. We have divided the following discussion into two sections. In section II, we give details of the fabrication process flow, and in section III we discuss the fabricated devices and optical performance of the waveguides.

II. Fabrication Process

For fabricating the waveguides, we used a 6 inch SOI wafer with 220-nm-thick top silicon layer on 2-µm-thick Buried Oxide (BOx). The surface orientation of the top silicon layer was (110). We started the fabrication process by growing a 20

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nm of thermal oxide on the top silicon layer. For this oxidation process the wafer was annealed at 1000ºC in O_2 (dry anneal) for 6 minutes in a quartz furnace tube. The wafer was then spin-coated with a 450 nm thick e-beam resist ZEP-520A. Using e-beam lithography, the resist layer was exposed with rectangular patterns of different lengths and widths. After developing the exposed region using ZED-N50 resist developer, the patterns were transferred to the top silicon layer to create trenches, as shown in Fig. 2b, using an inductively coupled plasma (ICP) etcher with SF_6/C_4F_8 chemistry. Since the final slot waveguide would be formed around one of the side walls of the trench region, the surface roughness of the side wall would contribute to the overall loss of the slot waveguide. In order to smoothen the trench side wall roughness, we used Tetramethylammonium hydroxide (TMAH) based wet etching process. Using this process we have previously demonstrated low-loss silicon strip and slot waveguides [10,11]. Details of such smoothening process can be found in [11]. Once the trench region was created, the wafer was oxidized again to form the narrow dielectric region of the slot waveguide. Here we annealed the wafer at 950ºC for 2 mins to grow 10 nm of thermal oxide on the side walls of the trench, as shown in Fig. 2c. The oxide growth was monitored using a control wafer with surface orientation of (111). Since we are using thermal oxidation to realize the dielectric, the slot region can be arbitrarily narrow and uniform which is not possible with standard lithographic processes. The oxide layer on one of the side walls was then selectively covered using resist. Here we used negative e-beam resist UVN-30 and the entire wafer was dipped into Hydrofluoric Acid (HF) to remove the thermal oxide from everywhere except the resist covered regions, as shown in Fig. 2d. After removing the resist layer and a quick HF clean, to remove any native oxide, a 300 nm thick layer of amorphous silicon was deposited onto the wafer using plasma enhanced chemical vapor deposition (PECVD) process. The final HF cleaning step was necessary to ensure that there was no intermediate layer between the crystalline SOI layer and the deposited amorphous silicon layer over the entire wafer. The wafer was then annealed at 1000ºC in N_2 for 10 hours. The goal of this step is to crystallize the deposited amorphous silicon. Since the deposited amorphous silicon layer is connected directly to the crystalline SOI layer, we expected to achieve complete recrystallization of the deposited amorphous silicon layer into single-crystal, as the recrystallization process is initiated by the single-crystal SOI seed layer. The motivation behind this recrystallization process was to achieve single-crystal silicon on both sides of the slot to achieve low propagation loss. Here it is important to highlight that this fabrication process will also work without this recrystallization step, however the deposited silicon will be either amorphous or polycrystalline, which tend to have more loss in comparison to single-crystal silicon. After the recrystallization process, the wafer was planarized down to 200 nm thick top silicon layer using chemical mechanical polishing (CMP), as shown in Fig. 2g. Finally, using e-beam lithography and an ICP dry etching process, rib waveguides were fabricated with 10 nm oxide region at the center of the waveguide. The rib waveguides were 450 nm wide with 80 nm high slab regions. The waveguides were then coated with a 1 µm thick PECVD SiO_2 cladding before measurement.

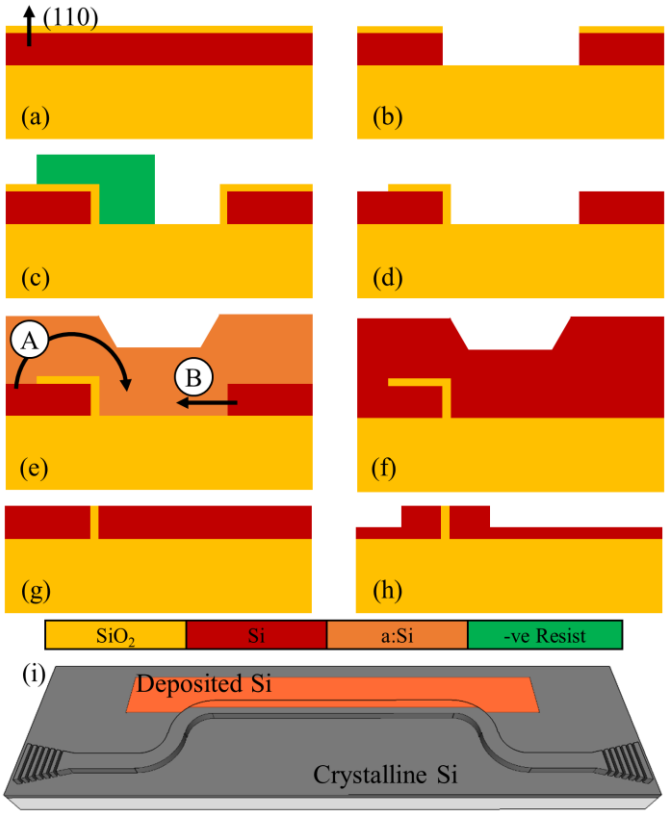

Fig. 2. Fabrication process flow: (a) 20 nm thick thermal oxide was grown on a (110)-oriented SOI wafer, (b) A trench was created in the top silicon layer using a combination of dry and wet etching process, (c) A 10 nm thick oxide was thermally grown on the trench side walls and one side wall of the trench was covered with negative resist, (d) Thermal oxide was selectively removed from everywhere except one of the trench side walls. (e) 300 nm of amorphous silicon was deposited using PECVD system. The arrows indicate the two different recrystallization paths of the deposited silicon within the trench region, (f) Deposited silicon layer was recrystallized with the help of single-crystal SOI layer, (g) The silicon layer was planarized using CMP down to 200 nm, (h) Rib waveguide was fabricated with 10 nm oxide region at the center of the waveguide. (i) Schematic of the slotted rib waveguide showing the relative position the deposited silicon region with respect to the waveguide position.

III. Observations and Measurements

As mentioned in the previous section, our design used different trench lengths and widths. Different trench lengths were used for estimating the propagation loss through the slot waveguides, whereas the motivation behind using different trench widths was to find the right condition for recrystallization of the deposited silicon within the trench region. Figs. 3a (3c) and Fig 3b (3d) show the cross-sectional (top) view of the deposited silicon layer around the trench regions after the recrystallization and before CMP processes for trench widths of 2 µm and 500 nm, respectively. After the 10 hour long recrystallization process, we found about 50 nm of thermal oxide had grown on top of the deposited silicon layer. This is visible in Fig. 3a and 3b. We believe this was due to the presence of some O_2 in the N_2 flow during the annealing process. Figs. 3c and 3d were taken after removing the thermal oxide layer. This step also enhances any poly grain boundaries

of the recrystallized layer. In Fig. 3a and 3c, we can clearly see poly grains within the trench region, although there were no poly grains observed outside the trench region confirming complete recrystallization of the deposited silicon layer. Interestingly, for a trench width of 500 nm, we did not observe any poly grains even within the trench region, resulting in a complete recrystallization of the deposited silicon within the trench region. This is apparent from Fig. 3b and 3d.

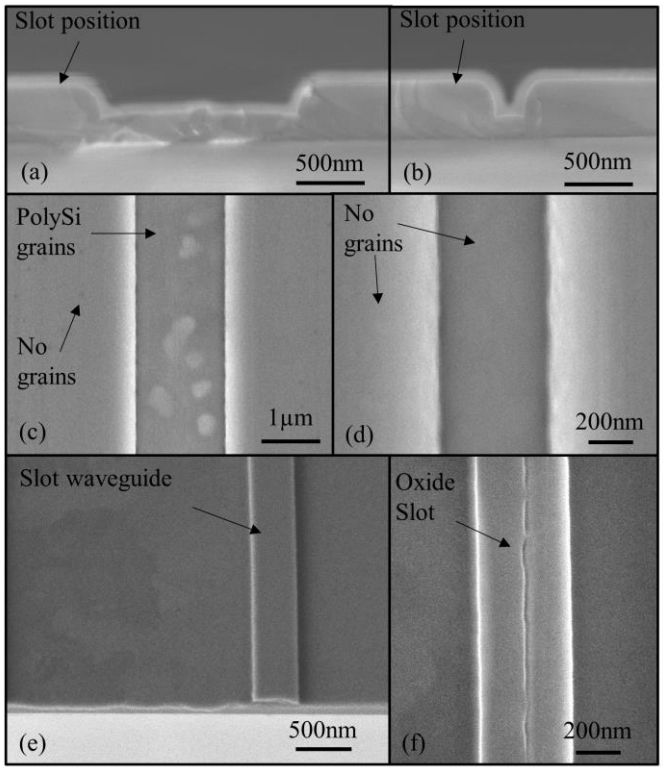

Fig. 3. Cross-sectional SEM image of the deposited silicon layer around the trench region of width (a) 2 µm and (b) 500 nm. Top view of the deposited silicon layer around the trench region of width (c) 2 µm and (d) 500 nm. (e) Fabricated rib waveguide with 10 nm oxide slot at the center. (f) The position of the exposed oxide trench after HF etch.

Figures 3a-3d suggest that the recrystallization of the deposited silicon within the trench region can be controlled simply by adjusting the width of the trench. As shown in Fig. 2e, there are two possible directions of recrystallization of the deposited silicon within the trench region: (A) From the exposed single-crystal silicon seed region close to the oxidized side wall of the trench and (B) from the exposed side wall of the trench itself, acting as seed layers. During the long anneal, recrystallization happens along both the directions. But if the trench region is narrow enough, so that the entire trench region is recrystallized along one of the directions before the other, we would expect a complete single-crystal region within the trench. In our current process, we found that 500 nm wide trench results in such a single-crystal region. On the other hand, if the trench region is relatively wide we would expect at least one grain boundary within the trench region. Moreover, poly grains will also form within the trench region, due to the presence of BOx layer underneath, before they can be recrystallized using the seed regions. This is what we found for any trench width over 500 nm. This suggests that the narrower the trench, the better chance of recrystallization. However, for narrow trench regions we found that the PECVD deposition rate within the trench is slower. This is obvious from the thickness difference of the deposited silicon layer within the 2 µm (Fig. 3a) and 500 nm (Fig. 3b) wide trenches. Moreover, there is also the possibility of creating voids within the deposited layer.

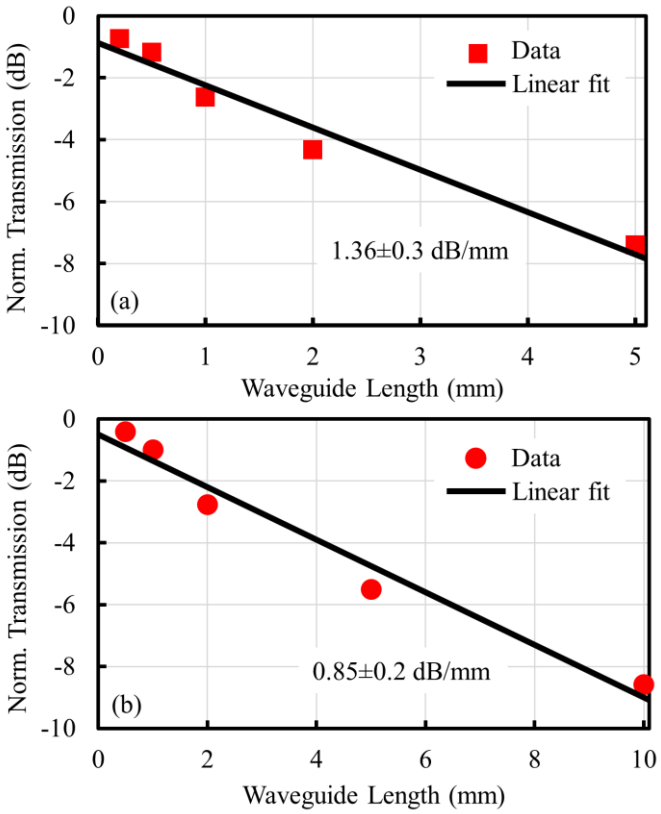

Fig. 4. Normalized optical output power vs. waveguide length for (a) slot waveguide with 10 nm wide slot and (b) rib waveguide at 1550 nm wavelength.

Therefore, for more reliable trench filling a wider trench is preferred. Even though, in such cases, we expect poly grain formation near the center of the trench, we found that closer to the oxidized side wall the deposited silicon became completely crystallized. This is apparent from Fig. 3e and 3f, where the 10 nm oxide slot is located at the center of the waveguide. Figure 3f gives a zoomed-in view of the waveguide with the 10 nm slot region clearly visible. To highlight the oxide slot, we dipped the sample in HF for 10 minutes to remove some of the thermal oxide within the slot. We could easily see the poly silicon grain boundaries away from the waveguide region, however, within the rib region we did not see any poly grain boundaries and the silicon was purely single-crystalline. The apparent roughness along the slot region we believe is an artifact from the HF wet etching process. Since the slot region was extremely narrow, we believe that the HF did not attack the oxide uniformly and hence the etching was not uniform along the waveguide giving an impression of bending, connected regions and roughness.

Next we carried out transmission loss measurements to determine the optical performance of the fabricated slot waveguides. To measure the transmission through the slot waveguides, we used a fiber-grating coupler set up and a tunable laser source with tuning range from 1530 nm to 1630

nm. Because of the thickness, the waveguides only supported a quasi-TE mode. Launching of quasi-Transverse Electric (TE) mode into the waveguide was ensured with the help of a fiber polarization controller and grating couplers. For estimating the propagation loss, a cut-back method was used. A schematic of the complete waveguide structure is shown in Fig. 2i. The grating couplers and the access waveguides were fabricated in the crystalline silicon. At the transition region between the all-silicon access waveguides and the slot waveguides, waveguide bends with 50µm radius were used to achieve a gradual transition between the waveguide regions. Waveguides with slot sections with 5 different lengths: 200 µm, 500 µm, 1 mm, 2 mm and 5 mm were designed. The red squares in Fig. 4a represents the normalized transmission through waveguides for different slot lengths. The transmission data were normalized by setting the background loss to zero. The black line represents the linear fit for the transmission data. From the linear fit, we estimated that the propagation loss to be 1.3±0.3 dB/mm for the slot waveguides. This value is relatively high in comparison to previously reported results for single-crystal silicon slot waveguides [11,12]. To understand the source of this relatively high propagation loss, we have also measured the propagation loss of simple all-crystalline silicon rib waveguides fabricated on the same wafer. The transmission data are shown in Fig. 4b and from the linear fit we estimated the propagation loss to be 0.85±0.2 dB/mm. This value is also higher than the typical propagation loss of 0.3 dB/mm for silicon waveguides. We believe this higher loss is a result of roughness caused due to the CMP process. After CMP the roughness of the top surface of the wafer was 8 nm (rms value), whereas for a typical SOI wafer the surface roughness is below 1 nm (rms value). Another possible source of loss in our slot waveguides could be the interface defects between the oxide layer and the deposited silicon, which could arise during the deposition process.

IV. Conclusion

In this work we have developed a fabrication process to realize extremely narrow dielectric slots within silicon waveguides. In our fabrication process, we took a sequential approach of realizing the slot region first using thermal oxidation and where one section of the waveguide is a single-crystal SOI, the other section is a deposited silicon layer. The deposited silicon layer was eventually recrystallized during long thermal anneal. Using this process, we have realized single-crystal silicon on both sides of the dielectric slot. The propagation loss through the fabricated slot waveguides, with 10 nm wide oxide slot, was found to be 1.36 ±0.3 dB/mm. We believe that the major contributor to this loss is the surface roughness of the top silicon layer after CMP process. This loss value can be significantly reduced by minimizing the surface roughness using an optimized planarization process.

References

[1] C. A. Barrios, K. B. Gylfason, B. Sánchez, A. Griol, H. Sohlström, M. Holgado, and R. Casquel, "Slot-waveguide biochemical sensor," *Opt. Lett.*, vol. 32, pp. 3080-3082, Sept. 2007.

[2] R. Guo, B. Wang, X. Wang, L. Wang, L. Jiang, Z. Zhou, "Optical amplification in Er/Yb silicate slot waveguide," *Opt. Lett.*, vol. 37, pp. 1427-1429, May 2012.

[3] Y. C. Jun, R. M. Briggs, H. A. Atwater, and M. L. Brongersma, "Broadband enhancement of light emission in silicon slot waveguides," *Opt. Exp.*, vol. 17, pp. 7479-7490, Apr. 2009.

[4] A. Martínez, J. Blasco, P. Sanchis, J. V. Galán, J. García-Rupérez, E. Jordana, P. Gautier, Y. Lebour, S. Hernández, R. Spano, and R. Guider, "Ultrafast all-optical switching in a silicon-nanocrystal-based silicon slot waveguide at telecom wavelengths," *Nano lett.*, vol. 31, pp. 1506-1511, Mar. 2010.

[5] Y. Li, J. Zheng, J. Gao, J. Shu, M. S. Aras, and C. W. Wong, "Design of dispersive optomechanical coupling and cooling in ultrahigh-Q/V slot-type photonic crystal cavities," *Opt. Exp.*, vol. 18, pp. 23844-23856, Nov 2010.

[6] M. Eichenfield, R. Camacho, J. Chan, K. J. Vahala, and O. Painter, "A picogram-and nanometre-scale photonic-crystal optomechanical cavity," *Nature*, vol. 459, pp. 550-555, May 2009.

[7] G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, "Silicon optical modulators," *Nat. photon.*, vol. 4, pp. 518-526, Jul. 2010.

[8] B. Milivojevic, S. Wiese, J. Whiteaway, C. Raabe, A. Shastri, M. Webster, P. Metz, S. Sunder, B. Chattin, S. P. Anderson, and B. Dama, "Silicon high speed modulator for advanced modulation: device structures and exemplary modulator performance," *Proc. SPIE*, vol. 8990, pp. 899013-899013, Mar. 2010.

[9] M. Douix, D. Marris-Morini, C. Baudot, S. Crémer, D. Rideau, D. Perez-Galacho, A. Souhaité, R. Blanc, E. Batail, N. Vulliet, and L. Vivien, "Design of integrated capacitive modulators for 56 Gbps operation," *Proc. IEEE*, pp. 90-91, Aug 2016.

[10] K. Debnath, H. Arimoto, M. K. Husain, A. Prasmusinto, A. Al-Attili, R. Petra, H. M. H. Chong, G. T. Reed, and S. Saito, "Low loss silicon waveguides and grating couplers fabricated using anisotropic wet etching technique," *Front. Mat.*, vol. 3, pp. 10, Feb. 2016.

[11] K. Debnath, A. Z. Khokhar, S. A. Boden, H. Arimoto, S. Z. Oo, H. M. H. Chong, G. T. Reed, and S. Saito, "Low-loss slot waveguides with silicon (111) surfaces realized using anisotropic wet etching," *Front. Mat.*, vol. 3, pp. 51, Nov. 2016.

[12] R. Ding, T. Baehr-Jones, W. J. Kim, X. Xiong, R. Bojko, J. M. Fedeli, M. Fournier, and M. Hochberg, "Low-loss strip-loaded slot waveguides in silicon-on-insulator," *Opt. Exp.*, vol. 18, pp. 25061-25067, Nov. 2010.