

# A CMOS MF energy harvesting and data demodulator receiver for wide area low duty cycle applications with 250 mV start-up voltage

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**Abstract** A low voltage start-up energy harvesting medium frequency receiver is presented, for use as the power and synchronisation part of a remote sensor node in a wide area industrial or agricultural application. The use of embedded low bandwidth network synchronisation data permits very low operational duty cycle without the need for real time clocks or wake up receivers at each node with their associated continuous power drain. The receiver consists of a rectifier, a power management unit and a phase-shift keying demodulator. The rectifier is optimised for low start-up and operating voltage rather than power efficiency. With standard MOS thresholds the rectifier can cold start with only 250 mV peak antenna input, and useful battery charging is delivered with 330 mV peak input. The QPSK demodulator consumes 1.27  $\mu$ W with a supply voltage of 630 mV at a data rate of 1.6 kbps with 1 MHz carrier frequency. The IC is implemented in a standard threshold 0.18  $\mu$ m CMOS technology, occupies 0.54 mm<sup>2</sup> and can deliver 10.3  $\mu$ W at 3 V to an external battery or capacitor.

**Keywords** Energy scavenging · Dead zone · Rectifier · Phase-shift keying (PSK) demodulator

## 1 Introduction

Remote sensor networks are becoming well established with the availability of very low power IC technology. For many applications, a simple battery remains the most sensible choice of power, and service lifetimes of several years are common. Where access for maintenance is restricted, energy harvesting or scavenging systems have become popular allowing indefinite operation. Photovoltaic cells are a common and very successful source provided that adequate illumination is available [1, 2], and in some industrial environments, periodic vibration from machinery can be used successfully [3].

For agricultural and industrial applications power can be obtained by a variety of methods depending on the specific circumstances. Where photovoltaic generation is not practical, wireless power becomes attractive [4–10]. Rather than attempt to recover adequate power from an ill-defined ambient electromagnetic environment at some high frequency, we investigate supplying power in the near field via very weak magnetic coupling from a medium frequency source using a large-area loop. In this frequency range a ferrite-cored loop receiver antenna may be used to increase effective area and ensure acceptably small volume [10]. The use of a lower-frequency source also reduces problems associated with localised signal attenuation due to walls etc., making deployment in less well-defined environments easier. The current in the transmitting loop is not a major issue provided that levels are not impractical and that the power required for the energising source does not exceed the limits of a single-phase AC mains outlet.

A further benefit of using a specified source is that low speed management and control data may be transmitted such that there is no significant bandwidth penalty. The average power consumption of a receiver and the

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associated sensor system can be significantly reduced by decreasing the active duty cycle, but such schemes require accurate synchronisation between transmitter and receivers, usually incurring the power overhead of real time clocks or wake-up receivers [11, 12]. In the proposed scenario, a receiver could receive an *activate* or *sleep* command from the transmitter by means of the slow data modulated onto the power source magnetic field. This approach provides the opportunity to deploy a number of sensor nodes operating at very low duty cycle ratios without the associated continuous power drain of internal timing or wake-up circuits [13–16].

To achieve a workable operating range in a physically small unit, the receiver power recovery circuits must be able to initiate operation from an unpowered condition (“cold start”) with the lowest possible voltage induced in the antenna coil, and hence with the weakest magnetic field in a given operation area. Rather than focus on power transfer efficiency, we have instead given priority to ensuring that the receiver can cold start with the minimum voltage at the antenna coil. It is envisaged that the operational duty cycle of the complete system can be adjusted to match the available power from the receiver, even if it is not operating at a theoretical optimum power efficiency. The main effort of this work is hence directed at demonstrating the feasibility of an IC that performs the functions of rectifier, power management and demodulator for the low speed embedded control data.

We first describe the overall architecture for the proposed system, and then the requirements for the receiver IC. We then present some aspects of the circuit design and show measured results from laboratory and field experiments.

## 2 System architecture

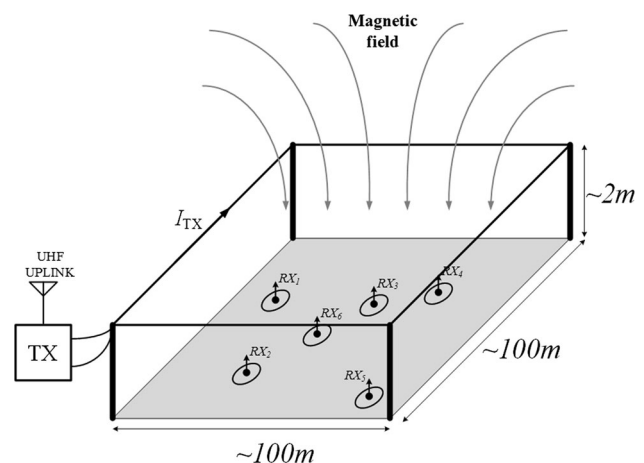
### 2.1 Wide-area MF loosely-coupled magnetic power transfer

Much research has been directed into harvesting or scavenging power from electromagnetic sources. In the main, these works have investigated extracting energy from the ambient conditions in the UHF and low microwave regions from cellular and wireless LAN transmissions [4–10, 16, 17]. At these frequencies, a physically small antenna can easily be of the order of a wavelength and thus achieve good efficiency. Whilst potentially attractive from the user’s perspective, there are some drawbacks. Any such receiver requires a finite voltage from a very simple antenna to overcome the forward voltage in the rectifier circuits, and this can imply a relatively large field strength. Operation at UHF also tends to increase the internal losses

in the rectifier due to parasitic capacitances on internal circuit nodes. Further, if the source is an RF service intended for another purpose, such as a cellular network, the field strength at the intended location may show considerable variation. Propagation can be an addition issue as the systems will be constrained to essentially line of sight or with only minor obstructions.

In this work, we consider the requirements of end use applications where more conventional methods of power delivery are not practical, or line of sight RF propagation is not possible, thus excluding UHF and microwave solutions. Such restrictions can exist in industrial and agricultural locations, but the site may well be suited to the use of a dedicated RF source. Figure 1 shows a possible configuration for such a wide area medium frequency (MF) magnetic, loosely-coupled, energy-harvesting system. A magnetic field is created by a large loop antenna that may be fixed close to the boundary of the deployment site. The power for the MF transmitter current can be from any convenient source, and in most cases AC mains will be typically available for other small industrial equipment.

The sensors, represented by several secondary coils, harvest energy from the magnetic field within the transmitter loop. The use of ferrite cores is the obvious choice to be able to reduce the physical size of a practical receiver to a few  $\text{cm}^3$ . The requirement for the magnetic system is to provide enough voltage at the receiver antenna coil terminals to activate the harvesting electronics. For the intended applications, the precise antenna voltage is undefined and likely to be very small, and further, will depend on the physical siting of the receiver. For the given transmitter loop coil size of  $100 \times 100 \text{ m}^2$ , the calculated coupling coefficient [18] between the source and the ferrite cores secondary coil with the physical size of a few  $\text{cm}^3$  is below  $10 \mu$ . In practice, the lower limit for the system to



**Fig. 1** Wide area MF magnetic loosely coupled energy harvesting concept

cold start is strongly linked to the semiconductor technology used, in terms of the forward voltage needed to activate a rectification function. The factors involved are discussed in more detail later; in this demonstrator system the target was set at 250 mV which is well below the threshold voltage ( $V_{th}$ ) of the process technology used in this work. The CMOS technology used was chosen primarily for reasons of cost and availability, and the device thresholds are optimised for digital circuitry. If low threshold MOS devices had been available then cold starting could be expected with significantly lower input voltage.

Figure 2 shows a plot of the magnetic field created by an example configuration of a 10 m  $\times$  10 m loop (as used in the experimental measurements). It can be seen that the field is relatively constant within the loop, and decays rapidly outside its perimeter [19], making interference with other spectrum users unlikely. Note that while the regulatory framework in many territories does not currently permit such proposed systems, some territories are permitting experimental work, and it is likely that the declining use of MF broadcasting will make narrow band non-radiating systems more acceptable elsewhere.

## 2.2 Synchronisation protocol

Almost all remote sensors are configured to operate with a low active duty cycle, as this enables very significant power savings when data collection is only needed at a very slow sample rate. An estimation of the average power required by a smart sensor node can be made using Eq. (1), where  $P$  is the average power consumption,  $P_n$  is the power consumption of the module,  $t_n$  is the active

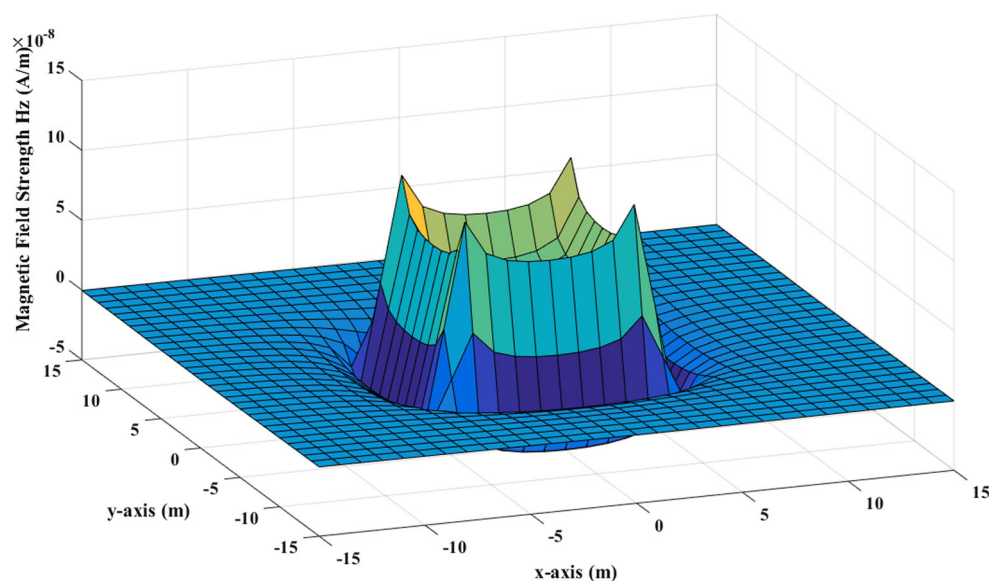
time of the module per period and  $t_T$  is the total time period.

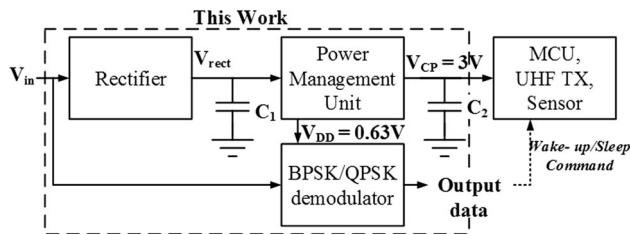
$$P = \frac{P_1 t_1 + P_2 t_2 + P_3 t_3 + \dots}{t_T} \quad (1)$$

The duration of the active time will not have much flexibility, constrained by the operation of sensor itself, and by the start-up and active time needed by ancillary and uplink circuitry, and hence reducing the duty cycle is the obvious means to reach some average power target. Problems arise when the duty cycle is made very low in terms of guaranteeing that a data burst sent from a node is received reliably by the controller. If the timing is not accurate, the controller itself may be in a sleep mode, or there may be a collision between data bursts from two or more remote nodes. Conventional means to control synchronisation employ high accuracy real-time clock circuits, or wake-up receivers that monitor a similar frequency to the uplink [11, 12]. In both cases, some significant power drain is associated with the circuits that are always on, making further demands on the energy harvesting and limiting the available energy for the data acquisition and uplink systems.

In the proposed system, we use the MF power transfer system to carry a low-speed data channel using slow quaternary phase-shift keying (QPSK), conveying basic system management and timing information. In this way, any receiver nodes within the transmit loop can maintain precise synchronisation and avoid data collisions while incurring only a small power overhead needed for a low-rate demodulator function. Figure 3 shows the basic arrangement of the proposed system, and highlights the work covered in this paper.

**Fig. 2** Calculated magnetic field pattern for a 10 mx10 m square transmit antenna loop





**Fig. 3** Block diagram of the wireless energy harvesting sensor concept

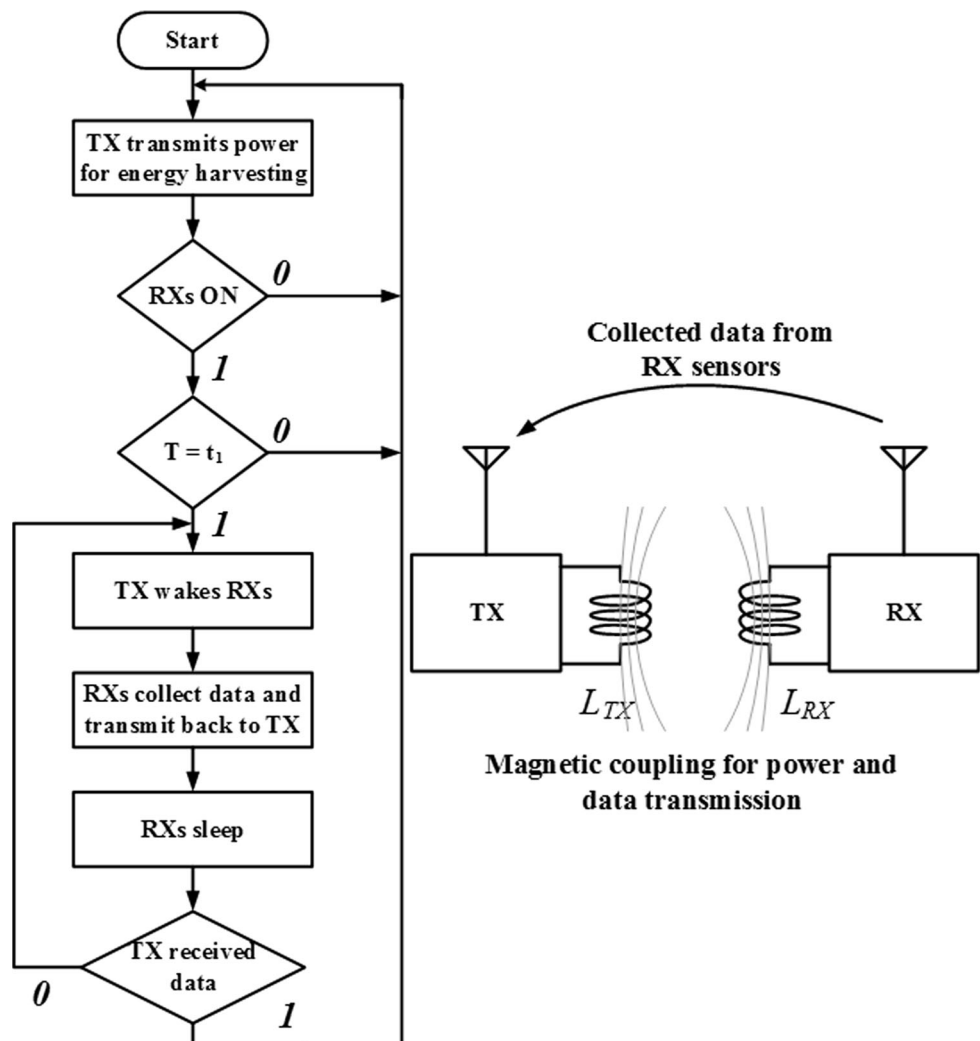
Figure 4 illustrates the flow chart of a possible synchronisation protocol for the system. Initially, the sensors harvest the magnetic energy from the primary source. When the receiver is ready to operate, an acknowledge command is transmitted to the source and the initialisation of the system is complete. In normal operating mode, the sensors are only active when they receive the *wake-up* command from the transmitter. The receiver can thus

consume less power as it operates with a very low duty cycle without timing problems.

### 3 Circuit description

Figure 3 shows a block diagram of the harvesting receiver IC. The incoming AC signal is first converted to a DC voltage by the rectifier, with an output at around 0.9 V. After some basic regulation, this low intermediate supply voltage is used to provide power for the clocking and demodulation functions in the IC. The power management unit also takes this low voltage output and boosts it up to approximately 3 V DC using a conventional latched charge pump (CP) circuit [20] to permit charging of an external storage capacitor or battery. The QPSK demodulator extracts a clock signal and data from the input to provide synchronisation and commands to the main sensor node functions.

**Fig. 4** Example of possible synchronisation protocol for sensor network



### 3.1 Low start-up voltage rectifier

As the IC design is intended to use a standard CMOS technology with no special device options, the choice of topology for the antenna coil rectifier is quite restricted, and becomes very dependent on the  $V_{th}$  of the MOS transistors. This is typically in the range of 0.3–0.8 V for common mixed signal CMOS processes. Figure 5 illustrates the problem: if  $V_{th}$  is large, the applied input voltage must be even larger. If the  $V_{th}$  is low, the gradual turn-on characteristics of the MOS device (weak and moderate inversion conduction) lead to non-negligible reverse current. Thus when input voltages from the antenna coil are reasonably large, a conventional voltage doubler implemented using MOS diodes can be used as for the AC to DC voltage conversion circuit. However, the circuit suffers from a dead zone issue as the output voltage is typically very low when the input voltage is not much greater than that of the MOS transistors used [21, 22].

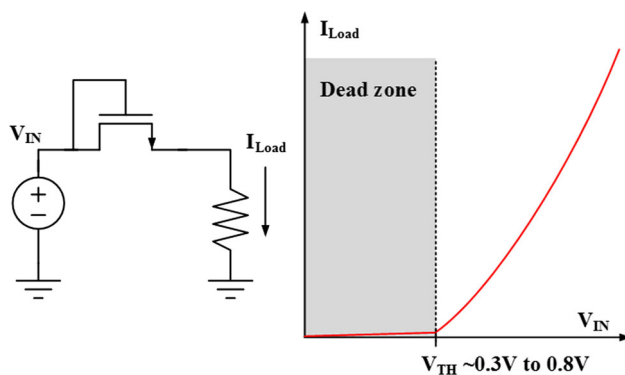
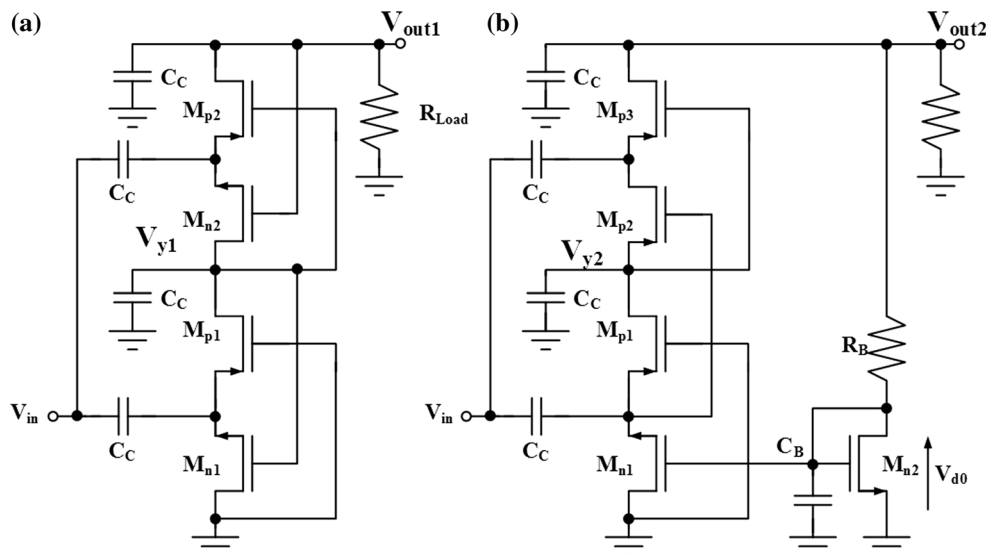


Fig. 5 MOS rectifier forward voltage

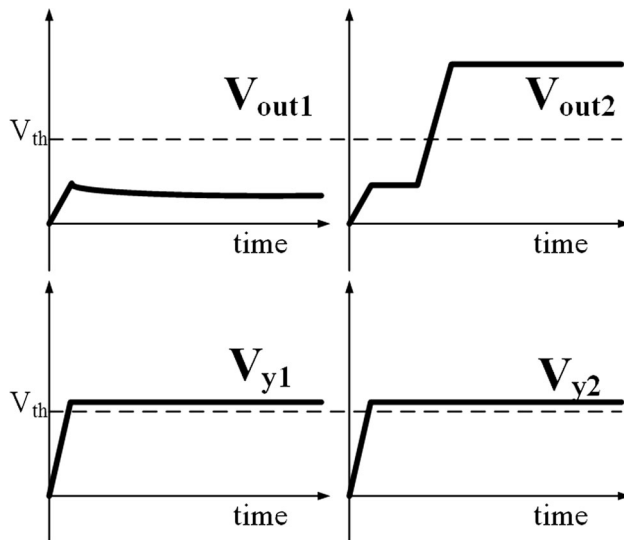
Several  $V_{th}$  cancellation techniques have been proposed to mitigate the dead zone issue in CMOS rectifiers [5–9, 22, 23], such as biasing the transistor gates from the output node [Fig. 6(a)] [8, 22] or from a diode connected transistor [7]. These circuits can rectify a relatively low input signal, but the dead-zone limitation still occurs when the input voltage is below  $V_{th}$ . Alternatively, a more expensive CMOS process with near-zero  $V_{th}$  transistors may be used to rectify a very low input signal [5, 9]. A rectifier that can operate with subthreshold input voltage is proposed by [23, 24]. In [23] a voltage bias for  $V_{th}$  cancellation is generated by using a secondary voltage source generated from a piezoelectric sensor. In [24] a photovoltaic cell is used to distribute the cancellation biasing voltage, however the system requires an additional light source. While effective in some contexts, due to the practical restrictions arising from such ancillary sources, these solutions are not preferred for the application under study.

An alternative two-stage rectifier configuration was developed to address the issue of operating with an input voltage below  $V_{th}$  as shown in Fig. 6(b). A diode connected NMOS  $M_{n2}$  provides a bias voltage to reduce the effective  $V_{th}$  of the NMOS transistor  $M_{n1}$ , while the  $V_{th}$  of the PMOS transistors are cancelled by the respective node voltages of the adjacent stages. Initially, the weak input signal is partially rectified by the PMOS transistors in subthreshold mode to create a DC output voltage. Whilst this output is initially very low, it can still provide the very small current needed to begin raising the bias voltage  $V_{d0}$  which gradually builds up and begins to cancel the  $V_{th}$  of the NMOS transistor  $M_{n1}$ . Note that the number of stages of the circuit can be increased by duplicating the second stage of the circuit shown in Fig. 6(b). Figure 7 illustrates the comparison between internal node voltages of the conventional self-threshold voltage cancellation (SVC)

Fig. 6 **a** Left conventional self-threshold voltage cancellation MOS rectifier. **b** Right proposed rectifier for improved subthreshold operation



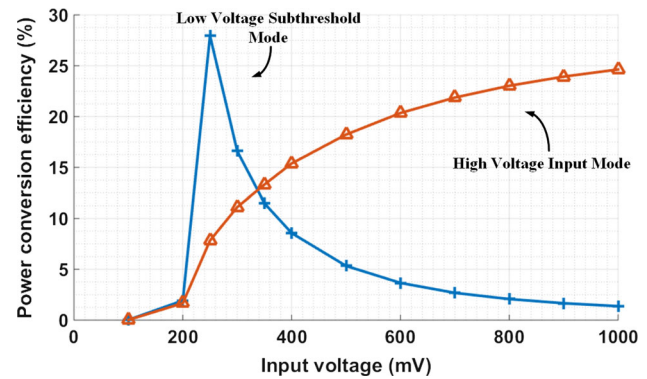




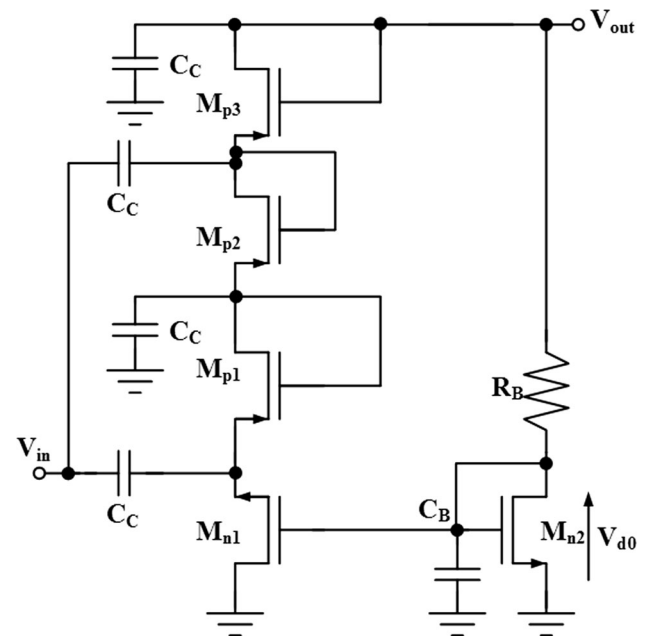
**Fig. 7** Comparison between internal node voltages of the conventional self-threshold voltage cancellation rectifier (*left*) and the proposed rectifier (*right*) in subthreshold mode ( $V_{in} < V_{th}$ )

MOS rectifier and the proposed rectifier operating in subthreshold mode, where the incoming voltage amplitude is below the MOS threshold voltage. As the output of the first stage  $V_{y1}$  of the SVC rectifier is not loaded, the leakage current weakly charges the coupling capacitor  $C_c$ . However the output node  $V_{out1}$  is limited by the output load. Consequently the voltage  $V_{y1}$  becomes greater than the output node  $V_{out1}$  which causes the transistor  $M_{n2}$  to conduct in the opposite direction. Thus the value of  $V_{out1}$  decreases. By contrast, the PMOS transistors in the proposed rectifier are biased by the unloaded voltage node, hence the transistors are not affected by the output loading resistance.

A limitation of this new circuit is that the efficiency decreases drastically when the input voltage is relatively large [7, 8, 22]. Consider the PMOS transistor  $M_{p1}$  in Fig. 6(b) when the input signal is in its negative phase; the channel is still conducting since the gate of  $M_{p1}$  is connected to ground. Thus, a reverse leakage current can flow, and grows as the input increases. The proposed four-stage rectifier configuration and voltage doubler configuration was simulated to show the power conversion efficiency (PCE) as illustrated in Fig. 8. The simulations indicate that the PCE of the proposed circuit is poor when the input voltage is above 400 mV while the PCE of a classical voltage doubler configuration is larger when the input is increased significantly. Hence to achieve optimum efficiency over a wide input range, switches are added to the proposed circuit to enable a reconfiguration of the rectifier as the input voltage rises. Figure 9 shows the topology of the rectifier when reconfigured in the high input voltage mode. MOS switches are used to change the gate



**Fig. 8** Simulated power conversion efficiency

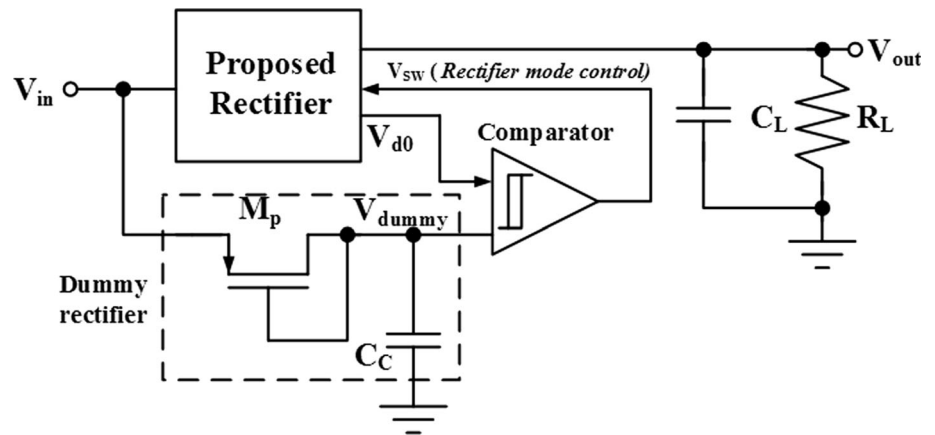


**Fig. 9** Reconfigured form of proposed rectifier for reduced reverse leakage current

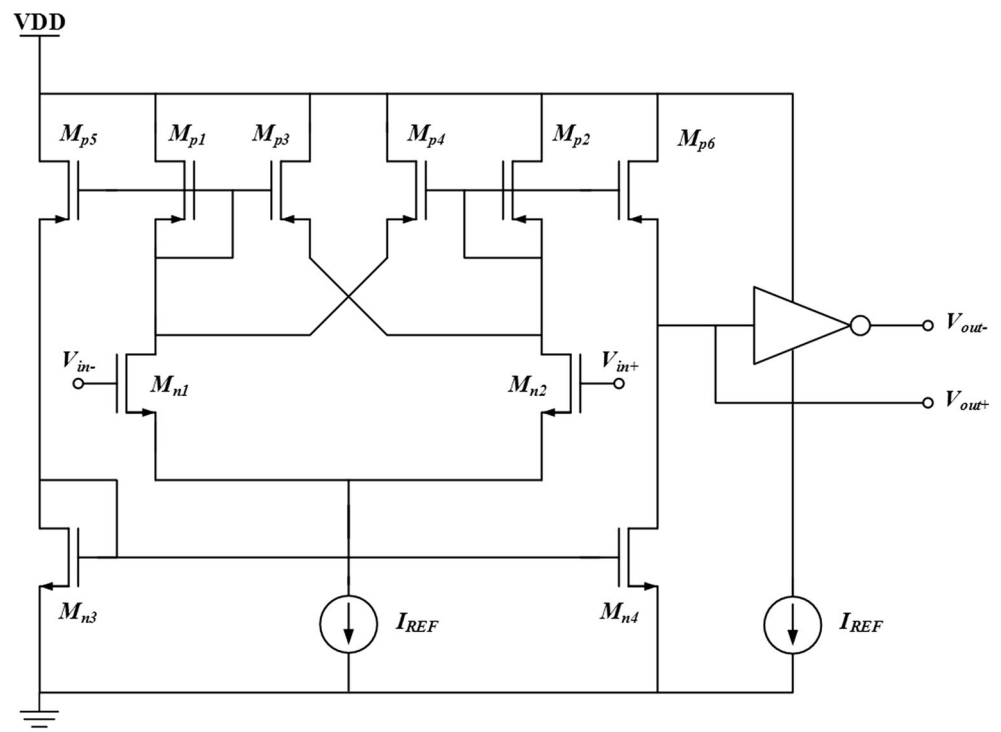
connections, and these switches are arranged so that with no bias (i.e., in a cold start condition) the rectifier is in the low input mode. Small parallel capacitors are needed across these switches since there is no voltage available to activate the MOS switches from a cold start condition.

To detect the condition when the rectifier should change mode to maintain efficiency, an input level detector/decision circuit is used. A bias voltage  $V_{d0}$  is taken from the rectifier (shown in Fig. 8) which is approximately equal to the PMOS  $V_{th}$  if the bias current is relatively small. This is compared with the output voltage from a dummy rectifier, as shown in Fig. 10. The dummy circuit is implemented from a single stage PMOS rectifier where the power consumption is negligible compared with the main rectifier, and gives an indication of the output expected from a simple conventional rectifier. The comparator is a simple

**Fig. 10** Rectifier mode switch-over detection circuit



**Fig. 11** Rectifier mode detection comparator. Bias currents are typically 20 nA



asynchronous design with some internal positive feedback to achieve reasonable gain with a very low bias current (Fig. 11). Special care is taken with the comparator's logic level translation circuit to avoid current flow due to mid-level conduction through simple inverters, bringing the risk of supply collapse while the rectifier output is still low.

### 3.2 Charge pump

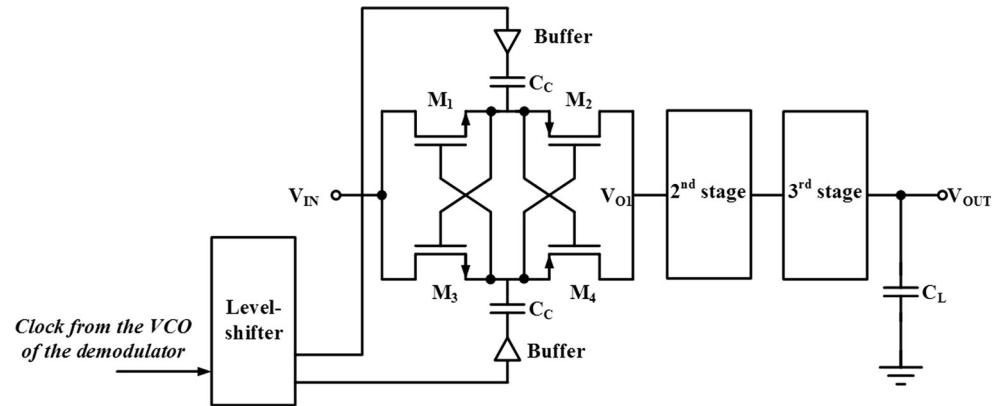
The output of the rectifier is at too low a voltage for optimum energy storage and subsequent use by sensor and other circuit functions. Hence when the rectifier output is detected as sufficiently high, a CP circuit (shown in Fig. 12) with 3 cascaded stages is enabled to deliver an

output with a nominal level of 3 V, suitable for charging lithium ion or supercapacitor storage. The design is a conventional latched CP type [20], where the clock is derived from the QPSK demodulator circuit.

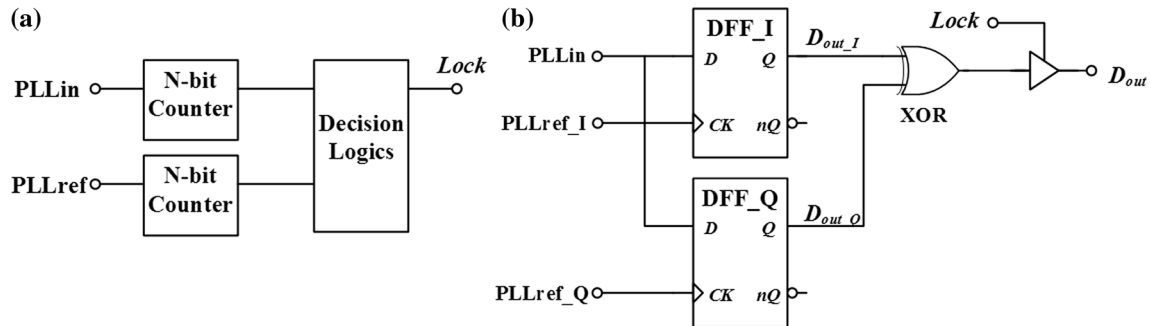
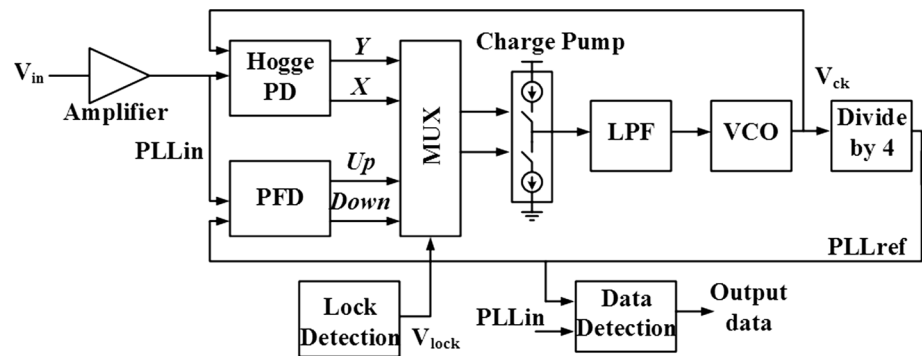
### 3.3 PSK demodulator

Since the pick-up coil of the inductively coupled harvesting system often has a high Q-factor [10, 14], a form of PSK modulation is the most efficient method as the modulated signal has, simplistically speaking, a constant amplitude and frequency.  $\pi/2$ -QPSK is the simplest suitable phase modulation since complete instantaneous phase reversals are prohibited, which would lead to temporary cancellation

**Fig. 12** Latched charge pump architecture



**Fig. 13** PLL based PSK demodulator



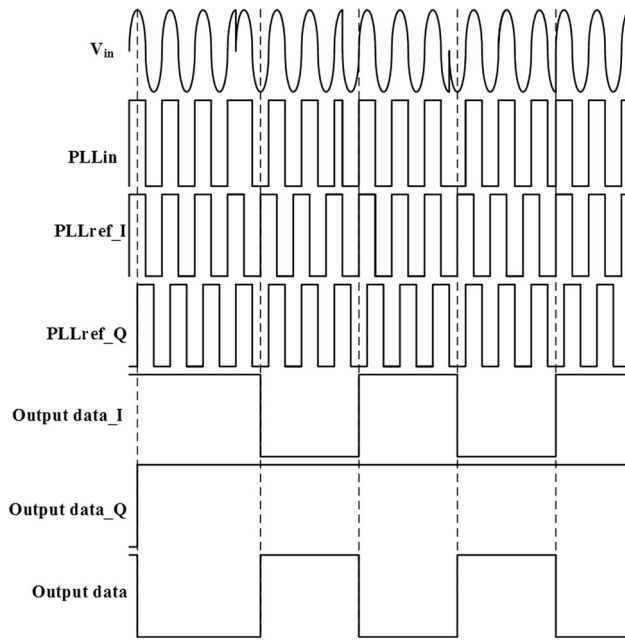
**Fig. 14** **a** Left lock detection circuit. **b** Right data detection circuit

of the drive to the receiver at each data transition. Further, the data rate is restricted to a low level consistent with the antenna coil Q-factor, thus ensuring that there are sufficiently long periods with constant phase to enable the antenna voltage to reach high enough levels for the rectifier.

Figure 13 shows a block diagram of the PSK demodulator. The system is based around a phase-locked loop (PLL) having two selectable phase detectors, a conventional phase-frequency detector (PFD) and a Hogge type phase detector [26]. To be able to retain lock while the phase is changing with the data content, the voltage-controlled oscillator (VCO) runs at four times the input signal

frequency so that there are edges available for the phase comparison process that are always in phase with the input for all states of the QPSK input signal. For this to operate, a phase detector is needed that can respond to inputs where there are only intermittent phase transitions, and hence the Hogge detector is used when the data detector is running. However, due to the periodic phase error output characteristic of this type of detector, there are severe restrictions on capture range that are not realistic for the tolerances of a low power ring type VCO. Hence when the lock detection (Fig. 14(a)) detects that the PLL is out of lock, the Hogge phase detector is disabled and the normal PFD is selected by means of a multiplexer. With only a slow data rate,



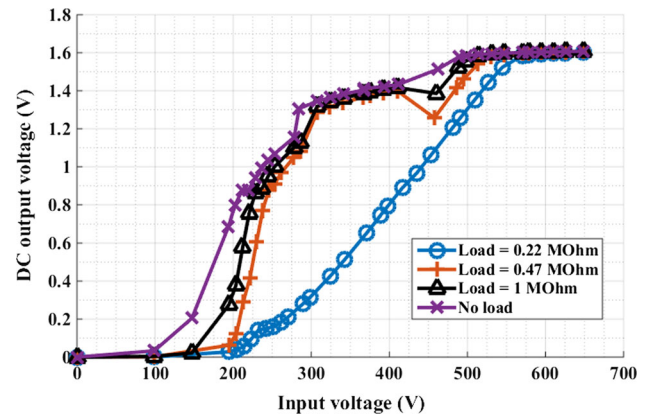
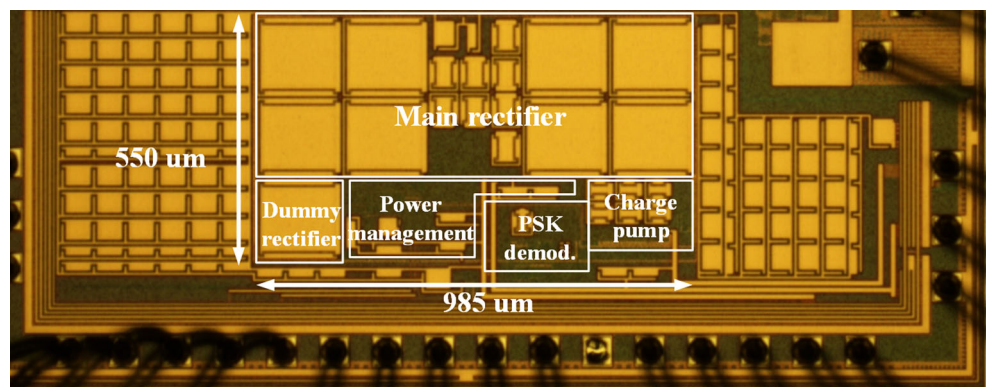


**Fig. 15** Ideal timing of the PSK demodulator

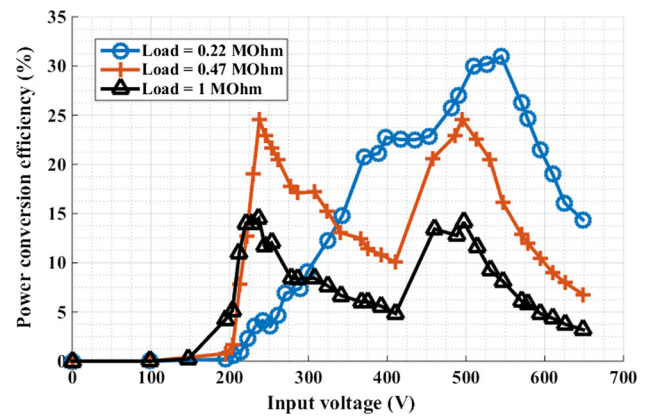
there is sufficient time to achieve lock with a constant input phase and then switch back to the Hogge detector. The input signal is compared with the locked VCO signal to recover the incoming data.

Figure 15 illustrates the ideal timing diagram of the QPSK demodulator when the Hogge PD takes over the control loop. The reference signal  $PLLref$  is not sensitive to the phase changes of the  $PLLin$  signal, and thus the data detection can distinguish the differences between the input and the reference. Note that the data detection circuit [Fig. 14(b)] requires I and Q reference signals which are produced by the divide by 4 circuit to detect the  $\pm 90$  degree phase shift of the  $PLLin$ . The output of the data detection is the result of the XOR operation between the output  $data\_I$  from the d-type flip-flop DFF\_I and  $data\_Q$  from DFF\_Q. Simulation of the circuits across process, voltage and temperature (PVT) fabrication corners confirm that the demodulated data output is not significantly affected, since

**Fig. 16** Chip micrograph



**Fig. 17** Measured DC output voltage

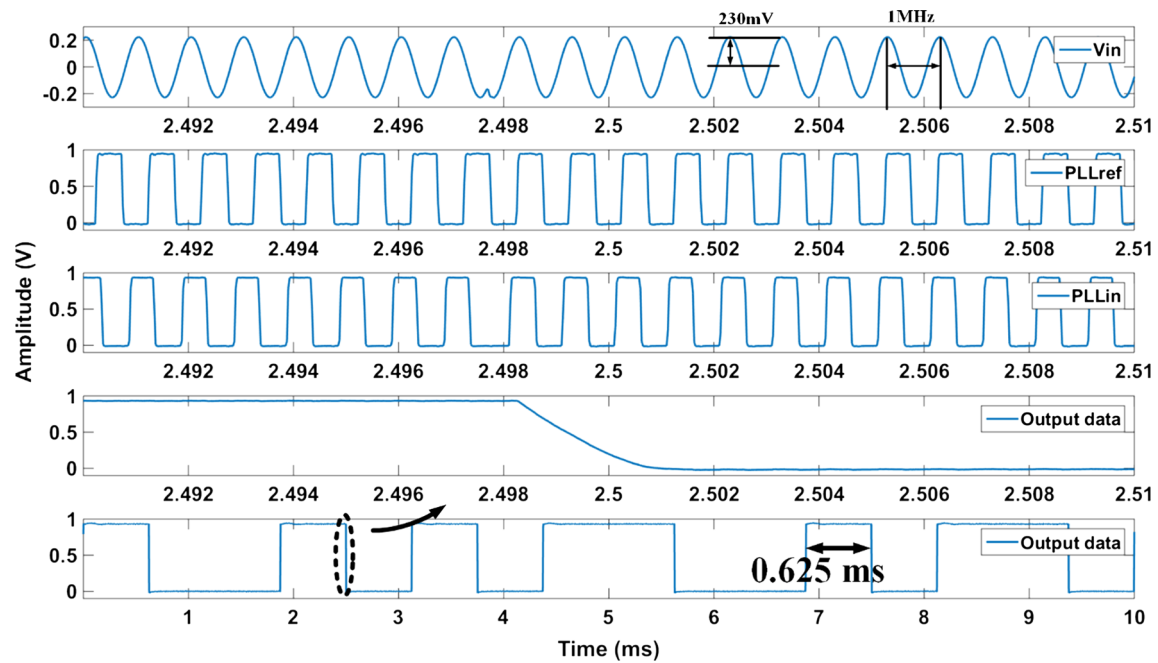


**Fig. 18** Measured power conversion efficiency

the data rate of the target application is much slower compared with the delays caused by the variations.

## 4 Measurement results

The wireless energy harvesting receiver was fabricated in a standard  $0.18 \mu\text{m}$  CMOS process. The nominal  $V_{th}$  values of the NMOS and PMOS devices are  $0.355 \text{ V}$  and



**Fig. 19** Measured waveforms of the PSK demodulator

**Table 1** Rectifier performance comparison

References	Process	Threshold voltage	Frequency	Additional requirements	Minimum input voltage	PCE
[5]	0.25 $\mu\text{m}$ SOS-CMOS	80 mV, −50 mV	100 MHz	Intrinsic devices	130 mV, $V_o > 15$ mV, $R_L = 1$ M $\Omega$	44%
[10]	0.18 $\mu\text{m}$ CMOS	<100 mV <sup>a</sup>	2.4 GHz	Intrinsic devices	$P_{in} = -20$ dBm, $V_o > 1$ V $R_L = 1$ M $\Omega$	38.4%
[21]	0.18 $\mu\text{m}$ CMOS	0.475 V	900 MHz	None	$P_{in} = -20$ dBm, $V_o = 500$ mV, $R_L = \infty$	–
[22]	0.35 $\mu\text{m}$ CMOS	0.56 V, −0.83 V	953 MHz	None	693 mV, $V_o = 600$ mV, $R_L = 10$ k $\Omega$	29%
[23]	90 nm CMOS	0.5 V <sup>a</sup>	13.56 MHz	Secondary source	100 mV, $V_o = 200$ mV, $R_L = 680$ k $\Omega$	24%
[25]	0.18 $\mu\text{m}$ CMOS	–	920 MHz	PV cell	$P_{in} = -20$ dBm, $V_o = 300$ mV, $R_L = 47$ k $\Omega$	20%
[This work]	0.18 $\mu\text{m}$ CMOS	0.355 V, −0.405 V	1 MHz	None	220 mV, $V_o = 400$ mV, $R_L = 470$ k $\Omega$	24%

<sup>a</sup> Estimated

**Table 2** PSK demodulator performance comparison

References	Process	Frequency (MHz)	Supply voltage (V)	Power ( $\mu$ W)	Max. data rate	Modulator type
[14]	0.18 $\mu$ m CMOS	10	1.8	610	1.12 Mbps	BPSK
[15]	0.18 $\mu$ m CMOS	4	1.2	324	80 kbps	BPSK
[This work]	0.18 $\mu$ m CMOS	1	0.63	1.27	1.6 kbps	QPSK

−0.405 V respectively. The chip micrograph is shown in Fig. 16. The core area is 0.54 mm<sup>2</sup>.

Laboratory measurement results of the four-stage low start-up dual mode voltage rectifier are shown in Figs. 17 and 18. Measurements have been made at a frequency of 1 MHz, as the receiver is designed to operate in the medium frequency band between 250 kHz and 2 MHz. Figure 19 shows that the rectifier output reaches 900 mV when the antenna port input voltage is 230 mV<sub>pk</sub>, which is significantly below  $V_{th}$  of the MOS transistors. It can be seen that the dead-zone of the proposed rectifier is approximately at 200 mV with a simple resistive load of 470 k $\Omega$ .

The measured PCE of the rectifier (Fig. 18) decreases when the input voltage is between 300 and 400 mV, and then rises again when the input voltage is between 400 and 500 mV, as the rectifier configuration is switched for efficiency improvement. The PCE decreases again when the input voltage is larger than 500 mV because the on-chip voltage clamp circuit limits the output voltage to 1.6 V to avoid breakdown of the thin-oxide MOS transistors. The CP in the power management unit delivers a maximum power of 10.3  $\mu$ W at 3 V to an external battery or capacitor. In the low voltage start-up mode when input voltage is just 300 mV, the CP can still provide a 0.94  $\mu$ W power to the external energy storage.

A 1 MHz carrier signal was modulated in QPSK from using the signal from a pattern generator to test the prototype data demodulator. On-chip test buffers powered from a separate 0.9 V supply were included to permit measurements with reliable power consumption figures; however the QPSK demodulator itself is self-powered by the proposed energy harvesting unit when the input amplitude reaches approximately 230 mV. Figure 19 shows the measured waveforms of the proposed QPSK demodulator. From top to bottom, the traces show the carrier ( $V_{in}$ ), reference signal ( $PLL_{ref}$ ), squared input voltage ( $PLL_{in}$ ) and output data zoomed at the phase-shifted transition. The bottom trace of the figure shows the recovered 1.6 kbps data. The overall power consumption of the demodulator is 1.27  $\mu$ W. Table I and II summarise the performance comparisons of the rectifier and the demodulator respectively. In Table 1, it can be seen that the rectifiers from [21] and [22] require the minimum input

voltage to be greater than  $V_{th}$  in order to generate a moderate output voltage. For [5, 10, 23, 25] the rectifier can operate with minimum voltage below the  $V_{th}$  but additional requirements, such as zero- $V_{th}$  NMOS, are needed. In Table 2, it can be seen that the demodulator in this work can demodulate both BPSK and QPSK modulated signal with the power consumption below 2  $\mu$ W.

## 5 Conclusion

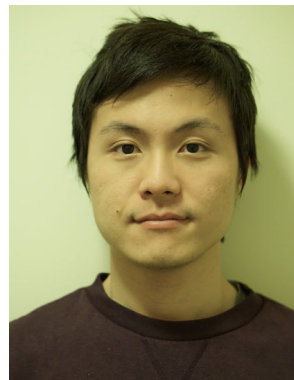
A low voltage start-up CMOS rectifier circuit and a micropower QPSK demodulator have been developed for loosely coupled magnetic energy harvesting applications. The proposed rectifier reduces the dead zone issue of previous rectifiers without requiring features such as secondary power sources or low-threshold MOS devices. An output DC voltage of 900 mV and a PCE of 24% is achieved across a 470 k $\Omega$  load with an input amplitude of 250 mV. Further, the power management unit can provide a maximum power of 10.3  $\mu$ W at 3 V to an external battery or capacitor. The QPSK demodulator achieves 1.6 kbps data rate with 1.27  $\mu$ W power consumption. The measurement results show that the receiver can be self-powered with a minimum input amplitude of 230 mV at 1 MHz carrier frequency, demonstrating the viability of the proposed system.

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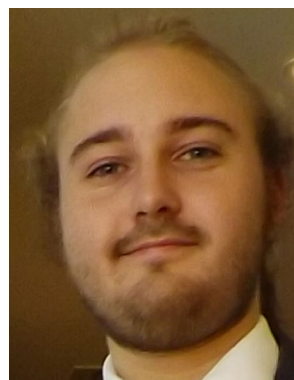
## References

1. Liu, X., & Sánchez-Sinencio, E. (2015). An 86% efficiency 12  $\mu$ W self-sustaining PV energy harvesting system with hysteresis regulation and time-domain MPPT for IOT smart nodes. *IEEE Journal of Solid-State Circuits*, 50(6), 1424–1437.
2. Lu, Y., Yao, S., Shao B., & Brokaw, P. (2016). A 200nA single-inductor dual-input-triple-output (DITO) converter with two-stage charging and process-limit cold-start voltage for photovoltaic and thermoelectric energy harvesting. In *Proceeding of*

- the *IEEE international solid-state circuits conference* (pp. 368–369).
3. Sanchez, D. A., Leicht, J., Hagedorn, F., Jodka, E., Fazel, E., & Manoli, Y. (2016). A parallel-SSHI rectifier for piezoelectric energy harvesting of periodic and shock excitations. *IEEE Journal of Solid-State Circuits*, 51(12), 2867–2879.
  4. Reinisch, H., Gruber, S., Unterassinger, H., Wiessflecker, M., Hoger, G., Pribyl, W., et al. (2011). An electro-magnetic energy harvesting system with 190 nW idle mode power consumption for a BAW based wireless sensor node. *IEEE Journal of Solid-State Circuits*, 46(7), 1728–1741.
  5. Theilmann, P. T., Presti, C. D., Kelly, D. J., & Asbeck, P. M. (2012). A  $\mu$ W complementary bridge rectifier with near zero turn-on voltage in SOS CMOS for wireless power supplies. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 59(9), 2111–2124.
  6. Umeda, T., Yoshida, H., Sekine, S., Fujita, Y., Suzuki, T., & Otaka, S. (2006). A 950-MHz rectifier circuit for sensor network tags with 10-m distance. *IEEE Journal of Solid-State Circuits*, 41(1), 35–41.
  7. Nakamoto, H., Yamazaki, D., Yamamoto, T., Kurata, H., Yamada, S., Mukaida, K., et al. (2007). A passive UHF RF identification CMOS tag IC using Ferroelectric RAM in 0.35- $\mu$ m technology. *IEEE Journal of Solid-State Circuits*, 42(1), 101–110.
  8. Papotto, G., Carrara, F., & Palmisano, G. (2011). A 90-nm CMOS threshold-compensated RF energy harvester. *IEEE Journal of Solid-State Circuits*, 46(9), 1985–1997.
  9. Zeng, Z., Li, X., Bermak, A., Tsui, C. Y., & Ki, W. H. (2016). A WLAN 2.4-GHz RF energy harvesting system with reconfigurable rectifier for wireless sensor network. In *Proceeding IEEE international symposium on circuits and systems* (pp. 2362–2365).
  10. Allen, B., Ajmal, T., Dyo, V., & Jazani, D. (2012). Harvesting energy from ambient radio signals: a load of hot air? In *Loughborough antennas and propagation conference* (pp. 1–4).
  11. Lee, Y., Giridhar, B., Foo, Z., Sylvester, D., & Blaauw, D. (2011). A 660pW multi-stage temperature-compensated timer for ultra-low-power wireless sensor node synchronization. In *Proceeding of IEEE international solid-state circuits conference* (pp. 46–48).
  12. Jeong, S., Lee, I., Blaauw, D., & Sylvester, D. (2015). A 5.8 nW CMOS wake-up timer for ultra-low-power wireless applications. *IEEE Journal of Solid-State Circuits*, 50(8), 1754–1763.
  13. Gamm, G. U., Sippel, M., Kostic, M., & Reindl, L. M. (2010). Low power wake-up receiver for wireless sensor nodes. In: *6th International conference on intelligent sensors, sensor networks and information processing, 2010* (pp. 121–126).
  14. Hu, Y., & Sawan, M. (2005). A fully integrated low-power BPSK demodulator for implantable medical devices. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(12), 2552–2562.
  15. Mohamed, S. A. S., & Manoli, Y. (2014). A novel fully integrated low-power CMOS BPSK demodulator for medical implantable receivers. In: *Proceeding of IEEE International Symposium on Circuits and Systems* (pp. 1098–1101).
  16. Tabesh, M., Dolatsha, N., Arbabian, A., & Niknejad, A. M. (2015). A power-harvesting pad-less millimeter-sized radio. *IEEE Journal of Solid-State Circuits*, 50(4), 962–977.
  17. Piñuela, M., Mitcheson, P. D., & Lucyszyn, S. (2013). Ambient RF energy harvesting in urban and semi-urban environments. *IEEE Transactions on Microwave Theory and Techniques*, 61(7), 2715–2726.
  18. Rao, N. N. (2004). *Elements of engineering electromagnetics*. Upper Saddle River, NJ: Pearson Prentice Hall.
  19. Fotopoulou, K., & Flynn, B. W. (2011). Wireless power transfer in loosely coupled links: coil misalignment model. *IEEE Transactions on Magnetics*, 47(2), 416–430.
  20. Palumbo, G., & Pappalardo, D. (2010). Charge pump circuits: An overview on design strategies and topologies. *IEEE Circuits and Systems Magazine*, 10(1), 31–45.
  21. Haeri, A. A. R., Karkani, M. G., Sharifkhani, M., Kamarei, M., & Fotowat-Ahmady, A. (2017). Analysis and design of power harvesting circuits for ultra-low power applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(2), 471–477.
  22. Kotani, K., & Ito, T. (2007). High efficiency CMOS rectifier circuit with self-V<sub>th</sub>-cancellation and power regulation functions for UHF RFIDs. In *Proceeding IEEE Asian solid-state circuits conference* (pp. 119–122).
  23. Nguyen, T. T., Feng, T., Häfliger, P., & Chakrabarty, S. (2014). Hybrid CMOS rectifier based on synergistic RF-piezoelectric energy scavenging. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(12), 3330–3338.
  24. Kotani, K. (2013). Highly efficient CMOS rectifier assisted by symmetric and voltage-boost PV-cell structures for synergistic ambient energy harvesting. In *Proceedings of the IEEE custom integrated circuits conference* (pp. 1–4).
  25. Kotani, K., Bando, T., & Sasaki, Y. (2012). Photovoltaic-assisted CMOS rectifier circuit for synergistic energy harvesting from ambient radio wave. In *IEEE Asian solid state circuits conference* (pp. 329–332).
  26. Razavi, B. (2002). Challenges in the design high-speed clock and data recovery circuits. *IEEE Communications Magazine*, 40(8), 94–101.



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