UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND THE ENVIRONMENT

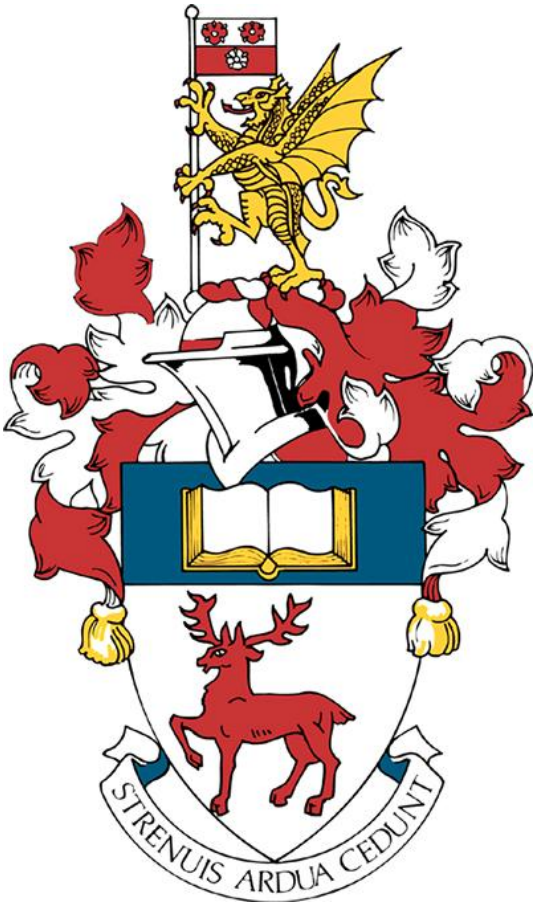
Engineering of Science

Mechatronics Research Group

Hybrid Modelling and Control for Switched-Mode Power Converters

by

Xingda Yan



Thesis for the degree of Doctor of Philosophy

Supervisor: Dr Zhan Shu

Prof Suleiman M Sharkh

November 8, 2017

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ABSTRACT

FACULTY OF ENGINEERING AND THE ENVIRONMENT
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Doctor of Philosophy

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Switched-mode power converters are some of the most widely used power electronics circuits due to their advantages of high conversion efficiency, flexible output voltage, light weight. A variety of control methods have been developed for the switched-mode power converters. However, in many practical situation, additional constraints need to be considered, e.g., safety measurement, current limiting or soft-starting, gross changes of operation point with guaranteed system stability, which has not been fully addressed in the available research works. On the other hand, the majority of the control design for power converters are based on the state-space averaged approach which involves considerable approximation in analysis and synthesis. Hence, advanced control techniques are in demand, which should be more constraints friendly and based on more precise models.

In this thesis, much attention has been spent on designing controllers for both DC-DC converters and DC-AC inverters based on hybrid modelling and Lyapunov stability theory. Due to the existence of the power switches, switched-mode power converters are hybrid systems with both continuous dynamics and discrete transition events. Instead of linearizing the converter model around a specific operating point, hybrid modelling captures both dynamics, which results in more accurate models.

Firstly, a novel sampled-data control approach is proposed for DC-DC converters. DC-DC converters are modeled as sampled-data switched affine systems according to the status of the power switch. In order to avoid the delay of the switching signal, an on-line prediction method is adopted to estimate the system state at the next switching instant. Based on the switched affine model and the predicted system state, a novel switching control algorithm is synthesized by using the switched Lyapunov theory. The proposed approach is able to not only drive the output to a prescribed set point from any initial condition, but also track a varying reference signal, and the switching frequency can be adjusted online with guaranteed stability. In addition, with this approach, Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) operations can be treated in a unified way. Experimental verification has been carried out to test the effectiveness and merits of the proposed method.

Furthermore, to compensate the information loss due to limited access to the state, a multiple sampling scheme is employed to derive a discrete-time switched affine model with an augmented measurement output for DC-DC converters. Based on the model, an output-feedback switching control law, which drives the system state to a set of attainable switched equilibria, is synthesized by using a quadratic state-space partition. The multiple sampling scheme not only facilitates the controller synthesis, but also improves the energy efficiency of the converter by allowing a lower switching frequency.

In addition, hybrid modelling techniques have been extended to more complicated cases – DC-AC inverters as the increasing number of power switches and the time-variant nature of the references. A current controller based on the hybrid model of the three-phase two-level inverter has been developed, which can drive the inverter currents tracking the desired power references in realtime and keep a unity power factor at the same time. This method has been extended to three-phase NPC inverters later on. However, in order to solve the neutral point balancing issue, a capacitor voltages prediction algorithm, modified from model predictive control, has been adopted. It should also be mentioned that a novel hybrid model for a grid-connected single-phase NPC inverter also has been presented, which models not only the dynamic of the inverter but also the dynamic of the current reference. An experimental test platform including a three-phase NPC inverter and a FPGA control board has been designed to demonstrate the implementation of the proposed control scheme in practice.

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Declaration of Authorship

I, Xingda Yan , declare that the thesis entitled *Hybrid Modelling and Control for Switched-Mode Power Converters* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as:

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2. Yan, Xingda, Zhan Shu, and Suleiman M. Sharkh. "Output-feedback switching control of DC-DC cuk converters using multiple sampling." Automatic Control Conference (CACS), 2015 International. IEEE, 2015.
3. Yan, Xingda, Zhan Shu, and Suleiman M. Sharkh. "Hybrid modelling and control of single-phase grid-connected NPC inverters." Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE. IEEE, 2016.
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Chapter 1

Introduction

1.1 Motivation

Since they were first developed through the introduction of power diode by Robert N. Hall in 1952, power semiconductor components have considerably ameliorated both in performance and price. Various power semiconductor components with good specifications for switching frequency and on-resistance, e.g., MOSFETs or IGBTs (Insulated Gate Bipolar Transistors) have become common. As a consequence, power converters, whose main functions are achieved by the switching property of power semiconductor components, have developed rapidly in recent years. A power converter is an electrical or electro-mechanical device for converting electric energy either converting between different forms like DC-AC/AC-DC or regulating voltage/frequency. Rectifiers are probably the most familiar example of power converters, and DC-DC converters and DC-AC/AC-DC inverters are also common applications [5][6] [7] [8].

Power converters exist almost in every kind of electronic device from industrial to residential applications. For DC-DC converters, one of the main applications is in power supplies, which contain DC-DC converters as their key parts. As the cost of electronic components declines dramatically, the power supply becomes a large fraction of system cost. Roughly speaking the power supply cost has almost reached 50% of a typical electronic product such as personal computers or hybrid electric vehicles. On the other hand, the specification requirements of power supplies are diversified as the development of electronic engineering. For example, a personal computer requires at least three different $5V$ supplies, two $+12V$ supplies, a $-12V$ supply and a $24V$ supply excluding supplies for peripheral devices. Therefore, development of high performance, low cost DC-DC converters is urgent.

Since a great number of household and industrial utilities needs AC supply, the DC-AC inverters could be found in a variety of applications. In order to adjusting the speed of AC motors, the DC-AC inverters are the essential part of AC motor drives [9][10]. For some situation, when only DC power sources, such as batteries or fuel cells, are available, the DC-AC

inverters could be used to drive the AC equipment [11][12]. Another important application of DC-AC inverters is the uninterruptible power supplies, which is widely used to protect vulnerable electrical equipment, such as data logging device, telecommunication equipment from an unexpected power disruption [13][14].

Due to the day-by-day increasing energy demand and the environmental problems caused by fossil fuel, alternative renewable and green distributed energy resources, such as solar power, wind energy, hydropower have drawn increasing attention to reduce the reliance on fossil fuel and cut emission [15][16]. As shown in Figure 1.1, the capacity of the utility-scale solar power has an exponential growth in the U.S during the last decade. In the meantime, the average price of the solar PV falls dramatically. A DC voltage is usually supplied by the distributed energy resources, such as photovoltaic (PV), fuel cells, and wind power. Hence, DC-AC inverters are used to interface these sources to the grid supplying high quality AC current in accordance with national standard [17][18][19][20].

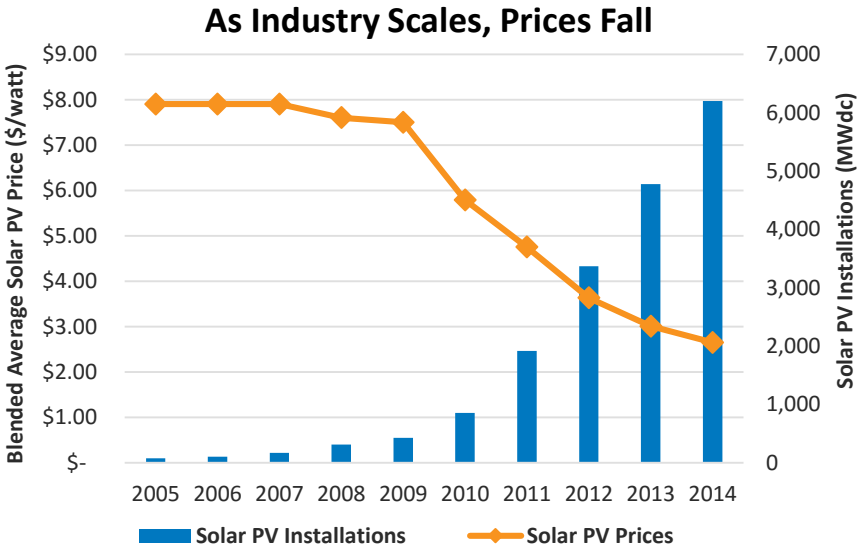

Figure 1.1: Solar PV installations and average solar PV price in US [Source:Solar Energy Industries Association]

As for the design of power converters, one of the most important parts is the control system. The main challenge in controlling a power converter arises from their hybrid nature which is caused by the use of semiconductor components as power switches. From the control point of view, the power converters are nonlinear system which contains both continues and discrete dynamics. The conventional control approach to the modelling and controller design of power converters is the state-space averaged approach and the design of linear controllers. The disadvantages of the conventional methods are obvious.

1. The model is linearized around a specific operating point.
2. The tuning procedure of the controller is complicated, and the design is further complicated when the operating point is changed.

3. Practical experience is essential for the controller tuning.

On the other hand, the development of advanced hybrid system control theory together with more powerful control platform such as DSP, FPGA gives us the possibility of tackling the control problem from a new perspective. In view of this, more systematics modelling and control methods can be developed. In my research, the main goals are as follows.

1. Power converters are modeled as switched affine models, a specific type of hybrid systems, which describe the system dynamic across the whole operating range and determines the active continues dynamic by a switching law.
2. The Lypunov stability theory and robust control are main methodologies to derive the controller synthesis conditions.
3. There is no complicated tuning involved. A unified systematics design procedure will be given, which can be easily applied on different power converters with different topologies.
4. The practical limitation of power converters, such as switching frequency, ripple reduction, neutral point balanced, can be included easily by adding constrained conditions to the synthesis conditions.
5. Most importantly, all the design is done off-line which can highly release the computation burden.
6. Experimental verification of the proposed control schemes will be carried out to demonstrate that these methods can be easily implemented in practice, which are not just methods on the papers.

Therefore, the main scope of this PhD project is to illustrate that advanced hybrid control methodologies can be applied on power converters conceivably and within reach. Two major types of power converters are considered in this thesis: DC-DC converters and DC-AC inverters.

1.2 Structure of the Thesis

This thesis generally includes three parts. First part is Chapter 1 and Chapter 2, which gives the motivation of this PhD project and reviews the modelling and control techniques for both DC-DC converters and DC-AC inverters.

The second part consists of Chapter 3, Chapter 4 and Chapter 5, which focuses on DC-DC converters. In Chapter 3, two conventional modelling and control techniques are reviewed in details, which are: linear controller design based on the state-space averaged model and model predictive control based on a hybrid model to act as benchmarks for the following chapters. In

Chapter 4, a novel sampled-data control approach is proposed, which not only guarantees the stability across all attainable operating points, but also has the ability to adjust the switching frequency. Experiments based on dSPACE control platform also have been carried out to verify the effectiveness of the proposed methods. In Chapter 5, a novel output feedback control approach is proposed . To compensate the information loss due to limited access to the state, a multiple sampling scheme is employed to derive a discrete-time switched affine model with an augmented measurement output. Based on the model, an output-feedback switching control law, which drives the system state to a set of attainable switched equilibria, is synthesized by using a quadratic state-space partition. The multiple sampling scheme not only facilitates the controller synthesis, but also improves the energy efficiency of the converter by allowing a lower switching frequency.

The third part of the thesis, which includes Chapter 6, Chapter 7, Chapter 8, and Chapter 9, deals with the hybrid modelling and control problems in DC-AC inverters. In Chapter 6, a grid-connected three-phase two-level inverter is studied. Hybrid models of the inverter are presented and a switching controller, which can stabilize the phase currents to the desired current references, is presented. In Chapter 7, a novel switching controller, which includes the current reference dynamics in the hybrid model, is proposed for a grid-connected single-phase Neutral Pointed Clamped (NPC) inverter. In Chapter 8, the control method developed in Chapter 6 is extended to a three-phase NPC inverter in conjunction with an additional capacitor voltage balancing controller. In Chapter 9, experimental work is presented to demonstrate how to implement the proposed switching control technique on a three-phase NPC inverter with RL load based on the DE-115 Field-Programmable Gate Array (FPGA) control board.

In the last Chapter 10, the proposed modelling and control schemes are compared with each others and also compared with the state-of-the-art modelling and control methods. In general, this PhD project gives a new perspective of modelling and control of switched-mode power converters. It demonstrates the advantages of the proposed methods over the traditional methods in several aspects. Firstly, the hybrid model captures both continuous and discrete dynamics which is more precise than the state-space averaged approach. Secondly, the proposed control approaches not only can guarantee the system stability within a much wider operation range, but also can be more constraints friendly. Last but not the least, the experiment verification carried out on both DC-DC converters and DC-AC inverters has proven that the proposed control scheme can be conveniently implemented on digital platforms with relatively low online computation burden.

Chapter 2

Literature Review

2.1 Control Methods for DC-DC Converters

There are numerous types of power converters. Among these, DC-DC converters, which convert a source of direct current (DC) from one voltage level to another, are one of the simplest power electronics devices. This type of converters have found widespread applications in practice, e.g., cellular phones, laptops, communication equipments, motor drives. A great number of control techniques based on different models have been employed for the control of DC-DC converters in industry including voltage-mode and current-mode control techniques [21]. Thus it is of interest to compare the dynamic response of these control approaches as well as their strength and weakness.

2.1.1 DC-DC Converters Control in The Past

A DC-DC converter consists a switching topology and the associated control circuit. The switching topology is a periodic time-varying circuit due to the discrete input and continuous output, and the control circuit is a hybrid circuit containing both nonlinear and linear stages. In order to use the classical control theory, approximations must be made to move from the time-varying nonlinear system to a time-invariant linear one. Thus the state-space averaged approach (SSA), a way to model DC-DC converter as a linear canonical circuit, was proposed [22, 23] and became one of the essential techniques for analyzing switched mode power conversion circuits. Based on the state-space averaged approach for the modeling of DC-DC converters, various control techniques have been adopted to investigate the dynamic responses of a DC-DC converter.

Generally, control techniques of DC-DC converters can be divided into voltage mode control and current mode control by the feedback signals. Both methods were initially implemented as analog approaches. For simplicity of explanation, in the following part, the different control methods are introduced based a typical buck converter.

Voltage mode control as shown in Figure 2.1 is a single loop control approach in which the output voltage is measured and compared to a reference voltage to generate an error signal. The duty ratio is regulated by comparing the error signal to a fixed frequency sawtooth waveform [24, 25]. Voltage mode control is still used in some industry applications because of following advantages: 1) Simple topology, single feedback loop, which is easy to design and low cost; 2) Less sensitive to noise; 3) Can work over a wide range of duty cycles. However, the drawbacks of voltage mode control are also obvious: 1) Loop gain proportional to input voltage leading to more complicated compensation; 2) The additional poles added by output filter may require Type III compensation (a three poles and two zeros compensation network); 3) Slow response to input voltage changes; 4) Current limiting must be done separately.

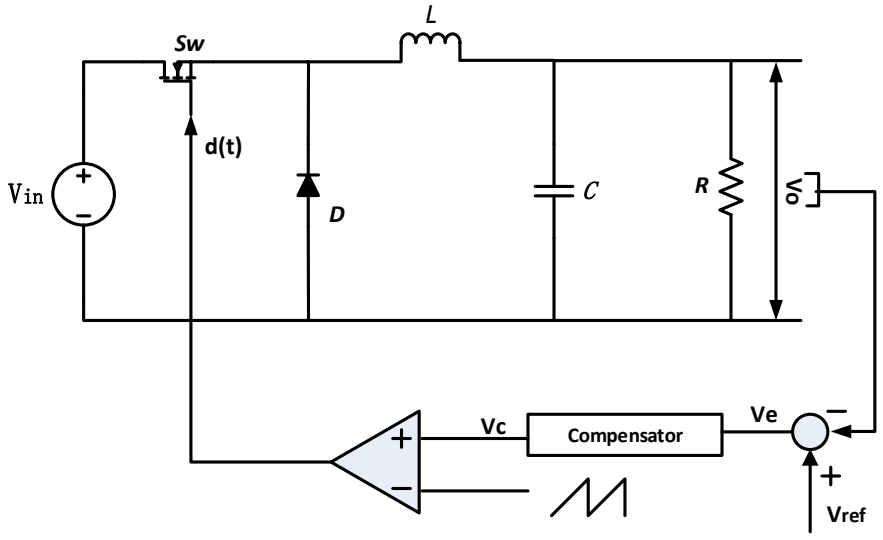

Figure 2.1: Block diagram of a basic voltage mode controller

Due to the disadvantages of voltage mode control, current mode control [24, 25, 26] is used to alleviate all the weak points above. More specifically, the inductor current is measured and employed to control the duty ratio as shown in Figure 2.2. An error signal is produced in the same way as voltage mode control by comparing output voltage to the reference voltage, and acts as a reference signal for the current control loop after a compensator. Then inductor current is compared with the reference current signal to modulate the duty ratio. In 1978, the implementation of current mode control of DC-DC buck converters was first proposed with the so-called name "peak current control" [27], which means that during each cycle switch closure is ended when the sensed inductor current hits an adaptable threshold (Figure 2.3). After this, a series of related works on the peak current control was published [28, 29, 30, 31, 32]. However, when the duty ratio exceeds 50%, instability occurs resulting in period-doubling, sub-harmonic oscillations or chaotic behavior. In order to avoid this serious issue, slope compensation [24] was introduced —— the sum of inductor current and an external ramp is compared with the reference current signal as shown in Figure 2.4.

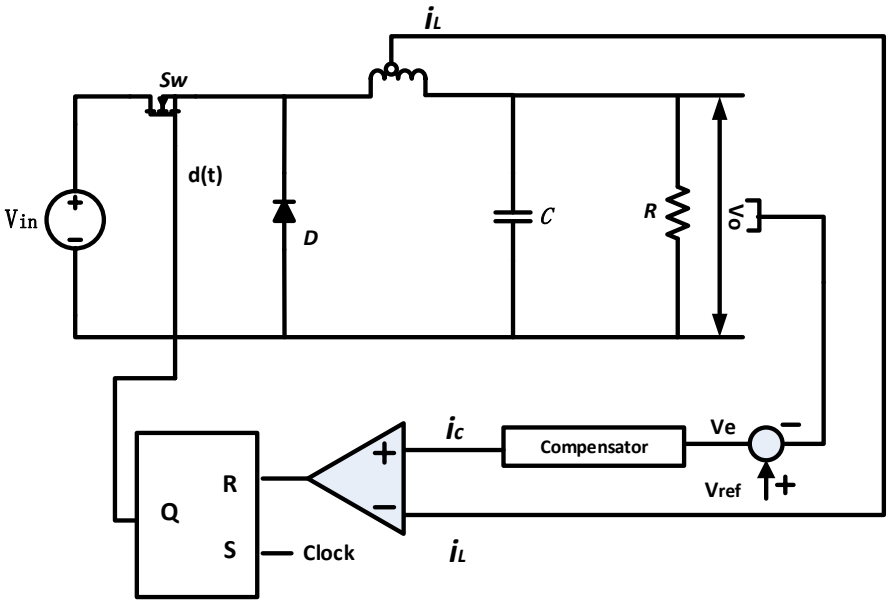

Figure 2.2: Block diagram of a basic current mode controller

Current mode control has several advantages over the classical voltage mode control: 1) The waveform of the inductor current responds promptly to the line voltage changes thus reducing the delayed response and gain variation with changes in the input voltage; 2) The output filter now offers only a single pole, hence compensation is simpler and higher gain bandwidth is obtained; 3) Cycle-by-cycle current limiting protection; 4) Ease of current sharing when converters operate in parallel. Although improvement has been made over the voltage mode control, the current mode control also comes with its unique set of challenges: 1) The two feedback loops brings more difficulty to the circuit analysis; 2) Oscillations appears when the duty cycle exceeds 50%; 3) Resonances from the power stage can insert noise into the control loop through the output current.

Initially, the implementation of both voltage mode and current mode control techniques for DC-DC converters was accomplished by analog circuits composed of passive components and amplifiers. Before the wide use of digital devices, using analog circuits was an essential approach to control power converters due to their simple structure and low cost. However, the disadvantages of analog circuit and components, such as bad flexibility, low reliability, and parameter deviation caused by the external influence (thermal, humidity, lifetime, etc), could not be neglected. In addition, linearized models of power converters are utilized in analog implementation which overlook the nonlinear properties.

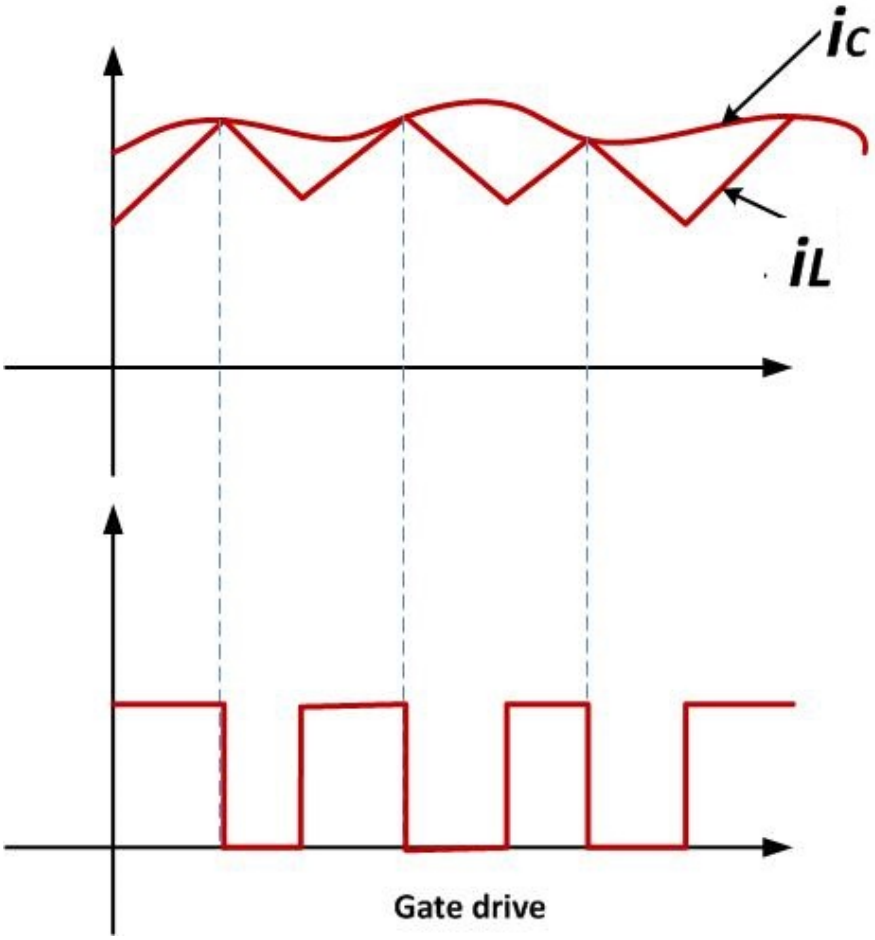

Figure 2.3: The waveforms of the signal in a current controller in peak current mode control

2.1.2 DC-DC Converters Control Today

In recent decades, the use of microprocessors for the control of power electronics systems has become a common solution for full digital implementation of controllers. Several control techniques developed for analog control circuits have been replicated in a digital way. Moreover, modern control platforms with high computational capabilities such as digital signal processors (DSP), field-programmable gate array (FPGA) allow the possibility of implementation of more advanced control algorithms [33].

Based on the idea of the peak current control method, various digital techniques for DC-DC converters have been presented in recent years including Valley Current Control [34], Average Current Control [35], Delayed Valley Current Control [36], Delayed Peak Current Control [36], Delayed Average Current Control, Prediction Current-Mode Control With Delay Compensation, Compensated Digital Current-Mode Control [37, 38, 39, 40].

Figure 2.5 depicts the general structure of a digital current-mode controller implemented

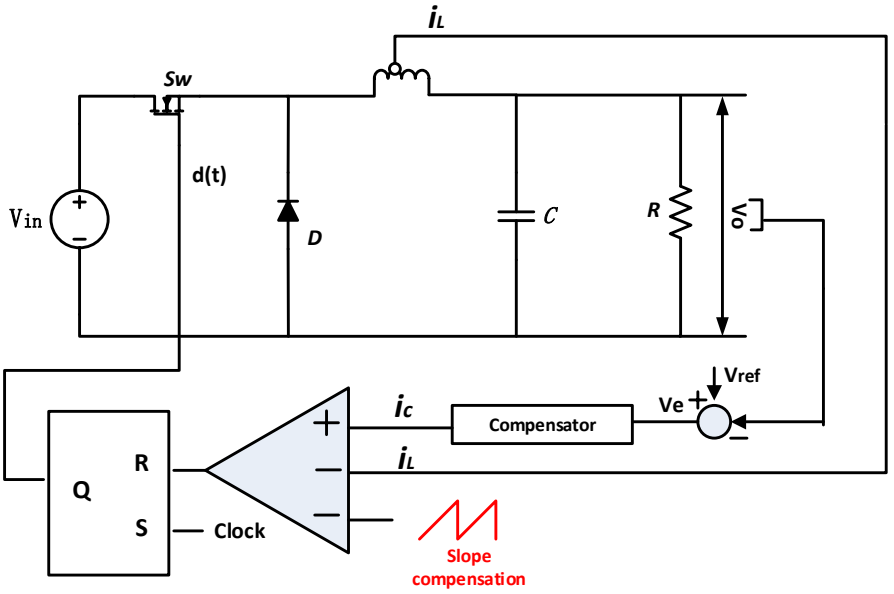

Figure 2.4: Block diagram of a peak current controller with the slope compensation

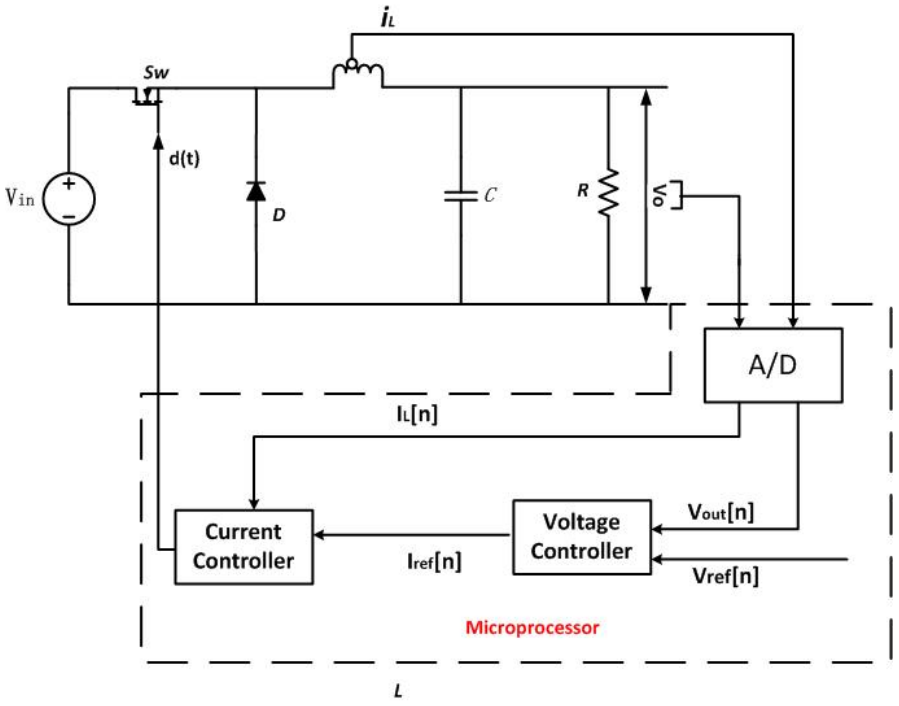

Figure 2.5: Block diagram of the general structure of a digital current-mode controller

by a microprocessor. The microprocessor attempts to find the right value of the duty cycle to satisfy the control objective using the sampled data of input and output voltages and the inductor current. All of these approaches make an attempt to let the valley, average, or peak value of the inductor current to follow the current reference signal named i_{ref}, which is obtained from the voltage controller.

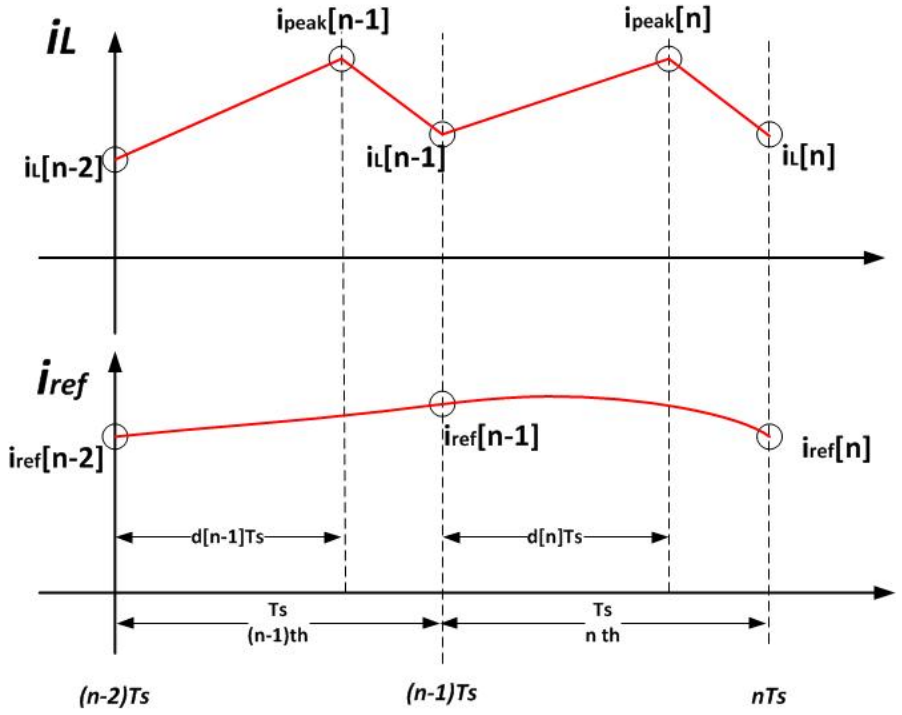

Figure 2.6: Current waveform of the inductor and reference signal in a digital current-mode controller

To compare the different digital control methods, a typical buck converter is considered. The inductor current waveform of a buck converter under continuous conduction mode is displayed in Figure 2.6. In order to make the following description about different techniques easy to access, notations are introduced first. T_s is the switching period of the DC-DC buck converter. $d[n]$ is the duty ratio during the n^{th} switching period. $i_L[n]$ is the sampled inductor current at time nT_s, which is the end of the n^{th} switching period, and $i_{ref}[n]$ is the sampled current reference at time nT_s. $V_{in}[n]$ and $V_o[n]$ are the sampled input and output voltage, respectively. The input and output voltage are treated as constants during each switching period as they both vary slowly. Thus, we can write:

$$\begin{aligned} V_o[n] &\approx V_o[n-1] \\ V_{in}[n] &\approx V_{in}[n-1] \end{aligned} \tag{2.1}$$

Valley current control is analog in nature [34]. However a digital controller can be obtained by changing the differential equations describing the dynamic of the power converter to difference equations. With this approach, the required value for the duty cycle is calculated in the ongoing period to make sure that

$$i_L[n] = i_{ref}[n-1] \tag{2.2}$$

To achieve the objective, the duty cycle of the n_{th} switching period can be calculated by (2.3) which is given in [34]:

$$d[n] = \frac{L}{V_{in}T_s}(i_{ref}[n-1] - i_L[n-1]) + \frac{V_o}{V_{in}} \tag{2.3}$$

In other words, the inductor current i_L, the reference current i_{ref} and the voltages are sampled at the beginning of each switching period. Then the duty ratio $d[n]$ is obtained by (2.3) and applied so that the final value of inductor current at the beginning of each switching cycle will be equal to the reference current at the beginning of the switching cycle. One thing that must be mentioned is that microprocessor must be fast enough to compute and apply the duty cycle.

In [36], the method called delayed valley current control is presented. In this approach, the duty ratio is calculated in the previous period to guarantee that

$$i_L[n] = i_{ref}[n-2] \tag{2.4}$$

To fulfill the above control objective, the equation used to calculate the duty cycle has been given in (2.5).

$$d[n] = \frac{L}{V_{in}T_s}(i_{ref}[n-2] - i_L[n-2]) - d[n-1] + \frac{2V_o}{V_{in}} \tag{2.5}$$

This way, the inductor current and reference are sampled at the beginning of the previous switching period ($(n-1)th$ period) and used to calculated the duty ratio applied in next switching period (nth period) to make the inductor current in the nth switching period following the current reference sampled at the beginning of the previous switching period. The advantage of this method is that the digital controller will have more time for the related computation at the cost of the introduction of an extra period of delay.

Average current control was first introduced in [35]. The control objective is that the average value of the inductor current in each switching period is equivalent to the current reference signal sampled at the start of the same cycle.

$$\frac{1}{T_s}\int_{(n-1)T_s}^{nT_s} i_L dt = i_{ref}[n-1] \tag{2.6}$$

According to [35], the duty ratio can be calculated as:

$$d[n] = \frac{L}{V_{in}T_s}(i_{ref}[n-1] - i_L[n-1] - \frac{T_s V_o}{2V_{in}} \cdot \frac{V_{in} - V_o}{L}) + \frac{V_o}{V_{in}} \tag{2.7}$$

The implementation procedure of this method is the same as the valley current control: inductor current, current reference and voltages are sampled at the beginning of each cycle and the duty ratio is calculated and applied using (2.7). It is proved in [35] that the control scheme

is stable for any value of the duty cycle without slope compensation.

A similar control method called "delay peak current control" is also proposed in [36]. Different from delay valley current control, the control scheme of this approach is to force the peak value of the inductor current during the coming period to be equivalent to the current reference sampled at the start of previous switching period.

$$i_{peak}[n] = i_{ref}[n-2] \tag{2.8}$$

Where $i_{peak}[n]$ is the peak value of the inductor current in nth switching period.

From [36], the required duty ratio of the nth period can be described as

$$d[n] = \frac{L}{(V_{in}-V_o)T_s}(i_{ref}[n-2]-i_{peak}[n-2]) - \frac{V_{in}}{V_{in}-V_o}d[n-1] - \frac{V_o}{V_{in}-V_o}d[n-2] + \frac{2V_o}{V_{in}-V_o} \tag{2.9}$$

For this method, the control objective has less than two period of time delay and when the duty cycle exceeds 50%, instability will occur. In addition, if the load change during the two period, as the sudden change of the current, the calculation of the duty ratio is invalid.

Prediction current mode control with delay compensation is introduced in [37, 39, 40, 38]. The control scheme is the same as the delay valley current control (2.4), however the duty ratio is updated every two switching periods. This would allocate more time for the microprocessor. The current reference is presumed to be constant during two switching period cycles.

$$i_{ref}[n] = i_{ref}[n-2] \tag{2.10}$$

The current at the end of nth switching period is assumed to be calculated as

$$i_L[n] = 2i_L[n-1] - i_L[n-2] \tag{2.11}$$

According to [39], every other period the duty ratio can be calculated as (2.12) using the assumptions above.

$$d[n] = \frac{L}{2V_{in}T_s}(i_{ref}[n-2] - 4i_L[n-2] + 3i_L[n-3]) + d[n-2] \tag{2.12}$$

Therefore, the inductor current, reference and voltages sampled in the former three cycles are used to calculated the duty ratio. The computational overhead of digital control is decreased compared with the previous techniques. This method is suitable for fast systems such as high-performance DC switchmode power supplies.

For the sake of avoiding instability that may exist in valley current control, compensated

digital current-mode control is presented in [41, 42]. Slightly different from (2.2) slightly, the control scheme can be defined as

$$i_L[n] = i_{ref}[n-1] + m_c d[n] T_s \tag{2.13}$$

Where, m_c is a compensating ramp.

According to [42], the equation to calculate the duty ratio can be modified as

$$d[n] = \frac{1}{1-\frac{Lm_c}{V_{in}}}\left(\frac{L}{V_{in}T_s}(i_{ref}[n-1] - i_L[n-1]) + \frac{V_o}{V_{in}}\right) \tag{2.14}$$

As for this method, the inductor current, reference and voltages are sampled at the beginning of every switching period and proper m_c is applied to calculate the duty ratio. According to [42], for buck converters, if $m_c > \frac{V_{in}}{L}$, the system is always stable.

To summarize, all of the control techniques described above are based on the state-space averaged approach and corresponding linearized approximate models. Most effort of these methods have been spent on finding a reasonable approach to calculate the duty ratio. However, the performance of these linear controllers would deteriorate under large parameter or load variations. Therefore, this has aroused a lot of interest in the development of nonlinear controllers for DC-DC converters. Some control schemes such as hysteresis control, sliding mode control are proposed in literature. By substituting the linear controllers with these nonlinear controllers in DC-DC converters, better regulation is achieved for a wider operating range.

Hysteresis controllers were first implemented in boost converters [43]. Since this control scheme has an inherently fast response in addition to being robust with simple design and implementation, a lot of related work can be found [44, 45, 46, 47]. Figure 2.7 is the diagram of a DC-DC converter with a simple voltage hysteresis controller [48]. Figure 2.8 shows the waveform of the output voltage (with hysteresis band used in the hysteresis controller) and the gate signal. The implementation of the hysteresis controller is simple. The switching states of the power stage is determined by comparison of the output voltage to its reference, considering a given hysteresis width for the error. DC-DC converters with hysteresis controllers responds to disturbances and load change right after the transient takes place [49]. Moreover, a compensation network is not needed for closed loop control. Due to all the advantages above, hysteresis control would be a good choice for DC-DC converters. However, the main concern associated with this method is that the switching frequency changes when the input voltage changes. This is not acceptable in many applications especially when converters are operated in parallel. Some work have been reported to deal with this problems in [50, 51, 52].

Sliding mode control (SM) is another nonlinear control strategy developed for controlling variable structure systems (VSSs) with good performance such as guaranteed stability and robustness against parameter, line, or load uncertainties [53, 54, 55]. The principle of SM control

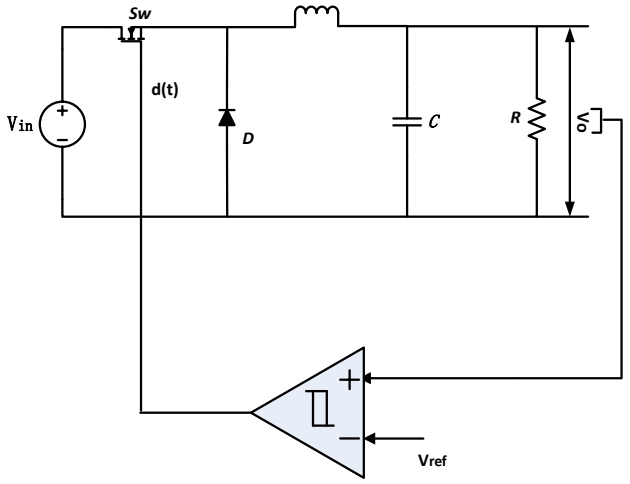

Figure 2.7: Block diagram of DC-DC converters with a hysteresis controller

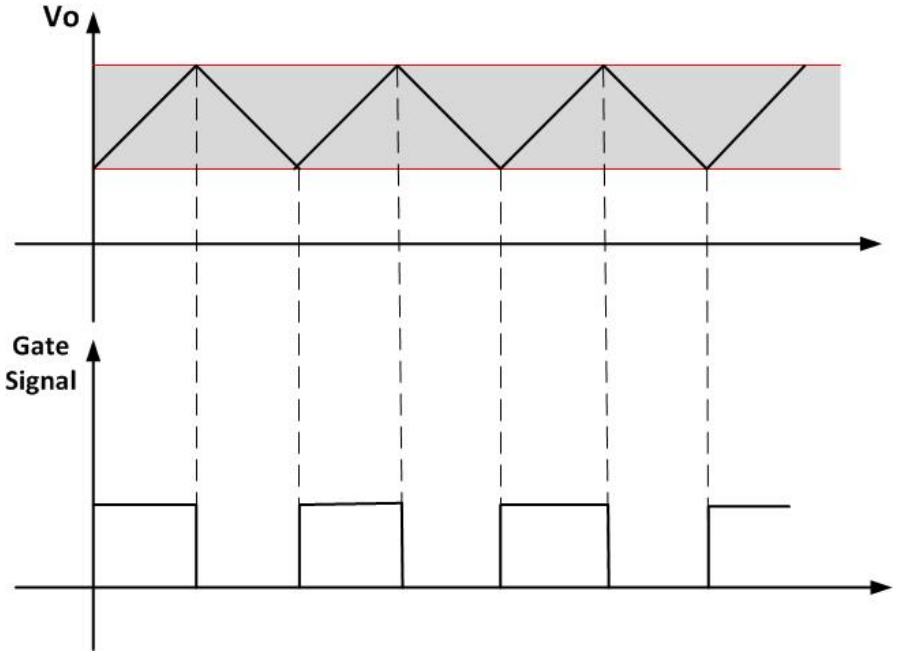

Figure 2.8: Waveform of the output voltage and the gate signal used in a hysteresis controller

is straightforward. A sliding surface is adopted as a reference path so that the controlled state variable can be directed towards the desired equilibrium as shown in Figure 2.9. DC-DC converters are inherently variable structure systems due to the switching property. Therefore, sliding control design and analysis for DC-DC converters has drawn lots of research interests. Bilalović *et al*. is the first group that worked on developing SM controller for DC-DC converters. In [56], a preliminary sliding mode controller was applied to a buck converter. Then SM control was applied to higher order converters such as second-order DC-DC converters by Venkataramanan *et al*. [57] and fourth-order Cuk converter by Huang *et al*. [58]. In 1997, a comparative study on buck converter's performance under different control scheme was presented by Raviraj and

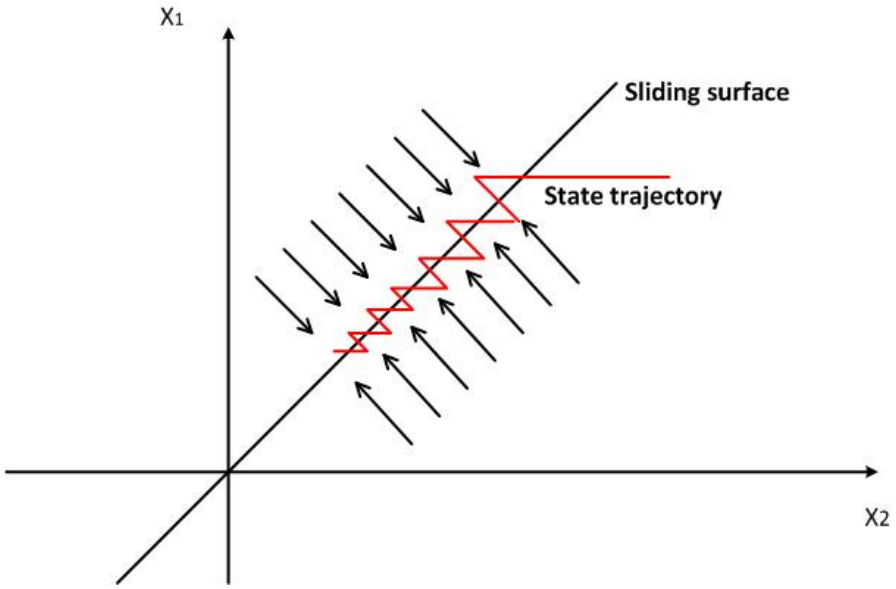

Figure 2.9: Sliding surface and state trajectory in the state-space

Sen [59]. It was found that fuzzy-logic and SM controller show certain similarities in the system behavior. SM controllers were also developed for parallel connected converters [60, 61]. However, in spite of being a popular research topic, most of the literature focus on theoretical aspects. Seldom SM control has been adopted in practical DC-DC converters. The main reason is the high and variable switching frequency, which would result in excessive power losses, electromagnetic-interference generation and filter-design complication.

2.1.3 Current Issues

Although these conventional control approaches may be adequate in some cases, the controller performance is quite limited, and the design involves a number of heuristic procedures, which lack theoretical guarantees. This motivates the study of advanced control technology for DC-DC power electronics converters, and a large number of control methods have been developed or tailored to control problems of DC-DC converters, e.g., sliding mode control [62, 63, 64, 65], fuzzy logic control [66], adaptive control [67], robust control [68] model predictive control [69, 38], artificial neural network control [70], Lyapunov-based control [71, 72, 73], to just mention a few.

Despite the effectiveness of these approaches, there are still a number of challenges that need to be tackled. In some applications, the output voltage of DC-DC power converters are required to track a changing reference signal or adjust manually, e.g., the power system of microprocessors [74, 75] or the power supply of a variable envelope radio frequency power amplifier [76, 77]. Many small-signal control approaches may not perform well for this scenario and even become unstable [78], since the controller is usually designed based on a model linearized or discretized at an operating point of interest. For large-signal control design, quantized

characterizations on stability, robustness, and performance are usually unavailable, and their stability, robustness, and performance need to be evaluated through experiment. In addition, digital implementation of most nonlinear controllers remains a problem as either the control design is based on continuous models or the online computation demand is too high.

Another issue in the design of DC-DC power electronics converters is the tradeoff between performance and efficiency. Fast dynamic response and low output ripple can be achieved by adopting a high switching frequency. However, over-rapid switching will impair energy efficiency and pose a challenge to thermal management [79]. It may be attractive if the switching frequency can be adjusted during the operation. For instance, in battery-operated systems, variable frequency operation is shown to give better energy efficiency and provide wider range of usable power [80]. Although there are some preliminary results along this direction [81], the problem has not been fully investigated.

2.2 Control Methods for DC-AC Inverters

DC-AC inverters are power conversion devices which can transfer power from direct current (DC) to alternating current (AC). The applications of DC-AC inverter can be found in a variety of sectors, such as industrial [82], transportation [83], power systems[13], renewable energies [84], etc. The development of the DC-AC inverter and its control has been mainly driven by industry application and the technology innovation, such as power semiconductors, digital signal processor and new inverter topologies. In the past, the control efforts have mainly been placed on stabilization and robustness of the inverters. However, nowadays as DC-AC inverters have been used in more complicated application, more flexible inverter control systems is required. Generally speaking, the most popular control methods of DC-AC inverters can be classified as four types:

- Linear control based on time-average model and PWM modulation
- Hysteresis control
- Sliding mode control
- Model predictive control

In the rest of this section, literature related to these four control types is introduced briefly.

2.2.1 Linear Control

Same as DC-DC converters, the most commonly used control methods on DC-AC inverters are linear controllers, such as proportional-integral(PI) controllers, in conjunction with PWM

modulation [85][86]. Due to the number of power switches, modulation techniques are adopted, such as, carrier-based sinusoidal PWM [87], and space vector PWM [88].

As DC-AC inverters are widely used in motor drives, a well-known control scheme based on linear control theory is field-oriented control (FOC) [89][90]. Figure 2.10 shows a FOC control diagram of AC motor drive control with a 3-phase bridge inverter [1]. Two PI controllers are used to produce the voltage references for the space vector modulation (SVM). Additional coordinate transformations are required in this control scheme. For motor drive application, the control design are subject to several technical contraints, such as total harmonic distortion (THD), maximum current, etc. Hence, the design of PI controllers can be very challenging task as these constraints cannot be included in the control design directly.

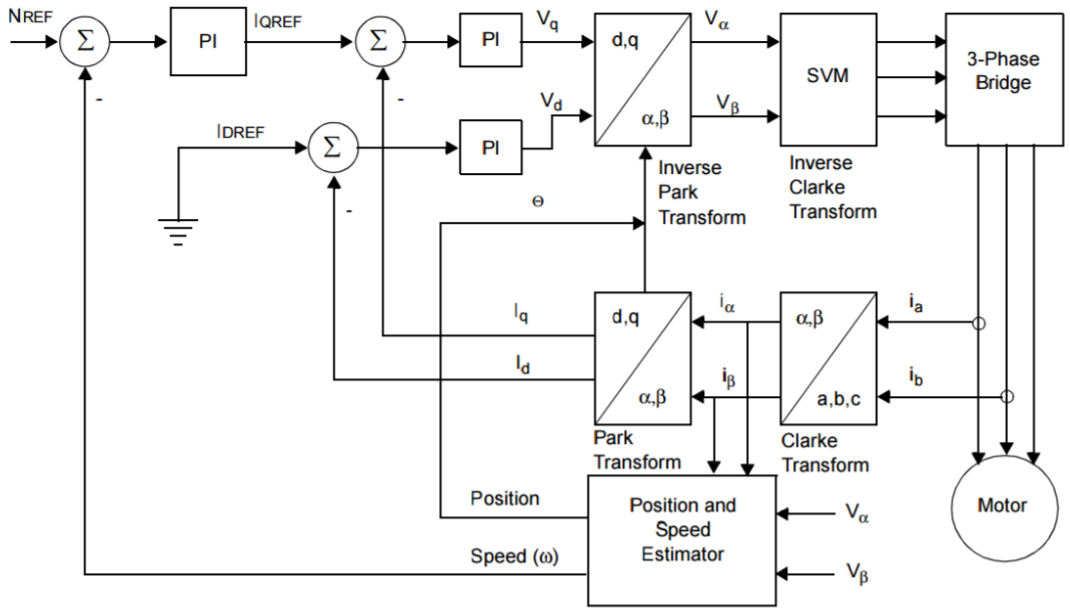

Figure 2.10: Field-oriented control diagram [1]

2.2.2 Hysteresis Control

Nonlinear control techniques were also developed for DC-AC inverters. However, most of them seldom can be seen in practical applications. Hysteresis controller is a exception. Direct torque control (DTC), which is based on hysteresis control, has been used extensively in ABB's variable-speed drives since 1996. The accuracy of motor speed and torque control has been greatly improved [91]. As shown in Figure 2.11, compared to Field-Oriented Control, it does not require any coordinate transformation. The switching states of the inverter are generated by comparing the motor torque and flux to their references with a given hysteresis band. However, in order to implement this kind of method on a digital platform, a high sampling frequency is required. Furthermore, the selection of the hysteresis band can be very tricky in some applications in order to avoid resonance problems [92].

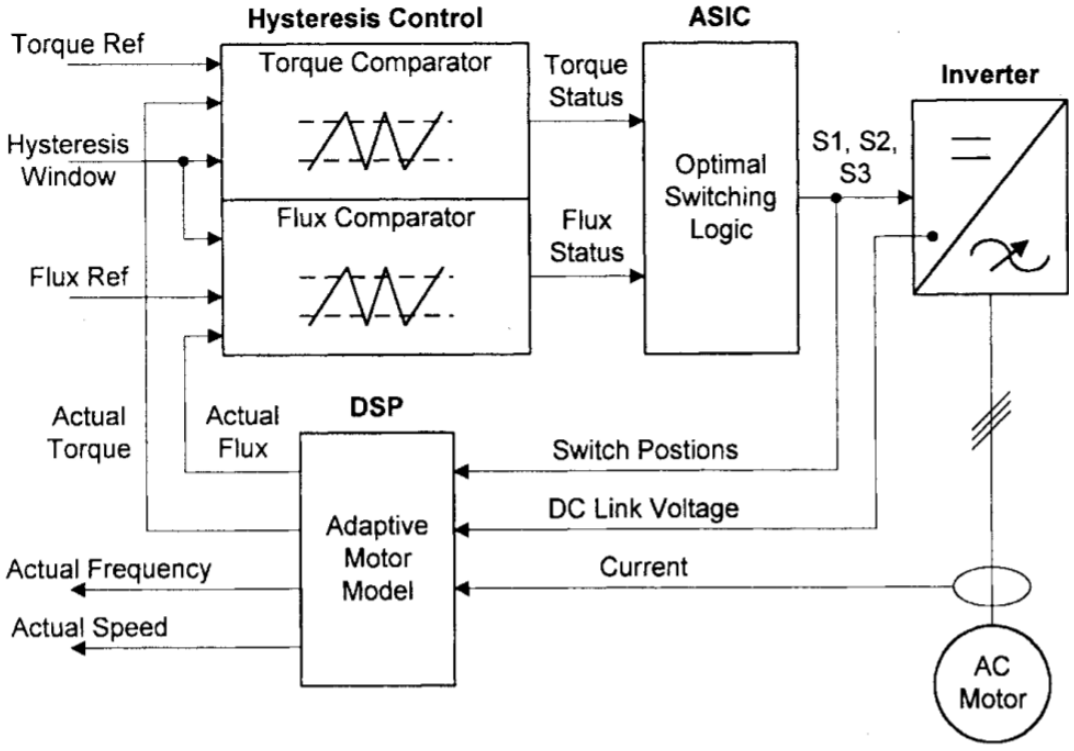

Figure 2.11: Direct torque control diagram [2]

2.2.3 Sliding Mode Control

Sliding mode control is another nonlinear control technique, which has attracted a great deal of research interests in the field of AC motor drive control [93][94][95]. Figure 2.12 demonstrate a current regulator based on sliding mode control. A sliding surface is designed for the error between the current and its reference. The sliding mode controller can generate the switching control signals for the power switches directly without modulation circuits. The main advantage of the sliding mode controller is the robustness behaviour against disturbances and uncertainties. However, the switching action of the controller can excite some unmodelled dynamics, which results in chattering problems. Additional efforts are needed to solve this issue [96].

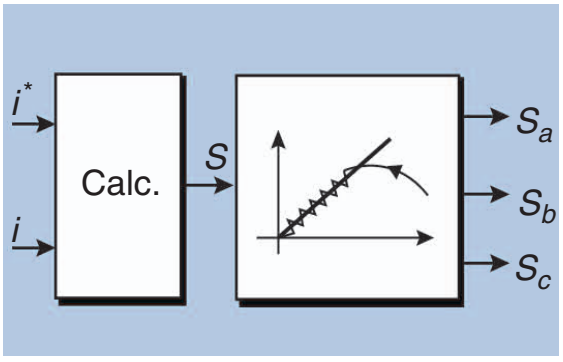

Figure 2.12: Sliding mode control diagram [3]

2.2.4 Model Predictive Control

Instead of considering the inverter as a linear system, another interesting alternative is predictive control[97][98][99]. The future behaviour of the system state is predicted based on the model of the system. The optimal actuation of the controller is obtained by using of the future information and obeying the predefined constraints. The predictive control method can be generally divided into four types: deadbeat control [100], hysteresis based [101], trajectory based [102] and model predictive control [103]. But in order to predict the behavior of the system in real time, a powerful microprocessor is necessary to handle the computational burden, and the accuracy of the predictions are highly sensitive to the variation of system parameters.

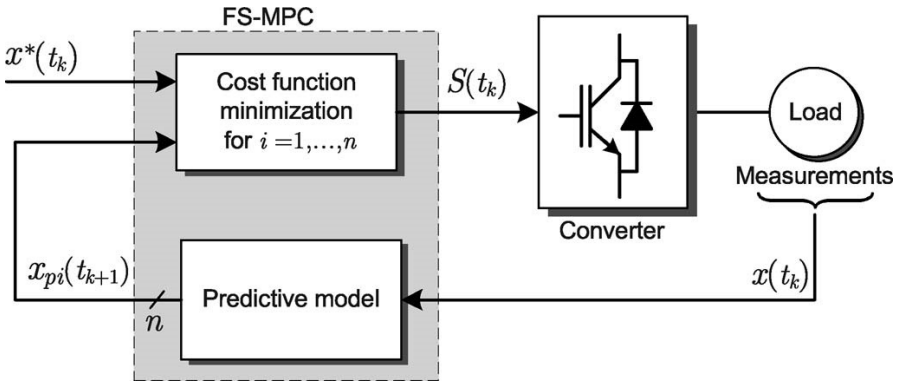

Figure 2.13: Model predictive control diagram [4]

2.3 Hybrid Modelling and Control

Due to the existence of switch circuits, the dynamical behavior of power converters contains both continuous and discrete dynamics. Furthermore, it should be emphasized that the continuous and discrete dynamics coexist and interact with each other. Extensive research literature have been proposed for improving the control synthesis, but most of the proposed control techniques are based on averaged models of the power converters.

Thus, the performance of power converters may be improved if advanced modelling theory can be applied to describe this kind of hybrid features and meanwhile corresponding control synthesis techniques can be developed. Hybrid modelling is one of most suitable modelling methods to capture both continues and discrete dynamics of power converters. There have been significant research activities in the area of hybrid modelling and control in the past decades involving researchers from several areas such as control engineering, mathematics and computer science [104, 105, 106, 107].

Several mathematical paradigms have been employed for modelling hybrid systems. Generally, two basic kind of models can be obtained.

1. **Hybrid automaton**, which is a finite-state machine, can be described by a triple (X, Q, E). $X \subset \mathbf{R}^n$ is the finite continuous state-space, $Q = q_1, \ldots, q_m$ is a finite set called the *alphabet*; the elements in Q are called symbols, which denote the discrete states of hybrid system. E is the subset of $X \times Q \times X$ called *transition strategy* and its elements are called *events*. A sequence $(q_0, q_1, \ldots, q_{m-1})$ with $(q_i, q_{i+1}) \in E$ for $i = 1, 2, \ldots, m$ is called a path or trajectory. Then the finite state-space can be separated as several subsets $I_q \subset X$ by the discrete states. This method was first used by Lucio in [108]. Nerode and Kohn [109] combined ordinary differential equations (ODEs) and finite automata to obtain a hybrid model. Brockett [110] took interacting ODEs and discrete phenomena to describe motion systems. On the other hand, different control techniques have been adopted based on this model. A semi-decision procedure was presented [111] for control a linear hybrid automata. Game theoretic methodologies were shown in [112] in a unified framawork for synthesizing controllers for nonlinear hybrid automata. Another common approach applied on hybrid system is model predictive control. As for the model predictive control, the system model is applied to predict the future behavior of the state variables over a finite time interval. Based on a so-called "cost function", available prediction actions are evaluated to produce a control sequence that minimizes the cost function. Only the first control policy is implemented, and then the same prediction procedure repeats every sampling period. Due to the high amount of calculations for the online implementation, model predictive control has few applications in power converter control [113, 114, 115, 116, 5]. In [113], one solution to overcome this shortcoming is to solve the optimization problem off-line. A search tree is employed to reduce the computational time. In [114], the optimization problem is solved analytically based on Generalised Predictive Control (GPC). However, system constraints and nonlinearities could not be considered via GPC.

2. **Switched system** is a combination of continuous-time subsystems and a switching law that determine which subsystem is active. It can be depicted as:

$$\dot{x}(t) = f_\sigma(x(t), u(t)) \tag{2.15}$$

where $x \in R^n$ and the index function $\sigma : R^n \to \Xi = \{1, 2 \ldots m\}$. At every time instant only one subsystem is active governed by the index function. The index function might be time-dependent, state-dependent or event-dependent. During the past decades, increasing research efforts have been placed on analysis and synthesis of the switched system [117] [118][119]. Ye et al. [120] developed a model suitable for the qualitative analysis of wide range switched systems. Sufficient conditions for uniform stability, uniform asymptotic stability, exponential stability, and instability of an invariant set of such systems were also established. In [121], Branicky, Borkar and Mitter propose a general framework

that systematizes the notion of a switched system. Multiple Lyapunov functions are utilized for stability analysis of switched systems. Johansson and Rantzer [122] presented a computational approach to stability analysis of nonlinear and hybrid systems. A convex optimization problem in terms of linear matrix inequalities (LMIs) is formulated to obtain the stability condition. A methodology for analyzing controllability and synthesizing control laws for a class of hybrid systems was defined in [123] which could be used to generate correct switching action to transfer the hybrid plant between predefined subsets of the hybrid state-space.

Research papers on the modelling, analysis and synthesis of hybrid systems are relatively rich, which provide sufficient theoretical foundation for the application in the area of power electronics. However, this is not a straightforward task. most of the attention has been placed on the theoretical research. It is still rarely applied in practical situation. The hybrid modelling theory applied to power electronics devices design is also a relative new area. The related research work in this field is also limited. There are various reasons for this.

1. There is a lack of understanding of how to use hybrid modelling theory in power converters design.
2. The more accurate dynamical behavior taken into consideration always means more complicated control techniques. The computation ability of conventional microprocessor limits the application of advanced control techniques.
3. The practical worthiness of using hybrid modelling is generally unproven.

2.4 Summary

	Linear controller	**Hybrid modelling and control**
Model	Linear model with approximation	Hybrid model without approximation
Controller design	Compensator parameter tuning (root locus or pole placement)	Cost function definition
Modulation	PWM	No modulation
Implementation	Analogical or digital	Direct digital implementation
Switching frequency	Fixed	Controllable (variable or fixed)
Flexibility	Constraints inclusion is not straight forward	Constraints include directly in the switching law design

Table 2.1: Comparison between classical linear controller and hybrid control

A summary of most distinctive characteristics of both conventional linear control and hybrid control is given in Table 2.1. Due to the advantages of hybrid modelling and control, it is of great interest to investigate new control scheme to obtain higher performance power converters.

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Part I

DC-DC Converters

Chapter 3

Review of Conventional Control Design for DC-DC Converters

3.1 Linear Controller Design Based on the SSA Approach

The DC-DC power stage performs the basic power conversion from the input voltage to the output voltage and includes switches. The control circuit is designed to derive the switching power semiconductors (switches). Among all kind of topologies, the DC-DC buck converter is a specific type of DC-DC converter used in many industry and home application, such as power management in personal computer, and regulation circuit in power supply. In this section, the analysis and design of linear control structures is done for the buck converter based on the state-space averaged approach (SSA).

3.1.1 Introduction of the DC-DC Buck Converter and Steady State Analysis

The buck converter, also called "step-down converter", is designed to convert DC voltage to a lower level with minimal ripple. Figure 3.1 shows a basic schematic of the buck power stage. It consists of a power semiconductor S_W which can be a MOSFET or an IGBT, a freewheeling diode D, an inductor L, a capacitor C and a load resistance R. During one operation period, S_W switchs on and off governed by the control circuit, The switching action results in a series of pulses at the junction node of S_W, D and L. Then the power from the input sources is filtered by the L/C output filter to generate a lower DC output voltage v_O.

Classified by the continuity of the inductor current flow, the buck power stage can be operated in two modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). It is assumed that all the components are ideal. Details of the two different modes are discussed below.

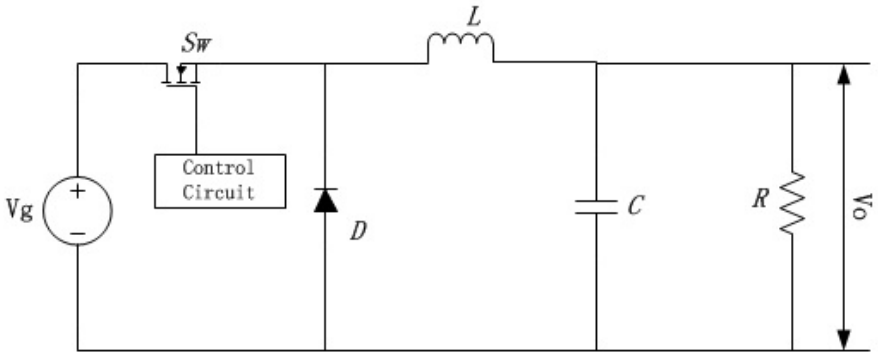
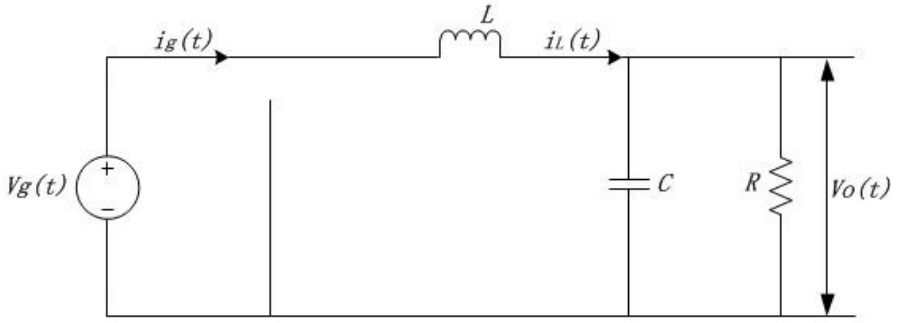


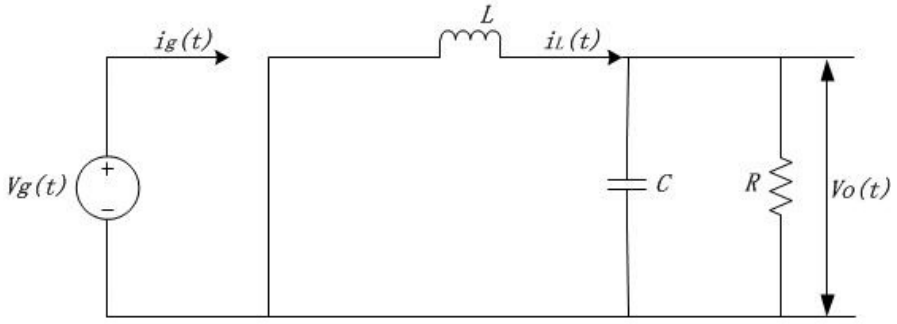
Figure 3.1: A buck converter topology

3.1.1.1 Continuous Conduction Mode

in continuous conduction mode, the buck converter has two states per switching period. a simple linear circuit can represent each of the two states where the switches in the circuit are replaced by ideal equivalent circuits. Figure 3.2 is the circuit diagram for each state. the dynamic behaviors of the inductor current and capacitor voltage are different between states.



(a) ON STATE



(b) OFF STATE

Figure 3.2: The equivalent circuit of buck converter (CCM)

ON STATE The ON state (Figure 3.2a) is when S_W is on and D is off during $(0, dT_s)$ for a switching period T_s (d is the duty ratio, and D_d is the steady value of the duty ratio d), and the

inductor is energised. The dynamic equations of the inductor current i_L and the capacitor voltage v_C are given by (3.1).

$$\begin{aligned} \frac{di_L}{dt} &= \frac{1}{L}(v_g - v_O) \\ \frac{dv_C}{dt} &= \frac{1}{C}\left(i_L - \frac{v_O}{R}\right) \end{aligned} \tag{3.1}$$

The input current i_g is equal to the inductor current i_L and the output voltage v_O is equal to the capacitor voltage v_C, then

$$\begin{aligned} i_g &= i_L \\ v_O &= v_C \end{aligned} \tag{3.2}$$

The state equation and output equation can be obtained from (3.1) and (3.2).

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.3}$$

$$\begin{bmatrix} i_g \\ v_O \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.4}$$

OFF STATE The OFF state (Figure 3.2b) is when S_W is off and D is on during (dT_s, T_s), the inductor is dis-energised. The dynamic equations of the inductor current i_L and the capacitor voltage v_C for this portion of switching period are given by (3.5).

$$\begin{aligned} \frac{di_L}{dt} &= \frac{1}{L}(-v_O) \\ \frac{dv_C}{dt} &= \frac{1}{C}\left(i_L - \frac{v_O}{R}\right) \end{aligned} \tag{3.5}$$

For S_W off, the input current i_g is zero and the output voltage v_O is equal to the capacitor voltage v_C, then

$$\begin{aligned} i_g &= 0 \\ v_O &= v_C \end{aligned} \tag{3.6}$$

The state equation and output equation can be obtained from (3.5) and (3.6).

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.7}$$

$$\begin{bmatrix} i_g \\ v_O \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.8}$$

The state-space representation of the buck converter operated as continuous conduction mode (CCM) is described as

$$\frac{dx}{dt} = \begin{cases} A_1 x + B_1 u & (ON) \\ A_2 x + B_2 u & (OFF) \end{cases} \tag{3.9}$$

$$y = \begin{cases} C_1 x + E_1 u & (ON) \\ C_2 x + E_2 u & (OFF) \end{cases} \tag{3.10}$$

Where $x = [i_L \quad v_C]^T$ is the state vector, $u = [v_g]$ is the input vector, and $y = [i_g \quad v_O]^T$ is the output vector.

The state matrices for the ON and OFF periods are

$$\begin{aligned} A_1 = A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \\ C_1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad C_2 = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \quad E_1 = E_2 \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{aligned} \tag{3.11}$$

Figure 3.3 shows the waveform of inductor current under continuous conduction mode (CCM).

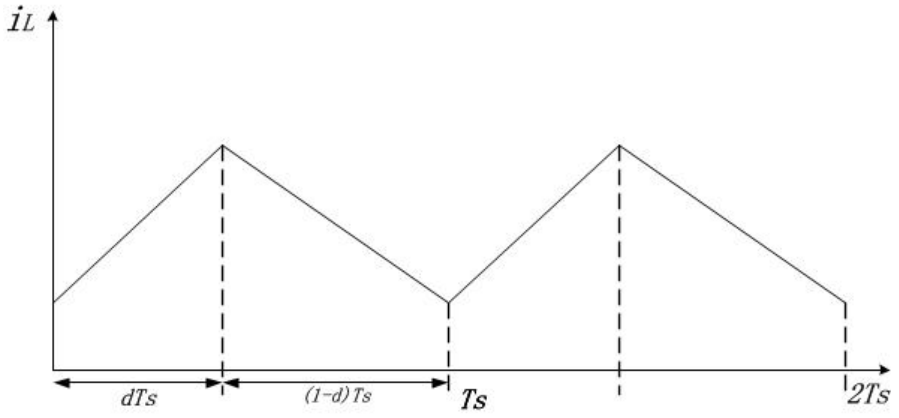


Figure 3.3: Inductor current waveform of the buck converter (CCM)

3.1.1.2 Discontinuous Conduction Mode

When the load is light enough (for example: large resistance value), the buck converter will operate in a discontinuous conduction mode (DCM). The buck converter has three states per switching period in this mode. During a switching cycle, the inductor current stays at zero for a while after ON and OFF period as shown in Figure 3.4, so it is called “discontinuous”. Same as CCM, a simple linear circuit can represent each of the three states where the switches in the circuit are replaced by ideal equivalent circuits. Figure 3.5 is the circuit diagram for each state. The dynamic behaviors of the inductor current and the capacitor voltage are different between states.

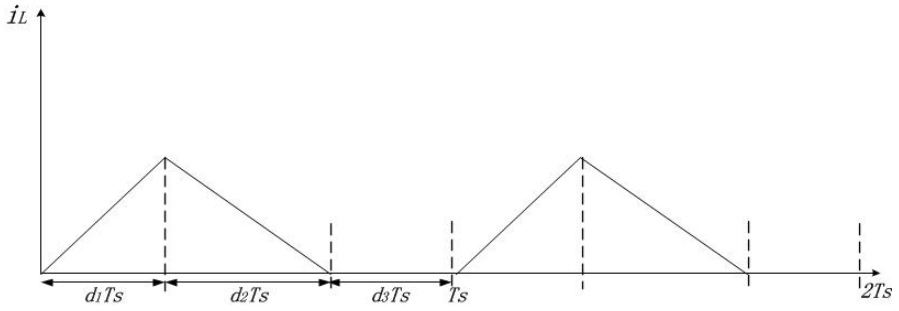


Figure 3.4: Inductor current waveform of the buck converter (DCM)

ON STATE The ON state (Figure 3.5a) is when S_W is on and D is off during $(0, d_1 T_s)$ for a switching period T_s, the inductor is energised. The dynamic equations of the inductor current i_L and the capacitor voltage v_C are given by (3.12).

$$\begin{aligned} \frac{di_L}{dt} &= \frac{1}{L}(v_g - v_O) \\ \frac{dv_C}{dt} &= \frac{1}{C}\left(i_L - \frac{v_O}{R}\right) \end{aligned} \tag{3.12}$$

The input current i_g is equal to the inductor current i_L and the output voltage v_O is equal to the capacitor voltage v_C, then

$$\begin{aligned} i_g &= i_L \\ v_O &= v_C \end{aligned} \tag{3.13}$$

The state equation and output equation can be obtained from (3.12) and (3.13).

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.14}$$

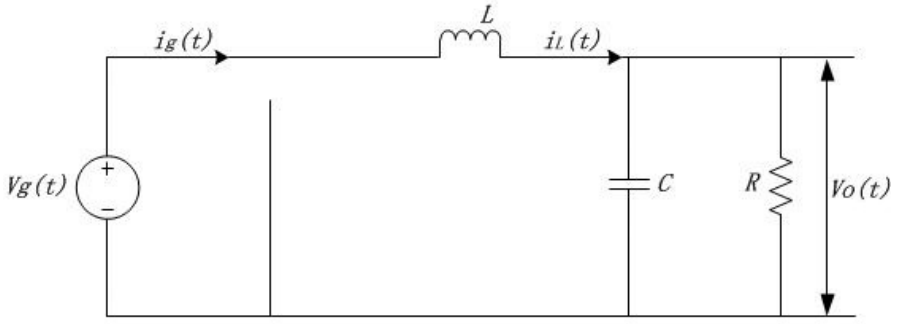
$$\begin{bmatrix} i_g \\ v_O \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.15}$$

OFF STATE The OFF state (Figure 3.5b) is when S_W is off and D is on during $(d_1 T_s, d_2 T_s)$, the inductor is dis-energised. The dynamic equations of the inductor current i_L and the capacitor voltage v_C for this portion of switching period are given by (3.16).

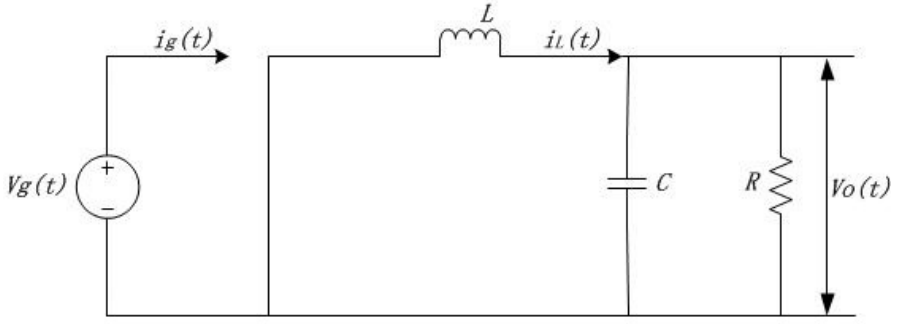
$$\begin{aligned} \frac{di_L}{dt} &= \frac{1}{L}(-v_O) \\ \frac{dv_C}{dt} &= \frac{1}{C}\left(i_L - \frac{v_O}{R}\right) \end{aligned} \tag{3.16}$$

For S_W is off, the input current i_g is zero and the output voltage v_O is equal to capacitor voltage v_C, then

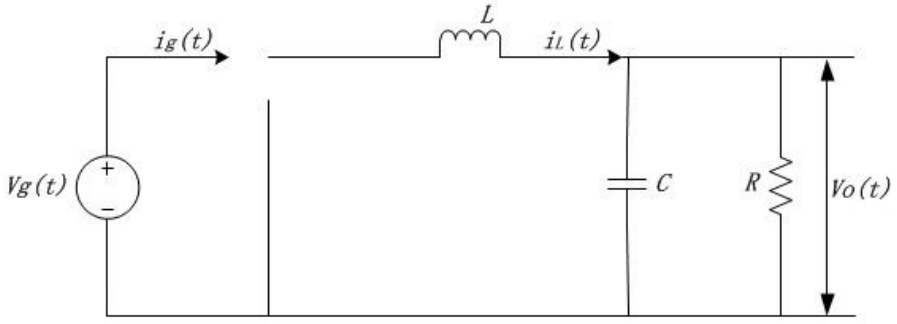
$$\begin{aligned} i_g &= 0 \\ v_O &= v_C \end{aligned} \tag{3.17}$$



(a) ON STATE



(b) OFF STATE



(c) ZERO STATE

Figure 3.5: The equivalent circuit of the buck converter (DCM)

The state equation and output equation can be obtained from (3.16) and (3.17).

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.18}$$

$$\begin{bmatrix} i_g \\ v_O \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.19}$$

ZERO STATE The zero state (Figure 3.5c) is when S_W and D are both off during (d_2T_s, T_s). This could happen because the inductor discharges totally and the current becomes zero before the next switching cycle. The dynamic equations of the inductor current i_L and the capacitor

voltage v_C for this portion of switching period are given by (3.20).

$$\begin{aligned} \frac{di_L}{dt} &= 0 \\ \frac{dv_C}{dt} &= -\frac{v_O}{RC} \end{aligned} \tag{3.20}$$

The input current and output voltage have the same form as OFF state (3.6). Then the state equation and output equation of zero state can be obtained from (3.20) and (3.6).

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.21}$$

$$\begin{bmatrix} i_g \\ v_O \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.22}$$

The state-space representation of the buck converter operating in discontinuous conduction mode (DCM) can therefore be described as

$$\frac{dx}{dt} = \begin{cases} A_1 x + B_1 u & (ON) \\ A_2 x + B_2 u & (OFF) \\ A_3 x + B_3 u & (ZERO) \end{cases} \tag{3.23}$$

$$y = \begin{cases} C_1 x + E_1 u & (ON) \\ C_2 x + E_2 u & (OFF) \\ C_3 x + E_3 u & (ZERO) \end{cases} \tag{3.24}$$

Where $x = [i_L \quad v_C]^T$ is the state vector, $u = [v_g]$ is the input vector, and $y = [i_g \quad v_O]^T$ is the output vector.

The state matrices for the ON, OFF and ZERO periods are

$$\begin{aligned} A_1 = A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \\ B_2 = B_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad C_1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad C_2 = C_3 = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \\ E_1 = E_2 = E_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{aligned} \tag{3.25}$$

3.1.2 Small Signal Analysis and State-Space Averaged Approach Modeling

It should be mentioned that the steady state analysis of the DC-DC converter above is based on the assumption that the input voltage is an ideal DC voltage source. However, in a real system,

the input voltage contains harmonic components. On the other hand, the power stage of a DC-DC converter is a nonlinear, time-varying system. Hence modeling the power stage presents one of the main challenges to the designer. Since it was introduced in 1977 [22], the State-Space Averaged approach (SSA) has became one of the essential techniques for modeling switched mode power conversion circuits. In this section, modelling of the buck power stage using the state-space averaged approach is discussed step by step. Only the continuous conduction mode (CCM) of buck converter is considered.

Step 1: State-Space Averaged Model

In order to eliminate the high frequency switching ripple, we take the average over one switching cycle of all the variables in (3.9).

$$\begin{aligned}\langle x(t)\rangle_{Ts} &= \frac{1}{T_s}\int_t^{t+T_s} x(\tau)d\tau \\ \langle u(t)\rangle_{Ts} &= \frac{1}{T_s}\int_t^{t+T_s} u(\tau)d\tau \\ \langle y(t)\rangle_{Ts} &= \frac{1}{T_s}\int_t^{t+T_s} y(\tau)d\tau\end{aligned} \tag{3.26}$$

Then the differential of state vector $\langle \dot{x}\rangle_{Ts}$ can be calculated as:

$$\langle \dot{x}(t)\rangle_{Ts} \quad = \frac{d}{dt}\left(\frac{1}{T_s}\int_t^{t+T_s} x(\tau)d\tau\right) = \frac{1}{T_s}\int_t^{t+T_s} \dot{x}(\tau)d\tau \tag{3.27}$$

Substituting (3.9) in (3.27), one obtains

$$\begin{aligned}\langle \dot{x}(t)\rangle_{Ts} &= \frac{1}{T_s}\left(\int_t^{t+dT_s} \dot{x}(\tau)d\tau + \int_{t+dT_s}^{t+T_s} \dot{x}(\tau)d\tau\right) \\ &= \frac{1}{T_s}\left(\int_t^{t+dT_s} [A_1x(\tau)+B_1u(\tau)]\,d\tau + \int_{t+dT_s}^{t+T_s} [A_2x(\tau)+B_2u(\tau)]\,d\tau\right)\end{aligned} \tag{3.28}$$

(3.28) can be simplified by (3.9) as

$$\langle \dot{x}(t)\rangle_{Ts} = \frac{1}{T_s}\left([A_1\langle x(\tau)\rangle + B_1\langle u(\tau)\rangle]\,dT_s + [A_2\langle x(\tau)\rangle + B_2\langle u(\tau)\rangle]\,d^{'}T_s\right) \tag{3.29}$$

where $d^{'} = 1-d$

After simplification of (3.29), the average state equation can be described as

$$\langle \dot{x}(t)\rangle_{Ts} = \left[d(t)A_1 + d^{'}(t)A_2\right]\langle x(t)\rangle_{Ts} + \left[d(t)B_1 + d^{'}(t)B_2\right]\langle u(t)\rangle_{Ts} \tag{3.30}$$

Using the same method, the average output equation can be easily obtained

$$\langle y(t)\rangle_{Ts} = \left[d(t)C_1 + d^{'}(t)C_2\right]\langle x(t)\rangle_{Ts} + \left[d(t)E_1 + d^{'}(t)E_2\right]\langle u(t)\rangle_{Ts} \tag{3.31}$$

Therefore, the state-space averaged model is expressed by (3.30) and (3.31)

Step 2: Steady State Equilibrium

We define that the capital letters of variables indicate the steady state. Substitute the steady state value into (3.30) and (3.31):

$$\begin{aligned} \dot{X} &= AX + BU \\ Y &= CX + EU \end{aligned} \tag{3.32}$$

where

$$\begin{aligned} A &= D_d A_1 + D_d^{'} A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\ B &= D_d B_1 + D_d^{'} B_2 = \begin{bmatrix} \frac{D_d}{L} \\ 0 \end{bmatrix} \\ C &= D_d C_1 + D_d^{'} C_2 = \begin{bmatrix} D_d & 0 \\ 0 & 1 \end{bmatrix} \\ E &= D_d E_1 + D_d^{'} E_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{aligned}$$

Because the differential of steady state is zero ($\dot{X} = 0$), the steady state equilibrium can be derived from (3.32) as

$$\begin{aligned} X &= \begin{bmatrix} I_L \\ V_C \end{bmatrix} = -A^{-1}BU = \begin{bmatrix} \frac{D_d}{R} \\ D_d \end{bmatrix} V_g \\ Y &= \begin{bmatrix} I_g \\ V_O \end{bmatrix} = (E - CA^{-1}B)U = \begin{bmatrix} \frac{D_d^2}{R} \\ D_d \end{bmatrix} V_g \end{aligned} \tag{3.33}$$

Step 3: Perturbation and Linearization

The main idea of perturbation and linearization is introducing a small variation (small signal) around the steady state equilibrium point. If the variation is kept small, the nonlinear behavior of a small signal can be represented accurately by a linear model. We divide the average

signal in two parts: DC quantity and small ac quantity.

$$\begin{aligned}
\langle x(t)\rangle_{Ts} &= X+\hat{x}\\
\langle u(t)\rangle_{Ts} &= U+\hat{u}\\
\langle y(t)\rangle_{Ts} &= Y+\hat{y}\\
\langle d(t)\rangle_{Ts} &= D_d+\hat{d}\\
\left\langle d^{'}(t)\right\rangle_{Ts} &= 1-d(t) = D_d-\hat{d}
\end{aligned} \tag{3.34}$$

where the ˆ(hat) above the quantities indicates small ac quantities.

Then substituting (3.34) into the state-space averaged model, we have

$$\begin{aligned}
\dot{X}+\dot{\hat{x}}(t) &= AX+BU+A\hat{x}(t)+B\hat{u}(t)+[(A_1-A_2)X+(B_1-B_2)U]\hat{d}(t)\\
&\quad +(A_1-A_2)\hat{x}(t)\hat{d}(t)+(B_1-B_2)\hat{u}(t)\hat{d}(t)\\
Y+\hat{y}(t) &= CX+EU+C\hat{x}(t)+E\hat{u}(t)+[(C_1-C_2)X+(E_1-E_2)U]\hat{d}(t)\\
&\quad +(C_1-C_2)\hat{x}(t)\hat{d}(t)+(E_1-E_2)\hat{u}(t)\hat{d}(t)
\end{aligned} \tag{3.35}$$

Combining (3.32) and (3.35), one obtains

$$\begin{aligned}
\dot{\hat{x}}(t) &= A\hat{x}(t)+B\hat{u}(t)+[(A_1-A_2)X+(B_1-B_2)U]\hat{d}(t)\\
&\quad +(A_1-A_2)\hat{x}(t)\hat{d}(t)+(B_1-B_2)\hat{u}(t)\hat{d}(t)\\
\hat{y}(t) &= C\hat{x}(t)+E\hat{u}(t)+[(C_1-C_2)X+(E_1-E_2)U]\hat{d}(t)\\
&\quad +(C_1-C_2)\hat{x}(t)\hat{d}(t)+(E_1-E_2)\hat{u}(t)\hat{d}(t)
\end{aligned} \tag{3.36}$$

(3.36) are nonlinear equations. The nonlinear components are all product of small signals. If we assume the small signals are small enough compared with DC quantities, the product of small signals can be eliminated from the nonlinear equation without introducing considerable errors. By doing this, the linear small signal model is as follow

$$\begin{aligned}
\dot{\hat{x}}(t) &= A\hat{x}(t)+B\hat{u}(t)+[(A_1-A_2)X+(B_1-B_2)U]\hat{d}(t)\\
\hat{y}(t) &= C\hat{x}(t)+E\hat{u}(t)+[(C_1-C_2)X+(E_1-E_2)U]\hat{d}(t)
\end{aligned} \tag{3.37}$$

Step 4: Small Signal Model Analysis

Based on the small signal model, we can analyse the dynamic behavior of the power stage, which is crucial for controller design. Taking the *Laplace* transform of (3.37) and letting the initial condition be zero, the state vector and output vector in frequency domain can be obtained

$$\begin{aligned}
\dot{\hat{x}}(s) &= (sI-A)^{-1}B\hat{u}(s)+(sI-A)^{-1}[(A_1-A_2)X+(B_1-B_2)U]\hat{d}(s)\\
\hat{y}(s) &= \left(C(sI-A)^{-1}B+E\right)u(s)\\
&\quad +\{C(sI-A)^{-1}[(A_1-A_2)X+(B_1-B_2)U]+[(C_1-C_2)X+(E_1-E_2)U]\}\hat{d}(s)
\end{aligned} \tag{3.38}$$

From (3.38), the transfer functions between different variables can be achieved.

1. Transfer function vector $G_{xg}(s)$ from the input voltage $\hat{v}_g(S)$ to the state vector $\hat{x}(s)$

$$G_{xg}(s) = \frac{\hat{x}(s)}{\hat{v}_g(S)}\bigg|_{\hat{d}(s)=0} = (sI - A)^{-1}B \tag{3.39}$$

2. Transfer function vector $G_{xd}(s)$ from the control input (duty ratio) $\hat{d}(s)$ to the state vector $\hat{x}(s)$

$$G_{xd}(s) = \frac{\hat{x}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_g(s)=0} = (sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_g] \tag{3.40}$$

3. Transfer function vector $G_{yg}(s)$ from the input voltage $\hat{v}_g(S)$ to the output vector $\hat{y}(s)$

$$G_{yg}(s) = \frac{\hat{y}(s)}{\hat{v}_g(s)}\bigg|_{\hat{d}(s)=0} = C(sI - A)^{-1}B + E \tag{3.41}$$

4. Transfer function vector $G_{yd}(s)$ from the control input (duty ratio) $\hat{d}(s)$ to the output vector $\hat{y}(s)$

$$\begin{aligned} G_{yd}(s) = \frac{\hat{y}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_g(s)=0} &= C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_g] \\ &+ (C_1 - C_2)X + (E_1 - E_2)V_g \end{aligned} \tag{3.42}$$

Substituting the parameters (3.11) into (3.39), the transfer function $G_{vg}(s)$ from the input voltage $\hat{v}_g(S)$ to the output voltage $\hat{v}_O(s)$ of the buck power stage is

$$G_{vg}(s) = \frac{\hat{v}_O(s)}{\hat{v}_g(s)}\bigg|_{\hat{d}(s)=0} = \frac{D_d}{1 + s\frac{L}{R} + s^2LC} \tag{3.43}$$

Then substituting the parameters (3.11) into (3.40), the transfer function $G_{vd}(s)$ from the control input (duty ratio) $\hat{d}(s)$ to the output voltage $\hat{v}_O(s)$

$$G_{vd}(s) = \frac{\hat{v}_O(s)}{\hat{d}(s)}\bigg|_{\hat{v}_g(s)=0} = \frac{V_g}{1 + s\frac{L}{R} + s^2LC} \tag{3.44}$$

By now, the small signal model is established (3.38) and two important transfer functions $G_{vg}(s)$ and $G_{vd}(s)$ are presented. Both are frequently used in the following controller design part.

3.2 Hybrid Modeling and Model Predicative Control

As described in Section 3.1, the conventional analysis for switching circuits such as DC-DC converters depends on averaging approaches involving considerable approximation, thus hindering the achievement of higher performance. Recently, with the development of advanced

control techniques and the increased computational power provided by the available hardware, analysis and synthesis of power converters in a new perspective is possible. Owing to the existence of switching actions, power converters are hybrid systems in nature. More specifically, these converters feature different modes of operation depending on the action of the switches, which can be seen as discrete states, where each mode has an associated continuous dynamics. Hence more precise modeling technique along with corresponding advanced control methods are needed to achieve higher performance. Motivated by the aforementioned difficulties, the hybrid modeling theory and model predictive control are employed to improve the design of the buck controller.

The term *"hybrid system"* refers to different meanings, among which is the follow: a dynamical system that contains continuous dynamics and discrete events. It should be stressed that the two kinds of dynamics not only coexist but also interact. A majority of dynamic systems in practice are inherently hybrid, e.g., stepper motors, constrained robotic systems, just to name a few. However, most research on dynamic modeling treats these systems from either continuous or discrete perspective. In recent year, some research from the angle of hybrid systems has emerged [124, 125, 126]. In [124], the general theory of hybrid systems is well-introduced. The following contents on hybrid modeling is based on [124]. For clarity, rather than demonstrating the hybrid model directly, we start from the well-known continuous model (ODEs), then add discrete phenomena using hybrid automaton theory [127, 128].

3.2.0.1 Continuous-time State-space Model

The basic continuous-time systems can be defined by the solutions of ordinary differential equations (ODEs) in the state-space form.

$$\dot{x}(t) = f(x(t)) \tag{3.45}$$

where $x(t) \in X$, and $X \subset \mathbf{R}^n$ is a continuous state-space.

The function $f : X \to \mathbf{R}^n$ is a vector field on $\mathbf{R}^n$, and the existence and uniqueness of solutions is assumed. The systems depicted by (3.45) is the so-called autonomous system because the dynamic behavior does not depend on time and no input and output exists. More generally, a state-space model with the input and the output [104][129] is given by

$$\dot{x}(t) = f(x(t), u(t), t) \tag{3.46}$$

$$y(t) = h(x(t), u(t), t) \tag{3.47}$$

where $x(t) \in X \subset \mathbf{R}^n$, $u(t) \in U \subset \mathbf{R}^m$, $y(t) \in Y \subset \mathbf{R}^p$,$f : \mathbf{R}^n \times \mathbf{R}^m \to \mathbf{R}^n$ and $h : \mathbf{R}^n \times \mathbf{R}^m \to \mathbf{R}^p$. $u(\cdot)$ and $y(\cdot)$ are the input and the output, respectively.

3.2.0.2 Adding Discrete Phenomena

As hybrid systems can be regarded as a combination of continuous dynamics and discrete transients, the main challenge is how to precisely specify the interaction between these continuous and discrete dynamics. Thus hybrid automaton theory is employed and next the standard definition of a finite-state automaton (*finite-state machine, finite automaton*) is given.

Definition 3.1. (Finite automaton) A finite-state automaton is a triple (X, Q, E). $X \subset \mathbf{R}^n$ is the finite continuous state-space, $Q = q_1, \ldots, q_m$ is a finite set called the *alphabet*; the elements in Q are called symbols which denote the discrete states of the hybrid system. E is the subset of $X \times Q \times X$ called *transition strategy* and its elements are called *events*. A sequence $(q_0, q_1, \ldots, q_{m-1})$ with $(q_i, q_{i+1}) \in E$ for $i = 1, 2, \ldots, m$ is called a path or trajectory.

Therefore, the model of the hybrid system can be obtained by introducing the finite automaton into (3.46) (3.47) and can be expressed as

$$\dot{x}(t) = f_q(x(t), u(t), t) \tag{3.48}$$

$$y(t) = h_q(x(t), u(t), t) \tag{3.49}$$

where $q \in Q$.

Define $I_q \subset X$ as the subset of the continuous state-space X, then $f_q(\cdot)$ and $h_q(\cdot)$ are functions defined on the corresponding continuous sub-state-spaces I_q depending on the discrete state q. The common approach to depict the finite-state automaton is by a graph called *state*

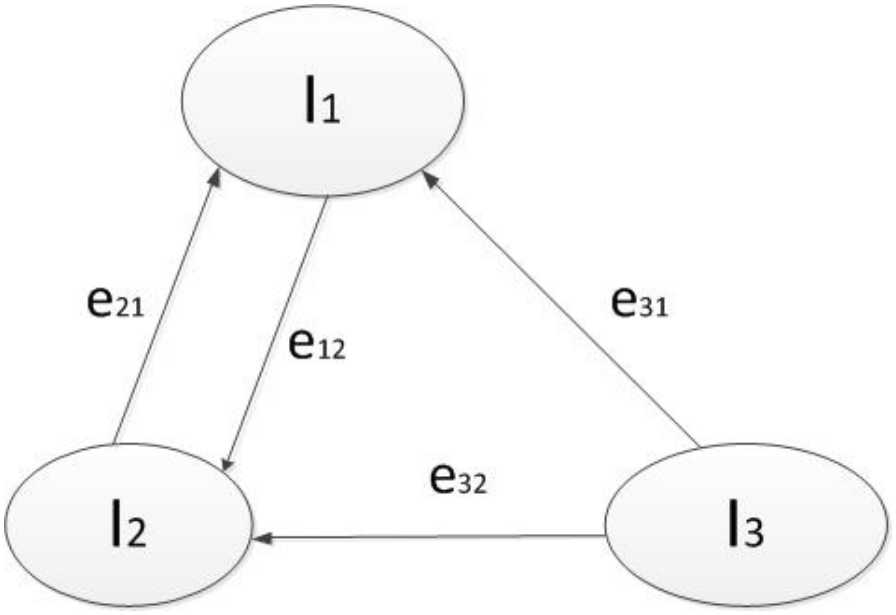


Figure 3.6: State diagram of hybrid system ($q = 1, 2, 3$)

diagram. Here a similar diagram is used to describe the hybrid model as seen in Figure 3.6. The

circular areas denote different continuous sub-state-spaces, and arrows with symbols denote the transitions or discrete states between these sub-state-spaces.

The hybrid modelling theory presented here will be employed to obtain the hybrid model of the DC-DC buck converter in following sections.

3.2.1 Model Predictive Control

Model predictive control (MPC) is one of the advanced control methodologies which has made a significant impact on control engineering. Given the limitation of computation power, for decades, it was only used in slow processes, for example, in the process industry [130]. In recent years, that has seen an incredible development of the modern computing hardware, the speed of solving a convex optimization problem——which is crucial to model predictive control——has been increased by a factor of 10^6 [131]. As a consequence, model predictive control has been employed as a powerful tool by researchers from different fields like power electronics which requires fast and simple control strategies [4, 132].

Model predictive control is based on a dynamic model of the process and the current measurement of the system state. The future values of output variables are predicted in a finite horizon according to the model. The optimal control strategy for next prediction period is obtained by solving a optimal problem on a so-called "cost function". The key point of model predictive control is the "receding horizon" idea that should be discussed in details.

The basic idea of a "receding horizon" can be depicted by Figure 3.7. We assume the process has a discrete-time setting, and that the current time is labelled as k. At time k, the future horizon is $(k \rightarrow k+p)$. The red line is the reference trajectory and the goal is to drive the output variable following the reference trajectory. The output variable during future horizon $(k \rightarrow k+p)$ is predicted based on the current state dynamic model, the past value of the output and assumed control actions which could have different choices. Then by solving the optimal problem on a cost function which considers about all the constraints and minimizes the output error, an optimal control input series can be obtained during the horizon like $u(k), u(k+1), \ldots, u(k+p)$. However, it should be mentioned that only the first element of the predicted control input series $u(k)$ is implemented. Then the horizon moves for a step and all the calculations are repleaded starting from the updated horizon, yielding a new control input series and a new predicted output trajectory. The horizon keeps receding forward so the key point of predictive control is called "receding horizon method".

3.2.2 Hybrid Modeling of the DC-DC Buck Converter

In this section, a hybrid model of the DC-DC buck converter is developed. Unlike the modeling techniques introduced in Chapter 3.1, the hybrid model takes the exact dynamic behavior into

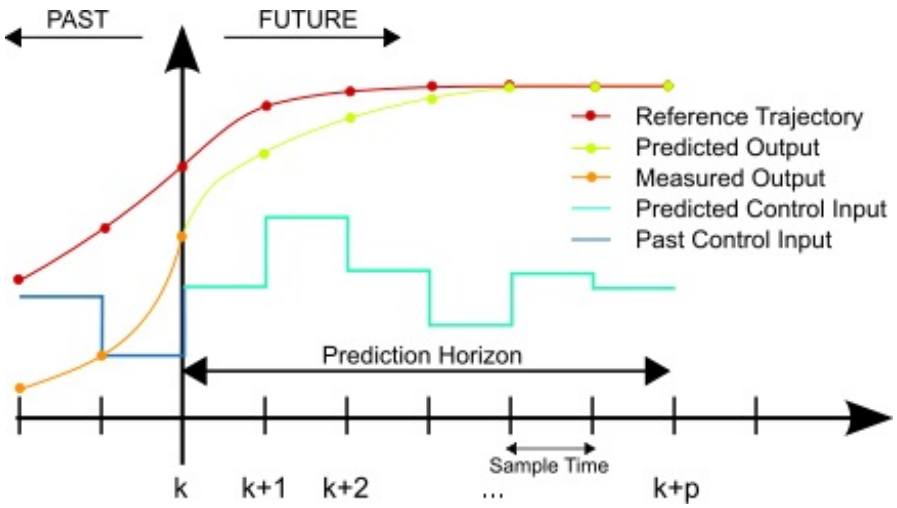


Figure 3.7: Receding horizon idea (*image from wikipedia—licensed under the Creative Commons Attribution-Share Alike 3.0 Unported*)

consideration, without any approximation.

The circuit topology of the DC-DC buck converter is shown in Figure 3.8. The state of the system is defined as $x = [i_L, v_C]^T$ where i_L is the inductance current and v_C is the output voltage, which is equal to the capacitor voltage. Both of the state variables can be easily measured in practice. The converter features two operation modes or two discrete states due to the switching action of S_w : the ON mode and the Off mode which are symbolled as q_1 and q_2, respectively. Thus, according to the hybrid modelling theory presented above, $Q = q_1, q_2$ and $E = (q_1, q_2), (q_2, q_1)$. The state equations of each mode are described by affine continuous-time state-space equation as follow

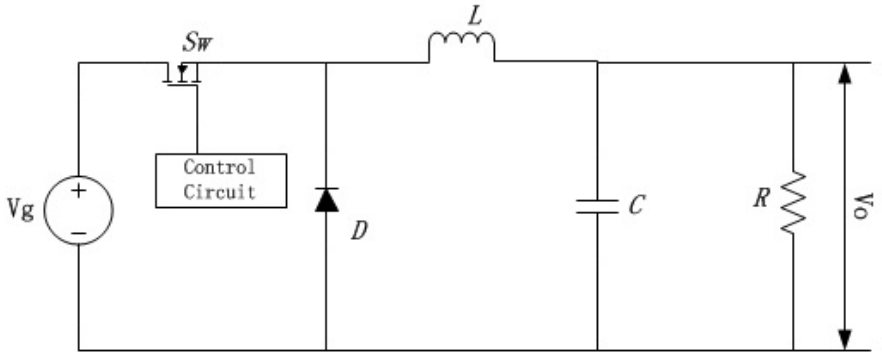


Figure 3.8: A buck converter topology

$$\dot{x}(t) = A_{q_1} x(t) + B_{q_1} u(t) \tag{3.50}$$

$$\dot{x}(t) = A_{q_2} x(t) + B_{q_2} u(t) \tag{3.51}$$

where

$$\begin{aligned} A_{q_1} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\ A_{q_2} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\ B_{q_1} &= \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \\ B_{q_2} &= \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{aligned} \tag{3.52}$$

Then, the output voltage across the load is defined as $y = [v_o]$

$$y = Cx \tag{3.53}$$

where

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{3.54}$$

Motivated by [133], a similar method is used to build up an interactional hybrid automaton system H with two finite-state automaton H_1 and H_2 as shown in Figure 3.9. H_1 governs the discrete transition which depends on the continuous signal from H_2 and generate the gate signal G transmitting to H_2. H_2 governs the continuous evolution according to the gate signal accepting from H_1. The behavior of H_2 is simple: when $G = 1$, turn to state q_1; when $G = 0$, turn to state q_2. The key challenge left to the control scheme design is the transition strategy of H_1 which will be discussed in the following sections.

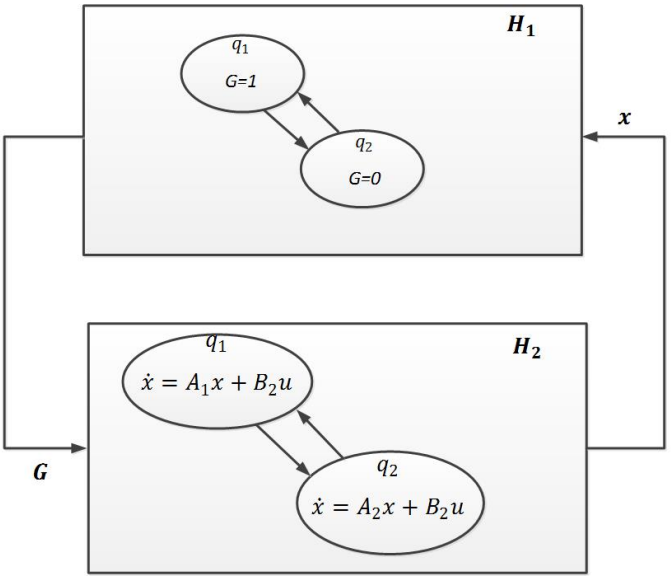


Figure 3.9: Hybrid automaton of the DC-DC buck converter

3.2.3 Modeling for Controller Design

In order to implement the model predictive control, a predictive model is needed. Thus in this section, the hybrid model obtained above is transformed to a discrete-time predictive model.

The general solution of state variable in (3.50) (3.51) can be derived from the state equation

$$x(t) = \phi(t-t_0)x_{t_0} + \int_{t_0}^{t} \phi(t-\tau)Bu(\tau)d\tau \tag{3.55}$$

where

$$\phi(t-t_0) = e^{A_{q_1}(t-t_0)} \tag{3.56}$$

or

$$\phi(t-t_0) = e^{A_{q_2}(t-t_0)} \tag{3.57}$$

We define the sample time as T_s, and consider the time interval $[kT_s \rightarrow (k+1)T_s]$. Hence $t_0 = kT_s$ and $t = (k+1)T_s$. (3.55) can be rewritten as:

$$x((k+1)T_s) = \phi(T_s)x(kT_s) + \int_{kT_s}^{(k+1)T_s} \phi((k+1)T_s - \tau)Bu(\tau)d\tau \tag{3.58}$$

As long as the sample time is small enough, it could be assumed that input signal $u(t)$ keep constant during the sample interval. For simplicity of notation, we will use k for kT_s. Let $t = (k+1)T - \tau$, one obtains:

$$x((k+1)T_s) = \phi(T_s)x(kT_s) + \int_{0}^{T_s} \phi(t)dtBu(kT) \tag{3.59}$$

From the view of implementation, one problem for (3.59) is how to calculate $\phi(T_s)$ and $\int_0^{T_s} \phi(t)dt$ which are exponential functions. From [134], we know that the exponential function can be approximated by the first two terms of its Taylor series. Hence, (3.56)(3.57) can be approximated as

$$\phi(T_s) = e^{A_{q_1}T_s} / \left(e^{A_{q_2}T_s}\right) \approx I + A_{q_1}T_s / \left(I + A_{q_2}T_s\right) \tag{3.60}$$

Substituting (3.60) into (3.59), the predictive model can be obtained.

$$x(k+1) = G_{q_1}x(k) + H_{q_1}u(k) \tag{3.61}$$

$$x(k+1) = G_{q_2}x(k) + H_{q_2}u(k) \tag{3.62}$$

where

$$\begin{aligned} G_{q_1} &= \begin{bmatrix} 1 & -\frac{T_s}{L} \\ \frac{T_s}{C} & 1-\frac{T_s}{RC} \end{bmatrix} \\ G_{q_2} &= \begin{bmatrix} 1 & -\frac{T_s}{L} \\ \frac{T_s}{C} & 1-\frac{T_s}{RC} \end{bmatrix} \\ H_{q_1} &= \begin{bmatrix} \frac{T_s}{L} \\ 0 \end{bmatrix} \\ H_{q_2} &= \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{aligned} \tag{3.63}$$

The predictive output equation is given as

$$y(k+1) = Cx(k+1) \tag{3.64}$$

3.2.4 Model Predictive Controller Design

In this section, a model predictive controller is designed based on the predictive model development above (3.61)(3.62) and (3.64).

For the buck converter, the aim of the controller design is to let the output voltage v_o follow a reference voltage v_{ref}. Motivated by [6], a short horizon MPC strategy is adopted. We set the horizon as two sample interval. According to the predictive model (3.61)(3.62) and (3.64), the predictive equation of the output voltage in two horizon can be obtained

$$v_o(k+2) = \frac{T_s}{C}\left[i_l(k) - \frac{T_s}{L}v_o(k) + \Gamma\frac{T_s}{L}v_g(k)\right] + \left(1-\frac{T_s}{RC}\right)\left[\frac{T_s}{C}i(k) + \left(1-\frac{T_s}{RC}\right)v_o(k)\right] \tag{3.65}$$

where

$$\Gamma = \begin{cases} 1 & ON \\ 0 & OFF \end{cases} \tag{3.66}$$

That is: at the current time k, the inductance current $i_l(k)$, the output voltage $v_o(k)$ and the input voltage $v_g(k)$ are measured. The output voltage at time $k+2$ is predicted. Now we introduce the cost function J.

$$J = |v_o - v_{ref}| \tag{3.67}$$

For every step, the cost function of each mode can be calculated i.e. J_{q_1} and J_{q_2}. The mode that can minimize the cost function is selected to implement in next sample time. Hence, the flow diagram of the implemented control algorithm is given in Figure 3.10.

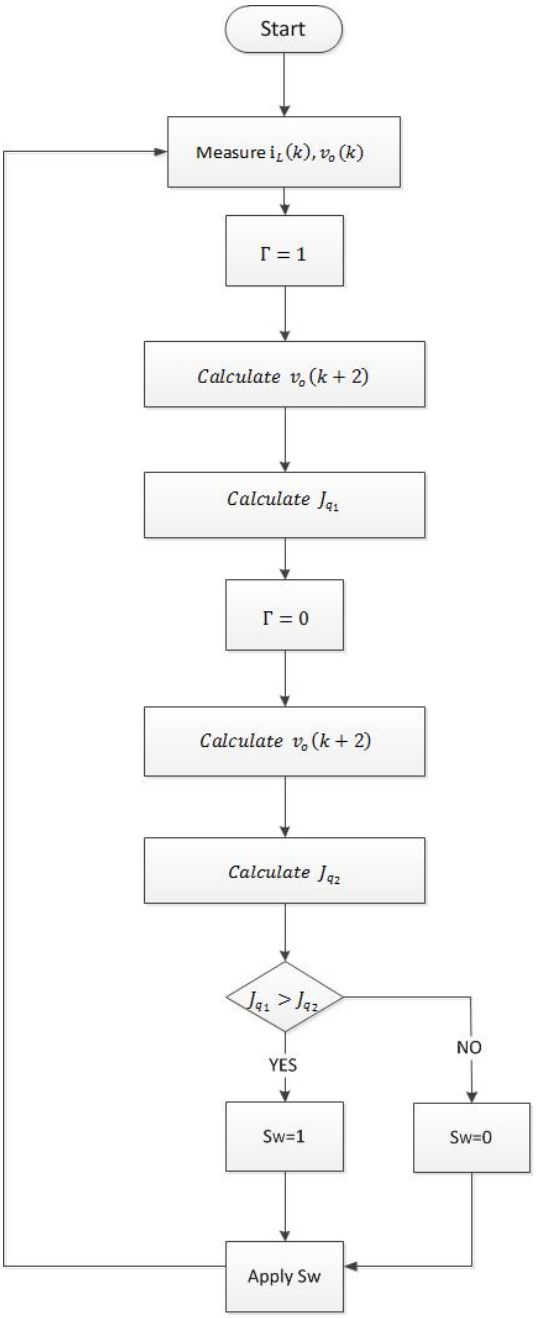


Figure 3.10: Flow diagram of the implemented control algorithm

3.3 Summary

In this Chapter, two mainstream modelling and control scheme, which are linear control design based on state-space averaged model and model predicative control based on hybrid model, have been reviewed in details. These two methods will act as benchmarks for the following chapters and give a clear comparison with the new modelling and control methods proposed in this thesis.

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Chapter 4

Sampled-Data Control with Adjustable Switching Frequency

4.1 Hybrid Modelling in State-Space

In this section, a unified hybrid model is proposed for no-transformer non-isolated DC-DC power electronics converters. We only consider three simplest and most commonly used topologies, that is, Buck, Boost, and Buck-Boost as shown in Figure 4.1, since more complex DC-DC converters, such as Ćuk, Sepic, and Zeta converters, can be treated as the combination of these basic topologies [135].

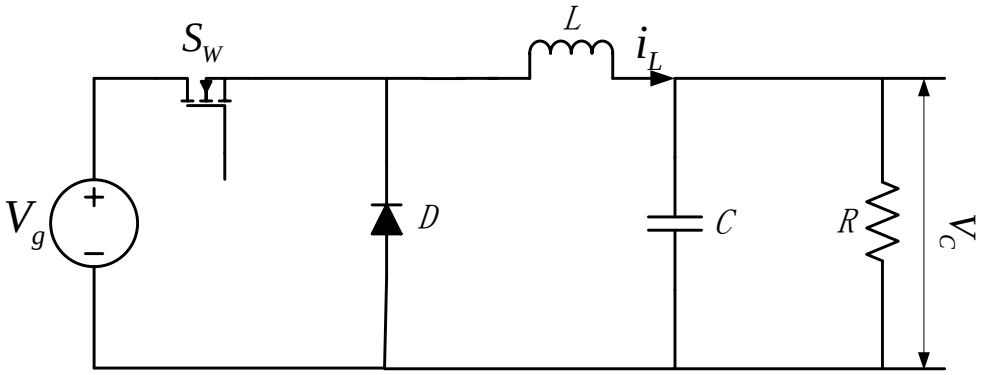
For all the topologies: V_g is the source DC voltage; L is the inductance of a inductor; C is the capacitance of a capacitor; and R represents load resistance. The current through the inductors and the voltage across the capacitors are indicated in Figure 4.1. The voltage across the resistive load is to be regulated.

The principle of operations for these three converters is to control the status of the transistor (S_W) such that a source of direct current (DC) can be converted from one voltage level to another. In term of the position of the switch S_w, all these DC-DC converters have two switching states: the ON state and the OFF state. For each switching state, the continuous dynamics of the converter can be described by a state-space model:

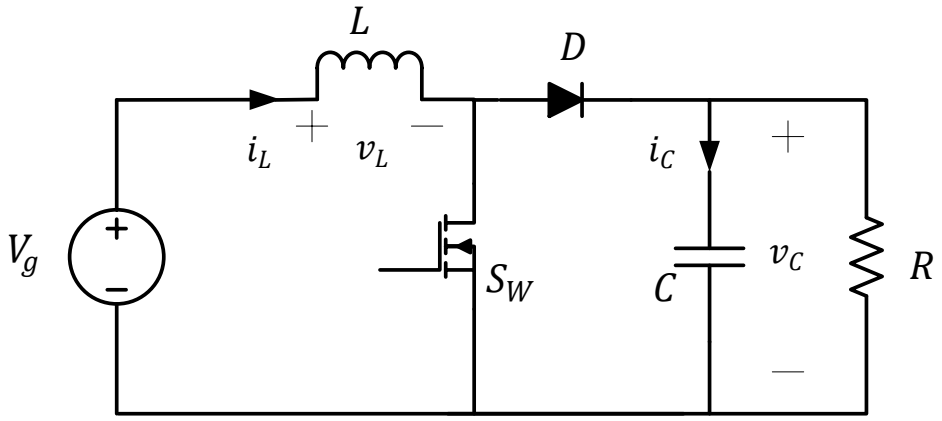
$$\dot{x}(t) = A_\sigma x(t) + B_\sigma,\ \sigma \in \Xi \triangleq \{1,2\} \tag{4.1}$$

with the system states $x(t) = [i_L, v_C]^T \in \mathbb{R}^2$ for buck, boost, buck-boost converters. (A_1, B_1) and (A_2, B_2) are the system matrices for the ON state and OFF state respectively, which are given in Table 4.1.

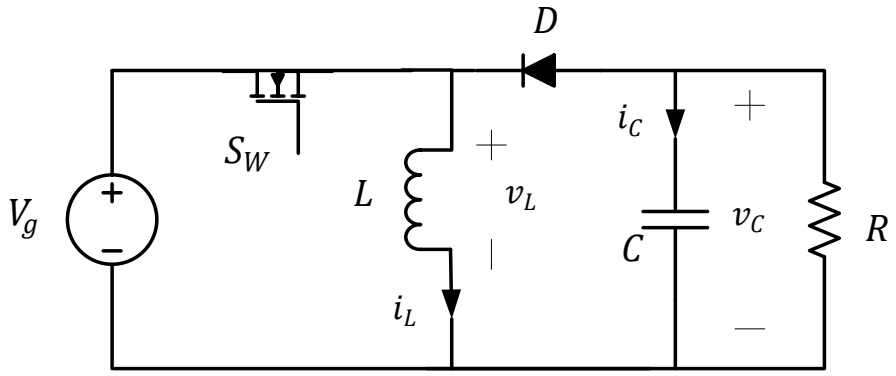
Due to the complementary operation of the transistor S_W, the evolution of the system state



(a) Buck Converter



(b) Boost Converter



(c) Buck-Boost Converter

Figure 4.1: Topologies for different DC-DC Converters

is determined by the continuous dynamics together with the status of the switch ($\sigma = 1$ or 2). Hence, a unified switched model (4.1) with two subsystems is proposed for the three DC-DC converters of interest. It is stressed here that although similar models have been used for the simulation of DC-DC converters, control design, particularly sampled-data control, based on the switched model remains rare.

Table 4.1: State matrices of switched model for different topologies.

Topologies	A_i	B_i
Buck Converter	$A_1 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$	$B_1 = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$
	$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$	$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$
Boost Converter	$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$	$B_1 = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$
	$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$	$B_2 = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$
Buck-Boost Converter	$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$	$B_1 = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$
	$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$	$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$

From the standpoint of control theory, the system in 4.1 has a discontinuous vector field and thus classic equilibrium solution is no longer applicable. However, our goal is to regulate the output voltage to some reference points, which are some sorts of "equilibria". To solve this issue, we employ the so-called Filippov solutions to obtain the attainable reference points [136]. The basic idea is to replace the right-hand side of 4.1 with a differential inclusion, that is,

$$\dot{x}(t) = A(\lambda)x(t) + B(\lambda), \tag{4.2}$$

where

$$\begin{aligned} A(\lambda) =& \lambda A_1 + (1-\lambda)A_2 \\ B(\lambda) =& \lambda B_1 + (1-\lambda)B_2 \\ \lambda \in& [0,1] \end{aligned}$$

With this "averaged" system, the attainable equilibrium can be obtained as

$$x_e = -A^{-1}(\lambda)B(\lambda),\ \lambda \in [0,1]. \tag{4.3}$$

An interesting finding is that the Filippov equilibrium in 4.3 is equal to the equilibrium obtained by using classic approaches, and the parameter λ is equal to classic duty ratio. Despite the similarity in the steady state, we manipulate the power switch directly instead of controlling the duty ratio as often used in classic control approaches.

4.2 Sampled-Data Control Scheme

In this section, a state-feedback switching controller based on the sampled state is proposed. A significant difference between the proposed method and most digital control schemes for DC-DC converters such as DPWM [137] and model predictive control [69] is that: in order to capture more transition information of the converters, the design is based on a continuous-time plant (4.1) with full-time information rather than a discrete-time model that neglects the inter-sample behaviour of the converters.

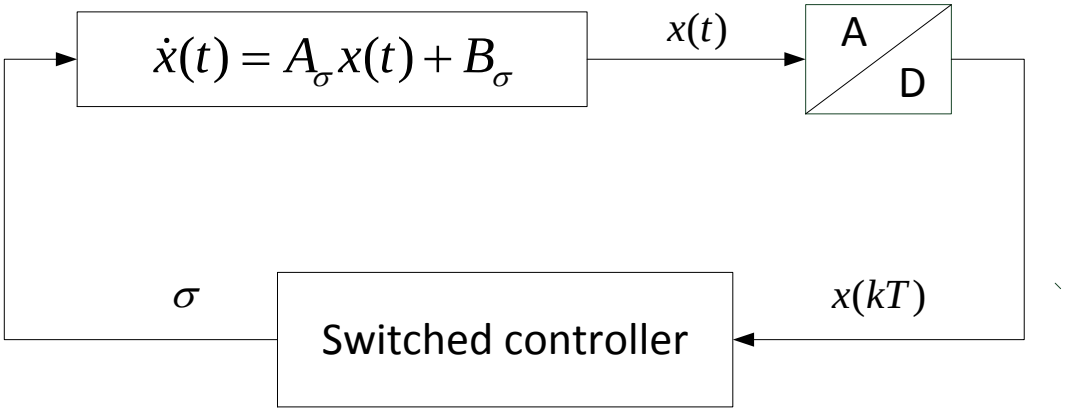


Figure 4.2: General sampled-data control structure for DC-DC buck converters.

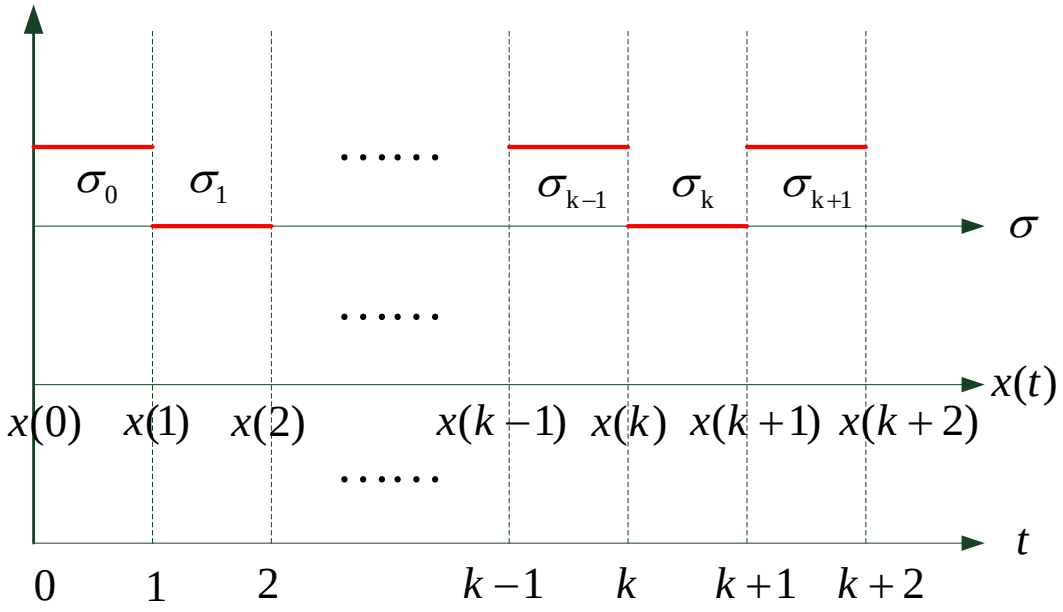


Figure 4.3: The time relationship among different variables.

The general structure of the proposed sampled-data control scheme is depicted in Figure 4.2. The system state is sampled as $x(kT)$, where T is the sampling period and $k =$

$0,1,2,3\cdots$. For notational simplicity, k stands for kT in the remaining part. Before proceeding, the following assumptions are presented:

1. Define switching signal $\sigma(x(k)):\mathbb{R}^2\rightarrow\Xi=\{1,2\}$ as a piecewise constant function, mapping the full state-space $\mathbb{R}^2$ to the available switching signal set Ξ.
2. The switching signal $\sigma(x(0))$ needs to be initialized manually based on the initial condition of the DC-DC converters.
3. The switching signal $\sigma(x(k))$ is updated at the start of the sampling instants kT and keeps constant during the whole sampling period $[k,k+1)$ as shown in Figure 4.3.

Based on these assumptions, a closed-stability guaranteed switching controller (i.e. the switching signal function $\sigma(x(k))$ is designed off-line.

4.2.1 Off-line Design of Switching Controller

A state-feedback switching control law $\sigma(*)$ is proposed as

$$\sigma(x(k))=\arg\min_{(i,j)\in\Xi\times\Xi}\{2w_1\left((x(k)-x_e)^TP_j(A_ix(k)+B_i)\right)+2w_2|i-\sigma(x(k-1))|\},\qquad(4.4)$$

where $x_e=[i_e,v_e]^T$ is the reference point obtained by 4.3; $\Xi=\{1,2\}$, w_1, w_2 are two positive weighting factors for adjustment of switching frequency; $P_j\in\mathbb{R}^{2\times2}$ are parameter matrices to be determined later. $\left((x(k)-x_e)^TP_j(A_ix(k)+B_i)\right)$ is the derivative of the Lyapunov functional. Hence, the switching law is to be able to drive the system state along the fastest converging direction which guarantees the system stability. The second part of the switching law $|i-\sigma(x(k-1))|$ is adopted to adjust the switching frequency which will be explained later. The following theorem states that under some conditions the proposed switching control law will drive the system to the neighborhood of the desirable reference points.

Firstly, a technical lemma which will be used in the following part is presented.

Lemma 4.1. *(Jensen's inequality)[138] Given a positive definite matrix Q,*

$$\int_{t_0}^{t}\dot{x}^T(s)Q\dot{x}(s)ds\geq(t-t_0)v^T(t)Qv(t)\qquad(4.5)$$

where $v(t)=\frac{x(t)-x(t_0)}{t-t_0}$.

Theorem 4.2. *For given positive scalars ξ, ρ, ε, β, κ, a Lyapunov-Krasovskii functional candidate is defined as*

$$V(\phi(t),t)=V_1(\phi(t))+V_2(\phi(t),t),\qquad(4.6)$$

where $\phi(t) = x(t) - x_e$, *and*

$$V_1(\phi(t)) = \min_{j\in\Xi}\{\phi^T(t)P_j\phi(t)\} \tag{4.7}$$
$$V_2(\phi(t),t) = (T-\tau)\int_{t-\tau}^{t} e^{\xi(s-t)}\dot{\phi}^T(s)Q_\sigma\dot{\phi}(s)ds \quad \tau = t-t_k,\ t\in[k,k+1).$$

If the following condition is satisfied

$$\dot{V}(\phi(t),t) + \xi V(\phi(t),t) < \rho T + \kappa||x_e||_2 + (\varepsilon+2\beta)\frac{w_2}{w_1},\ \ \forall t\in[k,k+1),. \tag{4.8}$$

then under the switching signal $\sigma(x(k))$ *the state of the DC-DC converters* $x(t)$ *will converge to a finite region* Θ *around the reference point* x_e, *where*

$$\Theta \triangleq \{x(t)\in\mathbb{R}^2 : \min_{j\in\Xi}\{eig_{min}(P_j)\}||x-x_e||_2 \le \frac{T\rho+\kappa||x_e||^2}{\xi} + \frac{\varepsilon+2\beta}{\xi}\frac{w_2}{w_1}\}, \tag{4.9}$$

Proof. We note from the min property of $V_1(\phi(t))$ that at the switching instant k,

$$V_1(\phi(k),t_k^+) = \phi^T(k)P_{j(\sigma_k)}\phi(k) \le \phi^T(k)P_{j(\sigma_{k-1})}\phi(k) = V_1(\phi(k),t_k^-) \tag{4.10}$$

which means that the Lyapunov functional $V_1(e(t))$ does not grow after each switching instant. By using the comparison principle, we have that if (4.8) holds, then

$$\begin{aligned} V_1(\phi(t),t) &\le e^{-\xi(t-t_k)}V_1(\phi(k),t_k^+) + \theta\int_{t_k}^{t_{k+1}} e^{-\xi(t-s)}ds \\ &\le e^{-\xi(t-t_{k-1})}V_1(\phi(k-1),t_{k-1}^+) + \theta\int_{t_{k-1}}^{t} e^{-\xi(t-s)}ds \\ &\le \ldots \le e^{-\xi t}V_1(\phi(0),0) + \theta\int_0^t e^{-\xi(t-s)}ds, \end{aligned}$$

where

$$\theta = \rho T + \kappa||x_e||_2 + (\varepsilon+2\beta)\frac{w_2}{w_1},$$

which means that for $t\to\infty$, $x(t)$ exponentially converges to the region Θ. □

Therefore, if the system is practically stable under the proposed switching signal $\sigma(x(k))$, the inductor current i_L and capacitor voltage v_C will be stabilized around the desired DC steady state i_e and v_e respectively with bounded ripple. Furthermore, The boundary of the current ripple and voltage ripple are defined by the region Θ.

Remark 4.3. The minimum function $V_1(\phi(t))$ ensures that the abstract energy associate with the system will not increase at the switching instant. To guarantee that the energy will decrease along the trajectory of the system, it suffices to require that the Lypuanov function does not increase during the sampling interval $[k,k+1)$. A discontinuous term $V_2(\phi(t),t)$ is added to achieve this.

We are now in a position to present the main result. The details of how to solve the unknown Lyapunov matrices P_j, with which the practical stability condition (4.8) is satisfied, is demonstrated in the form of Bilinear Matrix Inequalities (BMIs).

Theorem 4.4. *Consider the switched model* (4.1) *with sampling period* T *and given parameters* $\xi > 0$, $\rho > 0$, $\varepsilon > 0$, $\kappa > 0$, $w_1 > 0$, $w_2 \geq 0$, *for a specific reference point* x_e *with corresponding* $\lambda \in [0,1]$, *if there exist matrices* $P_j > 0$, $Q_i > 0$, *scalars* $\beta > 0$, $\mu_{jr} > 0$, *for* $\forall (i,j) \in \Xi \times \Xi$, $r \in \Xi$ *such that*

$$\Psi(0,0,\lambda) < 0, \tag{4.11}$$

$$\Psi(T,T^2,\lambda) < 0, \tag{4.12}$$

where

$$\Psi(\tau,\tau^2,\lambda) = \Pi(\tau) + \beta(\Omega(\tau,\tau^2) + \Omega(\tau,\tau^2,\lambda)) - \sum_{r}^{\Xi} \mu_{jr} \Upsilon_j(\tau,\tau^2), \tag{4.13}$$

$$\Pi(\tau) = \begin{bmatrix} \Pi(\tau)_{11} & \Pi(\tau)_{12} & 0 & \Pi(\tau)_{14} \\ * & \Pi(\tau)_{22} & 0 & \Pi(\tau)_{24} \\ * & * & -\tau Q_i e^{-\xi T} & 0 \\ * & * & * & \Pi(\tau)_{44} \end{bmatrix},$$

$$\begin{aligned}
\Pi(\tau)_{11} &= A_i^T P_j + P_j A_i + \xi P_j + (T-\tau) A_i^T Q_i A_i, \\
\Pi(\tau)_{12} &= (T-\tau) A_i^T Q_i A_i + P_j A_i, \\
\Pi(\tau)_{14} &= (T-\tau) A_i^T Q_i B_i + P_j B_i, \\
\Pi(\tau)_{22} &= (T-\tau) A_i^T Q_i A_i - \kappa, \\
\Pi(\tau)_{24} &= (T-\tau) A_i^T Q_i B_i, \\
\Pi(\tau)_{44} &= (T-\tau) B_i^T Q_i B_i - \rho T - (\varepsilon + 2\beta) \frac{w_2}{w_1},
\end{aligned}$$

$$\Omega(\tau,\tau^2)=\begin{bmatrix} -A_i^TP_j-P_jA_i & -P_iA_i & \tau(A_i^TP_j+P_jA_i) & -P_jB_i \\ * & 0 & \tau A_i^TP_j & 0 \\ * & * & -\tau^2(A_i^TP_j+P_jA_i) & \tau P_iB_i \\ * & * & * & 2\frac{w_2}{w_1}\boldsymbol{I} \end{bmatrix},$$

$$\Omega(\tau,\tau^2,\lambda)=\begin{bmatrix} A^T(\lambda)P_j+P_jA(\lambda) & 0 & -\tau(A^T(\lambda)P_j+P_jA(\lambda)) & 0 \\ * & 0 & 0 & 0 \\ * & * & \tau^2(A^T(\lambda)P_j+P_jA(\lambda)) & 0 \\ * & * & * & 0 \end{bmatrix},$$

$$\Upsilon_j(\tau,\tau^2)=\begin{bmatrix} P_j-P_r & 0 & -\tau(P_j-P_r) & 0 \\ * & 0 & 0 & 0 \\ * & * & \tau^2(P_j-P_r) & 0 \\ * & * & * & 0 \end{bmatrix},$$

the condition (4.8) *is fulfilled. Then the DC-DC converter is practically stabilizable to the region* Θ *around the desired reference point* x_e *under the switching signal* (4.4).

Proof. Without loss of generality, we assume that at time k, $\sigma(x(k))=i$, and $V_1(\phi(k))=\min\limits_{j\in\Xi}\{\phi(k)^TP_j\phi(k)\}=\phi(k)^TP_j\phi(k)$.

Then along the solution of (4.1), the derivative of the chosen Lyapunov functional (4.7) can be calculated:

$$\begin{aligned}\dot{V}_1&=\min\{\dot{\phi}^T(t)P_j\phi(t)+\phi^T(t)P_j\dot{\phi}(t)\}=\min\{2\phi^T(t)P_j(A_i\phi(t)+A_ix_e+B_i)\}\\&\le\phi^T(t)(A_i^TP_j+P_jA_i)\phi(t)+2\phi(t)P_j(A_ix_e+B_i).\end{aligned}\tag{4.14}$$

Applying Lemma 4.1 yields,

$$\dot{V}_2+\xi V_2\le(T-\tau)(A_i\phi(t)+A_ix_e+B_i)^TQ_i(A_i\phi(t)+A_ix_e+B_i)-\tau v^T(t)Q_iv(t)e^{-\xi T},\tag{4.15}$$

where $v(t)=\frac{\phi(t)-\phi(t_k)}{\tau}$, $\tau=t-t_k$.

Define $\eta(t)=\begin{bmatrix}\phi(t) & x_e & v(t) & 1\end{bmatrix}^T$, the condition (4.8) holds if

$$\eta^T(t)\,\Pi(\tau)\,\eta(t)<0,\tag{4.16}$$

where

$$\Pi(\tau)=\begin{bmatrix} \Pi(\tau)_{11} & \Pi(\tau)_{12} & 0 & \Pi(\tau)_{14} \\ * & \Pi(\tau)_{22} & 0 & \Pi(\tau)_{24} \\ * & * & -\tau Q_ie^{-\xi T} & 0 \\ * & * & * & \Pi(\tau)_{44} \end{bmatrix},$$

$$\begin{aligned}
\Pi(\tau)_{11} &= A_i^T P_j + P_j A_i + \xi P_j + (T-\tau) A_i^T Q_i A_i, \\
\Pi(\tau)_{12} &= (T-\tau) A_i^T Q_i A_i + P_j A_i, \\
\Pi(\tau)_{14} &= (T-\tau) A_i^T Q_i B_i + P_j B_i, \\
\Pi(\tau)_{22} &= (T-\tau) A_i^T Q_i A_i - \kappa, \\
\Pi(\tau)_{24} &= (T-\tau) A_i^T Q_i B_i, \\
\Pi(\tau)_{44} &= (T-\tau) B_i^T Q_i B_i - \rho T - (\varepsilon + 2\beta)\frac{w_2}{w_1}.
\end{aligned}$$

Based on the proposed switching signal function (4.4), for $\forall l \in \Xi$, the following inequality holds:

$$\begin{aligned}
&2w_1\phi(k)^T P_j(A_l\phi(k) + A_l x_e + B_l) + 2w_2|l-\sigma_{k-1}| \geq \\
&\quad 2w_1\phi(k)^T P_j(A_i\phi(k) + A_i x_e + B_i) + 2w_2|i-\sigma_{k-1}|.
\end{aligned} \tag{4.17}$$

Rearranging the inequality yields,

$$\begin{aligned}
&2w_1\phi(k)^T P_j(A_l\phi(k) + A_l x_e + B_l) + 2\frac{w_2}{w_1}(|l-\sigma_{k-1}| - |i-\sigma_{k-1}|) \geq \\
&\quad 2w_1\phi(k)^T P_j(A_i\phi(k) + A_i x_e + B_i).
\end{aligned} \tag{4.18}$$

Since $-1 \leq |l-\sigma_{k-1}| - |i-\sigma_{k-1}| \leq 1$, $\forall l \in \Xi$, if (4.18) holds, the following inequality holds:

$$2w_1\phi(k)^T P_j(A_l\phi(k) + A_l x_e + B_l) + 2\frac{w_2}{w_1} \geq 2w_1\phi(k)^T P_j(A_i\phi(k) + A_i x_e + B_i). \tag{4.19}$$

When $l = 1$, multiplying the inequality (4.19) by λ yields,

$$2w_1\phi(k)^T P_j(\lambda A_1\phi(k) + \lambda A_1 x_e + \lambda B_1) + 2\frac{w_2}{w_1} \geq 2w_1\phi(k)^T P_j(\lambda A_i\phi(k) + \lambda A_i x_e + \lambda B_i). \tag{4.20}$$

When $l = 2$, multiplying the inequality (4.19) by $(1-\lambda)$ yields,

$$\begin{aligned}
&2w_1\phi(k)^T P_j((1-\lambda)A_2\phi(k) + (1-\lambda)A_2 x_e + (1-\lambda)B_2) + 2\frac{w_2}{w_1} \\
&\quad \geq 2w_1\phi(k)^T P_j((1-\lambda)A_i\phi(k) + (1-\lambda)A_i x_e + (1-\lambda)B_i).
\end{aligned} \tag{4.21}$$

Summing up (4.20) and (4.21), the following inequality holds:

$$2\phi^T(k)P_j(A(\lambda) - A_i)\phi(k) - 2\phi^T(k)P_j(A_i x_e + B_i) + 2\frac{w_2}{w_1} \geq 0, \tag{4.22}$$

where the relations $A(\lambda) = \lambda A_1 + (1-\lambda)A_2$, $B(\lambda) = \lambda B_1 + (1-\lambda)B_2$, and $A(\lambda)x_e + B(\lambda) = 0$ are used.

For $\phi(k) = \phi(t) - \tau v(t)$, and using the same variable $\eta(t)$, the above inequality becomes:

$$\eta^T(t)(\Omega(\tau,\tau^2) + \Omega(\tau,\tau^2,\lambda))\eta(t) \geq 0 \tag{4.23}$$

where

$$\Omega(\tau,\tau^2) = \begin{bmatrix} -A_i^T P_j - P_j A_i & -P_i A_i & \tau(A_i^T P_j + P_j A_i) & -P_j B_i \\ * & 0 & \tau A_i^T P_j & 0 \\ * & * & -\tau^2(A_i^T P_j + P_j A_i) & \tau P_i B_i \\ * & * & * & 2\frac{w_2}{w_1}\mathbf{I} \end{bmatrix}, \tag{4.24}$$

$$\Omega(\tau,\tau^2,\lambda) = \begin{bmatrix} A^T(\lambda)P_j + P_j A(\lambda) & 0 & -\tau(A^T(\lambda)P_j + P_j A(\lambda)) & 0 \\ * & 0 & 0 & 0 \\ * & * & \tau^2(A^T(\lambda)P_j + P_j A(\lambda)) & 0 \\ * & * & * & 0 \end{bmatrix}. \tag{4.25}$$

Another assumption $V_1(\phi(k)) = \min_{j\in\Xi}\{\phi(k)^T P_j \phi(k)\} = \phi(k)^T P_j \phi(k)$ is satisfied only if

$$\phi^T(k) P_j \phi(k) \leq \phi^T(k) P_r \phi(k),\ \forall r \in \Xi \tag{4.26}$$

Using the expression $\phi(k) = \phi(t) - \tau v(t)$ and the same variable $\eta(t)$, the above inequality becomes:

$$\eta^T(t)\ \Upsilon_j(\tau,\tau^2)\ \eta(t) \leq 0 \tag{4.27}$$

where

$$\Upsilon_j(\tau,\tau^2) = \begin{bmatrix} P_j - P_r & 0 & -\tau(P_j - P_r) & 0 \\ * & 0 & 0 & 0 \\ * & * & \tau^2(P_j - P_r) & 0 \\ * & * & * & 0 \end{bmatrix}$$

Therefore, (4.8) holds if (4.16) holds in the condition of (4.23), (4.27), that is,

$$\eta^T(t)\ \Pi(\tau)\ \eta(t) < 0$$

$$\begin{aligned} s.t.\ & \eta^T(t)\left(\Omega(\tau,\tau^2) + \Omega(\tau,\tau^2,\lambda)\right)\eta(t) \geq 0 \\ & \eta^T(t)\ \Upsilon_j(\tau,\tau^2)\ \eta(t) \leq 0 \\ & \forall (i,j) \in \Xi \times \Xi \end{aligned}$$

Applying the S-procedure, the above condition holds if

$$\eta^T(t)\,\Pi(\tau)\,\eta(t)+\beta\eta^T(t)\left(\Omega(\tau,\tau^2)+\Omega(\tau,\tau^2,\lambda)\right)\eta(t)-\sum_{r}^{\Xi}\mu_{jr}\eta^T(t)\Upsilon_j(\tau,\tau^2)\eta(t)<0 \tag{4.28}$$

$$\exists\beta>0,\ \exists\mu_{jr}>0,\ \forall(i,j)\in\Xi\times\Xi.$$

Rearranging the inequality yields,

$$\Psi(\tau,\tau^2,\lambda)=\Pi(\tau)+\beta(\Omega(\tau,\tau^2)+\Omega(\tau,\tau^2,\lambda))-\sum_{r}^{\Xi}\mu_{jr}\Upsilon_j(\tau,\tau^2)<0 \tag{4.29}$$

Since $\Psi(\tau,\tau^2,\lambda)\in co\{\Psi(0,0,\lambda),\Psi(T,0,\lambda),\Psi(T,T^2,\lambda)\},\forall\tau\in[0,T]$, (4.29) holds if

$$\Psi(0,0,\lambda)<0 \tag{4.30}$$
$$\Psi(T,0,\lambda)<0 \tag{4.31}$$
$$\Psi(T,T^2,\lambda)<0. \tag{4.32}$$

Because (4.32) implies (4.31), the conditions (4.30)–(4.32) are sufficient to guarantee the stability with the proposed switching law.

□

Remark 4.5. The model (4.1) is a continuous-time model with sampling, which is different from normal digital control based on a discrete-time model.

Remark 4.6. The tightness of the region (4.9) is proportional to the sampling period T. Thus, for fixed other parameters, a high sampling frequency will result in a tighter boundary, which means a smaller converter output voltage ripple.

Remark 4.7. The switching signal function $\sigma(x(k))$ is designed off-line, and this will undoubtedly reduce computational burdens. More importantly, closed-loop stability with our method is guaranteed theoretically.

Remark 4.8. The parameters $\xi,\rho,\varepsilon,\kappa,w_1,w_2$ are used to specify the size of the region Θ, and should be given before solving the inequalities. Then by partitioning the scalars $\beta>0$, $\mu_{jr}>0$, the conditions are converted to a set of LMI problems.

It should be mentioned that unlike the traditional PWM control which has a fixed switching frequency, the switching frequency is unfixed for the proposed method. However, the switching signal keeps constant during each sampling cycle. Hence, the average switching frequency of the proposed control scheme is bounded by the sampling frequency which is more applicable than the other similar stability based methods [139] with the assumption of infinite switching frequency in practice. It is obvious that the switching frequency is inversely proportional to

the ripple. Hence, it is crucial to reach a compromise between ripple minimization and switching frequency reduction because over-rapid switching will reduce the energy efficiency of the converter and pose a challenge to thermal management.

In the proposed switching signal function

$$\sigma(x(k)) = \arg \min_{(i,j)\in\Xi\times\Xi} \{2w_1 \left((x(k)-x_e)^T P_j(A_i x(k)+B_i)\right) + 2w_2|i-\sigma(x(k-1)|\},$$

the weighting factors w_1 and w_2 are introduced to adjust the average switching frequency. For the term $|i-\sigma(x(k-1)|$, if i is equal to the previous switching state $\sigma(x(k-1))$, it will be zero; otherwise it will be one. Due to the min property of the switching signal function, it will prevent the change of the switch state if the practical stability can be guaranteed. By this way, some unnecessary switching can be avoided and the switching frequency is reduced.

The region Θ is proportional to the weighing factor w_2 for a fixed w_1. Hence, if w_2 increases, the region become larger which means larger current and voltage ripple. In the meantime, the average switching frequency is decreased. One may argue that the change of the factor w_2 will result in the invalidity of inequalities (4.11) and (4.12). In the following corollary, the practical stability holds when the weighting factor w_2 changes.

Corollary 4.9. *Consider the switched model (4.1) with sampling period T and parameters $\xi > 0$, $\rho > 0$, $\varepsilon > 0$, $\kappa > 0$ for a specific reference point x_e with corresponding $\lambda \in [0,1]$. If there exist matrices $P_j > 0$, $Q_i > 0$, scalars $\beta > 0$, $\mu_{jr} > 0$, for $\forall (i,j) \in \Xi\times\Xi$, $r \in \Xi$ such that*

$$\Psi(0,0,\lambda) < 0, \tag{4.33}$$

$$\Psi(T,T^2,\lambda) < 0, \tag{4.34}$$

with a given $w_1 > 0$ and $w_2 = 0$, then the condition (4.8) is fulfilled and the DC-DC converter is practically stabilizable to the region Θ around the desired reference point x_e under the switching signal

$$\sigma(x(k)) = \arg \min_{(i,j)\in\Xi\times\Xi} \{2w_1 \left((x(k)-x_e)^T P_j(A_i x(k)+B_i)\right) + 2w_2|i-\sigma(x(k-1)|\},$$

with the same $w_1 > 0$ and any $w_2 \geq 0$.

Proof. Continuing with the proof of Theorem 2, the inequality (4.29) can be separated as two parts: one with the weighting factor w_1 and w_2 and the other without.

$$\begin{bmatrix} 0 & 0 & 0 & 0 \\ * & 0 & 0 & 0 \\ * & * & 0 & 0 \\ * & * & * & -\rho T - \varepsilon\frac{w_2}{w_1} \end{bmatrix} + \Delta < 0 \tag{4.35}$$

Δ represents the inequality without the weighting factor w_1 and w_2. For simplicity, the details of the Δ is omitted.

Obviously, the inequality (4.35) with a given $w_1 > 0$ and any $w_2 > 0$ holds, if the inequality (4.35) with a given $w_1 > 0$ and $w_2 = 0$ holds. Hence, when the inequalities (4.33)–(4.34) hold, Theorem 2 is satisfied. □

Remark 4.10. According to Corollary 1, the weighting factor w_2 can be adjusted online without re-design the switching function $\sigma(x(k))$. The benefit is that the balance between ripple minimization and switching frequency reduction can be adapted depending on the practical situation in real-time.

Remark 4.11. Even though the practical stability preserves theoretically for any $w_2 > 0$, one should be careful when increasing the weighting w_2. A very large w_2 will result in very large current and voltage ripple. In such a situation, the DC-DC converter is practically unstable.

Until now, the proposed method is designed for a specific reference point x_e. As we mentioned, in some applications, the output voltage of DC-DC power converters is required to track a changing reference signal or adjust manually. In the following corollary, the proposed control scheme is extended to a range of reference points. Therefore, the switching signal function can drive the state of DC-DC converters tracking different reference points within the range in real-time without re-design.

Corollary 4.12. *Consider the switched model (4.1) with sampling period T and given parameters $\xi > 0$, $\rho > 0$, $\varepsilon > 0$, $\kappa > 0$, $0 < \lambda_{min} < \lambda_{min} < 1$. If there exist matrices $P_j > 0$, $Q_i > 0$, scalars $\beta > 0$, $\mu_{jr} > 0$, for $\forall (i,j) \in \Xi \times \Xi$, $r \in \Xi$ such that*

$$\Psi(0,0,\lambda_{min}) < 0, \tag{4.36}$$
$$\Psi(T,T^2,\lambda_{min}) < 0, \tag{4.37}$$
$$\Psi(0,0,\lambda_{max}) < 0, \tag{4.38}$$
$$\Psi(T,T^2,\lambda_{max}) < 0, \tag{4.39}$$

with a given $w_1 > 0$ and $w_2 = 0$, then the condition (4.8) is fulfilled and the DC-DC converter is practical stabilizable to the region Θ around any desired reference point x_e with corresponding $\lambda \in [\lambda_{min}, \lambda_{max}]$ under the switching signal

$$\sigma(x(k)) = \arg \min_{(i,j)\in\Xi\times\Xi} \{2w_1 \left((x(k)-x_e)^T P_j (A_i x(k) + B_i)\right) + 2w_2 |i - \sigma(x(k-1))|\}$$

with the same $w_1 > 0$ and any $w_2 \geq 0$.

Proof. Continuing with the proof of Theorem 2, $\Omega(\tau,\tau^2,\lambda)$ is the only term dependent on λ. By substituting $A(\lambda) = \lambda A_1 + (1-\lambda)A_2$ into $\Omega(\tau,\tau^2,\lambda)$ and rearranging the matrix, one can

have:

$$\Omega(\tau,\tau^2,\lambda)=\lambda M+(1-\lambda)N=\lambda(M-N)+N \tag{4.40}$$

where

$$M=\begin{bmatrix} A_1^TP_j+P_jA_1 & 0 & -\tau(A_1^TP_j+P_jA_1) & 0\\ * & 0 & 0 & 0\\ * & * & \tau^2(A_1^TP_j+P_jA_1) & 0\\ * & * & * & 0 \end{bmatrix}$$

$$N=\begin{bmatrix} A_2^TP_j+P_jA_2 & 0 & -\tau(A_2^TP_j+P_jA_2) & 0\\ * & 0 & 0 & 0\\ * & * & \tau^2(A_2^TP_j+P_jA_2) & 0\\ * & * & * & 0 \end{bmatrix}.$$

Because $\lambda\in[\lambda_{min},\lambda_{max}]$, we can define:

$$\lambda=p\lambda_{max}+(1-p)\lambda_{min},\ p\in[0,1]. \tag{4.41}$$

The condition (4.36)–(4.39) can be written as:

$$\Lambda(0,0)+\beta(\lambda_{min}(M-N)+N)<0 \tag{4.42}$$
$$\Lambda(T,T^2)+\beta(\lambda_{min}(M-N)+N)<0 \tag{4.43}$$
$$\Lambda(0,0)+\beta(\lambda_{max}(M-N)+N)<0 \tag{4.44}$$
$$\Lambda(T,T^2)+\beta(\lambda_{max}(M-N)+N)<0, \tag{4.45}$$

where $\Lambda(\tau,\tau^2)=\Pi(0)+\beta\Omega(0,0)-\sum_r^{\Xi}\mu_{jr}\Upsilon_j(0,0)$.

Then multiplying $(1-p)$ to (4.42)–(4.43) and multiplying p to (4.44)–(4.45), one obtains:

$$(1-p)\Lambda(0,0)+\beta((1-p)\lambda_{min}(M-N)+pN)<0 \tag{4.46}$$
$$(1-p)\Lambda(T,T^2)+\beta((1-p)\lambda_{min}(M-N)+pN)<0 \tag{4.47}$$
$$p\Lambda(0,0)+\beta(p\lambda_{max}(M-N)+(1-p)N)<0 \tag{4.48}$$
$$p\Lambda(T,T^2)+\beta(p\lambda_{max}(M-N)+(1-p)N)<0. \tag{4.49}$$

Summing up (4.46)–(4.48) and (4.47)–(4.49) respectively yields,

$$\Psi(0,0,\lambda)=\Lambda(0,0)+\beta(\lambda(M-N)+N)<0 \tag{4.50}$$
$$\Psi(T,T^2,\lambda)=\Lambda(T,T^2)+\beta(\lambda(M-N)+N)<0. \tag{4.51}$$

Now we can claim, if the conditions (4.36)–(4.39) hold, the conditions (4.11)–(4.12) hold for $\forall\lambda\in[\lambda_{min},\lambda_{max}]$. □

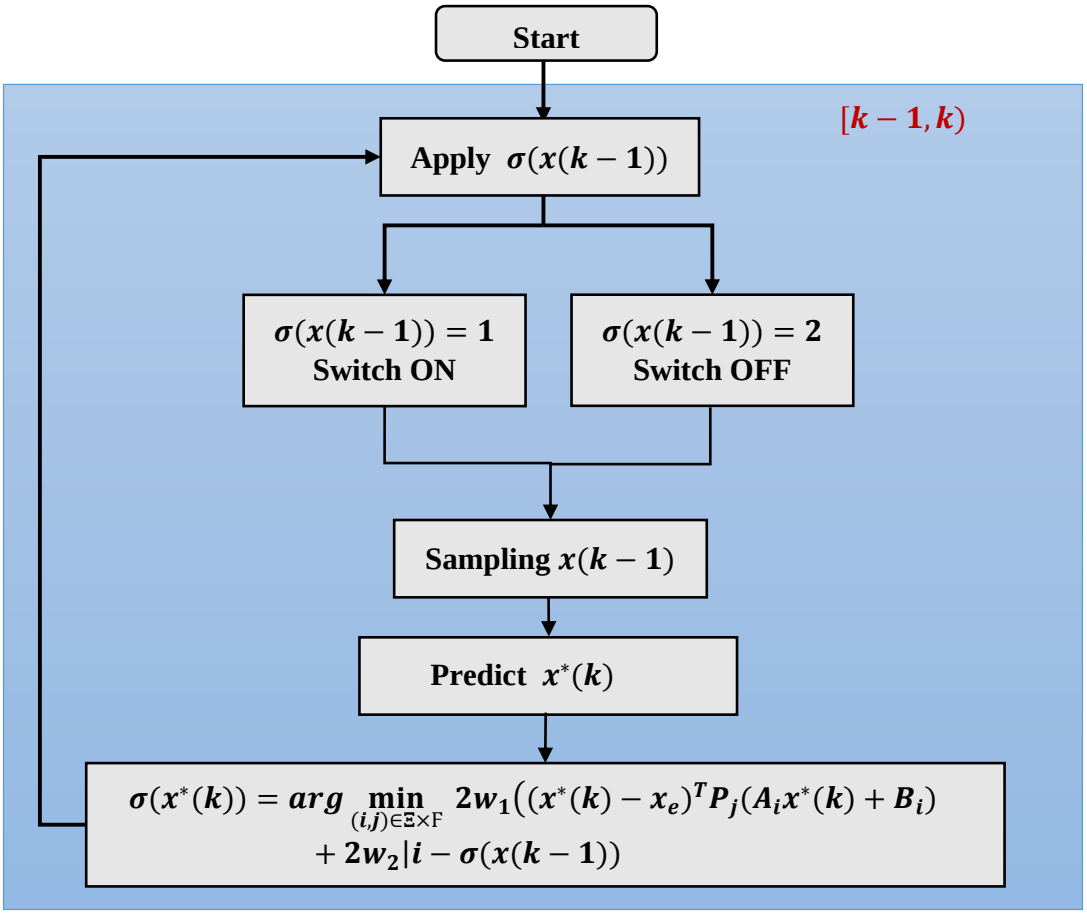


Figure 4.4: Flow chart of the proposed algorithm.

4.2.2 Online Implementation

This section explains in details of how to implement the off-line designed switching controller based on LMI conditions.

At the beginning, the switching signal $\sigma(x(0))$ needs to be initialized manually based on starting condition of the DC-DC converters. It is obvious that, in practice, the switching signal $\sigma(x(k))$ cannot be generated based on $x(k)$ as the time for computation of the switching signal cannot be zero. In this chapter, a novel online state prediction strategy is developed.

As shown in Figure 4.4, during the interval $[k-1,k])$, the switching signal $\sigma(x(k-1))$ which is calculated in previous interval $[k-2,k-1]$ is applied first and keeps constant in the current interval. At the same time, the system state $x(k-1)$ is sampled and the next state $x(k)$ is predicted based on the solution of the differential equation (4.1).

$$x^*(k)=\Phi_{\sigma(x(k-1))}(T)x(k-1)+\int_0^T \Phi_{\sigma(x(k-1))}(t)\mathrm{d}tB_{\sigma(x(k-1))} \tag{4.52}$$

where $\Phi_\sigma(t)=e^{A_\sigma t}$.

Then the switching signal $\sigma_{x^*(k)}$ for the next interval can be calculated and stored based on the proposed switching signal function (4.4). One may worry that the prediction error due to uncertainties in system model may affect the stability and performance. To treat this issue, one may use the technique in [140] to bound the prediction error, and convert it to an uncertainty in measurement. Since the proposed conditions are *strict* matrix inequalities, small uncertainties in measurement can be tolerated.

4.3 Simulation Results

In order to test the effectiveness of the proposed control algorithm, the switching controller is applied on a DC-DC buck converter as shown in Figure 4.1a. Numerical simulation is conducted first to show the validity of the mathematical model (4.1). The simulations were conducted using Matlab. The state matrices can be found in Table 4.1. The parameters for the buck converter are shown in Table 4.2. The sampling frequency $f = 40kHz$. For simplification, only the simulation results of CCM load ($R = 4.90\ \Omega$) are presented in this section.

The BMI conditions (4.36)-(4.39) in Corollary 2 are solved off-line by partitioning the S-procedure parameters β, μ_{jr} and converting the conditions to a set of LMI problems. Although solving general BMIs is NP-hard, the computational burden for the problem considered in this chapter remains affordable, since the order of the system is only 2.

Table 4.2: The buck converter parameters

Buck Converter Parameters	
	in *S.I.*
L	$616.3\mu H$
C	$880\mu F$
R	4.90Ω
V_g	$20V$

4.3.1 Model Normalization

Substituting all the parameter into the model based on Table 4.1, the state matrices is as follow:

$$A_1 = 10^3 \times \begin{bmatrix} -0.6490 & -1.6226 \\ 1.1364 & -0.2319 \end{bmatrix} \qquad B_1 = \begin{bmatrix} 32452 \\ 0 \end{bmatrix}$$

$$A_2 = 10^3 \times \begin{bmatrix} -0.6490 & -1.6226 \\ 1.1364 & -0.2319 \end{bmatrix} \qquad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

It can be seen that the value of the entries are very large due to the value of the inductor and capacitor. It will result in ill conditioned matrix inequalities. Hence, a Per-Unit technique,

which is a popular normalization method in the power systems analysis, is adopted to get a numerically friendly model. First, it is assumed that the input voltage V_g, the load resistance R, and the sampling frequency f are time-invariant. Then we can choose them as base quantities: $V_b = V_g$, $R_b = R$, $f_b = f$. The base inductance and capacitance can be deduced as:

$$L_b = \frac{R_b}{2\pi f_b} \qquad C_b = \frac{1}{2\pi f_b R_b} \tag{4.53}$$

Similarly, the base current $I_b = \frac{V_b}{R_b}$.
Therefore, the per unit values of all the parameters and states of the buck converter are defined as:

$$\bar{L} = \frac{L}{L_b} \qquad \bar{C} = \frac{C}{C_b} \qquad \bar{R} = \frac{R}{R_b} \tag{4.54}$$

$$\bar{v}_g = \frac{v_g}{V_b} \qquad \bar{v}_C = \frac{v_C}{V_b} \qquad \bar{i}_L = \frac{i_L}{I_b} \tag{4.55}$$

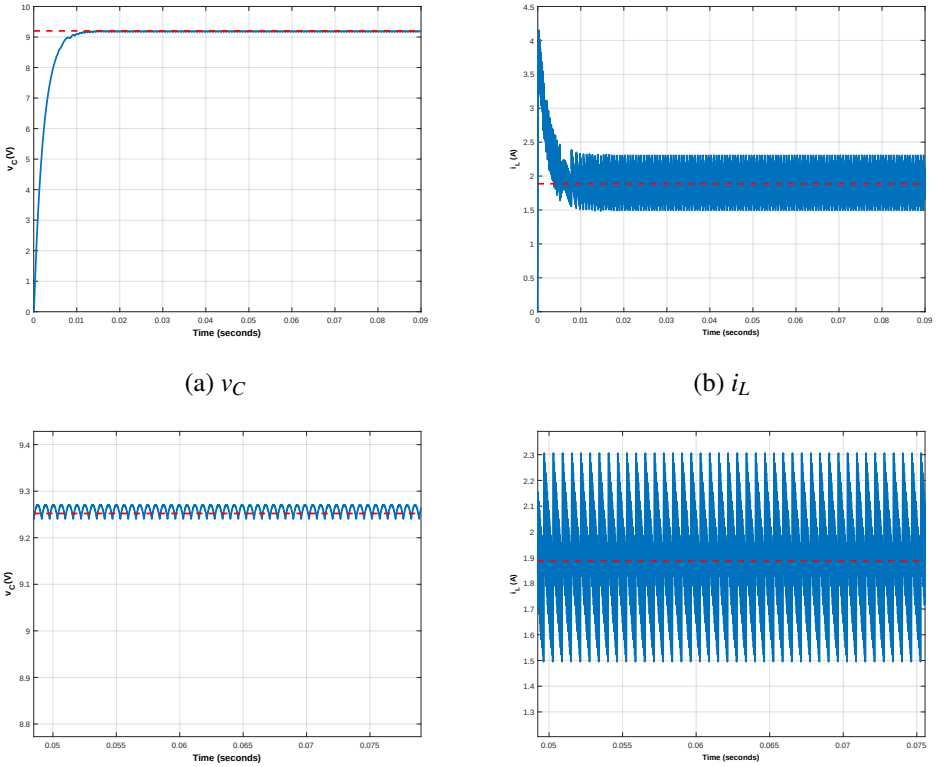
Hence, the normalized system state is $\bar{x}(t) = [\bar{i}_L \ \bar{v}_C]$, and the parameters of the converter are summarized in Table 4.3

Table 4.3: Converter parameters of the simulation results

Converter Parameter			
	in *S.I.*		in *P.U.*
L	$616.3\mu H$	$\bar{L}$	31.61
C	$880\mu F$	$\bar{C}$	1083.70
R	4.90Ω	$\bar{R}$	1.00
V_g	$20V$	$\bar{V}_g$	1.00

4.3.1.1 Start-up response without switching frequency tuning

Firstly, the tuning parameters are given as: $\xi = 2 \times 10^{-4}$, $\rho = 1 \times 10^{-4}$, $\varepsilon = 2$, $\kappa = 1 \times 10^{-4}$, $w_1 = 1$, $w_2 = 0$. λ is set as 0.46, which is corresponding to the reference point $x_e = [1.89\ 9.25]^T$. When $\beta = 1$, $\mu_{12} = 1.5$, $\mu_{21} = 1.1$, the conditions (4.36)–(4.39) are feasible. The value of the matrices P_j, Q_i are omit due to space limit. Then under the switching signal function $\sigma(x(k))$, the state response is depicted in Figure 4.5. It can be seen that output voltage v_C and inductance current i_L have been driven to the desired reference point x_e respectively during a short transition period and there is no overshoot for output voltage $v_C(t)$.



(a) v_C (b) i_L

(c) Ripple of v_C (d) Ripple of i_L

Figure 4.5: The start-up responses of v_C and i_L without switching frequency tuning (Simulation).

4.3.1.2 Switching signal function analysis

Although the stability condition for the switching signal function design seems complicated, the precalculation of the parameters makes it very simple to implement. The nature of the switching signal function $\sigma(x(k))$ is to partition the state-space into different regions. After searching the state-space, the switching surface for different reference points can be calculated. The state-space partition can be seen in Figure 4.6. For the Buck converter, A_1 and A_2 are equal and the matrices P_1, P_2 are similar. Hence, the switching surfaces are almost linear as seen in Figure 4.6, which are presented by the dashed lines. The switching signal is defined as ON if the system state is recognized in the left of the selected switching surface, otherwise the switching signal is defined as OFF. In Figure 4.6, the transition behaviour of the system state with three different reference points is presented as examples. The colours of asterisks mean different switching signals, that is: red means ON, black means OFF; and the arrows indicate the time revolution of the system state $x(t)$. As it can be seen, if the state is away from the switching surface, the switching signal will drive the state towards the switching surface. If the state is around the switching surface, then it will be driven to the origin along the surface. Finally, the system state $x(t)$ will be stabilized around the desired reference point.

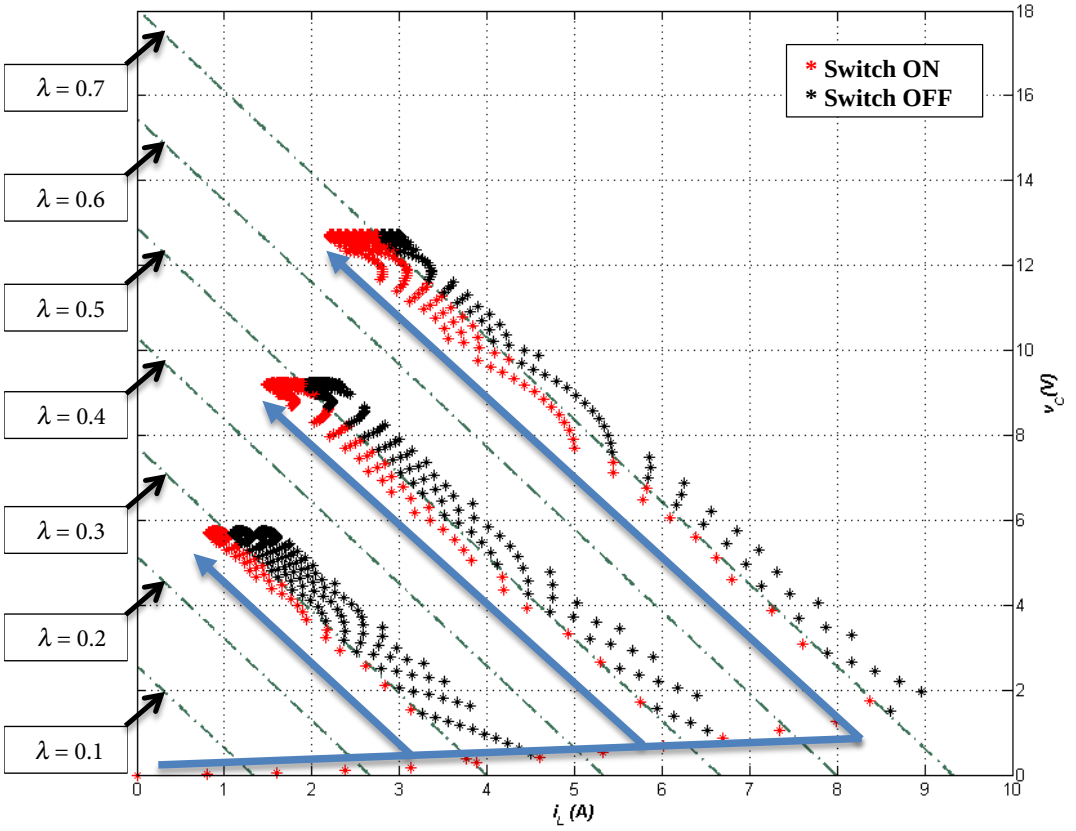


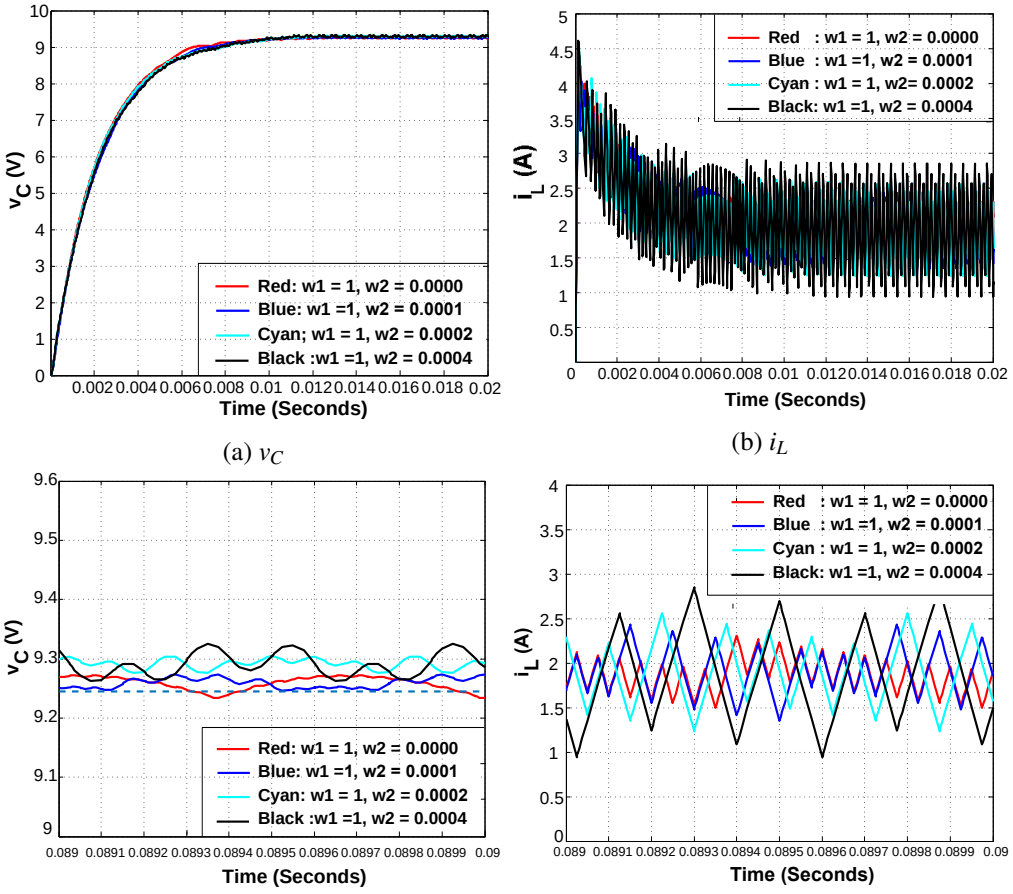
Figure 4.6: Switching surface for different reference points.

Table 4.4: Weighting factors, average switching frequency and voltage ripple (Simulation).

w_1	w_2	$f_s(averge)$(V)	ΔV_C(V)
1	0	18.9kHz	0.03
1	0.00001	12.7kHz	0.05
1	0.00002	8.6kHz	0.07
1	0.00004	5.2kHz	0.10

4.3.1.3 Start-up responses with switching frequency tuning

In this section, the impact of weighting factors are studied with the same switching controller. Four different values of w_2: 0, 0.00001, 0.00002, 0.00004 are tested. The responses of v_C and i_L under different weighting factors are shown in Figure 4.7. As it can be seen, the system presents quite similar behaviour even if the weighting factor w_2 is changed. In Table 4.4, it can be seen that when the weighting factor w_2 is increasing, the average switching frequency decreases rapidly at the cost of sightly larger voltage and current ripple. It follows that a trade-off between switching frequency and voltage ripple can be achieved through manipulating the weighting factor w_2.



(a) v_C (b) i_L

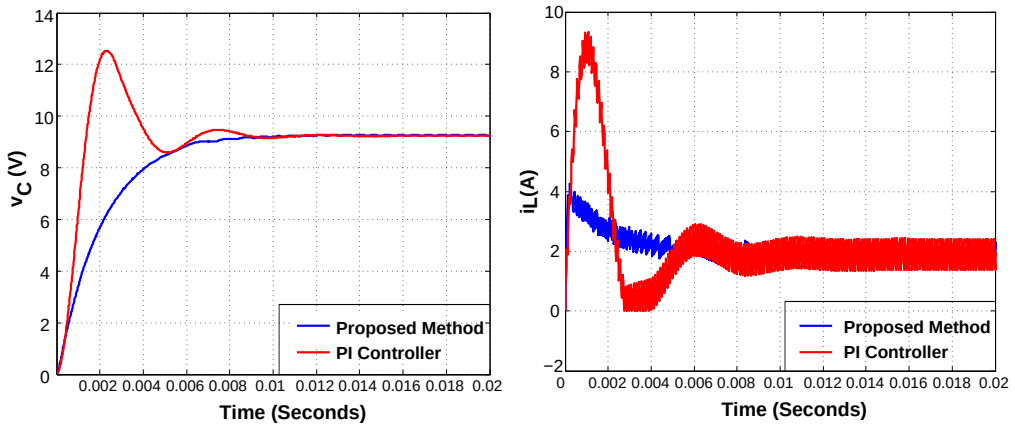
(c) Ripple of v_C (d) Ripple of i_L

Figure 4.7: The responses of v_C and i_L with switching frequency tuning (Simulation).

4.3.2 Comparison with Other Control Schemes

In this subsection, the proposed switching control approach is further compared with a traditional industry-standard PI-type controller tuned on the basis of a linearized averaged model (averaged control scheme) [141]. Simulation results are shown in Figure 4.8.

The phase diagrams for both proposed method and PI controller are shown in Figure 4.9. Obviously, the trajectory of the proposed method is more straightforward than PI controller towards the origin which results in shorter transition period, no voltage overshoot, and lower current ripple. In addition, the proposed method does not involve any complicated modulation, and can be extended to DCM operation readily, thus simplifying the design and implementation.



(a) v_C (b) i_L

Figure 4.8: The responses of v_C and i_L under proposed method and a PI controller (Simulation).

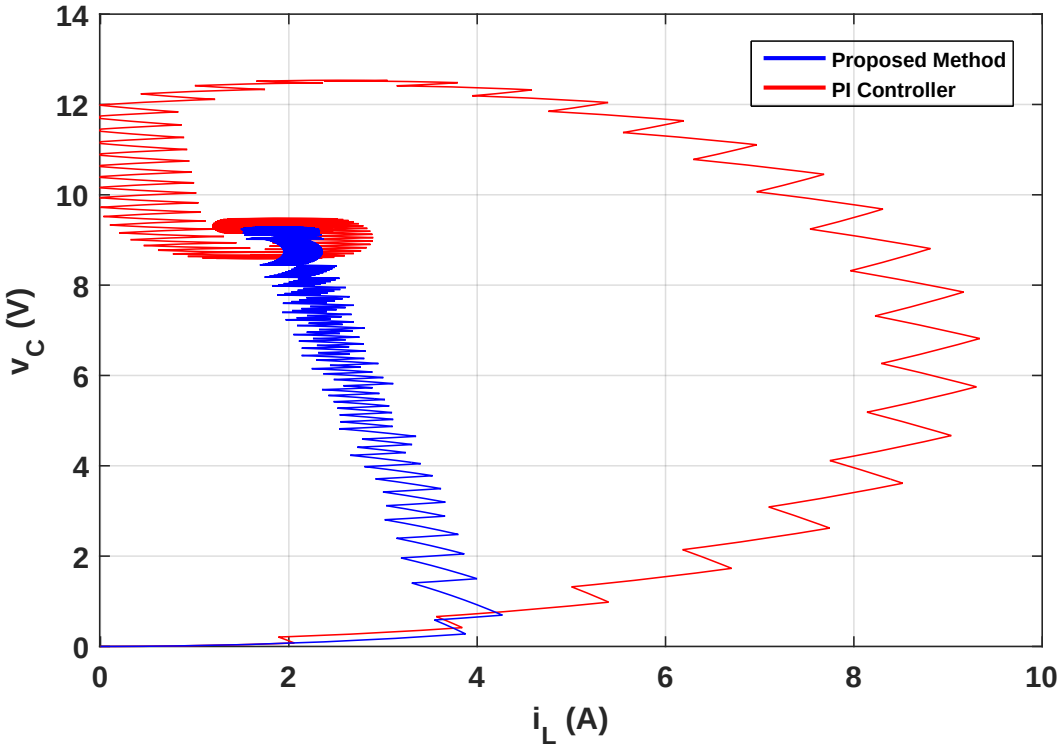


Figure 4.9: Phase diagrams of the proposed method and a PI controller.

4.4 Experiment Platform for Buck Converter Test

4.4.1 The Buck Stage

In order to test the proposed control algorithms on the buck converter, a prototype has been designed and built. The PCB for the buck stage is shown in Figure 4.10. The parameters for the

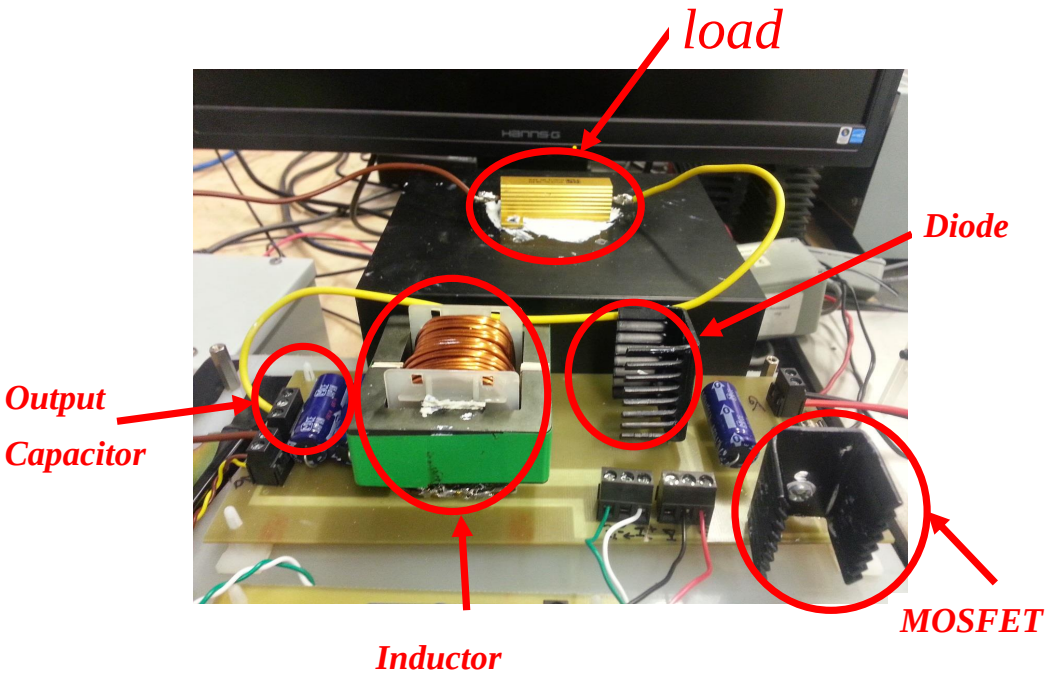


Figure 4.10: Buck stage PCB board

buck stage are shown in Table 4.5. This design is based on the conventional design procedure in [24].

Table 4.5: System parameters and component values

Parameter name	Symbol	Value
DC-Link Voltage	V_g	20V(dc)
Nominal Output Voltage	V_O	10V(dc)
Sampling Frequency	f_s	50kHz
Inductor	L	616.3μH
Capacitor	C	880μF
Load	R	4.7Ohm(Ω)

4.4.2 Current Measurement

For closed-loop control of the buck converter, the inductor current i_L needs to be measured. Here, the LAH 25-NP current transducer, which has excellent accuracy, is employed. The PCB board designed for the current sensor is shown in Figure 4.11. The accuracy of a sensor relates to how closely the measurement value can be converted to the real value of the current. Hence, the current sensor needs to be calibrated before use.

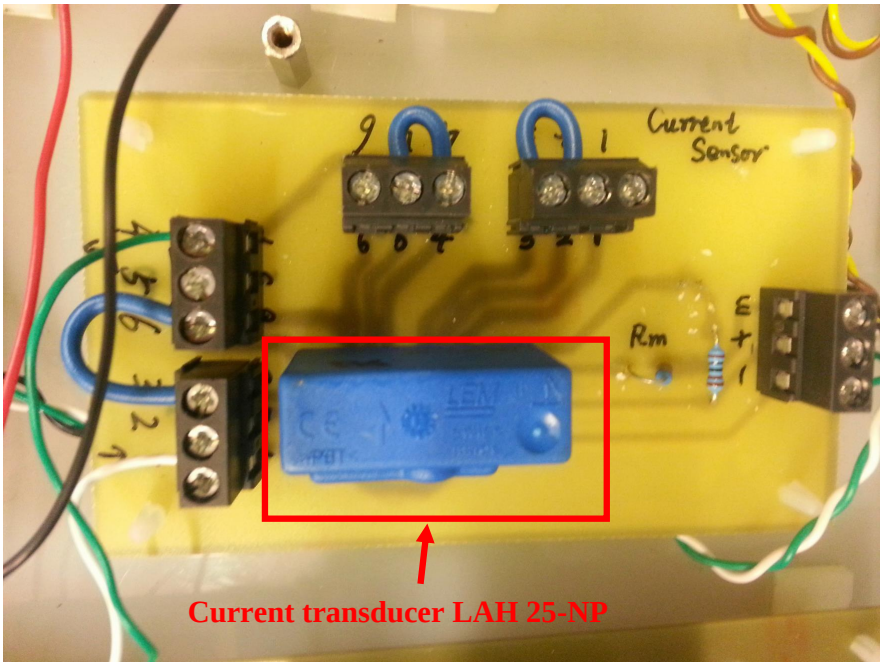


Figure 4.11: Current measurement PCB board

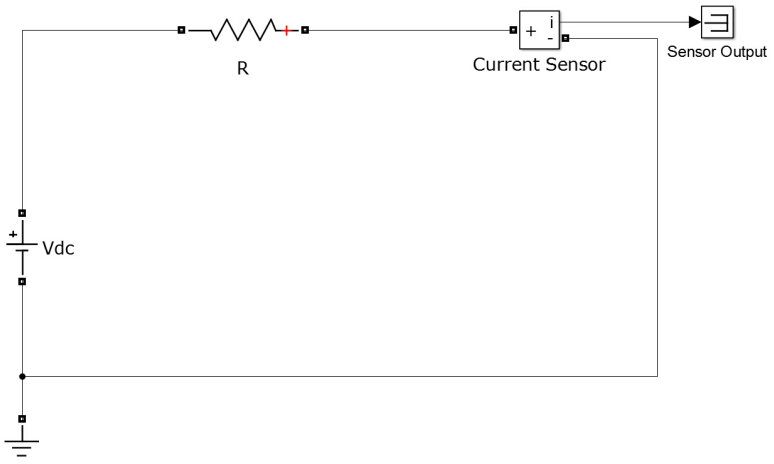


Figure 4.12: Current calibration circuit

4.4.2.1 Current Calibration

The current sensor is used to measure the current of a simple circuit (Figure 4.12) whose current can be calculated because the resistor value is known ($R = 4.9\Omega$) Then the voltage V_{dc} is changed in a range and the corresponding sensor output voltage can be obtained, which is shown in Table 4.6. Hence, the data can be fitted with a linear interpolation shown in Figure 4.13. The measured voltage output from the current sensor can be converted to a current value in unit of A by (4.56).

$$I = 1.063V_{sensor} - 0.0673 \tag{4.56}$$

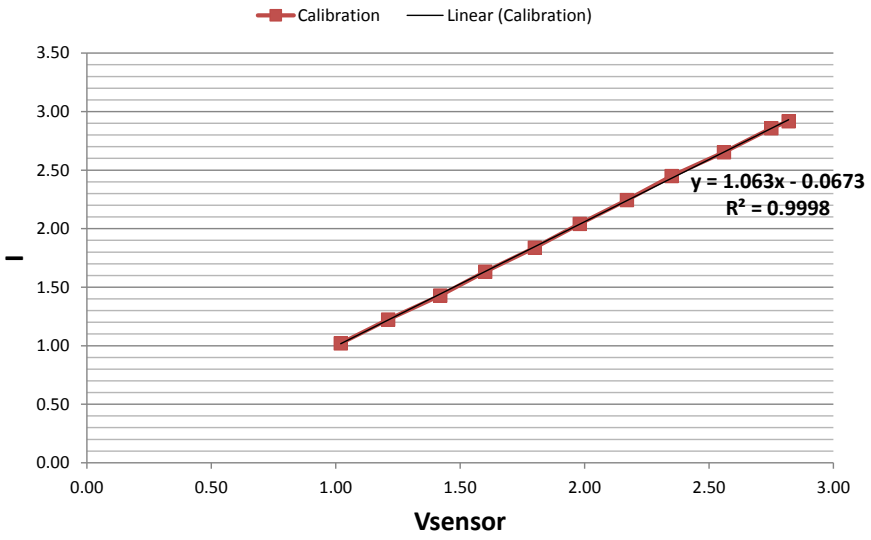


Figure 4.13: Linear fitting of current sensor calibration

Table 4.6: Current calibration data

V_{dc}(V)	I(A)	V_{sensor}(V)
5	1.02	1.02
6	1.22	1.21
7	1.43	1.42
8	1.63	1.60
9	1.84	1.80
10	2.04	1.98
11	2.24	2.17
12	2.45	2.35
13	2.65	2.56
14	2.86	2.75

4.4.3 Voltage Measurement

The voltage across the Capacitor v_C is measured by the voltage transducer LV25-P. The PCB board designed for the voltage sensor is shown in Figure 4.14. The voltage sensor also needs to be calibrated as the current sensor.

4.4.3.1 Voltage Sensor Calibration

The circuit used for voltage sensor calibration is shown in Figure 4.15. The voltage source in the circuit is changed in a range and the sensor output voltage can be measured which is shown in Table 4.7. Hence, the data can be fitted with a linear interpolation shown in Figure 4.16. The measured voltage output from the voltage sensor can be converted to a voltage value in unit of A by (4.57).

$$V = 1.063V_{sensor} - 0.0673 \tag{4.57}$$

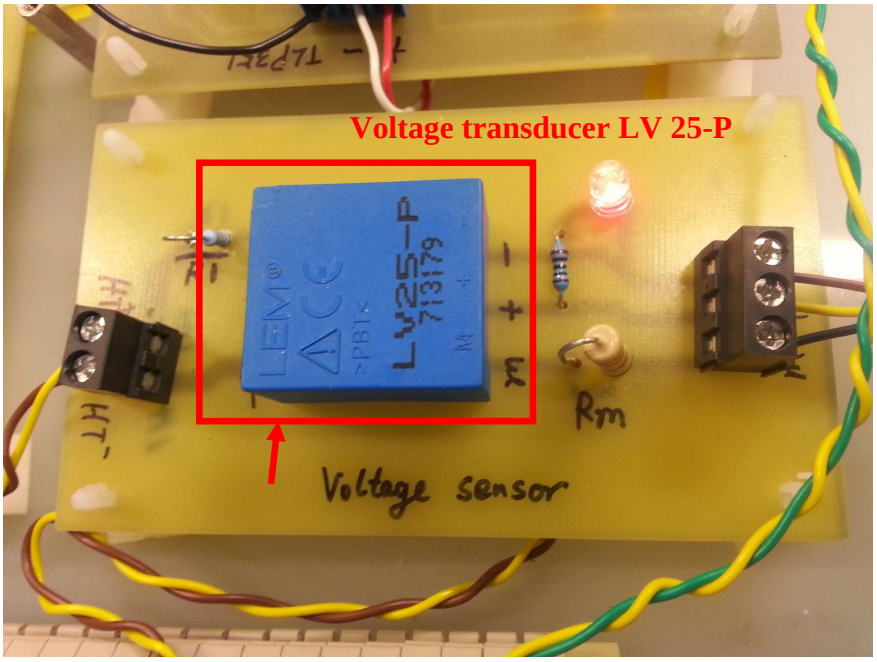


Figure 4.14: Voltage measurement PCB board

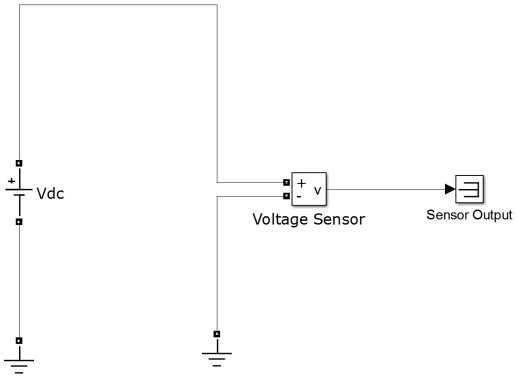


Figure 4.15: Voltage calibration circuit

Table 4.7: Voltage calibration data

V_{dc}	5	6	7	8	9	10	11	12	13	14	15	16	17
V_{sensor}	1.23	1.48	1.71	1.99	2.23	2.48	2.72	2.96	3.21	3.45	3.69	3.93	4.17
V_{dc}	18	19	20	21	22	23	24	25	26	27	28	29	30
V_{sensor}	4.43	4.67	4.92	5.16	5.40	5.64	5.88	6.12	6.38	6.60	6.85	7.08	7.32

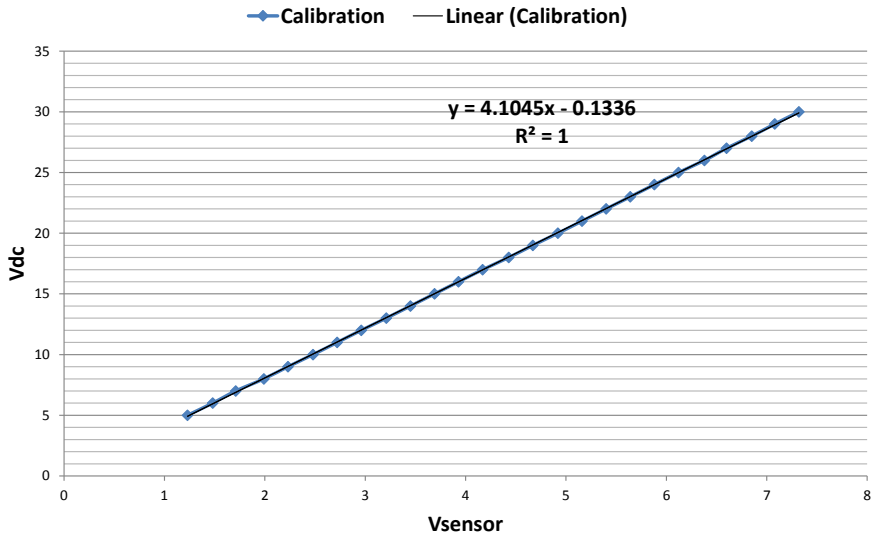


Figure 4.16: Linear fitting of voltage sensor calibration

4.4.4 MOSFET Gate Drive

The key component of the buck converter is the MOSFET. A proper gate drive circuits is essential to guarantee the MOSFET's switching behaviour. There are two task for the gate drive of the buck converter.

- Convert the switching signal from the control platform to MOS level, which is suitable to open and close MOSFET.
- Isolate the buck stage and the control platform, so when problems (short circuits, etc.) happen in the buck stage, the control platform stays safe.

Hence, "TLP351" insolate the signal from the control platform and gate signal, then "SN74LS07" converts the switching signal to MOS level. The PCB board for the MOSFET gate drive is shown in Figure 4.17 The whole buck converter system without control platform is shown in Figure 4.18

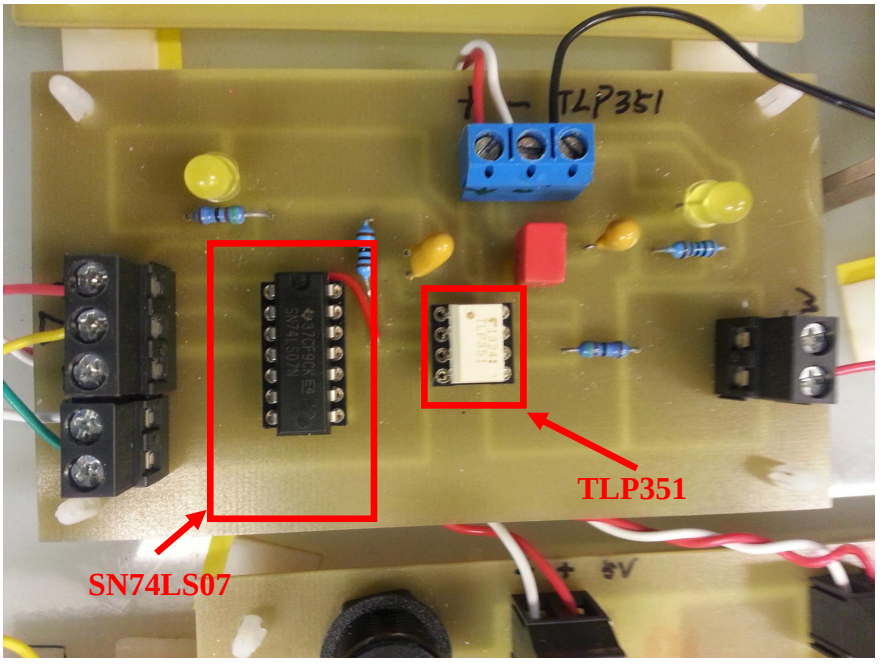


Figure 4.17: MOSFET drive board

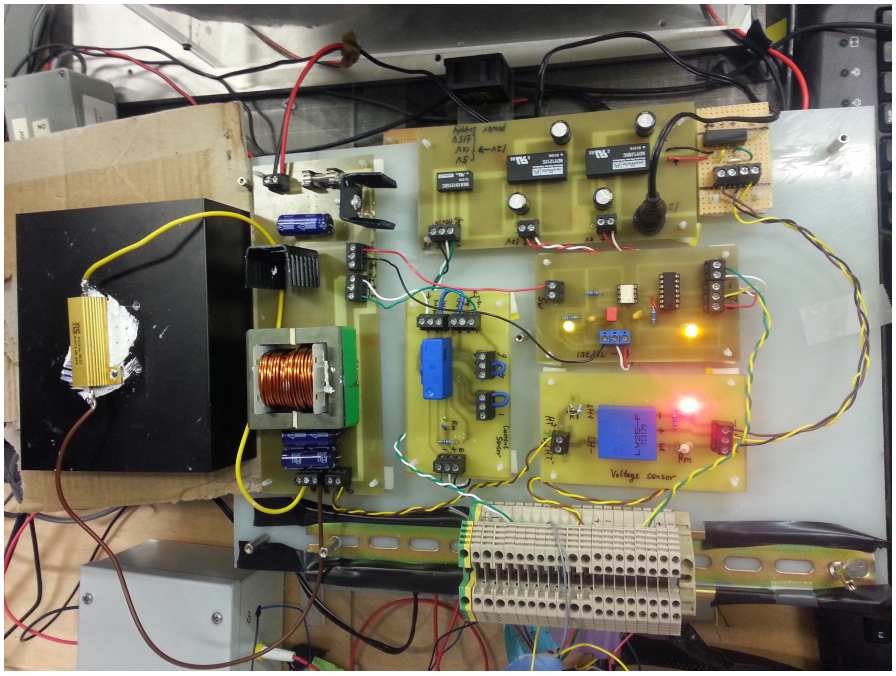


Figure 4.18: Whole buck converter system without control platform

4.5 Experimental Results

The proposed algorithms are implemented on the dSPACE MicroAutoBox(1401/1511) 2nd generation with built-in *IBM PPC 750GL, 900 MHZ* processor. In this section, both continuous conduction mode (CCM) and discontinues conduction mode (DCM) are tested under different operation conditions.

4.5.1 Start Up and Close Down Response

The start up and close down response of the output voltage v_C is shown in Figure 4.19. The buck converter is controlled to start up to a reference level and close down several times. As we can see, the transition period is less than $10ms$ and there is no overshoot. A zoomed start up response is shown in Figure 4.20.

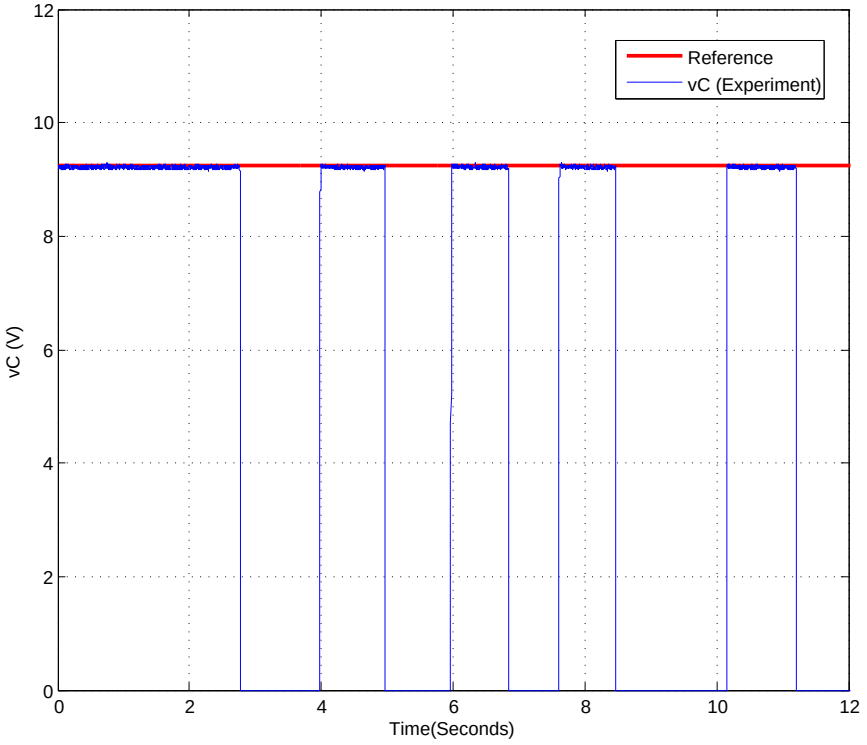


Figure 4.19: The response of the output voltage v_C

4.5.2 Continuous Conduction Mode (CCM)

In this mode, the load is set as 4.90Ω.

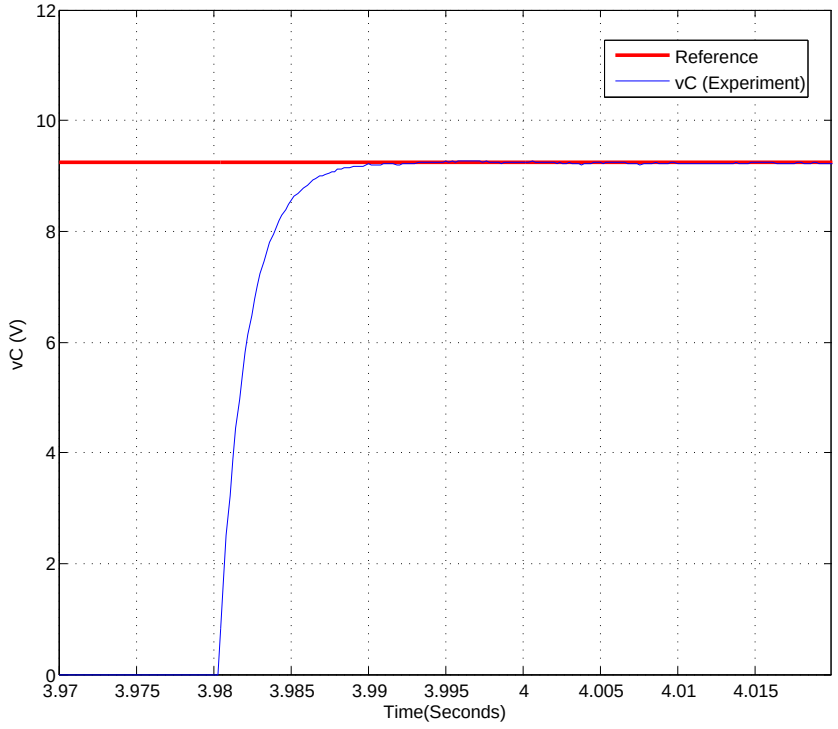


Figure 4.20: The zoomed response of the output voltage v_C

Start-up response under different sampling frequency In this part, the switching controller in Corollary 2 are solved for different sampling frequency. The tuning parameters are given as: $\xi = 2\times10^{-4}$, $\rho = 1\times10^{-4}$, $\varepsilon = 2$, $\kappa = 1\times10^{-4}$, $w_1 = 1$, $w_2 = 0$. The conditions (4.36)–(4.39) are feasible for sampling frequency: $f_s = 10\ kHz$ ($\beta = 1$, $\mu_{12} = 1.5$, $\mu_{12} = 1.1$), $f_s = 20\ kHz$ ($\beta = 1$, $\mu_{12} = 1.5$, $\mu_{12} = 1.1$), $f_s = 40\ kHz$ ($\beta = 1$, $\mu_{12} = 1.5$, $\mu_{12} = 1.1$). Figs. 4.21–4.23 show the experimental behavior of the system state under different sampling frequencies. One can clearly observe that the proposed methods can be applicable to a wide sampling frequency range and generate similar transition performance as shown in simulation results.

Reference tracking As we claimed in Corollary 2, the proposed switching controller is solved for $\forall\lambda \in [0,1]$, which means that the switching controller is able to drive the converter to track different reference point x_e. In the part, the sampling frequency is 10 kHz with parameters $\xi = 2\times10^{-4}$, $\rho = 1\times10^{-4}$, $\varepsilon = 2$, $\kappa = 1\times10^{-4}$, $w_1 = 1$, $w_2 = 0$, $\beta = 1$, $\mu_{12} = 1.5$, $\mu_{12} = 1.1$. As pointed out previously, the controller is robust to the change of the reference points as shown in Figure 4.24. Both the capacitor voltage and the inductor current have been controlled to track the corresponding reference effectively.

Switching frequency tuning As we proposed, the average switching frequency can be optimized by tuning a set of weighting factors. It gives more flexility for the balance between the

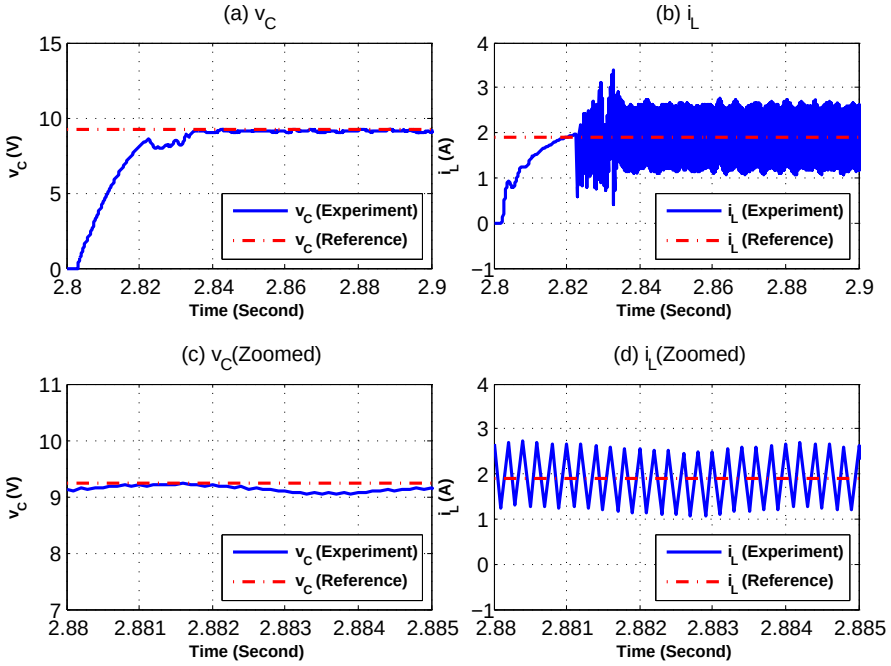


Figure 4.21: The responses of v_C and i_L ($f_s = 10\ kHz$, CCM)

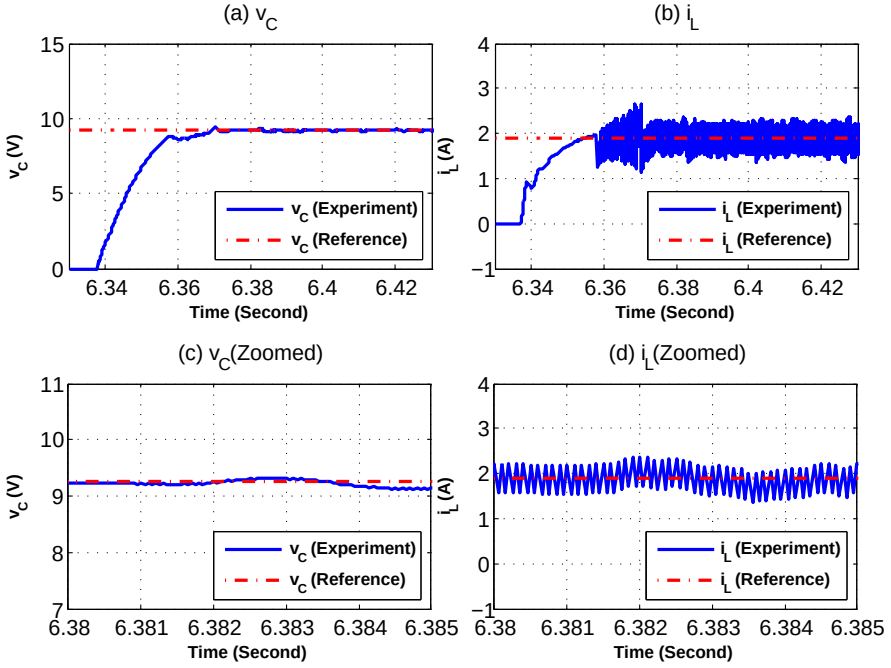


Figure 4.22: The responses of v_C and i_L ($f_s = 20\ kHz$, CCM)

voltage ripple and switching frequency. This is also verified in the real experiment. A high sampling frequency $40kHz$ is used to solve the switching controller in Corollary 2 with parameters $\xi = 2\times10^{-4}$, $\rho = 1\times10^{-4}$, $\varepsilon = 2$, $\kappa = 1\times10^{-4}$, $w_1 = 1$, $w_2 = 0$, $\beta = 1$, $\mu_{12} = 1.5$, $\mu_{12} = 1.1$. The result is shown in Figure 4.25. As we can see, as w_2 is increasing, the average switching frequency decreased rapidly but the voltage ripple just increases slightly.

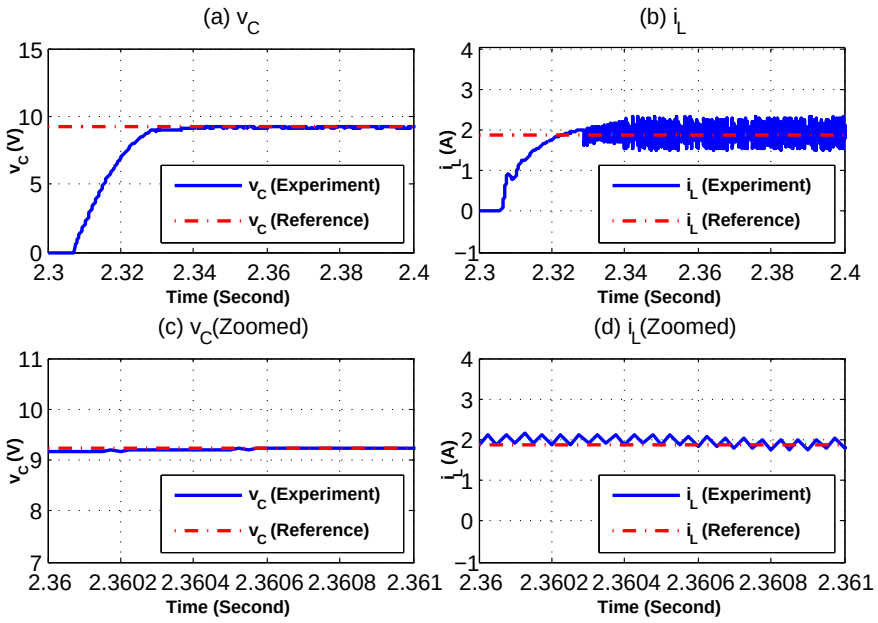
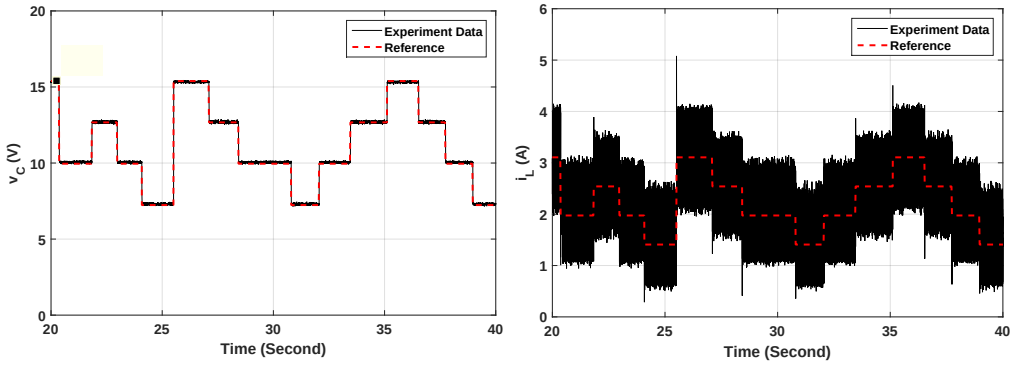


Figure 4.23: The responses of v_C and i_L ($f_s = 40\ kHz$, CCM)



(a) v_C (b) i_L

Figure 4.24: The responses of v_C and i_L to different reference points (CCM mode).

4.5.3 Discontinuous Conduction Mode (DCM)

In this mode, the load is set as 30Ω and sampling frequency is fixed as 40 kHz. The parameters that is used to solve the switching controller $\sigma(x(k))$ in Corollary 2 are $\xi = 2\times10^{-3}$, $\rho = 1\times10^{-4}$, $\varepsilon = 2$, $\kappa = 1\times10^{-4}$, $w_1 = 1$, $w_2 = 0$, $\beta = 1$, $\mu_{12} = 1.3$, $\mu_{12} = 1.2$. The start-up response is shown in Figure 4.26. One can easily notice that the inductor current i_L is discontinuous. The transition time is around $10ms$ and no overshoot is presented for the output voltage. Furthermore, the converter is also controlled to track different reference points by the proposed switching controller as depicted in Figure 4.27. The output voltage is controlled to several voltage level: $16V$, $12V$, $10V$, $8V$, $2V$ with similar transition period and no overshoot. From Figure 4.28, it can be seen that when increasing the weighting factor w_2, the average switching frequency decreases as well as the ripple of the output voltage and inductor current. This behaviour is similar to CCM mode.

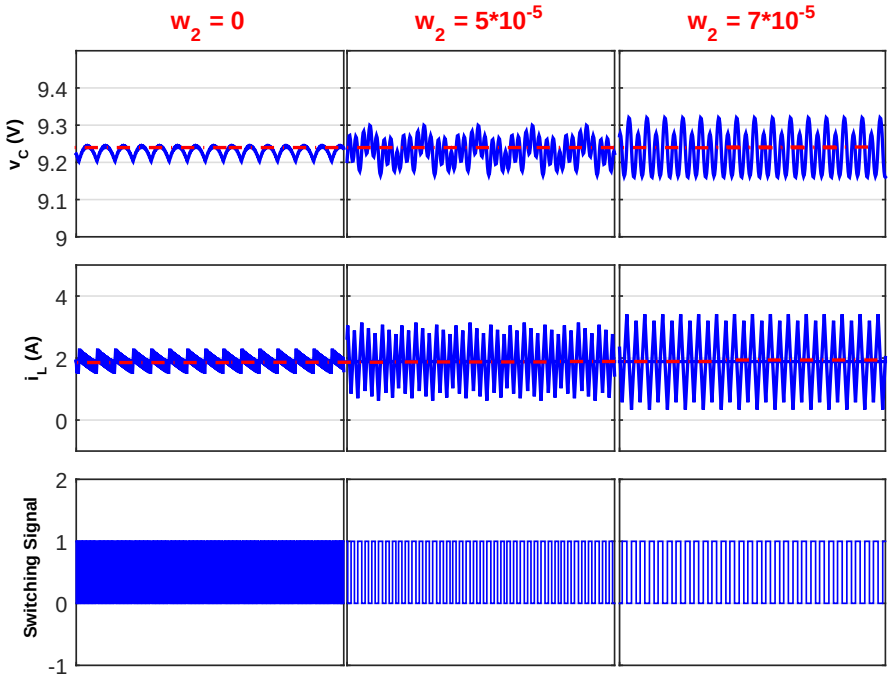


Figure 4.25: Experimental behaviour of v_C, i_L and switching signal σ when tuning the weighting factor w_2 (CCM mode).

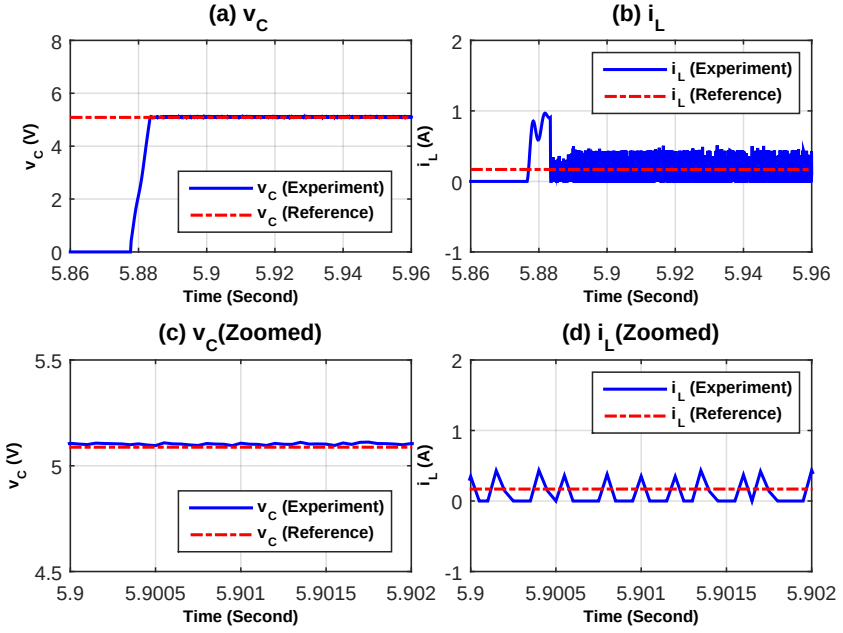
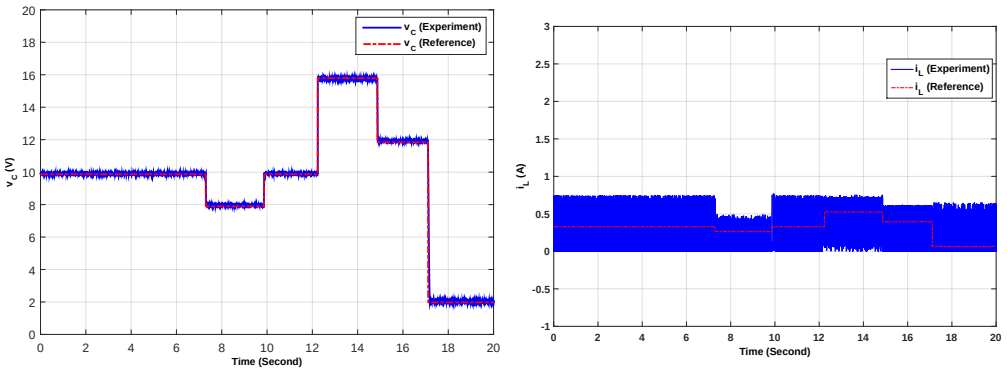


Figure 4.26: The start-up responses of v_C and i_L (DCM mode)



(a) v_C (b) i_L

Figure 4.27: The responses of v_C and i_L to different reference points (DCM mode).

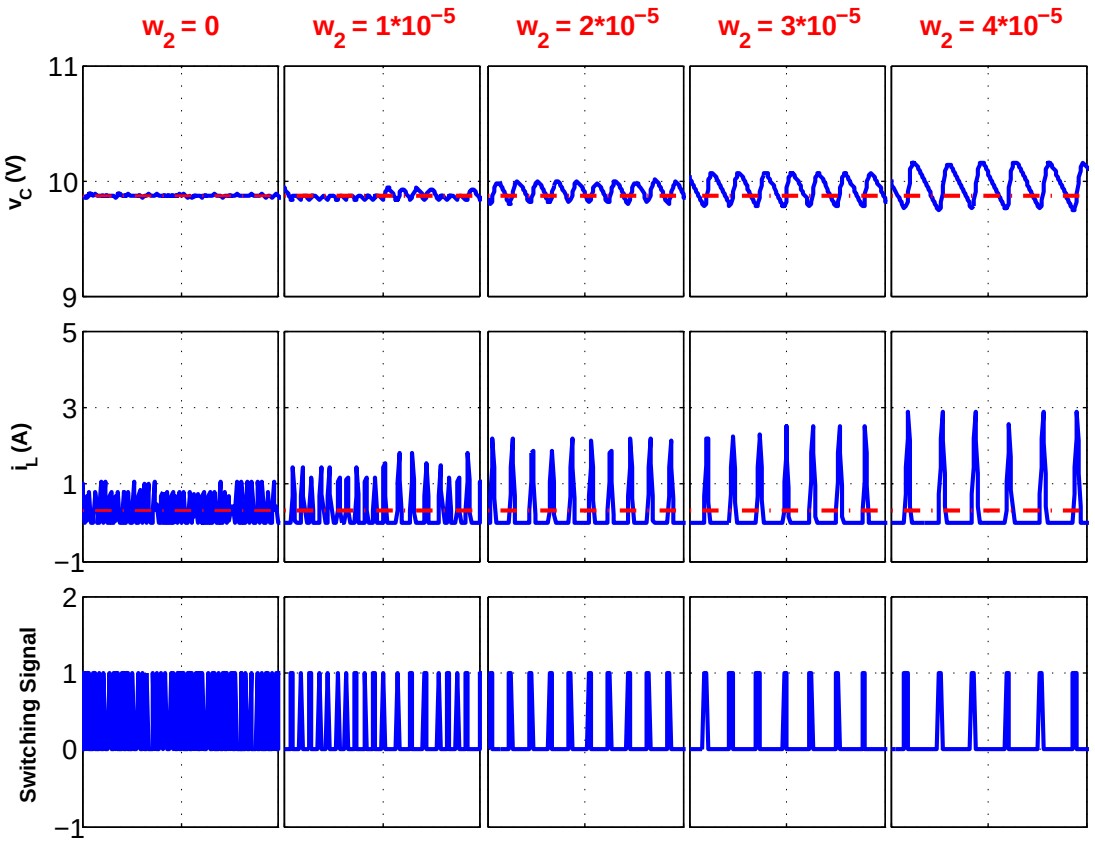


Figure 4.28: Experimental behaviour of v_C, i_L and switching signal σ when tuning the weighting factor w_2 (DCM mode).

4.6 Summary

In this chapter, the DC-DC power electronics converters are considered to be controlled by a digital controller. A sampled-data switched model is established to describe the closed-loop dynamics. Our goal is to design a switching controller with guaranteed closed-loop stability in the entire state-space for varying reference points. In order to address the issue of time delay in switching signal generation, an online state prediction is introduced such that the switching signal is computed one period before its implementation. Comparing with the existing results, the main contributions of this chapter are summarized as:

1. The proposed sampled-data switched model captures full-time information instead of a discrete-time model without the inter-sample behaviour of the power electronics converters, and the switching controller can be implemented easily with digital devices.
2. The designed controller is able to track changing reference signals without re-design, and this is guaranteed theoretically.
3. Switching frequency can be adjusted online without losing closed-loop stability.
4. The parameters of the switching controller is calculated offline, thus significantly reducing the online computation burden.
5. CCM and DCM operations can be treated in a unified approach.

Chapter 5

Output Feedback Switching Control Using Multiple Sampling

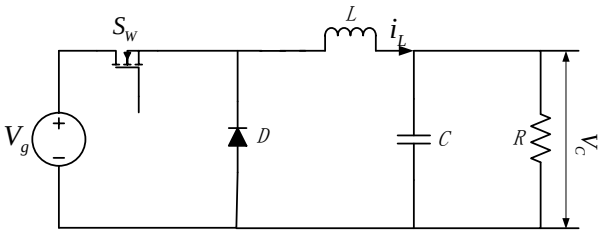
5.1 Problem Formulation

5.1.1 Switched Models for Different DC-DC Topologies

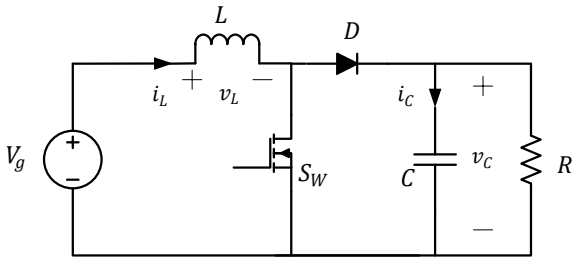
The circuit topologies for a series of DC-DC converters (Buck, Boost, Buck_Boost and Cuk) are shown in Figure 5.1a- Figure 5.1d. The function of the converter is to convert the unregulated DC source V_g to a regulated DC output level with satisfactory performance and robustness. For all the topologies: V_g is a DC voltage source; D is a diode; L is the inductance of a inductor; C is the capacitance of a capacitor; and R represents a resistive load. The two key components for the converter are the power semiconductor S_W (MOSFET, IGBT, or else), which can be modelled as an ideal switch, and the diode D.

The behaviour of the power semiconductor S_W is controlled by a switching signal σ taking values from a set $[0,\infty) \rightarrow \Xi = \{1,2\}$, where 1 and 2 represent "on" and "off" of the switch, respectively. Restricted by the design limit of the power semiconductor, the switch frequency must be upper bounded. Hence, a **dwell period** is defined as T_d. During the dwell period, the switching signal σ keeps constant. The sampling period T_s is equal or less than the dwell period, which mean during dwell period the system output state will be sampled equal or more than once.

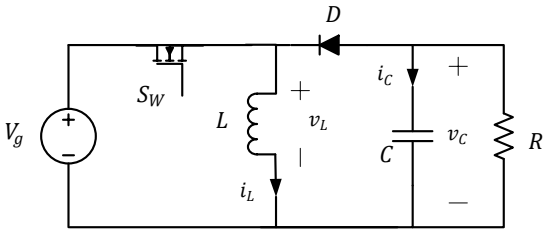
For brevity, it is assumed that the converter is always operated in the continuous conduction mode (CCM). Hence, the converter has two switching modes due to the action of the switch S_W: ON mode and OFF mode. For each mode, the converter can be described by a differential equation. According to the switched systems theory, all these converters can be described as a uniform affine continuous state-space equations (5.1), where $x(t) \in R^{n\times 1}, A_\sigma \in R^{n\times n}$, and



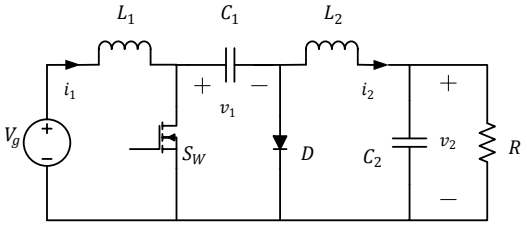
(a) DC-DC Buck Converter



(b) DC-DC Boost Converter



(c) DC-DC Buck_Boost Converter



(d) DC-DC Ćuk Converters

Figure 5.1: Topologies for different DC-DC Converters

$B_\sigma \in R^{n\times 1}$. The only difference is the state matrixes A_σ, B_σ. The corresponding state matrices can be seen in Table 5.1.

$$\dot{x}(t) = A_\sigma x(t) + B_\sigma \tag{5.1}$$

Due to the affine terms and state-dependent switching, the equilibrium for the switched model (5.1) is designable. However, there is a trivial null equilibrium for the model but it is not what we need. The desired switched equilibrium x_e can be obtained by taking the convex combination of two subsystems.

Table 5.1: State matrices of switched model for different topologies

Topologies	A_σ	B_σ
Buck Converter	$A_1 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$	$B_1 = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$
	$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$	$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$
Boost Converter	$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$	$B_1 = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$
	$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$	$B_2 = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$
Buck_Boost Converter	$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$	$B_1 = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$
	$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$	$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$
Ćuk Converters	$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix}$	$B_1 = \begin{bmatrix} \frac{V_g}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$
	$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix}$	$B_2 = \begin{bmatrix} \frac{V_g}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$

Consider a simplex

$$\Gamma = \left\{ [\gamma_1, \gamma_2],\ \gamma_i > 0,\ \sum_i^2 \gamma_i = 1 \right\} \tag{5.2}$$

The convex combinations of state matrices are defined as

$$A_\gamma = \sum_i^2 \gamma_i A_i \quad B_\gamma = \sum_i^2 \gamma_i B_i \quad [\gamma_1, \gamma_2] \in \Gamma$$

There exists a set of attainable switched equilibria

$$Xe = \left\{ x_e : x_e = -A_\gamma^{-1} B_\gamma,\ \forall [\gamma_1, \gamma_2] \in \Gamma \right\} \tag{5.3}$$

The proposed switching controller will drive the system to any desirable switched equilibrium x_e in the sex X_e from any initial condition. In real practice, the equilibriums of the DC-DC

converters should be non-zero. In order to apply the Lyapunov theory to design the controller, the non-zero equilibrium needs to be shifted to the original point. To this end, we define an error state as $e(t) = x(t) - x_e \in R^{n\times 1}$. Then the switched error system can be described by:

$$\dot{e}(t) = A_\sigma e(t) + \hat{B}_\sigma, \quad \forall t \in [k, k+1) \tag{5.4}$$

where $\hat{B}_i = A_i x_e + B_i \in R^{n\times 1}, \forall i \in \Xi$, for which $\sum_i^2 \gamma_i \hat{B}_i = 0$.

5.2 A Discrete Model Under Multiple Sampling

A more realistic situation for power converter implementation is that the state is not fully accessible due to various reasons, e.g., hardware, cost, and reliability. It is meaningful to design a controller based on the known dynamic model and limited measurement. Herein, it is assumed that the accessible state can be described by $y(t) \in \Re^{m\times 1}$ (m is number of the measured state, and $m \leq n$) and

$$y(t) = Ce(t) \tag{5.5}$$

In this chapter, we would like to seek a quadratic partition [142] based on the output only to construct switching laws. However, it is not easy to obtain a feasible partition for an output with limited dimension ($m < n$) because $y(t)$ provides limited information of the state. To tackle this issue, a novel multiple sampling scheme inspired by [143] is used here to acquire more information.

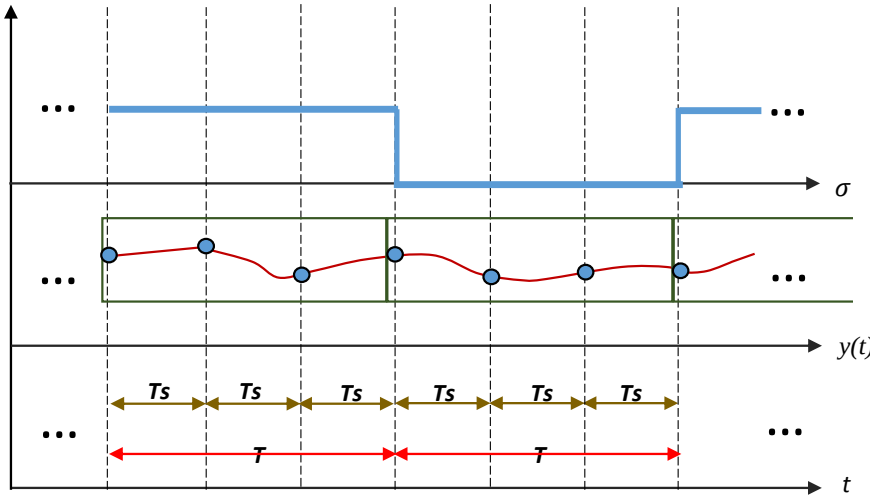


Figure 5.2: Multiple sampling technique ($h = 3, m = 1$)

For brevity, we assume that the dwell period T_d is h times of the sampling period T_s ($T_d = hT_s$). Hence, during one dwell period, the output $y(t)$ is sampled h times at every kT_d, $kT_d + T_s$, $kT_d + 2T_s, \ldots, kT_d + (h-1)T_s$. For example, the sampling and switching behaviors for $h = 3$ and

$m = 1$ are shown in Figure 5.2. The switching signal keeps constant during each dwell period T_d, and the output $y(t)$ is sampled three times before the next dwell period.

Hence,

$$\begin{aligned} y(kT_d) &= Ce(kT_d) \\ y(kT_d + T_s) &= Ce(kT_d + T_s) \\ &\vdots \\ y(kT_d + (h-1)T_s) &= Ce(kT_d + (h-1)T_s) \end{aligned} \tag{5.6}$$

The solution of (5.4) during $[kT_d, (k+1)T_d)$ is

$$e(kT_d + t) = \Phi(t)e(kT_d) + \int_0^t \Phi(s)ds\hat{B}_\sigma \tag{5.7}$$

where $\Phi(t) = \exp\{A_\sigma t\}$.

Hence,

$$\begin{aligned} y(kT_d) &= Ce(kT_d) \\ y(kT_d + T_s) &= Ce(kT_d + T_s) \\ &= C\Phi(T_s)e(kT_d) + C\int_0^{T_s} \Phi(s)ds\hat{B}_\sigma \\ &\vdots \\ y(kT_d + (h-1)T_s) &= Ce(kT_d + (h-1)T_s) \\ &= C\Phi((h-1)T_s)e(kT_d) \\ &\quad + C\int_0^{(h-1)T_s} \Phi(s)ds\hat{B}_\sigma \end{aligned} \tag{5.8}$$

Define an augmented output

$$\bar{y}(k) \triangleq \begin{bmatrix} y(kT_d) \\ y(kT_d + T_s) \\ \vdots \\ y(kT_d + (h-1)T_s) \end{bmatrix} \in \Re^{hm \times 1}$$

Then, simple algebraic manipulation gives

$$\bar{y}(k) = \begin{bmatrix} C \\ C\Phi(T_s) \\ \vdots \\ C\Phi((h-1)T_s) \end{bmatrix} e(k) + \begin{bmatrix} 0 \\ C\int_0^{T_s}\Phi(s)ds\hat{B}_\sigma \\ \vdots \\ C\int_0^{(h-1)T_s}\Phi(s)ds\hat{B}_\sigma \end{bmatrix}$$

With this, a discrete model under multiple sampling can be obtained:

$$e(k+1) = \bar{A}_\sigma e(k) + \bar{B}_\sigma \tag{5.9}$$

$$\bar{y}(k) = \bar{C}_\sigma e(k) + \bar{D}_\sigma \tag{5.10}$$

where

$$\bar{A}_\sigma = \Phi(T_d) \qquad \bar{B}_\sigma = \int_0^T \Phi(s)ds\hat{B}_\sigma$$

$$\bar{C}_\sigma = \begin{bmatrix} C \\ C\Phi(T_s) \\ \vdots \\ C\Phi((h-1)T_s) \end{bmatrix} \qquad \bar{D}_\sigma = \begin{bmatrix} 0 \\ C\int_0^{T_s}\Phi(s)ds\hat{B}_\sigma \\ \vdots \\ C\int_0^{(h-1)T_s}\Phi(s)ds\hat{B}_\sigma \end{bmatrix}$$

Remark 5.1. It is stressed here that for output-feedback control, one should distinguish the dwell period T_d and sampling period T_s. For the switched affine system considered in this chapter, the switching signal only update after each dwell period. Hence, the switched error state model should be discretized based on the dwell period (T_d) rather than the sampling period (T_s).

5.3 Stabilization

In this section, a quadratic partition based on the augmented output $\bar{y}(k)$ is proposed as:

$$\Omega_i \triangleq \{\bar{y}(k) | \chi_i \triangleq \bar{y}^T(k)Q_{i1}\bar{y}(k) + Q_{i2}^T\bar{y}(k) + \bar{y}^T(k)Q_{i2} + Q_{i3} > 0\} \tag{5.11}$$

where $\forall i \in \Xi$, $Q_{i1} = Q_{i1}^T \in \Re^{hm\times hm}$, $Q_{i2} \in \Re^{hm\times 1}$, and $Q_{i3} \in \Re^{1\times 1}$.

The idea is that the state-space would be separated as different regions Ω_i by the partition and the subsystem of (5.9) is active only if the system state is in the corresponding region. A similar largest region function strategy as in [142] is adopted here to generate the switching signal:

$$\sigma = \arg\left(\max_{i\in\Xi} \chi_i\right) \tag{5.12}$$

By well-designed partitions, the error system will converge to the origin from any initial condition under the switching signal σ. To be specific, a desirable partition should fulfill the following conditions based on the theory of multiple Lyapunov functions [144] [145]:

1. An quadratic function $V_i(e) = e^T(k)P_ie(k)$ $(P_i = P_i^T)$ measuring the energy of each subsystem is positive-definite in region Ω_i.
2. The function $V_i(e)$ is decreasing when inside the region Ω_i.
3. When changing region (for example: from Ω_i to Ω_j), the energy doesn't increase, that is,

$$V_j(e) < V_i(e)$$

4. The partition covers the full state-space, that is,

$$\Omega_1 \bigcup \Omega_2 = \Re^n$$

Before proceeding, we present a technical lemma, which will be used frequently later.

Lemma 5.2. *(Finsler's Lemma [146]): Let $z \in \Re^n$, $P = P^T \in \Re^{n\times n}$, and $H \in \Re^{m\times n}$ such that $rank(H) = r < n$. The following statement are equivalent.*

1. *$z^T Pz < 0$, for all $z \neq 0$, $Hz = 0$;*
2. *$\exists X \in \Re^{n\times m}$ such that $P + XH + H^T X^T < 0$*

Then a sufficient condition for stability of the switched error system (5.9) under the proposed switching law is given in the following theorem.

Theorem 5.3. *If there exist symmetric matrices P_i, Q_{i1}, matrices E_i, G_i, F_i, E_{ij}, G_{ij}, and F_{ij}, vector Q_{i2}, scalars Q_{i3}, α, β, η_i, ρ_i, θ_i, θ_{ij}, θ_{ii}, ω_i, where $i, j \in \Xi$, $i \neq j$, such that matrices inequalities (5.13)-(5.17) hold, then the switched error system (5.9) under the switching law (5.12) is stable.*

$$\begin{bmatrix} \alpha I - P_i + \eta_i \bar{C}_i^T Q_{i1} \bar{C}_i & \eta_i \left(\bar{C}_i^T Q_{i1} \bar{D}_i + \bar{C}_i^T Q_{i2}\right) \\ * & \eta_i \left(\bar{D}_i^T Q_{i1} \bar{D}_i + \bar{D}_i^T Q_{i2} + Q_{i2}^T \bar{D}_i + Q_{i3}\right) \end{bmatrix} \leq 0 \tag{5.13}$$

$$\begin{bmatrix} P_i - \beta I + \rho_i \bar{C}_i^T Q_{i1} \bar{C}_i & \rho_i \left(\bar{C}_i^T Q_{i1} \bar{D}_i + \bar{C}_i^T Q_{i2}\right) \\ * & \rho_i \left(\bar{D}_i^T Q_{i1} \bar{D}_i + \bar{D}_i^T Q_{i2} + Q_{i2}^T \bar{D}_i + Q_{i3}\right) \end{bmatrix} \leq 0 \tag{5.14}$$

$$\begin{bmatrix} P_i - E_i - E_i^T & E_i\bar{A}_i - G_i^T & E_i\bar{B}_i - F_i^T \\ * & -P_i + \upsilon I + G_i\bar{A}_i + \bar{A}_i^T G_i^T + \theta_i \bar{C}_i^T Q_{i1} \bar{C}_i & G_i\bar{B}_i + \bar{A}_i^T F_i^T + \theta_i (\bar{C}_i^T Q_{i1} \bar{D}_i + \bar{C}_i^T Q_{i2}) \\ * & * & F_i\bar{B}_i + \bar{B}_i^T F_i^T + \theta_i \left(\bar{D}_i^T Q_{i1} \bar{D}_i + \bar{D}_i^T Q_{i2} + Q_{i2}^T \bar{D}_i + Q_{i3}\right) \end{bmatrix} < 0 \tag{5.15}$$

$$\begin{bmatrix} \begin{pmatrix} P_j - P_i - E_{ij} - E_{ij}^T \\ +\theta_{ij} \bar{C}_i^T Q_{j1} \bar{C}_i \end{pmatrix} & E_{ij}\bar{A}_i - G_{ij}^T & E_{ij}\bar{B}_i - F_{ij}^T + \theta_{ij} \left(\bar{C}_i^T Q_{j2} \bar{D}_i + \bar{C}_i^T Q_{j2}\right) \\ * & \begin{pmatrix} G_{ij}\bar{A}_i + \bar{A}_i^T G_{ij}^T \\ +\theta_{ii} \bar{C}_i^T Q_{i1} \bar{C}_i \end{pmatrix} & G_{ij}\bar{B}_i + \bar{A}_i^T F_{ij}^T + \theta_{ii} \left(\bar{C}_i^T Q_{i2} \bar{D}_i + \bar{C}_i^T Q_{i2}\right) \\ * & * & \begin{pmatrix} F_{ij}\bar{B}_i + \bar{B}_i^T F_{ij}^T + \theta_{ij} \left(\bar{D}_i^T Q_{j1} \bar{D}_i + \bar{D}_i^T Q_{j2} + Q_{j2}^T \bar{D}_i + Q_{j3}\right) \\ +\theta_{ii} \left(\bar{D}_i^T Q_{i1} \bar{D}_i + \bar{D}_i^T Q_{i2} + Q_{i2}^T \bar{D}_i + Q_{i3}\right) \end{pmatrix} \end{bmatrix} < 0 \tag{5.16}$$

$$\omega_1 \begin{bmatrix} Q_{i1} & Q_{i2} \\ * & Q_{i3} \end{bmatrix} + \omega_2 \begin{bmatrix} Q_{j1} & Q_{j2} \\ * & Q_{j3} \end{bmatrix} \geq 0 \tag{5.17}$$

Proof. In the following, we show that the four conditions aforementioned are satisfied.

Condition **1)** is satisfied if

$$\alpha_i ||e(k)||^2 \leq V_i(e(k)) \leq \beta_i ||e(k)||^2 \tag{5.18}$$

holds for all $\bar{y}(k) \in \Omega_i$.

Applying the S-procedure [147], this is equivalent to the following inequalities:

$$\begin{aligned} &\alpha_i e^T(k) I e(k) - e^T(k) P_i e(k) \\ &\quad + \eta_i (\bar{y}^T(k) Q_{i1} \bar{y}(k) + Q_{i2}^T \bar{y}(k) + \bar{y}^T(k) Q_{i2} + Q_{i3}) \leq 0 \end{aligned} \tag{5.19}$$

$$\begin{aligned} &e^T(k) P_i e(k) - \beta_i e^T(k) I e(k) \\ &\quad + \rho_i (\bar{y}^T(k) Q_{i1} \bar{y}(k) + Q_{i2}^T \bar{y}(k) + \bar{y}^T(k) Q_{i2} + Q_{i3}) \leq 0 \end{aligned} \tag{5.20}$$

Define $\xi(k) = \begin{bmatrix} e^T(k) & 1 \end{bmatrix}^T$, $\alpha = \min\{\alpha_i\}$, and $\beta = \max\{\beta_i\}$. Then inequalities (5.19) and (5.20) are equivalent to (5.13) and (5.14) respectively after substituting equation (5.10).

Condition **2)** is satisfied if

$$\Delta V_i(e(k)) = V_i(e(k+1)) - V(e(k)) \leq -\upsilon ||e(k)||^2 \tag{5.21}$$

for all $\bar{y}(k) \in \Omega_i$ and $e(k+1) = \bar{A}_i e(k) + \bar{B}_i$, during $[k, k+1)$.

Let $z(k+1) = [e^T(k+1)\ e^T(k)\ 1]^T$, $H = \begin{bmatrix} -I & \bar{A}_i & \bar{B}_i \end{bmatrix}$; then

$$Hz(k+1) = 0 \tag{5.22}$$

With this notation, the above condition becomes:

$$z^T(k+1) P z(k+1) < 0 \tag{5.23}$$

for all $\bar{y}(k) \in \Omega_i$ and $z(k+1)$ satisfying (5.22), where

$$P = \begin{bmatrix} P_i & 0 & 0 \\ * & -P_i + \upsilon I & 0 \\ * & * & 0 \end{bmatrix}$$

Furthermore, let $X = [E_i^T \; G_i^T \; F_i^T]^T$. Applying the Finsler's Lemma, (5.23) is equivalent to:

$$P + XH + H^T X^T < 0 \tag{5.24}$$

for some X and all $\bar{y}(k) \in \Omega_i$.

Using equation (5.10), $\bar{y}(k) \in \Omega_i$ is equivalent to

$$z^T(k)\Lambda z(k) > 0 \tag{5.25}$$

where

$$\Lambda = \begin{bmatrix} 0 & 0 & 0 \\ * & \bar{C}_i^T Q_{i1} \bar{C}_i & \bar{C}_i^T Q_{i1} \bar{D}_i + \bar{C}_i^T Q_{i2} \\ * & * & \bar{D}_i^T Q_{i1} \bar{D}_i + \bar{D}_i^T Q_{i2} + Q_{i2}^T \bar{D}_i + Q_{i3} \end{bmatrix}$$

Applying the S-procedure yields that (5.24) and (5.25) hold if (5.15) holds.

Condition **3)** holds if

$$e^T(k)(P_j - P_i)e(k) < 0 \tag{5.26}$$

for $\bar{y}(k) \in \Omega_j$, $\bar{y}(k-1) \in \Omega_i$.

This condition is further equivalent to:

$$z^T(k)\hat{P}z(k) < 0 \tag{5.27}$$

for $\bar{y}(k-1) \in \Omega_i$ and $\bar{y}(k) \in \Omega_j$, and $z(k)$ satisfying (5.22), where

$$\hat{P} = \begin{bmatrix} P_j - P_i & 0 & 0 \\ * & 0 & 0 \\ * & * & 0 \end{bmatrix}$$

Furthermore, let $X = [E_{ij}^T \; G_{ij}^T \; F_{ij}^T]^T$. Applying the Finsler's Lemma, (5.27) is equivalent to:

$$\hat{P} + \hat{X}H + H^T \hat{X}^T < 0 \tag{5.28}$$

for some $\hat{X}$ and

$$z^T(k)\Lambda_i z(k) > 0 \tag{5.29}$$

where

$$\Lambda_i = \begin{bmatrix} 0 & 0 & 0 \\ * & \bar{C}_i^T Q_{i1} \bar{C}_i & \bar{C}_i^T Q_{i1} \bar{D}_i + \bar{C}_i^T Q_{i2} \\ * & * & \bar{D}_i^T Q_{i1} \bar{D}_i + \bar{D}_i^T Q_{i2} + Q_{i2}^T \bar{D}_i + Q_{i3} \end{bmatrix}$$

$$z^T(k)\Lambda_j z(k) > 0 \tag{5.30}$$

where

$$\Lambda_j = \begin{bmatrix} \bar{C}_i^T Q_{j1} \bar{C}_i & 0 & \bar{C}_i^T Q_{j1} \bar{D}_i + \bar{C}_i^T Q_{i2} \\ * & 0 & 0 \\ * & * & \bar{D}_i^T Q_{j1} \bar{D}_i + \bar{D}_i^T Q_{j2} + Q_{j2}^T \bar{D}_i + Q_{j3} \end{bmatrix}$$

Applying the S-procedure yields that (5.28), (5.29), and (5.30) hold if (5.16) holds.

4) The covering condition can be proved by contradiction. Assume that there is an output $\bar{y}(k)$ does not belong to any Ω_i, i.e.,

$$\bar{y}^T(k) \begin{bmatrix} Q_{i1} & Q_{i2} \\ * & Q_{i3} \end{bmatrix} \bar{y}(k) < 0 \tag{5.31}$$

Multiplying positive constants ω_i and summing up, we have:

$$\omega_1 \bar{y}^T(k) \begin{bmatrix} Q_{11} & Q_{12} \\ * & Q_{13} \end{bmatrix} \bar{y}(k) + \omega_2 \bar{y}^T(k) \begin{bmatrix} Q_{21} & Q_{22} \\ * & Q_{23} \end{bmatrix} \bar{y}(k) < 0$$

which contradicts condition (5.17). Hence if (5.17) is satisfied, the regions Ω_i cover the whole state-space. □

Remark 5.4. The online implement procedure is shown in Figure 5.3. For each dwell period $([kT_d, (k+1)T_d))$, it can be divided into two part. During $[kT_d, kT_d + (h-1)T_s]$, the multiple sampling technique is applied, and the augment output $\bar{y}(k)$ can be obtained. Then during $(kT_d + (h-1)T_s, (k+1)T_d)$ period, the switch signal is computed. At the end of this dwell period, the switching signal is updated.

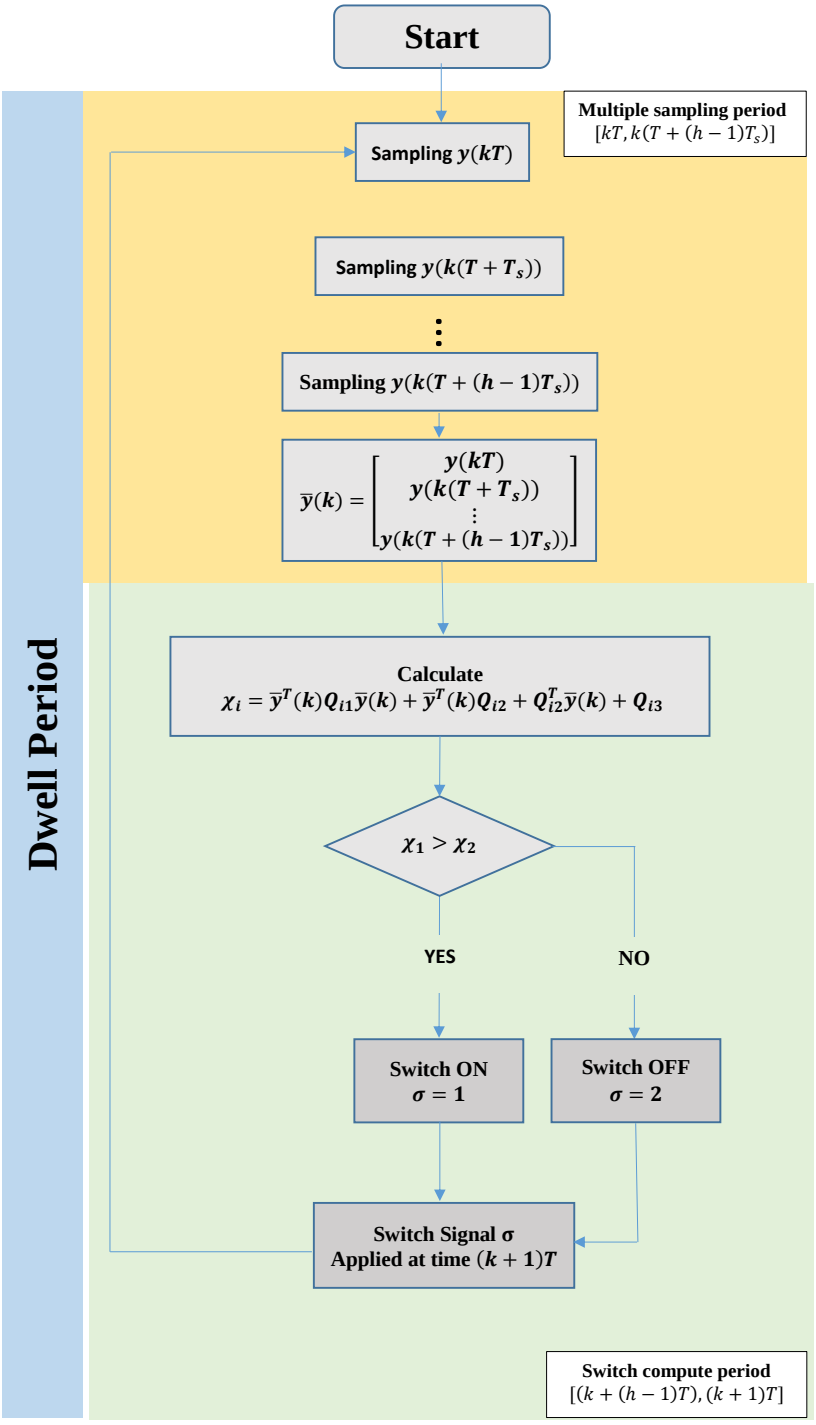


Figure 5.3: Flowchart of the proposed output feedback control

5.4 Simulation Results

Simulation results are shown below to illustrate the performance of the designed switching controllers on the buck converter (Figure 5.1a) and the Ćuk converters (Figure 5.1d). The simulations are conducted using Matlab.

5.4.1 Buck Converter

The parameters for the buck converter are: $V_g = 30V$, $L = 60mH$, $C = 880\mu F$, $R = 5\Omega$. The sampling frequency $f = 10kHz$, hence, $T_s = 1/f$. The equilibrium is set as $x_e = [13.516\ 2.705]^T$.

5.4.1.1 State Feedback Control

For the first case, if both inductor current i_L and capacitor voltage v_c can be measured and the dwell time T_d is equal to the sampling period T_s, it becomes a state feedback control problem $(m = 2, h = 1)$. According to Theorem 5.3, if the matrices conditions ((5.13)-(5.17)) can be satisfied, the state feedback switching law $\sigma = \arg(\max_{i\in\Xi} \chi_i)$ can be applied to the buck converter. After griding up all the unknown scalars in Theorem 5.3, the matrices conditions become a LMI problem which can be solved by Matlab LMI toolbox. The precalculation is done off-line. Then, a state-space partition based on $e(k)$ is obtained as follow:

$$\chi_i = \left\{ e(k) | e^T(k) Q_{i1} e(k) + Q_{i2}^T e(k) + e^T(k) Q_{i2} + Q_{i3} > 0 \right\} \quad i = 1,2 \tag{5.32}$$

where

$$Q_{11} = \begin{bmatrix} -0.25423 & 0.25601 \\ 0.25601 & -0.25791 \end{bmatrix} \qquad Q_{21} = \begin{bmatrix} 0.25431 & -0.25609 \\ -0.25609 & 0.25799 \end{bmatrix}$$

$$Q_{12} = \begin{bmatrix} 2.726 \\ -2.7343 \end{bmatrix} \qquad Q_{22} = \begin{bmatrix} -2.726 \\ 2.7343 \end{bmatrix}$$

$$Q_{13} = \begin{bmatrix} 0.14709 \end{bmatrix} \qquad Q_{23} = \begin{bmatrix} -0.010578 \end{bmatrix}$$

Hence, the responses of the output voltage v_C and inductor current i_L are shown in Figure 5.4.

5.4.1.2 Output feedback control

It is assumed that only the inductor current i_L can be measured. The sampling period is fixed $(T_s = 1/f)$. When $h > 1$, as defined above, the dwell time is $T_d = hT_s$. In each dwell period, the

inductor current is sampled h times. For brevity, we only compare the results when $h = 1,2,3,4$. Hence, the partition based on the augmented output $\bar{y}(k)$ is as follow:

$$\chi_i = \left\{ \bar{y}(k) | \bar{y}^T(k) Q_{i1} \bar{y}(k) + Q_{i2}^T \bar{y}(k) + \bar{y}^T(k) Q_{i2} + Q_{i3} > 0 \right\} \tag{5.33}$$

where

1. $m = 1, h = 1$**: Dwell time** $T_d = 2T_s$
   The BMI problem is infeasible.

2. $m = 1, h = 2$**: Dwell time** $T_d = 2T_s$

$$Q_{11} = \begin{bmatrix} -512.6000 & 514.2500 \\ 514.2500 & -515.9200 \end{bmatrix} \qquad Q_{21} = \begin{bmatrix} 514.0400 & -515.7000 \\ -515.7000 & 517.3700 \end{bmatrix}$$
$$Q_{12} = \begin{bmatrix} 513.5800 \\ -513.9600 \end{bmatrix} \qquad Q_{22} = \begin{bmatrix} -513.5700 \\ 513.9600 \end{bmatrix}$$
$$Q_{13} = \begin{bmatrix} 2.7986 \end{bmatrix} \qquad Q_{23} = \begin{bmatrix} -0.2008 \end{bmatrix}$$

3. $m = 1, h = 3$**: Dwell time** $T_d = 3T_s$

$$Q_{11} = 10^6 \begin{bmatrix} 30.5950 & -61.0250 & 30.4300 \\ -61.0250 & 121.7200 & -60.6940 \\ 30.4300 & -60.6940 & 30.2630 \end{bmatrix}$$
$$Q_{21} = 10^6 \begin{bmatrix} 30.0580 & -60.7530 & 30.6970 \\ -60.7530 & 122.7900 & -62.0380 \\ 30.6970 & -62.0380 & 31.3430 \end{bmatrix}$$

$$Q_{12} = 10^6 \begin{bmatrix} -155.3400 \\ 311.8900 \\ -156.5600 \end{bmatrix} \qquad Q_{22} = 10^6 \begin{bmatrix} 155.3400 \\ -311.8900 \\ 156.5500 \end{bmatrix}$$
$$Q_{13} = 10^3 \begin{bmatrix} 7.7602 \end{bmatrix} \qquad Q_{23} = 10^3 \begin{bmatrix} -1.0004 \end{bmatrix}$$

4. $m = 1, h = 4$**: Dwell time** $T_d = 4T_s$

$$Q_{11} = 10^6 \begin{bmatrix} 52.8310 & -70.2830 & -18.8240 & 36.4290 \\ -70.2830 & 121.9300 & -32.0280 & -20.0790 \\ -18.8240 & -32.0280 & 121.2500 & -69.9470 \\ 36.4290 & -20.0790 & -69.9470 & 53.4460 \end{bmatrix}$$

$$Q_{21} = 10^6 \begin{bmatrix} 53.3790 & -70.1290 & -20.0260 & 36.6250 \\ -70.1290 & 120.6500 & -30.8590 & -19.2110 \\ -20.0260 & -30.8590 & 122.1200 & -71.6930 \\ 36.6250 & -19.2110 & -71.6930 & 54.4300 \end{bmatrix}$$

$$Q_{12} = 10^6 \begin{bmatrix} -198.2000 \\ 199.3600 \\ 198.2000 \\ -199.3700 \end{bmatrix}$$

$$Q_{22} = 10^6 \begin{bmatrix} 198.2000 \\ -199.3600 \\ -198.2000 \\ 199.3600 \end{bmatrix}$$

$$Q_{13} = 10^3 \begin{bmatrix} 10.8690 \end{bmatrix}$$

$$Q_{23} = 10^3 \begin{bmatrix} -1.6963 \end{bmatrix}$$

Therefore, we can follow the online implementation procedure as Figure 5.3. Even if only the inductor current is sampled, the responses of both inductor current i_L and capacitor voltage v_C are drawn in Figure 5.5, and the above state feedback control results are also included. After observing zoomed results in the steady part (Figure 5.6), it can be seen that:

- Under single sampling, a state-feedback controller can be found using the proposed approach, while an output-feedback one cannot. If the multiple sampling technique is applied, then the output-feedback case becomes feasible.
- When the dwell time $T_d = 2T_s$, the responses of the buck converter are exactly same between output feedback control and state feedback control. The difference is that the inductor current i_L has been sampled twice during each dwell time under output feedback control, but for state feedback control, the inductor current and capacitor voltage are sampled only at the beginning of each dwell time.
- When the dwell time is increased to $3T_s$ and $4T_s$, the inductor current can be sampled three times and four times respectively. The transition performance with different samplings are quite similar. The only difference is that the ripple is slightly larger when sampling times increase. However, the extended dwell period results in a lower average switching frequency, which can improve the energy efficiency (higher priority in converter design)

because more power is lost in the switching mode than the conduction mode for the power semiconductor.

5.4.1.3 Comparison with other control schemes

In this subsection, the proposed output feedback control approach ($m = 1, h = 2$) is also compared with the traditional industry-standard PI-type controller tuned on the basis of a linearized averaged model (averaged control scheme) [141] , the MPC controller in Charpter 3.2 and the prediction based sampling-data controller in Charpter 4. For MPC controller, the prediction horizon has been set to 1 step and 2 step. Simulation results are shown in Figure 5.7. Because for the buck converter, people are always concerned more about the voltage output, for brevity, only the response of the capacitor voltage is compared. It should be stressed that the sampling frequency has been set as $10kHz$. We tried to compare the performance of different controllers under relative low switching frequency.

- Both the proposed output feedback controller and the controller in Charpter 4 have excellent transition performance with no overshoot. The transition period are longest and overshoot is largest for the PI controller.
- In steady state, the ripple of the proposed output feedback controller, the MPC controllers and the PI controller are almost same. However, the output voltage has larger ripple under the controller of Charter 4, which is different from the performance under high sampling and switching frequency.

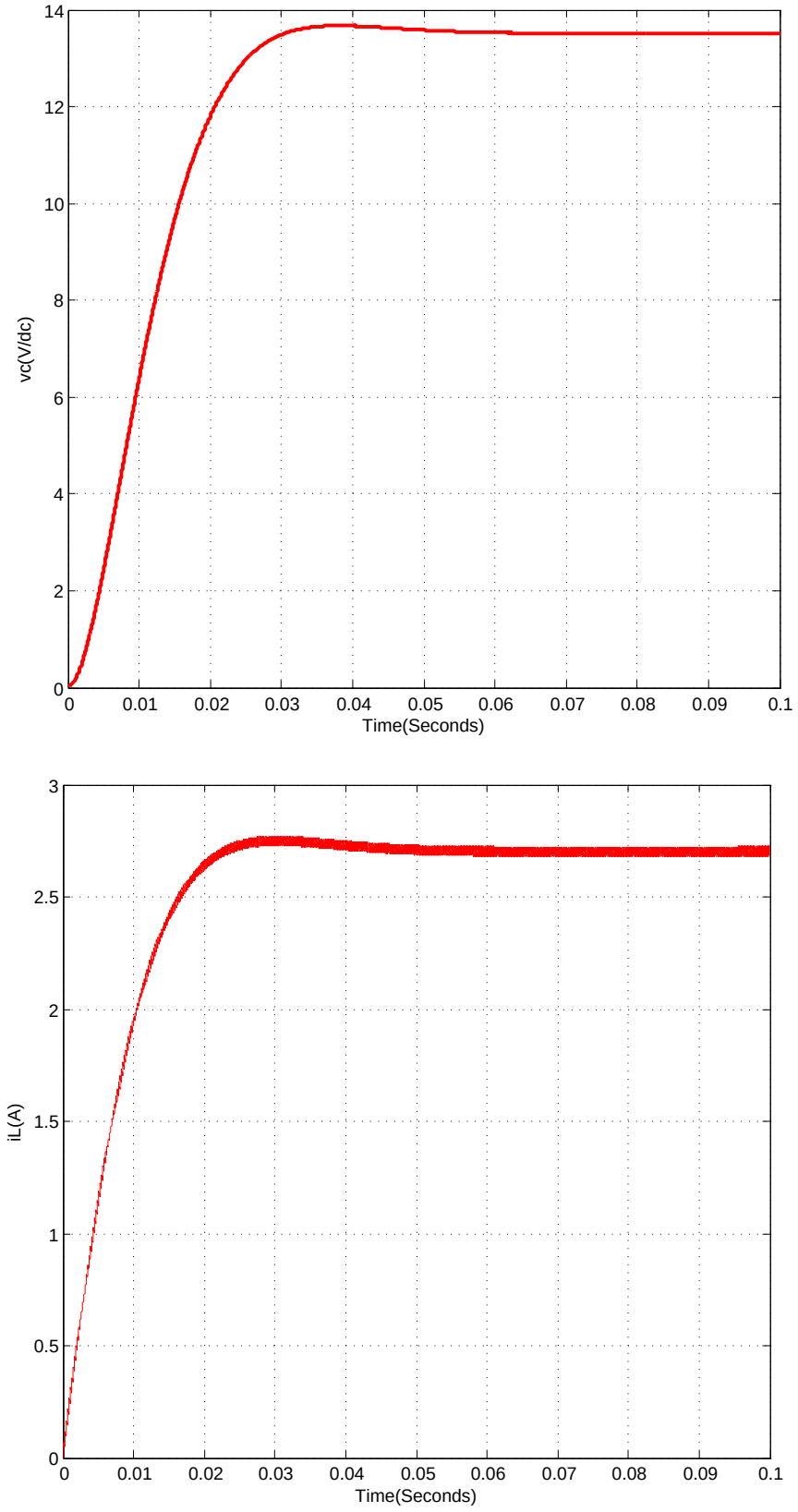


Figure 5.4: The responses of v_C and i_L under state feedback control (Buck converter)

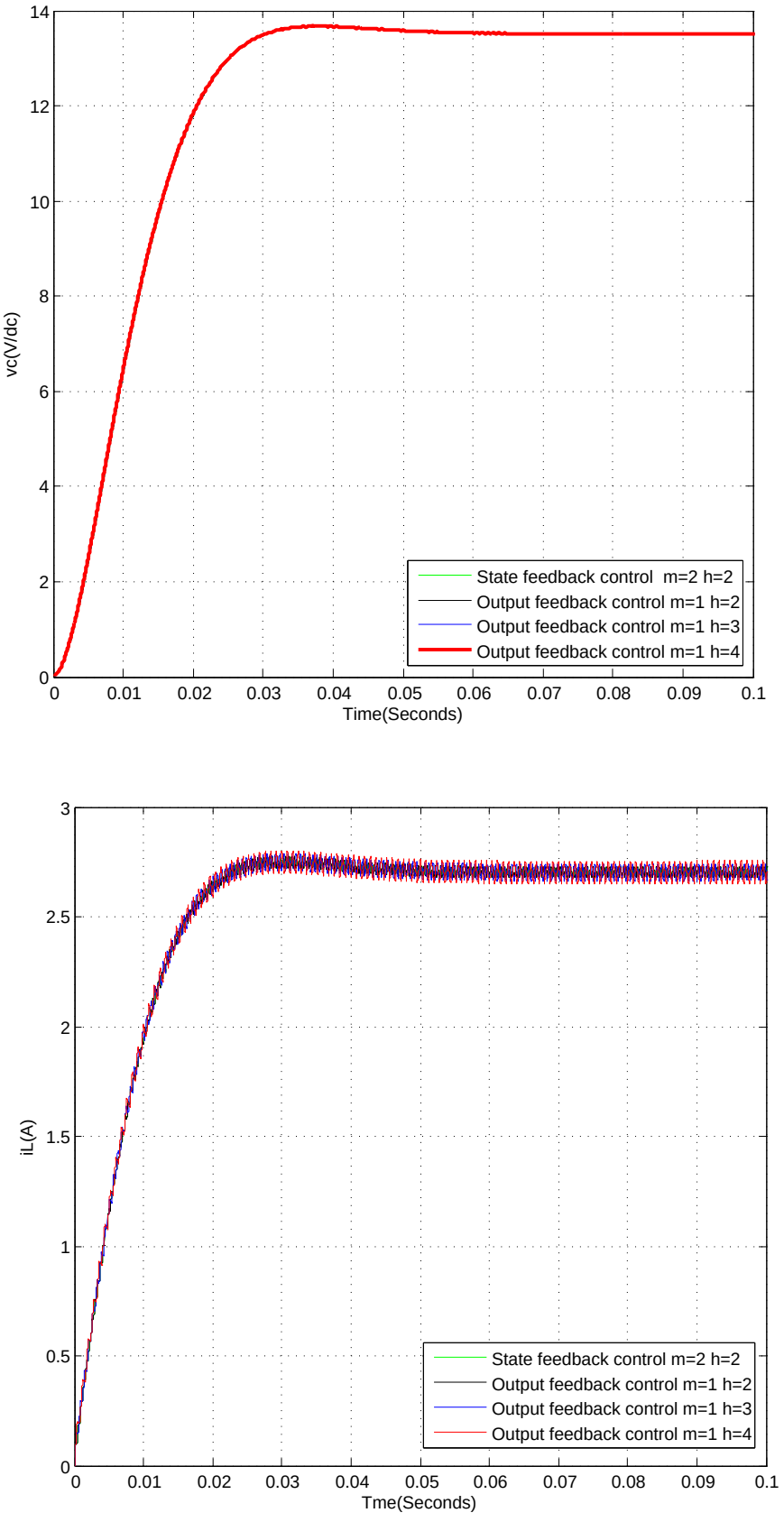


Figure 5.5: The responses of v_C and i_L under output feedback control (Buck converter)

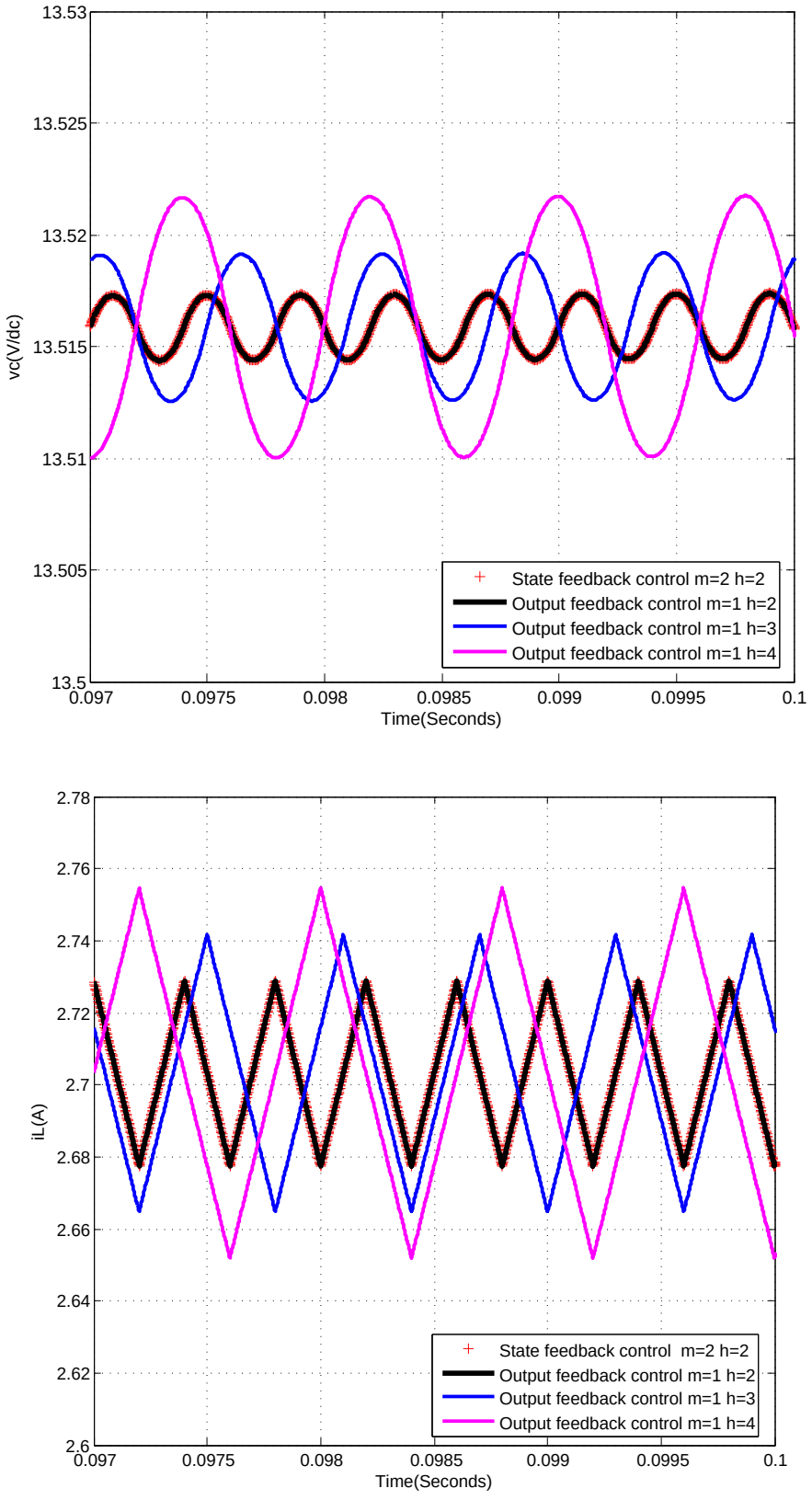


Figure 5.6: The zoomed responses of v_C and i_L under output feedback control(Buck converter)

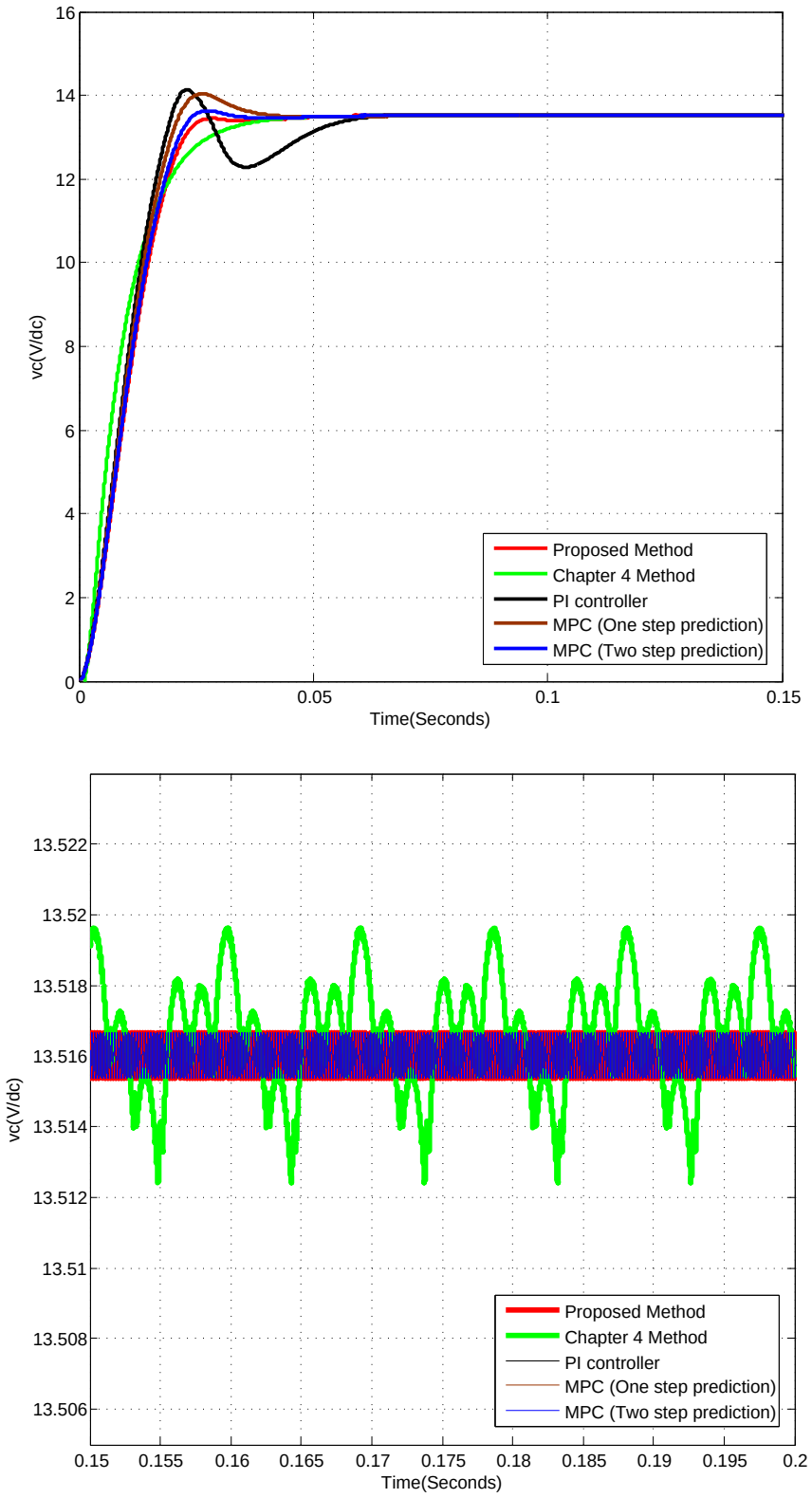


Figure 5.7: The response of v_C and zoomed under different control scheme (Buck converter)

5.4.2 Ćuk Converter

The parameters for the Ćuk converters are: $V_g = 25V$, $L_1 = 1mH$, $L_2 = 2mH$, $C_1 = 100\mu F$, $C_2 = 1mF$, $R = 3\Omega$. The sampling frequency $f = 100kHz$, hence, $T_s = 1/f$. The equilibrium is set as $x_e = [17.50 \ -12.00 \ 62.5 \ -36.00]^T$. The same technique has been used to solve the BMIs, that is , gridding up the unknown scalars in Theorem 5.3 and solving the corresponding LMI problem.

5.4.2.1 State Feedback Control

Firstly, we assume the full state $[i_{L1}, i_{L2}, v_{C1}, v_{C2}]^T$ is measured. The dwell time $T = T_s$. Hence, it is a state feedback control problem $(m = 4, h = 1)$. A feasible solution has been obtained. The parameters for the partition (5.11) based on error state $e(k)$ are as follow:

$$Q_{11} = \begin{bmatrix} 0 & 0.0116 & 0.0087 & 0.0162 \\ 0.0116 & -0.0043 & -0.0057 & -0.0311 \\ 0.0087 & -0.0057 & 0.0067 & -0.0296 \\ 0.0162 & -0.0311 & -0.0296 & 0.0832 \end{bmatrix}$$

$$Q_{21} = \begin{bmatrix} 0.0774 & -0.0975 & -0.0204 & 0.0278 \\ -0.0975 & 0.1359 & 0.0200 & -0.0397 \\ -0.0204 & 0.0200 & -0.0077 & 0.0313 \\ 0.0278 & -0.0397 & 0.0313 & 0.0728 \end{bmatrix}$$

$$Q_{12} = \begin{bmatrix} -4.9080 \\ 5.4124 \\ 2.7602 \\ -1.5358 \end{bmatrix} \qquad Q_{22} = \begin{bmatrix} 7.1887 \\ -7.8609 \\ -4.0688 \\ 2.4948 \end{bmatrix}$$

$$Q_{13} = \begin{bmatrix} 0.1573 \end{bmatrix} \qquad Q_{23} = \begin{bmatrix} 0.1573 \end{bmatrix}$$

Therefore, the state feedback switching controller $\sigma = \arg(\max_{i \in \Xi} \chi_i)$ can be implemented on the Ćuk converters.

5.4.2.2 Output feedback control

In this subsection, we assume that only the two inductor current i_{L1} and i_{L2} can be measured. The sampling period is fixed $(T_s = 1/f)$. When $h > 1$, as defined above, the dwell time $T_d = hT_s$. In each dwell period, both inductor currents are sampled h times. Here, we only compare the results when $h = 1, 2, 3$. The measured output:

$$y(k) = Ce(k)$$

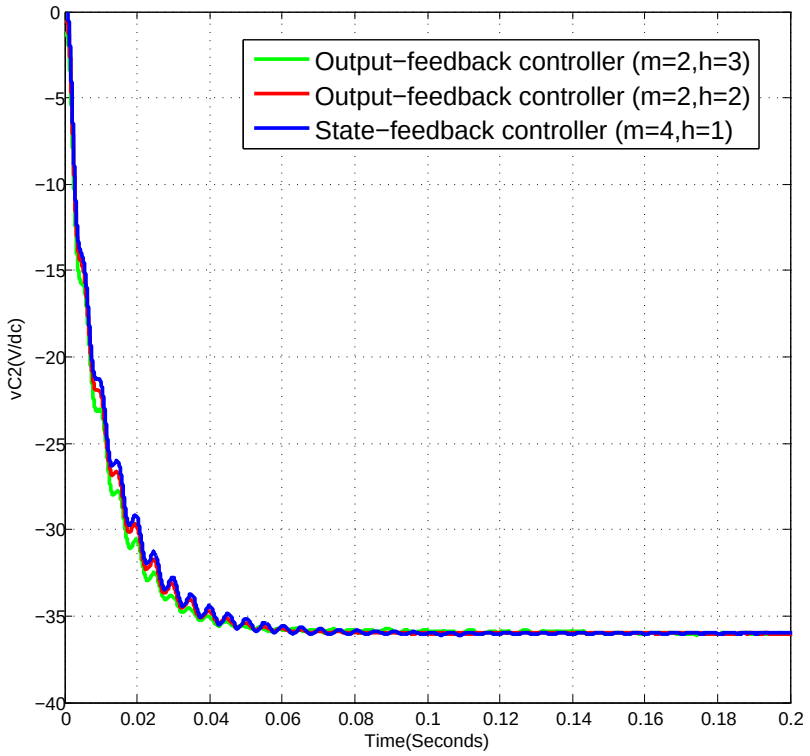


Figure 5.8: The response of v_{C2} for the Ćuk converters under output feedback control

where

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$$

Hence, the augmented output:

$$\bar{y}[k] = \begin{bmatrix} y(k) \end{bmatrix} \quad \text{for } h = 1$$

$$\bar{y}[k] = \begin{bmatrix} y(k) \\ y(k+T_s) \end{bmatrix} \quad \text{for } h = 2$$

$$\bar{y}[k] = \begin{bmatrix} y(k) \\ y(k+T_s) \\ y(k+2T_s) \end{bmatrix} \quad \text{for } h = 3$$

Based on the corresponding augmented output $\bar{y}(k)$, the partition is as follow:

$$\chi_i = \left\{ \bar{y}(k) | \bar{y}^T(k) Q_{i1} \bar{y}(k) + Q_{i2}^T \bar{y}(k) + \bar{y}^T(k) Q_{i2} + Q_{i3} > 0 \right\} \tag{5.34}$$

where

1. m=2, h=1: **Dwell time** $T_d = T_s$
   The BMI problem is infeasible.

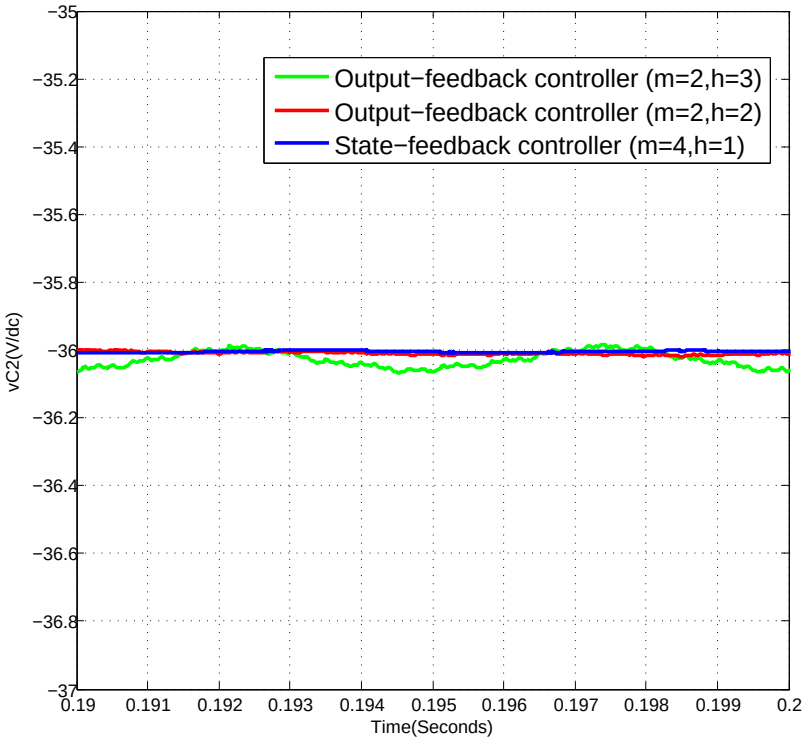


Figure 5.9: Zoomed of the response of v_{C2} for the Ćuk converters under output feedback control

2. m=2, h=2: **Dwell time** $T_d = 2T_s$

$$Q_{11} = 10^6 \begin{bmatrix} 1.7732 & -0.1953 & -1.7826 & 0.1796 \\ -0.1953 & 1.1332 & -0.6999 & -1.6548 \\ -1.7826 & -0.6999 & 1.7818 & 0.7137 \\ 0.1796 & -1.6548 & 0.7137 & 2.1776 \end{bmatrix}$$

$$Q_{21} = 10^6 \begin{bmatrix} -0.8097 & 0.1942 & 0.8160 & -0.1863 \\ 0.1942 & -0.1677 & 0.7065 & 0.6882 \\ 0.8160 & 0.7065 & -0.8121 & -0.7125 \\ -0.1863 & 0.6882 & -0.7125 & -1.2099 \end{bmatrix}$$

$$Q_{12} = 10^6 \begin{bmatrix} 6.4448 \\ -0.0262 \\ -6.4657 \\ -0.0262 \end{bmatrix} \qquad Q_{22} = 10^6 \begin{bmatrix} -6.4448 \\ 0.0262 \\ 6.4657 \\ 0.0262 \end{bmatrix}$$

$$Q_{13} = 10^6 \begin{bmatrix} 1.3902 \end{bmatrix} \qquad Q_{23} = 10^6 \begin{bmatrix} 0.5427 \end{bmatrix}$$

3. m=2, h=3: **Dwell time** $T_d = 3T_s$

$$Q_{11} = 10^7 \begin{bmatrix} 4.1802 & 0.0235 & -2.4665 & -0.0711 & -3.1336 & 0.0296 \\ 0.0235 & -0.1338 & 0.0218 & 0.3314 & -0.0353 & -0.1518 \\ -2.4665 & 0.0218 & 1.3506 & 0.0041 & 3.9387 & 0.0101 \\ -0.0711 & 0.3314 & 0.0041 & -0.7913 & 0.0469 & 0.3681 \\ -3.1336 & -0.0353 & 3.9387 & 0.0469 & -2.2081 & -0.0296 \\ 0.0296 & -0.1518 & 0.0101 & 0.3681 & -0.0296 & -0.1704 \end{bmatrix}$$

$$Q_{21} = 10^7 \begin{bmatrix} -3.8800 & -0.0235 & 2.3148 & 0.0711 & 2.9851 & -0.0296 \\ -0.0235 & 0.2095 & -0.0218 & -0.4830 & 0.0353 & 0.2276 \\ 2.3148 & -0.0218 & -1.0471 & -0.0041 & -4.0904 & -0.0101 \\ 0.0711 & -0.4830 & -0.0041 & 1.0947 & -0.0469 & -0.5198 \\ 2.9851 & 0.0353 & -4.0904 & -0.0469 & 2.5083 & 0.0296 \\ -0.0296 & 0.2276 & -0.0101 & -0.5198 & 0.0296 & 0.2463 \end{bmatrix}$$

$$Q_{12} = 10^8 \begin{bmatrix} -2.5404 \\ -0.0354 \\ 5.1175 \\ 0.0708 \\ -2.5774 \\ -0.0354 \end{bmatrix} \qquad Q_{22} = 10^8 \begin{bmatrix} 2.5441 \\ 0.0354 \\ -5.1175 \\ -0.0708 \\ 2.5738 \\ 0.0354 \end{bmatrix}$$

$$Q_{13} = 10^5 \begin{bmatrix} -3.1568 \end{bmatrix} \qquad Q_{23} = 10^5 \begin{bmatrix} 5.0805 \end{bmatrix}$$

Therefore, we can follow the online implementation procedure as Figure 5.3. Because for DC-DC Ćuk converters the output voltage v_{C2} is the state to be controlled, for brevity, we only present the response of v_{C2} under the two designed output feedback controllers and state feedback controller above as shown in Figure 5.8 and Figure 5.9. In Table 5.2, these proposed

Table 5.2: Results under different operation conditions

	State feedback	Output feedback		
m	4	2		
h	1	1	2	3
f_s	$100kHz$	$100kHz$	$100kHz$	$100kHz$
T_s	$10ns$	$10ns$	$10ns$	$10ns$
T_d	$10ns$	$10ns$	$20ns$	$30ns$
Feasibility	$\surd$	$\times$	$\surd$	$\surd$
Output Ripple	$4mV$ (0.01%)	N/A	$9mV$ (0.03%)	$77mV$ (0.21%)

controllers are compared from several aspects:

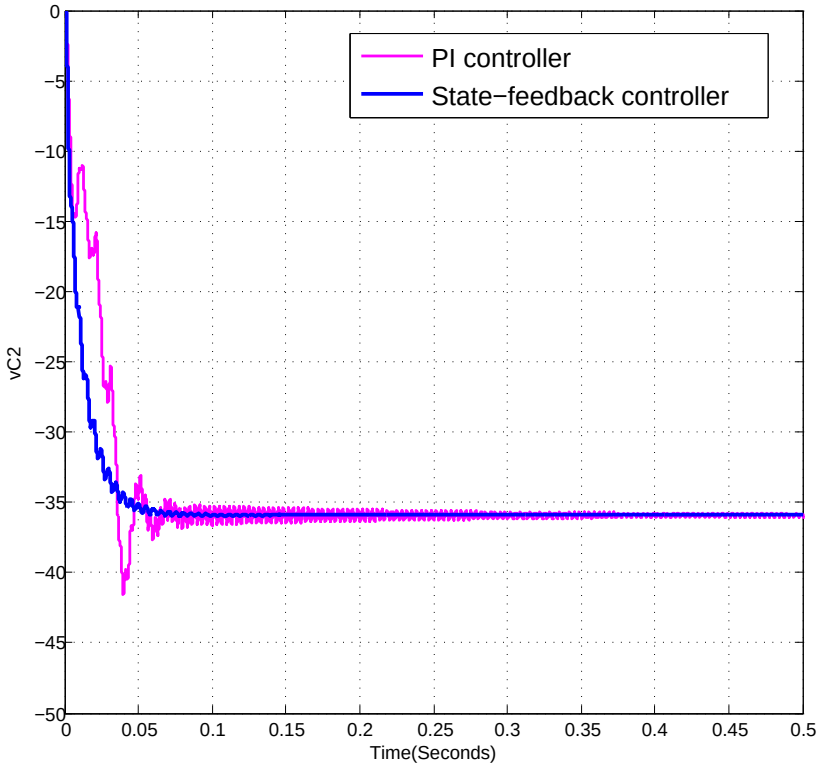


Figure 5.10: The responses of v_{C2} under the proposed controller and a PI controller

1. Under single sampling, a state-feedback controller can be found using the proposed approach, while an output-feedback one cannot. If the multiple sampling technique is applied, then the output-feedback case becomes feasible.

2. If the sampling period T_s is fixed, the dwell period T_d can be longer by sampling three-times ($m = 2, h = 3$) than twice ($m = 2, h = 2$). The transition performance with different samplings are quite similar as shown in Figure 5.8. The only difference is that the ripple for $h = 3$ is slightly larger than that for $h = 2$. The increase in ripple is still acceptable as the most industrial standards require only that the ripple is less than 1% [148]. However, the extended dwell period results in a lower switching frequency, which can improve the energy efficiency (higher priority in converter design) because more power is lost in the switching mode than the conduction mode for the power semiconductor.

5.4.2.3 Comparison Between the Proposed Method and PI Controller

In this section, the proposed method ($m = 4, h = 1$) is further compared with a PI controller from [148]. The PI controller is based on a conventional small-signal model. The responses of v_{C_2} under both controllers are shown in Figure 5.10. It can be seen that the proposed method shows better transition performance over the PI controller. What's more, there is no systematic method that can guide the tuning procedure of the PI controller for this 4^{th} order system.

5.5 Summary

It is easy to know that the nature of the control scheme developed in Chapter 4 is to partition the state-space into different regions in a specific way that is based on the fastest decrease direction of the Lypanouv function. A specific switching signal will be generated to activate the corresponding mode when the current state enters each region. The switching law is state-dependent, which requires the full state is measurable. In this Chapter, to compensate the information loss due to limited access to the state, a multiple sampling scheme is employed to derive a discrete-time switched affine model with an augmented measurement output. Based on the model, an output-feedback switching control law, which drives the system state to a set of attainable switched equilibria, is synthesized by using a quadratic state-space partition. The multiple sampling scheme not only facilitates the controller synthesis, but also improves the energy efficiency of the converter by allowing a lower switching frequency. Numerical examples and simulations are provided to demonstrate the effectiveness and merits of the proposed approach.

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Part II

DC-AC Converters

Chapter 6

Switching Control of Grid-Connected Three-Phase DC-AC Inverters

In the first Part of this thesis, hybrid modelling and switching control techniques have been proposed for the DC-DC converters. In this chapter, these technique will be extended to a more complicated case:a three-phase grid-connected DC-AC inverter. The main difficulty to this kind of extension are:

- There are six power switches for a three-phase inverter. Hence, there are eight possible switching states, while DC-DC converters normally only have two switching states.
- In term of current control, the currents of the three-phase inverter are controlled to track three-phase sinusoidal signals, which is not a constant equilibrium any more, making the control more complicated.
- For grid-connected inverters, the active and reactive power delivered to the grid need to be controlled in order to minimise the negative impact on the grid stability.

6.1 Hybrid Modelling of DC-AC Inverters

In this chapter, the three-phase grid-connected inverter shown in Figure 6.1 is modelled as a hybrid model. The main contribution of this chapter is that, based on the Lyapunov stability theory, a novel switching current control law is designed to drive the grid currents to track the current references. Similar control techniques were proposed for DC-DC converters [149][139][150]. However, the problem in this chapter differs considerably from [149][139][150] due to the nonlinearity of the reference signal and the grid, and the number of power switches. The proposed switching control law designed by solving a set of linear matrix inequalities guarantees the stability of the closed-loop system [151]. Another advantage of the proposed approach is that the

switching law coefficients can be calculated off-line, which results in a very light online computation burden. Simulation results are presented to demonstrate the performance and robustness of the current controller.

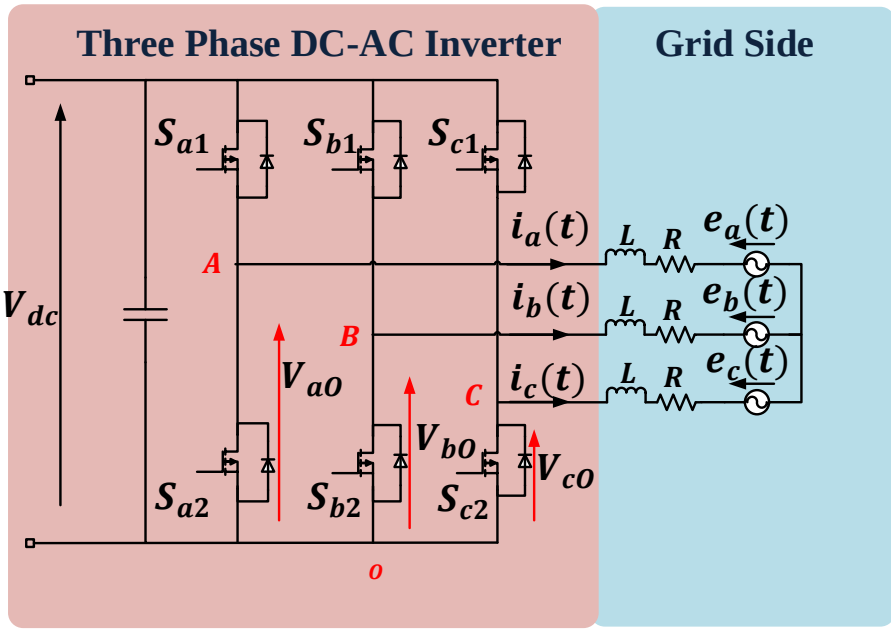


Figure 6.1: Three-phase grid-connected inverter

As shown in Figure 6.1, a three-phase DC-AC inverter, which is connected to the grid via an L-filter, is under consideration. R is the filter resistance, and L is the filter inductance. e_a, e_b and e_c are the three-phase grid voltage. V_{aO}, V_{bO} and V_{cO} are the phase to neutral (O) voltage of the inverter. Each phase, which consists of two IGBTs (S_{x1}, S_{x2}, $x = A/B/C$), has two possible states. The operation of each IGBT for two states is defined in Table 6.1.

Table 6.1: State definition for each Phase

Phase State	P	O
S_{x1}	ON	OFF
S_{x2}	OFF	ON

Table 6.2: Switching modes and voltage vectors

A	B	C	$Index$	v_α	v_β
O	O	O	1	0	0
P	O	O	2	$\frac{2}{3}V_{dc}$	0
P	P	O	3	$\frac{1}{3}V_{dc}$	$\frac{\sqrt{3}}{3}V_{dc}$
O	P	O	4	$-\frac{1}{3}V_{dc}$	$\frac{\sqrt{3}}{3}V_{dc}$
O	P	P	5	$-\frac{2}{3}V_{dc}$	0
O	O	P	6	$-\frac{1}{3}V_{dc}$	$-\frac{\sqrt{3}}{3}V_{dc}$
P	O	P	7	$\frac{1}{3}V_{dc}$	$-\frac{\sqrt{3}}{3}V_{dc}$
P	P	P	8	0	0

For simplicity, the output voltages of the inverter are expressed as a voltage vector in $\alpha\beta$ coordinates by following transformation [88]:

$$\mathbf{v} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} V_{aO} \\ V_{bO} \\ V_{cO} \end{bmatrix}, \tag{6.1}$$

where

$$T_{\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$$

Considering all the possible combination of the three phases, eight switching modes and corresponding voltage vectors are shown in Table 6.2. And the vector diagram is shown in Figure 6.2.

With the assumption that the filter and grid are balanced, the phase currents and the grid voltages also can be transformed into $\alpha\beta$ coordinates.

$$\mathbf{i} = \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{6.2}$$

$$\mathbf{e} = \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{6.3}$$

The current dynamic can be described as

$$L\frac{d\mathbf{i}}{dt} + R\mathbf{i} + \mathbf{e} = \mathbf{v}. \tag{6.4}$$

If we define the system state as $x(t) = [i_\alpha \; i_\beta]$ and define $\sigma : [-\infty, \infty) \to \Xi = \{1, 2, ..., 8\}$ as a piecewise constant function, which is a mapping from the state-space to the index of the active voltage vector, a hybrid model of the inverter can be established as

$$\dot{x}(t) = Ax(t) + B_\sigma, \tag{6.5}$$

where

$$A = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \qquad B_\sigma = \begin{bmatrix} \frac{v_\alpha(\sigma) - e_\alpha}{L} \\ \frac{v_\beta(\sigma) - e_\beta}{L} \end{bmatrix}.$$

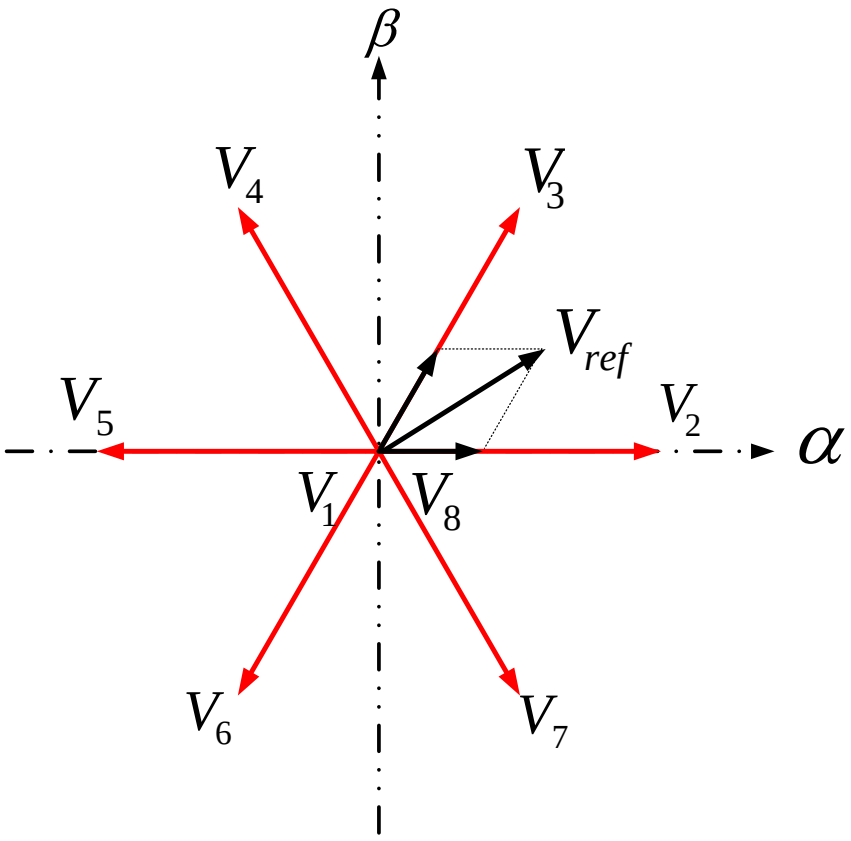


Figure 6.2: Voltage vectors in $\alpha\beta$ coordinates

6.2 Current Control Law Design

6.2.1 Online Implementation

Before presenting the control design, we give the entire system architecture in Figure 6.3. The current reference is generated based on the desired active and reactive power to regulate the power factor. The three-phase grid currents and grid voltages are measured. Then the measured grid currents and grid voltages are converted to $\alpha\beta$-frame respectively. These measured data along with the current references are transmitted to the switching current controller which determines the switching signals of the IGBTs.

6.2.2 Current Reference Generation

The objective of the current controller is to drive the grid current tracking a current reference $\mathbf{i}^* = [i_\alpha^* \; i_\beta^*]^T$. If we assume the grid current i_α, i_β and the grid voltage e_α, e_β are measurable, the

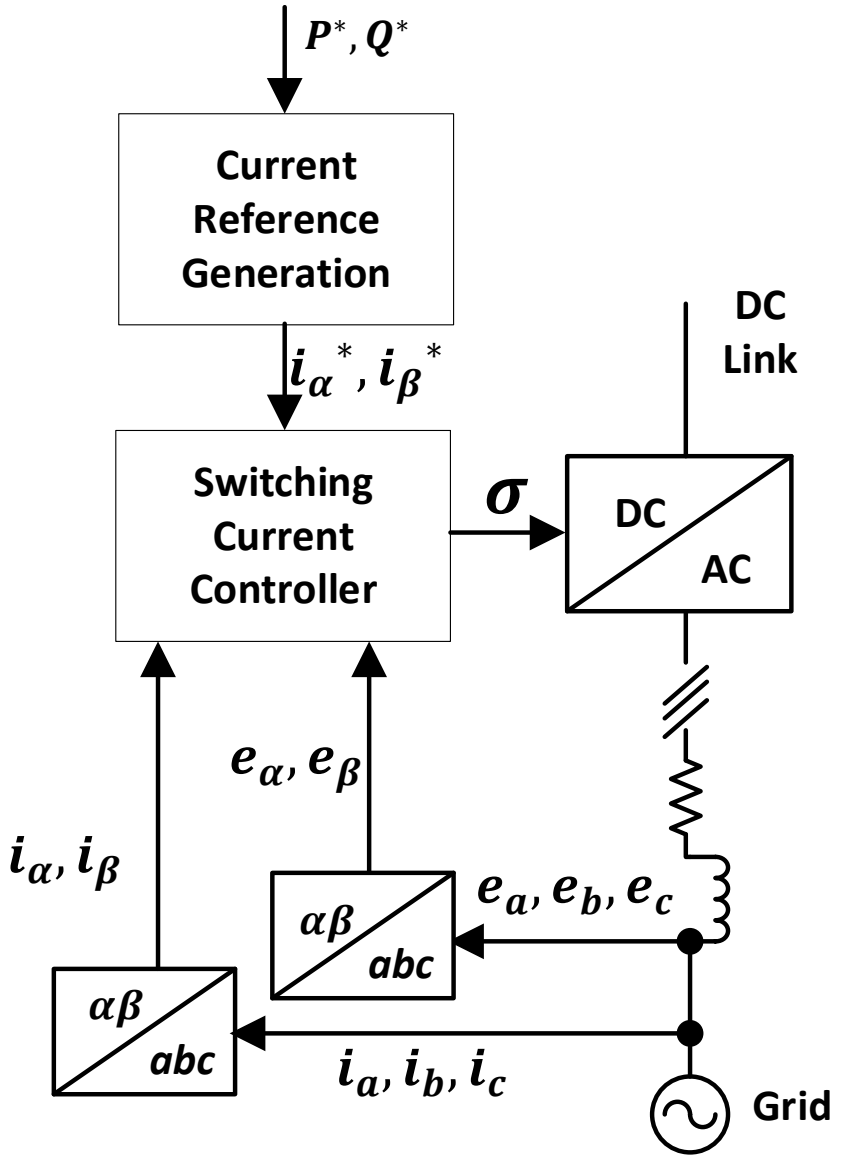


Figure 6.3: Setup of the grid-connected inverter

instantaneous active and reactive powers delivered to the grid can be calculated via [152]

$$P = i_\alpha e_\alpha + i_\beta e_\beta \tag{6.6}$$

$$Q = i_\beta e_\alpha - i_\alpha e_\beta. \tag{6.7}$$

By inverting (6.6) and (6.7), the current references can be generated based on desired active and reactive powers P^*, Q^* supplied to the grid

$$i_\alpha^* = \frac{P^* e_\alpha - Q^* e_\beta}{e_\alpha^2 + e_\beta^2} \tag{6.8}$$

$$i_\beta^* = \frac{P^* e_\beta + Q^* e_\alpha}{e_\alpha^2 + e_\beta^2}. \tag{6.9}$$

6.2.3 Stabilization of the Error System

If the tracking error is defined as $\varepsilon(t) = x(t) - \mathbf{i}^*$, the tracking error system is

$$\dot{\varepsilon}(t) = A\varepsilon(t) + \hat{B}_\sigma \tag{6.10}$$

where

$$A = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \qquad \hat{B}_\sigma = \begin{bmatrix} \frac{v_\alpha(\sigma)-e_\alpha}{L} - \frac{R}{L}i_\alpha^* - \frac{di_\alpha^*}{dt} \\ \frac{v_\beta(\sigma)-e_\beta}{L} - \frac{R}{L}i_\beta^* - \frac{di_\beta^*}{dt} \end{bmatrix}.$$

Hence, the proposed current controller is expected to stabilize the tracking error $\varepsilon(t)$ to the origin. The following theorem states that under some conditions the designed switching control law will drive the error system (6.10) to track the current reference with guaranteed closed-loop stability.

Theorem 6.1. *Define $\lambda = [\lambda_1, \lambda_2, ..., \lambda_8]^T$ belongs to the set Λ composed by all non-negative vectors such that $\sum_{i=1}^{8} \lambda_i = 1$. Consider the error system (6.10) and given matrix $Q > 0$, if there exists matrix $M > 0$ and $\lambda \in \Lambda$, $i \in \Xi$, such that*

$$A^T M + MA + Q < 0 \tag{6.11}$$

$$A\varepsilon_e + \hat{B}_\lambda = 0 \tag{6.12}$$

where

$$\hat{B}_\lambda = \sum_{i=1}^{8} \lambda_i \hat{B}_i \tag{6.13}$$

then under the switching law

$$\sigma(\varepsilon) = arg \min_{i \in \Xi} \varepsilon^T(t) M \hat{B}_i \tag{6.14}$$

the error system (6.10) is asymptotically stable.

Proof. Consider a Lyapunov functional

$$V(\varepsilon(t)) = \varepsilon^T(t) M \varepsilon(t). \tag{6.15}$$

Then along the solution of (6.10), the derivative of the chosen Lyapunov functional can be calculated:

$$\begin{aligned} \dot{V}(\varepsilon(t)) &= \dot{\varepsilon}^T(t) M \varepsilon(t) + \varepsilon^T(t) M \dot{\varepsilon}(t) \\ &= (A\varepsilon(t) + \hat{B}_\sigma)^T M \varepsilon(t) + \varepsilon^T(t) M (A\varepsilon(t) + \hat{B}_\sigma) \\ &= \varepsilon^T(t)(A^T M + MA)\varepsilon(t) + 2\varepsilon^T(t) M \hat{B}_\sigma. \end{aligned}$$

Under the switching law (6.14),

$$\begin{aligned}\dot{V}(\varepsilon(t)) &= \min_{i\in\Xi}\left[\varepsilon^T(t)(A^TM+MA)\varepsilon(t)+2\varepsilon^T(t)M\hat{B}_i\right]\\ &= \min_{i\in\Xi}\left[\varepsilon^T(t)(A^TM+MA+Q)\varepsilon(t)+2\varepsilon^T(t)M\hat{B}_i\right]\\ &\quad -\varepsilon^T(t)Q\varepsilon(t).\end{aligned} \tag{6.16}$$

According to the result of [139], the proof continues:

$$\begin{aligned}\dot{V}(\varepsilon(t)) &= \min_{\lambda\in\Lambda}\left[\varepsilon^T(t)(A^TM+MA+Q)\varepsilon(t)+2\varepsilon^T(t)M\hat{B}_\lambda\right]\\ &\quad -\varepsilon^T(t)Q\varepsilon(t).\end{aligned} \tag{6.17}$$

Since the equilibrium of the error system $\varepsilon_e \equiv 0$ and the conditions (6.11)(6.12),

$$\begin{aligned}\dot{V}(\varepsilon(t)) &= \min_{\lambda\in\Lambda}[\varepsilon^T(t)(A^TM+MA+Q)\varepsilon(t)\\ &\quad +2\varepsilon^T(t)(MA\varepsilon_e+M\hat{B}_\lambda)]-\varepsilon^T(t)Q\varepsilon(t)\\ &< -\varepsilon^T(t)Q\varepsilon(t)\end{aligned} \tag{6.18}$$

Hence based on the switched Lyapunov theory, the error system (6.10) is asymptotically stable under the switching law (6.14). □

Since the state matrix A is Hurwitz , a positive definite matrix M exists that condition (6.11) satisfied. Next, it will be shown that there always exists $\lambda \in \Lambda$ such that the condition (6.12) is fulfilled.

$$A\varepsilon_e+\hat{B}_\lambda=\hat{B}_\lambda=\frac{1}{L}\left(\sum_{i=1}^{8}\lambda_i\mathbf{v}_i-\left(L\frac{d\mathbf{i}^*}{dt}+R\mathbf{i}^*+\mathbf{e}\right)\right) \tag{6.19}$$

Based on Figure 6.2, the term $\sum_{i=1}^{8}\lambda_i\mathbf{v}_i$ is all the attainable voltage vectors in the $\alpha\beta$ coordinates with the eight switching modes. It is easy to show that the term $\left(L\frac{d\mathbf{i}^*}{dt}+R\mathbf{i}^*+\mathbf{e}\right)$ is the reference voltage vector $\mathbf{v}^*$ of the inverter based on the current dynamic equation (6.4). Hence, it is obvious that by choosing appropriate $\lambda \in \Lambda$, the reference voltage vector $\mathbf{v}^* = \sum_{i=1}^{8}\lambda_i\mathbf{v}_i$, that is,

$$A\varepsilon_e+\hat{B}_\lambda=\hat{B}_\lambda=0. \tag{6.20}$$

Remark 6.2. The controller variables M can be obtained off-line by solving the LMI conditions (6.11) through MATLAB combined with YALMIP interface [153], which is a Matlab toolbox. Hence, the online computation of the switching rule (6.14) is simple and straightforward.

Table 6.3: Grid-connected inverter parameters

Three-phase DC-AC inverter Configuration	
V_{dc}	$600V$
L	$10mH$
R	10Ω
Grid Voltage	$100V$
Grid Frequency	$50Hz$
Switching/Sampling Frequency	$10kHz$

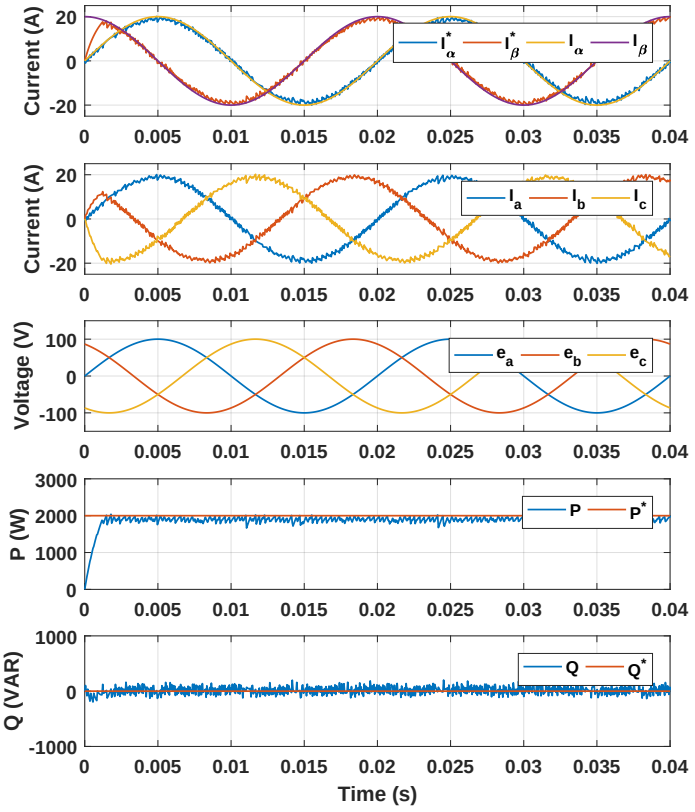


Figure 6.4: The waveforms of the grid currents i_α, i_β in $\alpha\beta$-frame, i_a, i_b, i_c in abc-frame, grid voltages e_a, e_b, e_c, active power and reactive power when the power references are in nominal value.

6.3 Simulation Results

The proposed control scheme is verified on a $600V$ $2kVA$ system. Both the grid-connected inverter and the controller are implemented in MATLAB Simulink, and the parameters of the nominal operation are given in Table 6.3. Before the real-time simulation, the LMI (6.11) was solved with a given unity matrix Q. The pre-calculated parameters of the switching current

controller was obtained as:

$$M = 10^5 \times \begin{bmatrix} 2.4751 & 0 \\ 0 & 2.4751 \end{bmatrix} \tag{6.21}$$

6.3.1 Nominal Operation

In the first case, in order to test the stability of the whole system under the proposed switching law (6.14), the active power reference P^* is set to $2kW$ and the reactive power reference Q^* is set to 0 VAR to achieve a unity power factor. As shown in Figure 6.4, the current references i_α^*, i_β^* are generated based on (6.8) and (6.9) with fixed amplitude, frequency, and phase shift since the grid voltage is assumed balanced and the power references are constant. The grid currents are controlled to track the current references with reasonable ripple. The instantaneous active power P is stabilized to the power reference within a short transition period, and the average value of reactive power is close to zero. Furthermore, the phase voltages V_{aO}, V_{bO}, V_{cO} are shown in Figure 6.5. One can observe that different voltage vectors are selected by the switching current controllers. The mean value of the phase voltages has been plotted on the same figure. As shown in the figure, the three phase mean voltages are sinusoidal as well.

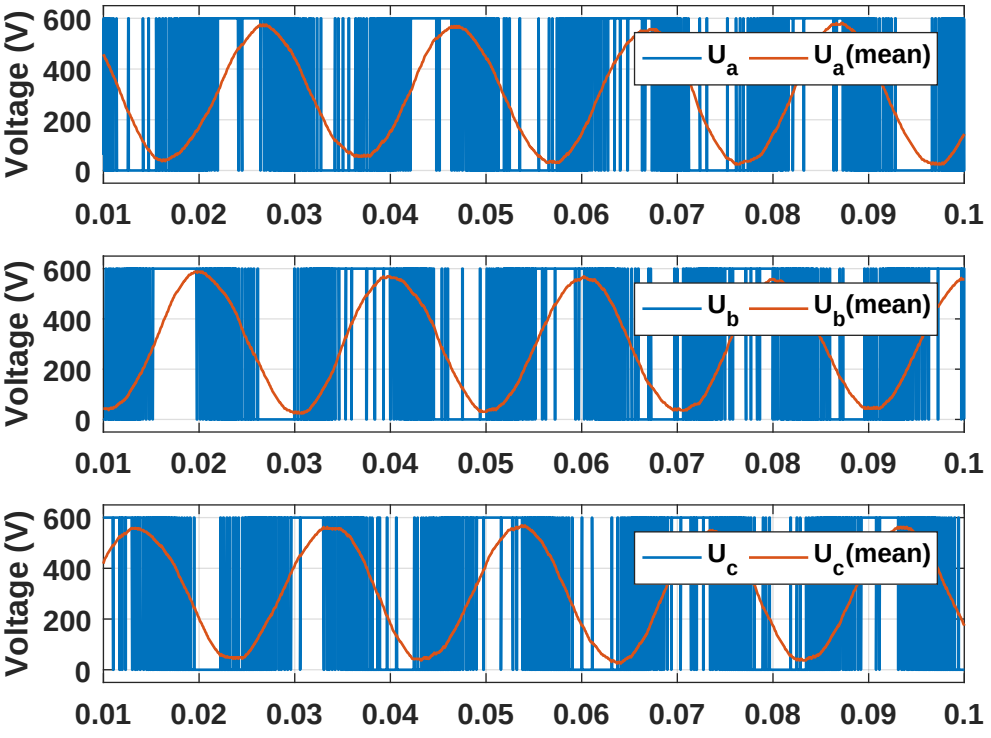


Figure 6.5: The waveforms and the mean of the phase voltages V_{aO}, V_{bO}, V_{cO} when the power references are in nominal values.

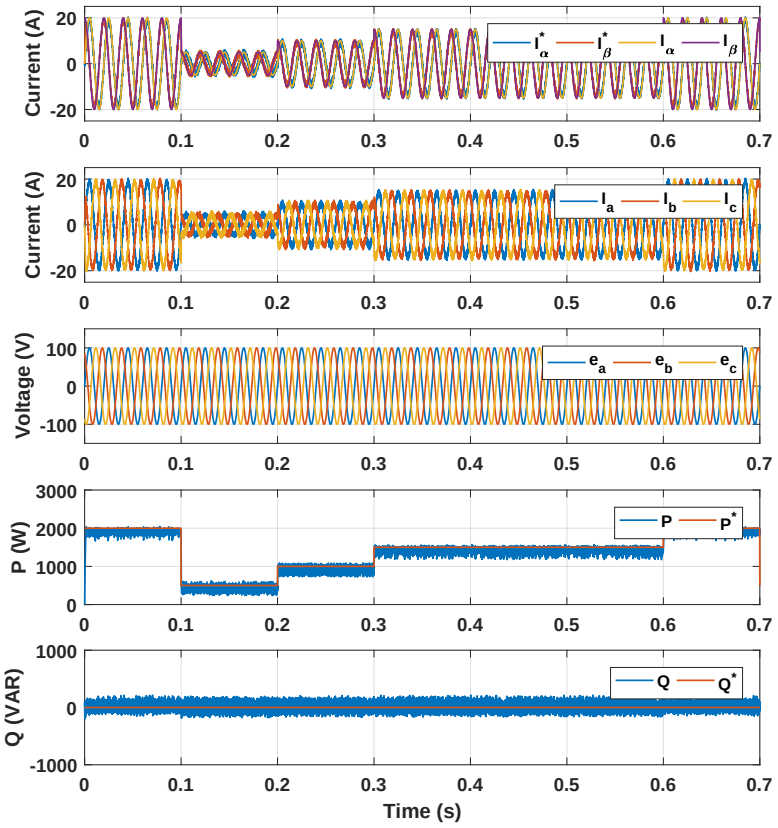


Figure 6.6: The waveforms of the grid currents i_α, i_β in $\alpha\beta$-frame, i_a, i_b, i_c in abc-frame, grid voltages e_a, e_b, e_c, active power and reactive power with various active power steps.

6.3.2 Active Power Tracking

In this section, the robustness of the switching controller is tested. As shown in Figure 6.6, the active power reference P^* stepped from $2kW$ to $0.5kW$ at $0.1s$, then to $1kW$ at $0.2s$, back to $1.5kW$ at $0.3s$, finally to $2kW$ at $0.6s$. Correspondingly, the current references i^*_α, i^*_β are generated with varying amplitude. In order to demonstrate the transition performance, the waveforms are zoomed between $0.09s$ and $0.12s$ during which the active power reference P^* stepped down from $2kW$ to $0.5kW$. The grid current are well controlled during the step with very short transition period, and the active power P also responded to the step with same transition period and no overshoot. In the meantime, the reactive power Q is controlled close to zero during the whole simulation. The total harmonic distortion of the grid current has been analysed via the Matlab PowerSystem FFT tool. The THD of the grid current is only 3.98% in nominal operation and as the power reference decreases, THD increases, which is because the magnitude of voltage and current decrease, but the ripple of voltage and current stay the same.

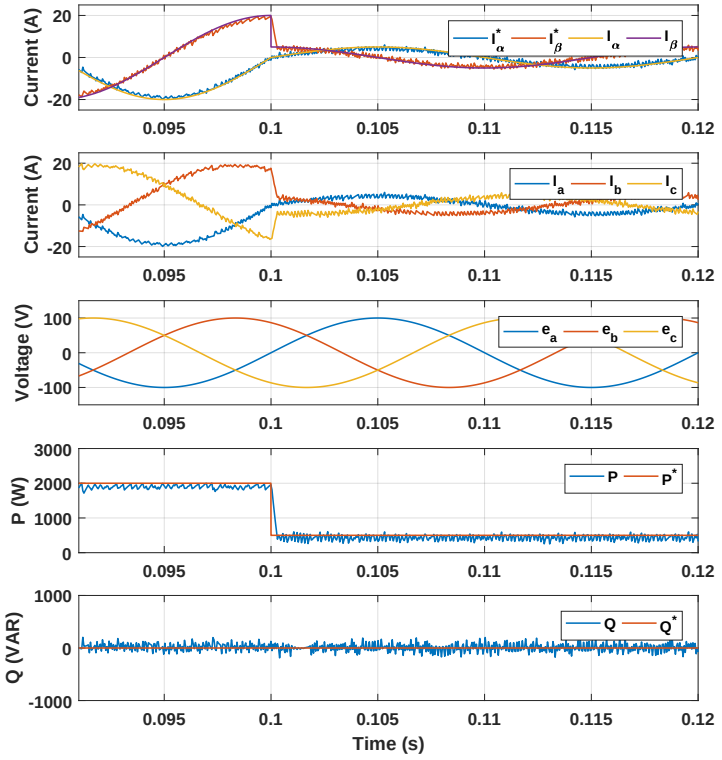
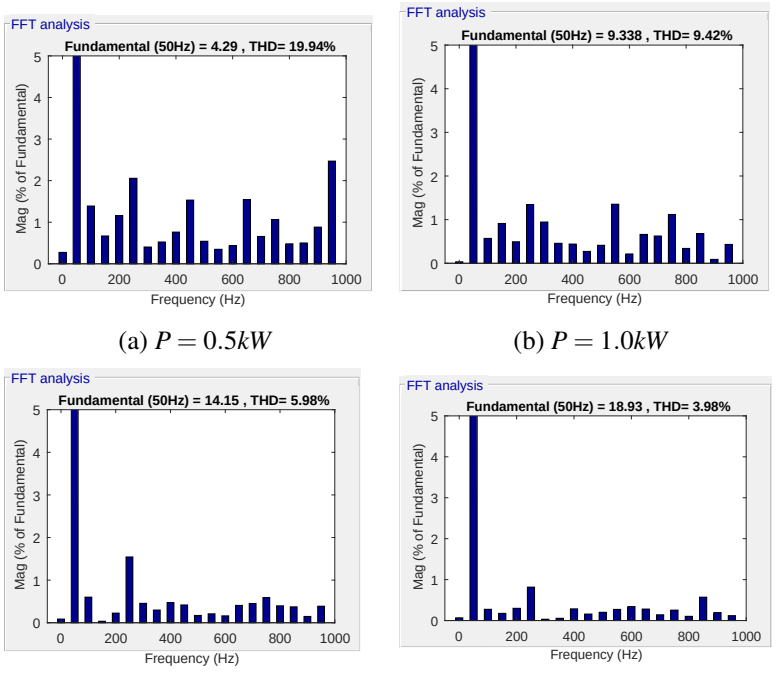


Figure 6.7: The zoomed waveforms of the grid currents i_α, i_β in $\alpha\beta$-frame, i_a, i_b, i_c in *abc*-frame,grid voltages e_a, e_b, e_c, active power and reactive power with various active power steps.



(a) $P = 0.5kW$ (b) $P = 1.0kW$

(c) $P = 1.5kW$ (d) $P = 2kW$

Figure 6.8: Total Harmonic Distortion (THD) of grid current

6.4 Summary

In this chapter, a new modelling and control scheme is proposed for a three-phase grid-connected inverters that can interface distributed generation systems to the grid. Compared with conventional PWM control approaches, the controller determines the switching states of the inverter directly. Furthermore, compared with predictive control approaches, the proposed method can be implemented on basic microprocessors with low sampling rates since the coefficients of the switching law are computed off-line and the sampling frequency is equal to switching frequency. The robustness of the method is tested by tracking varying power references. In the future, experiment validation will be carried out and the proposed methods can be extended to more complex inverter topologies. At the same time, the popular maximum power point tracking (MPPT) can be combined with the proposed control strategy with application to wind turbines and photovoltaic (PV) solar systems.

Chapter 7

Switching Control of Grid-Connected Single-Phase NPC Inverters

7.1 Switching States of Single-Phase Grid-Connected NPC Inverter

A two-leg single-phase NPC inverter is shown in Figure 7.1. Each leg (A or B), which consists of four IGBTs ($S_{x1}, S_{x2}, S_{x3}, S_{x4}$, $x = A\ or\ B$) connected in series and two clamped diodes, has three possible states as shown in Table I(a), where P, O and N stand for positive, neutral, negative state. The operation of each IGBT for different states is also defined in the table. For the specific inverter described in this chapter, there are nine switching states, due to the combination of the two legs, which are PP (Leg A in P state, and leg B in P state), PO, PN, OP, OO, ON, NP, NO, NN. However, if we neglect the unbalance issue of the neutral point, only five voltage levels can be output to the filter part, which are V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$ and $-V_{dc}$. Table I(b) shows the possible switching states for a given voltage output U_σ. Figure 7.2 shows the working principle of the NPC inverter to output five different voltage level.

- $\mathbf{U_{AB} = V_{dc}}$: When the upper two switches of phase A and the lower two switches of phase B are conducting, the voltage output U_{AB} is equal to the input voltage V_{dc} as shown in Figure 7.2a.
- $\mathbf{U_{AB} = \frac{V_{dc}}{2}}$: When the upper two switches of phase A and the middle two switches of phase B are conducting, the voltage output U_{AB} is equal to half of the input voltage V_{dc} as shown in Figure 7.2b. The redundant state, ON, produces the same voltage output if we assume the two capacitors are balanced.
- $\mathbf{U_{AB} = 0}$: When the two phases have same leg state, the voltage output is equal to zero. For example, Figure 7.2c. The other two redundant states are OO, PP.
- $\mathbf{U_{AB} = -\frac{V_{dc}}{2}}$: When the middle two switches of phase A and the upper two switches of phase B are conducting, the voltage output U_{AB} is equal to negative half of the input

Table 7.1: Switching states for each leg and the whole inverter

(a) State definition for each leg

Leg state	P	O	N
S_{x1}	ON	OFF	OFF
S_{x2}	ON	ON	OFF
S_{x3}	OFF	ON	ON
S_{x4}	OFF	OFF	ON

(b) Voltage output and redundant switching states

Voltage Output U_σ	Index σ	Switching states
V_{dc}	1	PN
$V_{dc}/2$	2	PO,ON
0	3	PP,OO,NN
$-V_{dc}/2$	4	OP,NO
$-V_{dc}$	5	NP

voltage V_{dc} as shown in Figure 7.2d. The redundant state, NO, produces the same voltage output.

- $\mathbf{U_{AB} = -V_{dc}}$: When the lower two switches of phase A and the upper two switches of phase B are conducting, the voltage output U_{AB} is equal to the negative sign of input voltage V_{dc} as shown in Figure 7.2e.

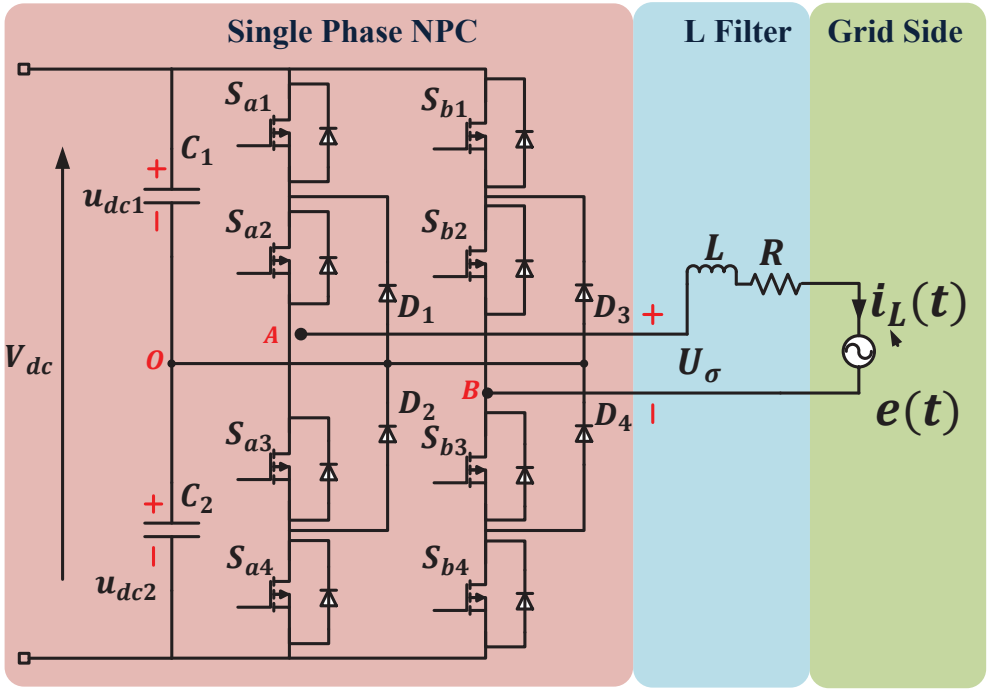
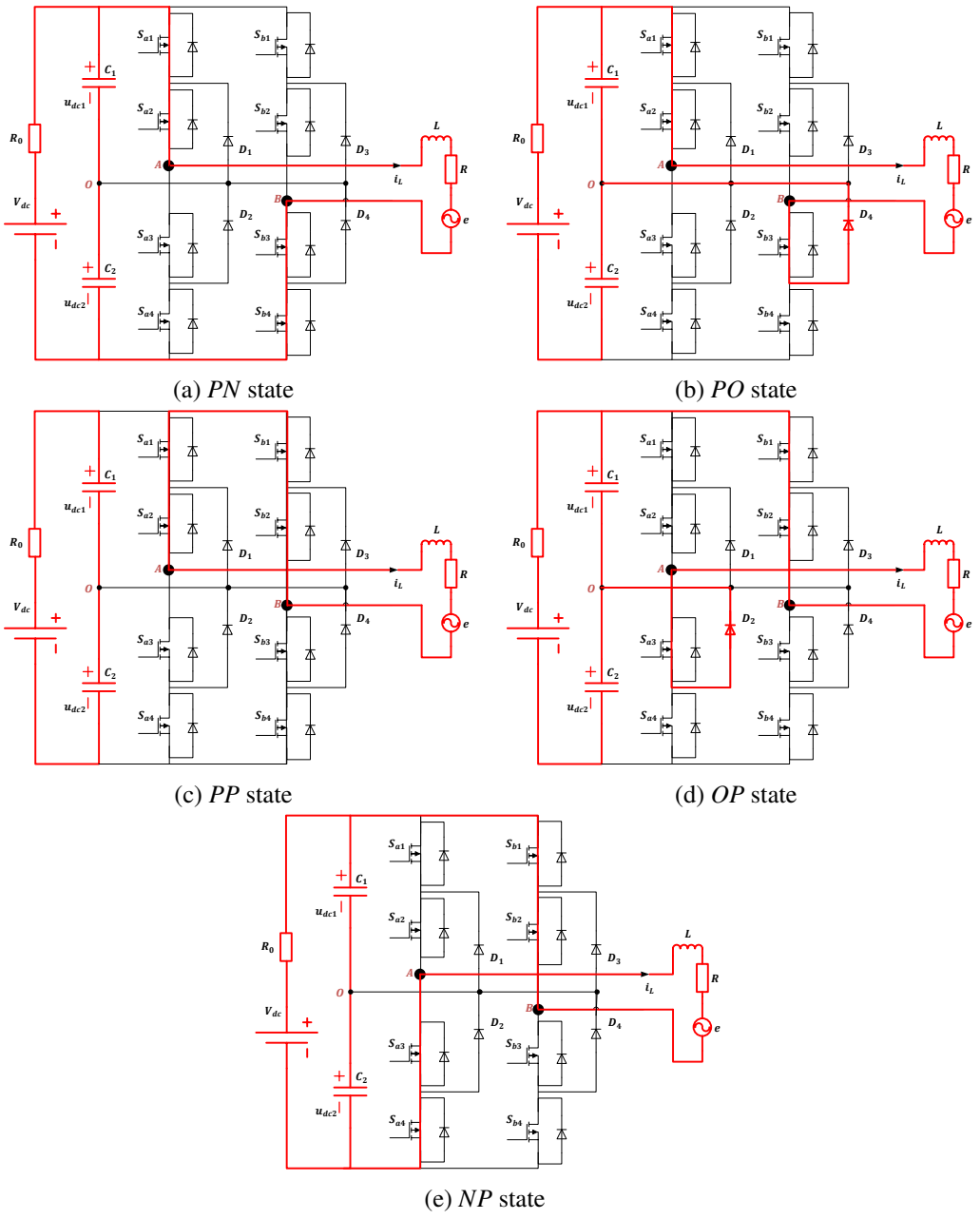


Figure 7.1: Single-phase grid-connected NPC inverter for distributed energy source application



(a) *PN* state

(b) *PO* state

(c) *PP* state

(d) *OP* state

(e) *NP* state

Figure 7.2: The circuit diagram of four possible switching states with five different voltage level

7.2 Hybrid Modelling and Switching Controller Design

A novel control scheme is proposed as shown in Figure 7.3. The whole system is separated as the inverter part and the filter part. A switching controller will only choose the proper voltage output U_σ, which can force the output current i_L to track the time-variant current reference i_{ref}; then an auxiliary voltage balancing controller will take advantage of the redundant switching states to balance the neutral-point voltage. For example, if $U_2 = V_{dc}/2$ is chosen by the switching controller, two different switching states can be activated: *PO* or *ON*. The voltage balancing

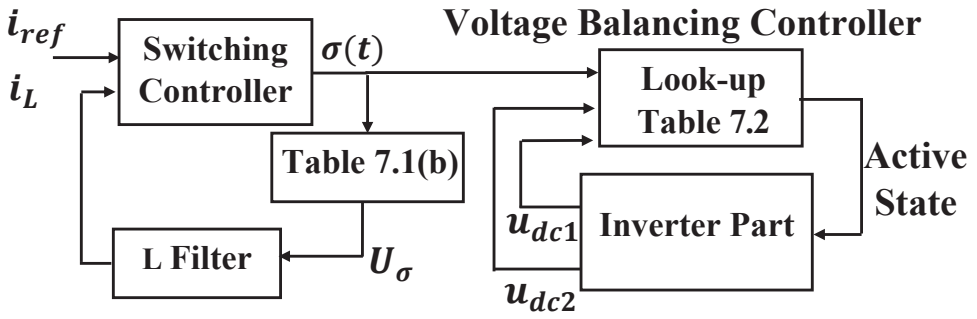


Figure 7.3: A proposed control structure

controller will decide which is more suitable based on the measurement of u_{dc1} and u_{dc2}. The details of the design are as follow.

7.2.1 Hybrid Model of the Filter Part

In this subsection, it is assumed the dc-link capacitors are balanced ($u_{dc1} = u_{dc2} = \frac{V_{dc}}{2}$).

Define $\sigma : [0,\infty) \to \Xi = \{1,2,...,5\}$ as a piecewise constant function, which is a mapping from the state-space to the index of the active voltage output U_σ. The relation between the voltage output U_σ and the index is shown in Table I(b).

Then a hybrid model with both continuous and discrete dynamics can be defined as:

$$\dot{i}_L(t) = Ai_L(t) + BU_\sigma + D(e), \tag{7.1}$$

where $A = -\frac{R}{L}$, $B = \frac{1}{L}$, $D(e) = -\frac{e(t)}{L}$, and U_σ is defined in Table I(b).

7.2.2 Switching Controller Design

In order to describe the dynamic of the sinusoidal reference $i_{ref}(t)$, a reference model is proposed in which $z(t)$ is the state of the model, $i_{ref}(t)$ is the output, ω is the angular frequency, and I is the magnitude.

$$\dot{z}(t) = Hz(t), \;\; z'(t)Nz(t) = I^2, \tag{7.2}$$

$$i_{ref}(t) = Zz(t), \tag{7.3}$$

where

$$z(t) = \begin{bmatrix} I\sin(\omega t) \\ I\cos(\omega t) \end{bmatrix} \qquad H = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}$$
$$N = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \qquad Z = \begin{bmatrix} 1 & 0 \end{bmatrix}.$$

The relation $z'(t)Nz(t) = I^2$ specifies the magnitude since $(I\sin(\omega t))^2 + (I\cos(\omega t))^2 = I^2$.

Furthermore, if the tracking error is defined as $\varepsilon(t) = i_L(t) - i_{ref}(t)$, the tracking error system is

$$\dot{\varepsilon}(t) = A\varepsilon(t) + BU_\sigma + D(e) + (AZ - ZH)z(t). \tag{7.4}$$

Hence, the switching law $\sigma(t)$ should be able to drive the error state $\varepsilon(t)$ to the origin. In this chapter, the following switching law $\sigma(\varepsilon(t))$ and a mode-dependent Lyapunov function $V(\varepsilon(t),\sigma)$ are considered.

$$\sigma(\varepsilon(t)) \triangleq \arg\max_{i\in\Xi}\{v_i(\varepsilon(t))\}, \tag{7.5}$$
$$V(\varepsilon(t)) \triangleq \max_{i\in\Xi}\{v_i(\varepsilon(t))\}, \tag{7.6}$$
$$\text{where } v_i(\varepsilon(t)) \triangleq \varepsilon(t)'P_i\varepsilon(t) + 2\varepsilon(t)'Q_i(z(t)),$$
$$Q_i(z(t)) \triangleq Q_{i0} + Q_{i1}z(t).$$

Note: *The* $\arg\max\{v_1,\ldots v_5\}$ *is used to denote the index of the maximum element* v_i*. For example,* $v_1 = 1$, $v_2 = 3$, $v_3 = 4$, $v_4 = 5$, $v_5 = 2$*. Hence,* $V(\varepsilon(t)) = v_4$*.* $\sigma(\varepsilon(t))$ *will equal to the index of the maximum* $v_i(\varepsilon(t))$*, which is* $\sigma = 4$*. Then the voltage output* $-V_{dc}/2$ *will be activated according to Table I(b).*

The performance requirement is proposed as:

$$\dot{V}(\varepsilon(t)) + \alpha_\sigma V(\varepsilon(t)) < 0, \tag{7.7}$$
$$V(\varepsilon(t)) > 0, \tag{7.8}$$

where α_σ are given non-negative constants.

Then the LMI condition, which can guarantee the closed-loop globally asymptotically stability of the tracking error system (7.4) is presented below. Two technical lemmas are given beforehand.

Lemma 7.1. *(Bilinear Matrix Decompositions)[154] Consider two matrices with same dimension* $X, Y \in \mathbb{R}^{n*m}$*,*

1. *The mappings* $f(X) = X^T X$ *and* $g(X) = XX^T$ *are positive semidefinite and convex on* $\mathbb{R}^{n*m}$.

2. *The bilinear matrix form* $b(X,Y) = X^T Y + Y^T X$ *can be decomposed as the difference of two positive semidefinite and convex parts*

$$b(X,Y) = \frac{1}{2}\left[(X+Y)^T(X+Y) - (X-Y)^T(X-Y)\right] \tag{7.9}$$

Lemma 7.2. *(Schur Complement) [147] Suppose that matrix A is symmetric. Then the following two matrices inequality is equivalent.*

1.
$$BB^T - A < (\leq) 0 \tag{7.10}$$

2.
$$\begin{bmatrix} A & B \\ B^T & I \end{bmatrix} > (\geq) 0 \tag{7.11}$$

Theorem 7.3. *Assume* $z(t)$ *and* $e(t)$ *are bounded by a given polytope* Π. *Consider the tracking error system* (7.4) *and given non-negative constants* α_i, $i \in \Xi$, *if the following parameter-dependent LMIs with variables* P_i, $Q_i(z(t))$, $\forall i \in \Xi$ *are satisfied at the vertices of* Π.

$$P_i > 0 \quad \sum_{i=1}^{\Xi} Q_{i0} = 0 \quad \sum_{i=1}^{\Xi} Q_{i1} = 0 \tag{7.12}$$

$$\Delta_{i1} + \alpha_i \Delta_{i2} + \Delta_{i3} < 0 \tag{7.13}$$

where

$$\Delta_{i1} = \begin{bmatrix} A'P_i + P_i A & P_i(AZ - ZH) & \theta_{13} \\ * & 0 & (AZ - ZH)' Q_i(z(t)) \\ * & * & \theta_{33} \end{bmatrix}$$

$$\theta_{13} = P_i B_i + P_i D(e) + A' Q_i(z(t)) + Q_{i1} H z(t)$$

$$\theta_{33} = Q_i'(z(t)) B_i + B_i' Q_i(z(t)) + Q_i'(z(t)) D(e) + D(e)' Q_i(z(t))$$

$$\Delta_{i2} = \begin{bmatrix} P_i & 0 & Q_i(z(t)) \\ * & 0 & 0 \\ * & * & 0 \end{bmatrix}$$

$$\Delta_{i3} = \begin{bmatrix} 0 & 0 & 0 \\ * & N & 0 \\ * & * & -I^2 \end{bmatrix}$$

Then the tracking error system (7.4) *is globally asymptotically stable with the switching law* (7.5) *and the condition* (7.7)(7.8) *satisfied.*

Proof. Due to the convexity of the LMIs, if the conditions are satisfied at the vertices of the Π, it can also be fulfilled by $\forall z(t)$ and $\forall e(t)$ in the polytope Π.

Multiplying (7.13) by $\xi = [\varepsilon(t)\ z(t)\ 1]^T$ to the right and the transpose to the left, one can easily get:

$$\dot{v}_i(\varepsilon(t)) + \alpha_i v_i(\varepsilon(t)) + (z'(t)Nz(t) - I^2) < 0 \tag{7.14}$$

Due to $z'(t)Nz(t) = I^2$, the condition (7.7) is obtained.

Then we have:

$$\begin{aligned}\sum_{i=1}^{\Xi} v_i(\varepsilon(t)) =& \varepsilon'(t)\left(\sum_{i=1}^{\Xi} P_i(z(t))\right)\varepsilon(t) \\ &+ 2\varepsilon'(t)\left(\sum_{i=1}^{\Xi} Q_{i0}\right) + 2\varepsilon'(t)\left(\sum_{i=1}^{\Xi} Q_{i1}\right) z(t)\end{aligned} \tag{7.15}$$

Substituting (7.12),

$$\sum_{i=1}^{\Xi} v_i(\varepsilon(t)) > 0 \tag{7.16}$$

hold. One can conclude that at least one of the $v_i(\varepsilon(t)$ is positive definite. Hence,

$$V_\sigma(\varepsilon(t)) = \max_{i\in\Xi} v_i(\varepsilon(t) > 0 \tag{7.17}$$

hold. For the global stability, an additional condition is required, which $V_\sigma(\varepsilon(t))$ is radially unbounded. Since $\sum_{i=1}^{\Xi} v_i(\varepsilon(t))$ is positive definite, it is radially unbounded.

Because

$$\sum_{i=1}^{\Xi} v_i(\varepsilon(t)) < 5V_\sigma(\varepsilon(t)) \tag{7.18}$$

hold, $V_\sigma(\varepsilon(t))$ is radially unbounded.

Thus, the tracking error system (7.4) is globally asymptotically stable with the switching law (7.5). □

Remark 7.4. The controller variables P_i, Q_{i0}, Q_{i1}, $\forall i \in \Xi$ can be obtained off-line by solving the LMI conditions (7.12)(7.13) through Matlab combined with YALMIP interface [153]. Hence, the online computation of the switching rule (7.5) is simple and straightforward.

7.2.3 Auxiliary Voltage Balancing Controller

In order to maintain the balance of the neutral-point O and relieve the stress on each power switch. An auxiliary voltage balancing controller is proposed in the form of a look-up table (Table 7.2).

Table 7.2: Auxiliary voltage balancing controller

Voltage Output Index	Criteria		Active State
$\sigma = 1$	NA		PN
$\sigma = 2$	$u_{dc1} > u_{dc2}$		ON
	$u_{dc1} < u_{dc2}$		PO
$\sigma = 3$	Previous Switching State	PN,PO,PP	PP
		ON,OP,OO	OO
		NO,NP,NN	NN
$\sigma = 4$	$u_{dc1} > u_{dc2}$		OP
	$u_{dc1} < u_{dc2}$		NO
$\sigma = 5$	NA		NP

Table 7.3: NPC inverter parameters

NPC inverter Configuration	
	in S.I
V_{dc}	$400V$
L	$50mH$
C	$750\mu F$
R	0.1Ω
I	$10A$
Grid Voltage	$230V$
Grid Frequency	$50Hz$
Switching/Sampling Frequency	$20kHz$

7.3 Simulation Results

The proposed control scheme is verified through simulation. Both the grid-connected NPC inverter and the controllers are implemented in Matlab Simulink, and the parameters of the nominal operation in shown in Table 7.3.

7.3.1 Nominal Operation

First of all, the controller is tested when the inverter is in nominal mode. The responses is shown in Figure 7.4. As we can see, the inductor current i_L is able to track the sinusoidal reference i_{ref} with ripple of $0.8A$. The capacitor voltages u_{dc1} and u_{dc2} are generally balanced with the proposed auxiliary voltage balancing controller.

7.3.2 Reference Variation

In order to test the robustness of the proposed method, the current reference is changed as shown in Figure 7.5. At $0.025s$, the reference signal i_{ref} is changed to $5V$ peak to peak from $10V$ peak

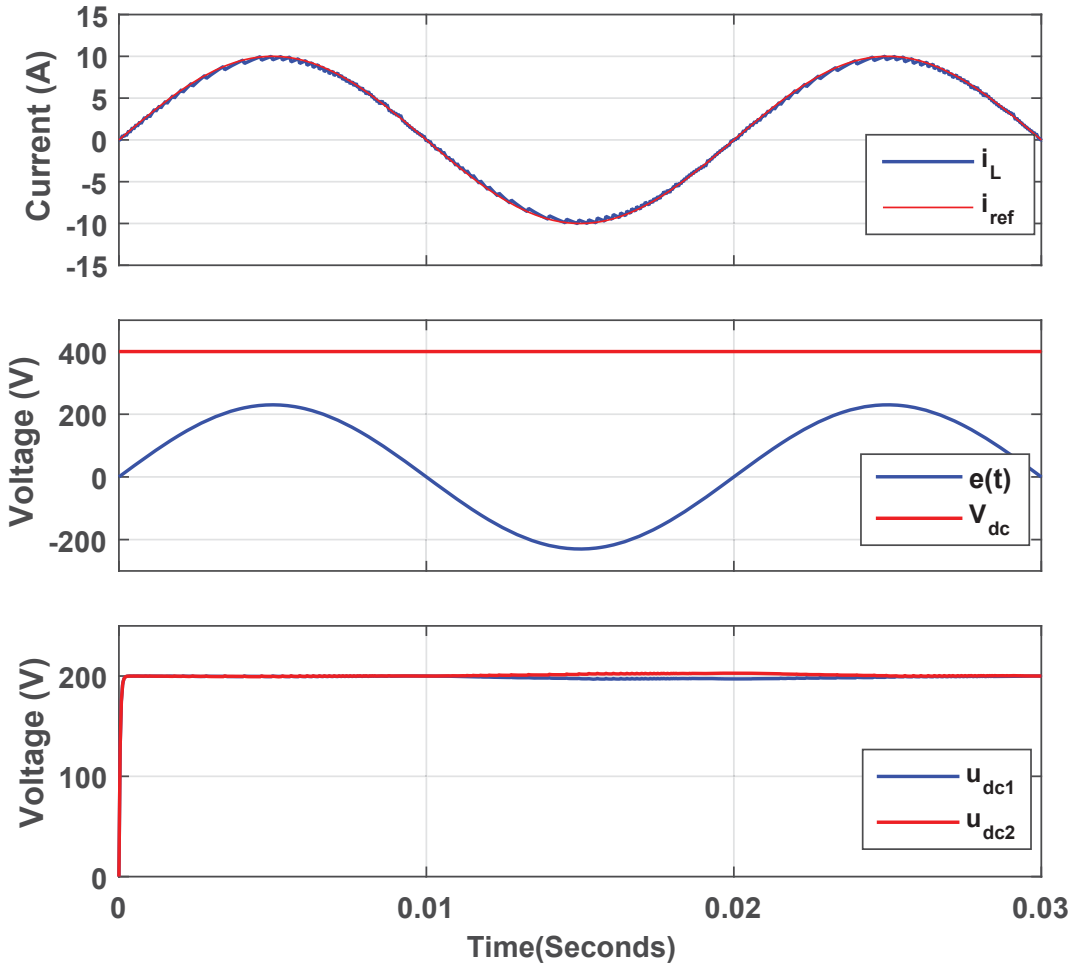


Figure 7.4: Nominal operation

to peak, then at $0.045s$ i_{ref} is changed back to $10V$ peak to peak. Under the proposed control scheme, the inductor current i_L followed the change of the reference signal with fast dynamic responses. At the same time, the balance of the neutral point is kept under the proposed auxiliary voltage balancing controller.

7.3.3 DC-link Voltage Variation

In practice, the DC-link voltage may suffer from ac noise and variation. A robust controller should be able to handle this realistic situation. In this part, some ac noise is added to the DC-link voltage V_{dc} as shown in Figure 7.6. However, the inductor current i_L is still tracking the reference current with good performance. The capacitor voltages u_{dc1} and u_{dc2} are balanced but with similar ac noise which is acceptable.

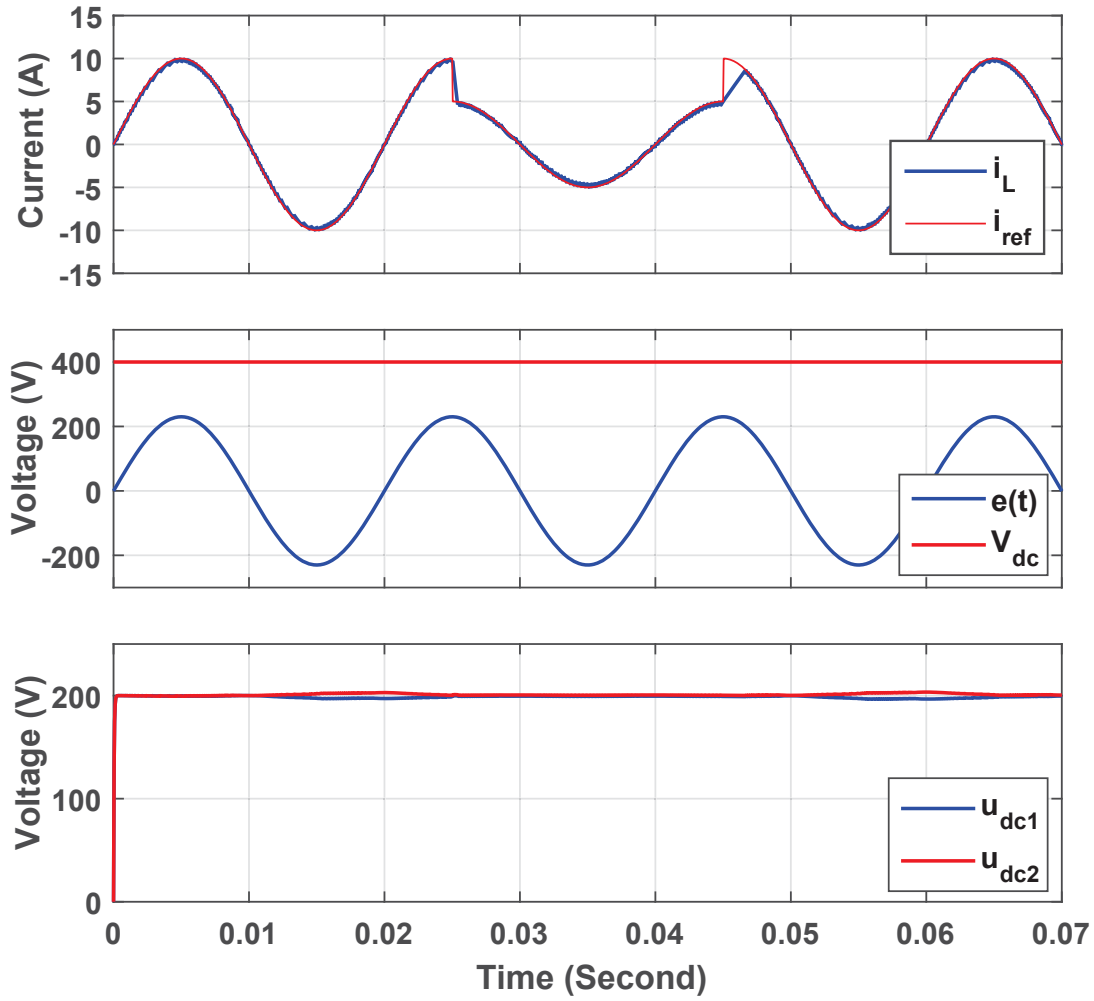


Figure 7.5: Reference magnitude changed to $5V$ during $0.025s$ to $0.045s$

7.3.4 Model Parameters Tolerances

In this part, the inductor value is changed to $40mH$ from $50mH$ to test if the proposed controllers can handle the uncertainty of the model parameter. As shown in 7.7, the inductor current i_L is generally not affected. The difference of the capacitor voltages u_{dc1} and u_{dc2} is more obvious but is still varied around the balanced point.

7.4 Summary

In this chapter, hybrid modelling of a single-phase grid-connected Neutral-Point Clamped (NPC) inverter is studied. Compared to conventional two-level DC-AC inverter as we discussed in the previous chapter, the three-level NPC inverter considered in this chapter has doubled power switches for each leg and the capacitor balancing issue needs to be considered as well. The main contribution of this chapter is that a novel state-feedback switching control law is designed

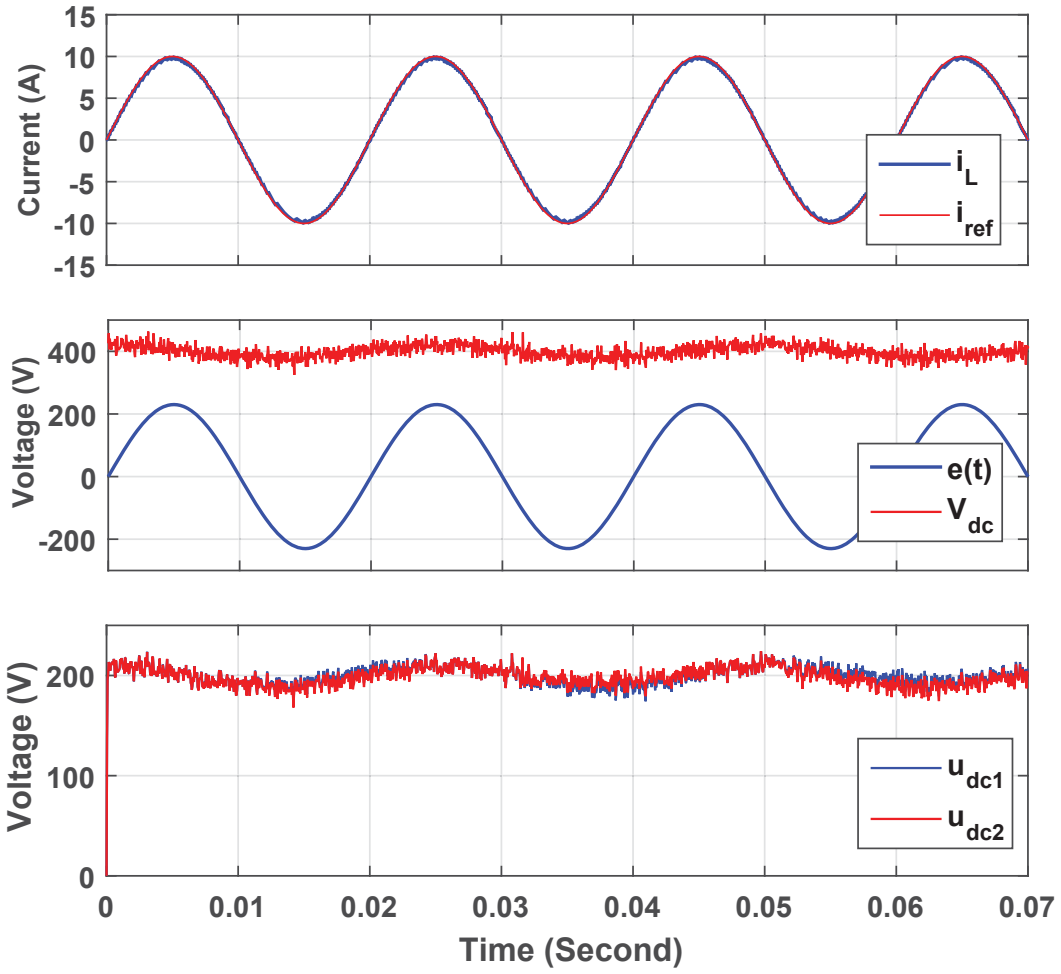


Figure 7.6: DC-link voltage with large ripple and variation

to force the output current to track a desired sinusoidal current reference. Furthermore, the neutral point voltage ripple is minimized by a capacitors voltage balancing controller. Simulation results validate the performance of the proposed control scheme in different operating conditions including reference tracking, reference variation, DC-link voltage variation, and parameters tolerances.

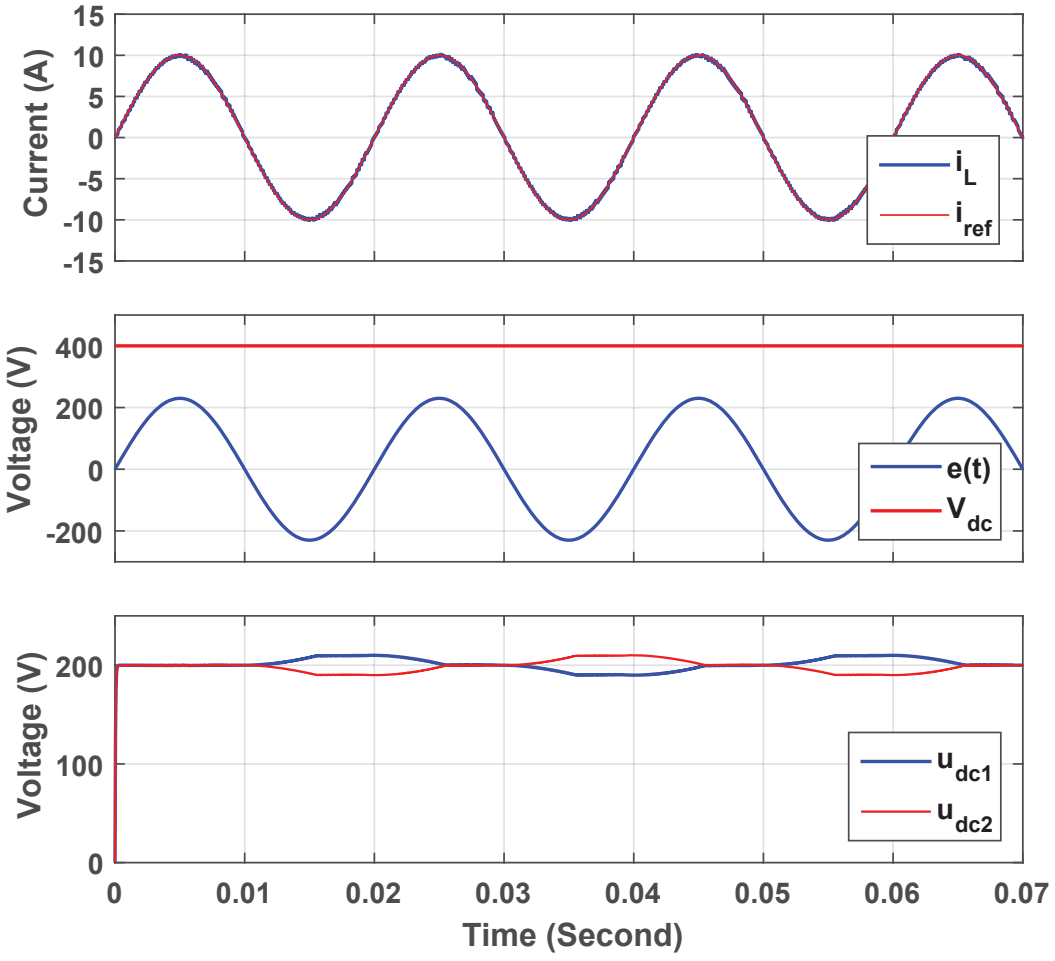


Figure 7.7: Inductor value changed to 40mH

Chapter 8

Switching Control of Three-Phase NPC Inverters

8.1 Hybrid Modelling of Three-Phase NPC Inverters

As shown in Figure 8.1, a three-phase grid-connected NPC inverter, which is connected to the grid via an L-filter, is under consideration. R is the filter resistance, and L is the filter inductance. e_a, e_b and e_c are the three-phase grid voltage. Each phase, which consists of four IGBTs (S_{x1}, S_{x2}, S_{x3}, S_{x4}, $x = A/B/C$), has three possible states. The operation of each IGBT for the three states is defined in Table 8.1.

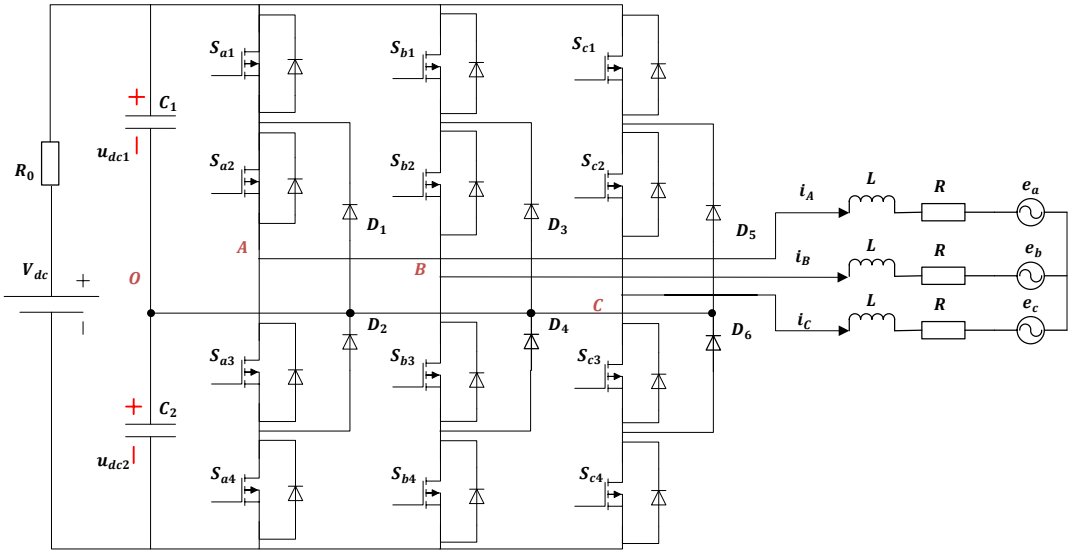


Figure 8.1: Circuit diagram of a grid-connected three-phase NPC inverter

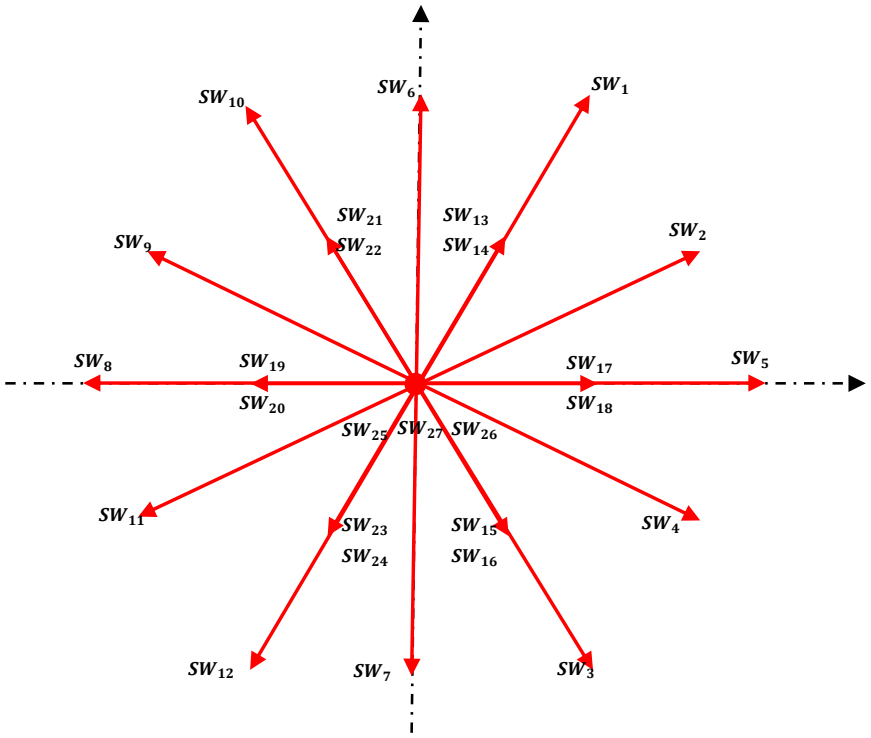


Figure 8.2: Voltage vectors in $\alpha\beta$ coordinates

Table 8.1: State definition for each Phase

Phase State	P	O	N
S_{x1}	ON	OFF	OFF
S_{x2}	OFF	ON	OFF
S_{x3}	ON	ON	ON
S_{x4}	OFF	OFF	ON

For simplicity, the output voltages of the inverter are expressed as a voltage vector in $\alpha\beta$ coordinates by the following transformation [88]:

$$\mathbf{v} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} V_{aO} \\ V_{bO} \\ V_{cO} \end{bmatrix}, \tag{8.1}$$

where

$$T_{\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$$

Considering all the possible combination of the three phases, 27 switching states and corresponding voltage vectors are shown in Table 8.2. And the vector diagram is shown in Figure 8.2. As seen in Figure 8.2, there are only 19 different voltage vector, which means some of the switching states produce the same voltage vector. For instances, SW_{17} and SW_{18} have same α and β components. For notation, the index of the switching state is θ and the index for the

Table 8.2: Switching states and voltage vectors

A	B	C	State Index θ	$Vector\sigma$	v_α	v_β
P	P	N	1	1	$\frac{2}{3}V_{dc}$	$\frac{2\sqrt{3}}{3}V_{dc}$
P	O	N	2	2	V_{dc}	$\frac{\sqrt{3}}{3}V_{dc}$
P	N	P	3	3	$\frac{2}{3}V_{dc}$	$-\frac{2\sqrt{3}}{3}V_{dc}$
P	N	O	4	4	V_{dc}	$-\frac{\sqrt{3}}{3}V_{dc}$
P	N	N	5	5	$\frac{4}{3}V_{dc}$	0
O	P	N	6	6	0	$\frac{2\sqrt{3}}{3}V_{dc}$
O	N	P	7	7	0	$-\frac{2\sqrt{3}}{3}V_{dc}$
N	P	P	8	8	$-\frac{4}{3}V_{dc}$	0
N	P	O	9	9	$-V_{dc}$	$\frac{\sqrt{3}}{3}V_{dc}$
N	P	N	10	10	$-\frac{2}{3}V_{dc}$	$\frac{2\sqrt{3}}{3}V_{dc}$
N	O	P	11	11	V_{dc}	$-\frac{\sqrt{3}}{3}V_{dc}$
N	N	P	12	12	$-\frac{2}{3}V_{dc}$	$-\frac{2\sqrt{3}}{3}V_{dc}$
P	P	O	13	13	$\frac{1}{3}V_{dc}$	$\frac{\sqrt{3}}{3}V_{dc}$
O	O	N	14	13	$\frac{1}{3}V_{dc}$	$\frac{\sqrt{3}}{3}V_{dc}$
P	O	P	15	14	$\frac{1}{3}V_{dc}$	$-\frac{\sqrt{3}}{3}V_{dc}$
O	N	O	16	14	$\frac{1}{3}V_{dc}$	$-\frac{\sqrt{3}}{3}V_{dc}$
P	O	O	17	15	$\frac{2}{3}V_{dc}$	0
O	N	N	18	15	$\frac{2}{3}V_{dc}$	0
O	P	P	19	16	$-\frac{2}{3}V_{dc}$	0
N	O	O	20	16	$-\frac{2}{3}V_{dc}$	0
O	P	O	21	17	$-\frac{1}{3}V_{dc}$	$\frac{\sqrt{3}}{3}V_{dc}$
N	O	N	22	17	$-\frac{1}{3}V_{dc}$	$\frac{\sqrt{3}}{3}V_{dc}$
N	N	O	23	18	$-\frac{1}{3}V_{dc}$	$-\frac{\sqrt{3}}{3}V_{dc}$
O	O	P	24	18	$-\frac{1}{3}V_{dc}$	$-\frac{\sqrt{3}}{3}V_{dc}$
P	P	P	25	19	0	0
O	O	O	26	19	0	0
N	N	N	27	19	0	0

different voltage vector is σ.

With the assumption that the filter and grid are balanced, the phase currents and the grid voltages also can be transformed into $\alpha\beta$ coordinates.

$$\mathbf{i} = \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{8.2}$$

$$\mathbf{e} = \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{8.3}$$

The current dynamics can be described as

$$L\frac{d\mathbf{i}}{dt}+R\mathbf{i}+\mathbf{e}=\mathbf{v}. \tag{8.4}$$

If we define the system state as $x(t)=[i_\alpha\ i_\beta]$ and define $\sigma:[-\infty,\infty)\rightarrow\Xi=\{1,2,...,19\}$ as a piecewise constant function, which is a mapping from the state-space to the index of the active voltage vector, a hybrid model of the inverter can be established as

$$\dot{x}(t)=Ax(t)+B_\sigma, \tag{8.5}$$

where

$$A=\begin{bmatrix}-\frac{R}{L} & 0\\ 0 & -\frac{R}{L}\end{bmatrix} \qquad B_\sigma=\begin{bmatrix}\frac{v_\alpha(\sigma)-e_\alpha}{L}\\ \frac{v_\beta(\sigma)-e_\beta}{L}\end{bmatrix}.$$

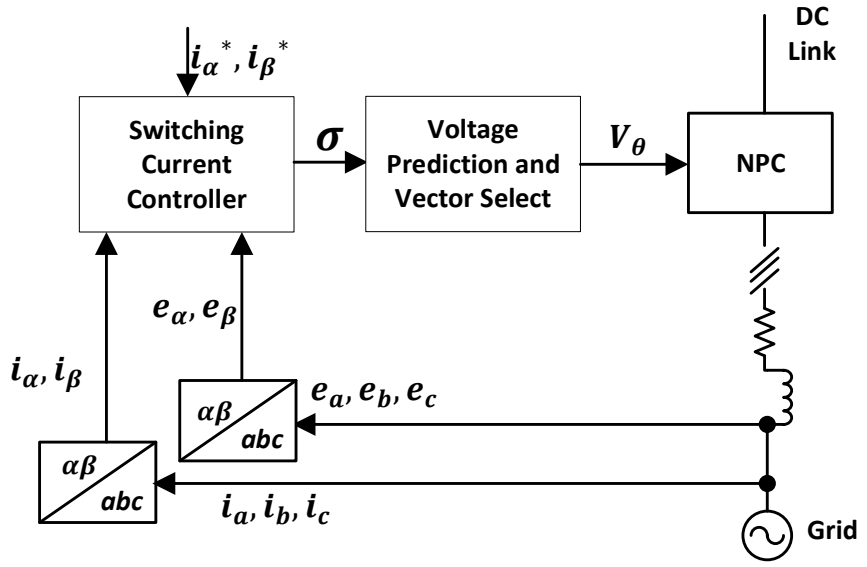


Figure 8.3: Setup of the grid-connected inverter

8.2 Current Control Law Design

8.2.1 Online Implementation

Before presenting the control design, we give the entire system architecture in Figure 8.3. The three-phase grid currents and grid voltages are measured. Then the measured grid currents and grid voltages are converted to $\alpha\beta$-frame respectively. These measured data along with the current references are transmitted to the switching current controller which determines the voltage vector θ. Then in order to keep the two capacitor voltages balanced, these two voltage are predicted for the next sampling period. The switching state, which results in a smaller

voltage deviation, will be selected and the corresponding switching signals are generated to control the twelve power switches.

8.2.2 Stabilization of the Error System

If the tracking error is defined as $\varepsilon(t) = x(t) - \mathbf{i}^*$, the tracking error system is

$$\dot{\varepsilon}(t) = A\varepsilon(t) + \hat{B}_\sigma \tag{8.6}$$

where

$$A = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \qquad \hat{B}_\sigma = \begin{bmatrix} \frac{v_\alpha(\sigma)-e_\alpha}{L} - \frac{R}{L}i_\alpha^* - \frac{di_\alpha^*}{dt} \\ \frac{v_\beta(\sigma)-e_\beta}{L} - \frac{R}{L}i_\beta^* - \frac{di_\beta^*}{dt} \end{bmatrix}.$$

Hence, the proposed current controller is expected to stabilize the tracking error $\varepsilon(t)$ to the origin. The following theorem states that under some conditions the designed switching control law will drive the error system (8.6) to track the current reference with guaranteed closed-loop stability.

Theorem 8.1. *Define $\lambda = [\lambda_1, \lambda_2, ..., \lambda_{19}]^T$ belongs to the set Λ composed by all non-negative vectors such that $\sum_{i=1}^{19} \lambda_i = 1$. Consider the error system (8.6) and given matrix $Q > 0$, if there exists matrix $P > 0$ and $\lambda \in \Lambda$, $i \in \Xi$, such that*

$$A^T P + PA + Q < 0 \tag{8.7}$$

$$A\varepsilon_e + \hat{B}_\lambda = 0 \tag{8.8}$$

where

$$\hat{B}_\lambda = \sum_{i=1}^{19} \lambda_i \hat{B}_i \tag{8.9}$$

then under the switching law

$$\sigma(\varepsilon) = arg \min_{i \in \Xi} \varepsilon^T(t) P \hat{B}_i \tag{8.10}$$

the error system (8.6) is asymptotically stable.

Proof. Consider a Lyapunov functional

$$V(\varepsilon(t)) = \varepsilon^T(t) P \varepsilon(t). \tag{8.11}$$

Then along the solution of (8.6), the derivative of the chosen Lyapunov functional can be calculated:

$$\begin{aligned}\dot{V}(\varepsilon(t)) &= \dot{\varepsilon}^T(t)P\varepsilon(t) + \varepsilon^T(t)P\dot{\varepsilon}(t)\\ &= (A\varepsilon(t) + \hat{B}_\sigma)^T P\varepsilon(t) + \varepsilon^T(t)P(A\varepsilon(t) + \hat{B}_\sigma)\\ &= \varepsilon^T(t)(A^TP + PA)\varepsilon(t) + 2\varepsilon^T(t)P\hat{B}_\sigma.\end{aligned}$$

Under the switching law (8.10),

$$\begin{aligned}\dot{V}(\varepsilon(t)) &= \min_{i\in\Xi}\left[\varepsilon^T(t)(A^TP + PA)\varepsilon(t) + 2\varepsilon^T(t)P\hat{B}_i\right]\\ &= \min_{i\in\Xi}\left[\varepsilon^T(t)(A^TP + PA + Q)\varepsilon(t) + 2\varepsilon^T(t)P\hat{B}_i\right]\\ &\quad - \varepsilon^T(t)Q\varepsilon(t).\end{aligned} \tag{8.12}$$

According to the result of [139], the proof continues:

$$\begin{aligned}\dot{V}(\varepsilon(t)) &= \min_{\lambda\in\Lambda}\left[\varepsilon^T(t)(A^TP + PA + Q)\varepsilon(t) + 2\varepsilon^T(t)P\hat{B}_\lambda\right]\\ &\quad - \varepsilon^T(t)Q\varepsilon(t).\end{aligned} \tag{8.13}$$

Since the equilibrium of the error system $\varepsilon_e \equiv 0$ and the conditions (8.7)(8.8),

$$\begin{aligned}\dot{V}(\varepsilon(t)) &= \min_{\lambda\in\Lambda}[\varepsilon^T(t)(A^TP + PA + Q)\varepsilon(t)\\ &\quad + 2\varepsilon^T(t)(PA\varepsilon_e + P\hat{B}_\lambda)] - \varepsilon^T(t)Q\varepsilon(t)\\ &< -\varepsilon^T(t)Q\varepsilon(t)\end{aligned} \tag{8.14}$$

Hence based on the switched Lyapunov theory, the error system (8.6) is asymptotically stable under the switching law (8.10). □

Since the state matrix A is Hurwitz , if a positive definite matrix P exists, condition (8.7) is satisfied. Next, it will be shown that there always exists $\lambda \in \Lambda$ such that the condition (8.8) is fulfilled.

$$A\varepsilon_e + \hat{B}_\lambda = \hat{B}_\lambda = \frac{1}{L}\left(\sum_{i=1}^{19}\lambda_i\mathbf{v}_i - \left(L\frac{d\mathbf{i}^*}{dt} + R\mathbf{i}^* + \mathbf{e}\right)\right) \tag{8.15}$$

Based on Figure 8.2, the term $\sum_{i=1}^{19}\lambda_i\mathbf{v}_i$ is all the attainable voltage vectors in the $\alpha\beta$ coordinates with the nineteen switching modes. It is easy to show that the term $\left(L\frac{d\mathbf{i}^*}{dt} + R\mathbf{i}^* + \mathbf{e}\right)$ is the reference voltage vector $\mathbf{v}^*$ of the inverter based on the current dynamic equation (8.4). Hence, it is obvious that by choosing appropriate $\lambda \in \Lambda$, the reference voltage vector $\mathbf{v}^* =$

$\sum_{i=1}^{19} \lambda_i \mathbf{v}_i$, that is,

$$A\varepsilon_e + \hat{B}_\lambda = \hat{B}_\lambda = 0. \tag{8.16}$$

Remark 8.2. The controller variables P can be obtained off-line by solving the LMI conditions (8.7) through MATLAB combined with YALMIP interface [153]. Hence, the online computational of the switching rule (8.10) is simple and straightforward.

8.2.3 Capacitor Voltage Deviation Prediction

The neutral-point balancing problem for NPC inverters has attracted a great deal of research interests in recent years. Since most of control methods proposed for NPC are based on PWM techniques, in the literature hysteresis control or PI controller are used mostly to balance the neutral point in conjunction with PWM [88, 155]. In this chapter, a capacitor voltage prediction method, which is used in model predictive control [4], are adapted to balance the neutral point. Once defined the sampling frequency T_s, the two capacitor voltage can be calculated by the

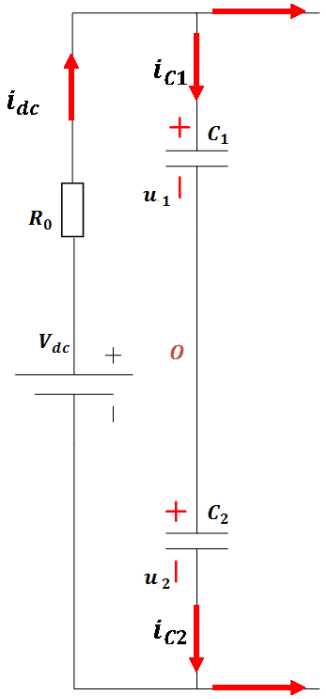


Figure 8.4: Circuit diagram about DC side current follow of the NPC inverter

following equation:

$$u_1(k+1) = u_1(k) + \frac{1}{C_1} i_{C1} T_s \tag{8.17}$$

$$u_2(k+1) = u_2(k) + \frac{1}{C_2} i_{C2} T_s \tag{8.18}$$

where i_{C1} and i_{C2} are the currents flowing through two capacitor respectively as shown in Figure 8.4. Then based on Kirchhoff's circuit laws (KCL), the capacitor currents can be calculated as:

$$i_{C1}(k) = i_{dc}(k) - G_{1a}i_a(k) - G_{1b}i_b(k) - G_{1c}i_c(k) \tag{8.19}$$

$$i_{C2}(k) = i_{dc}(k) + G_{2a}i_a(k) + G_{2b}i_b(k) + G_{2c}i_c(k) \tag{8.20}$$

where i_{dc} is the current from the voltage source V_{dc}. The variables $G_{1x}(\theta)$ and $G_{2x}(\theta)$ are dependent on the switching state of the phase x ($x = a/b/c$). The rules to decide the value of $G_{1x}(\theta)$ and $G_{2x}(\theta)$ are as follow:

- $G_{1x}(\theta) = 1$ when the switching state of phase x is P.
- $G_{1x}(\theta) = 0$ when the switching state of phase x is O or N.
- $G_{2x}(\theta) = 1$ when the switching state of phase x is N.
- $G_{2x}(\theta) = 0$ when the switching state of phase x is P or O.

Hence, the deviation of the two capacitor voltage is defined as:

$$\Delta u = |u_1 - u_2| \tag{8.21}$$

We assume the two capacitors have same value ($C = C_1 = C_2$). Then substituting (8.17) to (8.20) into the equation above, one can have:

$$\Delta u(k+1)(\theta) = \left| u_1(k) - u_2(k) - \frac{T_s}{C}\left((G_{1a}(\theta) - G_{2a}(\theta))i_a(k) + (G_{1b}(\theta) - G_{2b}(\theta))i_b(k) + (G_{1c}(\theta) - G_{2c}(\theta))i_c(k)\right)\right| \tag{8.22}$$

Hence, for a specific voltage vector σ, there may exsit several available switching states with index $\theta = i/j/p$. A simple minimization problem can be formed as:

$$\theta = \arg\min(\Delta u(k+1)(\tau)),\ \tau = i, j, p. \tag{8.23}$$

In this way, the switching state which gives the minimum of capacitor voltages deviation will be selected.

Table 8.3: Grid-connected NPC inverter parameters

Three-phase DC-AC inverter Configuration	
V_{dc}	$600V$
L	$10mH$
R	10Ω
Grid Voltage	$110V$
Grid Frequency	$50Hz$
Sampling Frequency	$10kHz$

8.3 Simulation Results

Both the grid-connected inverter and the controller are implemented in MATLAB Simulink, and the parameters of the nominal operation are given in Table 8.3. Before the real-time simulation, the LMI (8.7) was solved with give unity matrix Q. The pre-calculated parameters of the switching current controller was obtained as:

$$P = 10^5 \times \begin{bmatrix} 2.4751 & 0 \\ 0 & 2.4751 \end{bmatrix} \tag{8.24}$$

In the first case, in order to test the stability of the whole system under the proposed switching law (8.10), the peak value of the current reference is set as $10A$ and the frequency is set as $50Hz$. As shown in Figure 8.5, the grid currents are controlled to track the current references with reasonable ripple. From $0s$ to $0.1s$, the capacitor prediction is disabled. As it can be seen in the figure, the capacitor voltages are not balanced. Then from $0.1s$, the capacitor prediction is enabled. Thus, the deviation of the capacitor voltages decrease dramatically. Furthermore, the line voltages U_{AB}, U_{AC}, and U_{BC} are shown in Figure 8.6. The general shape of the waveforms are sinusoidal. There are three voltage levels for the line voltage, which is the main advantage of the NPC inverter over the conventional two-level inverter. The total harmonic distortion of the gird current also has been analysed. From Figure 8.7, the THD of grid current is 4.16% with the capacitor voltage prediction algorithm and the THD value increases to 4.76% without the prediction algorithm.

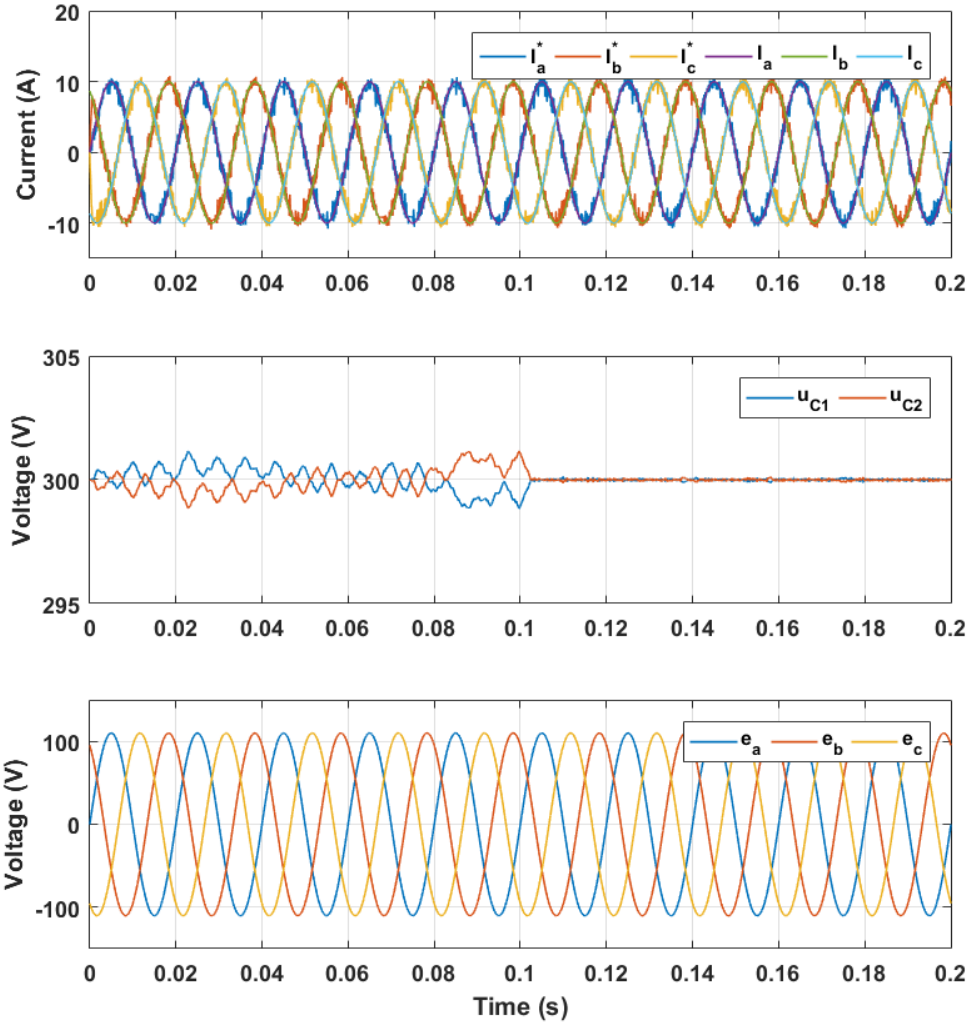


Figure 8.5: The waveforms of the grid currents i_a, i_b, i_c in *abc*-frame as well as the current references, the capacitor voltage u_{C1} and u_{C2}, grid voltages e_a, e_b, e_c.

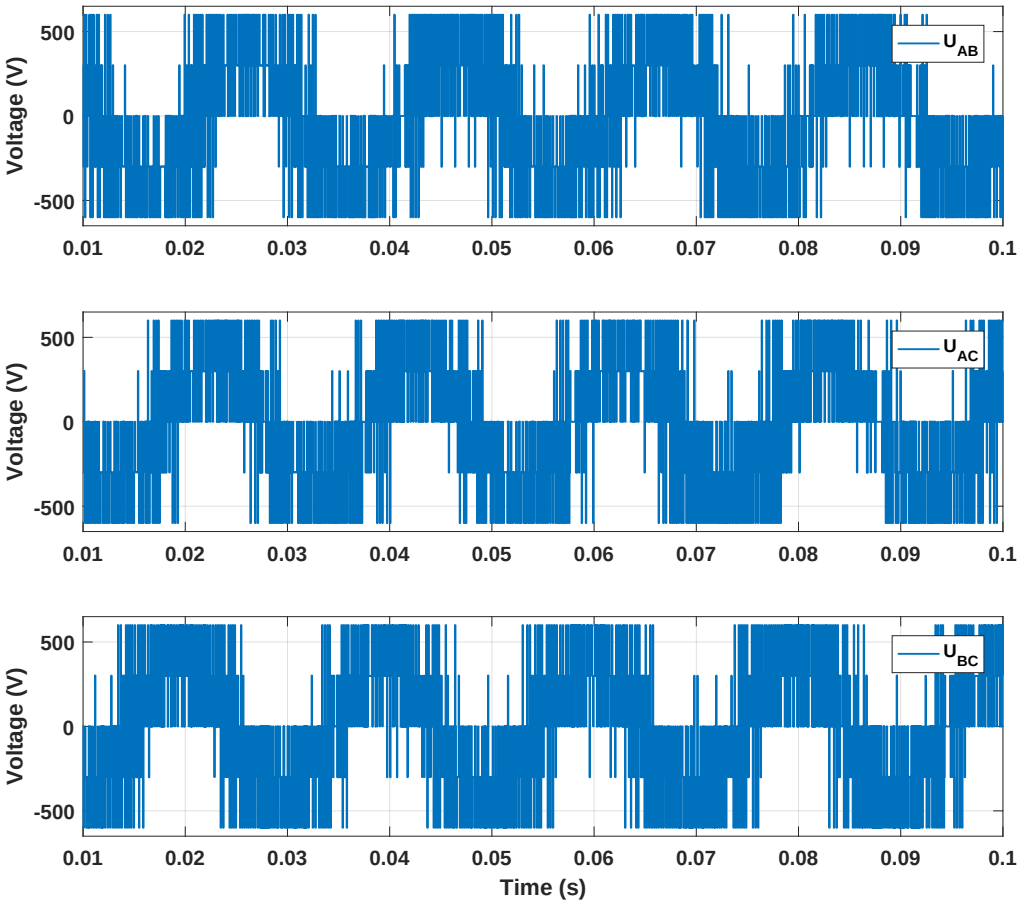
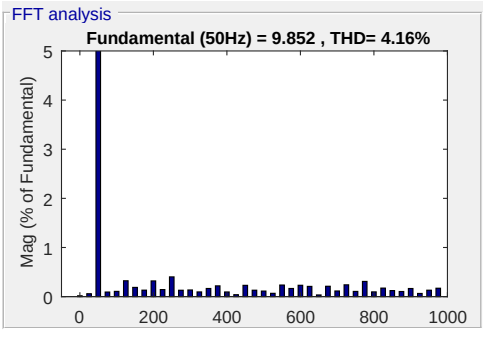
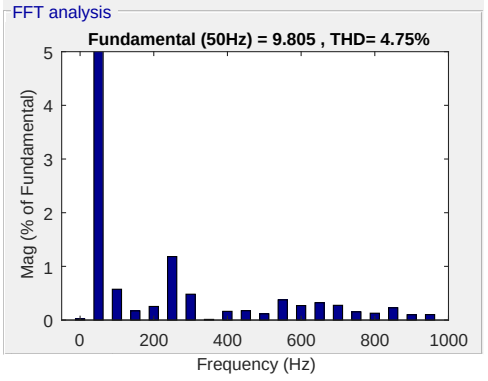


Figure 8.6: The waveforms and the mean of the line voltages U_{AB}, U_{AC}, U_{BC}



(a) With prediction algorithm



(b) Without prediction algorithm

Figure 8.7: Total Harmonic Distortion (THD) of Grid Current before and after capacitor voltage prediction enabled

8.4 Summary

In this chapter, the control scheme proposed in Chapter 6 is extended to a more complicated topology: three-phase NPC inverter. In order to solve the issue of the neutral point balance, a capacitor voltage balancing control, which has been used with MPC control, has been adopted. Simulation results is presented to demonstrate the effectiveness of the proposed method. In next chapter, experimental verification will be carried out on a simpler case, which replace the grid load with a three-phase RL load.

Chapter 9

Experiment Validation on Three Phase NPC Inverters

In order to validate the control algorithm proposed in Chapter 8, experiments have been carried out. Since the grid-connected scenario is difficult to set up in the laboratory, a special case is considered, which is NPC inverter with three-phase RL load. The proposed method can be easily extended to this case by assuming the grid voltages are equal to zero.

9.1 Switching Controller for NPC Inverters with RL Load

For legibility, the proposed control scheme in Chapter 8 is re-presented below.

9.1.1 Phase Current Controller Design

By defining the system state as $x(t) = [i_\alpha \; i_\beta]$, which are the phase current in $\alpha\beta$ coordinates and define $\sigma : [-\infty, \infty) \to \Xi = \{1, 2, ..., 19\}$ as a piecewise constant function, which is a mapping from the state-space to the index of the active voltage vector, a hybrid model of the inverter can be established as

$$\dot{x}(t) = Ax(t) + B_\sigma, \tag{9.1}$$

where

$$A = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \qquad B_\sigma = \begin{bmatrix} \frac{v_\alpha(\sigma)}{L} \\ \frac{v_\beta(\sigma)}{L} \end{bmatrix}.$$

If the tracking error is defined as $\varepsilon(t) = x(t) - \mathbf{i}^*$ where i^* is the current reference in complex form, the tracking error system is

$$\dot{\varepsilon}(t) = A\varepsilon(t) + \hat{B}_\sigma \tag{9.2}$$

where

$$A = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \qquad \hat{B}_\sigma = \begin{bmatrix} \frac{v_\alpha(\sigma)}{L} - \frac{R}{L} i_\alpha^* - \frac{di_\alpha^*}{dt} \\ \frac{v_\beta(\sigma)}{L} - \frac{R}{L} i_\beta^* - \frac{di_\beta^*}{dt} \end{bmatrix}.$$

Hence, the proposed current controller is expected to stabilize the tracking error $\varepsilon(t)$ to the origin. The following theorem states that under some conditions the designed switching control law will drive the error system (9.2) to track the current reference with guaranteed closed-loop stability.

Theorem 9.1. *Define $\lambda = [\lambda_1, \lambda_2, ..., \lambda_{19}]^T$ belong to the set Λ composed by all non-negative vectors such that $\sum_{i=1}^{19} \lambda_i = 1$. Consider the error system (9.2) and given matrix $Q > 0$, if there exists matrix $P > 0$ and $\lambda \in \Lambda$, $i \in \Xi$, such that*

$$A^T P + PA + Q < 0 \tag{9.3}$$

$$A\varepsilon_e + \hat{B}_\lambda = 0 \tag{9.4}$$

where

$$\hat{B}_\lambda = \sum_{i=1}^{19} \lambda_i \hat{B}_i \tag{9.5}$$

then under the switching law

$$\sigma(\varepsilon) = arg \min_{i \in \Xi} \varepsilon^T(t) P \hat{B}_i \tag{9.6}$$

the error system (9.2) is asymptotically stable.

9.1.2 Capacitor Voltage Deviation Prediction

For a specific voltage vector σ, there may exist several available switching states with index $\theta = i/j/p$. A simple minimization problem can be formed as:

$$\theta = \arg\min(\Delta u(k+1)(\tau)),\ \tau = i, j, p. \tag{9.7}$$

where

$$\Delta u(k+1)(\theta) = \left| u_1(k) - u_2(k) - \frac{T_s}{C}\left((G_{1a}(\theta) - G_{2a}(\theta))i_a(k) + (G_{1b}(\theta) - G_{2b}(\theta))i_b(k) + (G_{1c}(\theta) - G_{2c}(\theta))i_c(k)\right)\right| \tag{9.8}$$

and

- $G_{1x}(\theta) = 1$ when the switching state of phase x is P.

- $G_{1x}(\theta) = 0$ when the switching state of phase x is O or N.
- $G_{2x}(\theta) = 1$ when the switching state of phase x is N.
- $G_{2x}(\theta) = 0$ when the switching state of phase x is P or O.

9.2 SEMIKRON Three Level Evaluation Inverter

Since designing a three-phase NPC inverter is time-consuming, the SEMIKRON three level evaluation inverter as shown in Figure 9.1 is adopted as the control target and more efforts can be placed on control algorithm implementation, which is more important for this thesis. It is able to carry a maximum current of $100A_{RMS}$ at a DC-link voltage of up to $750V_{DC}$. Drivers and sensors (voltage, current, temperature) are on board. The inverter offers a high degree of self-protection: overvoltage, overcurrent, overtemperature and desaturation events are monitored and lead to a safe shut down.

Figure 9.1: SEMIKRON three level evaluation inverter kit

9.3 Experimental Setup

For safety purpose, the NPC inverter is operated at low voltage and low current. The parameters of the experimental configuration are shown in Table 9.1. Since the onboard current sensors are designed for high current application, the resolution of the measured current is very poor for low current configuration. Hence, a three-phase low current sensor board was designed.

Table 9.1: NPC inverter experiment configuration

Three-phase DC-AC inverter Configuration	
V_{dc}	$25V$
L	$5mH$
R	10Ω
Current Peak Value	$2A$
Current Frequency	$50Hz$
Switching/Sampling Frequency	$10kHz$

9.4 Implementation based on FPGA

The SEMIKRON three level (3L) evaluation inverter provides a 40 pin control interface, which can be easily connected to Altera DE2-115 Development FPGA board. Hence, the control algorithm is implemented based on Altera FPGA. The main difference between FPGA and the common used DSP controller is that FPGA can only accepts digital signals and produces digital signals. Hence, the signal processing flow can be described as follow:

- Phase currents and capacitor voltages will be measured by corresponding sensors in the format of voltage signal output.
- In order to passing signal to FPGA, the analog signals from sensors will go through the Analog-to-Digital Conversion(ADC) chips: ADS1204. The output of ADS1204 are series of 1-bit boolean numbers.
- The digital signals from ADCs will be passed to FPGA. Hardware programming code is written using software Quartus II, which interprets the signals and generate the switching signal based on the proposed control algorithms.

In following part, the VHDL modules developed in Quartus II will be explained in details.

9.4.1 VHDL Modules

9.4.1.1 Digital Filter

In order to translate the 1-bit signal from the ADC to meaning value, a $Sinc^3$ is implemented. The inputs and outputs of the module (Figure 9.2) are as follow:

Inputs:

- *RESN*: System reset signal.

- *MOUT*: 1-bit digital signal from ADC1204.
- *MCLK*: Sampling clock of ADC1204.
- *CNR*: Decimation clock with ratio 256

Outputs:

- *CN*5: 25-bits processed signal, which is the fix-point number of the measured signal.

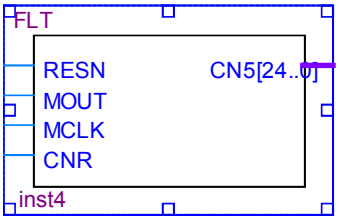


Figure 9.2: VHDL Module: digital filter

9.4.1.2 Current Sensor Calibration

Since the output of digital filter is the voltage signal regulated by ADC, there is a relationship between the voltage signal and the actual current signal measured. This VHDL as shown in Figure 9.3 will translate the output from digital filter to the correct current signal.

Inputs:

- *RESN*: System reset signal.
- *clk*: System clock signal
- *I_IN*: 25-bits digital filter output

Outputs:

- *I_OUT*: 22-bits current signal in fix-point.

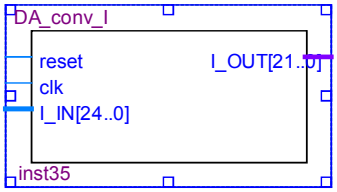


Figure 9.3: VHDL Module: current sensor calibration

9.4.1.3 Voltage Sensor Calibration

Same as current sensor, there is a fix relationship between the voltage signal from the digital filter and the actual voltage signal measured. This VHDL as shown in Figure 9.4 will translate the output from digital filter to the correct voltage signal.

Inputs:

- *RESN*: System reset signal.
- *clk*: System clock signal
- *V_IN*: 25-bits digital filter output

Outputs:

- *V_OUT*: 25-bits voltage signal in fix-point.

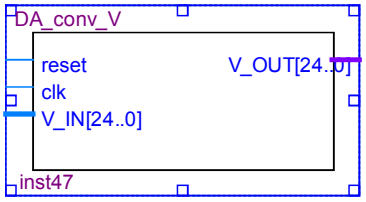


Figure 9.4: VHDL Module: voltage sensor calibration

9.4.1.4 Current Reference Generation

The module shown in Figure 9.5 generates three-phase reference signals.

Inputs:

- *RESN*: System reset signal.

- *clk*: System clock signal

Outputs:

- *REF_U*: 22-bits fix-point reference signal of phase A.
- *REF_V*: 22-bits fix-point reference signal of phase B.
- *REF_W*: 22-bits fix-point reference signal of phase C.

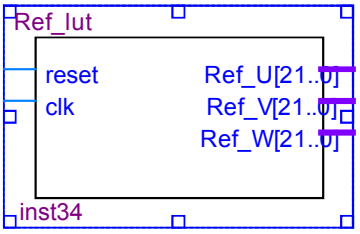


Figure 9.5: VHDL Module: current reference generation

9.4.1.5 $\alpha\beta$ Transformation

The module shown in Figure 9.6 transfering the three-phase signal in *abc* coordinate to $\alpha\beta$ coordinates.

Inputs:

- *RESN*: System reset signal.
- *clk*: System clock signal
- *Sig_U*: 22-bits phase A of the three phase signals
- *Sig_U*:22-bits phase B of the three phase signals
- *Sig_U*:22-bits phase C of the three phase signals

Outputs:

- *Sig_A*: 28-bits the α component of the input signal
- *Sig_B*:28-bits the β component of the input signal

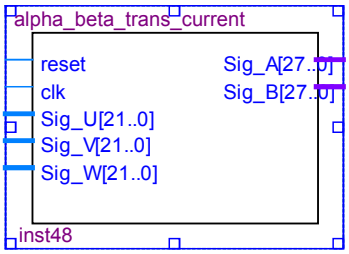


Figure 9.6: VHDL Module: $\alpha\beta$ transformation

9.4.1.6 Switching Controller

The proposed control algorithm is implemented in this module as shown in Figure 9.7.

Inputs:

- *RESN*: System reset signal.
- *clk*: Switching clock, which is $9.7kHz$
- *clk*1: Calculation clock as during each switching period, a series of calculation need to be done. Hence, this clock is much faster than the switching clock.
- *IAC_U_A*:25-bits fix-point phase A current signal from the current calibration module.
- *IAC_V_A*:25-bits fix-point phase B current signal from the current calibration module.
- *IAC_W_A*:25-bits fix-point phase C current signal from the current calibration module.
- *VDC_TOP_A*:25-bits fix-point top capacitor voltage signal from the voltage calibration module.
- *VDC_BOT_A*:25-bits fix-point bottom capacitor voltage from the voltage calibration module.

Outputs:

- *Index*: the 5-bits index of the selected switching state.

9.4.1.7 Switching Signal to Leg Signal

This module, shown in Figure 9.8, maps the index of the desired switching state to the state of each leg according to Table 8.2.

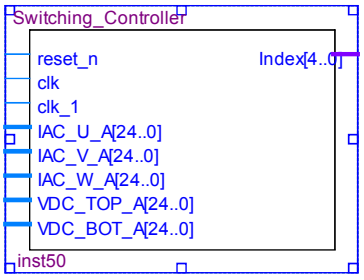


Figure 9.7: VHDL Module: switching controller

Inputs:

- *RESN*: System reset signal.
- *clk*: Switching clock, which is $9.7kHz$
- *Index*: the 5-bits index of the selected switching state.

Outputs:

- *Leg_sig_U*: the 2-bits leg signal of phase A
- *Leg_sig_V*: the 2-bits leg signal of phase B
- *Leg_sig_W*: the 2-bits leg signal of phase C

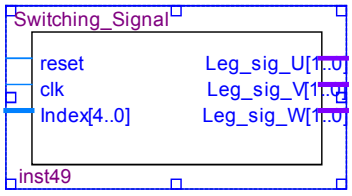


Figure 9.8: VHDL Module: switching signal to leg signal

9.4.1.8 Leg Signal to Switches

This module, shown in Figure 9.9, maps the leg signal to the switching signal for each power switches according to Table 8.1.

Inputs:

- *RESN*: System reset signal.
- *clk*: Switching clock, which is $9.7kHz$
- *Leg_sig*:the 2-bits leg signal

Outputs:

- $T1$: the 1-bit switching signal for the switch S_1
- $T2$: the 1-bit switching signal for the switch S_2
- $T3$: the 1-bit switching signal for the switch S_3
- $T4$: the 1-bit switching signal for the switch S_4

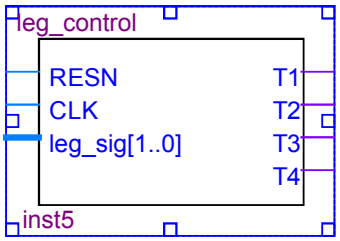


Figure 9.9: VHDL Module: leg Signal to switches

9.5 Experimental Results

Figure 9.10 shows the whole experiment platform, which includes the SEMIKRON three level (3L) evaluation inverter, three-phase RL loads, the DE2-115 FPGA board, voltage source power supply, oscilloscope, and a PC. The setting up parameters are shown in the in Table 9.1. The VHDL module are implemented on the Altera Quartus II which is programmable logic device design software produced by Altera. Then the design are downloaded to the DE-115 FPGA board. The voltage source power supply is connected to the DC input of the SEMIKRON three level (3L) evaluation inverter. The phase/line voltages and currents are measured by the oscilloscope.

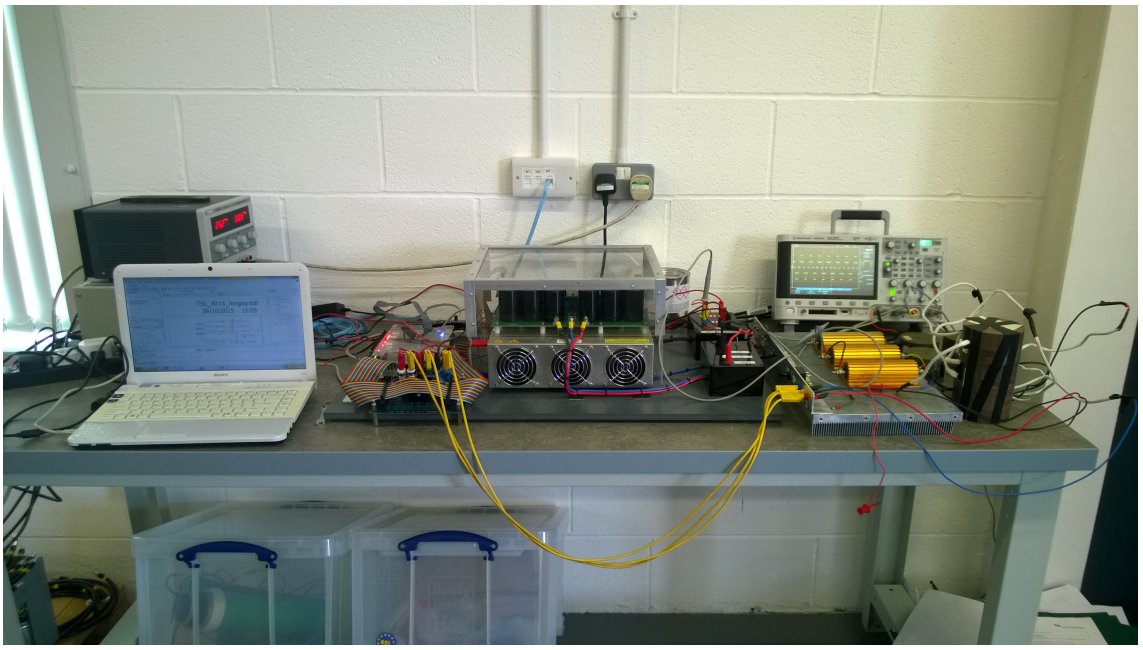


Figure 9.10: Whole experiment setting up

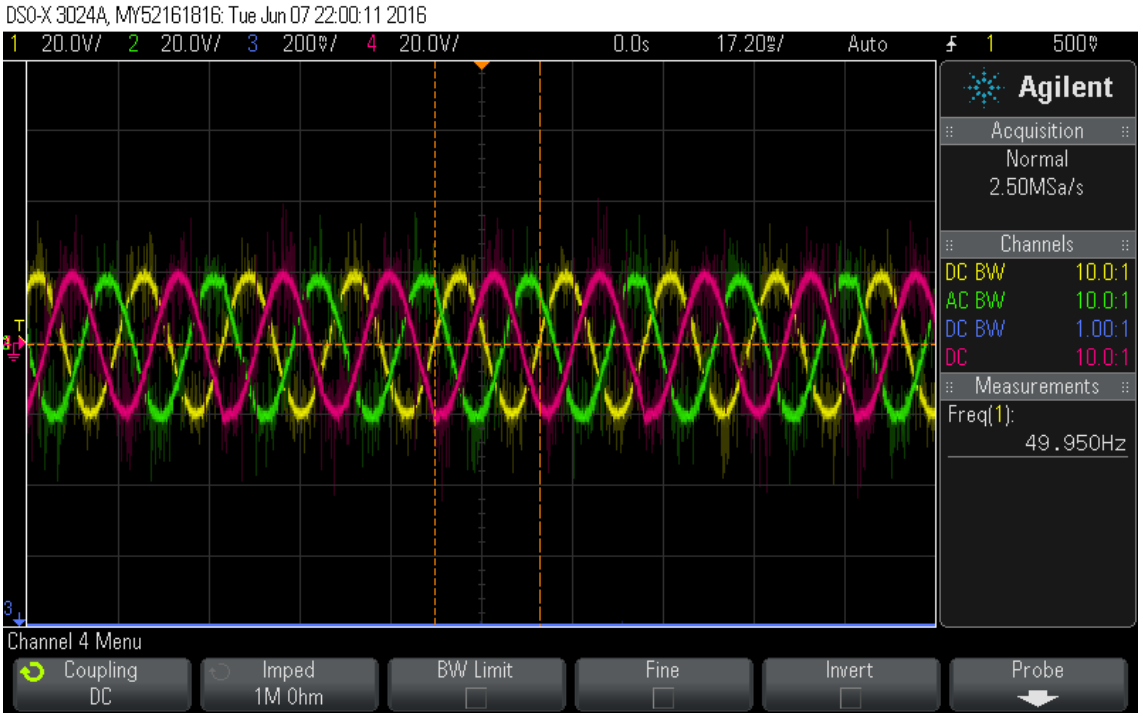


Figure 9.11: Three-phase current signals

The waveforms of the phase currents are shown in Figure 9.11. The frequency of the currents is $50Hz$ as expected. The phase shift between the three-phase are 120 degree. In addition, the peak value of the currents is $2A$ as the oscilloscope probes have gain of ten.

The line voltage between phase A and phase B are shown in Figure 9.12. One can clearly see the three voltage levels, which is the reason for the name ”three-level” NPC inverter. The

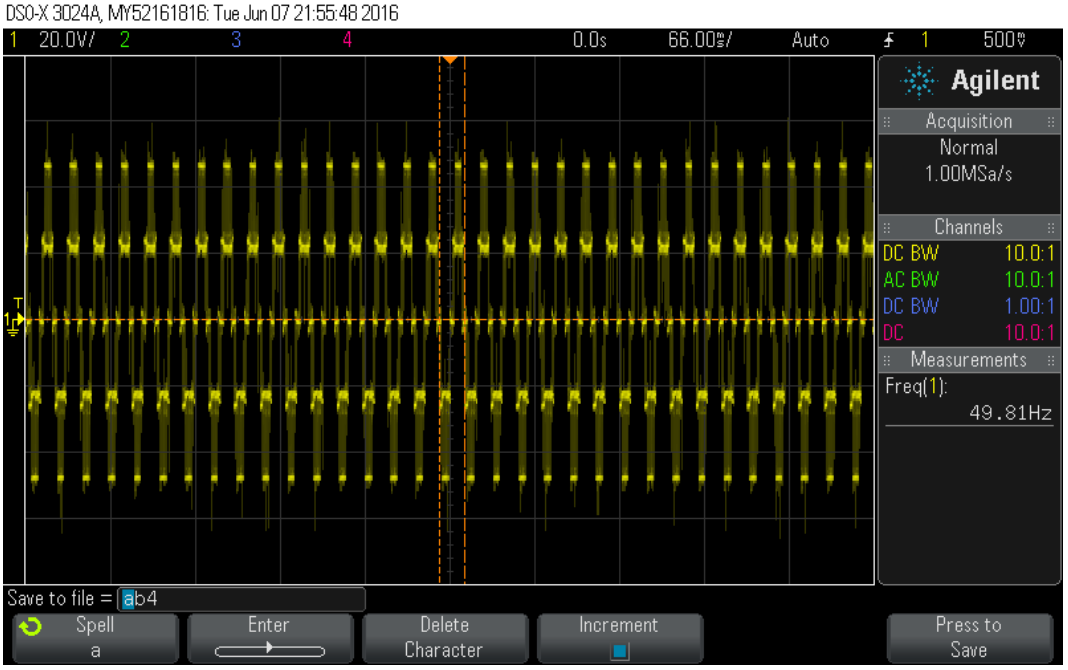


Figure 9.12: Line A to B voltage

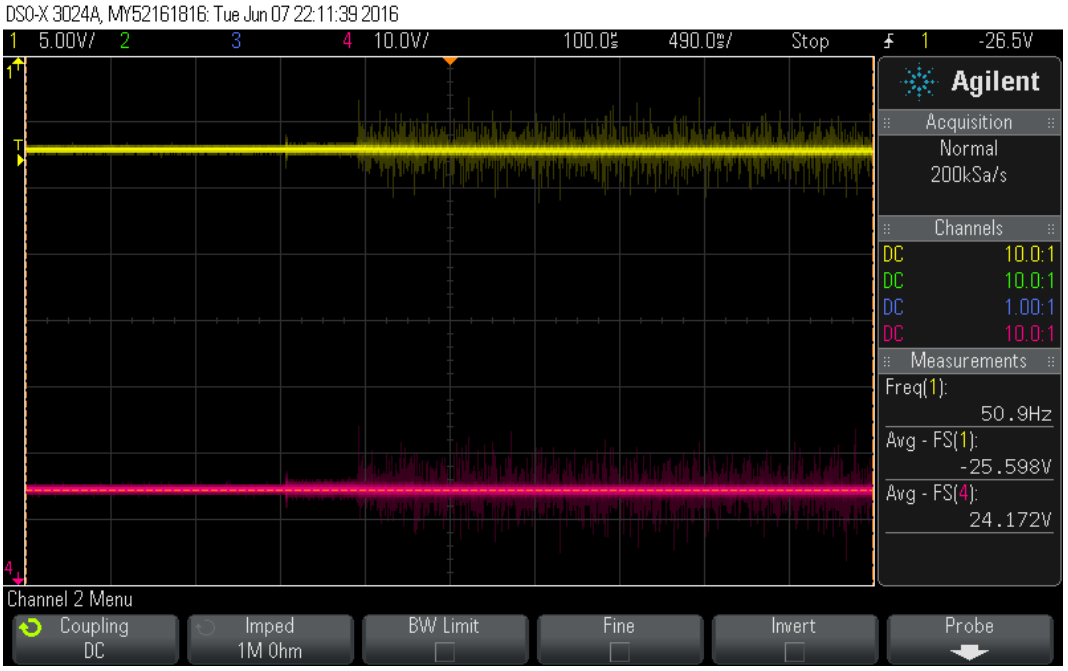


Figure 9.13: Capacitor Voltages: top capacitor (Yellow) and bottom capacitor (Red)

frequency of the line voltage is also $50Hz$.

The performance of the capacitor balancing algorithms is demonstrated in the Figure 9.13. The mean value of the top capacitor voltage is $25.6V$, while the mean value of the bottom capacitor voltage is $24.2V$. Hence, the deviation of the capacitor voltages is $1.4V$. Although the performance is not as good as the simulation result, the deviation is still acceptable and it is not growing as time goes on.

9.6 Summary

In this chapter, the information about verification of the proposed control scheme on the three-phase NPC inverter with RL load has been explained in details. Firstly, the controller design procedure has been presented first. Then the configuration of the SEMIKRON three level evaluation inverter, which is used in the experiment, is given. The control scheme is implemented on FPGA in the language of VHDL. In addition, the essential VHDL modules are presented from the input information processing, controller implementation, to the output switching signal generation. In the end, the experimental results is displayed to prove the effectiveness of the whole control scheme.

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Chapter 10

Conclusions and Future Research

10.1 Conclusions

In this chapter, the novel hybrid modelling and control techniques for DC-DC converters and DC-AC inverters are compared with each others and traditional control methods, which are summarized in Figure 10.1. It is no doubt that the tradional design procedure of the linear controller based on the state-space averaged approach is more complicated, e.g., the setting of poles and zeros, the selection of reasonable crossover frequency and phase margin. The controllers designed are highly restricted on the system model topologies. Any change of model may result in re-design, and this impose a restriction on fully automated design. On the other hand, for the state-space averaged approach, the modelling and controller design is around a operating point or a steady state equilibrium. In some practical situation, additional constraints need to be considered, e.g., safety measurement, current limiting or soft-starting, gross changes of operation point. Under these condition, the control problem becomes more complicated. Another shortcoming of the state-space averaged approach is the considerable approximation in analysis and synthesis. The hybrid nature of power converters which contains continuous and discrete dynamics has been neglected. The main disadvantages of state-space averaged approach can be summarized as below:

- Considerable approximation involved.
- Analysis and control synthesis around a specific operation point.
- Complicated design procedure, highly restricted by the model, imposing a restriction on fully automated design.
- More complicated control problem arises when constraints introduced.
- It will result in multiple control loops if more system states are involved in the controller design.

<table>
<tr><td></td><td colspan="4">DC-DC Converters</td><td colspan="4">DC-AC Inverters</td></tr>
<tr><td></td><td colspan="2">Chapter 3</td><td>Chapter 4</td><td>Chapter5</td><td>Chapter 6</td><td>Chapter7</td><td>Chapter8</td></tr>
<tr><td rowspan="2">Controller</td><td>Linear controller</td><td>MPC controller</td><td>Sampled-Data Control</td><td>Output feedback controller</td><td colspan="3">Switching Controller (Phase Current Control)</td></tr>
<tr><td colspan="4"></td><td colspan="3">Neutral Point Balancing</td></tr>
<tr><td rowspan="5">Model</td><td rowspan="5">Linear model with approximation</td><td rowspan="5">Hybrid Automaton</td><td colspan="4">Hybrid model</td></tr>
<tr><td colspan="4">Switched affine model</td></tr>
<tr><td rowspan="3">Continues model with sampling data</td><td rowspan="2">Discrete model</td><td colspan="3" rowspan="3">Continues Model</td></tr>
<tr><td>Multiple samplings</td></tr>
<tr><td>Reference dynamic included</td></tr>
<tr><td>Modulation</td><td>PWM</td><td colspan="6">No modulation</td></tr>
<tr><td>Controller design</td><td>Compensator parameter tuning (root locus or pole placement)</td><td>Cost function definition</td><td colspan="6" rowspan="2">Lyapunov stability theory</td></tr>
<tr><td>Stability</td><td>Guaranteed locally</td><td>Unsure</td></tr>
<tr><td>Implementation</td><td>Analogical or digital</td><td colspan="7">Direct digital implementation</td></tr>
<tr><td>Switching frequency</td><td>Fixed</td><td>Variable</td><td>Controllable</td><td colspan="4">Variable</td></tr>
<tr><td rowspan="2">Flexibility</td><td rowspan="2">Constraints inclusion is not straight forward</td><td rowspan="2">Constraints include directly in the cost function</td><td rowspan="2">Constraints include in the switching law</td><td>Fast sampling, slow switching</td><td rowspan="2"></td><td rowspan="2">Redundant voltage vectors for neutral point balancing</td></tr>
<tr><td>Less sensor needed</td></tr>
<tr><td>Online complexity</td><td>Depend on the control structure</td><td>Depended on prediction horizon</td><td colspan="5">Very simple</td></tr>
</table>

Figure 10.1: Comparison among different control techniques discussed in the thesis

Thus, given all the limitations of the conventional modelling and control techniques, it is worthwhile to reconsider the system analysis and controller synthesis in light of the hybrid system theory. What's more, power converters with power switches are a good candidate for hybrid theory. The hybrid models of the DC-DC converters and DC-AC converters are more precise than the traditional small signal model, which could make a well combination of the

continuous dynamics and the discrete transition.

The theory of model predictive control is suitable with the hybrid model. The control algorithm is easy to be developed. What should be mentioned is that constraints from practical requirement could be easily added in the algorithm by changing the cost function that is employed. However, the disadvantages are also obvious.

- First, the stability and robustness is generally not guaranteed.
- The prediction horizon affects the performance of the controller, but if the prediction horizon is too far away, the computation load is highly increased, which is unacceptable for high frequency implementation

The main focus of this PhD project has been put on how to developed control schemes based on switched affine models.

The challenge is that because of the affine term, the equilibrium of the system is non-trivial. The piecewise constant switching signal σ need to be carefully designed to drive the system to a designed switched equilibrium with guaranteed stability. Based on the property of power converters, the switching frequency of the switch is not infinity. Hence, a proper dwell time T_d needs to be ensured based on the practical situation.

The proposed prediction based sampling-data switching control in Chapter 4 can not only achieve guaranteed closed-loop stability, but also include constraints in a similar way as model predictive control. For this approach, the continue model with sampled data is used. The synthesis condition is given by matrices inequalities. One drawback that has been noticed is that under relative low sampling frequency, the ripple of the output is larger than other control schemes.

The results of Chapter 4 have been published with the following two papers.

- Yan, Xingda, Zhan Shu, and Suleiman M. Sharkh. "Prediction-based sampled-data control for DC-DC buck converters." *Smart Grid and Renewable Energy (SGRE), 2015 First Workshop on. IEEE, 2015.*

Motivated by the structure of the switching law proposed in Chapter 4, a novel output feedback control approach is proposed in Chapter 5. To compensate the information loss due to limited access to the state, a multiple sampling scheme is employed to derive a discrete-time switched affine model with an augmented measurement output. Based on the model, an output-feedback switching control law, which drives the system state to a set of attainable switched equilibria, is synthesized by using a quadratic state-space partition. The multiple sampling scheme not only facilitates the controller synthesis, but also improves the energy efficiency of the converter by allowing a lower average switching frequency.

The results of Chapter 5 have been published with the following paper.

- Yan, Xingda, Zhan Shu, and Suleiman M. Sharkh. "Output-feedback switching control of DC-DC cuk converters using multiple sampling." *Automatic Control Conference (CACS), 2015 International. IEEE, 2015.*

In Part II, efforts have been placed on extending this control scheme on DC-AC inverters. Compared to DC-DC converters, it is a more challenging task since there are more switching states and the reference are time-variant signals whereas DC-DC converters only have constant references. In Chapter 6, a current controller based on hybrid model of the three-phase two-level inverter has been developed, which can track the desired power reference and maintain a unity power factor at the same time. This methods has been extended to three-phase NPC inverters in Chapter 8. However, in order to solve the neutral point balancing issue, a capacitor voltage prediction algorithm modified from model predictive control has been adopted. In Chapter 7, a novel hybrid model for a grid-connected single-phase NPC inverter has been presented, which models not only the dynamic of the inverter, but also the dynamic of the current reference. However, it is still troublesome to extend this control scheme to the three-phase case. Duo to the large number of the switching states and the three current references, the stability problem formed by linear matrix inequalities is infeasible.

The results of Chapter 6 and Chapter 7 have been published with the following two papers.

- Yan, Xingda, Zhan Shu, and Suleiman M. Sharkh. "Hybrid modelling and control of single-phase grid-connected NPC inverters." *Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE. IEEE, 2016.*
- Yan, Xingda, Zhan Shu, Suleiman M. Sharkh, Zhengguang Wu, and Michael Z. Q. Chen. *"A novel current control strategy for three-phase gird-connected inverters." Control Conference (CCC), 2016 35th Chinese. IEEE, 2016.*

Generally speaking, this thesis demonstrates that advanced nonlinear control techniques based on hybrid modelling and Lyapunov stability can be a new perspective of modelling and control switched-mode power converters. These techniques have some advantages over the conventional methods.

- More accurate models by considering both continuous dynamics and discrete transitions.
- Stability of the controller is guaranteed within all attainable equilibria.
- The control algorithms can easily include additional constraints, such as switching frequency adjustment, ripple reduction.
- Convenient to implement on digital platforms.
- The online computation burden is light as the the complicated switching laws are calculated off-line.

10.2 Future Research

There are several research direction arising from this work which might be pursued in the future.

One of the issues that has not been fully addressed in this work is the influence of model parameter uncertainty. In practice, the load of power converters may vary because of a variety of reasons, such as changing of operation condition, temperature changing, etc. Since the proposed methods are based on a more precise model, it is more sensitive to the variation of certain model parameters. Hence, more research could be carried out on investigate the robustness of the proposed methods. The hybrid model could be improved to include the uncertainty of model parameters and robust control techniques could be adopted to improve the robustness of the proposed methods.

Due to funding constraints, experimental work was only carried out to verify the control method on NPC inverters with a simple RL load instead of the grid-connected case. More work is worth to be carried out to implement the proposed control method in the case of integrating renewable energy sources into the grids by NPC inverters. Moreover, the proposed control techniques could be further developed if the NPC inverters is connected to the grid with a L-C-L filter.

The control methods proposed in Chapter 4 are based on sampled-data instead of the continuous state. This could be extended to DC-AC inverters as well.

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