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High-speed Si/GeSi hetero-structure Electro Absorption Modulator

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Abstract: The ever-increasing demand for integrated, low power interconnect systems is pushing the bandwidth density of CMOS photonic devices. Taking advantage of the strong Franz-Keldysh effect in the C and L communication bands, electro-absorption modulators in Ge and GeSi are setting a new standard in terms of device footprint and power consumption for next generation photonics interconnect arrays. In this paper, we present a compact, low power electro-absorption modulator (EAM) Si/GeSi hetero-structure based on an 800 nm SOI overlayer with a modulation bandwidth of 56 GHz. The device design and fabrication tolerant process are presented, followed by the measurement analysis. Eye diagram measurements show a dynamic ER of 5.2 dB at a data rate of 56 Gb/s at 1566 nm, and calculated modulator power is 44 fJ/bit.

OCIS codes: (250.7360) Waveguide modulators; (230.2090) Electro-optical devices; (200.4650) Optical interconnects.

References and links

1. Cisco, "Cisco visual networking index: Forecast and methodology," 2015–2020 (2016).
2. R. Soref, "The past, present, and future of silicon photonics," IEEE J. Sel. Top. Quantum Electron. **12**(6), 1678–1687 (2006).
3. D. J. Thomson, C. G. Littlejohns, S. Stanković, M. Nedeljkovic, and S. A. Reynolds, *Silicon Photonics* (Wiley Encyclopedia of Electrical and Electronics Engineering, 2015).
4. Y. Chen, T. Domínguez Bucio, A. Z. Khokhar, M. Banakar, K. Grabska, F. Y. Gardes, R. Halir, Í. Molina-Fernández, P. Cheben, and J. J. He, "Experimental demonstration of an apodized-imaging chip-fiber grating coupler for Si3N4 waveguides," Opt. Lett. **42**(18), 3566–3569 (2017).
5. T. D. Bucio, A. Z. Khokhar, C. Lacava, S. Stankovic, G. Z. Mashanovich, P. Petropoulos, and F. Y. Gardes, "Material and optical properties of low-temperature NH3-free PECVD SiNx layers for photonic applications," J. Phys. D Appl. Phys. **50**(2), 025106 (2016).
6. H. Liu, C. F. Lam, and C. Johnson, "Scaling optical interconnects in datacenter networks opportunities and challenges for WDM," in *Proceedings of 2010 18th IEEE Symposium on High Performance Interconnects* (2010), pp. 113–116.
7. P. Chaisakul, D. Marris-Morini, G. Isella, D. Chrastina, M.-S. Rouifed, X. Le Roux, S. Edmond, E. Cassan, J.-R. Coudevylle, and L. Vivien, "10-Gb/s Ge/SiGe Multiple Quantum-Well Waveguide Photodetector," IEEE Photonics Technol. Lett. **23**(20), 1430–1432 (2011).
8. C. G. Littlejohns, Y. Hu, F. Y. Gardes, D. J. Thomson, S. A. Reynolds, G. Z. Mashanovic, and G. T. Reed, "50 Gb/s silicon photonics receiver with low insertion loss," IEEE Photonics Technol. Lett. **26**(7), 714–717 (2014).
9. J. J. Ackert, D. J. Thomson, L. Shen, A. C. Peacock, P. E. Jessop, G. T. Reed, G. Z. Mashanovich, and A. P. Knights, "High-speed detection at two micrometres with monolithic silicon photodiodes," Nat. Photonics **9**(6), 393–396 (2015).
10. H. T. Chen, P. Verheyen, P. De Heyn, G. Lepage, J. De Coster, P. Absil, G. Roelkens, and J. Van Campenhout, "High-responsivity low-voltage 28-Gb/s Ge p-i-n photodetector with silicon contacts," J. Lightwave Technol. **33**(4), 820–824 (2015).
11. Y. Hu, R. M. Jenkins, F. Y. Gardes, E. D. Finlayson, G. Z. Mashanovich, and G. T. Reed, "MMI for wavelength filtering and WDM on the SOI platform," in *Proceedings of IEEE Photonic Society 24th Annual Meeting* (2011), 615–616.

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12. C. Lacava, R. Marchetti, V. Vitali, I. Cristiani, G. Giuliani, M. Fournier, S. Bernabe, and P. Minzioni, "Reduced nonlinearities in 100-nm high SOI waveguides," in *Proceedings of Photonics West 2016* (2016).
13. F. Gardes, G. Reed, N. Emerson, and C. Png, "A sub-micron depletion-type photonic modulator in Silicon On Insulator," Opt. Express **13**(22), 8845–8854 (2005).
14. D. Marris-Morini, L. Vivien, G. Rasigade, J.-M. Fédéli, E. Cassan, X. Le Roux, P. Crozat, S. Maine, A. Lupu, P. Lyan, P. Rivallin, M. Halbwax, and S. Laval, "Recent progress in high-speed silicon-based optical modulators," Proc. IEEE **97**(7), 1199–1215 (2009).
15. Y. Liu, R. Ding, M. Gould, T. Baehr-Jones, Y. Yang, Y. Ma, Y. Zhang, A. E. J. Lim, T. Y. Liow, S. H. G. Teo, G. Q. Lo, and M. Hochberg, "30Ghz silicon platform for photonics system," in *Optical Interconnects Conference* (2013), pp. 27–28.
16. G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, "Silicon optical modulators," Nat. Photonics **4**(8), 518–526 (2010).
17. K. Li, D. J. Thomson, S. Liu, P. Wilson, and G. T. Reed, "A 30 Gb/s cmos driver integrated with silicon photonics MZM," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC)* (2015), pp. 311–314.
18. D. J. Thomson, F. Y. Gardes, Y. Hu, G. Mashanovich, M. Fournier, P. Grosse, J.-M. Fédéli, and G. T. Reed, "High contrast 40Gbit/s optical modulation in silicon," Opt. Express **19**(12), 11507–11516 (2011).
19. D. J. Thomson, F. Y. Gardes, J.-M. Fédéli, S. Zlatanovic, Y. Hu, B. P. P. Kuo, E. Myslivets, N. Alic, S. Radic, G. Z. Mashanovich, and G. T. Reed, "50-Gb/s silicon optical modulator," IEEE Photonics Technol. Lett. **24**(4), 234–236 (2012).
20. A. M. Gutierrez, J. V. Galan, J. Herrera, A. Brimont, D. Marris-Morini, J.-M. Fédéli, L. Vivien, and P. Sanchis, "High linear ring-assisted MZI electro-optic silicon modulators suitable for radio-over-fiber applications," *in Proceedings of The 9th International Conference on Group IV Photonics (GFP)* (2012), pp. 57–59.
21. F. Y. Gardes, A. Brimont, P. Sanchis, G. Rasigade, D. Marris-Morini, L. O'Faolain, F. Dong, J.-M. Fédéli, P. Dumon, L. Vivien, T. F. Krauss, G. T. Reed, and J. Martí, "High-speed modulation of a compact silicon ring resonator based on a reverse-biased pn diode," Opt. Express **17**(24), 21986–21991 (2009).
22. M. Ziebell, D. Marris-Morini, G. Rasigade, P. Crozat, J.-M. Fédéli, P. Grosse, E. Cassan, and L. Vivien, "Ten Gbit/s ring resonator silicon modulator based on interdigitated PN junctions," Opt. Express **19**(15), 14690–14695 (2011).
23. K. Debnath, L. O'Faolain, F. Y. Gardes, A. G. Steffan, G. T. Reed, and T. F. Krauss, "Cascaded modulator architecture for WDM applications," Opt. Express **20**(25), 27420–27428 (2012).
24. W. Franz, "Einfluß eines elektrischen feldes auf eine optische Absorptionskante," Zeitschrift Naturforschung Teil A **13**, 484–489 (1958).
25. L. V. Keldysh, "Behavior of non-metallic crystals in strong electric fields," Soviet J. Experimental Theoretical Phys. **6**, 763 (1958).
26. C. G. Littlejohns, A. Z. Khokhar, D. J. Thomson, Y. Hu, L. Basset, S. A. Reynolds, G. Z. Mashanovich, G. T. Reed, and F. Y. Gardes, "Ge-on-Si plasma-enhanced chemical vapor deposition for low-cost photodetectors," IEEE Photonics J. **7**(4), 1–8 (2015).
27. C. G. Littlejohns, M. Nedeljkovic, C. F. Mallinson, J. F. Watts, G. Z. Mashanovich, G. T. Reed, and F. Y. Gardes, "Next generation device grade silicon-germanium on insulator," Sci. Rep. **5**(1), 8288 (2015).
28. L. Mastronardi, M. Banakar, A. Z. Khokhar, T. Domínguez Bucio, C. G. Littlejohns, N. Bernier, E. Robin, J.-R. Rouviere, H. Dansas, N. Gambacorti, G. Z. Mashanovich, and F. Y. Gardes, "SiGe bandgap tuning for high speed eam," Trans. 231st ECS Meeting **77**(6), 59–63 (2017).
29. G. P. Agrawal, *Lightwave Technology: Components and Devices* (Wiley, 2004).
30. J. F. Lampin, L. Desplanque, and F. Mollot, "Detection of picosecond electrical pulses using the intrinsic Franz-Keldysh effect," Appl. Phys. Lett. **78**(26), 4103–4105 (2001).
31. J. Liu, *Gesi Photodetectors and Electro-Absorption Modulators for Si Electronic-Photonic Integrated Circuits* (Massachusetts Institute of Technology, 2007).
32. D. Feng, W. Qian, H. Liang, C. C. Kung, Z. Zhou, Z. Li, J. S. Levy, R. Shafiiha, J. Fong, B. Jonathan Luff, and M. Asghari, "High-speed GeSi electroabsorption modulator on the SOI waveguide platform," IEEE J. Sel. Top. Quantum Electron. **19**(6), 64–73 (2013).
33. S. A. Srinivasan, M. Pantouvaki, S. Gupta, H. T. Chen, P. Verheyen, G. Lepage, G. Roelkens, K. Saraswat, D. V. Thourhout, P. Absil, and J. V. Campenhout, "56 Gbps germanium waveguide electro-absorption modulator," J. Lightwave Technol. **34**(2), 419–424 (2016).
34. K. Nozaki, A. Shakoor, S. Matsuo, T. Fujii, K. Takeda, A. Shinya, E. Kuramochi, and M. Notomi, "Ultralow-energy electro-absorption modulator consisting of InGaAsP-embedded photonic-crystal waveguide," APL Photonics **2**(5), 056105 (2017).

1. Introduction

It has been shown [1] that the Annual Global IP traffic is expected to exceed a zettabyte (1 trillion gigabytes) in 2017 and then double by 2019. An integrated photonic system based on CMOS based silicon photonics circuitry is considered to be a key enabling technology for highly integrated optical interconnects providing a means to cope with the rising data rate

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requirements and associated costs. Over the last two decades, research efforts have been pursued to develop integrated silicon and multilayer based systems [2–6] including high speed photodetectors [7–10], wavelength division multiplexing (WDM) filters [11,12] and modulators [13–15]. Often the modulator is seen as the workhorse at the heart of an optical transmission link. In group IV based materials, especially silicon, the free carrier dispersion effect is the most commonly used physical mechanism to enable phase modulation. Amplitude modulation is therefore obtained with interferometric devices such as Mach-Zehnder Interferometers (MZI) [16–18]. Nowadays MZI-based device [19,20] are reaching maturity in terms of fabrication stability and performance nevertheless a common and inevitable issue of this class of modulators is the intrinsic footprint that remains on the order of mm^2, leading to power consumption levels of the order of the ~pJ/bit. The power consumption can be reduced dramatically using resonant devices such as ring resonators [21,22] or photonic crystals [23], but the advantages have to be mitigated by issues linked to fabrication and temperature tolerance as well as reduced operational optical bandwidth. To alleviate some of these issues whilst increasing bandwidth density, low power consumption, optical bandwidth and switching speed; Ge and/or GeSi electro absorption modulators (EAM) based on the Franz-Keldysh (FK) [24,25] effect can be envisioned.

Progress in GeSi deposition onto Si [26,27] makes these alloys suitable, in particular, for large scale integration and pushes further the limits of modern telecommunication systems. In a recent work, we have also demonstrated [28] the possibility of fine wavelength tuning over 40 nm by means of rapid thermal annealing, enabling the possibility of tunability of modulators arrays working at specific wavelengths. Therefore, covering some of the requirements for WDM in telecommunication [29] whilst providing a platform enabling channel number scalability.

In this paper, we present an innovative Si/GeSi hetero-structure modulator developed on an 800 nm thick Silicon-On-Insulator platform. The device, is formed by a wrap-around PIN hetero junction in a rib waveguide with dimensions of 1.5 µm x 40 µm. The advantage of the structure is provided by the wrap-around diode structure enabling a better control of the junction width whilst alleviating the constraint linked to the width of the waveguide. The coupling scheme chosen between the SiGe waveguide and the Si waveguide grants self-alignment of the waveguide between the two materials simplifying the fabrication process. The customizable device structure and simple manufacturing process also allow high speed performance and large manufacturing tolerances.

The device eye is measured at a data rate of 56.2 Gb/s and shows a dynamic ER of 5.2 dB and modulator power of 44 fJ/bit. The 3 dB bandwidth of 56 GHz demonstrates a leading capability of this design for high speed applications.

2. Modulator design

The fabricated modulator is based on the FK effect, where an applied electric field modifies the optical properties of direct bandgap semiconductors by increasing the absorption of photon with energies near the material bandgap. The absorption change is reached in less than a picosecond [30] allowing fabrication of amplitude modulators where data rate can exceed 50 Gb/s.

A wrap-around PIN Si/GeSi hetero-structure is chosen for the modulator and implemented in an 800 nm platform. The heterostructure design in Fig. 1 shows the diode configuration integrated in a 1.5 µm wide rib waveguide, where the P doping is defined in a 100 nm thick silicon layer (light green), the intrinsic region (total thickness of 600 nm) is defined by a bottom Ge seed layer (black) and a GeSi area (gold) where the N doping (thickness ~100 nm) follows the contour of the top of the rib waveguide (orange/red area). Compared to previous works, this solution is advantageous because the waveguide width does not interfere or limit the strength of the electric field distribution and can also be tailored to improve, if required, the propagation of both polarizations and optical confinement of the optical mode.

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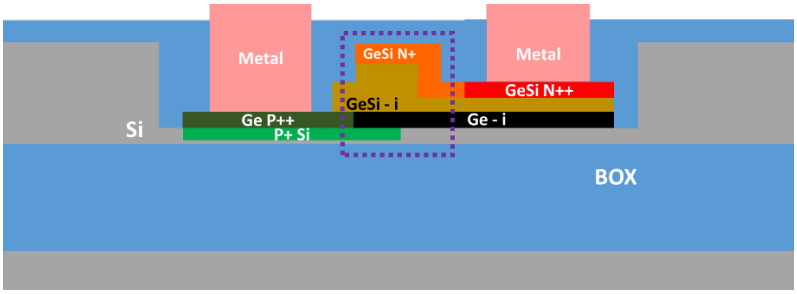

Fig. 1. Device cross-section schematics.

Electro-optical simulations, using Silvaco and Matlab tools, were carried out to engineer the cross-section parameters such as the rib waveguide dimensions, the doping profiles and levels for maximizing the electric field and series resistance. The optical model for GeSi is based on the pioneering work from Liu et al. [31] to exploit the FK effect and find the best trade-off between optical loss and device speed. Indeed, whilst high doping levels can lead to low resistance, making the device potentially very fast, they can also induce strong optical losses. On the other hand, low doping level reducing the optical loss at the cost of higher resistance is not suitable for high-speed operation purposes. The engineering of the doping profile is, also, of critical importance as N+/P + doping species diffusing in the intrinsic region increase the optical loss.

In Fig. 2(a) the TE mode distribution from the optical simulation is overlaid with the electric field distribution at –2 V, in the area delimited by the dashed line of Fig. 1. However, for an applied voltage of 2 volts, the electric field remains strong (~40 kV/cm) in the core of the rib waveguide, ensuring a good electro-optical overlap. In Fig. 2(b), a horizontal cut of the electric field distribution along the dashed line of Fig. 2(a) is compared to electric field distributions found in [32,33]. We can take note that, unlike our wrap-around geometry, these demonstrations are based on lateral pin implantations that inherently limit the width of the waveguide as a larger width is likely to decrease the field strength over the optical mode.

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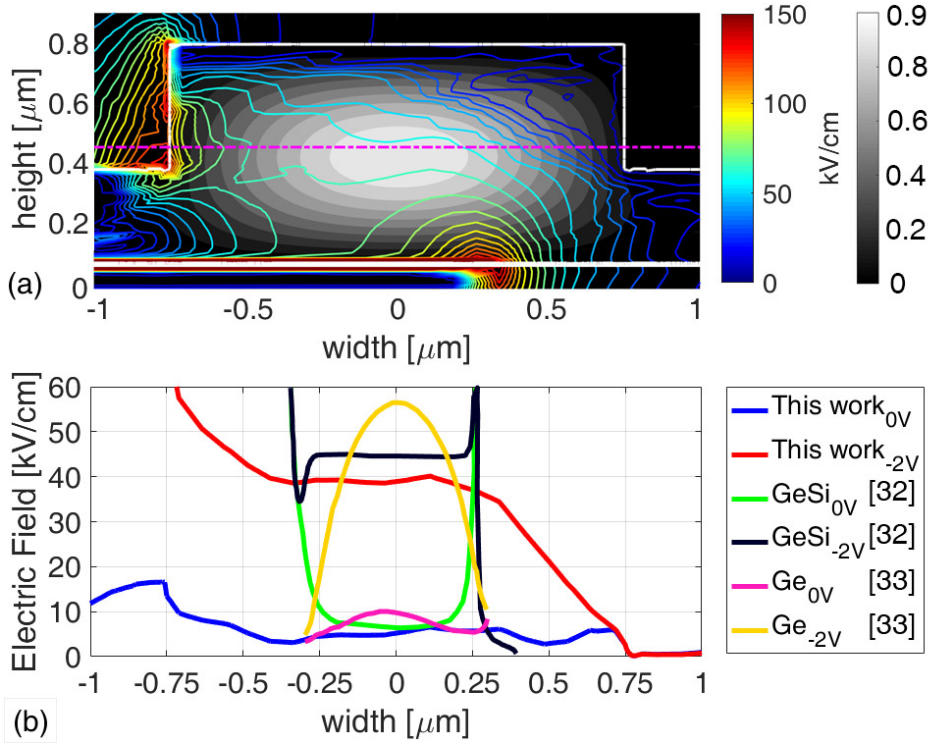

Fig. 2. (a) Overlay of the TE mode distribution (grey contour) and the electric field distribution (coloured contour) at –2 V. (b), the extrapolated electric field along the dashed line compared with different works [32,33].

For this reason, the fabrication tolerances and the effect of the waveguide width on the electric field is lowered dramatically. Another aspect of this concept is the possibility to tune the polarisation sensitivity of the modulator without affecting the electric field strength. Finally, because Si and GeSi can be dry etched using a single etch step, it is here possible to simplify the fabrication process by defining the SOI waveguide and the Si/GeSi device at the same time, hence avoiding overlay misalignments. The interface loss between Si and the Si/Ge/GeSi stack for a wider waveguide configuration is estimated to be up to 0.3 dB loss per facet for TE polarisation.

3. Fabrication

The main process steps are shown in Fig. 3. The fabrication is performed on an 800 nm thick Silicon on insulator wafer with 3 µm buried oxide. Trenches of 50x40 μm^2 are defined by etching the top silicon layer leaving 100 nm of silicon at the bottom of the cavity. Then, the bottom P + doping area is formed using a Boron implant Fig. 3(a) and doped to a concentration of ~10^{18} cm^{-3}.

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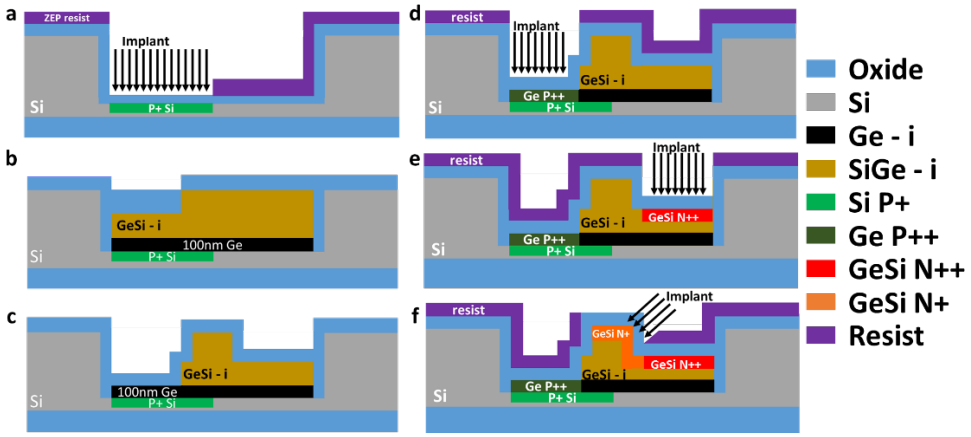

Fig. 3. Fabrication steps of the GeSi EAM heterostructure.

The GeSi layer is selectively grown in the cavity using RPCVD by growing ~100 nm of low temperature Ge buffer layer followed by an overgrowth of GeSi with a Si nominal composition of about 1.5%. The thin Ge layer is used as a low temperature ”seed” for the growth of high quality GeSi layer at high temperature. The GeSi layer is then overgrown to make sure the cavities are filled with the compound material over the whole wafer. The wafer is then put through Chemical mechanical polishing (CMP) to planarize the GeSi structures and remove the excess of GeSi above the Si layer.

The wrap-around PIN rib junction is then formed by a two-step etch. First, only the left hand side of the cavity is etched by about 200 nm Fig. 3(b), then another 400 nm etching is performed for defining the waveguide rib and the coupling gratings Fig. 3(c). For optical normalisation purposes, a silicon waveguide with identical length is etched next to every device. On the left hand side of the rib, the total etch depth of the trench is 600 nm, ensuring the highly doped P + + layer could be defined across the whole 100 nm Ge buffer layer. On the right hand side of the rib, the 400 nm etch depth ensures the formation of the rib waveguide. Once the rib doping regions have been defined, high dose ion implantation steps are performed, P + + using BF2 on the left side in the germanium recess Fig. 3(d) and N + + (Phosphorus) on the right hand side, in the GeSi slab Fig. 3(e). The target doping concentrations are ~10^{20} cm^{-3} and ~10^{19} cm^{-3}, respectively. The last implantation step Fig. 3(f) is performed at 45° to define the wrap-around junction formed by the N + phosphorus doped surface layer with a concentration target of ~10^{18} cm^{-3}. Finally, RTA activation at 650 °C, oxide deposition, VIAS definition and metal deposition/etch conclude the fabrication run. A FIB cross section, highlighting the two-step etch result, and metallisation is shown in Fig. 4.

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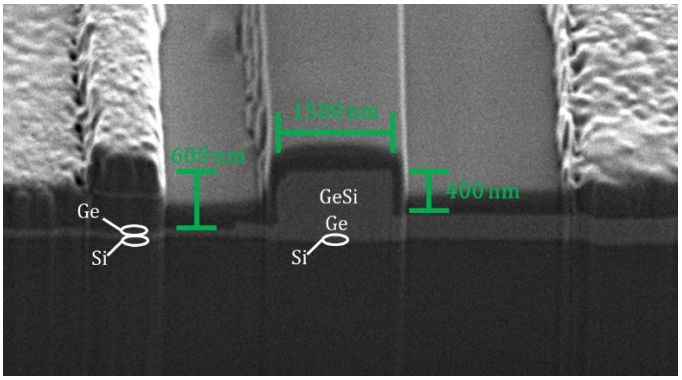

Fig. 4. FIB cross-section of the fabricated device.

4. DC measurements

The performances of our device are first measured in DC using the setup illustrated in Fig. 5. Each device is electrically probed using tungsten tip DC probes from Cascade Microtech. A Matlab routine allows to measure the optical and electrical behaviours of the EAM independently.

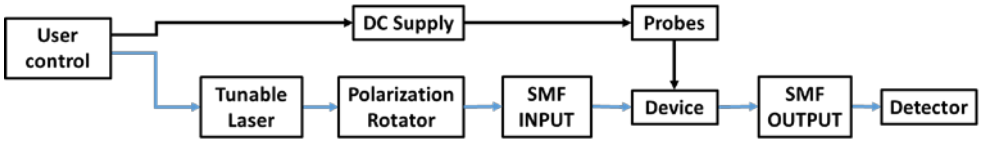

Fig. 5. DC opto-electric setup diagram.

The major contributions to the dark current are estimated to originate from surface current and crystal defects and to increase the static power consumption. For this device, the dark current level is measured to be below 1 µA at a reverse bias of 2 V, further reduction of the leakage current could be achieved by improving the epitaxial seed layer and the surface passivation step.

Optical transmission spectra are then measured in DC in order to determine the modulator performances which, in EAM, are a compromise between loss without electric field (IL) and absorption variation for a given voltage swing (ER). In Fig. 6(a), the Insertion Loss (IL) and the Extinction Ratio (ER) for different applied voltages are depicted, respectively. For the proposed structure, the IL is due to the Ge direct bandgap and GeSi indirect bandgap absorption and extra loss linked to the built-in electric field, coupled to doping loss and waveguide loss. The simulated loss at the interface between the Si and GeSi waveguide is removed. It is important to point out that the total insertion loss is increased by the presence of the underlying Ge layer that is intrinsic to the adopted process rather than the design and introduces a second ER peak for wavelengths above 1570 nm. Therefore, it is expected that an improved epitaxial growth recipe would improve dramatically the IL.

The ER spectrum reaches a maximum peak of 3 dB for a reverse bias of 1 V at 1540 nm. For higher reverse biases, the ER increases up to 7.5 dB (bias = –4 V); this translate to a calculated incremental ER rate of about 1.5 dB/V around 1540-1545 nm.

To assess the EAM performance across the C and part of the L band, we define the FOM = ER/IL as the ratio between the losses with and without reverse bias. The FOM, depicted in Fig. 6(b), is a good indicator of the trade-off between extinction ratio and insertion losses for a voltage swing from –1 V to –4 V. It is clear that the FOM is affected by the IL of the device nevertheless the modulated ER between –1 and –4 volts stays constant across the whole C band and part of the L band enabling the FOM to reach a value of 1 at 1590 nm.

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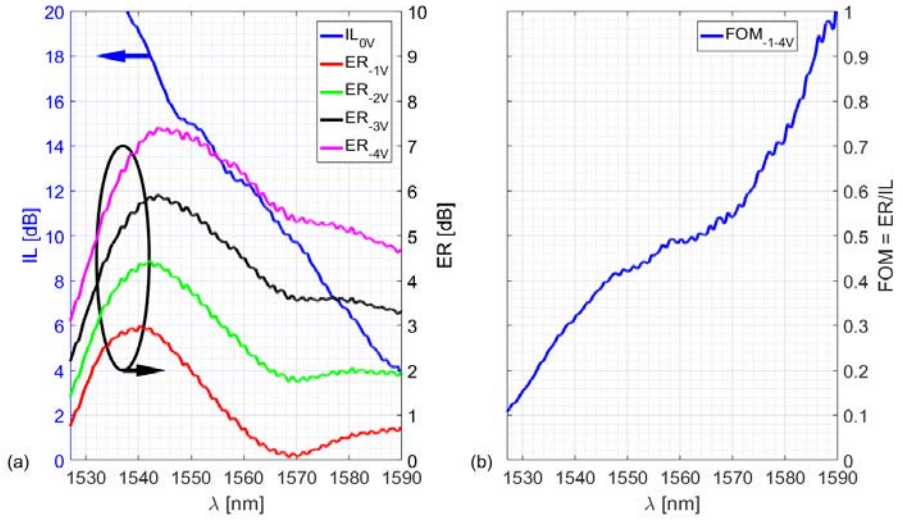

Fig. 6. (a) Measured Insertion Loss and Extinction Ratio for different reverse biases, (b) ER, IL ratio for the selected high speed modulation voltage swing.

5. High-Speed measurements

The high-speed measurements setup includes a 56 Gbps pseudorandom binary sequence (PRBS) generator coupled to an RF amplifier where the signal is attenuated (using in line RF attenuators) to the require swing voltage. A bias T sets the reverse voltage and the signal is fed to GS probes, which are not 50 ohms terminated. A low noise EDFA coupled to a bandpass filter is also used to amplify the modulated optical signal to the DCA, the fixed wavelength optical signal is generated by an Agilent tunable laser coupled to the EAM using grating couplers. The overall diagram of the setup is shown in Fig. 7.

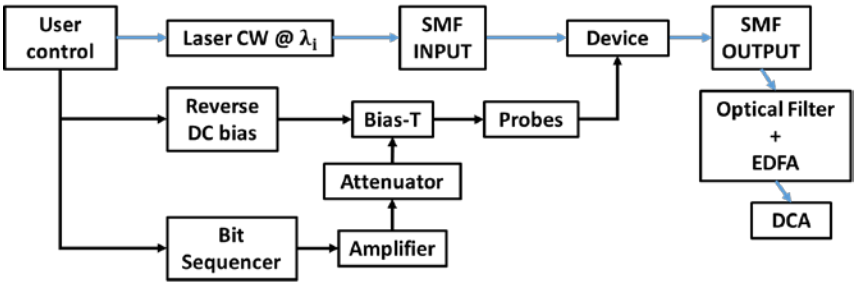

Fig. 7. High-speed opto-electric setup diagram.

The RF signal has a voltage swing of 2.2 V peak-to-peak or ~2.7 V rail-to-rail while the DC reverse bias is 2.7 V. Figure 8 shows the input electrical eye diagram and Fig. 9 shows the measured optical eye diagram from the device operating at 1566 nm. This wavelength is chosen to obtain the best trade-off between the FOM and the optical measurement limitation of our setup. The observed open eye has a dynamic ER of 5.2 dB at a speed of 56.2 Gbps. In this case the data rate is limited by the pattern generator and setup at our disposal. It must be noted that, since the GS probes are not 50 ohms terminated, there is a signal increase of the RF peak to peak voltage applied to the device. The estimated voltage at the device ports, reaches a ~4 V peak-to-peak. The RF reflection is successfully attenuated by a 6dB in-line microwave attenuator. As shown in Figs. 8 and 9 below, the rise time of the optical eye is τ_o = 16.8 ps whilst the rise time of the electrical input eye is τ_e = 15.6 ps. The device rise time can be defined by:

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$$\tau_r = \sqrt{(\tau_o^2 - \tau_e^2)}. \quad (1)$$

From Eq. (1), we calculate τ_r for the available readings (Table 1), which indicates an analogue EO modulation bandwidth ranging from 42 GHz up to 66 GHz, with a current value of 56 GHz.

Table 1. EAM time rise measurement and EO bandwidth calculation.

Eye reading	τ_e (ps)	τ_o (ps)	τ_r (ps)	EO bandwidth (GHz)
current	15.60	16.80	6.24	56
min	14.56	16.80	8.38	42
max	15.95	16.80	5.28	66

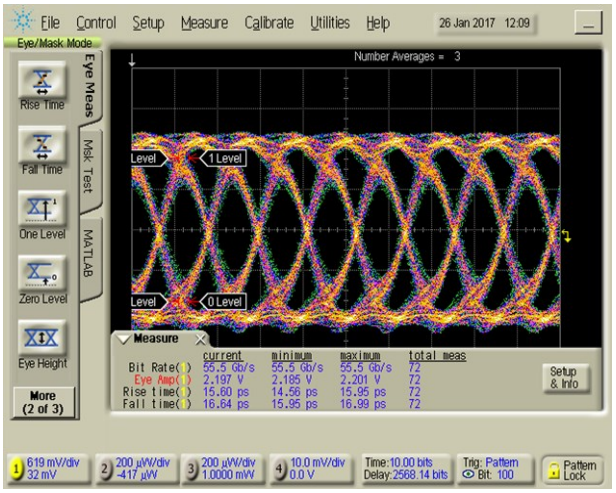

Fig. 8. 56 Gbps input electrical eye of 2.2Vpp.

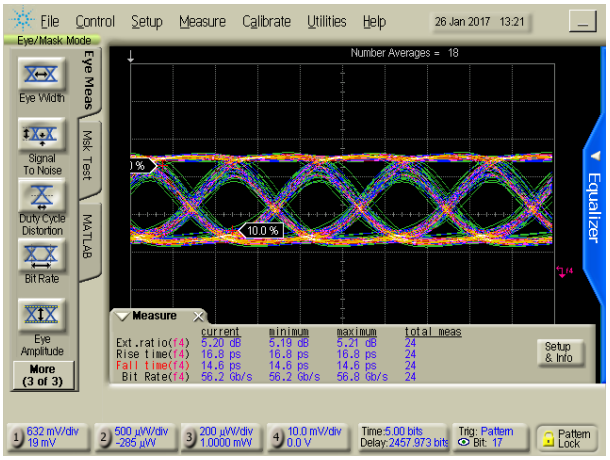

Fig. 9. Measured 56.2 Gb/s device eye diagram with an ER of 5.2 dB.

Measuring the S11 and parameters, the EAM electrical equivalent circuit (Fig. 10) is modelled.

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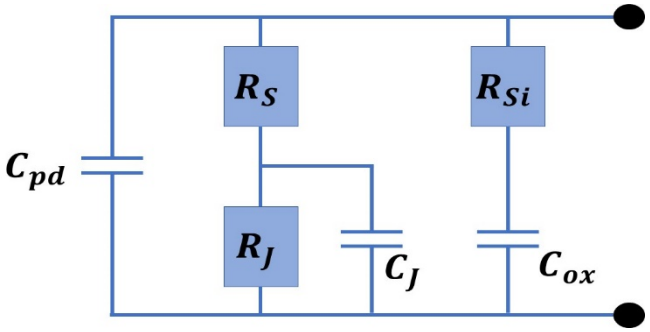

Fig. 10. Equivalent electric circuit.

The equivalent electrical circuit consists of the pad capacitance C_{pd}, the series resistance R_S, the p-i-n junction resistance R_J, the p-i-n junction capacitance C_J, the capacitance due to the BOX layer C_{ox}, and the resistance due to the SOI and substrate R_{Si}. Using the S-parameters model available in Agilent Advance Design System, we found the lumped element values of the equivalent electrical circuit to match the experimental data, as shown in Fig. 11. We calculated C_{pd} = 5 fF, R_S = 150 Ω, R_J = 1500 Ω, C_J = 11 fF, C_{ox} = 30 fF and R_{Si} = 350 Ω. We can, then, calculate the power of the EAM at 56 Gbps to be $C_J Vpp^2/4 = 44$ fJ/bit with the swing voltage Vpp = 4 V (taking into account the signal increase due to GS probe without termination).

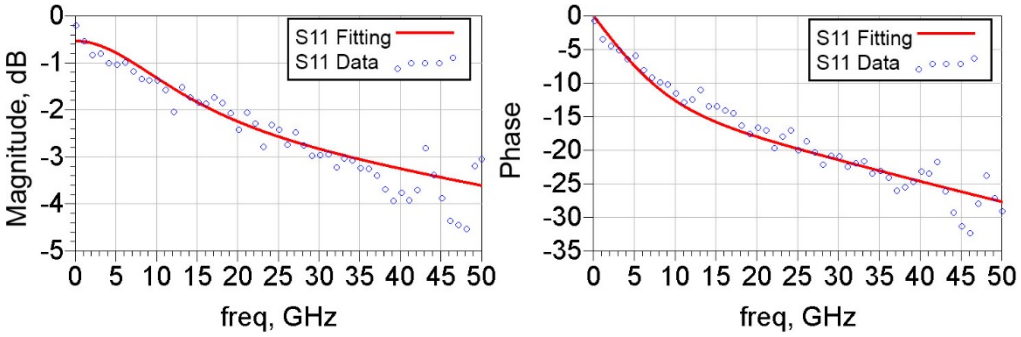

Fig. 11. S11 Parameter at –3 V.

In Table 2 our device is compared to devices found in the literature [32–34]. The first iteration of the Si/Ge/GeSi heterostructure device demonstrated here, is a transitional device that is currently affected by epitaxy constraints and the extra insertion losses generated by the Ge seeding layer. Future work will therefore focus on either direct GeSi-on-Si growth or Si diffusion into Ge to achieve a uniform GeSi layer throughout the entire cavity with an aim to reduce the IL. Nevertheless, the compact footprint, the low energy per bit, and the high bit-rate demonstrate the capability of this design. Furthermore, we believe that the proposed design provides important advantages such as simpler, and more tolerant fabrication due to the possibility to fabricate a diode in a wider GeSi waveguide with a simple self-alignment of the GeSi waveguide to the Si waveguide. The concept also provides a better control of the junction width due to the low dependence on implantation depth enabled by the wrap-around doping profile whilst the opposite doping type (n-type) is being contained within the bottom silicon layer.

Table 2. EAM in literature compared to our device.

Ref.	λ (nm)	Area (μm²)	Voltage swing (V)	3dB Band (GHz)	Energy/bit (fJ/bit)	IL DC (dB)	Dynamic ER (dB)

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GeSi EAM [32]	1550	0.8x50	3	38	147	4.8	4.5
Ge EAM [33]	1610	40x0.6	2	>50	12.8	4.9	3.29
PhC EAM [34]	1530	70x0.4	1	28.3	2.2	3	3
This work	1566	40x1.5	~4	56	44	10.6	5.2

6. Conclusion

We have designed, fabricated and characterized a high-speed GeSi EAM developed on an 800 nm SOI platform, built in a 1.5 μm wide rib waveguide. Operating at a wavelength of 1566 nm, we have demonstrated a data rate, limited by the measurement setup, of 56.2 Gb/s, with a dynamic ER of 5.2 dB. With a small device footprint of 60 μm^2, the modulator power consumption and EO modulation bandwidth have been calculated to be 44 fJ/bit and 56 GHz, respectively. The wrap-around junction design enables, a simple, tolerant, and customizable fabrication process for high-speed and compact electro absorption modulators. Finally, the high EO modulation bandwidth and bandwidth density (~1 $Pbit/s/mm^2$) demonstrated by this device, coupled with the ability to vary the waveguide width without sacrificing the electric distribution, should ensure this concept to be one of the leading candidates for the next generation highly integrated WDM based telecommunication systems.

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