Resistive memories using Cu nanoparticles embedded amorphous SiC

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Resistive memories (RMs) have simple Metal/Insulator/Metal structures and are considered as outstanding candidates for future non-volatile memory applications [1]. The write and erase of RMs are based on the formation and rupture of conductive filament (CF) in the insulating medium, induced by applying a programming voltage on the device. The formation and rupture of CF switch the device between high resistance state (HRS) and low resistance state (LRS), defined as OFF and ON, respectively. Material properties of the insulating layer are directly linked to the filament formation and rupture and thus device performance. Among many materials exploited for RMs, amorphous SiC (a-SiC) based RMs have shown great promise [2, 3] with ultra-high ON/OFF ratio. However, relatively large forming voltages were required to achieve the first LRS for a pristine device [3] due to slow diffusion of Cu in a-SiC matrix [2]. In this study, Cu nanoparticles (NPs) embedded a-SiC (a-SiC:Cu) is exploited as the insulating layer for Cu/a-SiC:Cu/Au RMs. Key resistive switching performance of the Cu/a-SiC:Cu/Au RMs is investigated.

Cu/a-SiC:Cu/Au RMs with 50µm x 50µm device area were fabricated using similar microfabrication procedures descripted in [2]. The middle a-SiC:Cu films were deposited using co-sputtering from SiC (99.5%) and Cu (99.99%) targets in a Kurt J. Lesker sputter system. The Cu vol% in the deposited films was achieved by adjusting the target powers. 40nm thick a-SiC:Cu films with 0%, 20% and 30% Cu vol% were subsequently used to form Cu/a-SiC:Cu/Au RMs, respectively. Current-Voltage (I-V) measurements were conducted by grounding the Au electrode and applying a voltage to the Cu electrode, using a Keithley 4200SCS. 100µA current compliance was used for FORM and SET. 0.02V/0.5Sec ramping rate was used in DC measurements. In pulse measurements, pulse sweep composited by 90mSec pulses with a 0.02V/100mSec ramping rate was used for SET. Single 10mSec -3V pulse was used for RESET. DC read at 0.1V was used between SET and RESET.

Figure 1 shows the cross-sectional SEM image of a Cu/a-SiC:Cu/Au RM and the inset shows a typical TEM image of a Cu NPs embedded a-SiC, indicating well dispersed Cu NPs with a few nm diameters were achieved in the film. A number of devices have been measured and Figure 2 shows that the FORM voltage reduces clearly with Cu vol% in the a-SiC:Cu layers. It has been reported that the existence of metal particles in dielectric film increases the electric field in the direction of thickness [4]. The reduce of FORM voltage is likely attributed to the increase of electric field in the a-SiC:Cu along the direction of thickness which is also the forming direction of CF. It is also likely that the forming routine of CF passes through the location of co-sputtered Cu NPs, since the electric field is higher adjacent to the Cu NPs. This could reduce the effective length of CF percolation during the FORM process hence reducing the FORM voltage.

All RMs with device areas of 50µm x 50µm presented Bipolar resistive switching characteristics, as shown in Figure 3. LRS values at 0.1V are 76Ohm, 157Ohm, 247Ohm for devices with 0%, 20%, and 30% Cu vol% respectively, while HRS values at 0.1V are 630MOhm, 2.8GOhm, 3.9GOhm for devices with 0%, 20%, and 30% Cu vol%, respectively. This corresponds to high ON/OFF ratio of ~10^7. Detailed studies of these I-V switching characteristics suggest that all the devices have Ohmic conduction in LRS which implies conduction of metal filament at LRS; while Schottky conduction mechanism dominates HRS. Schottky barrier heights (SBHs) (~0.8eV) of HRS are much lower than that of pristine devices (~0.9-1 eV). The reduction of SBHs in devices is likely due to the existence of residual CF [5] at HRS. Pulsed measurements were also conducted to study the endurance of the device with 30% Cu vol% as a typical result shown in Figure 4. It is observed that, even with incorporation of 30% Cu NPs in a-SiC:Cu, the corresponding RM still demonstrated high ON/OFF ratio (~10^6) after multiple cycles. Excellent retention properties of the Cu/a-SiC:Cu/Au RMs were also obtained by applying constant voltage stress over a period of time. Detailed studies will also be presented.

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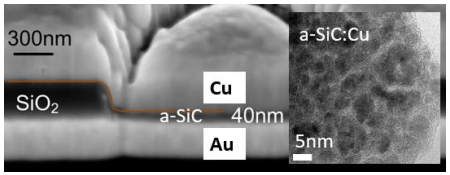

Figure 1. Cross-sectional SEM image of a Cu/a-SiC:Cu/Au RM device. Inset is a TEM image of Cu NPs embedded a-SiC.

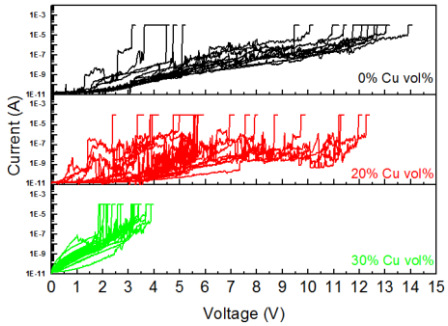

Figure 2Pristine I-V curves for many Cu/a-SiC:Cu/Au devices with 0%, 20%, and 30% Cu vol% showing distribution of FORM voltage.

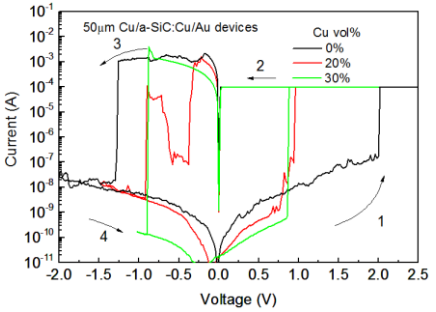

Figure 3. Bipolar resistive switching I-V of Cu/a-SiC:Cu/Au RM devices with 0%, 20%, and 30% Cu vol%.

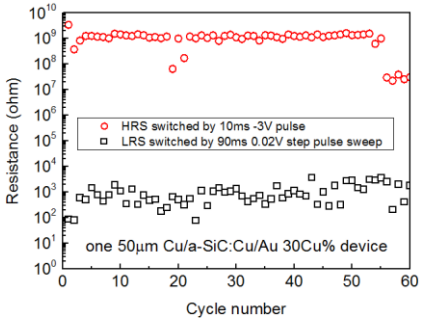

Figure 4. Bipolar endurance cycles of a Cu/a-SiC:Cu/Au device with 30% Cu vol%.