Quantum Dipole in a Silicon Transistor:
Quantum Simulation for Strongly Correlated System

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Abstract: We discovered anomalous transport properties in a conventional Si based Metal-Oxide-Semiconductor Field-Effect-Transistor with a wide and narrow hole-channel at low temperatures. We found the quantum dipole formed at the thin gate interface is responsible for the phase transition. We discuss its potential to use for a quantum simulator as a test bed to examine various theoretical concepts in condensed-matter physics.

1. Introduction

Strongly correlated electronic systems are well-known to exhibit various exotic behaviors such as spin-charge separation in Tomonaga-Luttinger Liquid (TLL) [1], quantum magnetization with Haldane gap [2,3], and high-T_c superconductivity. Grand challenge is to compare theories with experiments due to difficulties to solve theoretical models without prejudiced approximations. Quantum simulator will be a powerful tool to investigate these systems. In order to fabricate a quantum simulator, we need to prepare a quantum *pseudo* spin, which can point arbitrary directions to use the superposition principle to accelerate the convergence by quantum annealing [4].

Here, we demonstrate a quantum dipole formed at the MOS interface is useful to use as a *pseudo* half-spin. We discuss transport properties governed by these dipoles.

2. Device Structure and Operation Principle

We fabricated a *p*-MOSFET with a channel length (*L*) of 55nm and a width (*W*) of 10um (Fig. 1). The gate insulator was made of silicon-oxynitride (SiON) with a thickness of 2.4nm, and the poly-crystalline Si gate electrode was used. We think that the quantum dipole was made at this thin interface (Fig. 1). Holes will be confined at the source edge of the channel after the pinch-off, while no electric field was applied along the long axis of the channel. Therefore, the one-dimensional (*1D*) channel was formed at the source edge, and the system can be described by the Heisenberg XXZ model with strong transverse electric field as,

$$H = \sum_{\langle ij \rangle} J_{ij}^{xy}(P_i^x P_j^x + P_i^y P_j^y) + \sum_{\langle ij \rangle} J_{ij}^z P_i^z P_j^z - E_y \sum_i P_i^y - E_z \sum_i P_i^z,$$

where Pi is the dipole moment, which satisfies the spin-half commutation relationships. J^{xy} and J^z are exchange couplings along the plane and perpendicular to the plane, respectively.
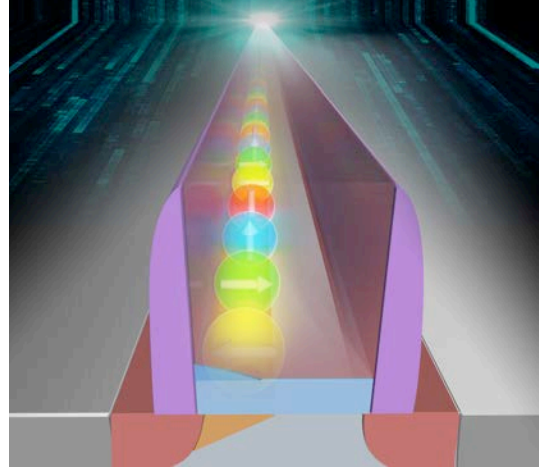

Fig. 1 Quantum dipole system formed at the source edge of the Si MOSFET.

3. Results and Discussions

Figs. 2 and 3 show typical transport characteristics of our device. Transport properties are normal at the low drain voltage, showing ballistic transport properties at low temperatures (Fig. 2). However, we found clear kinks at higher drain voltages, where the channel would be pinched-off (Figs. 2 and 3). There are 3 distinctive regimes: (i) At lower gate voltages, the carrier
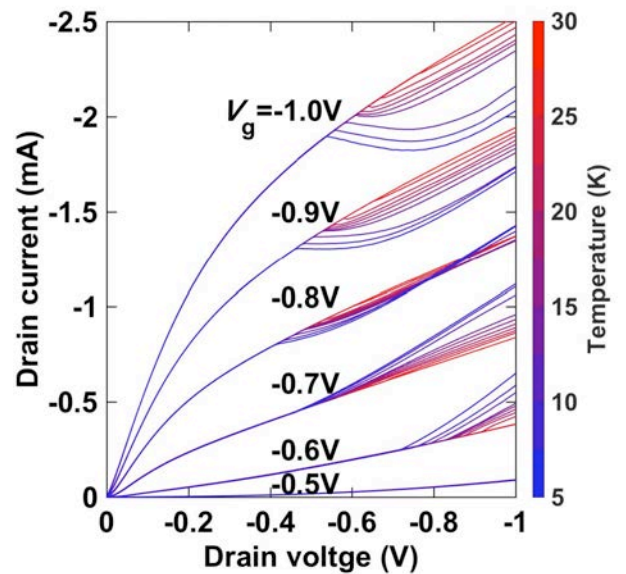

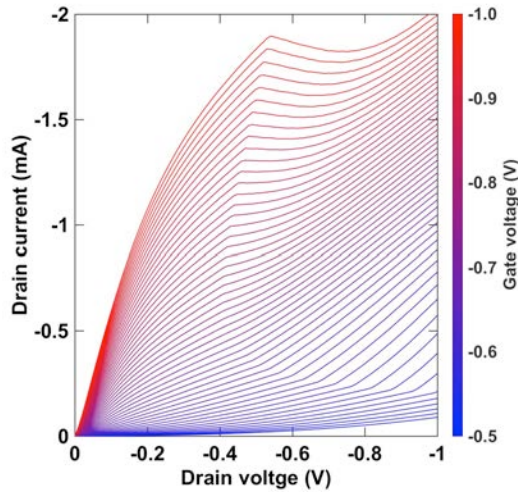*Fig. 2 Field-induced phase transition upon temperatures.*

Fig. 3 Impact of gate induced carrier doping on quantum dipoles.

concentration is low, and the dipole can align to the direction to the drain, and the current steeply increased with the help of the molecular field. We have assigned this state as a Ferroelectric state of the dipole. (ii) At higher gate voltages, we found the negative differential conductance and current decreased upon increasing the drain voltage (Fig. 3). The current would be reduced due to the alignments of dipoles. We have assigned this state as a AntiFerroelectric state of the dipole. (iii) At moderate carrier concentration, we found a new current plateau, where the current persists to keep a constant value regardless of the substantial change in the drain voltages (Fig. 3). We think this phenomenon was correlated with the theoretical prediction of the Haldane gap in spin-half systems, which will result in magnetization plateaus upon increasing magnetic fields [3]. Therefore, the local singlets would be formed to screen the electric field.

We obtained phase diagrams (Figs. 4 and 5) by making contour plots of drain transconductance. We have found clear boundary between classical and quantum
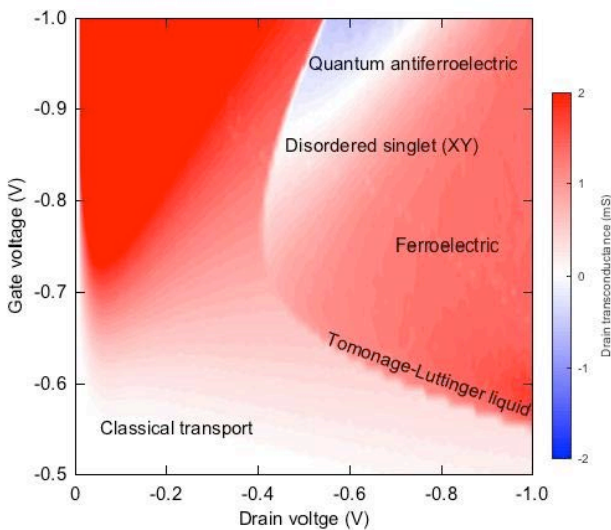

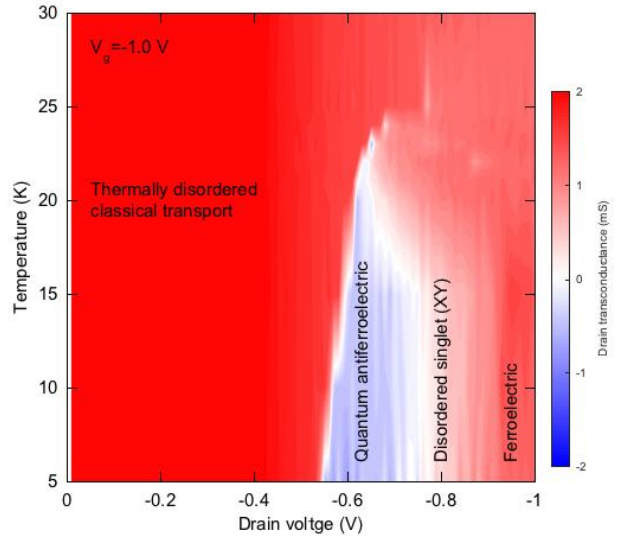*Fig. 4 Phase diagram upon changing electric fields.*

Fig. 5 Phase diagram on quantum dipole system.

transport regimes at 5K (Fig. 4). According to the prediction of the renormalization flow, the TLL behaviors are expected at the lower boundary between classical and quantum transports.

We also made a phase diagram upon changing temperatures and carrier doping concentrations (Fig. 5). To our surprise, the obtained phase diagram is resembled with the phase diagram of high-T_c superconducting cuprates [6]. This implies our device is already working as a quantum simulator to help understanding the mechanism of high-T_c cuprates. In particular, it addresses the long-thought mysteries of the origin of the pseudo gap [6]. According to our *quantum simulation*, the pseudo gap phase is equivalent to the magnetization plateaus, whose existence was rigorously proved theoretically in 1D XXZ model [3].

4. Conclusions

In this paper, we discussed our recent anomalous transport properties found in a conventional Si transistor at low temperatures based on a quantum dipole model. Our results suggest the advanced Si technologies are useful for making a quantum simulator to verify various theoretical concepts and tackle difficult problems, which were impossible to solve by using classical computers.

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