Advanced Layout Techniques for High-speed Analogue Circuits in a 28nm HKMG CMOS Process

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This paper investigates the effect of optimizing the transistor finger width on the performance of high-speed analogue circuits in deep sub-micron processes, demonstrated in a 28nm High-K/Metal Gate (HKMG) CMOS technology process. Silicon proven results demonstrate that the oscillator with a finger width of 440nm gives the best performance based on the Figure of Merit (=142) among the benchmark design examples used.

Introduction: In high-speed analogue integrated circuit (IC) design, the transistor dimensions have a direct impact on the circuit's overall performance. As has been discussed in recent works [1,2], prudent layout of each transistors is critical essential for ultra-small process nodes(<40nm). A reduction of standalone single transistor's width on improving analogue performance in the HKMG process has been presented in [2]. However, the situation starts to become more complex when the individual transistors are placed in the context of an analogue circuit. One of the key issues in ultra-small process nodes is that unlike the standard design process for the basic transistor dimensions, the selection of the individual finger width (*Wf*) of the transistor and the number of fingers is not commonly analysed, other than to carry out typically a common centroid design. Unfortunately, for modern small geometry processes, this specific aspect of the design has emerged as a significant challenge in practical circuit design scenarios, as the individual layout of each transistor becomes much more of a factor in the overall performance. The aim of this paper is to investigate the effects of different finger widths in transistors and the relationship to analogue circuit performance in the 28nm HKMG CMOS process.

Circuit Details: An inverter-based high speed oscillator structure (Fig. 1) was selected as a suitable practical test-bench circuit as it has clear performance metrics. The circuit was used to evaluate the optimal finger width to obtain the best performance in high-speed applications such as in Silicon-Photonics (SiP) communication systems. An oscillator topology with three delay stages was implemented to satisfy the Barkhausen's criteria for oscillation [3]. In addition, two stages of self-biasing common source amplifiers follow the oscillator as an output buffer to provide 50Ω impedance matching for testing purposes (This is also consistent with the termination commonly used in Silicon Photonics applications). A DC blocking capacitor was placed between the oscillator and buffer to reset the operation point, and therefore dummy loads were inserted to ensure that each delay stage in the oscillator had a similar load, thereby reducing the influence of unbalanced oscillation in practical measurements.

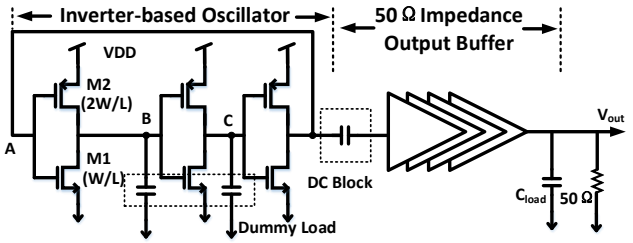

Fig. 1 Implemented Inverter-based Oscillator Example Structure with 50Ω Impedance Output Buffer

In the basic layout implementation, at least one contact via has to be placed at both the drain and source terminals, as illustrated in Fig 2 (a). The width of a single via in the process (to satisfy the minimum metal enclosure constraints in the design rules) is 210nm and therefore the minimum finger width of the transistor has to be 220nm with a small margin to account for tolerances as defined in the layout design rules. In order to evaluate the effect of finger width on performance, three different finger widths oscillator example were selected and fabricated in the 28nm HKMG CMOS technology, with the finger widths defined in each benchmark circuit being 220nm (1X Via), 440nm (2X Via) and 880nm (4X Via) with a minimum transistor length of 30nm. In order to ensure that the finger width of the transistor is the most significant factor in the design, all of the NMOS and PMOS elements used in the different oscillator benchmark circuits had the same transistor dimensions.

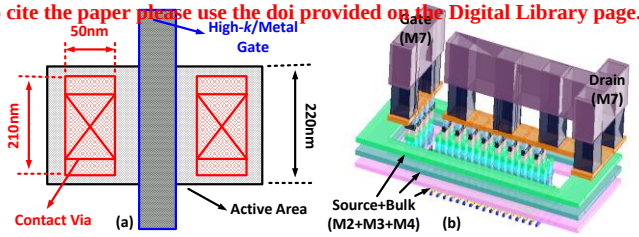

Fig. 2 (a) single transistor with minimum finger width (b) Optimal Transistor Layout with a Finger Width of 440nm

To minimize the impact of variation from the layout design and position of circuits, the three oscillator examples with different finger widths were implemented with the same basic layout structure, as presented in [4]. Fig 2 (b) indicates the optimal transistor layout with a finger width of 440nm. The gate of the transistor is contacted at both ends with metal 1(M1), merged and then built up to a thick metal layer (M7). The source of the transistor is connected to both sides of the bulk with three thin metal layers (M2, M3 and M4) to allow sufficient current flow. Moreover, to minimize the interconnect resistance; the drain terminal of the transistor is connected through a thick metal layer (M7).

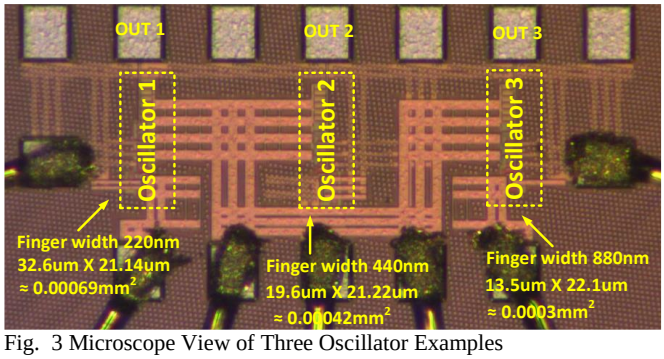

Fig. 3 Microscope View of Three Oscillator Examples

Fig 3 shows micrographs of the three oscillator design examples. The power supply for each oscillator example was provided separately. The fabricated silicon die was then mounted on a standard printed circuit board (PCB) with the DC Pads directly bonded via wire bonds to the PCB. The high-frequency output signal was fed into a spectrum analyser through an RF probe. As the individual finger widths in each oscillator reduced, the number of fingers required is increased which leads to a slight increase in area of each delay cell. This increase in area will lead to a greater parasitic capacitance as the number of fingers increases.

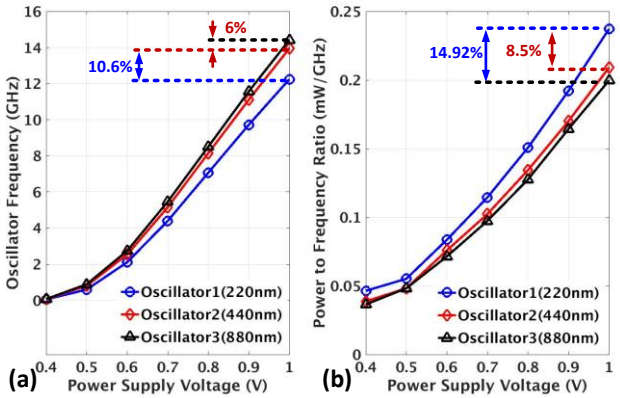

Fig. 4 Measured Results of Three Oscillator Examples (a) Oscillation Frequency (b) Power to Frequency Efficiency

Experimental Results: To investigate the optimal finger width for high-speed analogue applications, three performance aspects were taken into consideration including the oscillation frequency, power efficiency and phase noise (PN). The measurements were conducted at room temperature while the performance of the oscillator examples was monitored while varying the supply voltage from 0.4V to 1V. The three different oscillator examples were measured independently. The testing results presented in this paper were measured from 6 different silicon samples, three of them from wafer 1 and the other three are from wafer 2.

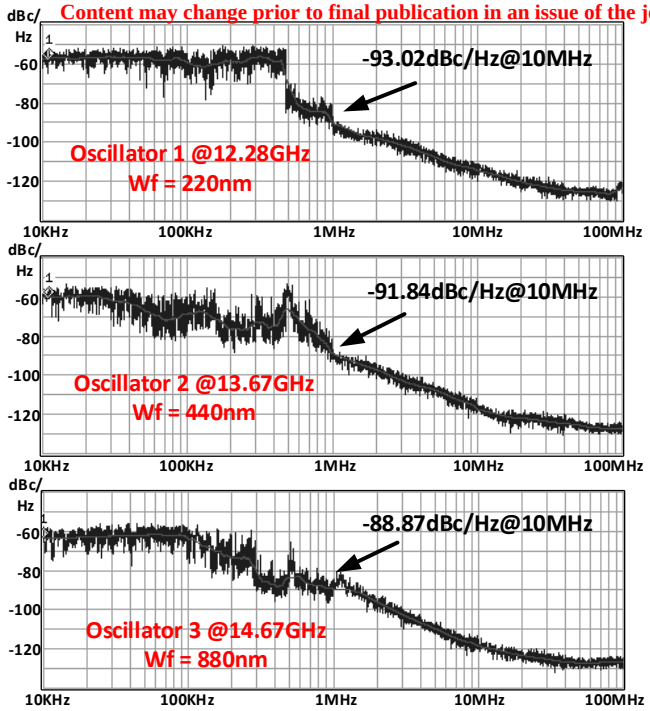

Fig. 5 Measured Phase Noise Results at 10MHz Offset Frequency of Three Oscillator Examples

Fig 4 (a) shows the oscillation frequency of the three different oscillator examples against the power supply voltage. The data presented in this figure is the average of the results from 6 different samples. It can be clearly seen that oscillator 3 provides the highest frequency. While the oscillator 1 has a relatively low frequency output. As noted previously in this paper, the reduction in individual finger width results in an increased layout area which thereby brings about more parasitic capacitance. As consequence, the oscillation frequency is potentially reduced. In the case of oscillators 2 and 3, twice the number of fingers were used in oscillator 2 than in oscillator 3, which in turn caused the layout area to be approximately 17% larger, yet the oscillation frequency of the two oscillators is very close (≈ 6% difference). When comparing oscillators 1 and 2, where the number of fingers was also doubled, there was a larger (33.7%) increase in the layout area and a consequent 10.6% drop in oscillation frequency. Therefore, larger finger width is obviously optimal in providing a high frequency performance while saving cost.

The power efficiency is another important aspect for designers in high-speed analogue applications. In this experiment, since the transistor dimensions of the three oscillator examples are the same overall, theoretically, the current consumed by each oscillator should also be the same. However, by considering the parasitic effects introduced by the layout, both the oscillation frequency and power consumption could dramatically vary from theoretical values. Therefore, instead of comparing the power consumption at different power supply voltages, the amount of energy that is consumed within each oscillation cycle is normalized to the frequency, using equation (1).

$$E_{cycle} = \frac{P_{DC}}{f_{osc}} \quad (1)$$

Fig 4 (b) shows the comparison of power to frequency ratio between the three different oscillator examples. Oscillator 3 consumes less energy within each oscillation cycle over the whole power supply range. The power that is consumed by oscillator 2 is very close to that of oscillator 3. As for oscillator 1, a considerable difference has been observed. The energy that is consumed within each oscillation cycle is about 8.5% and 14.92% higher than for oscillators 2 and 3 respectively. Therefore, in terms of the power to frequency ratio, a larger finger width provides a better power efficiency.

Another important performance metric in an oscillator is the phase noise. To investigate the effect of finger width on the oscillator's noise performance, the PN is measured at the highest oscillation frequency. Fig 5 shows the measured results of phase noise of three oscillator at 10MHz offset frequency. Although oscillator 3 has the highest frequency, the RF noise is worse than the other two oscillators. Equation (2)[5] is used to calculate the spectral density of the channel noise. R_G is total gate distributed resistance and N_{finger} is the number of transistor fingers. The smaller the transistor finger width, the more fingers that are required, therefore, the gate distributed resistance is reduced, which contributes less noise.

$$\overline{V_{n,out}^2} = 4kT\frac{R_G}{N_{finger}}(g_m r_o)^2 \quad (2)$$

As each oscillator example has advantages in different aspects, Figure of Merit (FOM) is used to trade off the advantages of the different finger widths, which the averaged values can be calculated by equation (3)[3].

$$\sum_{i=1}^{6} FOM = \sum_{i=1}^{6}\left(-PN_i(f_{offset}) + 20\log\frac{f_{osc\_i}}{f_{offset}} - 10\log\frac{power\_i}{1mW}\right) \quad (3)$$

The PN results summarized in Table I is the averaged results of 6 test samples. Although oscillator 2 has not obtained the best performance in any of the individual criteria: oscillation frequency, power efficiency or the phase noise, the overall performance (=142) is better than that of oscillators 1 and 3. On the other hand, another trade-off that should be taken into consideration is the area aspect. Larger finger width is easily to provide higher frequency with smaller area. However, this should be decided in association with overall performance.

TABLE I. AVERAGED FOM OF SIX SILICON SAMPLES

Design Examples	**Oscillator 1**	**Oscillator 2**	**Oscillator 3**
Frequency (GHz)	12.3	13.6	14.42
Area (mm^2)	0.0007	0.00042	0.0003
Power (mW)	2.9	2.92	2.88
PN dBc/Hz @10M	-93.47	-92.75	-87.38
Averaged FOM	140.7	142.0	138.4

Conclusion: In this paper, the influence of the transistor's finger width to its analogue performance in high speed applications has been investigated, based on three ring oscillator examples at 28nm HKMG CMOS process. Starting from a fixed circuit topology and transistor dimensions, the width of each finger is decided based upon the number of vias (=1/2/4) in drain/source node. The experimental results indicate that a finger width of 440nm provides the best performance in terms of the figure of merit (142) compared to the finger widths of 220nm (140.7) and 880nm (138.4). Advanced analogue circuit design surely requires careful trade-off among the specifications of bandwidth, power efficiency, noise and layout area. It is hoped the design methodology and measurement results present here can provide an elegant solution to simplify the decision of finger width at layout stage.

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